Computer System Architecture Assignment

1. Perform the arithmetic operations (+42)+(-13) and (-42)-(-13) in binary using signed 2's complement representation for negative numbers.

2. Represent the number $(+46.5)_{10}$ as a floating point binary number with 24 bits. The normalized fraction mantissa has 16 bits and the exponent has 8 bits.

3. Convert the following numbers:

   a. $(45)_6 = (?)_9$
   b. $(ABC)_{16}$= (?) BCD
   c. $(121121)_{2=}(?)_{10}$

4. Simplify the following Boolean functions using four-variable maps
   a) F(A,B,C,D)= $\sum(3,7,11,13,14,15)$
   b) F(A,B,C,D)= $\sum(0,2,4,5,6,7,8,10,13,15)$

5. Show that JK flip flop can be converted to a D flip flop with an inverter between the J and K inputs.
6. What is a flip- flop? Give the drawback of SR flip- flop and how is it removed in JK flip flop.
7. What is the role of FGI and FGO flip flop in basic computer. Explain indexed addressing mode and give advantage.

8. Draw the logic diagram of a 2 to 4 line decoder with only NOR gates. Include an enable input.

9. Simplify the Boolean function f together with the don't care conditions d in (1) S-O-P form (2) P-O-S form. F(w,x,y,z) = £ (0,1,2,3,7,8,10) d(w,x,y,z)=£ (5,6,11,15)

10. The content of PC in the basic computer is 3AF (all numbers are in hexadecimal). The content of AC is 7EC3. The content of memory at address 3AF is 932E. The content of memory at address 32E is 09AC. The content of memory at address 9AC is 8B9F. (Hint 9- ADD indirect opration)
    a) What is the instruction that will be fetched and executed next?
    b) Show the binary operation that will be performed in the AC when the instruction is executed
    c) Give the contents of registers PC, AR, DR, AC and IR in hexadecimal and the values of E, I and the sequence counter SC in binary at the end of the instruction cycle.

11. Construct a16 to 1 line multiplexer with two 8-to-1 line multiplexer and 2-to-1 line multiplexer. Use block diagram for the three multiplexer.
12. Draw the logic diagram of a 2-to-4 line decoder with only NOR gates. Include an enable input.
13. Convert the hexadecimal number F3A7C2 to binary and octal
14. 11010 – 10000 (subtraction using unsigned number)
15. Perform the arithmetic operations (+70) + (+80) and (-70) + (-80) with binary numbers in signed-2's complement representation. Use eight bits to accommodate each number together with its sign. Show that overflow occurs in both cases, that the last two carries are unequal, and that there is a sign reversal.
16. A non pipeline system takes 50 ns to process a task. The same task can be processed in a 6 segment pipeline with a clock cycle of 10 ns. Determine the speed up ratio of the pipeline for 100 tasks. What is the maximum speed up that can be achieved.
17. **What are the two instructions needed in the basic** computer in order to set the E flip-flop to 1?
18. Make the following changes to the basic computer.

a) Add a register to the bus system CTR(count register) to be selected with s2, s1, s0=000.
b) Replace the ISZ instruction with an instruction that loads a number into CTR.

    LDC Address CTR <-M [Address]

c) Add a register reference instruction ICSZ: Increment CTR and skip next instruction if zero.Discuss the advantage of this change

19. Draw a timing diagram similar to Fig. 5-7 assuming that SC is cleared to 0 at time T3 if control signal c, is active.
20. An instruction is stored at location 300 with its address field at location 301.The address field has the value 400. A processor register R1 contains the number200. Evaluate the effective address if the addressing mode of the instruction is(a) Direct(b) Immediate(c) Relative(d) Register Indirect(e) Index with R1 as the index