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NAME: Khushal Sachdeva
EXAMINATION ROLL NO.: 20003570032
COURSE NAME: (570) - (CBCS) B.Sc. (Hons.) Computer Science
SEMESTER: I
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NAME OF COLLEGE: (003) - Atma Ram Sanatan Dharam College
EMAIL ID: 88044@arsd.du.ac.in
MOBILE NO.: 8178594741

2000357 00032 Khushal

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QUESTION : 4

Ans

a)

Addressing Mode	Operand
90	Indirect
402	Immediate
800	Direct

402	800	
600	MODE	OPCODE
601	402	
800	90	

(i) effective address = address part + index register

$902 = 402 + i$

$\boxed{i = 500}$ → value of index register

(ii) * if OPCODE is ADD :
Value of PC → before :- 600
After :- 602

* if OPCODE is BUN :
Value of PC → before : 600
After : direct - 402
indirect - 800

(b) • (i) $TR \leftarrow M[PC]$

This can't be done in one clock cycle because Memory is not directly connected with PC.

Correct Sequence :

T_1 : $AR \leftarrow PC$

T_2 : $TR \leftarrow M[AR]$

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(ii) $M[AR] \leftarrow PC,\ PC \leftarrow AR + 1$

This can't be done in one clock cycle because both are using common bus and they can't be done simultaneously.

Correct Sequence :

T_1 : $M[AR] \leftarrow PC,\ AR \leftarrow AR + 1$

T_2 : $PC \leftarrow AR + 1$

(iii) $M[AR] \leftarrow DR + 1$

Incrementing takes one clock cycle and at the same time, data can't be transfered by that register

Correct Sequence :

T_1 : $DR \leftarrow DR + 1$

T_2 : $M[AR] \leftarrow DR$

(iv) $OUTR \leftarrow AC,\ FGO \leftarrow 1$

When $FGO = 1$, only then AC will be transfer to OUTR. Also, $FGO \leftarrow 1$ takes one clock cycle as CPU has to check flag as well

Correct Sequence :

T_1 : $FGO \leftarrow 1$

T_2 : $OUTR \leftarrow AC$