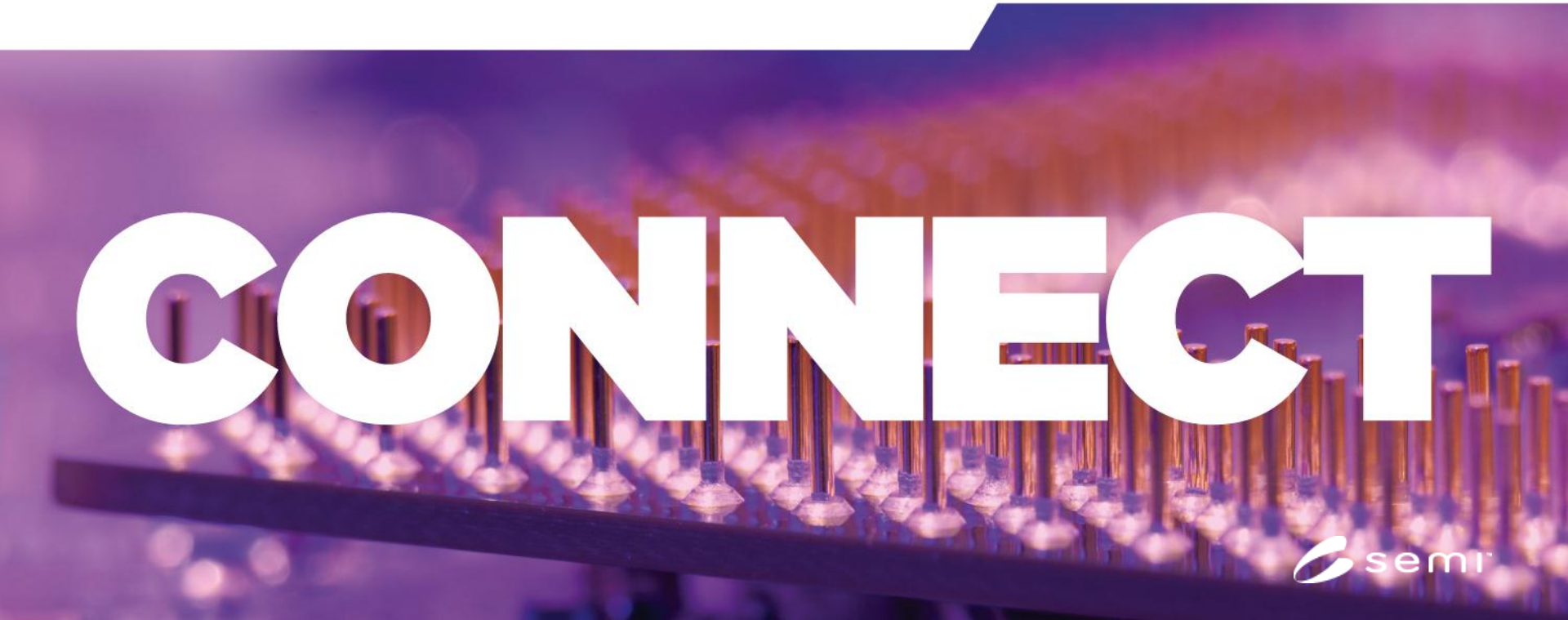
SEMICON® TAIWAN

Device architectures for the 5nm technology node and beyond

Nadine Collaert
Distinguished member of technical staff, imec



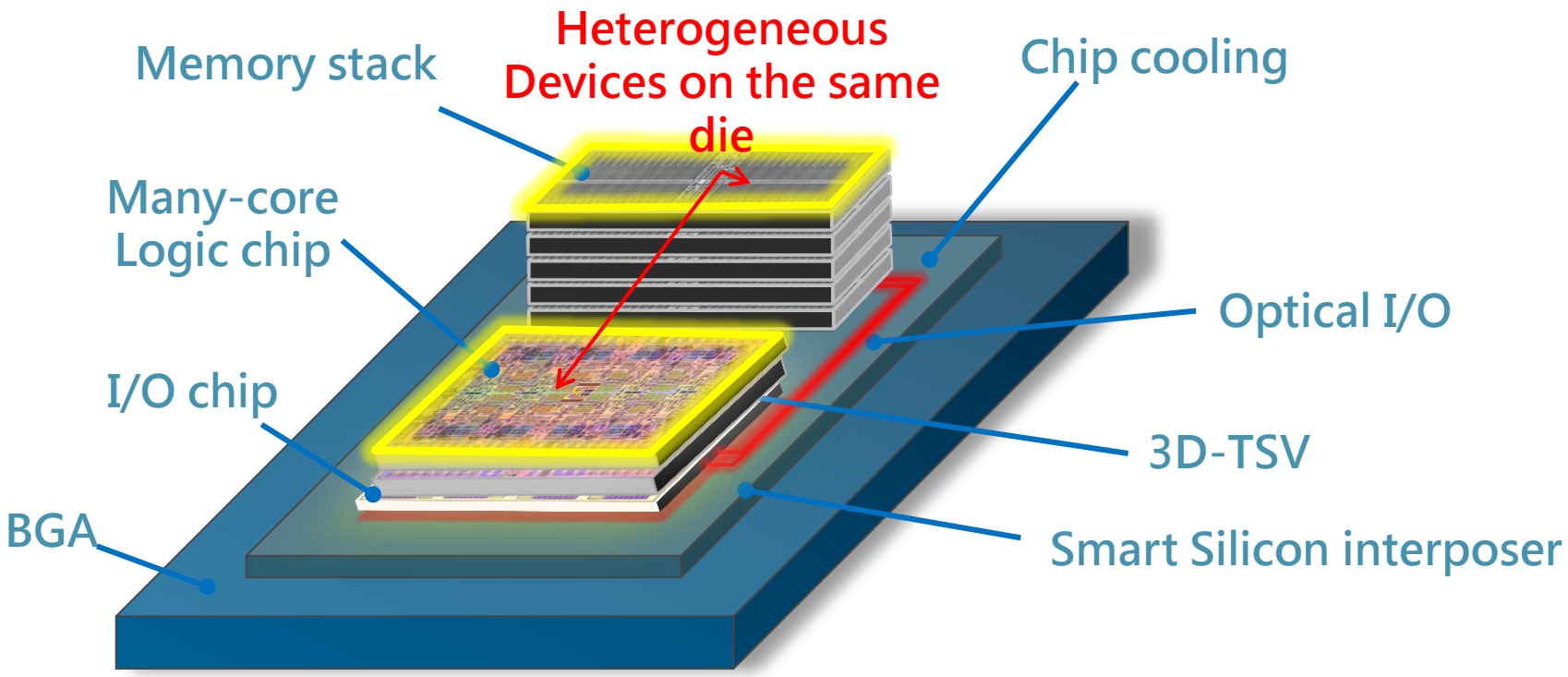
Outline

- Introduction
- Beyond FinFET: lateral nanowires and vertical transistors
- High mobility materials
- New switching mechanisms
- Summary

Introduction

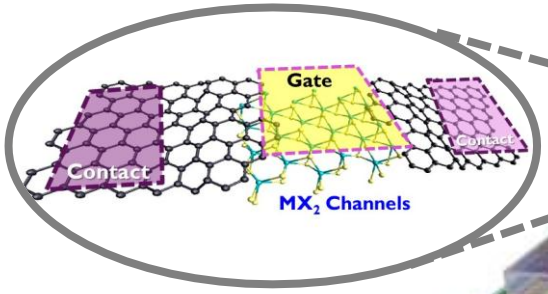
The future heterogeneous system

MAXIMIZING FUNCTIONALITY AND REDUCING POWER DENSITY

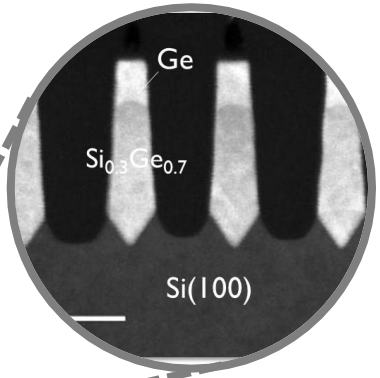


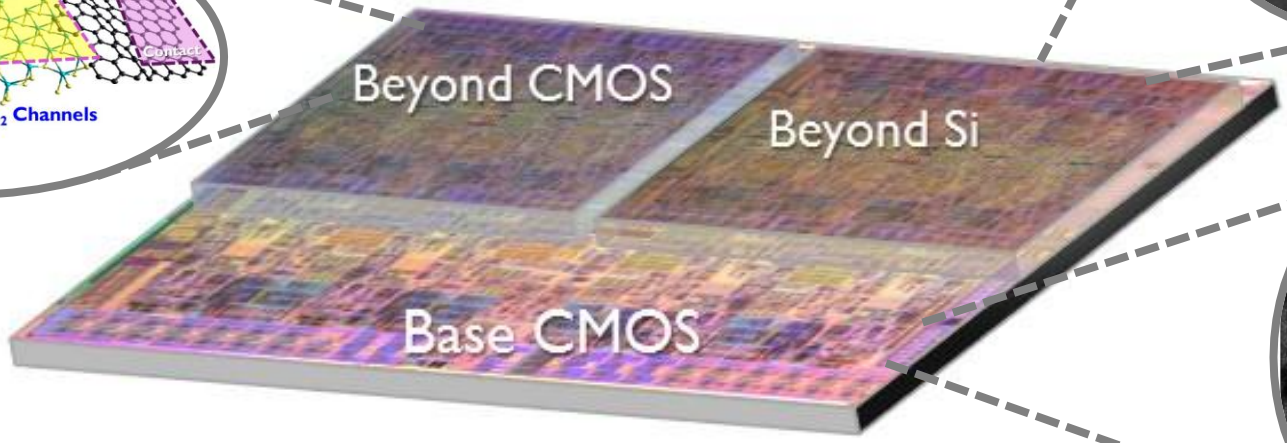
Standard CMOS, beyond Si & Beyond CMOS

High bandgap MX2 materials
Spin logic...

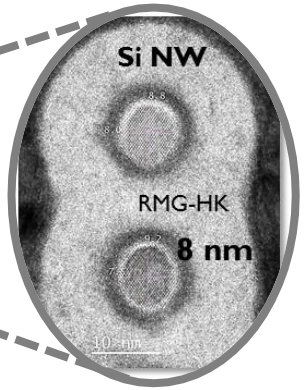


Low bandgap high mobility materials
Vertical devices



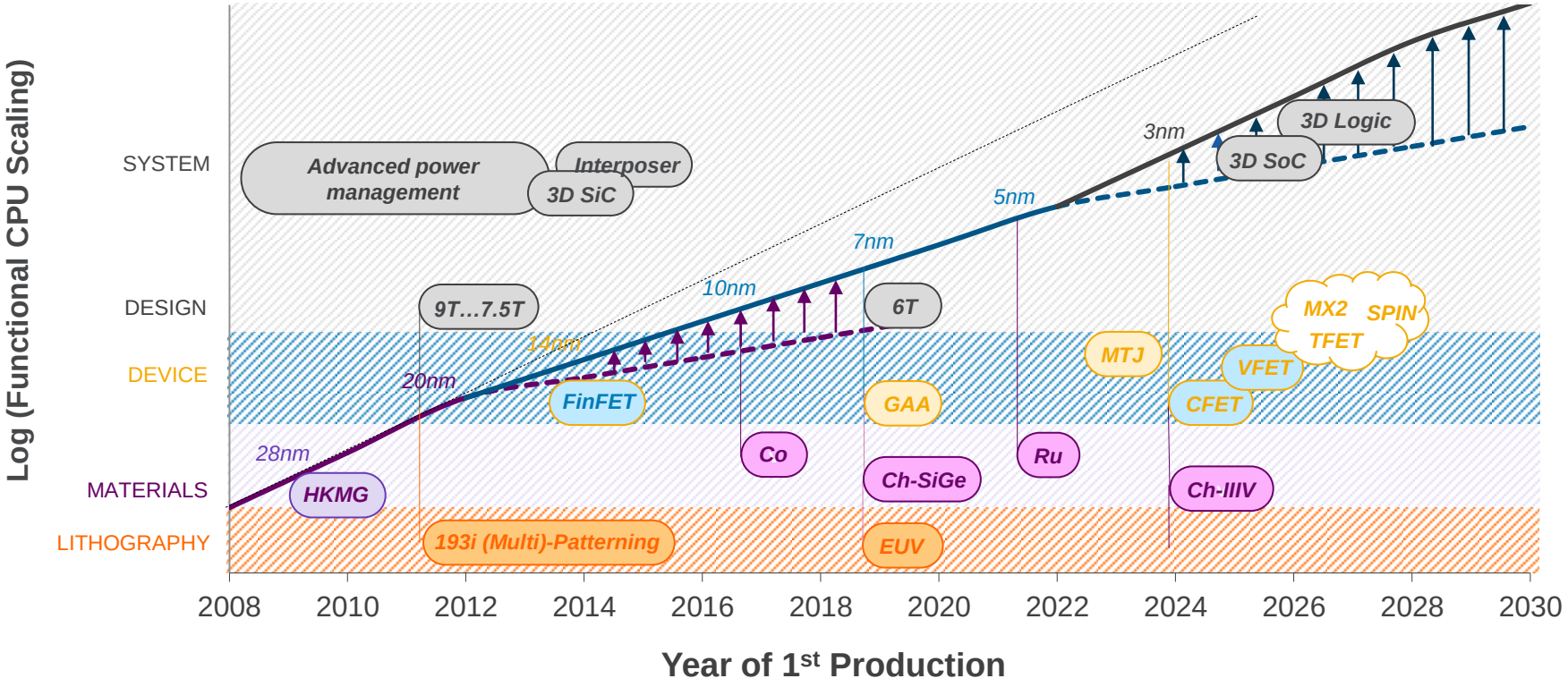


FinFET, GAA,...



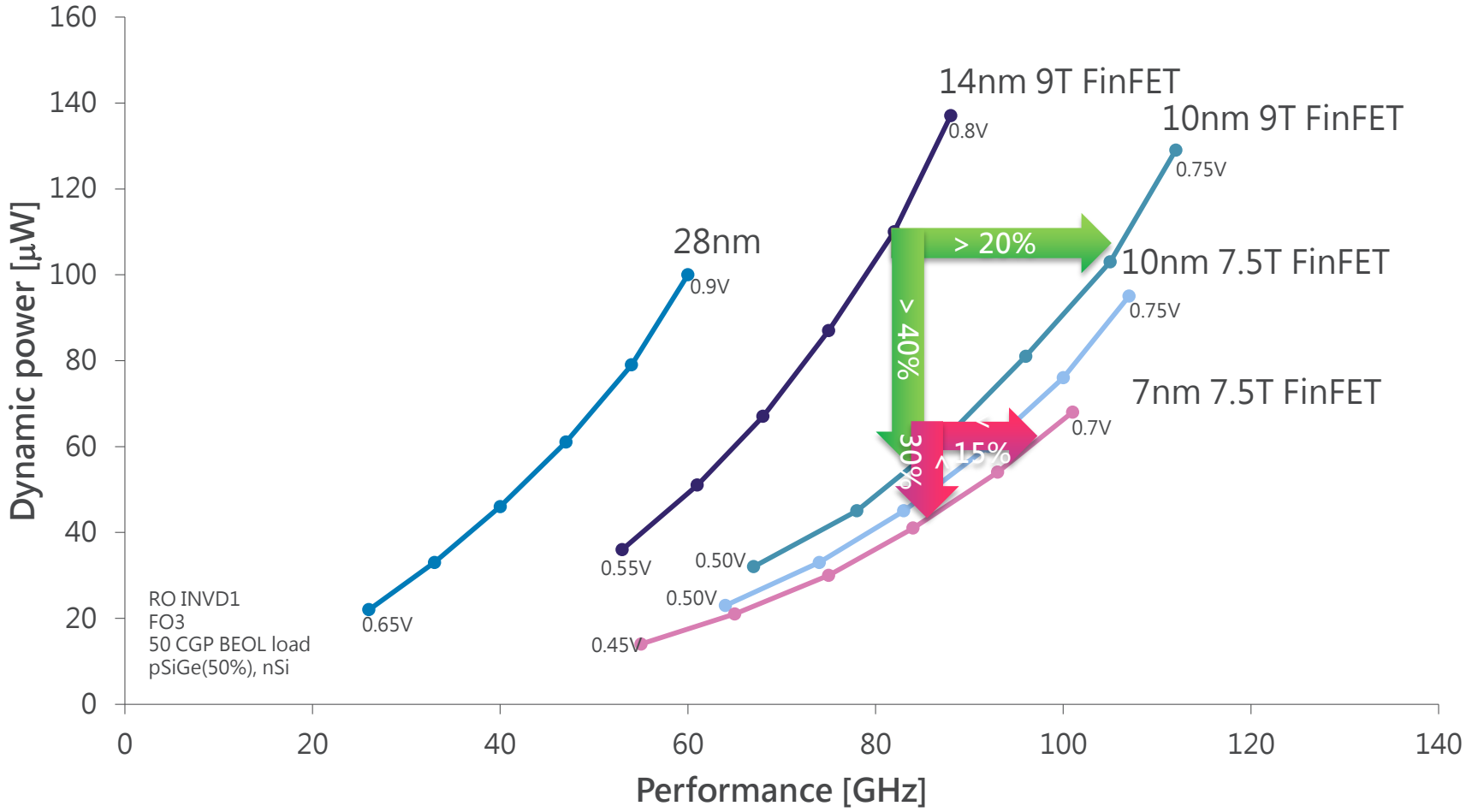
Standard CMOS and new devices to enable future **heterogeneous** systems
Ability to innovate & co-integrate devices to optimize performance & functionality is key

Increase compute power

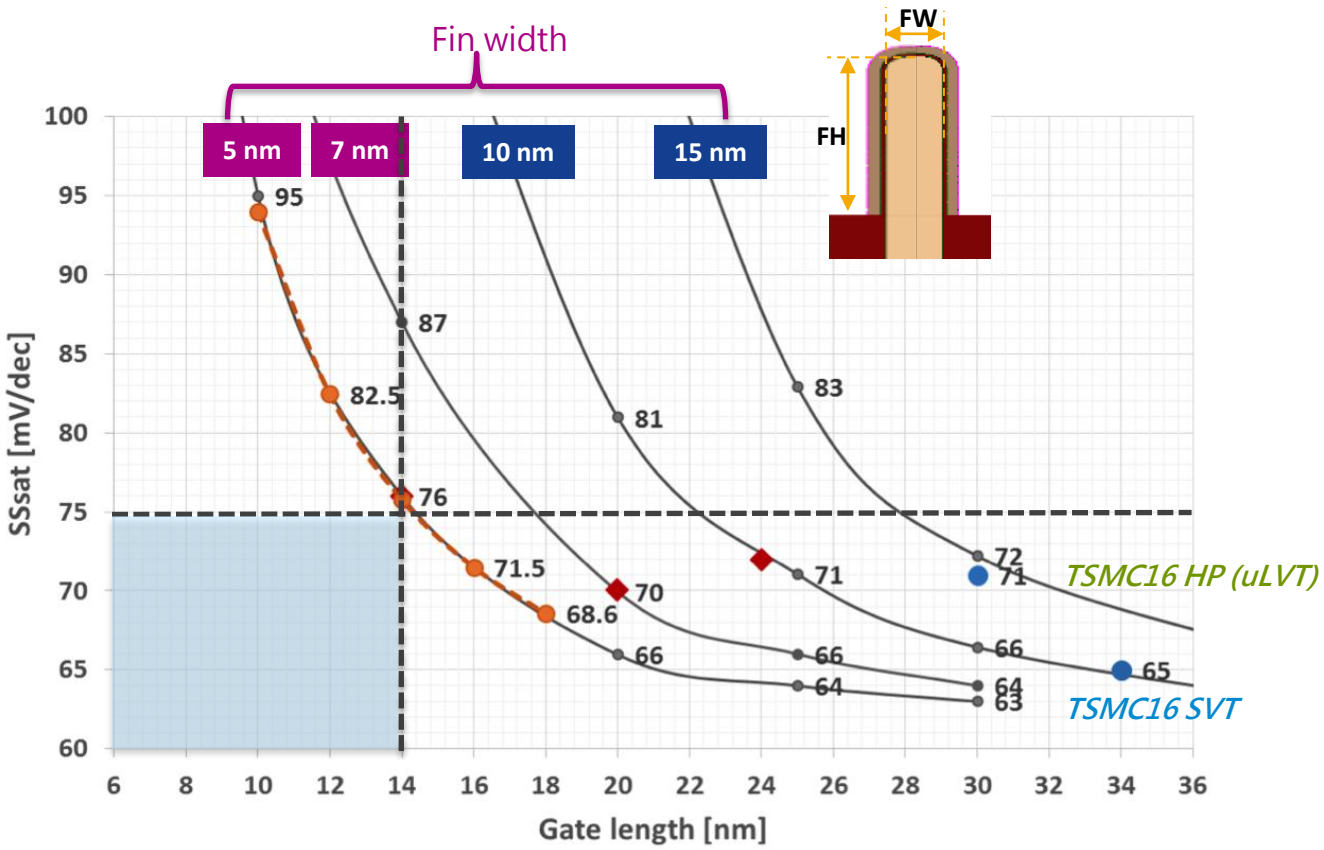


Beyond FinFET

Power-performance scaling: FinFET scaling to 7nm

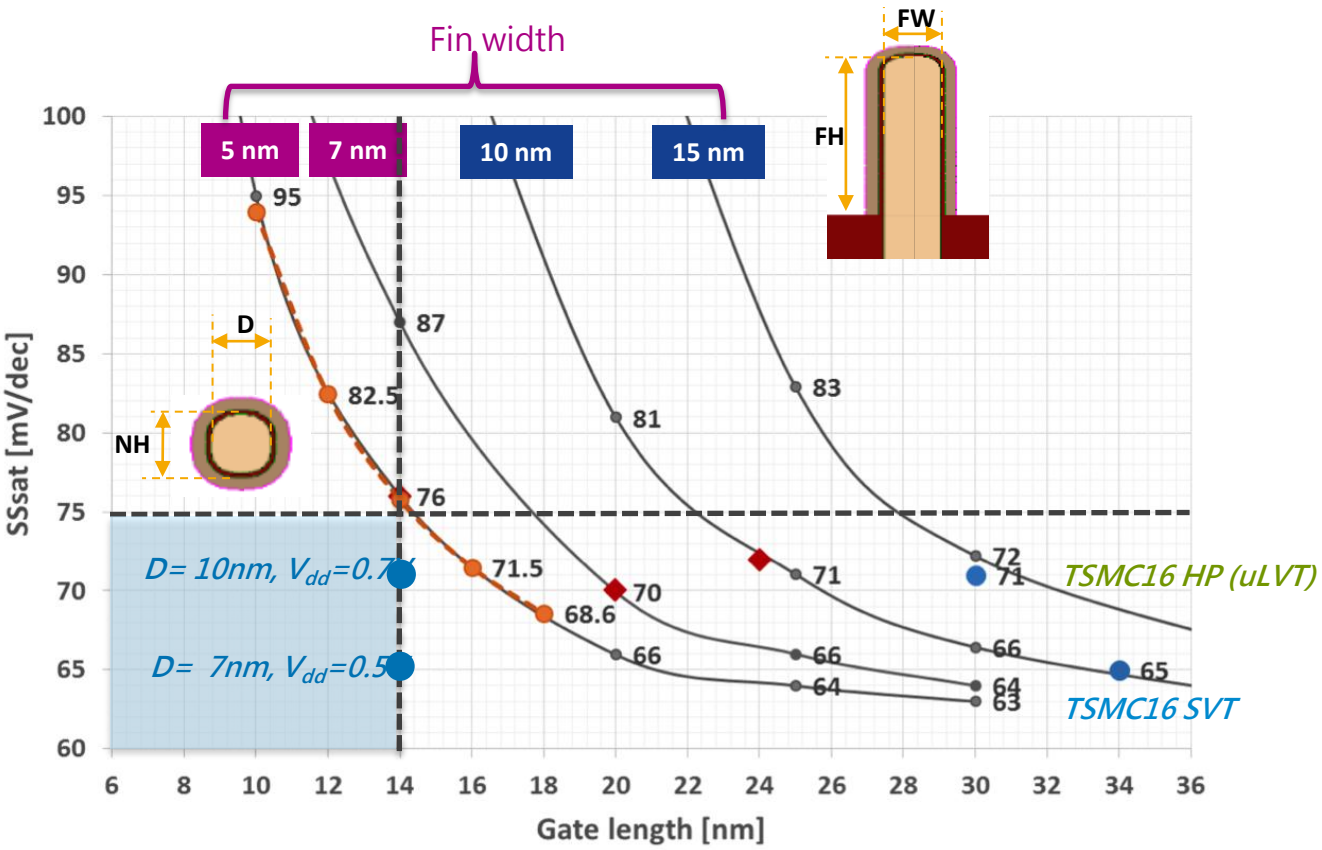


Scaling down the fin width to improve electrostatics



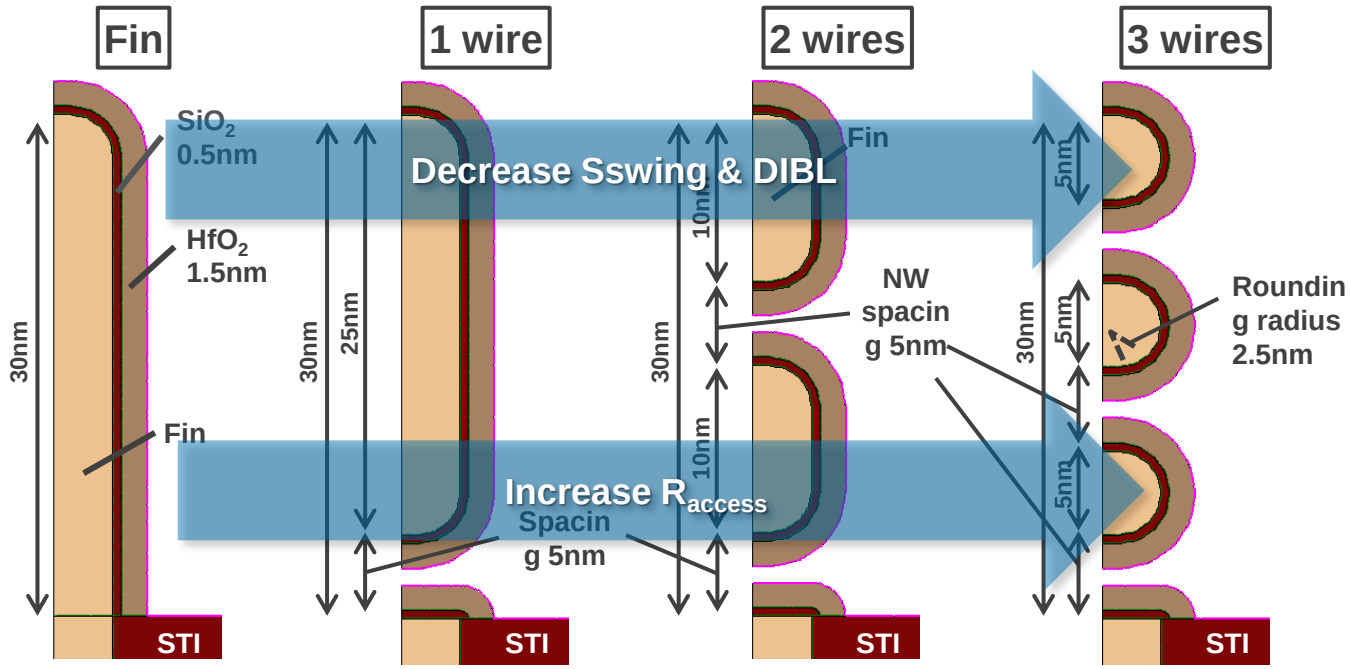
For a target gate length of 14nm, fin width has to be reduced to 5nm to meet device electrostatics.

From FinFET to lateral nanowires (NW)



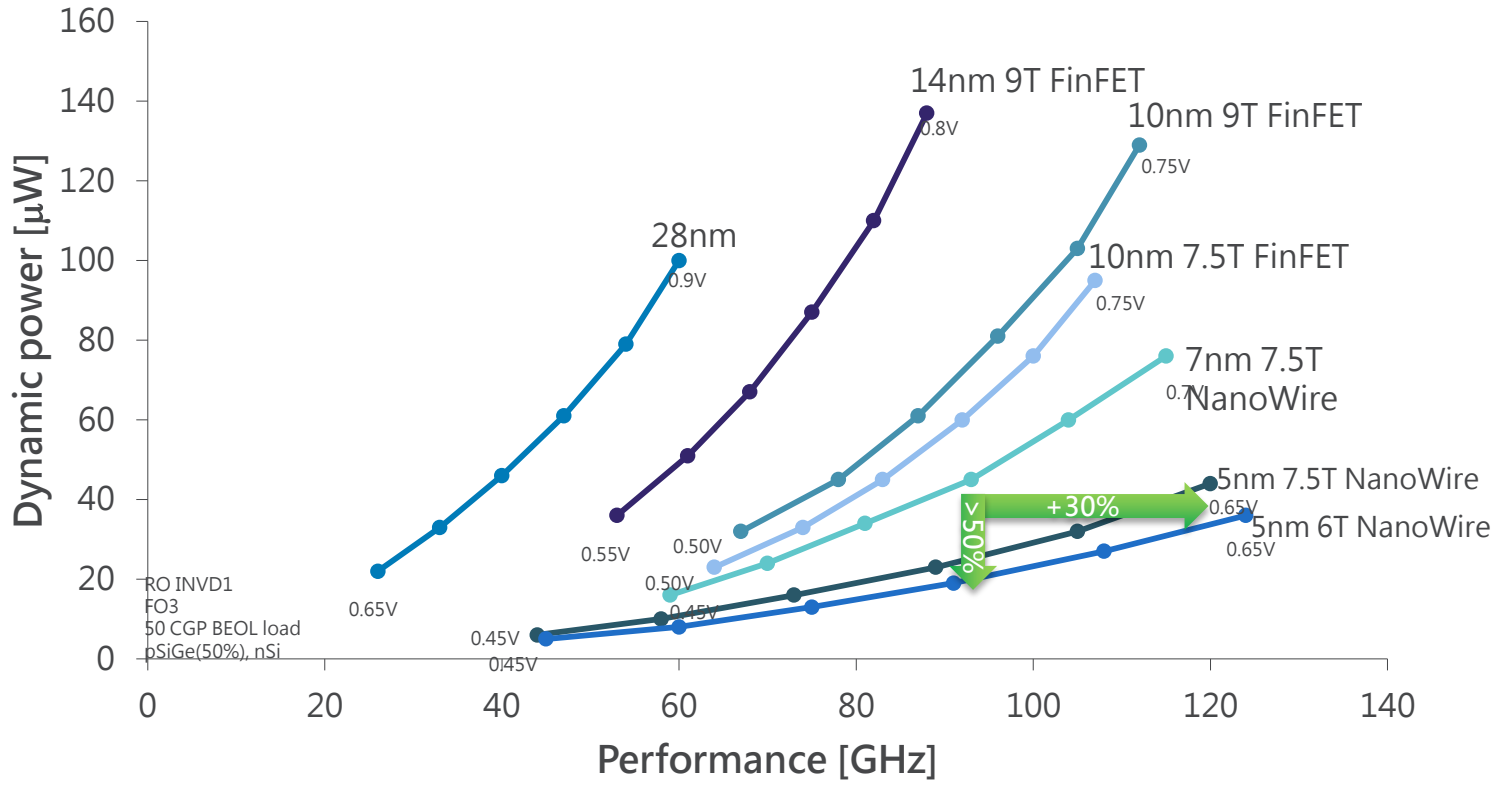
Nanowire FETs provide better electrostatics at relaxed nanowire diameter.

From FinFET to lateral NW



Higher stack is needed for nanowire FETs to compensate smaller cross section than FinFET.
Increased parasitics require the enabling of new features e.g. internal spacers

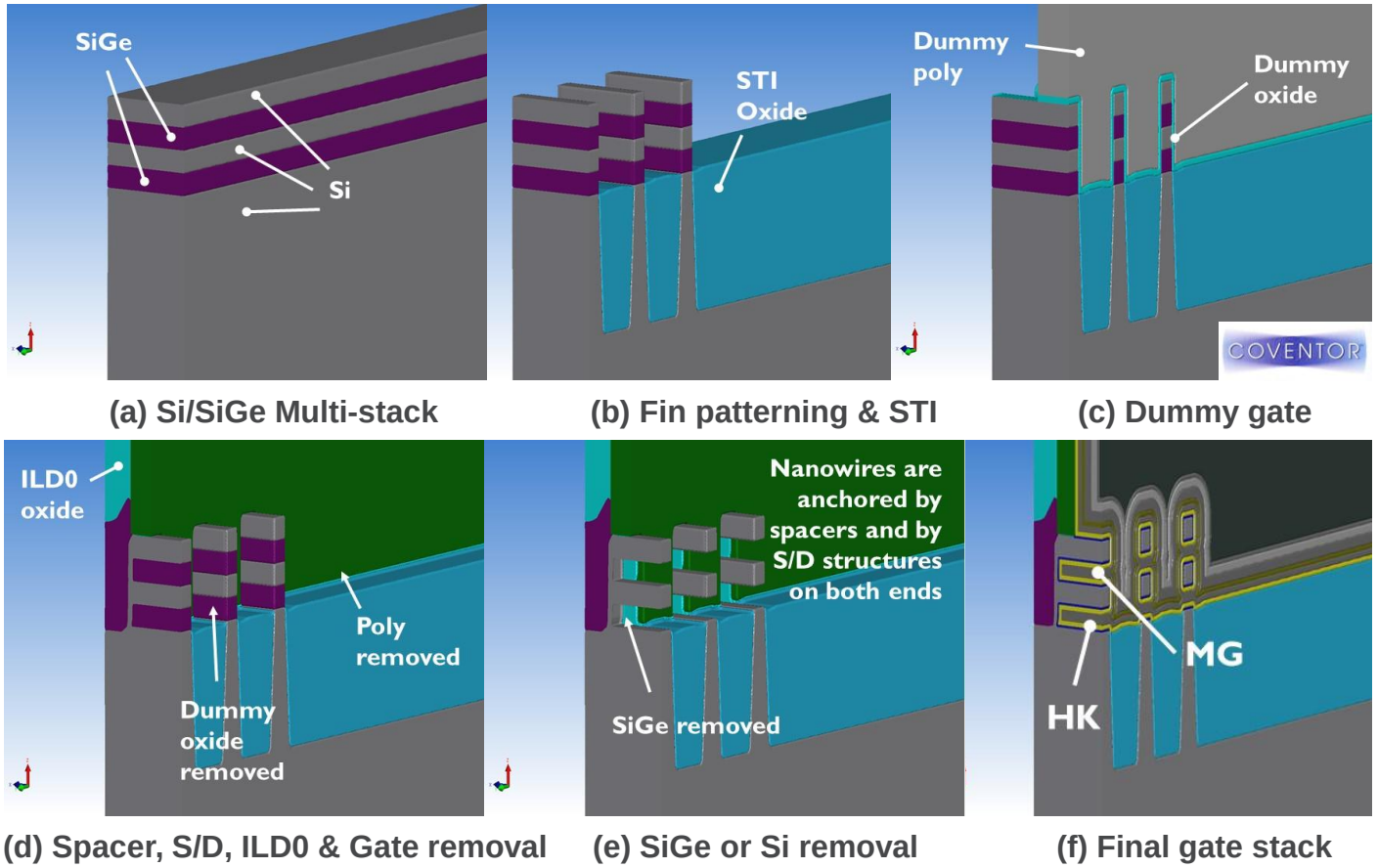
Power-performance scaling: from FinFET to lateral NW



NW device allows further voltage scaling and performance gains

Lateral NW: an evolutionary path from FinFET

H. Mertens et al., VLSI Symp. 2016.

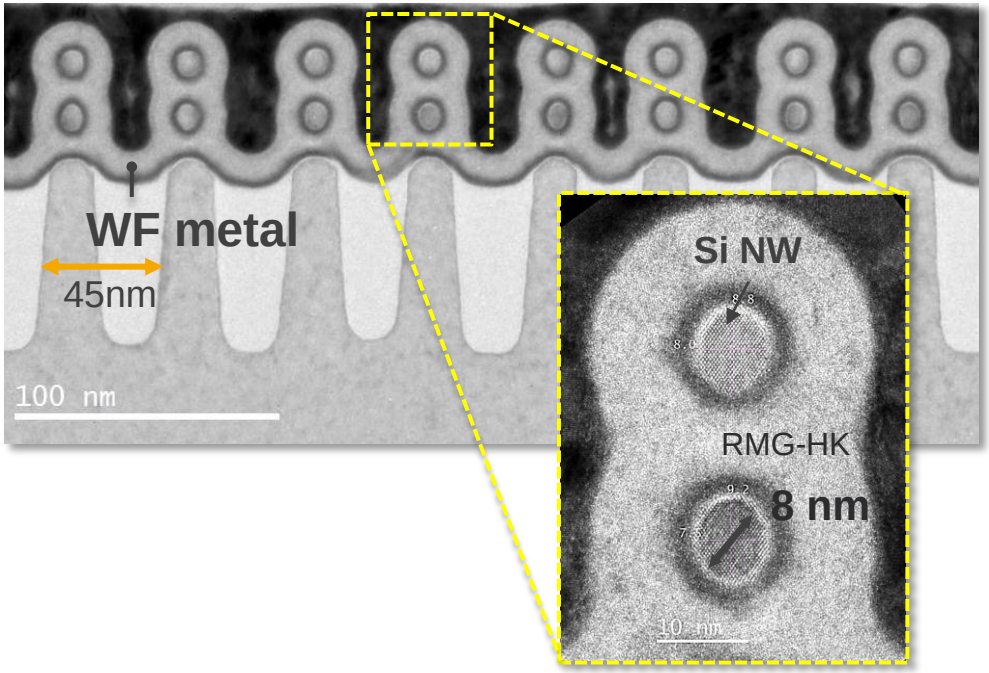


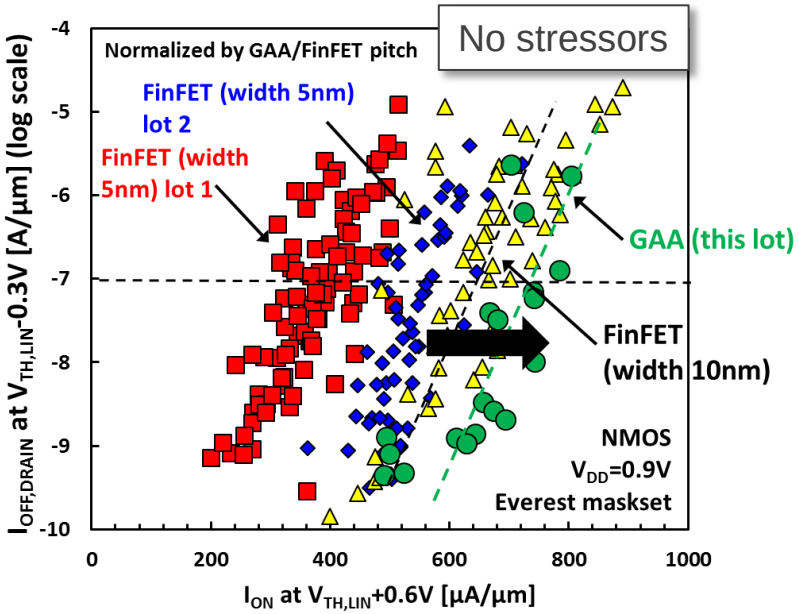
(a) Si/SiGe Multi-stack (b) Fin patterning & STI (c) Dummy gate

(d) Spacer, S/D, ILD0 & Gate removal (e) SiGe or Si removal (f) Final gate stack

Demonstration of a 2-stacked lateral nanowire device

H. Mertens et al., VLSI Symp. 2016.

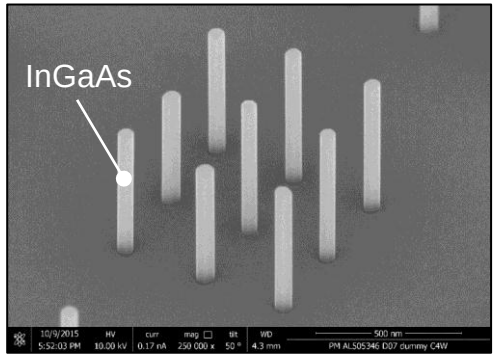


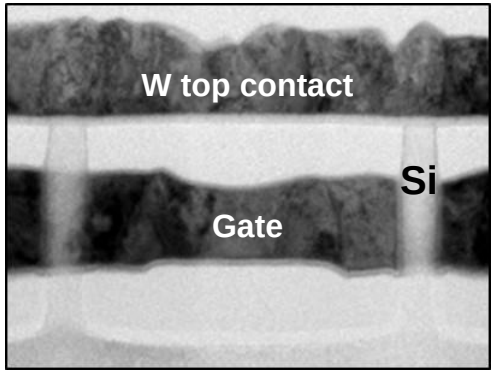


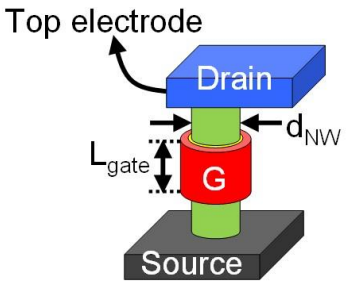
- Demonstrated 2-stacked Si NWFET
- Improved performance and electrostatics as compared to FinFETs

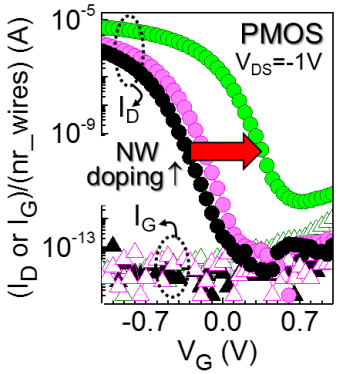
Going vertical

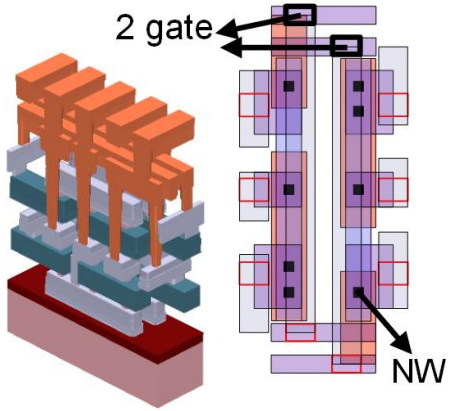
Integration	Device	Circuit	System

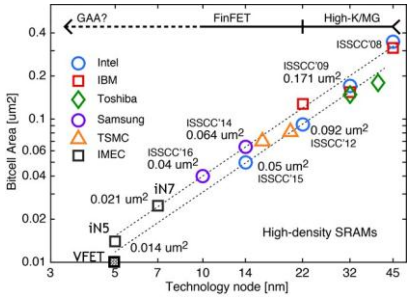


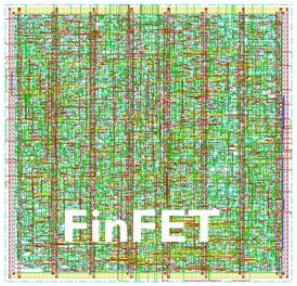










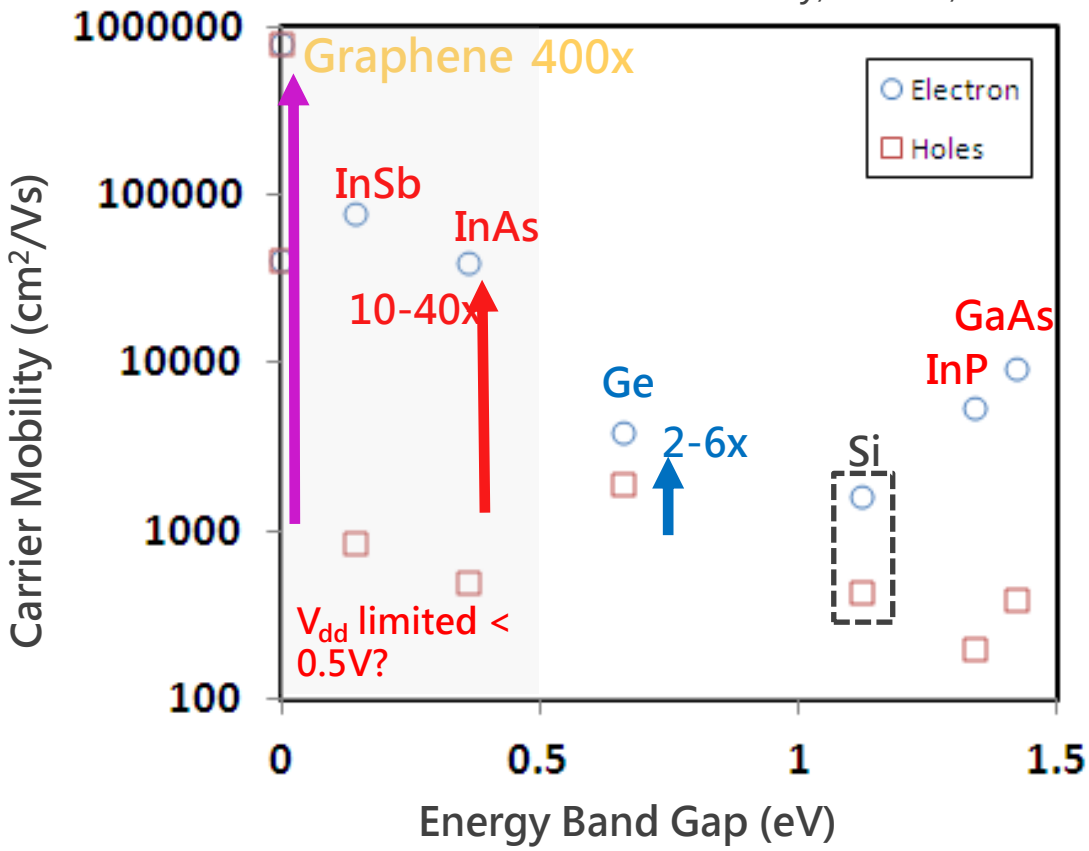


Parameters	N5 FinFET	N5 VFET
Area [μm²]	227.8	185.5
Wirelength [μm]	4578	4118
Vias	39207	43505

High mobility materials

Why high mobility materials?

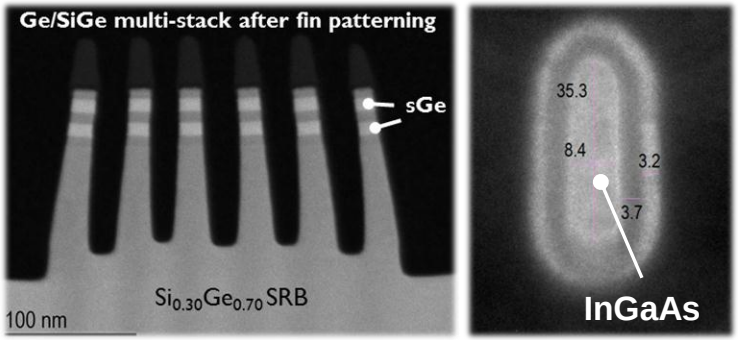
After R. Pillarisetty, Nature, 2011.



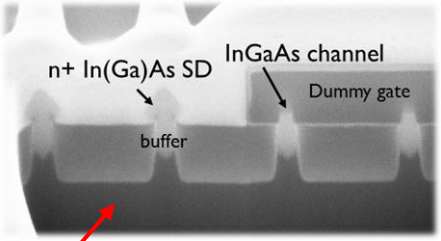
New Materials with Major Transport Enhancement over Si

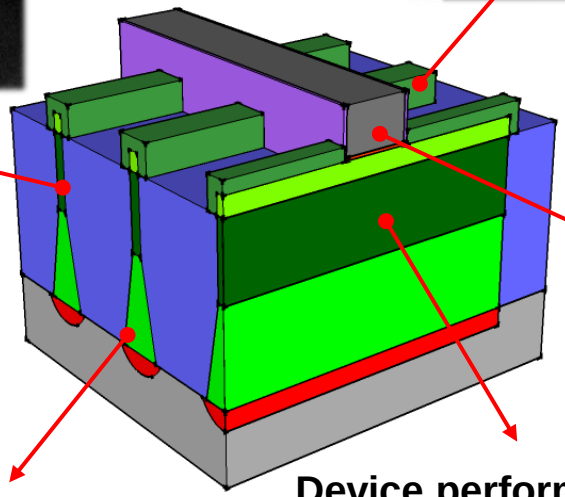
Challenges for high mobility materials

Fin Replacement/Wide field/SRB
Epi & Integration

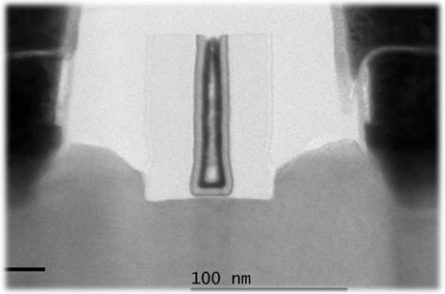


Junction engineering & contacting

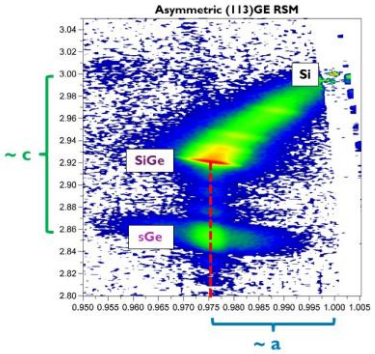


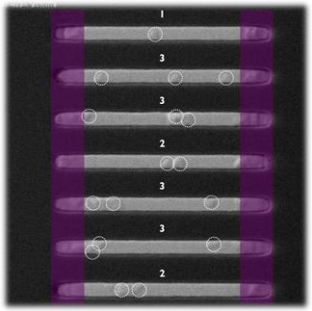


Gate stack & Surface Passivation

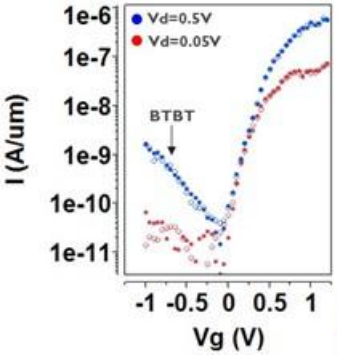


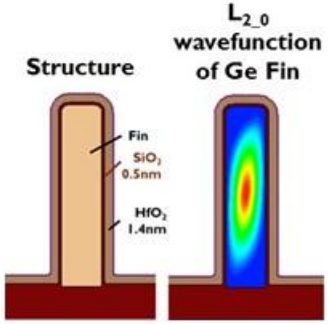
Defect & Phys. Metrology





Device performance and scalability



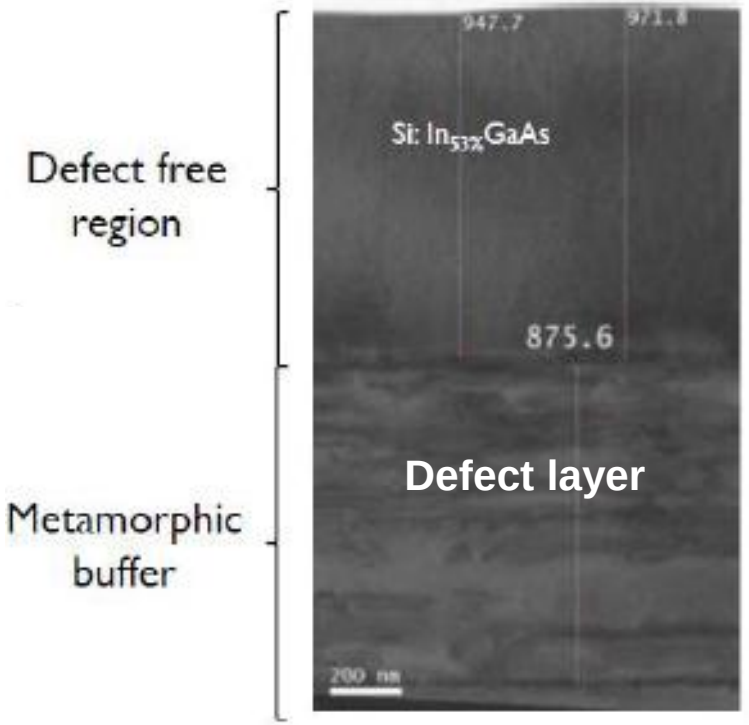


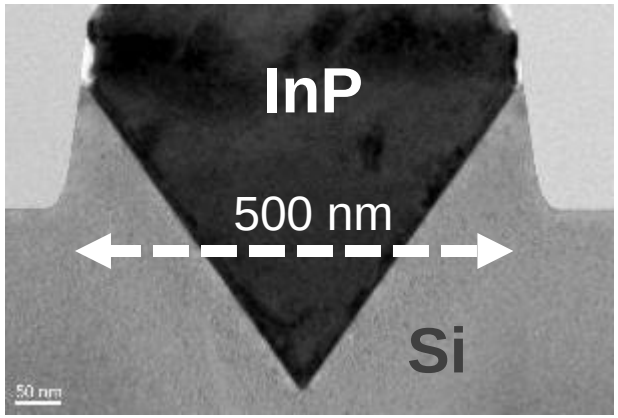
Challenges for epitaxial growth

Global
Wafer-level
Stress-Relaxed Buffer

Local
Wide-Area
Virtual Substrate
(Wide-Trench ART)

Local
Device-level
Virtual Substrate
(Narrow Trench ART)



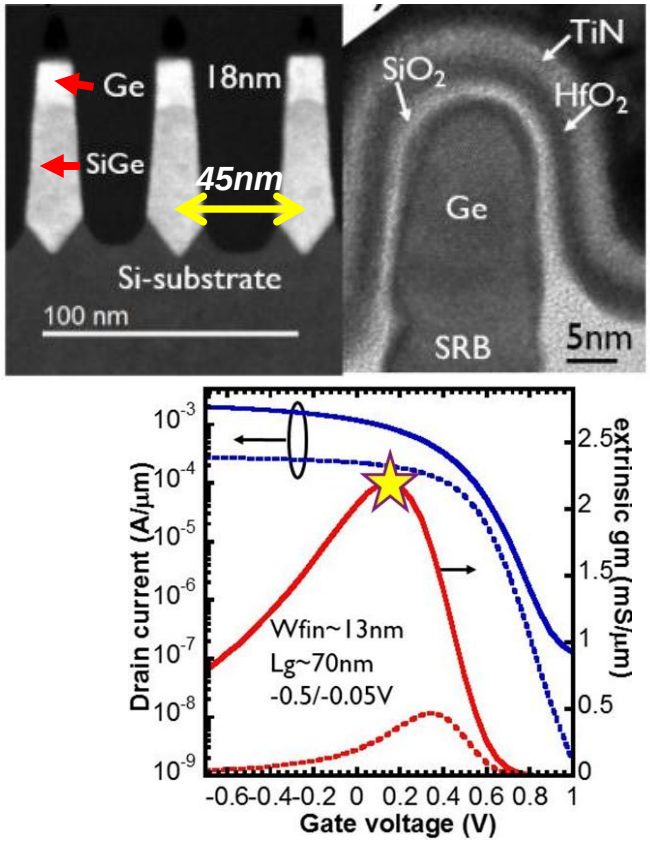


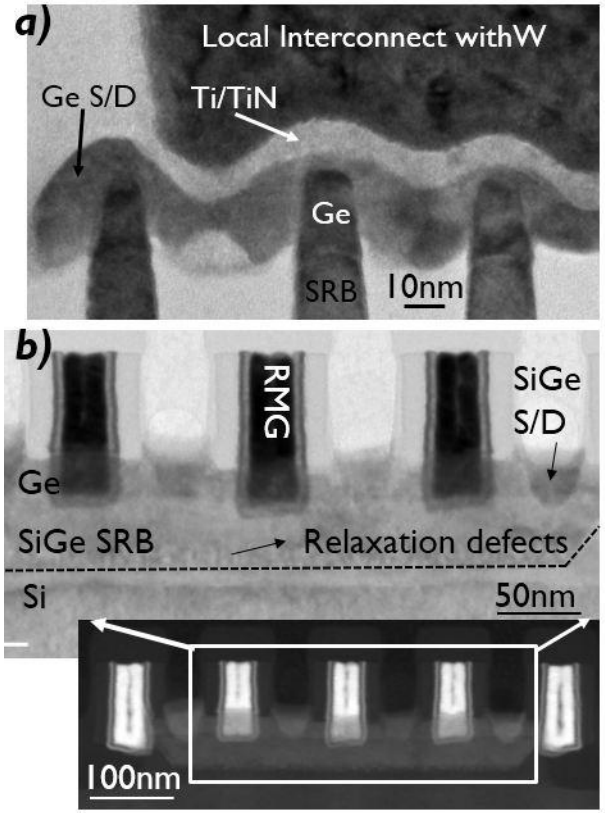
300mm | **0.5μm-500nm** | **< 50nm**

Ge FinFET using fin replacement technique

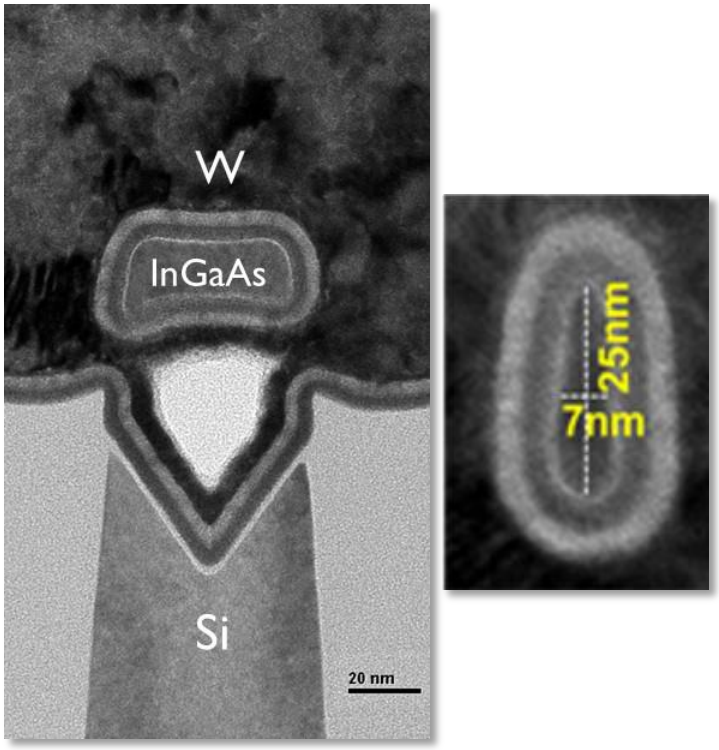
FIN PITCH DOWN TO 45NM

L. Witters et al., VLSI Symp. 2015.

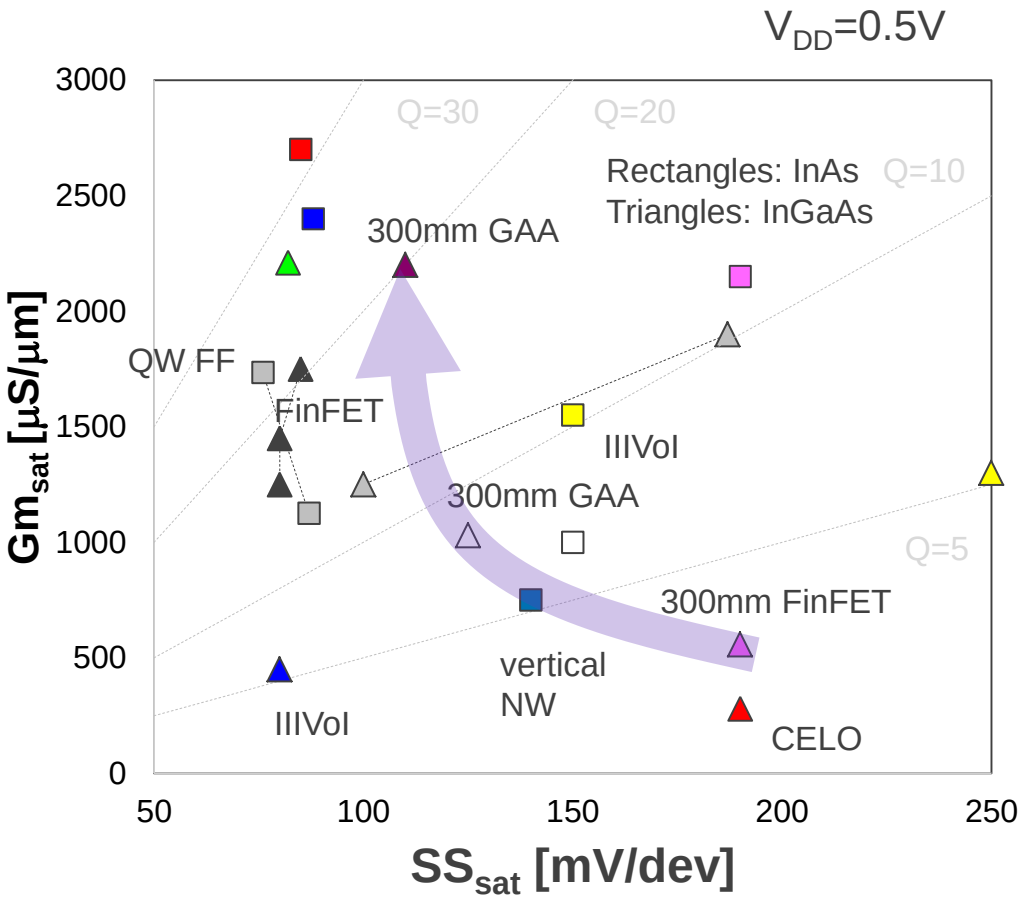




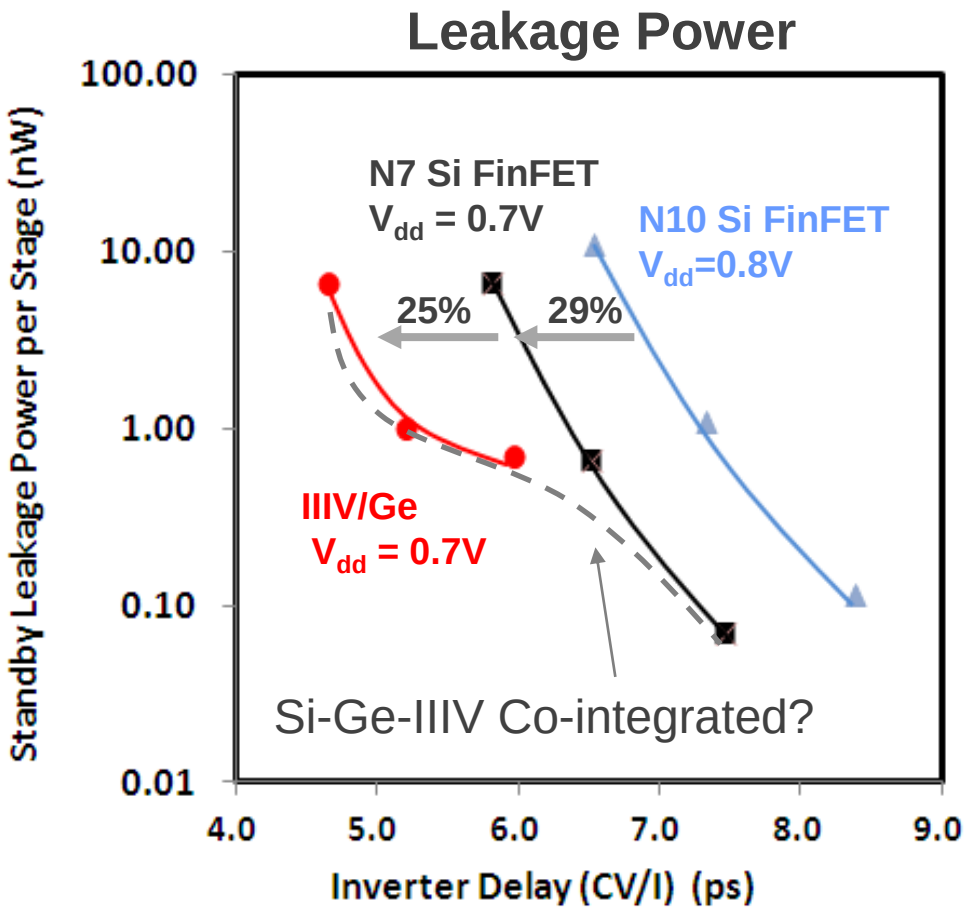
High performance III-V devices on 300mm Si



N. Waldron et al., IEDM, 2015.
X. Zhou et al., VLSI 2016.

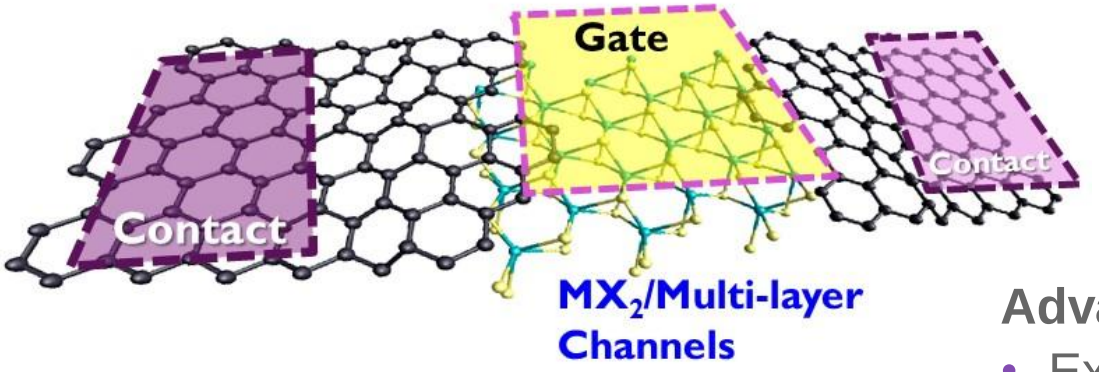


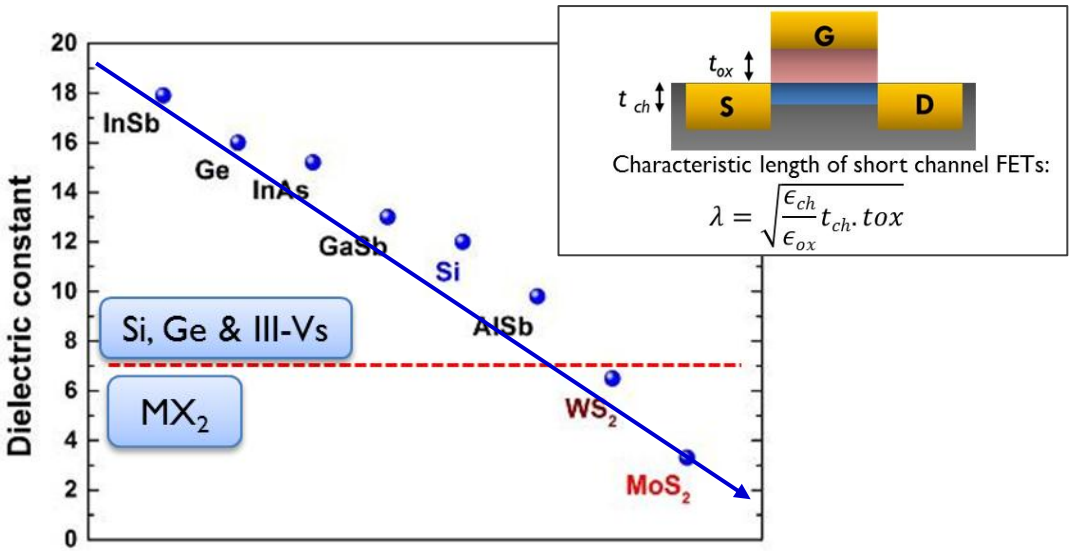
Need for co-integration with Si



High mobility channels offer more performance but leakage span limited
Need Si-channel co-integration for SOC

What about 2D materials?





Advantages:

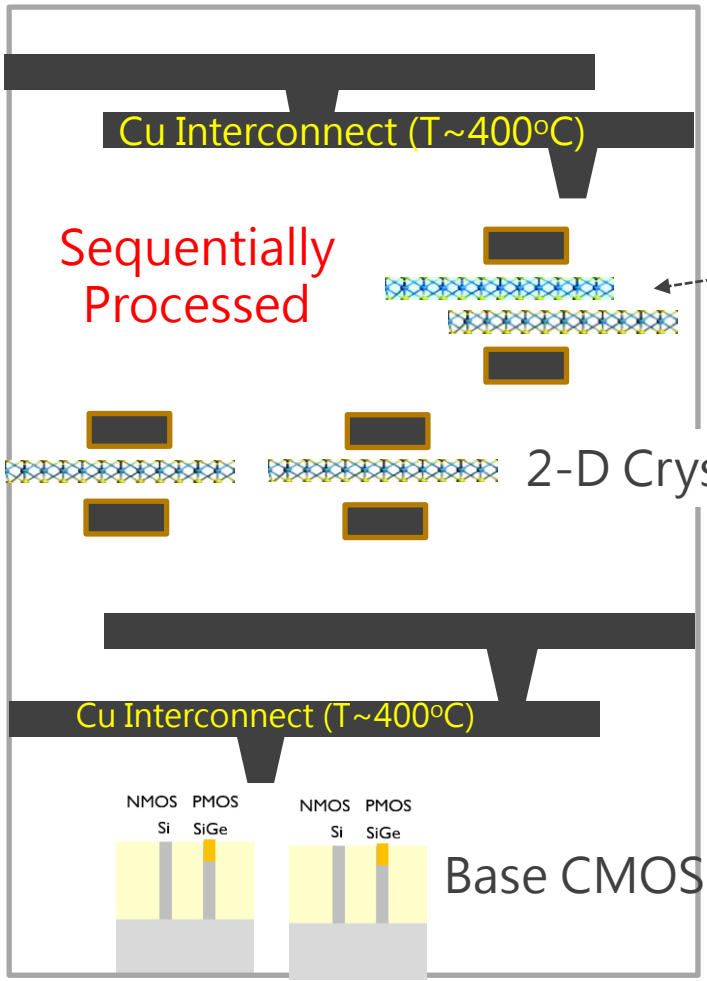
- Expected reduced SCE
- No dangling bonds
- Large choice of materials and bandgaps

Challenges:

- Large scale growth of MX2
- Choice of MX2 material for NFET and PFET
- Gate stack
- Contacts

Heterogeneous integration with base CMOS

3-D Hetero-SOC

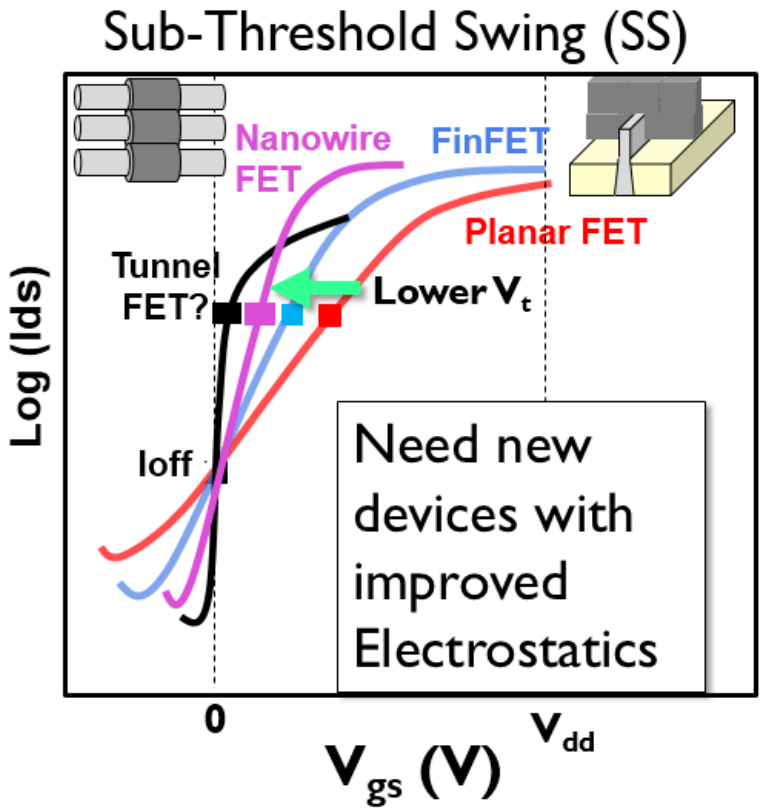


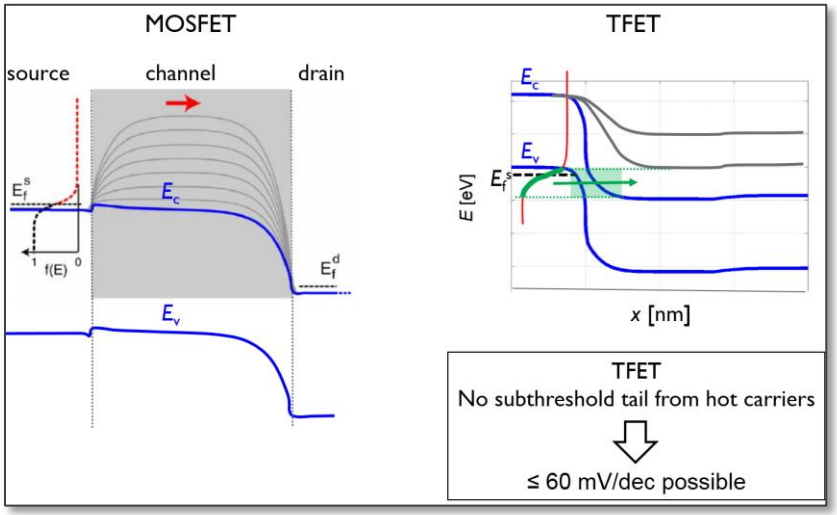
- Can the 2-D crystals be selectively grown between the interconnects? Or by transfer & bond?
- Thermal budget of 2-D device processing is typically low-T, but material growth is still unclear

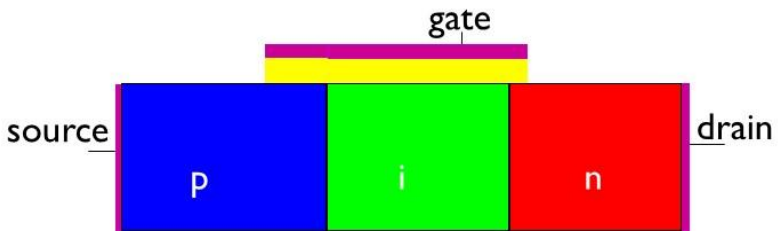
New switching mechanisms

Moving to tunnel FET

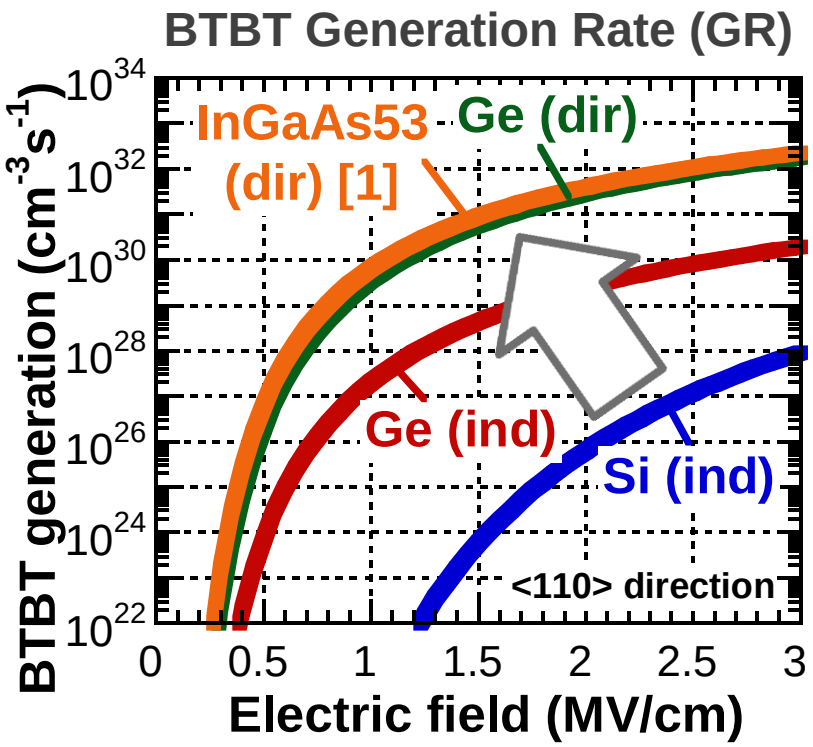
ULTRA-LOW VOLTAGE APPLICATIONS







From group IV to III-V



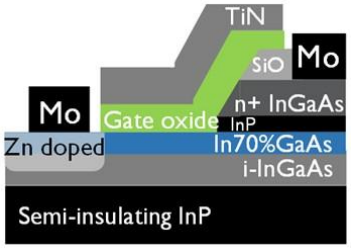
Probability of tunneling is dependent on bandgap

Higher tunneling generation rate for low bandgap materials

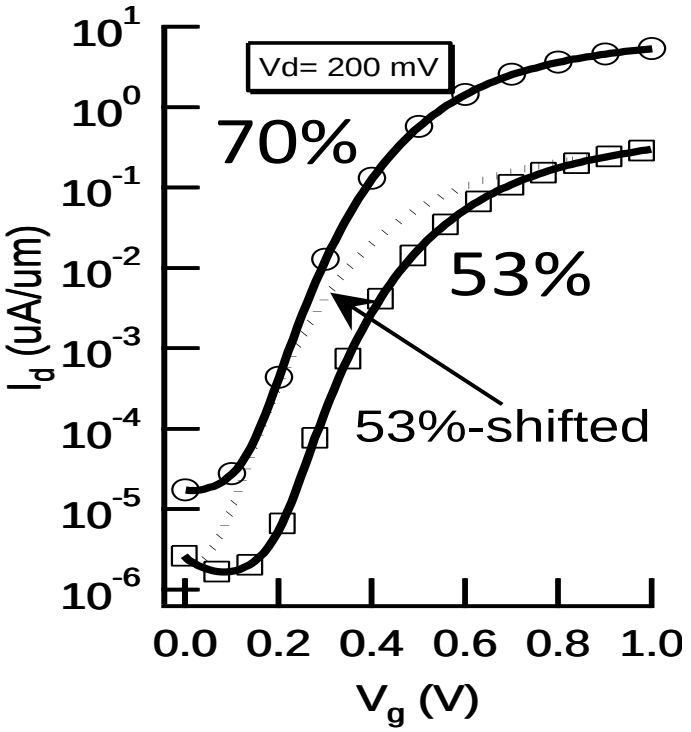
Increased performance expected for III-V

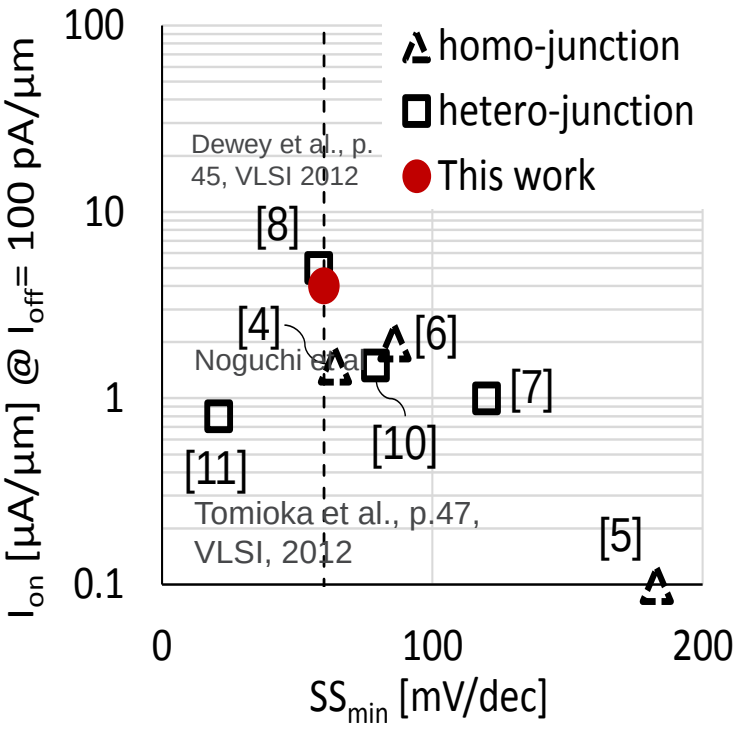
Kao et al, TED 59(2), 292 (2012) & [1] Q. Smets et al, SSDM 2013

III-V homojunction n-TFET process and device



A. Alian et al., IEDM, 2015.

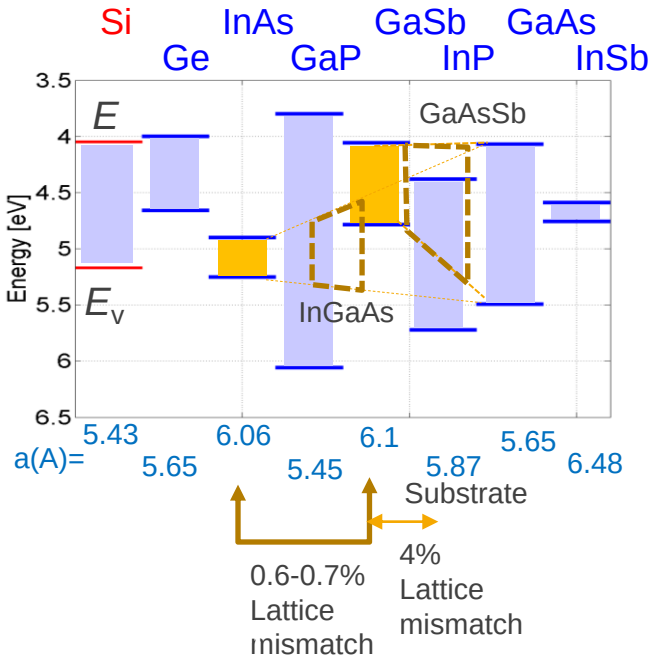


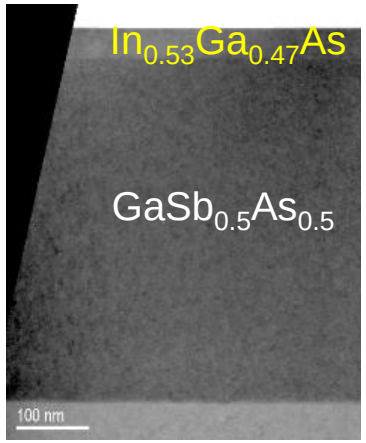


- Significant boost with 8nm strained InGaAs (70% In) (quantum confinement & bandgap)
- Very low TAT observed
- SS less degraded by D_{it} in TFET due to energy range for carrier exchange in TFET operations

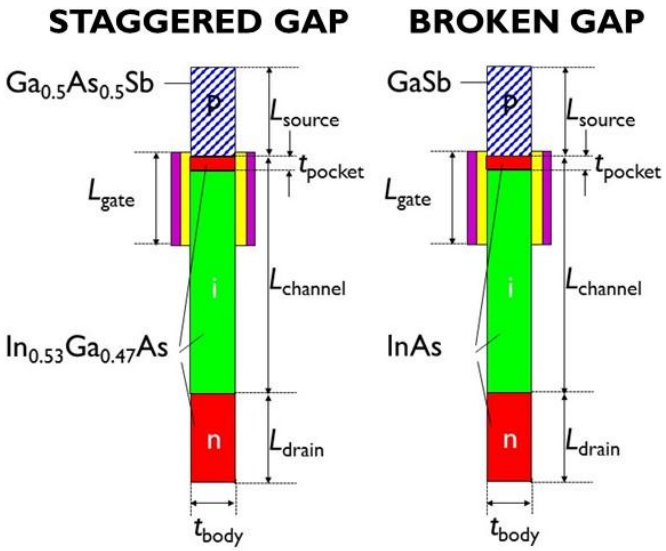
III-V Heterostructures

- Staggered and broken gap configurations





S. El Kazzi et al., EUROMBE 2015.

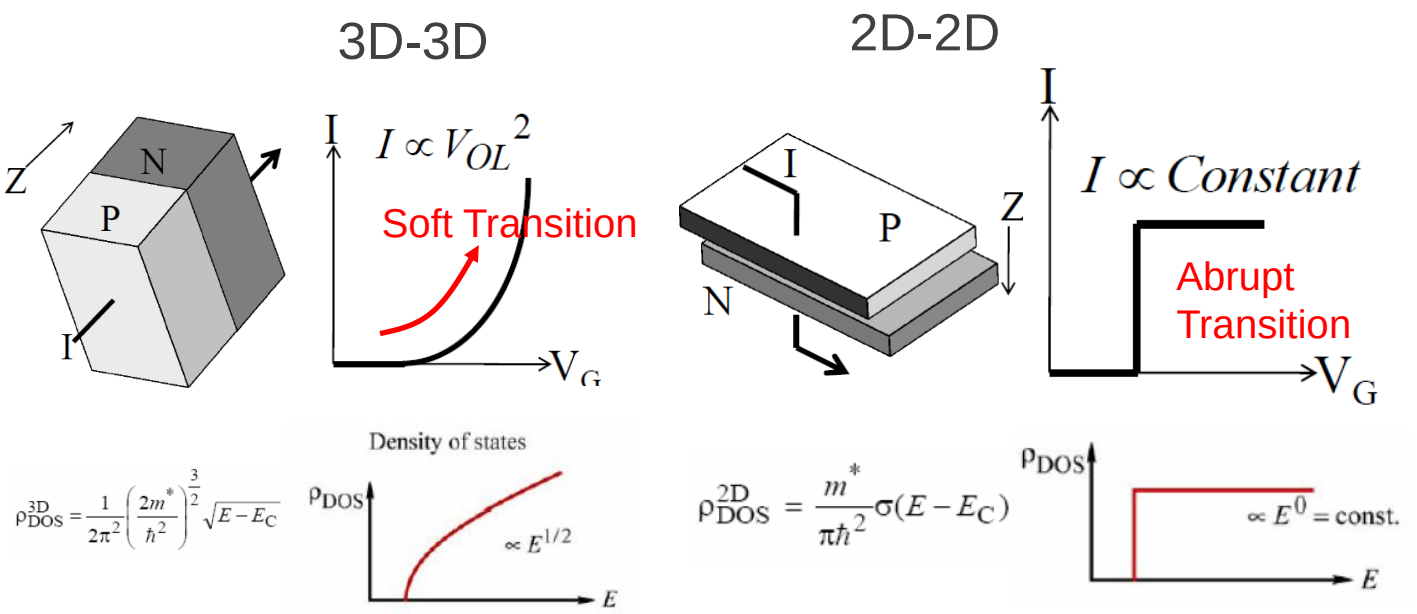


A. Verhulst et al., IEDM, 2014.

Sb-based materials needed to allow best trade-off between performance & electrostatics

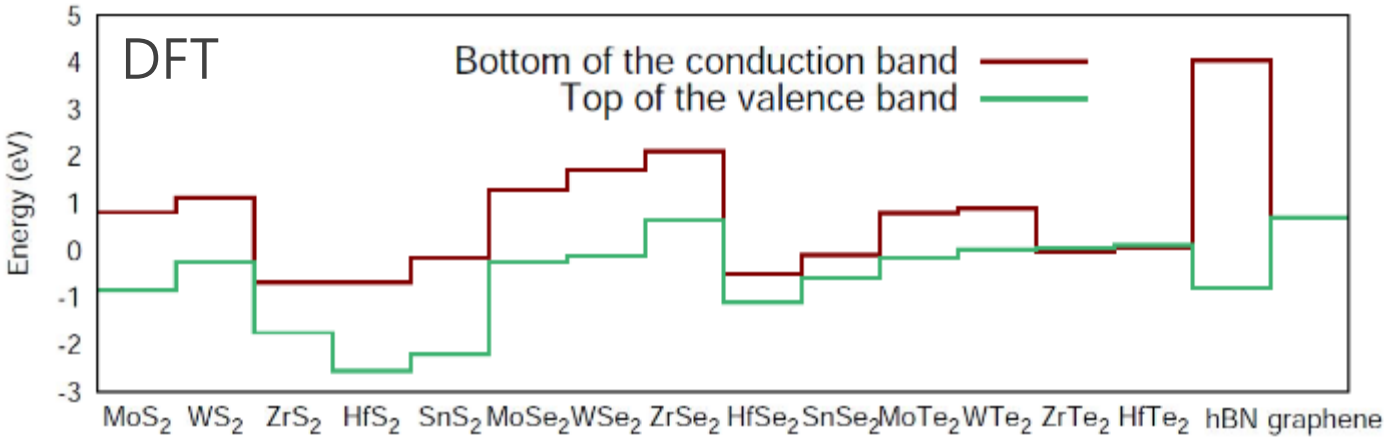
From 3D TFET to 2D TFET

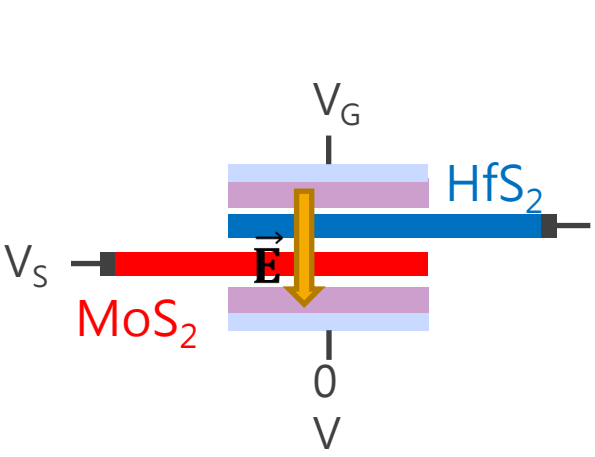
After Eli Yablonovitch 2012, UC Berkeley



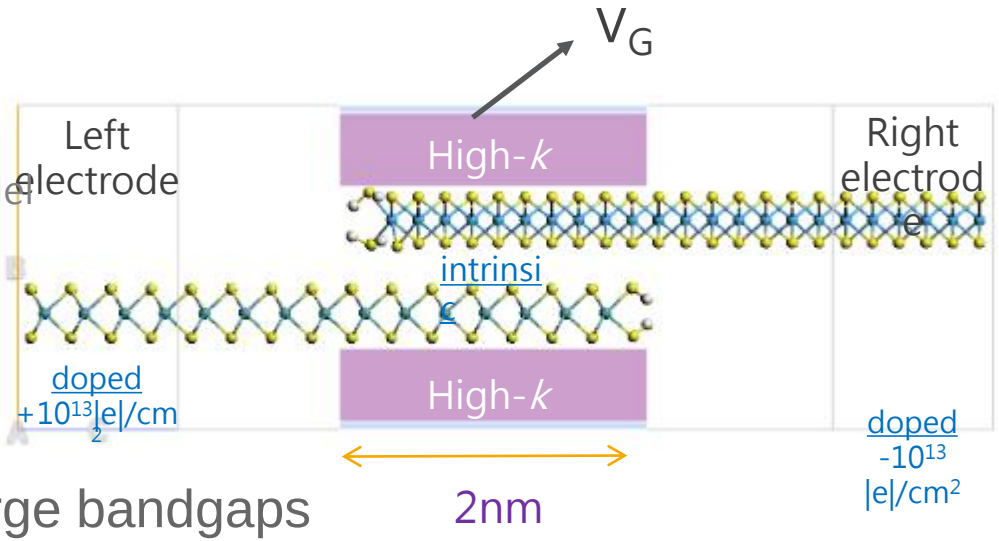
- Steepness of the swing over a wide-Vg range limited by 3-D DOS
- Investigate 2-D TFET options

2-D TFETS with 2-D MX_2 (TMD) heterostructures





Device model

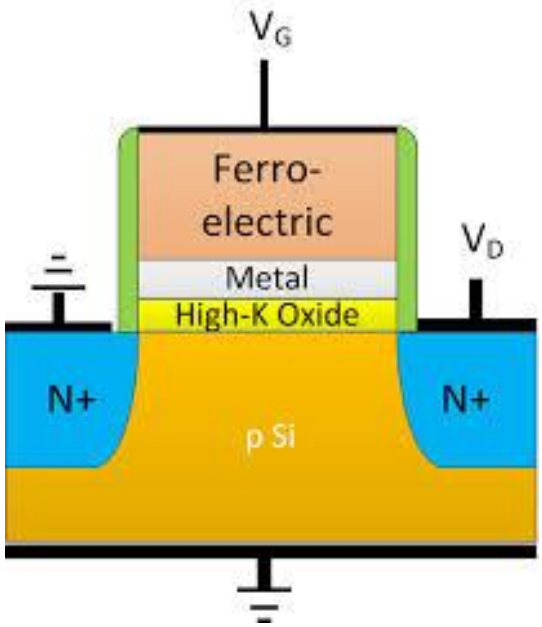


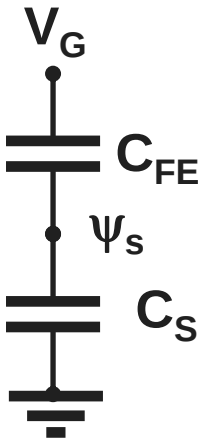
- Broken gap devices with large bandgaps
- Lattice mismatch is no longer an issue – van der Waals stacking

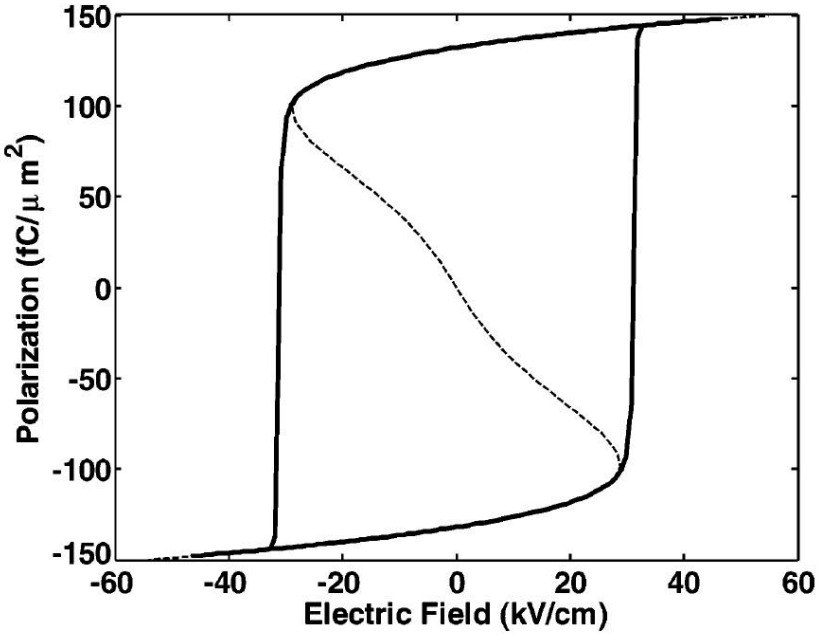
Negative capacitance FET (NC-FET)

$$SS = \frac{\partial VGS}{\partial \psi_s} \frac{\partial \psi_s}{\partial (logID)} = m \times n$$

S. Salahuddin et al., Nano letters, 2008.



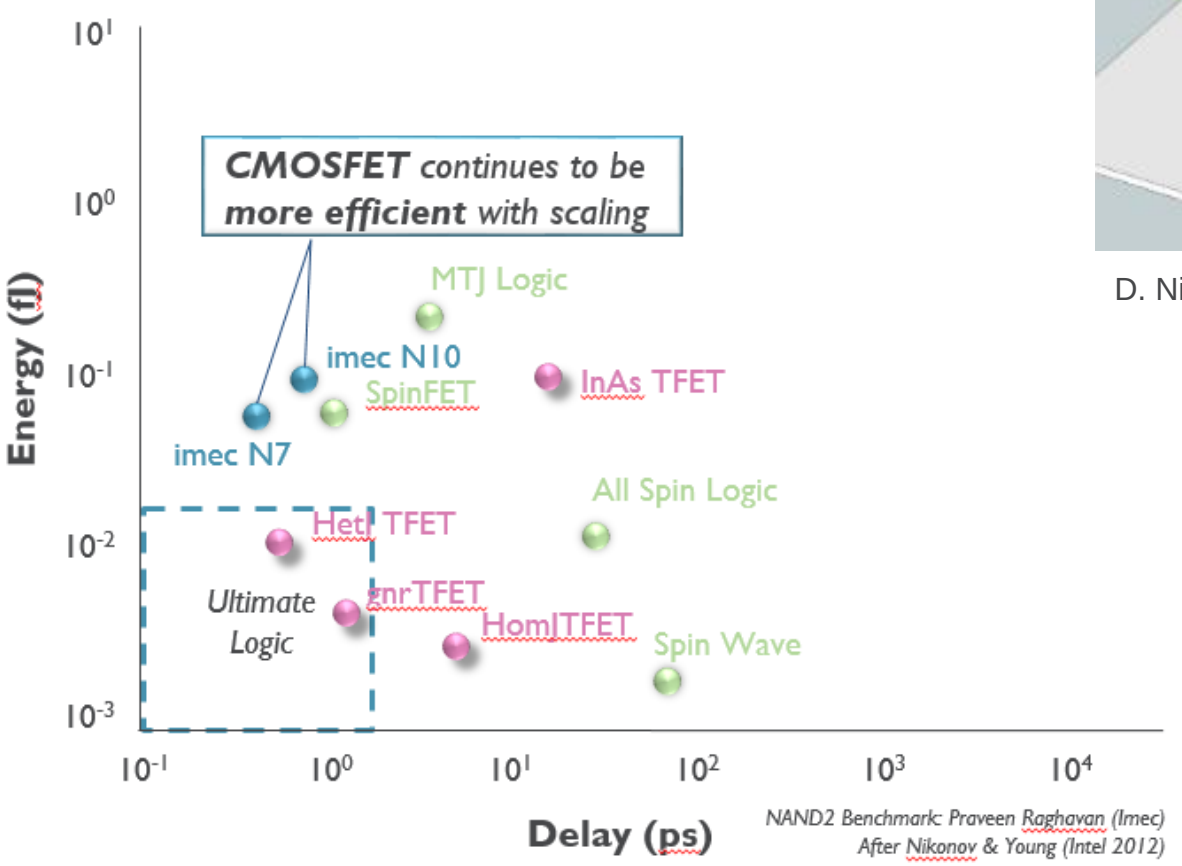




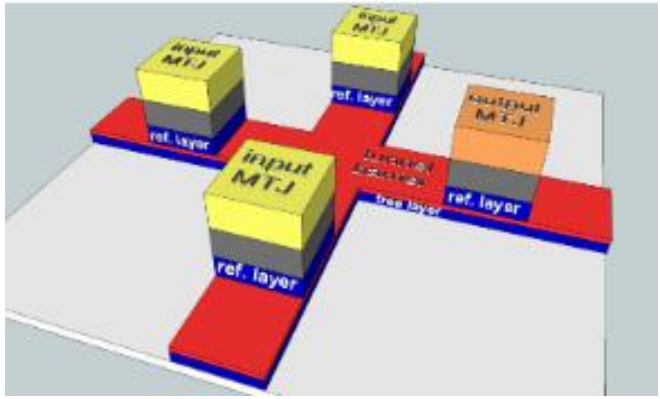
- Sub 60mV/dec due to negative capacitance of a ferroelectric oxide based gate stack (m < 1)
- Tunable hysteresis behavior: non-volatile circuits and noise immune logic

Spin logic

Spin based devices offer different Energy-Delay tradeoffs

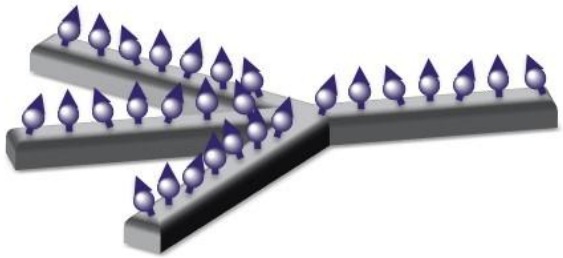


Spin torque majority gate



D. Nikonov et al., IEEE EDL, 2011.

Spin wave devices



Summary

Summary

- Need for more energy-efficient Core Logic Devices and specialty devices
- Lateral NW is a natural evolution from FinFET and will enable to continue scaling beyond 7nm due to improved electrostatics
- VFET offers 30-40% SRAM area benefit: 1st step towards vertical logic?
- Scaling of supply voltage is required to address power crisis and higher mobility channels are needed to increase performance at reduced V_{DD}
- New switching mechanisms like TFET, NCFET and spin logic being considered for ultra-low power applications