Chapter

24

Operational Amplifiers I

The operational amplifier (op-amp) is a fundamental building block in analog integrated circuit design. A block diagram of the two-stage op-amp with output buffer is shown in Fig. 24.1. The first stage of an op-amp is a differential amplifier. This is followed by another gain stage, such as a common source stage, and finally by an output buffer. If the op-amp is intended to drive a small purely capacitive load, which is the case in many switched capacitor or data conversion applications, the output buffer is not used. If the op-amp is used to drive a resistive load or a large capacitive load (or a combination of both), the output buffer is used.

Design of the op-amp consists of determining the specifications, selecting device sizes and biasing conditions, compensating the op-amp for stability, simulating and characterizing the op-amp A_{OL} (open-loop gain), CMR (common-mode range on the input), CMRR (common-mode rejection ratio), PSRR (power supply rejection ratio), output voltage range, current sourcing/sinking capability, and power dissipation.

We'll start this chapter off with a very simple two-stage op-amp (without an output buffer). By pointing out the weaknesses with this two-stage topology, we'll set the stage for developing practical op-amps in the rest of the chapter.

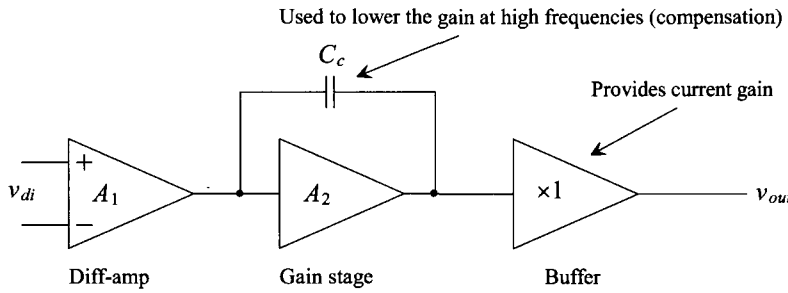


Figure 24.1 Block diagram of two-stage op-amp with output buffer.

24.1 The Two-Stage Op-Amp

Figure 24.2 shows the basic two stage op-amp made using an NMOS diff-amp and a PMOS common-source amplifier (M7). As seen in Fig. 22.8 M7 is biased to have the same current as M3 and M4 (10 μA from Table 9.2). Note also the addition of the compensating network consisting of a compensation capacitor, C_c, (*Miller compensation*) and a zero-nulling resistor R_z (see Figs. 21.25 and 21.33 along with the associated discussion). Because the op-amp doesn't have an output buffer, it is limited to driving capacitive loads and very large resistances (comparable to the output resistance of a MOSFET, that is, megaohms).

Low-Frequency, Open Loop Gain, A_{OLDC}

The low-frequency, open loop gain of the op-amp is calculated as the product of each stage gain, that is,

$$A_{OLDC} = A_1 \cdot A_2 = \overbrace{g_{mn} \cdot (r_{on} || r_{op})}^{A_1 = \text{diff-amp's gain}} \cdot \overbrace{g_{mp} \cdot r_{op}}^{A_2, \text{ M7's gain}} \tag{24.1}$$

where the output resistance of the cascode current source load, M8, is assumed to be much larger than the M7 output resistance, r_{op}. Using the values from Table 9.2, we get an A_{OLDC} of 832 *V/V*.

Input Common-Mode Range

The minimum input common-mode voltage is given by Eq. (22.11) or 450 mV. The maximum input common-mode voltage is given by Eq. (22.12) or 930 mV. This means, for proper operation of our two-stage op-amp, the input voltages (v_p and v_m) should fall within the range of 450 to 930 mV. If they go outside this range, the op-amp gain drops, and it is likely that the circuit employing the op-amp will not function properly. Figure 24.3 shows a SPICE DC sweep where the *inverting* input (v_m) is held at 500 mV and the *noninverting* input (v_p) is swept from 495 to 505 mV. The slope of this transfer curve is the DC open-loop gain of the op-amp, A_{OLDC}.

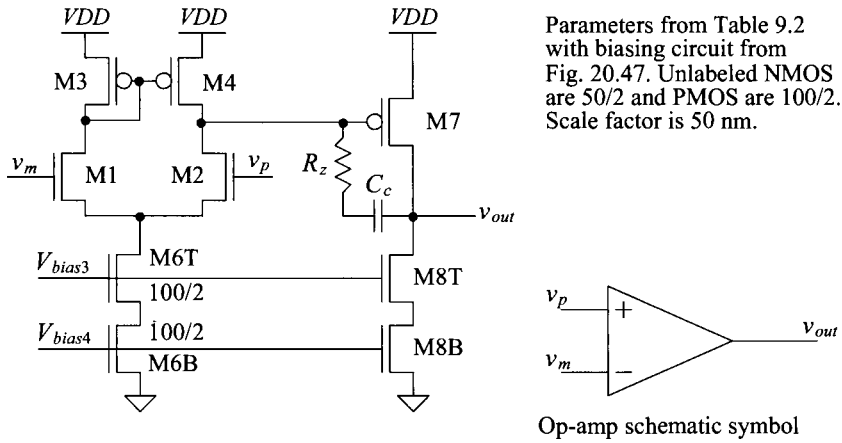


Figure 24.2 Basic two-stage op-amp.

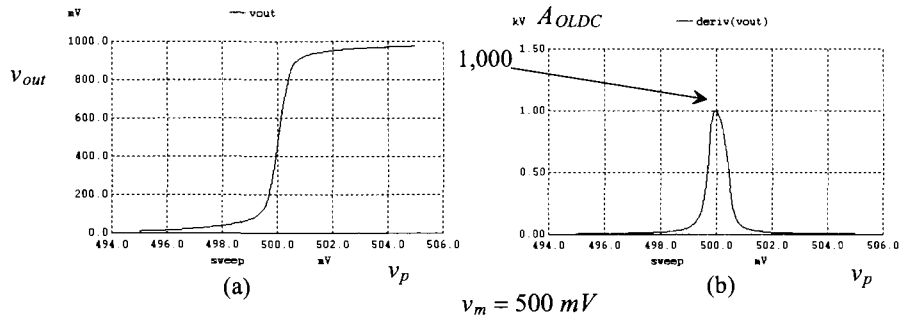


Figure 24.3 (a) DC transfer curves for the op-amp in Fig. 24.2 and (b) its gain (the derivation of (a)).

Power Dissipation

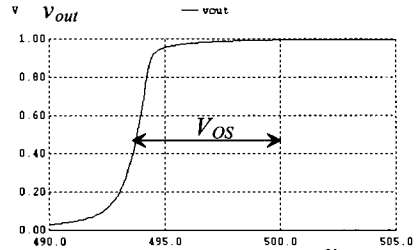
To determine the power dissipated by the op-amp, we sum the currents supplied by the constant current sources and multiply the result by *VDD*. For the op-amp in Fig. 24.2, the current through M6 is 20 μA and the current through M8 is 10 μA. The total power dissipation is then 30 μW (*VDD* = 1 *V*).

Output Swing and Current Sourcing/Sinking Capability

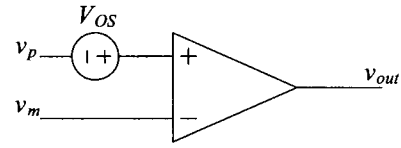
The maximum output swing (for the op-amp in Fig. 24.2) is limited by M7 going into the triode region. If we must keep at least 100 mV across M7, then the maximum output voltage is 900 mV. When M8 goes into triode or roughly 100 mV (see Fig. 20.48), the minimum output voltage is set. As seen in Fig. 24.3a, the high-gain (or large slope) region falls between v_{out} of 100 and 900 mV. Note that the maximum amount of current that this op-amp can sink is limited by the constant current sink M8 or 10 μA. The op-amp can source considerably more than 10 μA by pulling the gate of M7 downwards. Because this topology can source a considerable amount of current, it is useful as a voltage regulator (because the op-amp is always only sourcing current in a voltage regulator application).

Offsets

We've talked in great length (earlier in the book) about random offsets and how to design and layout circuits to minimize their effects. Another type of offset (that is not random) is termed a *systematic offset*. When we sized the MOSFETs in Fig. 24.2, for example, we made sure that M7 was sized to source 10 μA and M8 was sized to sink 10 μA. What would happen if we sized M7 to source 100 μA of current instead (changed its size from 100/2 to 1000/2)? Because M8 is a constant bias of 10 μA, M7 would move into the triode region until it was sourcing the 10 μA of current that M8 wants to sink. The output voltage would be very close to *VDD* with M7 in the triode region. Effectively we would get a shift or offset in the transfer curves seen in Fig. 24.3a (see Fig. 24.4a). To model this output voltage shift, we can refer it back to the op-amp input as an input-referred offset voltage, Fig. 24.4b. Note that unlike a random offset, which may be positive or negative in value, a systematic offset will always be a known polarity. Finally, note that while we chose to model the offset in series with the noninverting input terminal, in Fig. 24.4, we could just as easily have placed it in series with the inverting op-amp terminal (with a change in polarity).



(a)



(b) How the offset is modeled

$v_m = 500\ mV$

Figure 24.4 Showing how increasing M7's width to 1000 in Fig. 24.2 causes an input-referred (systematic) offset voltage.

Compensating the Op-Amp

An important step in op-amp design is the design of the compensation network. The op-amp takes the difference between the inverting and noninverting input terminal voltages and, ideally, multiplies the result by a very large number (the gain). A block diagram representation of an op-amp is seen in Fig. 24.5. The open-loop gain as a function of frequency is labeled $A_{OL}(f)$.

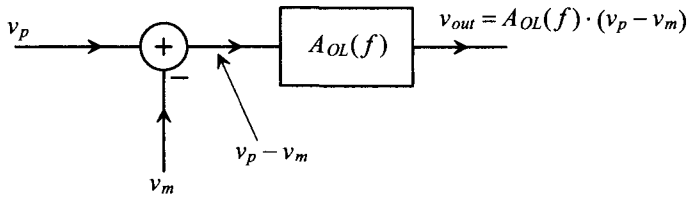


Figure 24.5 Block level diagram of an op-amp.

In all practical situations, the op-amp is used with feedback, Fig. 24.6. While our op-amp in Fig. 24.2 cannot drive a resistive load (unless it is megaohms, as a resistor on the op-amp output will kill the gain of the second stage), we'll still use this figure (Fig. 24.6) to illustrate the concept of feedback and compensation. We can write

$$v_{out} = A_{OL}(f) \cdot (v_{in} - v_f) \tag{24.2}$$

and

$$v_f = v_{out} \cdot \frac{R_2}{R_1 + R_2} \tag{24.3}$$

The amount of the output that is fed back is often called the feedback factor β or

$$\beta = \frac{R_2}{R_1 + R_2} \tag{24.4}$$

Substituting Eqs. (24.3) and (24.4) into Eq. (24.2) and solving for the closed loop gain gives

$$A_{CL}(f) = \frac{v_{out}}{v_{in}} = \frac{A_{OL}(f)}{1 + \beta \cdot A_{OL}(f)} \tag{24.5}$$

If we take $A_{OL}(f) \to \infty$, then the closed loop gain of this non-inverting topology is

$$A_{CL}(f) \to \frac{1}{\beta} = 1 + \frac{R_1}{R_2} \tag{24.6}$$

We have several important points that we need to discuss. To begin, notice that in Eq. (24.5) if

$$\beta \cdot A_{OL}(f) = -1 \tag{24.7}$$

or more precisely

$$|\beta \cdot A_{OL}(f)| = 1 \text{ and } \angle\beta \cdot A_{OL}(f) = \pm 180^\circ \tag{24.8}$$

the closed loop gain blows up (the feedback amplifier becomes unstable). The worst case situation (the largest value of β) occurs when all of the output is fed back to the op-amp input (assuming no transformer, amplifier, etc. in the feedback path). The voltage follower, Fig. 24.7, is an example of this situation. *To determine the stability of an op-amp, we'll look at the open loop gain when the feedback factor is one, that is,*

$$|A_{OL}(f)| = 1 \text{ and } \angle A_{OL}(f) = 180^\circ \tag{24.9}$$

Notice that the larger the closed loop gain, the smaller the value of β (the less output signal we feed back) and the more likely the op-amp circuit, with feedback, will be stable. *This is important.* While feedback helps to desensitize an amplifier's gain to variations in an op-amp's A_{OL}, the drawback is stability. In a high-performance op-amp that will never operate in a unity-follower configuration, we can get an enhancement in speed by reducing the amount of compensation (the amount of the reduction guided by Eq. (24.8) with the actual value of β used). While this discussion has focused on the non-inverting topology (voltage or series-shunt amplifiers, $\beta = v_f/v_{out}$) a similar discussion can be given for the inverting amplifier (shunt-shunt where $\beta = i_f/v_{out}$) topology, see Sec. 30.2.

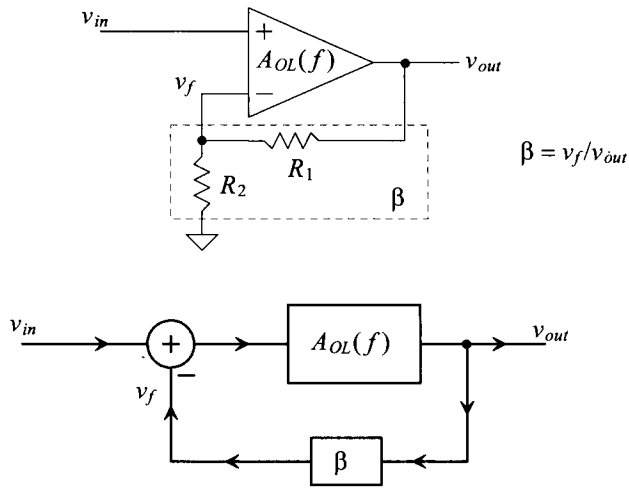


Figure 24.6 An example of feedback in an op-amp, see Sec. 30.2 for additional discussion.

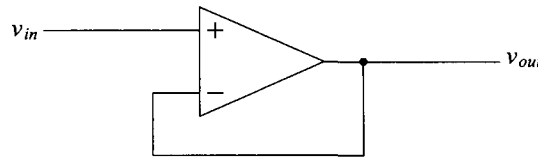


Figure 24.7 Voltage follower configuration, an example of a closed-loop amplifier with unity feedback factor.

To estimate the open-loop frequency response of the op-amp, let's use the generic model seen in Fig. 21.25. Figure 24.8 shows the location of nodes 1 and 2 on our two-stage op-amp. We've included a load capacitance in this figure. With the help of Table 9.2 we can write

$$R_1 = r_{on} || r_{op} = 111\ k\Omega$$

$$R_2 = r_{op} || R_{ocasn} \approx r_{op} = 333\ k\Omega$$

$$g_{m1} = g_{mn} = 150\ \mu A/V \text{ (diff-amp)}$$

$$g_{m2} = g_{mp} = 150\ \mu A/V \text{ (common-source)}$$

$$C_1 = C_{dg4} + C_{gd2} + C_{gs7} = 13.6\ fF$$

$$C_2 = C_L + C_{gd8} \approx C_L + 1.56\ fF$$

Let's calculate the open-loop response with a load and compensation capacitance of 100 fF, that is, $C_L = C_c = 100\ fF$. The pole associated with node 1, from Eq. (21.65), is

$$f_1 \approx \frac{1}{2\pi g_{m2} R_1 R_2 C_c} = 287\ kHz$$

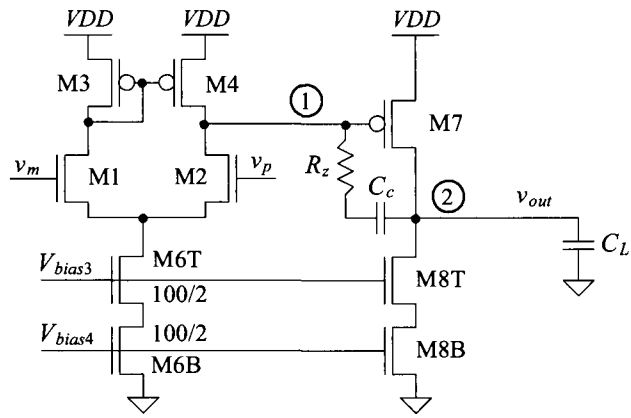


Figure 24.8 Calculating the frequency response of the op-amp.

The location of the pole associated with the output node (node 2) is, from Eq. (21.66),

$$f_2 = \frac{g_{m2}C_c}{2\pi(C_cC_1 + C_1C_2 + C_cC_2)} = 210\ MHz$$

The location of the zero, f_z in Eq. (21.63), is at 240 MHz (very near the second pole).

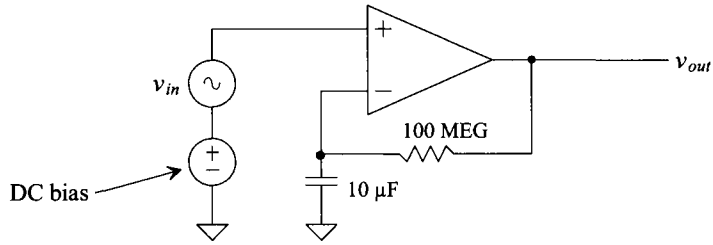


Figure 24.9 Circuit configuration used to simulate open-loop frequency response.

To simulate the open-loop response of the op-amp, we can use the configuration seen in Fig. 24.9. The feedback resistor and capacitor form a time constant so large that for all intents and purposes none of the AC output voltage is fed back to the inverting input. However, the DC bias level is fed back so that the op-amp biases up correctly (all MOSFETs are operating in the saturation region). With a DC bias voltage of 500 mV, Fig. 24.10 shows the open loop responses of the op-amp in Fig. 24.8 with 100 fF compensation capacitance and load capacitance. The simulated values are close to the

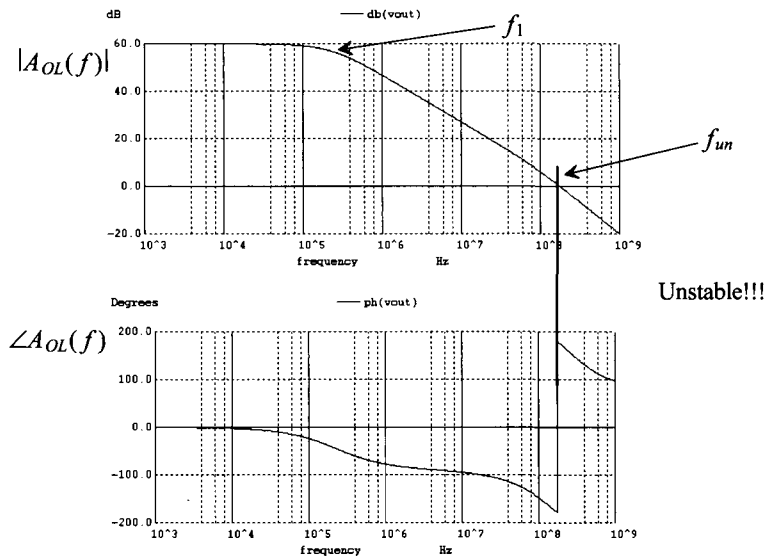


Figure 24.10 The open-loop frequency response of the op-amp in Fig. 24.8 with a 100 fF compensation capacitance and load capacitance.

hand-calculated values given above. However, from the criteria given in Eq. (24.9), the op-amp will clearly be unstable. *We want the open loop gain of the op-amp to be much less than one when the phase shift is 180°.* Looking at Fig. 24.10, we effectively want to shift the lower frequency pole (f_1) downwards in frequency. At the same time, we want to move the higher frequency pole, f_2 , higher in frequency (we want to *split the poles*). Remember this (pole-splitting) was the point of adding the compensation capacitor to an amplifier back in Ch. 21. Let's use Eq. (21.72) to select C_c. Looking at Fig. 24.10, we see that the phase shift is −100° at 10 MHz, so let's set the unity gain frequency to this value (in an attempt to make sure that the open loop gain is well under one when the phase shift is 180°).

$$f_{un} = \frac{g_{m1}}{2\pi C_c} = \frac{150\ \mu A/V}{2\pi \cdot C_c} = 10\ MHz \rightarrow C_c = 2.4\ pF \qquad (24.10)$$

The simulation results are seen Fig. 24.11. The unity-gain frequency, f_{un} , is close to 10 MHz. However, while the lower frequency moved downwards and the higher frequency pole moved upwards, the zero moved down to unity-gain frequency, see Eq. (21.63). This causes the open-loop gain to hover around unity instead of continuing to decrease (this is bad). The stability and step response of the op-amp will be degraded because of the zero. To illustrate this, consider the simulation results seen in Fig. 24.12. Notice that, in a transient simulation, we have to wait some time to let the bias circuit start up. Here, in this simulation, we've waited 500 ns before applying the input signal. Next, notice that our step input signal has a small amplitude change (5 mV). If we apply a larger step, the small-signal analysis used to derive pole-splitting is no longer valid (and we'll see the slew-rate limitations). Clearly the output of the op-amp doesn't behave well with the zero present. To eliminate the zero, we add the zero-nulling resistor, as seen in Fig. 21.33b. Figure 24.11 is regenerated in Fig. 24.13 with the addition of a zero-nulling resistor ($1/g_{mn}$ = 6.5k). Figure 24.14 shows the well-behaved step response.

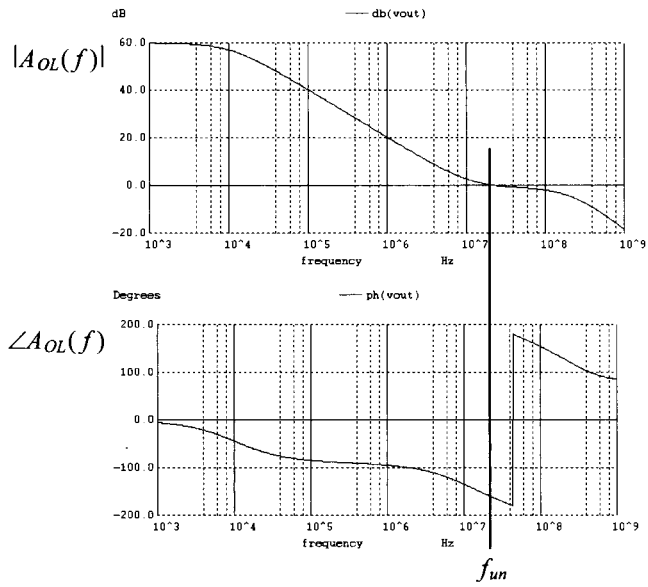


Figure 24.11 Increasing the compensation capacitor's value to 2.4 pF.

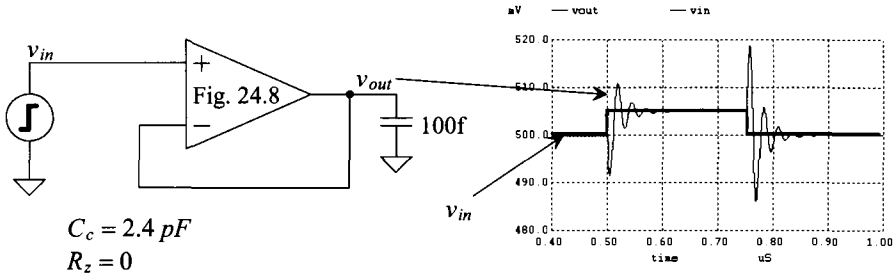


Figure 24.12 The poor step response of the op-amp with the zero present.

Gain and Phase Margins

In the previous discussions we assumed a load of 100 fF. If the load capacitance varies, the stability can (will) be affected. Further, with temperature, process, and power supply variations, the stability of the op-amp can change. In order to specify "how stable" the op-amp is at a given set of operating conditions, the parameters gain margin (GM) and phase margin (PM) are used. To determine an op-amp's PM, we look at the phase shift when the open-loop gain is unity. The amount of phase shift away from 180° is the PM of the op-amp. As seen in Fig. 24.13, the phase shift when the gain is unity is –90°. Taking the difference between this value and 180° gives a PM of 90°. To calculate the GM, we look at the difference between the open-loop gain and unity when the phase of the op-amp is ±180°. For the op-amp response in Fig. 24.13, the GM is approximately 25 dB. Note that as seen in Fig. 24.14, it is nice to have a PM of 90° because the step response of the op-amp has a first-order response (like an RC circuit).

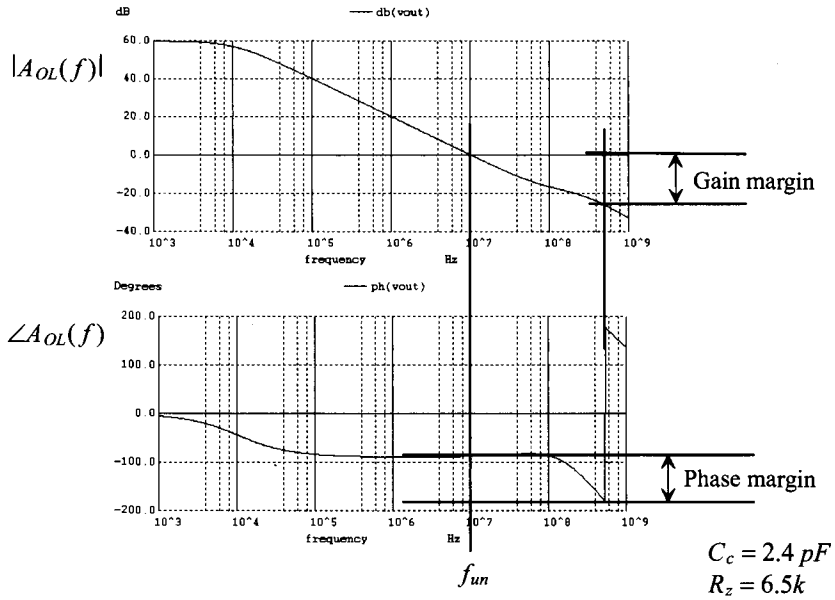


Figure 24.13 Adding a zero nulling resistor to the op-amp in Fig. 24.8.

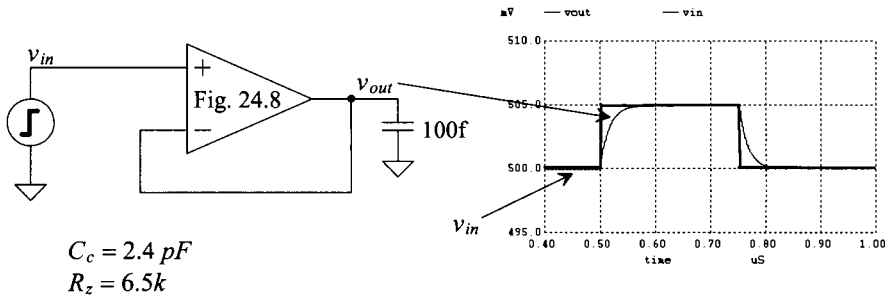


Figure 24.14 Good step response of the op-amp with the zero absent.

Removing the Zero

As the previous discussion illustrated, the RHP zero can raise issues concerning stability and settling time (this is important). As seen in Eq. (21.73) and the associated discussion, R_z can be added to eliminate ($R_z = 1/g_{m1}$) or move the zero into the LHP ($R_z > 1/g_{m1}$). When the zero is moved to the LHP, the phase response of the zero adds to the overall phase response, increasing the PM (this is called *lead compensation*). The practical problem with using R_z is that setting its value to a precise number (say $1/g_{m1}$) is challenging with shifts in process, temperature, or voltage. One solution to this problem is to replace the resistor with a MOSFET operating in the triode region, Fig. 24.15. Mz behaves like a resistor with a value of $1/g_{m1}$. Ideally, the source-gate voltage of M7 is the same as the V_{SG} of MP1. It then follows that the source-gate potential of MP2 equals the source-gate potential of Mz. The channel resistance of Mz is then, from Eq. (9.16), set to $1/g_{m1}$. The practical issues with this method are the wasted power dissipated by the additional circuitry and the fact that if the output swing becomes large (especially at higher frequencies where C_c has a small impedance), Mz can move out of the triode region, which can affect the large-signal behavior of the op-amp.

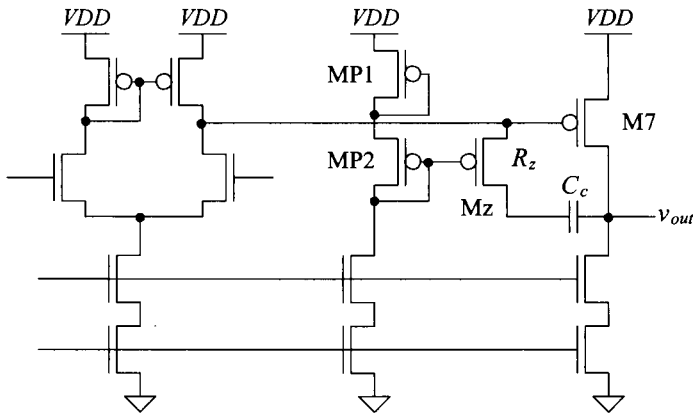


Figure 24.15 Making the zero-nulling resistor process independent.

The other method to remove the RHP zero seen in Fig. 21.33a is to add an amplifier with a gain of +1 in series with the compensation capacitor. Figure 24.16 shows the idea. A source follower allows the output signal to feed back through the compensation capacitor (so that the pole-splitting effect is still present). However, the root cause of the RHP zero, namely, C_c shorting the input of the second stage (the output of the diff-amp) to the output of the second stage (the output of the op-amp) at higher frequencies is removed. The concerns with this topology are, again, power dissipation and, perhaps more importantly, large signals. If the overall output voltage swings too low, it causes the source-follower to shut off.

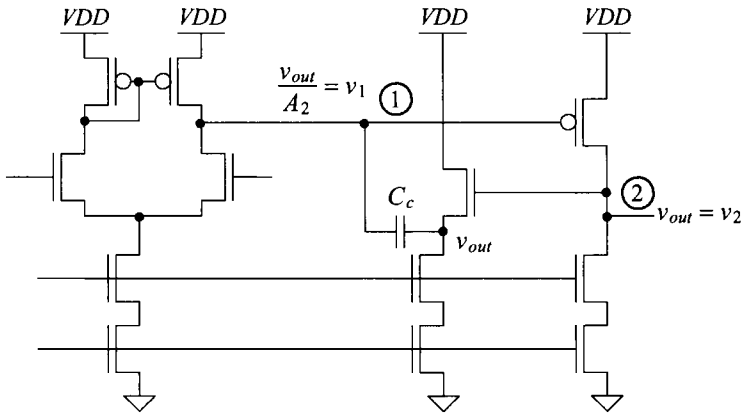


Figure 24.16 Using an amplifier to eliminate forward signal feedthrough via the compensation capacitor.

Compensation for High-Speed Operation

Notice, in Fig. 24.16 (or in any other of the topologies we've discussed up to this point), that the current fed back through C_c is

$$i_{Cc} = \frac{v_{out} - \frac{v_{out}}{A_2}}{1/j\omega C_c} \tag{24.11}$$

If the second-stage gain, A_2 ($g_{m2}R_2 = g_{m7}r_{o7}$) is reasonably large, then this equation can be approximated using

$$i_{Cc} \approx \frac{v_{out}}{1/j\omega C_c} \tag{24.12}$$

If we can feed back this current *indirectly* to the output of the diff-amp, we can still compensate the op-amp (and have pole-splitting). Further, if we do it correctly, we avoid connecting the compensation capacitor directly to the output of the diff-amp and thus avoid the RHP zero. Towards this goal, consider the modified op-amp schematic seen in Fig. 24.17. The added MOSFETs form a common-gate amplifier. (Note that here we are assuming $v_p << v_{out}$, so the source-follower action of MCG is negligible. MCG is connected to v_p to set its gate at the DC voltage of the input.) The current i_{Cc} is fed back through the common-gate MOSFET, MCG, to node 1 (the output of the diff-amp).

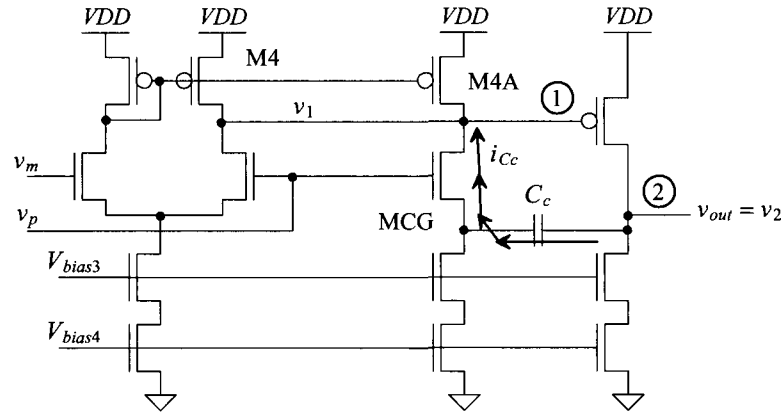


Figure 24.17 Feeding back a current indirectly to avoid the RHP zero.

To determine the frequency response of this amplifier, consider the model seen in Fig. 24.18 (modified from Fig. 21.25). Summing the currents at node 1 gives

$$-g_{m1}v_s + \frac{v_1}{R_1 \| \frac{1}{j\omega C_1}} - \overbrace{\frac{v_{out}}{1/j\omega C_c + 1/g_{mcg}}}^{i_{Cc}} = 0 \qquad (24.13)$$

where the resistance looking into the source of MCG is $1/g_{mcg}$. Solving for v_1 gives

$$v_1 = \frac{g_{m1}R_1}{1+j\omega R_1 C_1} \cdot \left(\frac{j\omega \frac{C_c}{g_{m1}}}{1+j\omega \frac{C_c}{g_{mcg}}} \cdot v_{out} + v_s \right) \qquad (24.14)$$

For the output node (node 2), we can write (noting that now C_2 includes both C_c and C_L)

$$v_{out} = -g_{m2}v_1 \cdot \left(\frac{R_2}{1+j\omega R_2 C_2} \right) \qquad (24.15)$$

Plugging Eq. (24.14) into this equation gives

$$v_{out} = -g_{m1}R_1 g_{m2}R_2 \cdot \frac{\frac{j\omega \frac{C_c}{g_{m1}}}{1+j\omega \frac{C_c}{g_{mcg}}} \cdot v_{out} + v_s}{(1+j\omega R_1 C_1)(1+j\omega R_2 C_2)} \qquad (24.16)$$

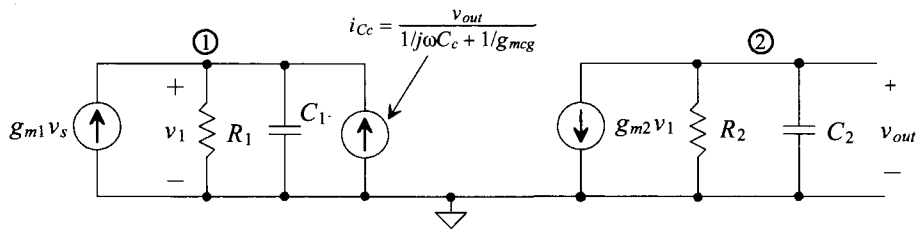


Figure 24.18 Model used to estimate bandwidth when indirect feedback current is used.

Letting

$$K = \frac{-g_{m1}R_1 g_{m2}R_2}{(1+j\omega R_1 C_1)(1+j\omega R_2 C_2)} \tag{24.17}$$

we can rewrite Eq. (24.16) as

$$v_{out} = \frac{j\omega\frac{C_c}{g_{m1}}}{1+j\omega\frac{C_c}{g_{mcg}}} \cdot K \cdot v_{out} + K \cdot v_s \tag{24.18}$$

and, assuming $|K \cdot \frac{C_c}{g_{m1}}| >> \frac{C_c}{g_{mcg}}$, thus

$$\frac{v_{out}}{v_s} \approx \frac{K \cdot \left(1+j\omega\frac{C_c}{g_{mcg}}\right)}{1-j\omega\frac{C_c K}{g_{m1}}} \tag{24.19}$$

Resubstituting in K gives

$$\frac{v_{out}}{v_s} = \frac{-g_{m1}R_1 g_{m2}R_2\left(1+j\omega\frac{C_c}{g_{mcg}}\right)}{(1+j\omega R_1 C_1)(1+j\omega R_2 C_2)+j\omega\frac{C_c}{g_{m1}} \cdot g_{m1}R_1 g_{m2}R_2} \tag{24.20}$$

or, with $s = j\omega$, we can write

$$\frac{v_{out}}{v_s} = \frac{-g_{m1}R_1 g_{m2}R_2\left(1+s\frac{C_c}{g_{mcg}}\right)}{s^2 \cdot (R_1 C_1 R_2 C_2)+s \cdot (R_1 C_1 + R_2 C_2 + R_1 g_{m2} R_2 C_c)+1} \tag{24.21}$$

Notice there is a LHP zero at

$$f_z = \frac{g_{mcg}}{2\pi C_c} \tag{24.22}$$

Since this zero is in the LHP, it will add to the phase response and enhance the speed of the op-amp. Intuitively, we can think that at high speeds the phase shift through C_c will cause the output signal to feed back and add to the signal at node 1. This *positive feedback* enhances the speed of the op-amp. To determine the location of the second pole, let's assume $R_1 g_{m2} R_2 C_c >> R_1 C_1$ or $R_2 C_2$ or $R_1 C_1 R_2 C_2$ so

$$s_{1,2} \approx \frac{-R_1 g_{m2} R_2 C_c \pm R_1 g_{m2} R_2 C_c}{2(R_1 C_1 R_2 C_2)} \tag{24.23}$$

Our approximation won't tell us the location of the lower frequency pole (it's given by Eq. (21.65)). The location of the second pole is

$$f_2 \approx \frac{g_{m2}C_c}{2\pi \cdot C_1 C_2} \approx \frac{g_{m2}C_c}{2\pi \cdot C_1(C_L + C_c)} \tag{24.24}$$

This result should be compared to Eq. (21.66). The location of the second pole is at a considerably higher frequency using this technique. *The result is that we can set the unity gain frequency to a higher value and still have a stable op-amp.* Further, the load capacitance (which is included in C_2) can be considerably larger for a given PM or GM. Again, Eq. (21.72) can be used to set the unity-gain frequency, f_{un}, assuming $f_2 \approx f_z$

$$f_{un} = \frac{g_{m1}}{2\pi C_c} \ (\approx f_z \ \text{if} \ g_{m1} \approx g_{mcg}) \tag{24.25}$$

Using the *indirect compensation* method seen in Fig. 24.17 in the op-amp of Fig. 24.8 with C_c = 240 *fF* (f_{un} = 100 MHz) gives the results seen in Fig. 24.19. The small-signal step response is seen in Fig. 24.20. This response should be compared to Figs. (24.12) and (24.14).

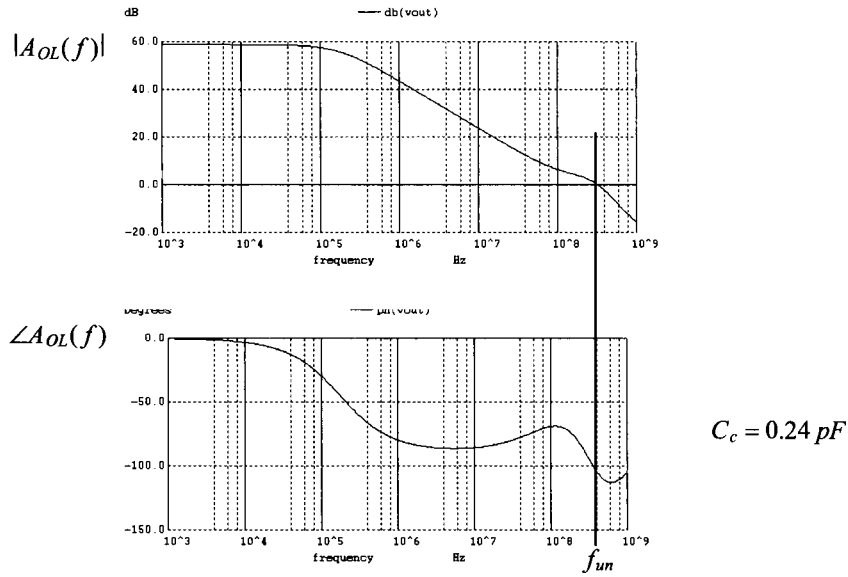


Figure 24.19 Simulating the op-amp of Fig. 24.8 using the indirect compensation scheme seen in Fig. 24.17 with a compensation capacitor of 240 fF.

The indirect feedback of the current through the compensation capacitor results in faster op-amp circuits and less layout area (the compensation capacitor generally dominates the layout area of an op-amp). However, the added circuit in Fig. 24.17 dissipates more power. To eliminate the additional power dissipation, consider the op-amp topology seen in Fig. 24.21. Here we've used the fact that a 100/2 PMOS device can be laid out as two 100/1 PMOS in series (see also Fig. 20.35). The current through the compensation capacitor is fed back through M4B to the output of the diff-amp. Note how we've also split M7 into two devices. It's important, for small offsets, to try to match both the drain-source and the gate-source voltages of the MOSFETs used in the op-amp. The step-response of the op-amp is seen in Fig. 24.22.

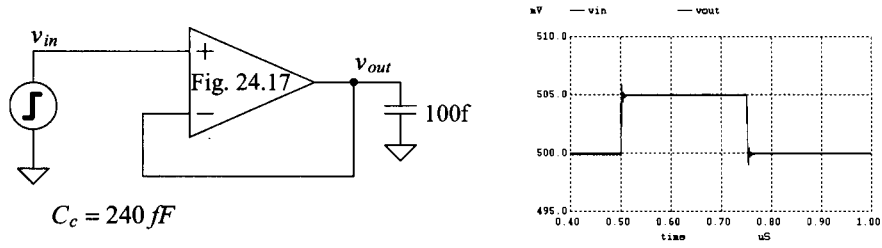


Figure 24.20 The step response of the op-amp in Fig. 24.17 with frequency response seen in Fig. 24.19.

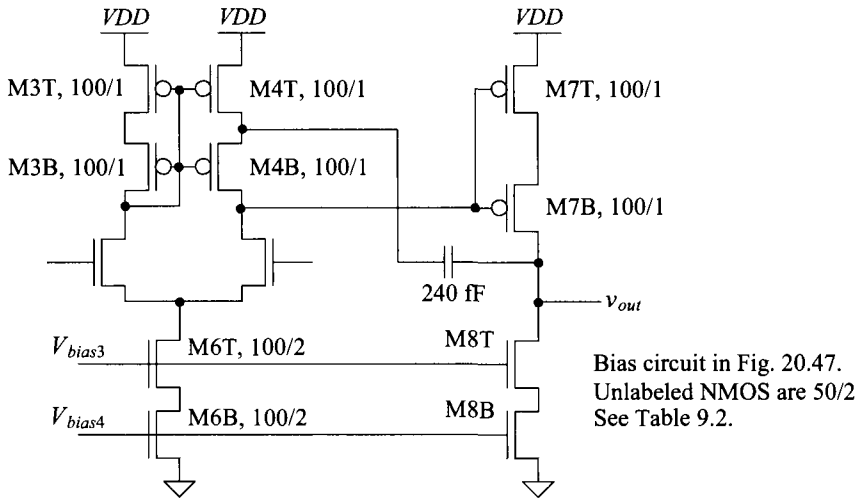


Figure 24.21 Implementing indirect feedback compensation without additional power dissipation in a two-stage op-amp.

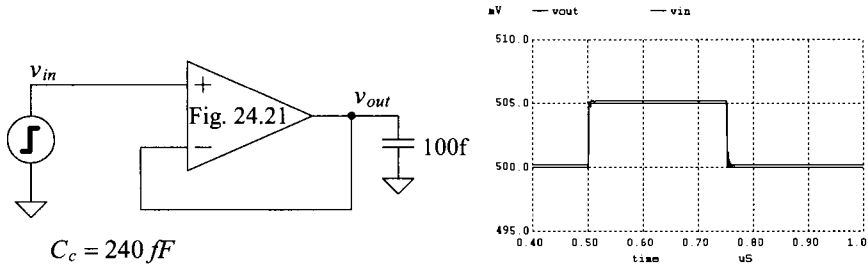


Figure 24.22 The step response of the op-amp in Fig. 24.21 driving 100 fF.

Slew-Rate Limitations

When we talked about step response, we limited the amplitude of the signals to small steps (5 mV) to avoid slew-rate limitations. Let's take the op-amp from Fig. 24.8 and put it in the configuration seen in Fig. 24.14, driving a 1 pF load capacitance. Further, let's increase the input pulse amplitude to (close to) the maximum allowable range, that is, from 500 mV to 900 mV (limited by the op-amp's input common-mode range). The simulated results are seen in Fig. 24.23. Referring to Fig. 24.8, notice that when the op-amp's noninverting input terminal (v_p) is driven high, M2 turns on and pulls the gate of M7 down. Since there isn't a current source in series with M7, it can quickly charge the 1 pF load capacitance. The only large-signal limitation is the bias current of the diff-amp, I_{SS} (= 20 μA here), charging C_c (= 2.4 pF here). This limits the output rate of change since any variation in v_{out} causes a displacement current through C_c, which must be sourced/sunk by the diff-amp. This slew-rate limitation is calculated as 20 μA/2.4 pF or 8.3 mV/ns. The change in the output voltage is 400 mV, so we would require roughly 50 ns to change the voltage across C_c.

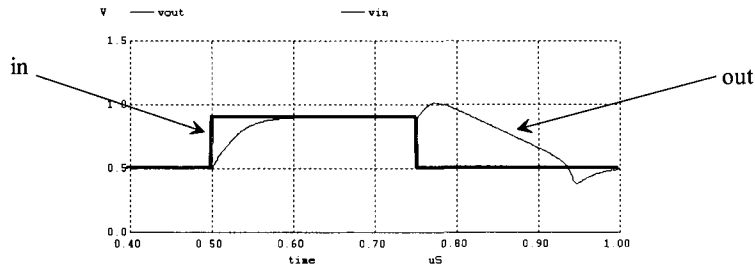


Figure 24.23 The large-signal (500 mV to 900 mV) performance of the op-amp in Fig. 24.8 with C_c = 2.4 pF and R_z = 6.5 k driving a 1pF load. The low-to-high settling time is roughly 100 ns, while the high-to-low settling time, which is slew-rate limited, is roughly 500 ns.

The more interesting behavior occurs when the input signal drops from 900 mV to 500 mV. This causes M2 to shut off, allowing all of the current from M4 to charge the gate of M7. The result is a positive pulse on the gate of M7 that feeds directly to the output through the compensation capacitor (this is bad, and it is another example of why it is desirable to use the indirect compensation method). This pulse accounts for the (unwanted) positive movement in the output voltage seen in Fig. 24.23 just after the input pulse transitions negative. Now the load capacitor and the compensation capacitor must both be discharged through the constant current source M8. The output slew-rate is estimated by how fast this constant current (here 10 μA) can discharge 3.4 pF (the sum of the compensation capacitor and the load capacitor). This rate is calculated as (roughly) 3 mV/ns. For the output to transition 400 mV requires 133 ns (this time will be longer because of the positive movement in the output voltage just after the input switches). Note that we might think that simply by sizing up the current conducting in M8 we can enhance the op-amp's slew-rate. This is true to the point where the diff-amp's current charging the compensation capacitor becomes the limiting factor.

Finally, note how the output voltage shoots past the final (desired) voltage level of 500 mV. This is because the gate of M7 is pulled to *VDD* to shut it off when slewing is taking place (both M4 and M7 are shut off because of this). When the inputs of the op-amp move to the same value (500 mV here), the gate of M7 must be pulled downwards to the quiescent value. The time it takes for this to happen results in the undershoot in the op-amp's output voltage seen in Fig. 24.23.

The same test setup used to generate the data in Fig. 24.23 is also used to generate the data in Fig. 24.24 except that here the op-amp in Fig. 24.21 is used. Note the compressed time scale. The settling time for the low-to-high transition is now 10 ns, while the high-to-low transition time is 60 ns. We would expect much faster settling because the compensation capacitor is now ten times smaller than the value used in the op-amp of Fig. 24.8. Again, the settling time is limited by how fast M8 can discharge the load capacitance and the compensation capacitance. This can be estimated as 10 μA/1.24 pF or 8 mV/ns. It takes 50 ns for the output to transition 400 mV. The size of M8 can be increased to meet a specific load capacitance and settling time requirement.

Because of the improved speed performance, smaller layout area, and (as we'll see) better power supply noise rejection, we'll use indirect compensation in place of Miller compensation in the remaining two-stage op-amps that we discuss in this book.

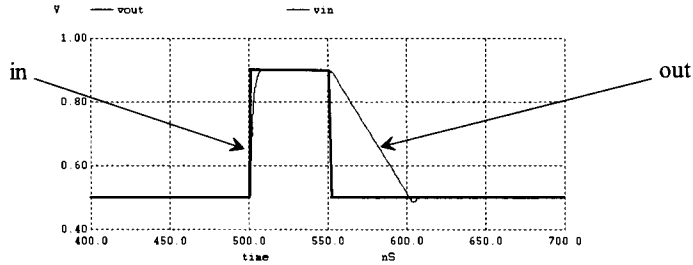


Figure 24.24 The large-signal (500 mV to 900 mV) performance of the op-amp in Fig. 24.21 with C_c = 0.24 pF driving a 1 pF load. The low-to-high settling time is roughly 10 ns, while the high-to-low settling time, which is slew-rate limited, is roughly 60 ns. Note the different time scale when compared to Fig. 24.23.

Common-Mode Rejection Ratio (CMRR)

The *CMRR* of an op-amp is calculated in the same way as the diff-amp in Sec. 22.1.3. The common-mode gain of the diff-amp is A_c. The common-mode gain of the op-amp is $A_c A_2$. The differential gain of the op-amp is $A_{OL}(f) = A_d \cdot A_2$ (where $A_d = A_1$). The *CMRR* of an op-amp in dB is given by

$$CMRR = 20 \cdot \log \left| \frac{A_{OL}(f)}{A_c \cdot A_2} \right| = 20 \cdot \log \left| \frac{A_d}{A_c} \right| \qquad (24.26)$$

which shows that the op-amp *CMRR* is determined by the differential stage. Simulating the *CMRR* of an op-amp can be accomplished with the circuits seen in Fig. 24.25. For the op-amps discussed so far in this chapter, the *CMRR* is approximately 50 dB (see Ex. 22.7, where the common-mode voltage is 500 mV). We can think of A_c as the open-loop gain of the op-amp for common-mode signals. If the applied differential voltage is zero, and we change the common-mode voltage by ΔV_c, then the output voltage will change by ΔV_o

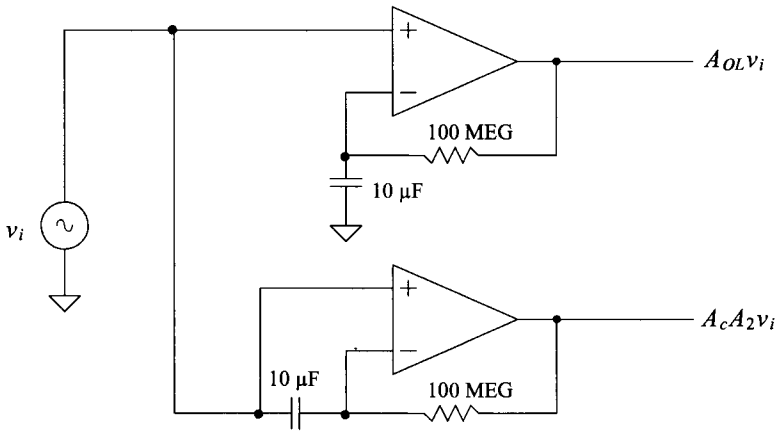


Figure 24.25 Circuit configuration used to simulate CMRR.

$= A_{cm} \cdot \Delta V_c$ (see Fig. 22.17). To compensate for the change in the output voltage, a nonzero input differential voltage develops on the input of the op-amp (an offset voltage that is a function of the common-mode voltage). This offset voltage can be estimated by

$$\Delta V_{OS} = \frac{\Delta V_o}{A_{OL}} = \frac{\Delta V_c \cdot A_{cm}}{A_{OL}} = \frac{\Delta V_c}{CMRR} \tag{24.27}$$

Knowing that 50 dB = 316, a change in the common-mode level on the inputs of the op-amp by 500 mV results in an input-referred offset voltage change of 500 mV/316 or 1.6 mV (if the gain of the diff-amp is 10, then its output voltage will change by 16 mV). This may not seem like such a big deal. However, notice that at higher frequencies, in Fig. 22.16, the *CMRR* falls off, indicating that the common-mode gain is increasing. This leads to distortion and forces the use of op-amp topologies in which common-mode voltage doesn't vary (the inverting op-amp topology, see Fig. 24.26).

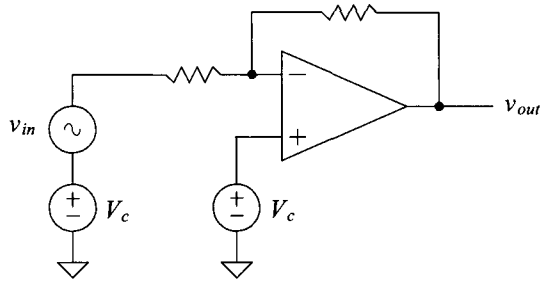


Figure 24.26 An inverting op-amp topology. The common mode voltage is held constant.

Power Supply Rejection Ratio (PSRR)

The power supply rejection ratio (PSRR) is a term used to describe how well an amplifier rejects noise or changes on the *VDD* and or ground power buses. This parameter can be extremely important in precision analog design. Consider the test setup shown in Fig. 24.27. The positive PSRR is defined by

$$PSRR^+ = \frac{A_{OL}(f)}{v_{out}/v^+} \tag{24.28}$$

while the negative PSRR is defined by

$$PSRR^- = \frac{A_{OL}(f)}{v_{out}/v^-} \tag{24.29}$$

Ideally, v_{out} doesn't vary with changes in *VDD* and ground (and so the *PSRR* is infinite).

To understand how variations in *VDD* or ground can feed to the output of the amplifier, consider the op-amp in Fig. 24.8. Variations in *VDD* feed through to the gate of M3. Because of the circuit's symmetry, this causes the drain of M4, and thus the gate of M7, to move around. However, the source of M7 is moving the same amount, causing the v_{sg} of M7 to remain constant. Again, because of the symmetry, the output voltage moves

at the same rate. Thus, noise on *VDD* feeds directly to the output of the op-amp. This is indicated in Fig. 24.27c, where v_{out} / v^+ is one. At higher frequencies (in the kHz range), the gate and drain of M7 get shorted together through the compensation capacitor. This, again, causes all of the noise from *VDD* to feed directly to the output of the amplifier (see netlists at cmosedu.com). The indirect compensation scheme used in the op-amp of Fig. 24.21 can be designed for larger f_{un} and, thus, has better *PSRR* at higher frequencies. Using the common-gate stage, Fig. 24.17, can result in an even higher *PSRR* by isolating the compensation capacitor from the power supplies. For this reason op-amp's that use a cascode-load diff-amp, Fig. 24.29, are very useful in practical design.

Noise on ground ideally won't affect the operation of the op-amp (in either of the topologies of Fig. 24.8 or 24.21). The noise appears as a voltage variation across the current sources. In reality, at low frequencies, some of the ground noise, v^-, appears at the output (this is especially true in nanometer processes that have low r_o). However, at higher frequencies, because of the compensation capacitance connected to the output of the op-amp, ground noise contributions to the output signal decrease.

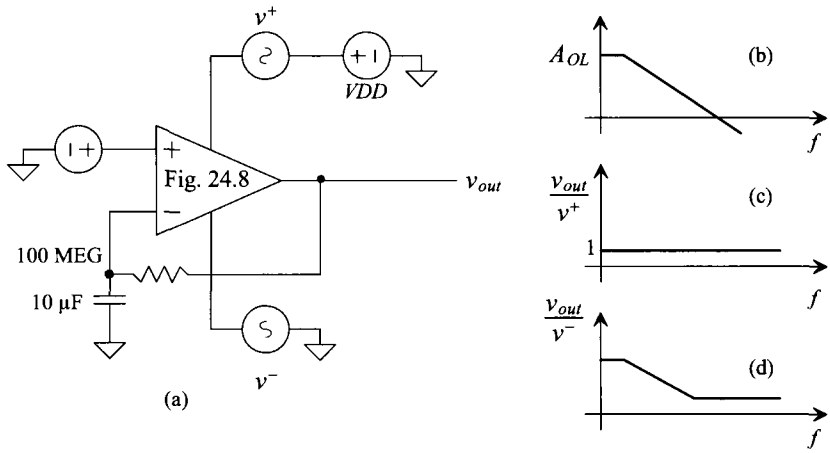


Figure 24.27 (a) Test setup to determine PSRR, (b) open-loop gain, (c) gain from AC signal on VDD to output, and (d) gain from AC signal on ground to output.

Increasing the Input Common-Mode Voltage Range

It may be useful in some situations to have an input common-mode voltage range that extends close to the power supply rails. For our op-amp in Fig. 24.21, the allowable input common-mode voltage range is from (roughly) 450 mV to 900 mV (basically half of *VDD*). Towards the goal of extending the input common-mode voltage range, consider the addition of a PMOS diff-amp to Fig. 24.21, as seen in Fig. 24.28. The circuitry on the right side of the schematic is the op-amp in Fig. 24.21 drawn a little differently. Here, we've drawn the current source of the diff-amp as two parallel current sources. In Fig. 24.21 the current source biasing the NMOS diff-amp used MOSFETs with 100/2 sizes. Here we supply the same current but use two 50/2-sized current sources. Also, we've bumped up the size of the PMOS devices (M3, M4, and M7) by two. This is to accommodate the extra current supplied by the added PMOS diff-amp (the left side of the schematic). We could keep the PMOS devices the same size as seen in Fig. 24.21 and the

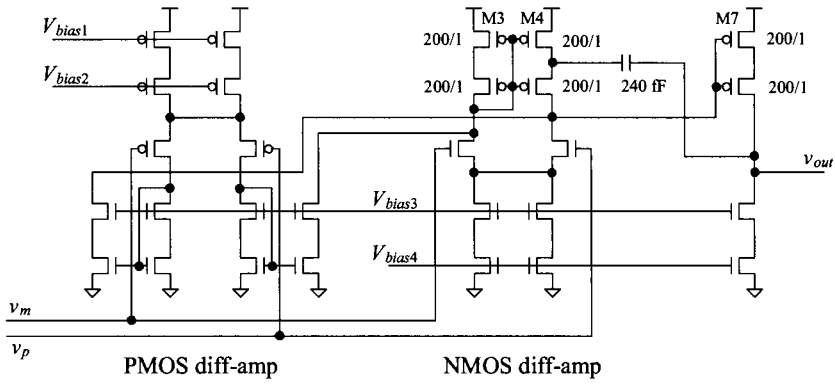


Figure 24.28 Two-stage op-amp of Fig. 24.21 with rail-to-rail input range.

circuit would still work fine (the V_{SG} voltages of the PMOS would simply be a little larger when both diff-amps are on). Two other notes: notice that the DC currents flowing in M3, M4, and M7 change depending on the input common-mode voltage. When the input common-mode voltage is large, the PMOS diff-pair is off; when it's small, the NMOS diff-pair is off. In the middle, both are conducting current. This means that the transconductance of the diff-amp will vary from g_{mn} to $g_{mn} + g_{mp}$ to g_{mp}. When both diff-amps are on (assuming $g_{mn} = g_{mp}$), the transconductance is twice as high as when a single diff-amp is on. This may require doubling the compensation capacitor. Finally, the change in the DC biasing conditions result in an offset that is a function of the input common-mode voltage.

Estimating Bandwidth in Op-Amp Circuits

When we finish designing an op-amp, its frequency response can be written using a single dominant-pole response (see Fig. 21.26 on page 680 with $A_{DC} = A_{OLDC}$) as

$$A_{OL}(f) = \frac{A_{OLDC}}{1 + j \cdot \frac{f}{f_{3dB}}} \tag{24.30}$$

For the op-amp response in Fig. 24.19, we can write

$$A_{OL}(f) = \frac{1{,}000}{1 + j\frac{f}{10\,kHz}} \tag{24.31}$$

To estimate the bandwidth of a closed-loop op-amp circuit where $f >> f_{3dB}$, we can write Eq. (24.30) as

$$|A_{OL}(f)| \approx \frac{A_{OLDC}}{\frac{f}{f_{3dB}}} = \frac{A_{OLDC} \cdot f_{3dB}}{f} = \frac{f_{un}}{f} \tag{24.32}$$

noting the unity-gain frequency is calculated using

$$f_{un} = A_{OLDC} \cdot f_{3dB} \tag{24.33}$$

From this equation, we should see why the unity-gain frequency, f_{un}, is called the *gain-bandwidth product*. Note that for every increase in frequency by 10 (decade) above f_{3dB}, we get a decrease in A_{OL} by 10 (–20 dB). Alternatively, for every increase in frequency by 2 (octave) above f_{3dB}, we get a decrease in A_{OL} by 2 (– 6 dB).

The closed-loop bandwidth (which we'll call f_{3dBCL}) of the op-amp circuit cannot be larger than the bandwidth of the op-amp. Therefore, to estimate the bandwidth of a closed-loop op-amp circuit, assuming the op-amp is the limiting factor, we can write

$$A_{CL} \cdot f_{3dBCL} = f_{un} = \text{gain-bandwidth product} \qquad (24.34)$$

If the op-amp circuit has a closed-loop gain of one (a follower configuration as seen in Fig. (24.7)), the bandwidth is f_{un}. The op-amp in Fig. 24.21 used in a follower configuration would have a bandwidth of (roughly) 100 MHz. If this op-amp were used in a closed-loop configuration with a gain of 10, then the bandwidth of the op-amp circuit would be estimated as 10 MHz.

24.2 An Op-Amp with Output Buffer

In the previous section, the low-frequency open loop gain of the op-amps in Figs. 24.8 or 24.21 was determined by a product of the diff-amp's gain, A_1, and the common-source's gain, A_2 or

$$A_{OLDC} = A_1 \cdot A_2 = \overbrace{g_{mn}(r_{o2} \| r_{o4})}^{A_1} \cdot \overbrace{g_{mp} r_{o7}}^{A_2} \qquad (24.35)$$

which, from the simulations (see Fig. 24.19 for example) was 1,000. The small-signal resistance on the output of the op-amp, r_{o7}, is (from Table 9.2) 333 kΩ. If we were to connect a 10 kΩ resistor to the op-amp output, then A_{OLDC} would drop to 33. As seen in Fig. 24.1, we can add a buffer to the output of second stage to isolate it from a load resistance (or a large capacitance). We could use a source-follower (that has a voltage gain of 1), as seen in Figs. 21.46 or 21.48. However, this addition limits the output swing of the op-amp (which may be OK in some situations). Next we could try using a push-pull topology, as seen in Fig. 21.49. However, the voltage gain of the push-pull amplifier is >1 (see Eq. (21.116)) so if we were to include it in our basic op-amp of Fig. 24.21, we would have a three-stage op-amp (meaning all three stages have voltage gains greater than one). A three-stage op-amp can be challenging to compensate over production corners (and temperature). Also, as seen in Eq. (21.116), a small load resistor (kΩ) would still kill the push-pull amplifier's gain. To keep the gain high, let's try to use a first-stage topology with a large gain (increase A_1) while using a push-pull amplifier for the second stage. The gain of the second stage can still drop but, since the gain of the first stage is large, we still end up with a reasonable overall gain.

Towards the goal of increasing the first-stage gain, consider the op-amp schematic seen in Fig. 24.29. For the first stage, we've used the cascode diff-amp originally seen in Fig. 22.30. The gain of this diff-amp (now A_1) is 500 (from Tables 9.2, and 20.1 and Eq. (22.48)). The second stage of the op-amp is the topology seen in Fig. 21.50. Its gain depends on the load resistance it drives. If no load is connected to its output, then

$$A_2 = -10 \cdot (g_{mn} + g_{mp}) \cdot \frac{(r_{op} \| r_{on})}{10} = -31.6 \; V/V \qquad (24.36)$$

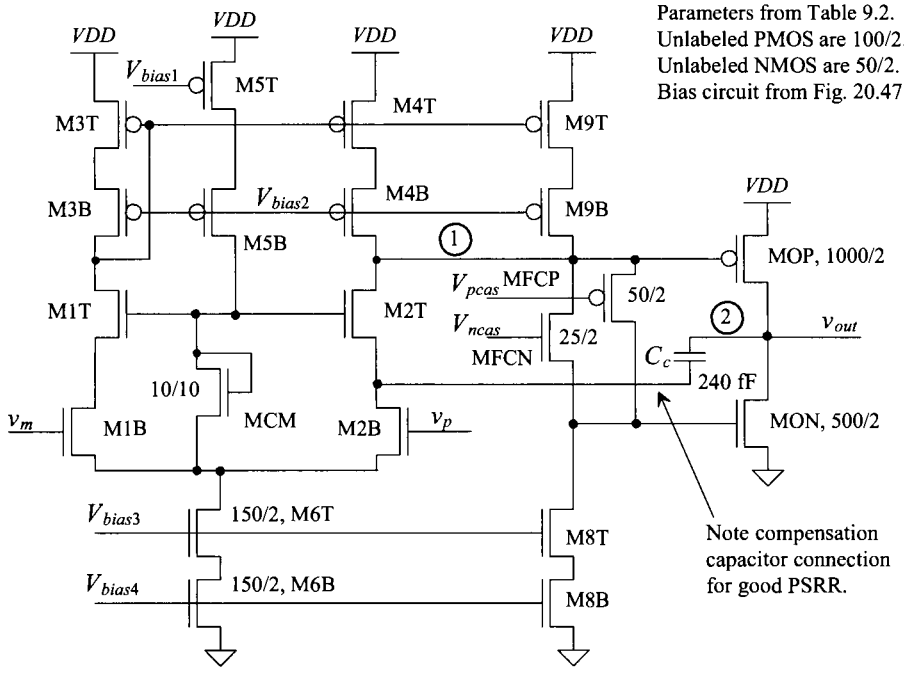


Figure 24.29 A CMOS op-amp with output buffer.

giving an overall low-frequency gain, A_{OLDC}, of 15,800 (= 84 dB). Note that the widths of MON and MOP are ten times wider than the values specified in Table 9.2 and so, as seen in Fig. 21.50, they conduct 100 μA of current. In Eq. (24.36) we multiplied the g_ms in Table 9.2 by 10 ($g_{mon} = 10 \cdot \beta_n(V_{GS} - V_{THN}) = 10 \cdot g_{mn,Table\ 9.2}$) and divided the output resistances given in Table 9.2 by 10 $\left(r_{omon} = \frac{1}{\lambda 10 \cdot 10\mu A} = \frac{r_{on}}{10}\right)$.

Compensating the Op-Amp

We increased the gain of the first stage by increasing R_1 (the resistance at node 1 is now set by cascoded current sources). As seen in Eq. (21.65), this pushes the pole lower in frequency. As just described in Eq. (24.33), this decrease in f_1 (= f_{3dB}) and increase in low-frequency gain *doesn't have any effect* on the gain-bandwidth product (= f_{un}) of the op-amp. What this indicates, to a certain extent, is that we can still compensate the op-amp with a 240 fF capacitor as we did in the last section. To feed the indirect compensation current to node 1 we connect the compensation capacitor to the source of M2T, as seen in Fig. 24.29. This ensures good PSRR.

The open-loop response of the op-amp in Fig. 24.29 (without a load) is seen in Fig. 24.30. The phase-margin is roughly 70 degrees. The step response of the op-amp driving a 1k resistor and a 10 pF capacitor is seen in Fig. 24.31. The input signal is a pulse from 100 mV to 900 mV. Since the gain of the amplifier is −1 and the common-mode voltage is 500 mV, the output swings from 900 mV to 100 mV.

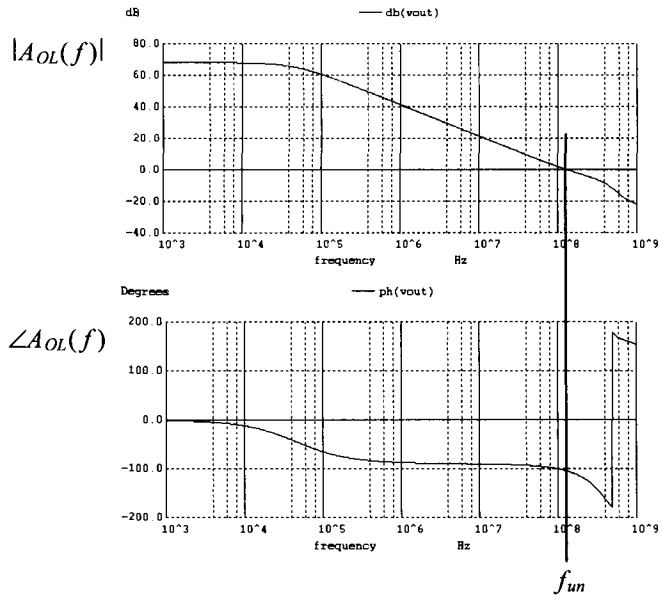


Figure 24.30 Open-loop response of the op-amp in Fig. 24.29.

This is a good point to remember one of the fundamentals we presented in Ch. 9: that is, for high-speed design, we must use minimum length devices (see Eq. (9.59)). If we reduce all of the length of 2 (100 nm) devices in Fig. 24.29 to length of 1 (50 nm) devices, we can increase the speed of the op-amp. Figure 24.32 shows how the step response in Fig. 24.31 changes when we make this reduction in length. The big problem with using minimum channel lengths is the reduction in gain. Close inspection of Fig. 24.32 shows that the output is never quite pulled up to the correct voltage (it is either slightly below 900 mV or 100 mV). Simulating the AC open-loop response results in a gain of 44 dB (= 159). An output voltage of 900 mV would result in a difference on the inputs of the op-amp of 5.66 mV (0.9/159 = $v_p - v_m$).

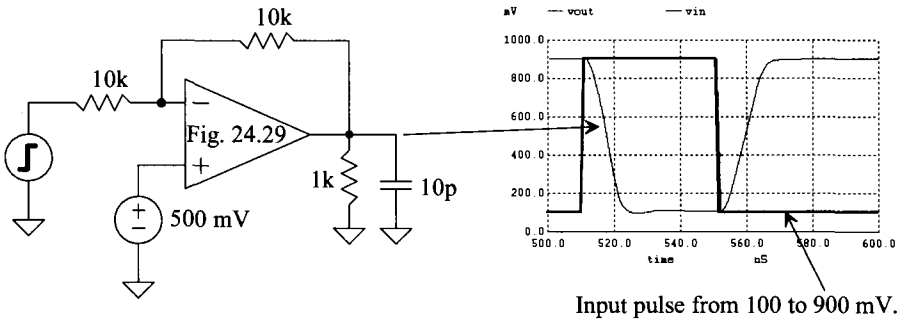


Figure 24.31 Step response of the op-amp in Fig. 24.29 driving 1k and 10 pF.

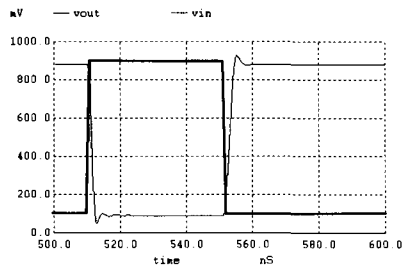


Figure 24.32 Step response of the amplifier in Fig. 24.29 when the lengths of the devices are reduced from 2 to 1 (from 100 nm to 50 nm). The load is still, as seen in Fig. 24.31, 1k and 10 pF.

24.3 The Operational Transconductance Amplifier (OTA)

The operational transconductance amplifier (OTA) can be defined as an amplifier where all nodes are low impedance except the input and output nodes. A simple example of an OTA is the diff-amp with current mirror load seen in Fig. 22.6. *An OTA without buffer can only drive capacitive loads.* A resistive load (unless the resistor is very large) will kill the gain of the OTA.

A sample OTA is shown in Fig. 24.33. Note that the basic op-amp in Fig. 24.2 is not considered an OTA because the drain of M4 is a high-impedance node and not the input or output of the amplifier. As seen in Fig. 24.33, except for the input and output nodes, all nodes have either a gate-drain-connected device or a source connected to them. The terminology "1:K" indicates that M4 and M5 can be sized K times wider (K > 1) than the other MOSFETs in the circuit. Assuming that $\beta_1 = \beta_2$, $\beta_{31} = \beta_{41}$, we observe that the current i_{d31} or i_{d41} is given by

$$-i_{d31} = i_{d41} = \frac{g_{mn}}{2}(v_p - v_m) = i_d \tag{24.37}$$

Furthermore, if $\beta_4 = K \cdot \beta_{41} = K \cdot \beta_{31} = K \cdot \beta_3$ and $K \cdot \beta_{51} = \beta_5$, then $i_{d4} = -i_{d5} = K \cdot i_{d41} = -K \cdot i_{d31}$. If the impedance of the capacitor is large compared to $r_{o4} \| r_{o5}$, then the output voltage of the OTA is given by

$$v_{out} = 2Ki_d(r_{o4} \| r_{o5}) \tag{24.38}$$

and the voltage gain is given by

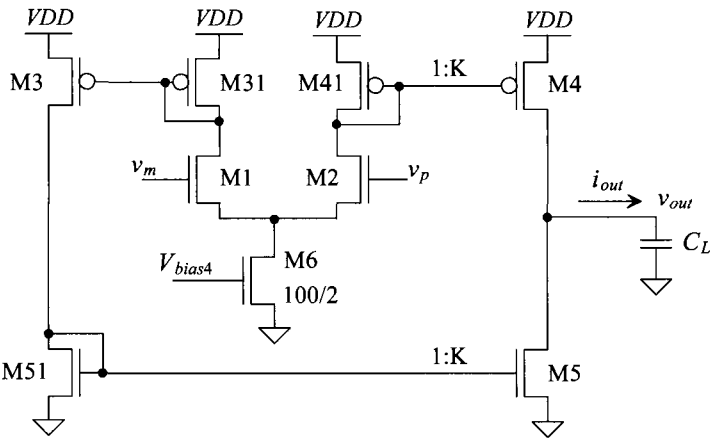
$$A_v = \frac{v_{out}}{v_p - v_m} = K \cdot g_m \cdot (r_{o4} \| r_{o5}) \tag{24.39}$$

noting that the noninverting input of the OTA is the gate of M2. While the derivation is interesting, as the name implies, we are interested in the transconductance of OTA. If the impedance of the capacitor is small compared to the OTA output resistance (at higher frequencies), we can write

$$i_{out} = i_{d4} - i_{d5} = 2Ki_d \tag{24.40}$$

The transconductance of the OTA is given by

$$g_{mOTA} = \frac{i_{out}}{v_p - v_m} = K \cdot g_m \tag{24.41}$$



Unless otherwise indicated, parameters from Table 9.2 with biasing circuit in Fig. 20.47.

Figure 24.33 Example of an operational transconductance amplifier (OTA).

Unity-Gain Frequency, f_{un}

To simulate the unity-gain frequency, f_{un}, (where the open loop gain is one) for the OTA, we can use the DC stability scheme seen in Fig. 24.34. We can write (for higher frequencies) the output voltage as

$$v_{out} = i_{out} \cdot \frac{1}{j\omega \cdot C_L} = g_{mn} v_{in} \cdot \frac{1}{j\omega \cdot C_L} \tag{24.42}$$

or

$$\frac{v_{out}}{v_{in}} = \frac{g_{mn}}{j\omega C_L} \rightarrow \left|\frac{v_{out}}{v_{in}}\right| = \frac{g_{mn}}{2\pi f \cdot C_L} \tag{24.43}$$

As before, we define the unity-gain frequency as the point where the open-loop gain is unity

$$\frac{g_{mn}}{2\pi f_{un} \cdot C_L} = 1 \rightarrow f_{un} = \frac{g_{mn}}{2\pi C_L} \tag{24.44}$$

For the OTA in Fig. 24.33 driving a 1 pF load capacitance, we can estimate the unity-gain frequency (with $K = 1$) as

$$f_{un} = \frac{150\ \mu A/V}{2\pi \cdot 1\,pF} = 24\ MHz$$

The simulation results are seen in Fig. 24.34. The location of the pole is estimated using

$$f_{3dB} = \frac{1}{2\pi(r_{o4} \| r_{o5})C_L} \tag{24.45}$$

For the OTA in Fig. 24.33, f_{3dB} = 1.4 MHz using the values in Table 9.2. The low-frequency gain is $g_m(r_{o4} \| r_{o5})$ = 16.65 V/V (= 24.4 dB).

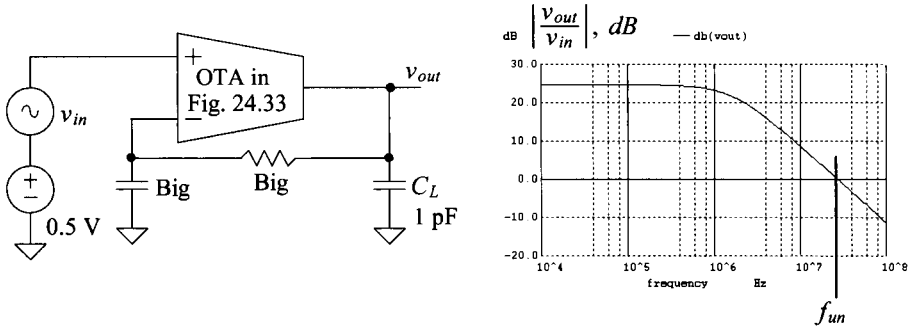


Figure 24.34 Simulating the open-loop response of the OTA in Fig. 24.33.

Note that the maximum value of i_{out} is KI_{SS} (the drain current of M6 multiplied by the increase in widths, K, in the current mirrors M41/M4 and M51/M5). This is important to understand because using an OTA for the first stage of an op-amp results in the same slew-rate limitations of I_{SS} driving C_c that we had when using a diff-amp.

Increasing the OTA Output Resistance

The ideal OTA has infinite output resistance. All of i_{out} flows in the external capacitive load and none flows in the OTA's own output resistance (which is $r_{o4}||r_{o5}$ for the OTA in Fig. 24.33). Towards increasing the OTA output resistance, consider the configuration seen in Fig. 24.35. This topology is based on the one seen in Fig. 24.33 except that now we've cascoded the current mirrors. Note how we've drawn the diff-amp's tail current source as four MOSFETs instead of two with twice the width (this is the way we would lay it out too). The low-frequency gain of the OTA is now increased to

$$A_v = g_{mn} \cdot (R_{ocasn}||R_{ocasp}) \tag{24.46}$$

The 3-dB frequency is now

$$f_{3dB} = \frac{1}{2\pi(R_{ocasn}||R_{ocasp}) \cdot C_L} \tag{24.47}$$

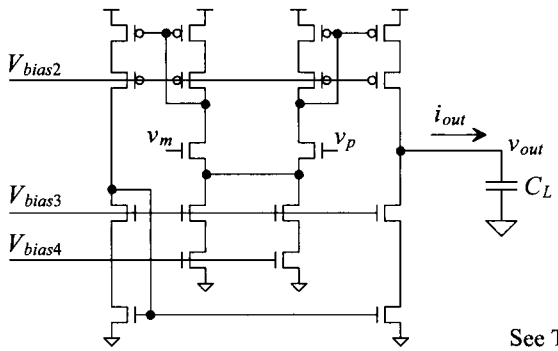


Figure 24.35 A cascode OTA circuit (higher output resistance).

As discussed before (Sec. 24.2 in the discussion concerning compensating the op-amp), when we get a decrease in the 3-dB frequency and an increase in the low-frequency gain, the effects cancel and the gain-bandwidth product (f_{un}) remains constant. The unity-gain frequency is still given by Eq. (24.44). For the OTA in Fig. 24.35, we can estimate the low-frequency gain, using Tables 9.2 and 20.1, as

$$A_v = (150) \cdot (16.6||4.2) = 500\ (54\ dB)$$

and the 3-dB frequency, driving a 1 pF load, is

$$f_{3dB} = \frac{1}{2\pi(16.6||4.2 \times 10^6)(1\ pF)} = 47\ kHz$$

Simulation results are seen in Fig. 24.36. The PM is roughly 85°.

An Important Note

Note, in Eq. (24.44), that increasing the load capacitance, decreases the unity-gain frequency, making the OTA more stable. Unlike the two-stage op-amps discussed in the first two sections of this chapter, where the op-amp can become unstable with a large load capacitance, the OTA only becomes more stable with large load capacitance. Also, the PM approaches 90° as the load capacitance increases. The step response of the OTA has a first-order shape (just as in an RC circuit). In many on-chip applications, the load is purely capacitive and so the OTA works great as an "op-amp" in a closed-loop configuration (thus we'll often call OTAs op-amps). Note that adding a second stage to the basic OTA forms a (two-stage) op-amp like those discussed earlier. We can use the methods already presented to compensate the resulting structure (but, again, driving a load capacitance that's too large with these two-stage structures can result in instability).

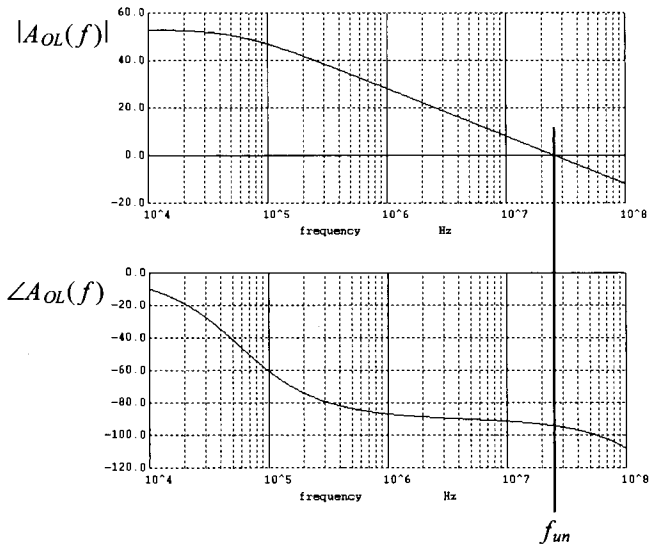


Figure 24.36 The open-loop gain and phase response for the OTA in Fig. 24.35.

OTA with an Output Buffer (An Op-Amp)

If we use the OTA in Fig. 24.35 (or Fig. 24.33) to drive a 1 pF load, we're limited to charging/discharging the capacitor at a rate of

$$\frac{I_{SS}}{C_L} = \frac{dv_{out}}{dt} = \frac{20\ \mu A}{1\ pF} = \frac{20\ mV}{ns} \tag{24.48}$$

For the OTA's output to change from ground to *VDD* (1 V) requires (just due to slewing) 50 ns. This length of time (the slew-rate limited portion of the settling time) may be fine for many applications. However, for high-speed design, we want faster settling times. Looking at Eq. (24.48), we see that we can decrease the settling time by increasing I_{SS}. However, as discussed in Ch. 9, this causes the gain of the circuit to decrease. To avoid the reduction in gain, we can make a corresponding increase in the size of the devices to keep the overdrive voltage constant. But this is doing nothing more than effectively reducing the size of the load capacitor (the load capacitance becomes comparable in size to the parasitic transistor capacitances).

To speed up the circuit, we may add an output stage, Fig. 24.37. The added stage is a common-source amplifier (with a negative gain indicating **we swap the inverting and noninverting terminals** of the op-amp or else we waste a lot of time). While M7 can turn on and charge a load capacitor quickly, the current source, M8, still limits the rate of load capacitance discharge. For this reason, we've bumped up the current in the output stage to 100 μA. The open-loop simulations driving a 1-pF load are seen in Fig. 24.38. The PM is 45° (too low if the op-amp will be used in a unity follower configuration). Figure 24.39 shows the step response of the op-amp.

We should compare this figure to the response we saw in Fig. 24.31. The op-amp in Fig. 24.31 is driving a heavier load but still has cleaner settling behavior. Further, a comparison of the current pulled from *VDD* reveals, under the same loading and operating conditions, that the op-amp in Fig. 24.37 pulls more current (see Fig. 24.39). The main difference in these two op-amps is the output buffer used. Let's consider adding a class AB buffer to the OTA in Fig. 24.35 (like the one used in the op-amp of Fig. 24.29). Since we are only driving a 1 pF load, we'll leave the output devices, MON and

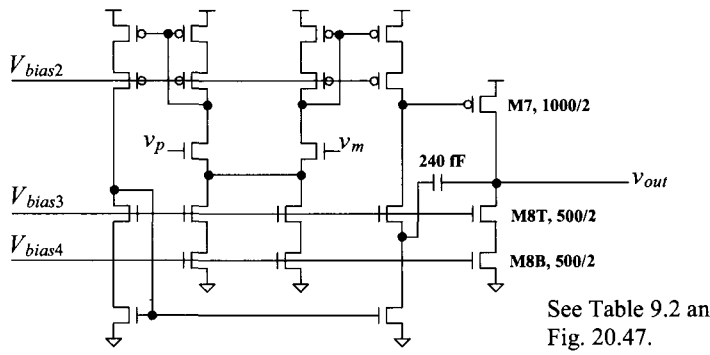


Figure 24.37 A cascode OTA circuit with common-source output buffer (an op-amp). Note the inverting and noninverting terminals are swapped from Fig. 24.35.

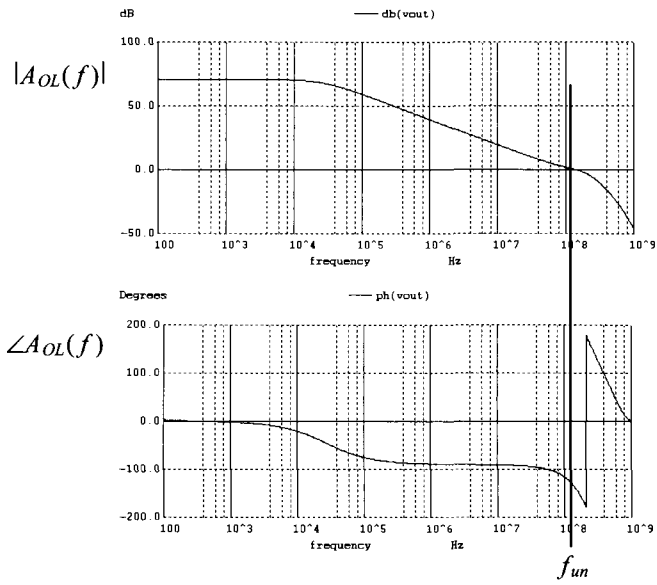
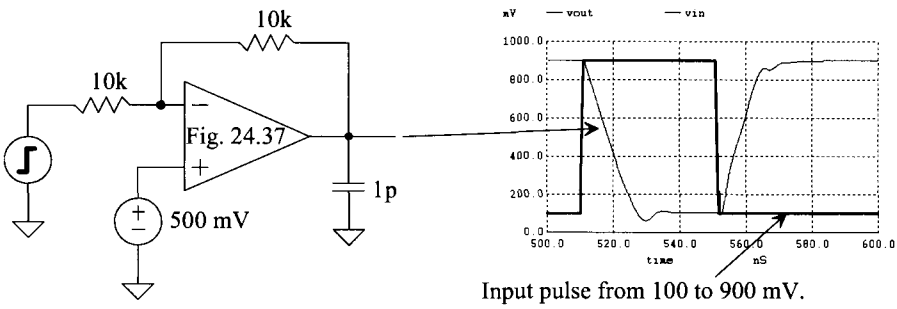
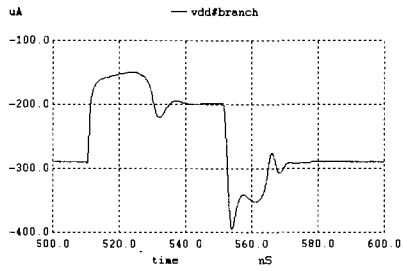


Figure 24.38 Open-loop response of the op-amp in Fig. 24.37 driving a 1-pF load.





Current from VDD. Includes the bias circuit's (Fig. 20.47) current (140 uA).

Figure 24.39 Step response of the op-amp in Fig. 24.37 driving a 1 pF.

MOP, at the same size as the other MOSFETs in the circuit (PMOS are 100/2 and NMOS are 50/2). The resulting op-amp is seen in Fig. 24.40. The step response (in the same configuration used to generate Fig. 24.39) is seen in Fig. 24.41. Notice that the current pulled from *VDD* by the op-amp in Fig. 24.40 is 100 μA less than the current pulled by the op-amp in Fig. 24.37. This lower current is the result of using a class AB output stage.

The performance of the op-amps in Figs. 24.37 and 24.40, with regard to high-speed operation and settling time, won't be quite as good as the topology in Fig. 24.29 (assuming the same biasing conditions, device sizes, and overdrive voltages). To understand why, look at the path, in Fig. 24.40, that the noninverting op-amp input, v_p, takes to get to the op-amp output, v_{out} (that is, M1 - M31 - M3 - M51 - M5 - MON). The delay through this path is longer than the delay, in Fig. 24.29, through M2 - MOP. Further, for high speed, M5 of the op-amp in Fig. 24.40 must turn on (above its quiescent current level) to pull the gate of MON down. For the op-amp in Fig. 24.29, the fact that both the gate of M9T and MOP are driven (in opposite directions) by the diff-amp allows us to use a simple pull-down current (M8) without losing speed. The issues with the cascode diff-amp-based, op-amp topology of Fig. 24.29 are the more limited input common-mode range and the limited voltage swing of node 1. Towards getting better input common-mode voltage range and output swing as well as improved high-speed operation, let's discuss the folded-cascode OTA (see Fig. 22.5).

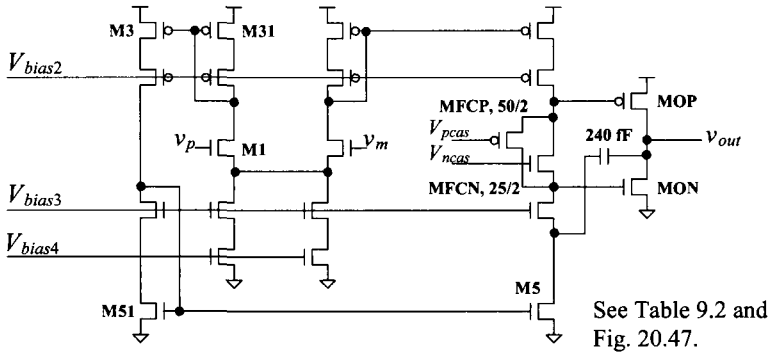


Figure 24.40 Using a class AB output stage with the OTA.

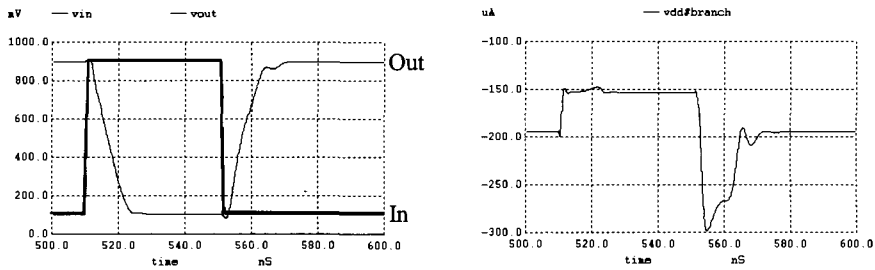


Figure 24.41 The step response and current in the topologies seen in Fig. 24.39 using the op-amp in Fig. 24.40.

The Folded-Cascode OTA and Op-Amp

An example of an NMOS diff-amp-based folded cascode OTA is seen in Fig. 24.42. It is assumed that the reader understands the biasing and operation of the circuits seen in Figs. 20.45, 20.46, and 22.5. To avoid labeling MOSFETs with twice the width, we've drawn the schematic in Fig. 24.42 with MOSFETs in parallel in the branches that supply or sink more current (for example, the diff-amp's tail current). All MOSFETs in Fig. 24.42 conduct 10 μA of current under equilibrium conditions. Before moving on, it may be a good idea to pause and make sure that the reader understands how the currents sum in this OTA.

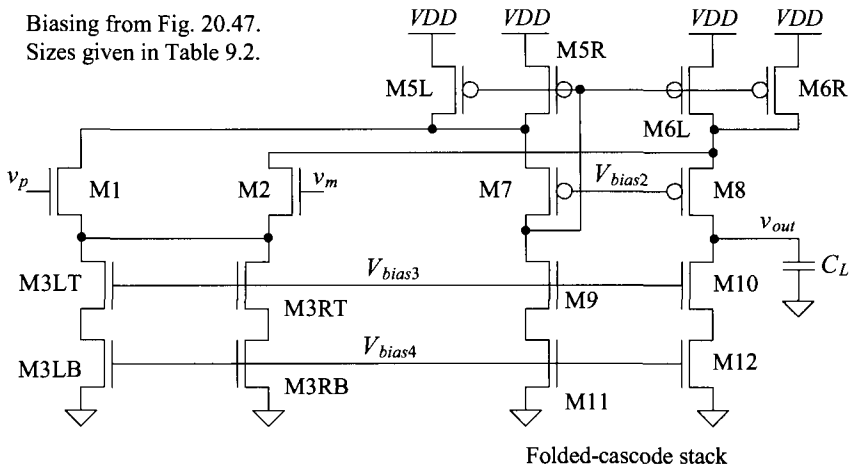


Figure 24.42 A folded-cascode OTA.

To qualitatively describe the operation of the OTA, let's look at what happens when v_p goes high (above v_m). This causes M1 to turn on and M2 to shut off. When M1 turns on, it pulls the drain of M5 down, shutting M7 off. As M7 shuts off, M9 and M11 pull the gate of M5 down. With the gate of M5 being pulled down, the current in M6 increases. At the same time, because the current in M2 is decreasing, the current in M8 is increasing and the output voltage increases. The maximum current the OTA output can supply (out of the OTA to the load) is in the neighborhood of 20 μA, while the maximum current the OTA can sink (into the OTA) is 10 μA (set by the current sink M10/M11).

The same AC equations presented at the beginning of this section also apply to this OTA. For example, the AC drain currents of M1 and M2 can be written as

$$i_{d1} = -i_{d2} = g_{mn} v_{gs1} = -g_{mn} v_{gs2} \tag{24.49}$$

which, again, indicates $v_{gs1} = -v_{gs2}$. However, we know

$$v_p - v_m = v_{gs1} + (-v_{gs2}) \tag{24.50}$$

so

$$i_{d1} = i_{d5} = i_{d6} = (v_p - v_m) \cdot \frac{g_m}{2} \tag{24.51}$$

noting that the AC current through M9/M11 (and thus M7) is ideally zero. The current through M8 is then

$$i_{d8} = i_{d6} - i_{d2} = 2 \cdot i_{d1} \tag{24.52}$$

and thus the output voltage (again, the AC current in M10/M11 is ideally zero) is

$$v_{out} = i_{d8} \cdot (R_{ocasn} || R_{ocasp}) \tag{24.53}$$

and thus the gain is

$$A_v = \frac{v_{out}}{v_p - v_m} = g_{mn} \cdot (R_{ocasn} || R_{ocasp}) \tag{24.54}$$

This result should be compared to Eq. (24.46). Equation (24.47) gives the 3-dB frequency of the OTA's open-loop response, while Eq. (24.44) gives the unity-gain frequency. Figure 24.43 shows the open-loop response of the folded-cascode OTA driving a 1 pF load capacitance.

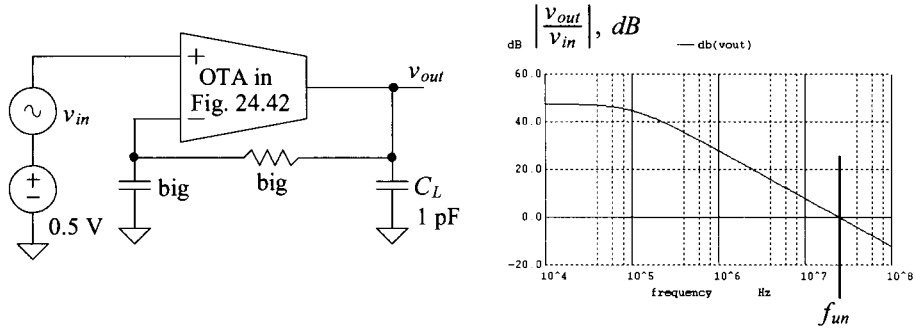


Figure 24.43 Simulating the open-loop response of the OTA in Fig. 24.42.

Figure 24.44 shows the schematic of a folded-cascode op-amp using a class AB output buffer. We've added floating current sources to equalize the voltages across M9/M10 (to minimize the input-referred offset). In the open-loop response of the op-amp (see Fig. 24.45), the load of the op-amp is a 1 pF capacitor. The step response is seen in Fig. 24.46, using the topology of Fig. 24.39 (gain of −1 driving 1 pF and the 10k feedback resistor). Reviewing the previous op-amp responses, we don't see much difference in performance. We can't seem to push the gain-bandwidth product, f_{un}, much above 100 MHz. Again, the only way to increase the speed is to reduce the channel length and/or increase the overdrive voltage.

Figure 24.47 shows what happens if we reduce the lengths of the MOSFETs used in the op-amp in Fig. 24.44 from 2 (100 nm) to 1 (50 nm). The gain-bandwidth product jumps to 400 MHz. However, the low-frequency gain drops to approximately 50 dB. The step response is clean, and the settling time is approximately 5 ns. While we can increase the speed further by redesigning the bias circuit and increasing the currents and overdrive voltage, let's, instead, concentrate on increasing the low-frequency gain of the op-amp. This won't increase the gain-bandwidth product of the op-amp, but it's necessary for precision amplification. To *enhance the gain,* we'll try to increase the OTA output resistance (R_1 or the resistance on node 1) by regulating the drain in the cascode current sources. We've already discussed this technique (see Fig. 20.40), but we haven't applied it to amplifiers. Before leaving this section, let's present one more example.

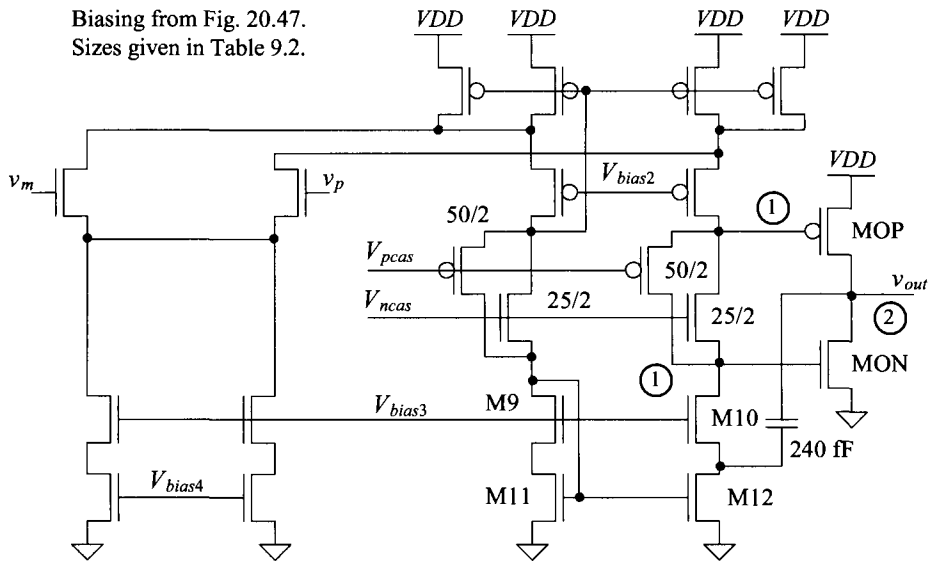


Figure 24.44 Folded-cascode op-amp with class AB output buffer.

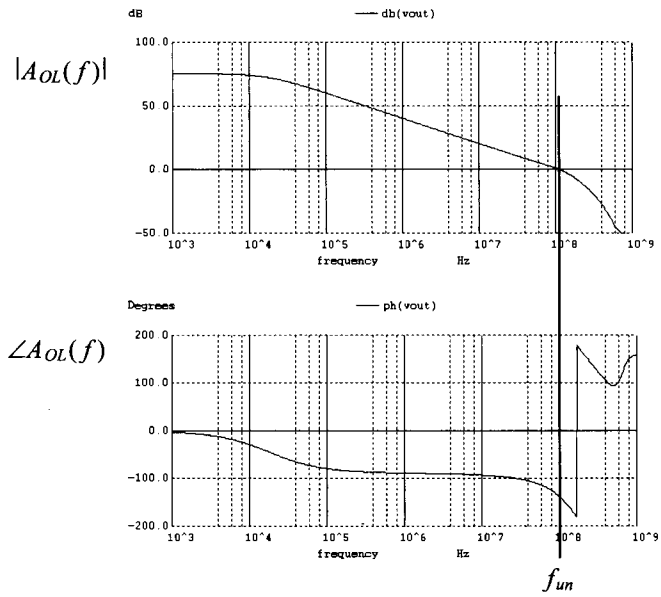


Figure 24.45 Open-loop response of the op-amp in Fig. 24.44 driving a 1-pF load.

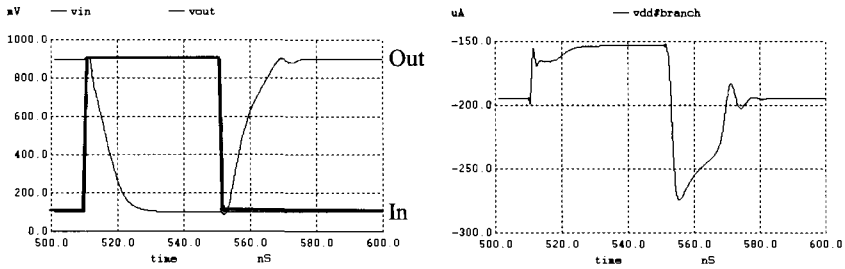


Figure 24.46 The step response and current in the topologies seen in Fig. 24.39 using the op-amp in Fig. 24.44.

Figure 24.48 shows a wide-swing op-amp based on the topology seen in Fig. 24.44. To get wide-swing operation (which means that the input common-mode voltage extends beyond the power supply rails and the op-amp still functions), we added a PMOS diff-amp stage. Further, to sink the additional current supplied by the PMOS diff-amp when it's on, we add two NMOS devices at the bottom of the folded-cascode stack. When, for example, the PMOS diff-amp shuts off with the input common-mode voltage moving towards *VDD,* the added two devices don't really affect the circuit's operation. The only result is that the V_{GS} of the bottom NMOS devices is slightly smaller when the PMOS diff-amp shuts off. A similar conclusion can be drawn when the NMOS diff-amp shuts off with the common-mode voltage moving towards ground. Note that when both diff-amps are on, the first-stage transconductance becomes, $g_{mn} + g_{mp}$. This means the gain-bandwidth product, f_{un} , moves to $(g_{mn} + g_{mp})/2\pi C_c$. The value of the compensation

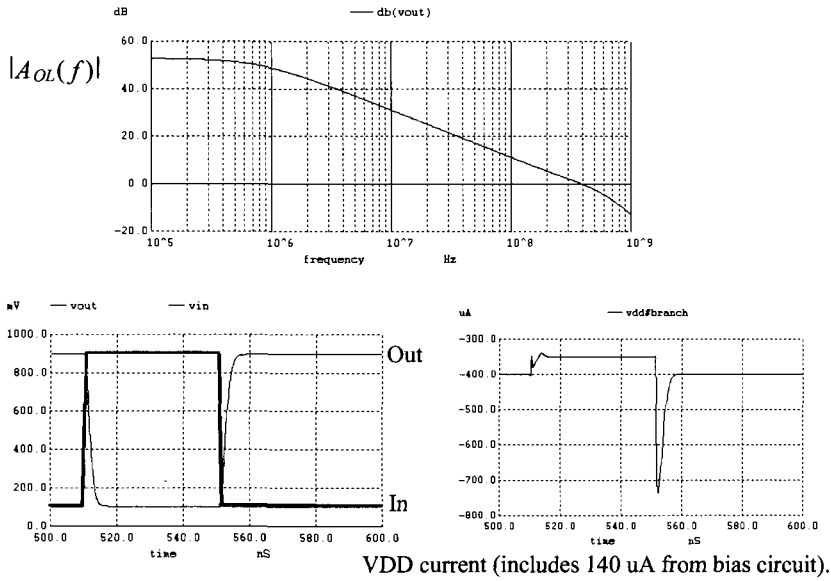
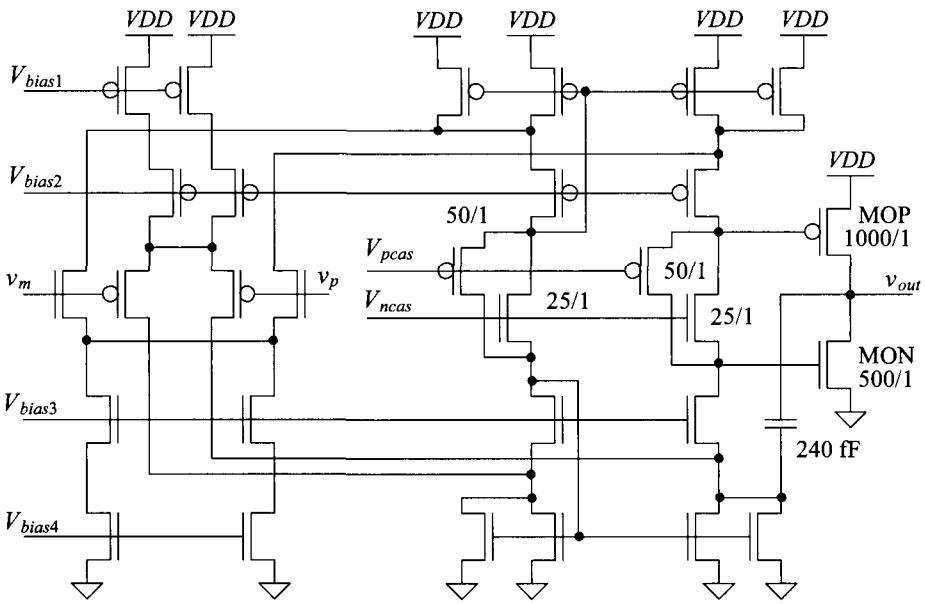


Figure 24.47 Reducing the length of the MOSFETs used in the op-amp in Fig. 24.44 from 2 to 1 and resimulating open-loop and step responses.



Biasing from Fig. 20.47.
Unlabeled NMOS are 50/1.
Unlabeled PMOS are 100/1.

Figure 24.48 An op-amp with an input common-mode range that extends beyond the power supply rails and that can drive heavy loads.

capacitor may need to be increased. When only one diff-amp is on, the transconductance of the other diff-amp goes to zero, resulting in a smaller gain-bandwidth product. The issue here is that the gain of the op-amp is changing with variations in the input common-mode voltage. This, as mentioned before, can lead to distortion and is the reason that the inverting topology, as seen in Fig. 24.39, is preferred (noting that the input common-mode voltage is fixed when using the inverting topology).

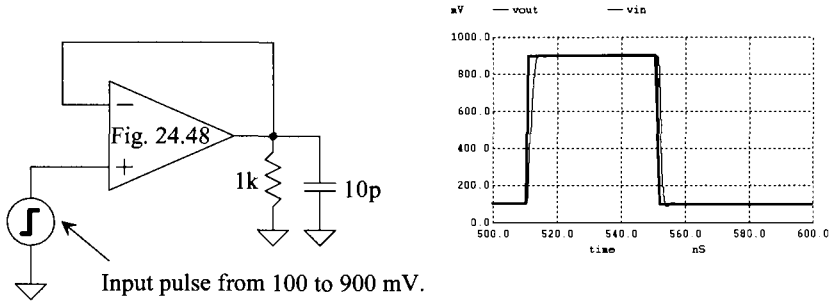


Figure 24.49 Step response of the op-amp in Fig. 24.48 driving 1k and 10 pF. Note that the op-amp is in the follower configuration and that the input common-mode voltage is changing.

Finally, in some applications, an op-amp that can supply significant amounts of current, say 100 mA, may be needed. To get such a large current, we may need to increase the widths of the output MOSFETs in the push-pull amplifier to, for example, 10,000 and 5,000 (for the PMOS and NMOS devices, respectively). The problem with this is that the quiescent current that flows in these devices, using the op-amp configuration in Fig. 24.44 as an example, is 1 mA. To reduce this current, we can increase the lengths of the floating current sources used in the folded-cascode section. This increases their gate-source voltage drops and moves the gates of the push-pull MOSFETs towards the power supply rails (shutting them off). Care must be exercised when doing this because shutting off the output MOSFETs can result in moving g_{m2} towards zero, causing, as indicated in Eq. (24.24), f_2 to move down in frequency, thus making the op-amp unstable.

24.4 Gain-Enhancement

While using minimum channel lengths (L = 1) results in the fastest op-amps, the open-loop gain, A_{OLDC}, is considerably reduced. Using gain-enhancement (GE) techniques (regulating the drain node in a cascode structure, see Fig. 20.40), we boost the low-frequency gain by increasing the cascode output resistance. However, the gain-bandwidth product, f_{un}, is still $g_m/2\pi C_c$. (We get the speed by using a smaller compensation capacitor and/or a larger diff-amp transconductance.) Note, in Fig. 24.47 for example, that our gain-bandwidth product went up by the increase in g_m with the reduction in the channel length. Reviewing Eqs. (24.30)–(24.34), we see that if A_{OLDC} goes up, f_{3dB} goes down (and f_{un} is a constant).

In the following discussion, we only concern ourselves with two-stage op-amps in which we are using GE to compensate for the low gain caused by our minimum channel lengths. While GE can be used in an OTA, the fact that the speed of the OTA is limited by the capacitance it is driving keeps them from being as fast as the two-stage op-amps we've discussed (unless, of course, the load capacitance is small).

As seen in Fig. 20.40, we need an additional amplifier to help regulate the drain of the cascode device. Consider the two differential amplifiers (OTAs) seen in Fig. 24.50. The source-followers on the inputs of the diff-amps are used to allow for the amplification of signals near ground (for the P amplifier) or *VDD* (for the N amplifier). The gains of the diff-amps are

$$A_P = g_{mp} \cdot (r_{on} || r_{op}) \text{ and } A_N = g_{mn} \cdot (r_{on} || r_{op}) \tag{24.55}$$

To simplify the equations, we'll assume

$$A_{GE} = A_P = A_N \tag{24.56}$$

The low-frequency gain of the op-amp in Fig. 24.44 is

$$A_{OLDC} = \overbrace{g_{mn} \cdot (R_{ocasn} || R_{ocasp})}^{\text{diff-amp gain}} \cdot \overbrace{(g_{mp} + g_{mn}) \cdot (r_{on} || r_{op})}^{\text{push-pull output stage}} \tag{24.57}$$

Using Eq. (20.67), we can write the open-loop gain *with gain-enhancement* as

$$A_{OLDC,GE} = A_{OLDC} \cdot A_{GE} \tag{24.58}$$

The open-loop gain is increased by the gain of the added amplifier. Figure 24.51 shows the op-amp of Fig. 24.44 with GE.

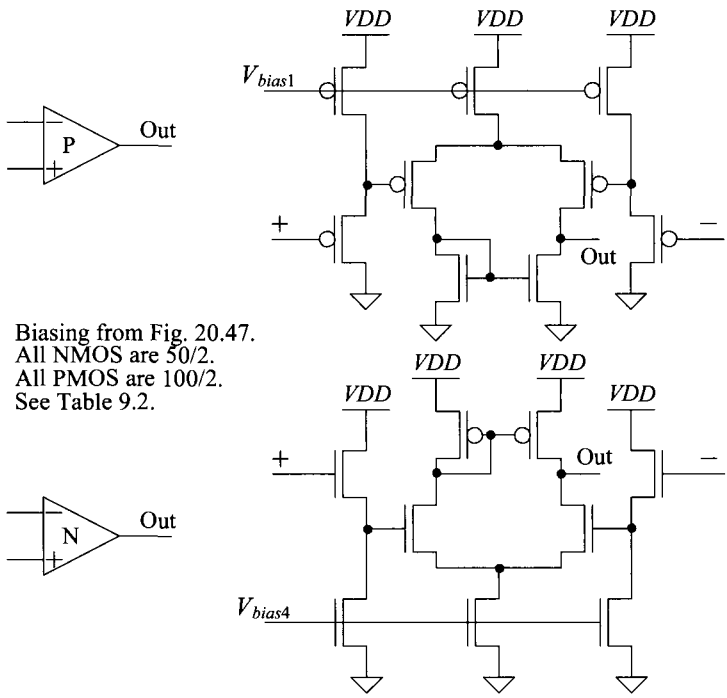


Figure 24.50 Diff-amps with source-follower level shifters for use in GE.

The simulation results in Fig. 24.47 were generated using the op-amp of Fig. 24.44 with the lengths reduced from 2 to 1. The low-frequency, open-loop gain was 53 dB. In Fig. 24.51 we added GE and used the resulting op-amp to generate the simulation results seen in Fig. 24.52 (with the GE compensation capacitors, C_{cGE}, set to zero). The low-frequency, open-loop gain is now 74 dB. The step response is seen as well. The current pulled from *VDD* is now 60 μA higher than the op-amp without GE. By replacing the diff-amps in the N and P amplifiers in Fig. 24.50 with folded-cascode OTAs (like the one seen in Fig. 24.42), we can get a greater increase in open loop gain. However, the stability of the regulated-drain feedback loop becomes even more important.

Bandwidth of the Added GE Amplifiers

Let's model the frequency response of the added amplifiers in Fig. 24.50 by

$$A_{GE}(f) = \frac{A_{GEDC}}{1 + j\frac{f}{f_{3dBGE}}} \tag{24.59}$$

Using this equation with Eqs. (24.30) and (24.58), we can write

$$A_{OLGE}(f) = \frac{A_{OLDC}}{1 + j \cdot \frac{f}{f_{3dB}}} \cdot \overbrace{\frac{A_{GEDC}}{1 + j \cdot \frac{f}{f_{3dBGE}}}}^{A_{GE}(f)} \tag{24.60}$$

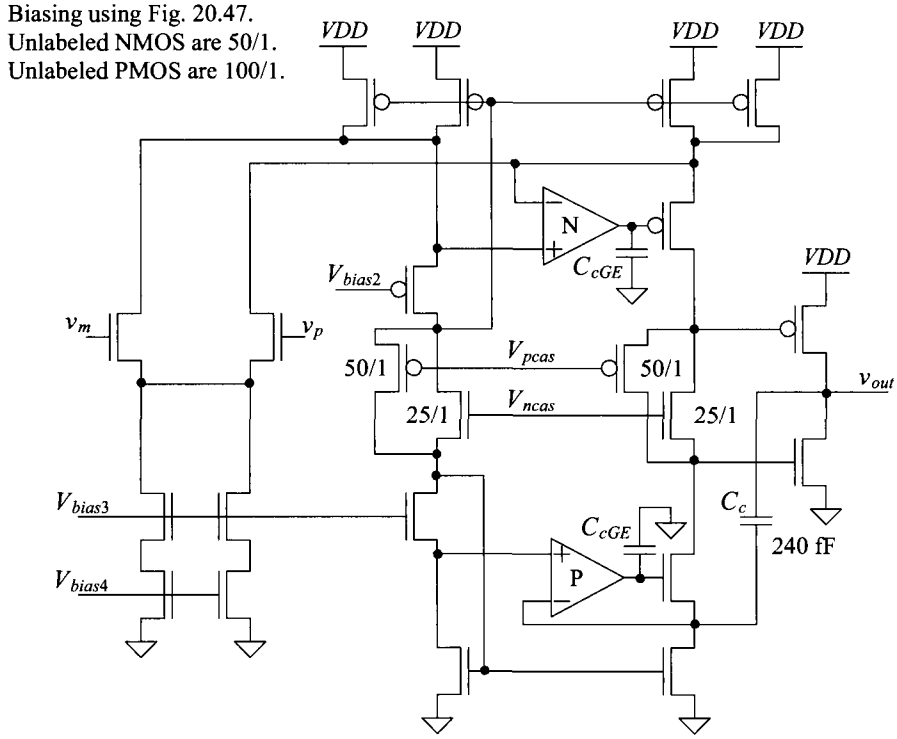


Figure 24.51 Folded-cascode op-amp with class AB output buffer and gain-enhancement.

However, the pole ($f_1 = f_{3dB}$) on the output of the folded-cascode OTA can be written, see Eqs. (20.67) and (24.47), with GE as

$$f_{3dB} = \frac{1}{2\pi(R_{ocasn} || R_{ocasp}) \cdot A_{GE}(f) \cdot C_c} \tag{24.61}$$

assuming the current through C_c is larger than the other currents, the output of the OTA may have to charge. If we substitute Eq. (24.61) into Eq. (24.60) and look at frequencies much larger than f_{3dB} (which from Fig. 24.52 is only a 100 kHz or so), we see that the frequency response of the added GE amplifiers cancels out of $A_{OLGE}(f)$. What this means is that the bandwidth of the added amplifiers doesn't need to be wide. As long as the bandwidths are larger than the f_{3dB} of the op-amp, the GE works as desired. Also, notice that when we substitute Eq. (24.61) into Eq. (24.60), the resulting transfer function shows a *doublet* (a pole and zero at the same frequency). If the pole and zero aren't at exactly the same frequency, then the settling time of the amplifier can be affected by the change in phase shift (noting that in Eq. (20.67) we are approximating the output resistance of the cascode structure). The output resistance of the cascode structures is decreasing with increasing frequency, while, at the same time, the decrease in the output resistance results in an increase in the circuit bandwidth (causing the gain-bandwidth product to be a constant).

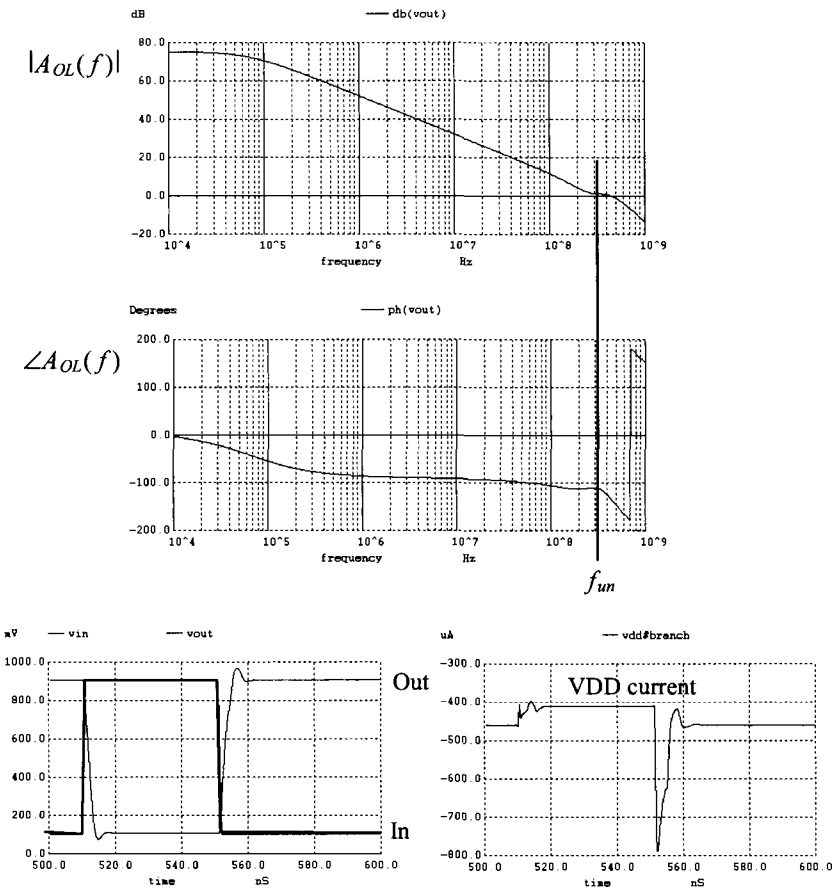
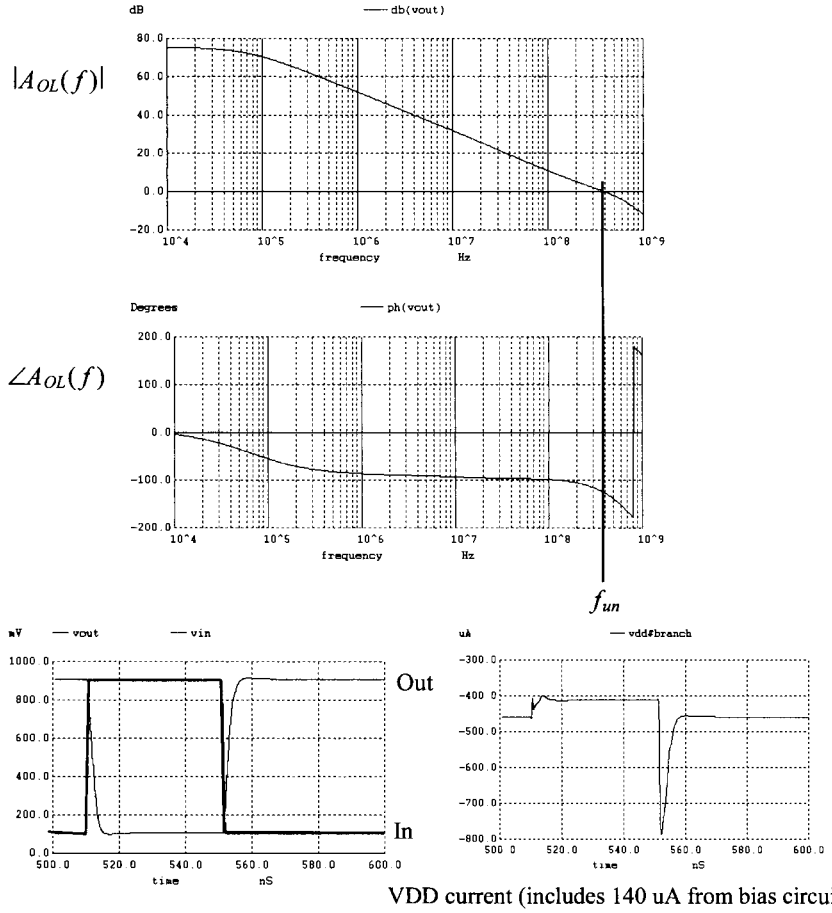


Figure 24.52 Operation of the op-amp in Fig. 24.51 driving a 1-pF load.

Compensating the Added GE Amplifiers

When we generated the simulations in Fig. 24.52, we didn't have compensation capacitors on the output of the added GE OTAs (N and P); that is, C_{cGE} were zero. The problem with this is that the resulting feedback loops aren't necessarily stable. As seen in Fig. 24.52, the step response shows some overshoot (indicating a low phase margin). Also, the frequency response isn't as monotonic as we would like (–20 dB/dec) around f_{un}. As with any feedback structure, compensation is important. *So we need to add capacitors to the outputs of the GE OTAs.* Figure 24.53 shows the response of the op-amp in Fig. 24.51 when C_{cGE}s are set to 240 fF (the GE OTAs then have f_{un} of 100 MHz, as calculated using Eq. (24.44)). The frequency response is more monotonic and the step response doesn't show overshoot and ringing. The gain-bandwidth product of the op-amp is 400 MHz. Note, it may be useful to regenerate Fig. 24.53, using larger values of C_{cGE}, to prove to oneself that indeed the bandwidth of the added GE amplifiers isn't critical. Also, it may be useful to replace the basic diff-amps with higher-gain OTAs to show that the low-frequency gain of the op-amp does indeed increase as Eq. (24.58) shows.



VDD current (includes 140 uA from bias circuit).

Figure 24.53 Operation of the op-amp in Fig. 24.51 driving a 1-pF load with GE compensation capacitors of 240 fF.

24.5 Some Examples and Discussions

A Voltage Regulator

One of the applications of an op-amp is in regulating a voltage on-chip. Figure 24.54 shows the basic topology. A voltage reference is used with the op-amp to generate a regulated voltage, V_{REG}. If the voltage reference is stable with temperature, the fact that the V_{REG} is a function of a ratio of resistors (so process or temperature changes in the resistance value don't affect the ratio) and the variation in the op-amp's open loop gain is desensitized using feedback makes the regulated voltage stable with process and temperature changes. The ideal (meaning that the op-amp has infinite open-loop gain) regulated voltage is

$$V_{REG} = V_{REF} \cdot \left(1 + \frac{R_A}{R_B}\right) \tag{24.62}$$

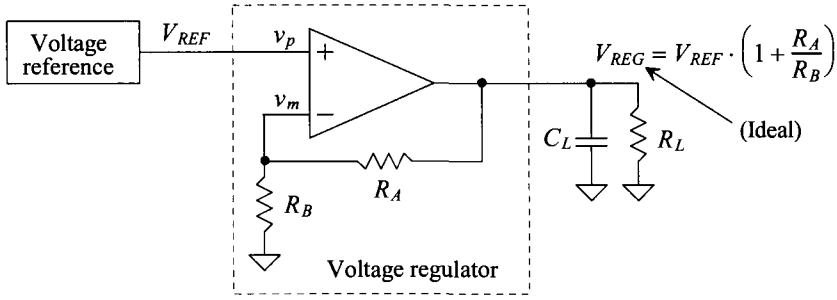


Figure 24.54 Schematic of a voltage regulator.

If the op-amp's open-loop gain is finite, then we can write

$$V_{REG} = A_{OL} \cdot (v_p - v_m) \tag{24.63}$$

and

$$v_m = V_{REG} \cdot \frac{R_B}{R_A + R_B} \text{ and } v_p = V_{REF} \tag{24.64}$$

Solving for the actual regulated voltage, gives

$$V_{REG} = V_{REF} \cdot \frac{1}{\frac{1}{A_{OL}} + \frac{R_B}{R_A + R_B}} \tag{24.65}$$

noting that when A_{OL} is infinite (or very large) this equation simplifies to Eq. (24.62). Equation (24.65) can be very revealing. Let's say that V_{REF} is 500 mV, R_B is an open, and R_A is a short (the op-amp is a voltage follower). Ideally, V_{REG} is also 500 mV. If we use a diff-amp with an open-loop gain of 20, then the actual regulated voltage is

$$V_{REG} = 0.5 \cdot \frac{1}{1.05} = 476\ mV \tag{24.66}$$

This simple example illustrates *why open-loop gain is important.* When op-amps are used in data converters (discussed in Chs. 28-30), they must amplify signals to within mV, which requires op-amp open-loop gains in the thousands.

Figure 24.55 shows a basic regulator topology using the two-stage op-amp. The regulator only sources current and so we've made the PMOS device, on the output, very large. One concern with using the large PMOS device is the op-amp offset (which can be considerable, see Fig. 24.4, for example). Another concern occurs when simulating. In some simulators both NRD and NRS (number of squares of implant area in the source or drain of a MOSFET) defaults to one. If the sheet resistance, rsh, is 50 ohms, then the resistance in series with the MOSFET is 100 ohms (limiting the current the MOSFET can supply). For large MOSFETs, it is generally a good idea to set NRD and NRS to zero. An example of a (large) SPICE MOSFET statement is

```
Mbig   vout   vn1   VDD   VDD   PMOS  L=1   W=10000  NRD=0   NRS=0
```

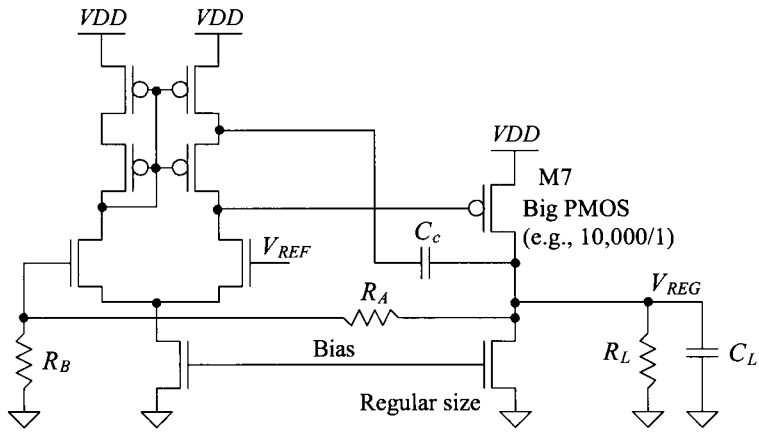


Figure 24.55 Schematic of a voltage regulator.

The point of making M7 big was to ensure that the regulator could supply a significant amount of current. However, notice that the gate of M7 cannot swing any lower (assuming that all MOSFETs remain in saturation) than

$$V_{G7,\min} = V_{REF} - V_{THN} \tag{24.67}$$

For example, if V_{REF} is 500 mV and V_{THN} is 250 mV, then the minimum voltage on the gate of M7 is 250 mV (25% of *VDD*). Ideally, we would like the gate of M7 to be able to swing to ground, fully turning it on. Towards this goal, consider the modified voltage regulator seen in Fig. 24.56. In this figure, we've used the OTA from Fig. 24.33 for the first stage of the op-amp. Now, when M5 turns on and M4 shuts off, the gate of M7 can get yanked down towards ground, allowing M7 to turn fully on.

In any practical regulator, a bypass capacitor (a big capacitor placed from V_{REG} to ground) is used to supply charge to the load for fast current transients. The required bandwidth of the regulator is reduced since the bypass capacitor (part of C_L in Figs. 24.55 and 24.56) takes care of the fast transients. It is desirable to have a large C_L for "filtering" the load's fast current needs. However, from our discussions earlier, this (large load capacitance) makes compensating the op-amp more challenging. In all of our compensation schemes, the pole associated with the output of the first stage was at a frequency much lower than the pole associated with the output stage (this was one of the reasons we used pole-splitting). To isolate the load from the second-stage gain, we might insert an NMOS source-follower (SF) between the load and the output of the second stage. The problem with this is that we won't be able to turn the SF on enough to supply significant amounts of current. Next, we might try replacing the common-source amplifier (M7) with a class AB stage (like the topology seen in Fig. 24.29). Here, again, the output won't be able to supply as much current as what we get with a full *VDD* across M7's V_{SG}. (Note that one of the reasons for using a voltage regulator is to hold V_{REG} constant even if *VDD* approaches V_{REG}.) If we must use a large load capacitor to supply charge for the fast variations in the load current and if the topology in Fig. 24.56 is used, then *we must try to compensate the op-amp with the load capacitance.*

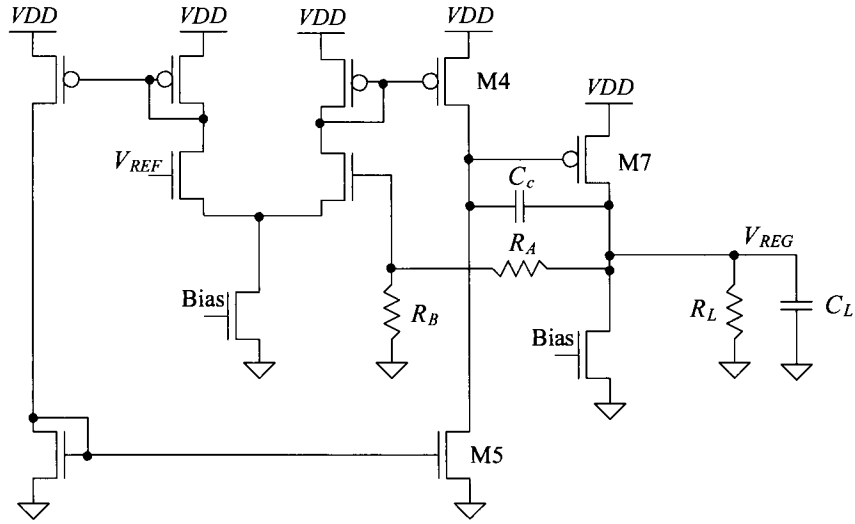


Figure 24.56 Schematic of a voltage regulator where the gate of M7 can be pulled all the way to ground.

If we are compensating the op-amp (the voltage regulator) using the load capacitance, then we've got to make sure that there is a minimum value of C_L. Further, increasing the load capacitance should make the regulator more stable, slowing the response of the op-amp. The reduction in the speed of the op-amp is offset by the fact that a larger load capacitance can supply more charge to a fast current transient before the op-amp must respond.

Why use a compensation capacitor, C_c , if we are compensating with the load capacitance? The compensation capacitor pushes the pole associated with the output node to a higher frequency (exactly what we don't want to do). We still use the capacitor (but with a smaller value) for large-signal reasons. If V_{REG} drops suddenly, the decrease in voltage is fed back directly to the gate of M7 through C_c. This turns M7 (quickly) on and allows it to pull V_{REG} back up (bypassing the slower feedback action of the op-amp). Note then that C_c is *not used* for compensating the op-amp (and actually makes the regulator more unstable). Further note that increasing the gain of the op-amp by making the first-stage gain larger (by, say, using a cascode diff-amp to increase the output resistance of the diff-amp, R_1) also hurts the regulator's stability. (By using a larger R_1, the pole associated with the output of the first stage is moved lower in frequency.)

To estimate the location of the output pole, assuming that it is the dominant pole in the system, let's calculate the closed-loop output resistance of the op-amp $R_{out,CL}$ (the open- loop output resistance is R_2). We know that the low-frequency, open-loop gain of the op-amp is

$$A_{OLDC} = \frac{v_{out}}{v_p - v_m} = g_{m1} R_1 g_{m2} R_2 \qquad (24.68)$$

If we replace the load in Fig. 24.54 with a test voltage, v_t , and note that V_{REF} (= v_p = 0) is AC ground, then with the help of Fig. 24.57 we can write

$$i_t = \frac{v_t}{R_2} + \frac{v_t}{R_A + R_B} + g_{m1}R_1 g_{m2} \cdot \frac{v_t}{A_{CL}} \tag{24.69}$$

If we assume that the current through the feedback path ($R_A + R_B$) is small, then the output resistance of the regulator is

$$R_{out,CL} \approx \frac{v_t}{i_t} = \frac{1}{\left(\frac{1}{R_2} + \frac{g_{m1}R_1 g_{m2}}{A_{CL}}\right)} \approx \frac{A_{CL}}{A_{OLDC}} \cdot R_2 \tag{24.70}$$

Our output pole is located at

$$f_2 = \frac{1}{2\pi R_{out,CL} \cdot C_L} = \frac{A_{OLDC}}{2\pi R_2 C_L \cdot A_{CL}} \tag{24.71}$$

For this pole to compensate the op-amp, we want to use a low value of open-loop gain, A_{OLDC}. Again, this means that we don't want a large value of resistance on node 1 (the output of the diff-amp). The problem with this is that the lower the open-loop gain, the more difficult it is to regulate the output voltage, as indicated in Eq. (24.66).

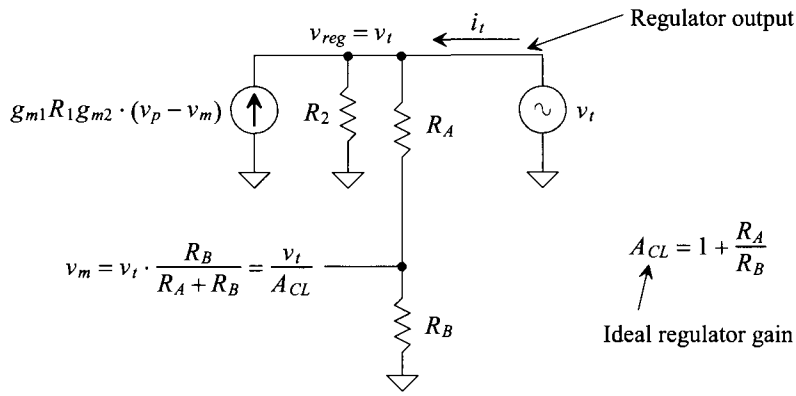


Figure 24.57 Determining the closed-loop output resistance of a two-stage op-amp.

To get an idea for the minimum size load capacitance required for a stable op-amp, let's use the parameters from Table 9.2. To begin, note that the more current the regulator supplies to a load (the more current flowing through M7), the smaller the value of R_2. This (decreasing R_2) means that the regulator becomes more likely to be unstable (f_2 increases) as it supplies more current. However, at the same time, the open-loop gain, A_{OLDC}, drops and the ability of the op-amp to regulate the output declines.

Let's assume M7's r_o and g_m are the values given in Table 9.2. Because M7 is so wide, this means (using these values for r_o and g_m) that it is conducting very little current. The value of f_1 can be estimated (assuming the $C_{gs7} >> C_c$ and the width of M7 is 10,000 or 100 times larger than the widths of the PMOS in Table 9.2) as

$$f_1 \approx \frac{1}{2\pi R_1 C_{gs7}} = \frac{1}{2\pi \cdot (167k \| 333k) \cdot 100 \cdot 8.34f} = 1.7\ MHz \tag{24.72}$$

The DC open-loop gain of the op-amp is calculated using Eq. (24.68) as 277 (no load). If we use the op-amp in the follower configuration where R_B is infinite and R_A is zero (A_{CL} is 1), then (knowing $R_2 = 167k||333k = 111k$)

$$f_2 = \frac{A_{OLDC}}{2\pi R_2 C_L \cdot A_{CL}} = \frac{277}{2\pi(111k)\cdot C_L} \tag{24.73}$$

Knowing we want $f_2 << f_1$, A_{OLDC} = 277, and f_1 = 1.7 MHz, we can set the unity-gain frequency to 1 MHz (making sure that it is less than f_1). If we want a –20 dB/decade roll-off above f_2 (now the low-frequency pole) then, as seen in Eq. (24.33), we can write

$$f_{un} = A_{OLDC} \cdot f_2 = \frac{A_{OLDC}^2}{2\pi R_2 C_{L\min} \cdot A_{CL}} = 1\ MHz \tag{24.74}$$

Solving for the minimum value of $C_{L\min}$ using these equations gives 110 nF. Clearly, this value is too large if we want the regulator to be completely on-chip. Rewriting Eq. (24.74)

$$C_{L\min} = \frac{(g_{m1}R_1 g_{m2})^2 R_2}{2\pi \cdot f_{un} \cdot A_{CL}} \tag{24.75}$$

Note that linearly increasing the current through M7 causes R_2 to decrease linearly (assuming that M7's output resistance dominates R_2) and g_{m2}^2 to increase linearly (see Eqs. (9.6) and (9.22)). The result is that $C_{L\min}$ doesn't change. However, notice what happens if we include R_L in the calculations. If $R_L << r_{o7}$, then we can write

$$\frac{C_{L\min}}{R_{L\max}} = \frac{(g_{m1}R_1 g_{m2})^2}{2\pi \cdot f_{un} \cdot A_{CL}} \tag{24.76}$$

If we select $C_{L\min} = 1000\,pF$, then $R_{L\max} = 1\,k\Omega$. We use the variable $R_{L\max}$ to indicate that this is the maximum value of load resistance possible for a stable regulator (we want the regulator to always supply at least $V_{REG}/R_{L\max}$ current). If the regulator's output voltage is 500 mV, it must be supplying at least 500 μA of current. This resistor keeps the open-loop gain low when the regulator is supplying small amounts of current. We might think, after looking at Eq. (24.73), that by supplying more current (R_L or R_2 decreasing further), the location of f_2 increases and the regulator moves towards instability. However, for further decreases in the load resistance, the current supplied by M7 increases and thus so does its g_m. What happens is this: we get the canceling of effects. As the current supplied to the output increases linearly with a linear decrease in R_L , the value of g_m^2 increases linearly and the effects cancel.

A final comment: because this design is different from the previous op-amp designs, thorough characterization using simulations is needed. Steps in the load current as well as a wide range of load capacitances and resistances should be simulated to ensure that the regulator remains stable under all possible *VDDs*, temperatures, and process shifts.

Bad Output Stage Design

In this section we'll discuss some problems with biasing in Class AB output stages. To begin, consider the op-amp design seen in Fig. 24.58. This topology is a diff-amp driving an inverter. The problem with this design is that the current flowing in the push-pull output stage (an inverter) isn't set by a bias circuit. Because of this, the current may be

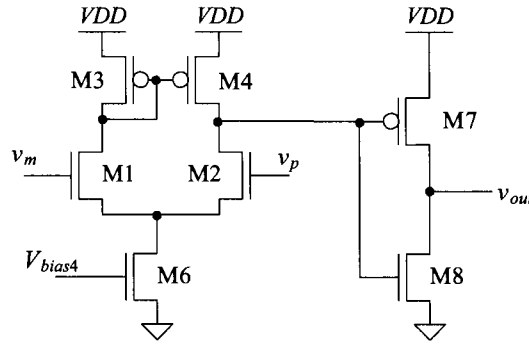


Figure 24.58 Bad op-amp design.

significant and vary greatly with both temperature and process shifts. Further, notice that when the inputs to the op-amp are equal, the drain of M4 is at the same potential as the drain of M3 (the currents in M3 and M4 are equal). This, as we've already discussed, can be used to set the bias current in M7 (we treat M7, for biasing purposes, as if its gate were tied to the gates of M3 and M4). If we call the gate potential of M7 (and thus the gate potential of M8) $VDD - V_{SG}$, then for M8 to be in saturation

$$V_{out} \geq VDD - V_{SG} - V_{THN} \tag{24.77}$$

If VDD is 1 V, $V_{SG} = 350$ mV, and $V_{THN} = 250$ mV, then V_{out} must be greater than 400 mV for M8 to be saturated. What this means is that for wide output swings, M8 will move into triode and the push-pull output amplifier gain will drop (killing the overall gain of the op-amp). What we need to do is drop the gate potential of M8 down so that its drain can swing to a lower voltage without it trioding. Towards this goal, consider adding a source-follower level shifter to the output of the op-amp, as seen in Fig. 24.59. Now the output voltage in the amplifier can swing lower without M8 trioding. However, we still aren't controlling the current in the output stage. By not controlling this current, as we've already discussed, we produce an op-amp with poor systematic, input-referred offset voltage. If, for example, we have an input-referred offset of 10 mV and the diff-amp gain is 20, then the change in the output voltage on the gate of M7 is 200 mV. This can cause

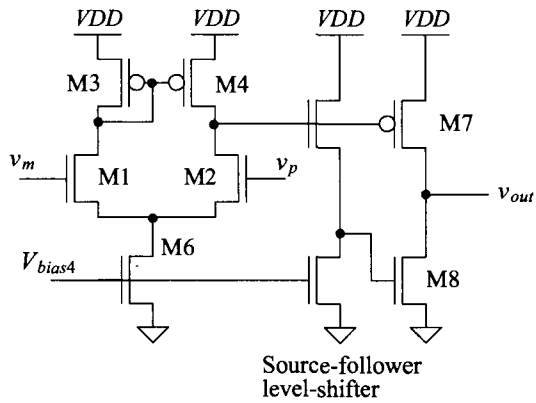


Figure 24.59 Another bad op-amp design.

the output current flowing in M7/M8 to be hundreds of μA above the current in the diff-amp.

We might try connecting the gate of M8 to the gates of M3/M4. When the noninverting input voltage, v_p , goes high, M2 turns on and causes the gate potential of M7 to drop (turning M7 further on). At the same time, the gate potential of M3 increases, causing M8 to also turn further on. The result is that M7 and M8 both turn on and fight each other for control of v_{out}. For proper operation, the gates of the output push-pull stage should move in the same direction.

To precisely control the current in the output stage, consider the topology seen in Fig. 24.60. Since, for biasing purposes, we treat the drain of M4 as if it's at the same potential as the gate of M3, the currents in M7, M9, and M10 are equal when the op-amp inputs are at the same potential. We also treat M8 as if its gate were tied to the gate of M11. The result is that the quiescent currents in M7 and M8 are equal and set by the biasing of M6. We seem to have solved the problem with biasing the class AB output stage.

However, a different problem arises. We now have three high-impedance nodes: the output of the diff-amp (a pole we've called f_1), the output of the op-amp (a pole we've called f_2), and, now, the gate of M8. If we try to make the node at the gate of M7 the dominant node, then the path that the op-amp inputs sees through M3 to M9 to the gate of M8 (the other high-impedance node) isn't affected. If we add compensation capacitors from the op-amp output to both the gates of M7 and M8, the current fed back isn't necessarily balanced. This imbalance may only be noticed when the op-amp's large signal step response is simulated. (It is generally not seen in an AC simulation.) The result is that the op-amp's settling time and stability become marginal in some situations. Having said this, the topology can still be useful in some situations (e.g., low power or low *VDD*).

In an attempt to improve or simplify the op-amp in Fig. 24.60, we might try to make M12 diode connected and remove M10/M11 from the circuit. With this change, however, we don't get class AB action (M9 mirrors the current in M3, which flows in the diode-connected M12 and is mirrored by M8). Finally, again, why not eliminate M9 and M12 followed by connecting the gate of M8 to the diode-connected M11? The gate potentials of M8 and M7 would then move in opposite directions, causing M7 to fight with M8 for control of the output voltage.

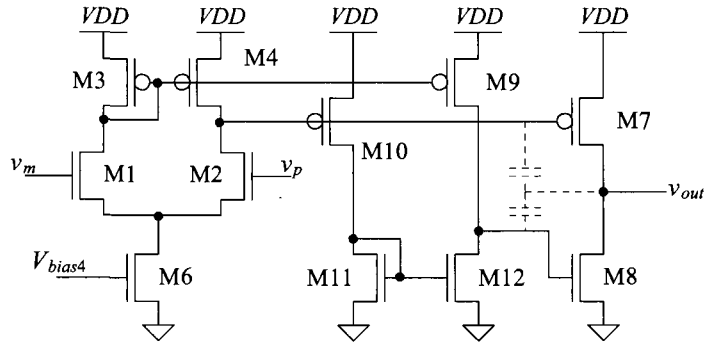
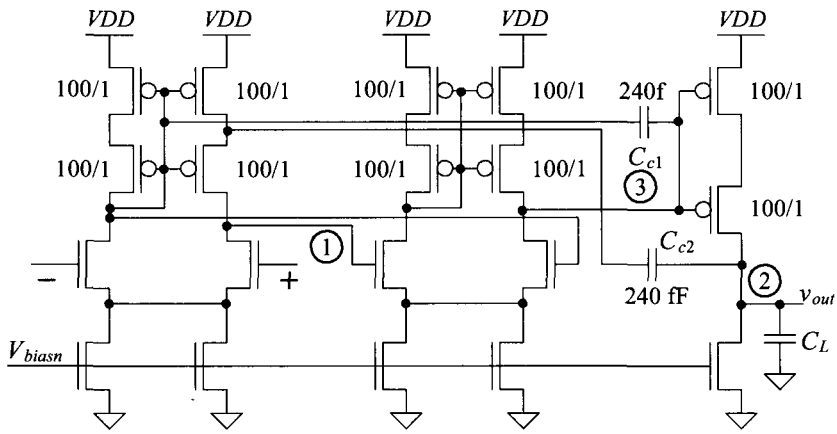


Figure 24.60 Controlling the current in a class AB output stage.

Three-Stage Op-Amp Design

In some applications we need an op-amp that can operate with a low power-supply voltage or with minimal power from *VDD*. The bias circuit we developed in Fig. 20.47 can pull more current from *VDD* than the op-amp it biases. (So, if possible, use the same bias circuit for multiple op-amps, if power and layout area are of concern.) If we look at the heart of this bias circuit (Fig. 20.47) and its operation, the Beta-multiplier in Figs. 20.22 and 20.23, we see that *VDD* can be decreased down to 500 mV with the bias currents relatively unaffected. The problem in using a *VDD* which is half of the normal *VDD* (= 1 V) is that our class AB output stage (Fig. 24.44 for example) fails to operate. For proper operation of the class AB output stage using the floating current sources (biased with V_{ncas} and V_{pcas}), we need a *VDD* > 800 mV (perhaps higher over process corners and temperature). Also, as already discussed, if we connect a resistive load to the output of the two-stage op-amp in Fig. 24.2, the gain is reduced.

Towards keeping a large gain and lowering the power supply voltage, consider the three-stage op-amp in Fig. 24.61. This design is a cascade of two diff-amps followed by a common-source amplifier. If we connect a resistive load to the output of the common-source stage, the overall op-amp gain remains relatively high due to the cascaded gain of the diff-amps. The concern with this topology (an op-amp with more than two stages), as alluded to earlier, is compensation. We still compensate the op-amp so that the pole associated with node 1 is dominant. The nesting of the compensation capacitors within the op-amp in Fig. 24.61 is sometimes called *nested Miller compensation*. We'll avoid the use of this label here since we aren't strictly using Miller compensation (Fig. 24.8 among others) but rather the indirect compensation method discussed earlier (see Fig. 24.18 and the associated discussion). Note how the current through C_{c1} feeds back to node 1 through the diode-connected load of the input diff-amp. This is necessary to ensure that the signal through C_{c1} adds with the signal fed back directly to node 1 through C_{c2}.



Bias circuit in Fig. 20.22.
See Table 9.2.

Figure 24.61 A three-stage op-amp.

Because of pole-splitting, the location of the pole at node 3 (the output of the second diff-amp) is pushed out to, see Eq. (24.24),

$$f_3 = \frac{g_{mn} \cdot C_{c1}}{2\pi \cdot C_1(C_{L2} + C_{c1})} \approx \frac{g_{mn}}{2\pi C_1} \tag{24.78}$$

a large frequency. Here we are assuming that the transconductance of the second diff-amp is g_{mn} and that C_{c1} is much larger than the input capacitance of common-source amplifier (which is the second diff-amp's C_{L2}). The location of the pole on the output of the amplifier is still given by

$$f_2 = \frac{g_{mp} \cdot C_{c2}}{2\pi \cdot C_1(C_L + C_{c2})} \tag{24.79}$$

where g_{mp} is the transconductance of the common-source amplifier. Note that we aren't discussing the LHP zeroes whose locations are specified using Eq. (24.22). We'll discuss these zeroes in a moment. We'll compensate, as usual, the op-amp so that the unity-gain frequency is less than the frequencies of the poles at f_2 and f_3.

The low-frequency, open-loop gain of the op-amp is given by

$$A_{OLDC} = \overbrace{g_{mn}(r_{on}||r_{op})}^{\text{first diff-amp's gain, } A_1} \cdot \overbrace{g_{mn}(r_{on}||r_{op})}^{\text{second diff-amp's gain, } A_2} \cdot \overbrace{g_{mp}(r_{on}||r_{op})}^{\text{common-source gain, } A_3} \tag{24.80}$$

At frequencies above the op-amp's f_{3dB} and below the gain-bandwidth product (the unity-gain frequency, f_{un}), the gain of the first-stage is rolling off. For all intents and purposes, the AC signal on the output of the first diff-amp is considerably smaller than the AC outputs of the second or third stages. In this situation the current fed back to node 1, knowing that the output voltage of the second diff-amp (at node 3) is v_{out}/A_3 , is

$$i_{Cctot} \approx \frac{v_{out}}{1/j\omega C_{c2}} + \frac{v_{out}/A_3}{1/j\omega C_{c1}} \tag{24.81}$$

The output current of the diff-amp is

$$i_{out1} = g_{mn}(v_p - v_m) \tag{24.82}$$

Because this current must equal the current fed back to node 1, we can equate Eqs. (24.81) and (24.82) to write

$$\frac{v_{out}}{v_p - v_m} = \frac{g_{mn}}{j\omega(C_{c2} + C_{c1}/A_3)} \tag{24.83}$$

The unity-gain frequency is then

$$f_{un} = \frac{g_{mn}}{2\pi(C_{c2} + C_{c1}/A_3)} \approx \frac{g_{mn}}{2\pi C_{c2}} \tag{24.84}$$

noting that the unity-gain frequency is a function of the third-stage gain. Here, we'll set C_{c2} to 240 fF to get a unity-gain frequency of 100 MHz. We still need C_{c1} to push node 3's pole to a higher frequency (pole splitting). We'll also set C_{c1} to 240 fF.

Figure 24.62 shows the frequency response of the op-amp in Fig. 24.61 without driving a load capacitance. As designed for using Eq. (24.84), the unity-gain frequency is 100 MHz. Also, as specified in Eqs. (24.22) and (24.25), we have zeroes around the unity-gain frequency. It appears from the frequency response in Fig. 24.62 that the zeroes

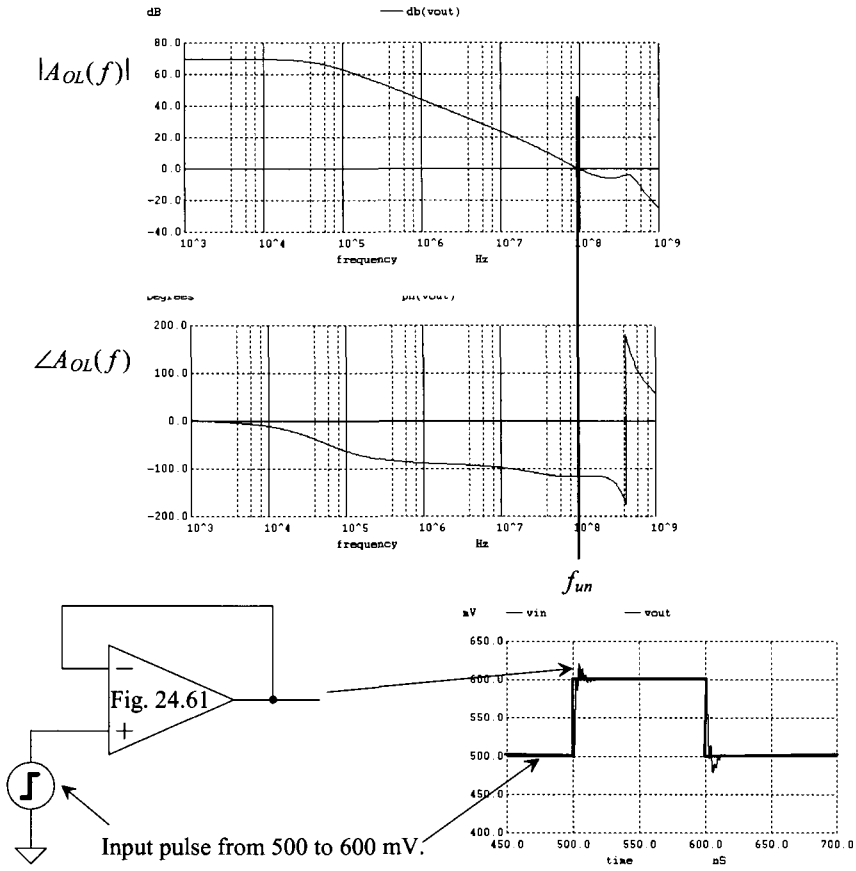


Figure 24.62 Unloaded AC and step responses for the op-amp in Fig. 24.61.

occur above the unity-gain frequency and cause the open-loop response to flatten out. What this indicates is that one of the zeroes is canceling one of the higher-frequency poles. Note that the PM is 45°. The step response seen in Fig. 24.62 shows the characteristic ringing associated with a PM of 45°.

If we drive a load capacitance, then we expect the third-stage gain, A_3, to start to decrease at a lower frequency (it starts to decrease sooner with increasing frequency). Looking at Eq. (24.84), we then expect f_{un} to drop in value. Figure 24.63 shows the simulation where the op-amp in Fig. 24.61 is driving a 1 pF load. As expected, the addition of the 1 pF load causes f_{un} to drop in value. The PM is approximately 25°. With such a low PM, we expect the output to show significant ringing (and, as seen in Fig. 24.63, it does). To increase the PM, we can increase the value of the compensation capacitor. We can increase C_{c2} to, say, 2400 fF, for a unity gain frequency of (roughly) 10 MHz. We don't necessarily need to increase C_{c1} to decrease f_{un}, as seen in Eq. (24.84).

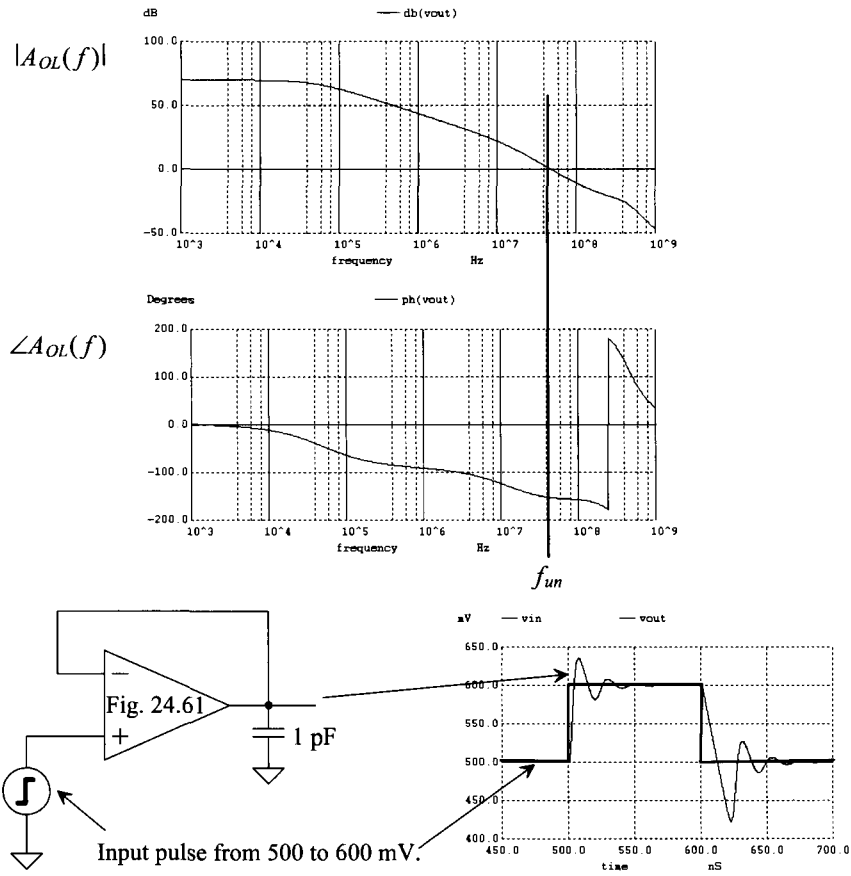


Figure 24.63 AC and step responses for the op-amp in Fig. 24.61 driving 1 pF.

Finally, why did we choose the topology seen in Fig. 24.61 for our three-stage op-amp example? The main reason for using this topology comes from biasing the common-source stage. If we were to replace the second diff-amp with a common-source stage (so our last two stages in the op-amp are common-source amplifiers), we wouldn't have a known second stage output voltage to bias the final common-source stage. The exact output voltage of a common-source amplifier, without feedback to set it, is unknown (the two drains of the NMOS and PMOS will either float up or float down, depending on which device is sourcing or sinking the most current). By using the diff-amp stages, as seen in Fig. 22.8, we ensure that each stage is biased with a known current. We don't use a diff-amp for the final stage of the op-amp because of the diff-amp's limited output swing.

Another benefit of using two diff-amps on the input of the op-amp is the increase in the *CMRR*. The overall common-mode gain is the product of each diff-amp's common-mode gain. If a single diff-amp has a *CMRR* of 80 dB, then the cascade of two diff-amps results in a *CMRR* of 160 dB.

ADDITIONAL READING

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PROBLEMS

24.1 Suggest, and verify with simulations, a method for reducing the minimum input common-mode voltage of the op-amp in Fig. 24.2.

24.2 Redesign the bias circuit for the op-amp in Fig. 24.2 for minimum power. Compare the power dissipation of your new op-amp design (actually the bias circuit) to the design in Fig. 24.2. Using your redesign, generate the plots seen in Fig. 24.3.

24.3 Show, using simulations, how a 1% mismatch in the widths of M1 and M2 in the op-amp of Fig. 24.2 affect the op-amp's input-referred offset voltage. Compare this offset to the offset caused by a 1% mismatch in the widths of M3 and M4. Quantitatively explain why one is worse than the other.

24.4 Simulate the use of the "zero-nulling" circuit in Fig. 24.15 in the op-amp of Fig. 24.8. Show AC, operating-point, and transient (step) operation of the resulting op-amp. Verify with the .op analysis that the gate of MP1 is at the same potential as the gate of M7 in quiescent conditions.

24.5 When we derived Eq. (24.24), we lumped C_c into C_2 and neglected the effects of MCG. A more accurate model for the indirect compensation, assuming $C_L >>$ the output capacitance of the amplifier, is seen in Fig. 24.64. Using this model, estimate the location of the output pole.

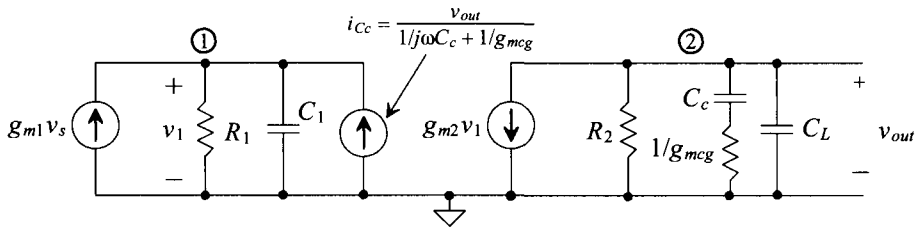

Figure 24.64 Model used to estimate bandwidth when indirect feedback current. See Problem 24.5.

24.6 Regenerate Fig. 24.19 using a 2.4 pF compensation capacitor. On the resulting simulation output, label the location f_1 , f_2 , f_z , and f_{un}. How do the simulated results compare to the hand calculated values?

24.7 For the op-amp in Fig. 24.21, determine the *CMRR* using hand calculations. Verify your hand calculations using simulations. How does the *CMRR* change based on the DC common-mode voltage?

24.8 Simulate the *PSRR*s for the op-amp in Fig. 24.8 (with an R_z of 6.5k and a C_c of 2.4 pF) and compare the results to the op-amp in Fig. 24.21 when C_c is set to (also) 2.4 pF (so each op-amp has the same gain-bandwidth).

24.9 Simulate the operation of the op-amp in Fig. 24.28. Show the open-loop frequency response of the op-amp. What is the op-amp's PM? Show the op-amp's step response when it is put into a follower configuration driving a 100 fF load with an input step in voltage from 100 mV to 900 mV.

24.10 The op-amp seen in Fig. 24.29 has a gain-bandwidth product (f_{un}) of about 100 MHz. Suppose that this op-amp is used in the amplifier seen in Fig. 24.65 (gain of −5). Estimate the amplifier's closed loop bandwidth (where the output of the amplifier is −3 dB down from its low-frequency value) using Eq. (24.34). Verify your results using simulations (transient analysis). What are the maximum and minimum voltages allowable for an input sinewave if the output voltage of the amplifier must lie between 100 and 900 mV?

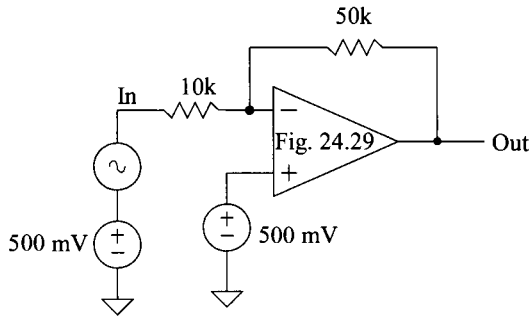

Figure 24.65 Amplifier used for Problem 24.10.

24.11 Suppose it is decided to eliminate the 500 mV common-mode voltage in the amplifier seen in Fig. 24.65 and use ground, as seen in Fig. 24.66. Knowing that the input voltage can only fall between ground and *VDD*, what is the problem one will encounter?

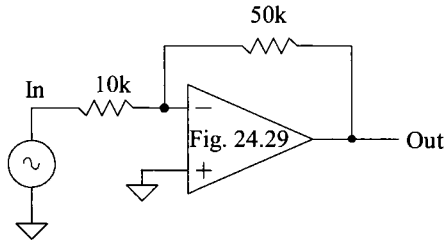

Figure 24.66 Amplifier used for Problem 24.11. What's wrong with this topology?

24.12 To limit the current flowing in MOP or MON in the op-amp of Fig. 24.29 (to protect the op-amp from destruction if its output is shorted to ground, for example), we may add 100 Ω resistors, as seen in Fig. 24.67. What is the maximum amount of current this modified op-amp can source/sink? How is the closed-loop output resistance of the op-amp affected. (Hint: see Eq. (24.70).) Simulate the operation of the op-amp using the topology seen in Fig. 24.31. Is there any noticeable difference between the simulation output in Fig. 24.31 and the output with the 100 Ω resistors present?

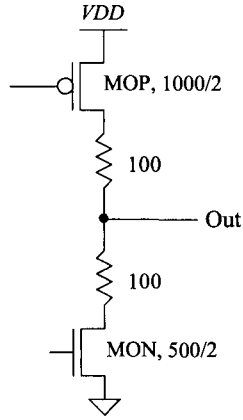

Figure 24.67 Adding resistors to the output of the op-amp in Fig. 24.29 for short circuit protection. See Problem 24.12.

24.13 Resimulate the OTA in Fig. 24.33 driving a 1 pF load (to determine f_{un}) if K = 10. How do the simulation results compare to the hand calculations using Eq. (24.41)? Estimate the parasitic poles associated with the gates of M4 and M5 (for example, the pole associated with the gate of M4 is $\approx 1/g_{m41} \cdot C_{sg4}$). Are these poles comparable to f_{un}?

24.14 Using the OTA in Fig. 24.35, design a lowpass filter with a 3 dB frequency of 1 MHz.

24.15 Suppose M8T in the op-amp of Fig. 24.37 is removed and replaced with a short from the output to the drain of M8B. How will the gain be affected? Verify your answer with SPICE.

24.16 Suppose, to simulate the open-loop gain of an OTA, the big resistor and capacitor used in Fig. 24.43 are removed and the inverting input is connected to 500 mV. Will this work? Why or why not? What happens if the OTA doesn't have an offset voltage? Will it work then?

24.17 Why is the noninverting topology (Fig. 24.49) inherently faster than the inverting topology (Fig. 24.39). What are the feedback factors, β, for each topology. Use the op-amp in Fig. 24.48 to compare the settling times for a +1 and a −1 amplifier driving 10 pF.

24.18 Suppose, to reduce power, the lengths of the current sources used in the amplifiers seen in Fig. 24.50 are increased from 2 to 10. Will the AC performance of the op-amp used to generate Fig. 24.53 change with this modification? Why or why not? Verify your answer using a SPICE simulation. Compare the currents used in the modified op-amp (with the lower power GE diff-amps) to the current seen in Fig. 24.53.

24.19 To increase the gain of the op-amp in Fig. 24.51, we may replace the GE diff-amps with folded-cascode OTAs. Will we need source-follower level-shifters

in the new design? Regenerate the simulation data seen in Fig. 24.53 using the folded-cascode OTAs.

24.20 Suppose an op-amp is to be used to amplify 250 mV to 500 mV with an error less than 1 mV. Estimate the minimum required op-amp open loop gain.

24.21 Design a voltage regulator to supply at least 50 mA of current at 500 mV with a *VDD* as low as 600 mV. Assume that a 500 mV voltage reference is available and that the load capacitance is, minimum, 1,000 pF. How does the design respond to a load current pulse from 0 to 50 mA? Use SPICE to verify your design.

24.22 Using the nominal sizes from Table 9.2 and the bias circuit in Fig. 20.47, simulate, using an .op analysis, the operation of the op-amp in Fig. 24.58 in the configuration seen in Fig. 24.9. What is the current flowing in M7 and M8 when *VDD* is 1 V? is 1.2 V?

24.23 Repeat Problem 24.22 for the op-amp in Fig. 24.59.

24.24 Using the information from Table 9.2 and the bias circuit in Fig. 20.47, demonstrate the operation (AC and transient) of the op-amp in Fig. 24.60 driving a 100 fF load. Show that the bias current pulled from *VDD* is relatively constant for a *VDD* of 1 or 1.2 V (put the op-amp in the configuration seen in Fig. 24.9).

24.25 Replace the common-source output stage in the op-amp of Fig. 24.61 with a class AB output stage like the one seen in Fig. 24.60. Simulate the operation of the amplifier (AC and transient).