USBPulse Registers

			7	6	5	4	3	2	1	0
0	SUR1	W-R	ClockMaster	TrigMaster	TrigManual		Counter Reset	Counter Bypass	Arm	Run
1	SUR2	W-R	J1 8 Drive	J1 7 Drive	J1 6 Drive	J1 8 Dir	J1 7 Dir	J1 6 Dir	Enable	Invert
2	SUR3	W-R							OneShot	Random
3	DACAR	W-R							DAC Address	
4	DACDR	W-R	DAC Data							
5	X0R	R	Pulse Repetition Period[7:0]							
6	X1R	R	Pulse Repetition Period[15:8]							
7	X2R	R	Pulse Repetition Period[23:16]							
8	X3R	R					Pulse Repetition Period[27:24]			
9	SR1	R	J1 8 sense	J1 7 sense	J1 6 sense			Raw Trig	Triggered	Run
10	MISCPLLCR	W-R		LED Control		PLL Mode	PLL S Update	PLL S Din	PLL S Shift	PLL S Clk
11										
12										
13										
14	REVR	R	FPGA Type			FPGA Revision				
15	Y0R	W-R	Pulse Start[7:0]							
16	Y1R	W-R	Pulse Start[15:8]							
17	Y2R	W-R	Pulse Start[23:16]							
18	Y3R	W-R					Pulse Start[27:24]			
19	Z0R	W-R	Pulse Stop[7:0]							
20	Z1R	W-R	Pulse Stop[15:8]							
21	Z2R	W-R	Pulse Stop[23:16]							
22	Z3R	W-R					Pulse Stop[27:24]			