Very High-Level View of a Computer Central Processing Unit (CPU) Main Memory Input/output (IO) DevicesIIICPU – execute instructionsIMemory – store program & dataIIO devices –System Bus 2

The components from which computers are built, i.e., computer organizationIIIn contrast, computer a Computer Architecture vs Organization

Computer architecture is the "what"—the logical design and programmer's view, defining the instructi Computer Architecture vs Organization

Computer architecture as the architect's blueprint for a building. It defines what the system needs Computer Architecture vs Organization

Computer Organization concerns about how the components are physically arranged and interconnected t Computer Architecture vs Organization

I VonINeumannIarchitectureIcomputerIisIalso referredItoIasIIASI(InstituteIforIAdvanced Studies, Princeton, US) computer.IComputer Structure o

I TheIclassicIdescriptionIof aIIcomputer's organizationIisIattributedItoIJohnIvon Neumann (1903-1957).ITheIvonINeumannImodelIisIcharacterizedIby five major subsystems:IMe

6 Memory Processor (CPU) Input-Output Control Unit ALU Store data and program Execute program Bus

I CPU - central processing unit: Decisions are made,IComputations are performed,IInput/output requests are performed.IMemory: Stor

The two main functions of the processor are control and arithmetic/logic.ITheseIareIrepresentedIbyI The ALU includes registers and circuits for doing the basic arithmetic and logical operations.IRegi

IIThe task of the control unit is to carry out the fetch- execute cycle over and over and over agai Fetch the next instruction from memory.IDecode the instruction.IExecute the instruction.IThe control

All instructions and data are stored in memory.IMemory is random access - RAM - in that any locati

I The shared bus between the program memory and data memoryIII Executes instructions seriallyII

I Established by Harvard MarkIII Facilitates to store codes and data in a separate I memoryIII Harvard Architecture

Harvard Architecture

Key Differences:

Main-memories (RAM) generally store and recall rows.IRows are multi-byte in length, e.g. 16-bit word = 2 bytesI32-bit word = 4 bytes mainImemoryIbyte-addressableIrather I

MostIcomputerIarchitecturesIhowever,ImakeIthan word addressable.II In such architectures the CPU and/or the Main Memory hardware is capable of rea
IIAnIexampleIofIaIMainImemoryIwithI16-bitImemory locations.
IINoteIhowItheImemoryIlocationsI(rows)IhaveIeven addresses.
In order to be able to move a word in and out of the memory, a distinct address has to be assigned
Three basic steps are needed in order for the CPU to perform a write operation into a specified mem
The address of the location from which the word is to be read is loaded into the MAR.IA signal, cal
Time period taken by the processor to fetch data or instruction through the bus from the memory is
CPU puts address of the instruction on the bus to be fetched.ICPU generates the control signal (i.e
NumberIofIstatesIrequiredItoIcompleteIone machine cycle.IState is changed only after one comple
All the circuits in the CPU are synchronized by the system clock.IThe speed of a computer processor
Fast, powerful CPUs need quick and easy access to large amounts of data in order to maximize their
The CPU accesses memory according to a distinct hierarchy.IWhether it comes from permanent storage
A,Ispecial,Ihigh-speedIstorageIareaIwithinIthe CPU.IAll data must be represented in a register befo
For example a 32-bit CPU is one in which each register is 32 bits wide.ITherefore, each CPU instruc
A register is a memory location within the CPU itself, designed to be quickly accessed for purpose
This register is used to hold the memory address of the next instruction that has to executed in a
This is used to hold the current instruction in the processor while it is being decoded and execut
I The accumulator is used to hold the result of operations performed by the arithmetic and logic u
I Used forIstorageIofImemoryIaddresses, usually the addresses involved in the instructions held in the instruction register.II The control
I These registers have no specific purpose, but are generally used for the quick storage of

pieces

Sample Program 41 100I101I102II103 104I105 Program memory 18 19I20 21IIData memory

Instruction Execution Sequence 42 Fetch next instruction from memory to IRIChange PC to point to next instructionIDetermine type of in

20 Before execution of 1st fetch cycle A E D C B ALU Address Bus Control Unit IR FLAG ALU 100 +1 Data Bus CTRL Bus

After 1st fetch cycle … 44 A E D C B ALU Address Bus Control Unit Load A,10 FLAG ALU 101 +1 Data Bus CTRL Bus

After 1st instruction cycle … 45 10 E D C B ALU Address Bus Control Unit Load A,10 FLAG ALU 101 +1 Data Bus CTRL Bus

Sample Program (Cont.) 23

After 2nd fetch cycle … 47 A E D C B ALU Address Bus Control Unit Load B,15 FLAG ALU 102 +1 Data Bus CTRL Bus

After 2nd instruction cycle … 48 10 E D C 15 ALU Address Bus Control Unit Load B,15 FLAG ALU 102 +1 Data Bus CTRL Bus

Sample Program (Cont.) 26

After 3rdIfetch cycle … 50 10 E D C 15 ALU Address Bus Control Unit ADD A,B FLAG ALU 103 +1 Data Bus CTRL Bus

After 3rdIinstruction cycle … 51 25 E D C 15 ALU Address Bus Control Unit ADD A,B FLAG ALU 103 +1 Data Bus CTRL Bus

Thank You