

Very High-Level View of a Computer

Central Processing Unit (CPU)

Main Memory

Input/output (IO) Devices ■■■ CPU – execute instructions ■ Memory – store program & data ■ IO devices –

System Bus

The components from which computers are built, i.e., computer organization ■■ In contrast, computer architecture ■■

Computer Architecture vs Organization

Computer architecture is the "what"—the logical design and programmer's view, defining the instructi
Computer Architecture vs Organization

Computer architecture as the architect's blueprint for a building. It defines what the system needs
Computer Architecture vs Organization

Computer Organization concerns about how the components are physically arranged and interconnected to

Computer Architecture vs Organization

■ Von■Neumann■architecture■computer■is■also

referred■to■as■IAS■(Institute■for■Advanced Studies, Princeton, US) computer.■Computer Structure c

■ The classic description of

a computer's organization is attributed to John von

Neumann (1903-1957). The von Neumann model is characterized by five major subsystems: Memory

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Memory

Processor (CPU)

Input-Output

Control Unit

ALU

Store data and program

Execute program

Bus

■ CPU - central processing unit:

Decisions are made, ■ Computations are performed, ■ Input/output requests are performed. ■ Memory: Store

The two main functions of the processor are control and arithmetic/logic. These are represented by the ALU and the Register File. The ALU includes registers and circuits for doing the basic arithmetic and logical operations. The Register File includes registers for storing data and instructions.

■ ■ The task of the control unit is to carry out the fetch- execute cycle over and over and over again
Fetch the next instruction from memory. ■ Decode the instruction. ■ Execute the instruction. ■ The control

All instructions and data are stored in memory. ■ Memory is random access - RAM - in that any locati

■ The shared bus between the program memory and data memory ■ ■ ■ Executes instructions serially ■ ■ ■

■ Established by Harvard Mark ■ ■ ■ Facilitates to store codes and data in a separate ■ memory ■ ■ ■
Harvard Architecture

Key Differences:

Main-memories (RAM) generally store and recall rows. ■ Rows are multi-byte in length, e.g.

16-bit word = 2 bytes ■ 32-bit word = 4 bytes

main ■ memory ■ byte-addressable ■ rather

■ Most ■ computer ■ architectures ■ however, ■ make ■ than

word addressable. ■ ■ In such architectures the CPU and/or the Main Memory hardware is capable of rea

■ ■ An ■ example ■ of ■ a ■ Main ■ memory ■ with ■ 16-bit ■ memory locations.

■ ■ Note ■ how ■ the ■ memory ■ locations ■ (rows) ■ have ■ even addresses.

In order to be able to move a word in and out of the memory, a distinct address has to be assigned

Three basic steps are needed in order for the CPU to perform a write operation into a specified mem

The address of the location from which the word is to be read is loaded into the MAR. ■ A signal, called

Time period taken by the processor to fetch data or instruction through the bus from the memory is

CPU puts address of the instruction on the bus to be fetched.■CPU generates the control signal (i.e

Number of states required to complete one machine cycle. State is changed only after one complete

All the circuits in the CPU are synchronized by the system clock.■The speed of a computer processor

Fast, powerful CPUs need quick and easy access to large amounts of data in order to maximize their

The CPU accesses memory according to a distinct hierarchy.■Whether it comes from permanent storage

A, ■special, ■high-speed ■storage ■area ■within ■the CPU. ■All data must be represented in a register before

For example a 32-bit CPU is one in which each register is 32 bits wide.■Therefore, each CPU instruc

A register is a memory location within the CPU itself, designed to be quickly accessed for purpose

This register is used to hold the memory address of the next instruction that has to be executed in a

This is used to hold the current instruction in the processor while it is being decoded and executed

■ The accumulator is used to hold the result of operations performed by the arithmetic and logic u

■ Used

for ■ storage ■ of ■ memory ■ addresses,

usually the addresses involved in the instructions held in the instruction register. ■ ■ The control

■ These registers have no specific purpose, but are generally used for the quick storage of pieces

Sample Program

41

100■101■102■■103

104■105

Program memory

18

19■20

21■■Data memory

Instruction Execution Sequence

42

Fetch next instruction from memory to IR ■ Change PC to point to next instruction ■ Determine type of in

20

Before execution of 1st fetch cycle

A

E

D

C

B

ALU

Address Bus

Control Unit

IR

FLAG

ALU

100

+1

Data Bus

CTRL Bus

After 1st fetch cycle ...

44

A

E

D

C

B

ALU

Address Bus

Control Unit

Load A,10

FLAG

ALU

101

+1

Data Bus

CTRL Bus

After 1st instruction cycle ...

45

10

E

D

C

B

ALU

Address Bus

Control Unit

Load A,10

FLAG

ALU

101

+1

Data Bus

CTRL Bus

After 2nd fetch cycle ...

47

A

E

D

C

B

ALU

Address Bus

Control Unit

Load B,15

FLAG

ALU

102

+1

Data Bus

CTRL Bus

After 2nd instruction cycle ...

48

10

E

D

C

15

ALU

Address Bus

Control Unit

Load B,15

FLAG

ALU

102

+1

Data Bus

CTRL Bus

After 3rd fetch cycle ...

50

10

E

D

C

15

ALU

Address Bus

Control Unit

ADD A,B

FLAG

ALU

103

+1

Data Bus

CTRL Bus

After 3rd instruction cycle ...

51

25

E

D

C

15

ALU

Address Bus

Control Unit

ADD A,B

FLAG

ALU

103

+1

Data Bus

CTRL Bus

Thank You