IC Package Design

Presented by

Oommen Mathews

World's First SEI CMM LEVEL 5 Software Services Company

Wipro Technologies
Innovative Solutions. Quality Leadership.

IC Package Design

Pre-requisites

- Familiar with PCB/VLSI Layout concepts
- Familiar with IC Packaging concepts

Agenda

- Name of the course: IC Package Design
- Duration: 3 hours
- Topic - IC Package Design Flow

References

- "ASIC Packaging Guidebook" from THOSHIBA Corporation
- "Microelectronics System Packaging" from IISc Bangalore
- "ASIC Packaging" by Sanjay Dandia
- http://www.amkor.com/Products/all_datasheets (Packaging Datasheets)
- "Design Guidelines for LTCC" from Kyocera Corporation

IC Package Design - Introduction

Purpose of Semi-Conductor Packaging

- *The purpose of IC packaging is to protect the silicon chip from outside environment without sacrificing the chip performance.*

Package – Major Functions

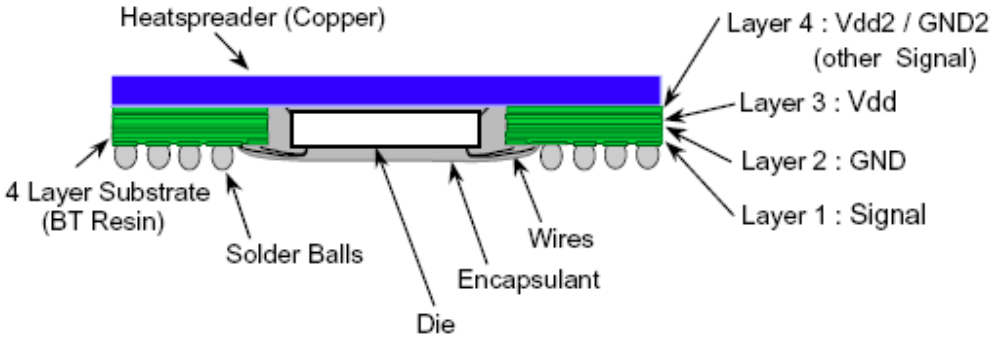
- *Protection (Mechanical, Chemical, and Electromagnetic)*
- *Enabling electrical connectivity*
- *Heat dissipation*
- *Space transformer*
- *Improve handling*

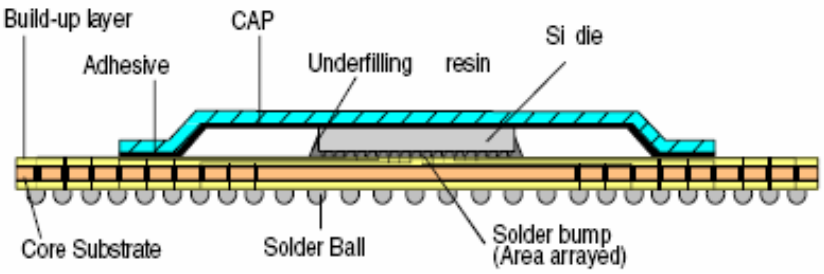
IC Package Design – Normal Considerations

- ***Package - Normal consideration***
  - *Cost*
  - *Physical attributes (Form factor, Routing density, etc.)*
  - *IC-Package interface (Pad pitch, Pad placement, etc.)*
  - *Package to PCB interface (Pinout, Routing etc.)*
  - *Power delivery and dissipation*
  - *Signal Integrity*
  - *Thermal Design*
  - *Mechanical Integrity (Cracking, Shock, Bending, etc.)*
  - *Manufacturability, Reliability, Testing, Handling, etc.*
- ***Generic / Open tool package***
  - *Package is tooled before the die*
  - *Select proper packageIC-Package interface (Pad pitch, Pad placement, etc.)*
- ***Custom package***
  - *Package is tooled with the die*
  - *Optimum performance*

Package Physical Parameters

Substrate Material	Ceramic	Organic	No Substrate
Die-Attach	Cavity-up	Cavity-down	Stacked
Die-Package Bonding	Wire-bond	TAB	Flip-chip
Encapsulation	Hermetic		Non-Hermetic
Package-PCB Attach	Leads/Pins	Balls	No Leads
Thermal Management	Heat Spreader		Thermal Vias
Package Size	Large	Small/Thin	Chip Scale



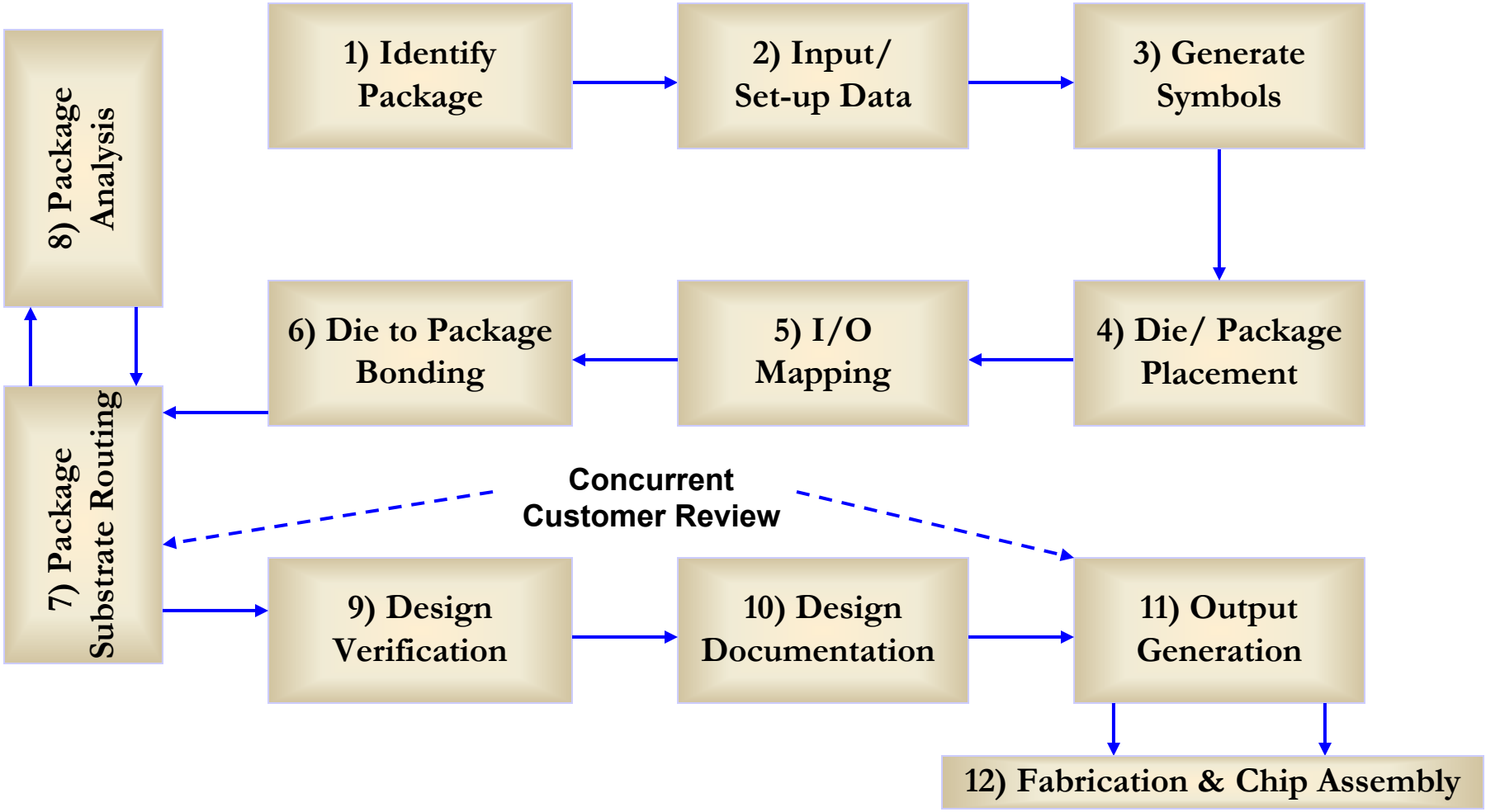


Tools Usage

- ***Primary Tools (Cadence)***
  - *Allegro Package Designer (APD) – 6xx*
  - *Allegro Package SI (APSI) – 6xx*
- ***Thermal Simulation (Flomerics)***
  - *Flotherm & Flopack*

☞ ***Tool selection depends on client requirements.***

Wipro – IC Package Design Flow

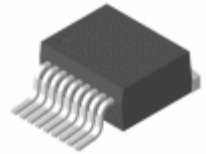


1) Identify Packages

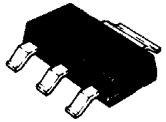
- ***Check different package options for the Die based on:***
  - ***Operating frequency, Thermal spec, Size limitation, End usage, Cost, etc.***
- ***Select the optimal packages***
  - ***From client's list***
  - ***Based on PCB manufacturers' constraints***
- ***Single Die can have multiple packages***
  - ***For example:***
    - ***Application Specific Standard Products***
    - ***Memory chips, FPGAs, CPLDs, etc.***

1) IC Package Types (General)

Discrete Packages


TO-263


TO-3


SOT


TO-46

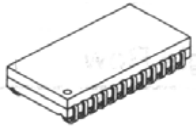
TO-252

SC-62

Dual Packages


DIP

SOP


SOJ


SOIC


SSOP


TSSOP

Quad Packages


PLCC

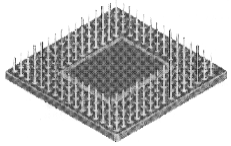

QFN


QFP

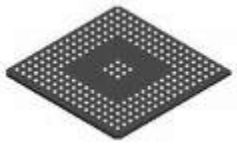

LCC

1) IC Package Types (General)

- ***Grid Array Packages***



PGA



BGA

LGA

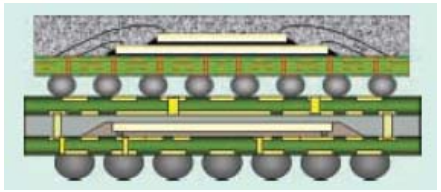
- ***Chip Scale Packages***

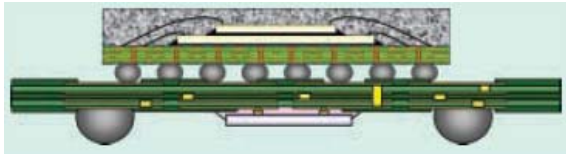
CSP

WLP

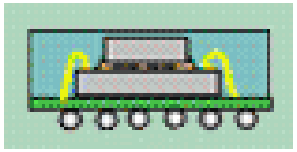
1) IC Package Types (General)

- *Package on Package*

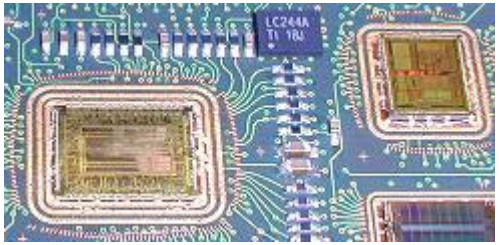




- *Chip on Chip*



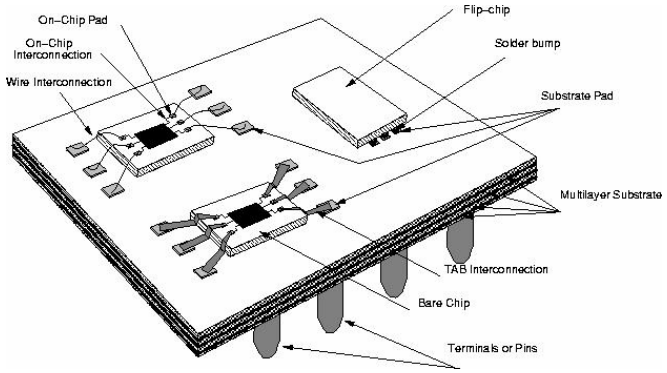
- *Chip on Board or*
  Direct Chip Attachment



1) IC Package Types (MCM / MCP)

MCM / MCP

- *A Multi-Chip Module or MCM is a specialized electronic package where multiple Integrated Circuits (ICs), semiconductor dies or other modules are packaged in such a way as to facilitate their use as a single IC.*



Different Type of MCM

- *MCM-L - laminated MCM. The substrate is a multi-layer laminated PCB (Printed circuit board).*
- *MCM-D - deposited MCM. The modules are deposited on the base substrate using thin film technology.*
- *MCM-C - ceramic substrate MCMs.*
- *MCM-S - uses a silicon substrate with tracks created in the silicon like regular ICs*

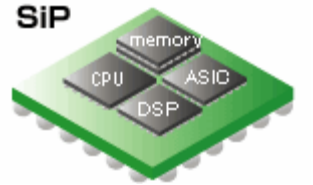
1) IC Package Types (SiP / SoP)

SiP / SoP

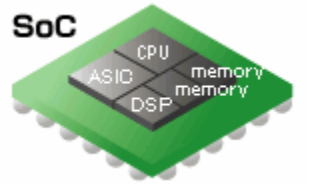
- *The term "System in a Package" or SiP refers to a semiconductor device that incorporates multiple chips and passives that make up a complete electronic system into a single package.*

Difference between SiP and SoC

- *SiP - Combines multiple chips and passives and encases them in to one package.*



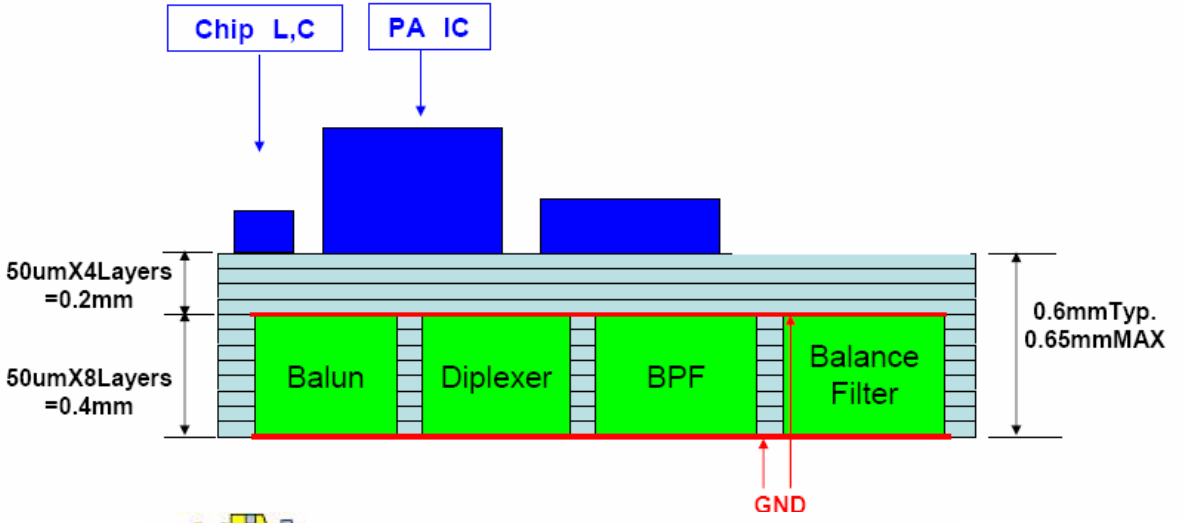
- *SoC - Builds multiple function-circuits on one chip.*

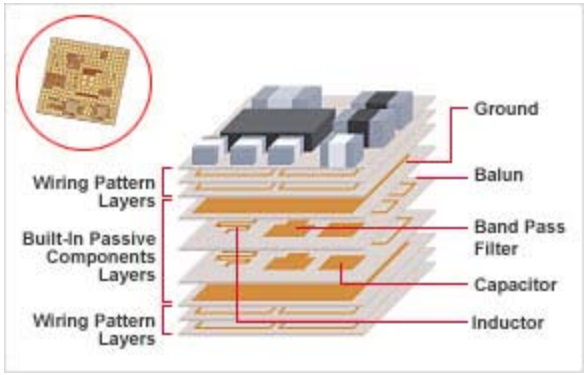


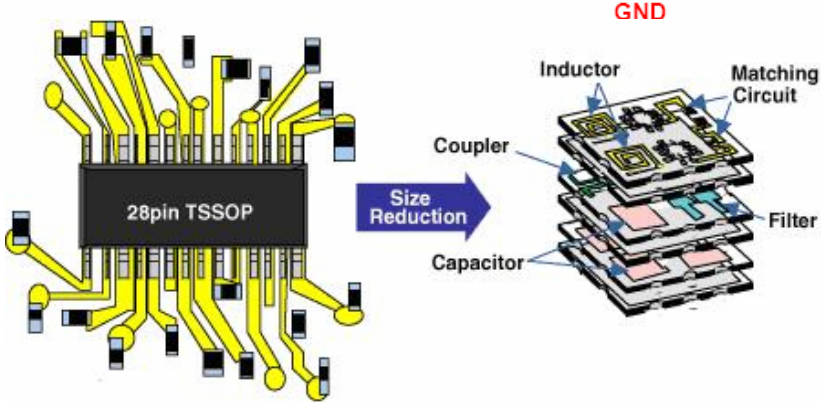
1) IC Package Types (Embedded Circuitry)

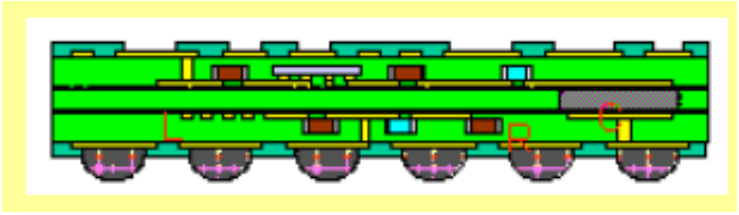
❖ Packages with Embedded Circuitry (Active Packages)

- *LTCC WLAN module with Embedded Circuitry*









1) Identify Packages

Package selection by Frequency

- Flat Packs for freq. < 200 MHz
- QFN for freq < 300 MHz
- Wire Bond BGA for freq < 500 MHz
- Flip-chip for freq > 500 MHz

Package selection by Power Dissipation

- BGA, QFP for power < 2.5 W
- Heat slug, Unique required for power < 5 W
- Heat Slug/ Heat spreader/ Thermally enhanced BGA required for power > 5W
- Heat Sink/ Heat spreader/ Heat cooling (recommended) for power > 12W/18 W
- AC/Fans required for power > 25 W

1) Identify Packages

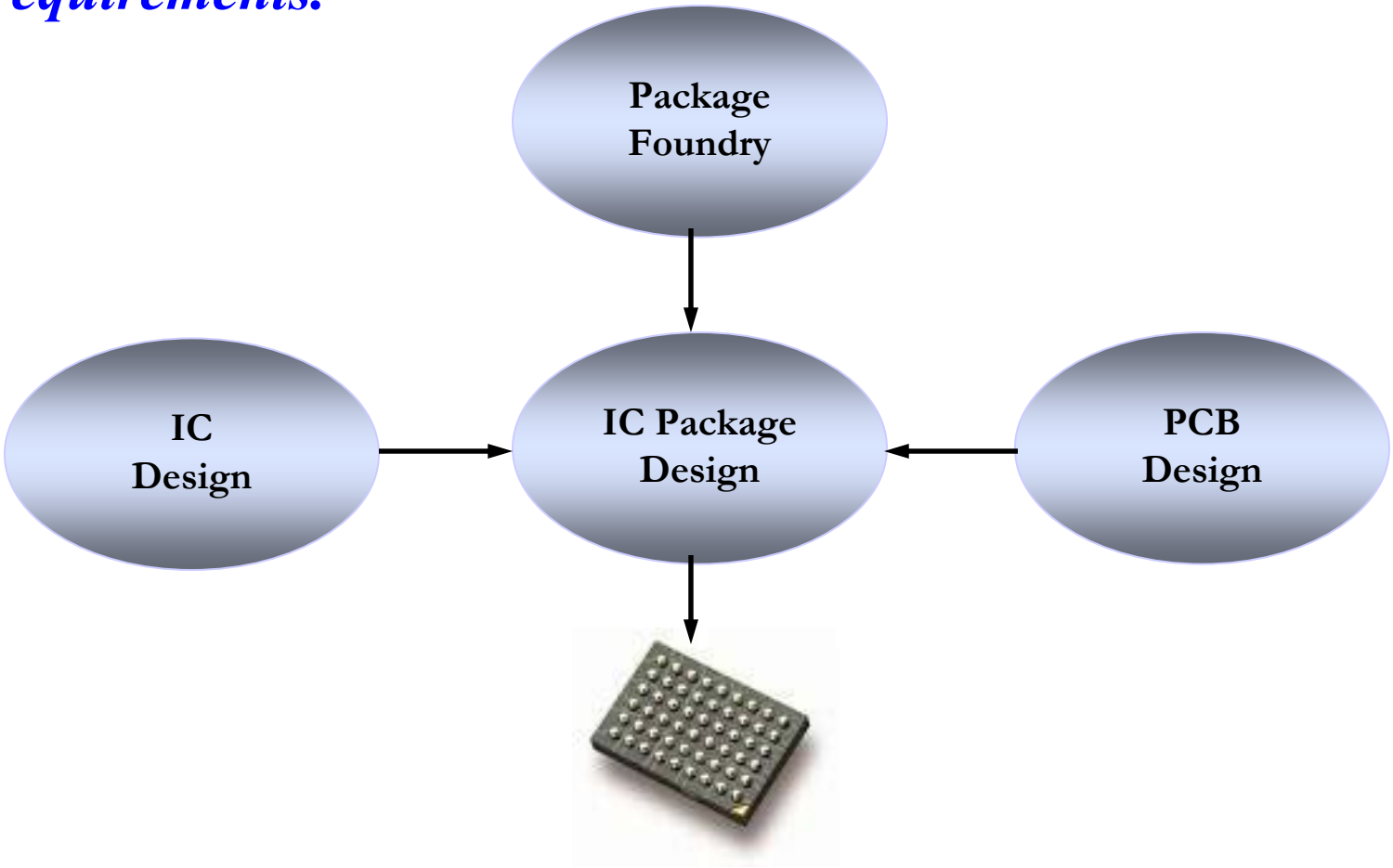
Package selection by Pin count

- Leads <25: SOP preferred
- Leads <50: TSOP, QFN are preferred
  - Other supported packages - QFP, WB BGA
- Leads <100: QFN preferred.
  - Other supported packages - TSOP, QFP, WB BGA
- Leads <200: WB BGA preferred.
  - Other supported packages – QFN, QFP
- Leads >200 and <800: Wire bond BGA preferred
- Leads >800: Flip chip BGA

Back to Package Flow

2) Input/ Set-up Data

- ***Package design is driven by IC Design and PCB design requirements.***

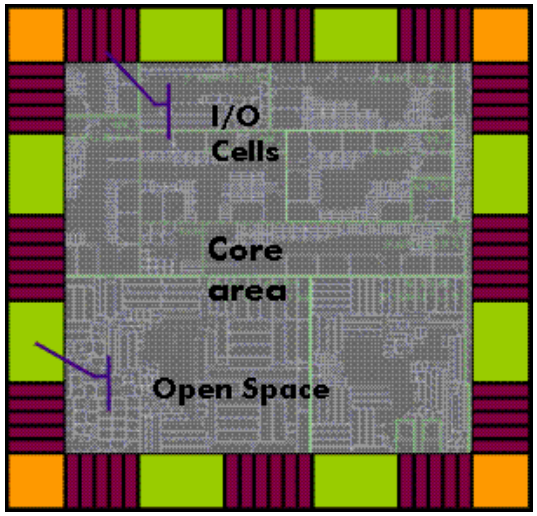


2) Input/ Set-up Data (IC design team)

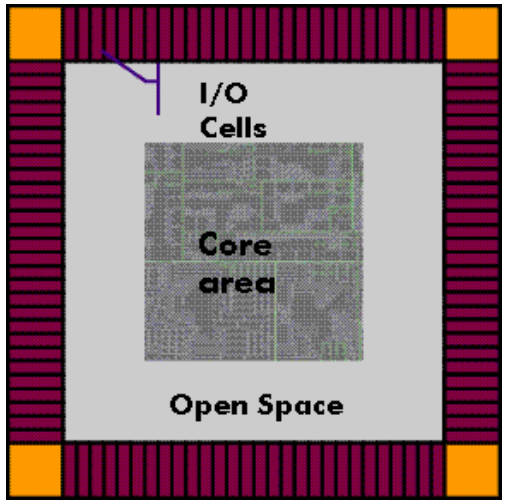
- ***IC design team***
  - ***I/O Netlist***
  - ***I/O Pad co-ordinates and pad opening***
  - ***Number of power and ground pins***
  - ***Die size & logo***
  - ***DEF (Die Exchange Format) data***
  - ***RLC targets for the output and power pads***
  - ***Signal types and Constraints - specification like Frequency, Power, Critical signals, etc.***

2) Input/ Set-up Data (IC design team)

- ***Optimized Die I/O placement***
  - *Placement information of Power/GND and Signal I/Os info*
  - *In case of Core Limited I/O; consider options like Circuit Under Pad (CUP)*
  - *In case of Pad Limited I/O; consider options like Flip Chip*



Core Limited I/O



Pad Limited I/O

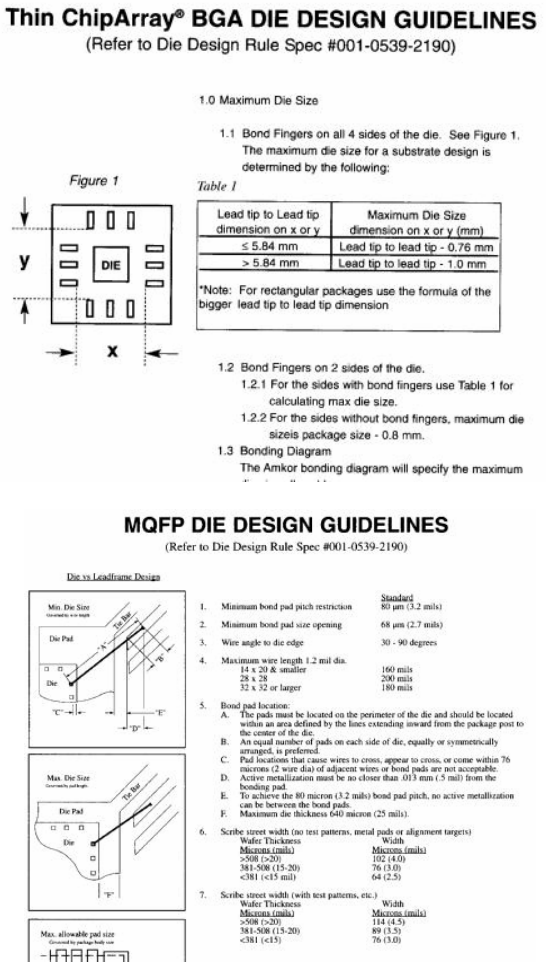
2) Input/ Set-up Data (PCB design team)

- ***PCB design team***
  - ***Initial I/O assignment draft***
  - ***Package PCB routability data***
  - ***Power delivery and Pin mapping***
  - ***RLC parameters for input ports***
  - ***PCB constraints***

2) Input/ Set-up Data (Package Foundry)

Package Foundry

- Package availability
- Package drawing and datasheet
- IO placement guidelines specific to package
- Package/Substrate design rules
- Assembly tooling
- Panelization details
- Die design guidelines (with respect to package)
  - Min/Max die size
  - I/O bond pad pitch
  - I/O bond pad location (two side, four side, etc.)
  - I/O bond pad size opening
  - Minimum scribe street width
  - Die thickness
  - Min/Max bond wire length
  - Min/Max Bond wire angle



Thin ChipArray® BGA DIE DESIGN GUIDELINES

(Refer to Die Design Rule Spec #001-0539-2190)

1.0 Maximum Die Size

1.1 Bond Fingers on all 4 sides of the die. See Figure 1. The maximum die size for a substrate design is determined by the following:

Figure 1

Table 1

Lead tip to Lead tip dimension on x or y	Maximum Die Size dimension on x or y (mm)
≤ 5.84 mm	Lead tip to lead tip - 0.76 mm
> 5.84 mm	Lead tip to lead tip - 1.0 mm

*Note: For rectangular packages use the formula of the bigger lead tip to lead tip dimension

1.2 Bond Fingers on 2 sides of the die.

1.2.1 For the sides with bond fingers use Table 1 for calculating max die size.

1.2.2 For the sides without bond fingers, maximum die sizeis package size - 0.8 mm.

1.3 Bonding Diagram

The Amkor bonding diagram will specify the maximum

MQFP DIE DESIGN GUIDELINES

(Refer to Die Design Rule Spec #001-0539-2190)

Die vs Leadframe Design

		Standard
1.	Minimum bond pad pitch restriction	80 µm (3.2 mils)
2.	Minimum bond pad size opening	68 µm (2.7 mils)
3.	Wire angle to die edge	30 - 90 degrees
4.	Maximum wire length 1.2 mil dia.	
	14 x 20 & smaller	160 mils
	28 x 28	200 mils
	32 x 32 or larger	180 mils

5. Bond pad location:
   - A. The pads must be located on the perimeter of the die and should be located within an area defined by the lines extending inward from the package post to the center of the die.
   - B. An equal number of pads on each side of die, equally or symmetrically arranged, is preferred.
   - C. Pad locations that cause wires to cross, appear to cross, or come within 76 microns (2 wire dia) of adjacent wires or bond pads are not acceptable.
   - D. Active metallization must be no closer than .013 mm (.5 mil) from the bonding pad.
   - E. To achieve the 80 micron (3.2 mils) bond pad pitch, no active metallization can be between the bond pads.
   - F. Maximum die thickness 640 micron (25 mils).

6. Scribe street width (no test patterns, metal pads or alignment targets)

Wafer Thickness Microns (mils)	Width Microns (mils)
>508 (>20)	102 (4.0)
381-508 (15-20)	76 (3.0)
<381 (<15 mil)	64 (2.5)

7. Scribe street width (with test patterns, etc.)

Wafer Thickness Microns (mils)	Width Microns (mils)
>508 (>20)	114 (4.5)
381-508 (15-20)	89 (3.5)
<381 (<15)	76 (3.0)

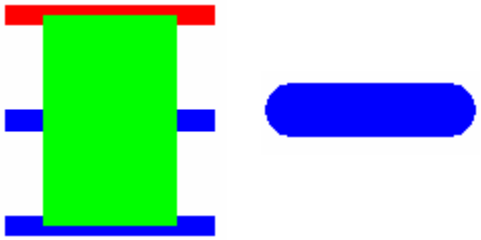
2) Input/ Set-up Data (Summary-Package Design)

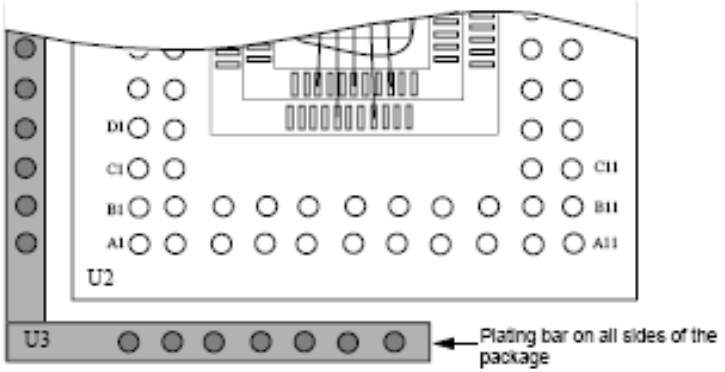
- *Die size and Pad locations (X-Y co-ordinates)*
- *Package mechanical drawing and dimensions*
- *Pin mapping details/ Signal name list (Die - Package)*
- *Signal types and Constraints*
  - *Example: Differential, Clocks, Controlled Impedance etc.*
- *Wire bonding/ Substrate/ Lead design rules*
  - *Spacing rules*
  - *Layer stack-up*
  - *Padstack (Die/ Wirebond/ Package/ Via) dimensions*
- *Electrical models/ Specifications*
- *Thermal/ Material data*

Back to Package Flow

3) Generate Symbols

- ***Create Padstacks***
  - *A padstack is a collection of information that is associated with a pin or a via, used to model different types of pads.*
  - *Padstacks – different types*
    - *Through Hole*
    - *Surface Mount*
    - *Vias*

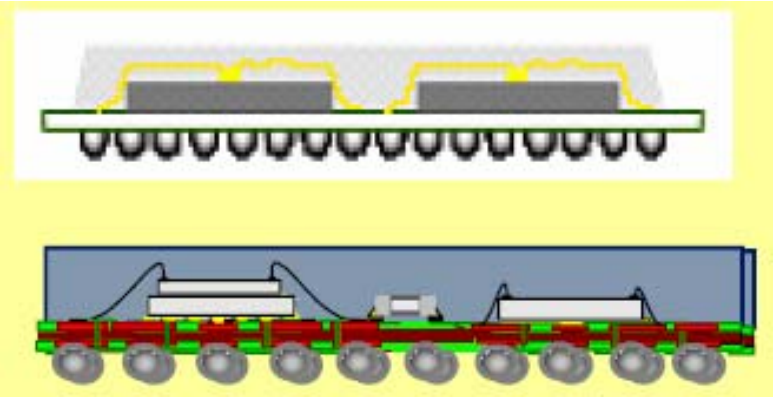




- ***Define die symbol***
- ***Define package symbol***
- ***Define passive component symbols***
- ***Mechanical symbols like Plating Bar, Holes, etc.***

Back to Package Flow

4) Die/ Package Placement



Die-to-Die Placement

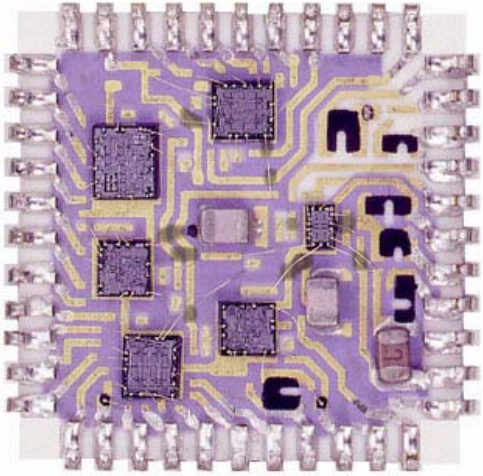
- *Reduce criss-cross*

Die-to-Package Placement

- *Right orientation and alignment*
- *Routabilitiy*
- *Place in package geometric centre for single die*
- *Distribute and try to align with the sides in case of multiple dies*

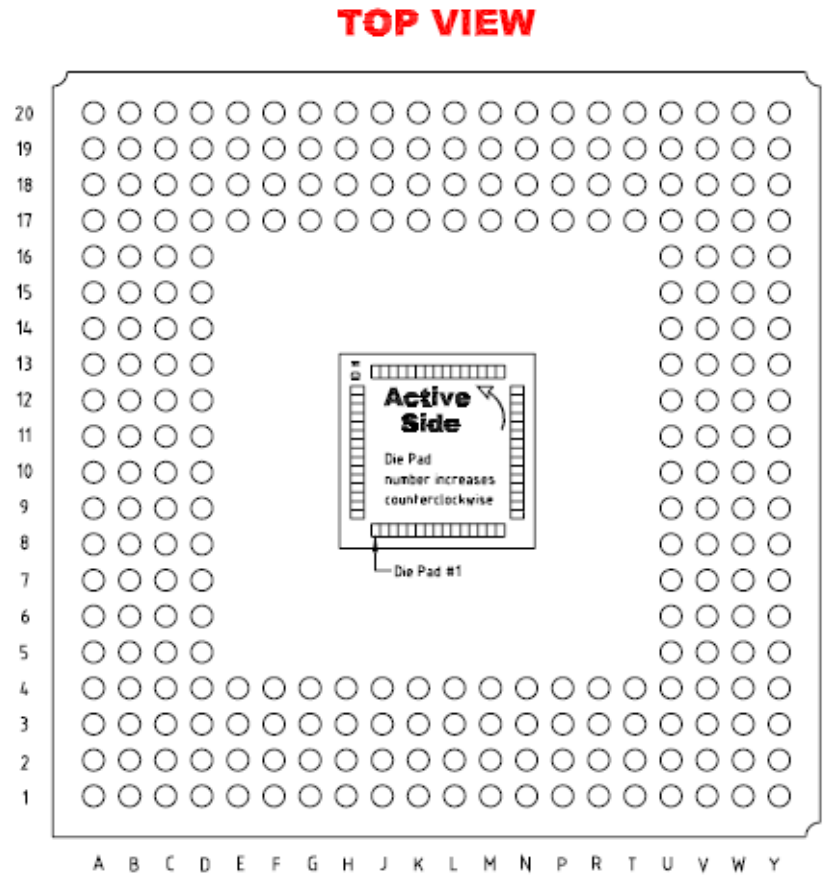
Passive Placement

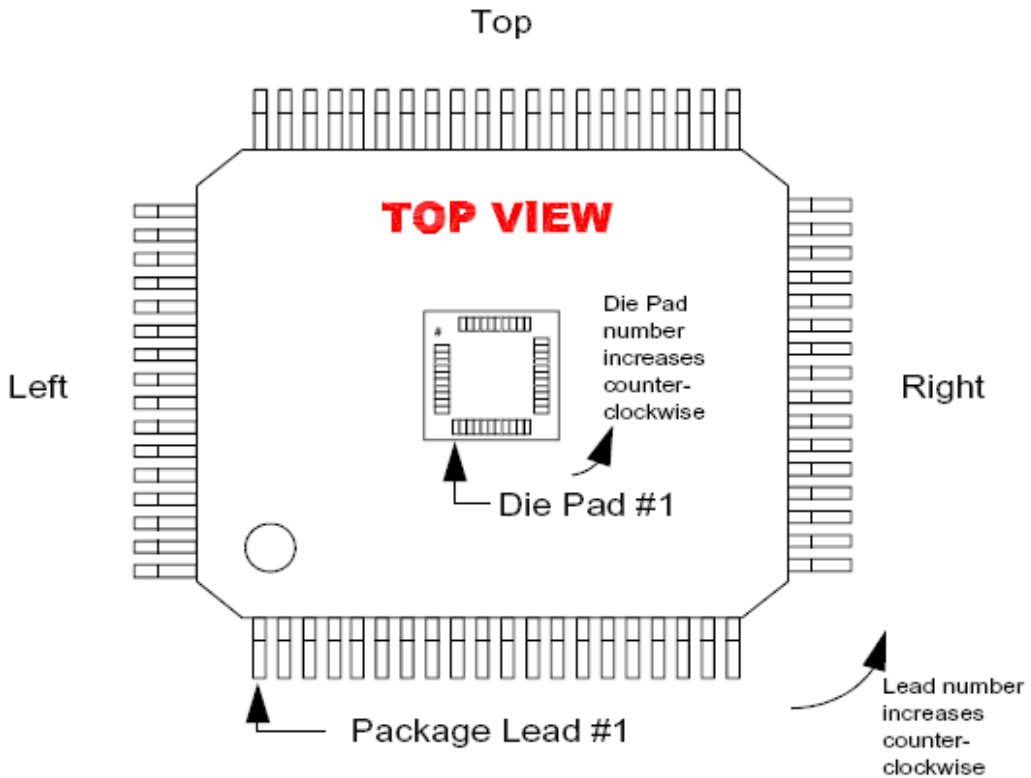
- *Distribute the passives according to the requirement*



4) Die/ Package Placement

❖ Die-to-Package Placement





Some Default Die-Package Orientation

4) Die/ Package Placement - Die Attach

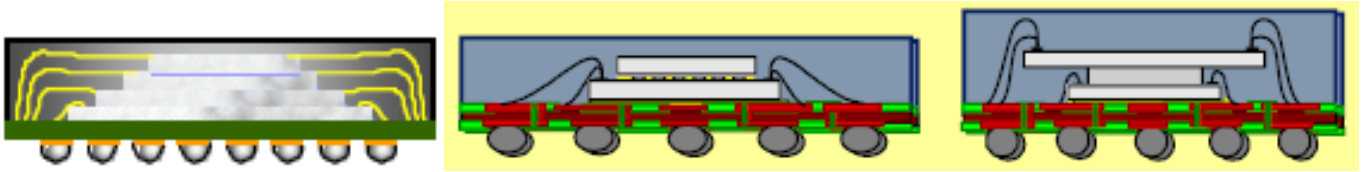
Die Attach

- *Die Attach (also known as Die Mount or Die Bond) is the process of attaching the silicon chip to the die pad or die cavity of the support structure (e.g the leadframe) of the semiconductor package.*

Die Attach – Cavity Up

Die Attach – Cavity Down

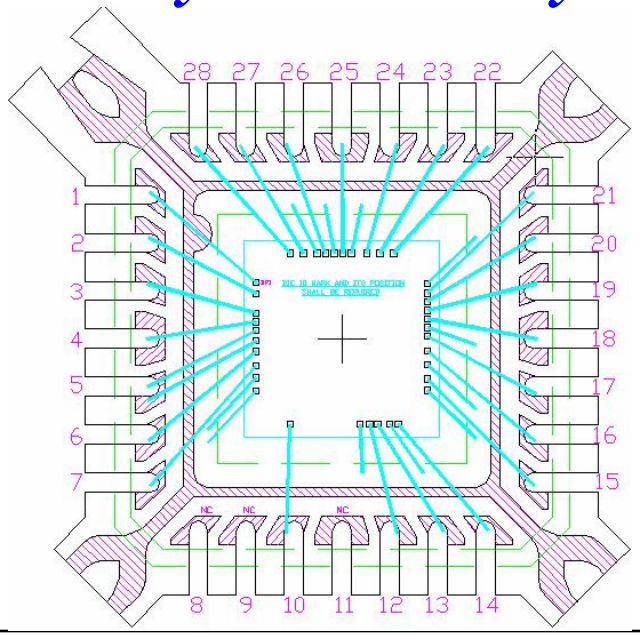
Die Attach – Stacked



Back to Package Flow

5) I/O Mapping

- ***Map the connectivity***
  - ***Mapping the connectivity from the Die to the Package pins***
- ***Should keep in mind***
  - ***Frequency of I/O signals***
  - ***PCB Routability/ Trace length, RLCs, etc.***
- ***Define connectivity automatically/manually***



Back to Package Flow

6) Die to Package Bonding

What is Die to Package Bonding?

- *Die bonding is the process of attaching die to the package. This will provide the electrical connectivity to the die from the package.*

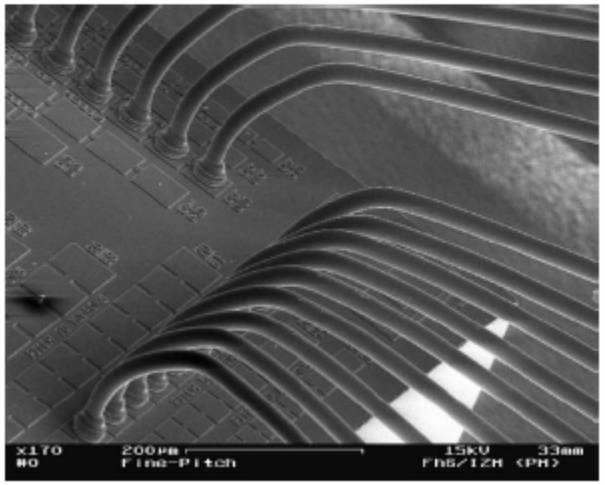
Normal Die to Package Bonding

- *Wire Bonding*
- *Tape Automated Bonding*
- *Flipchip Bonding*

6) Die to Package Bonding - Wire Bonding

Wire Bonding

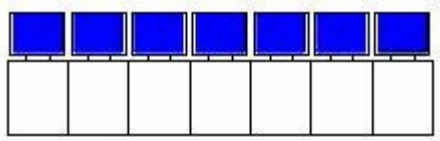
- *Wire bonding is the process of providing electrical connection between the silicon chip and the external leads/bond pads of the semiconductor package using very fine bonding wires.*
- *Gold/Aluminium/Copper wire is used to make a connection*
- *Thermo-compression or thermosonic energy to make a connection*
- *Design related critical features :*
  - *Pad size, Pad pitch*
  - *Pad location with respect to the bond finger*
- *Assembly related critical parameters*
  - *Wire angle & length - Wire crossing*
  - *Wire to wire space - Wire exit angle*



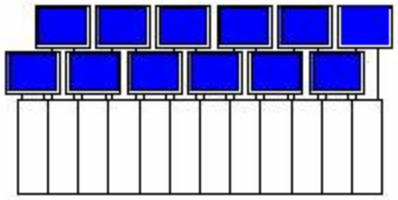
6) Die to Package Bonding - Wire Bonding

- ***Wire Bond – Data Required***
  - *Bondpad dimensions and bondwire connect location*
  - *Bondpad X or Y location (only for orthogonal)*
  - *Bondpad-to-bondpad spacing*
  - *Min and max wirebond length*
  - *Max wirebond angle (only for radial)*

- ***Different types of Bond Pad arrangements***

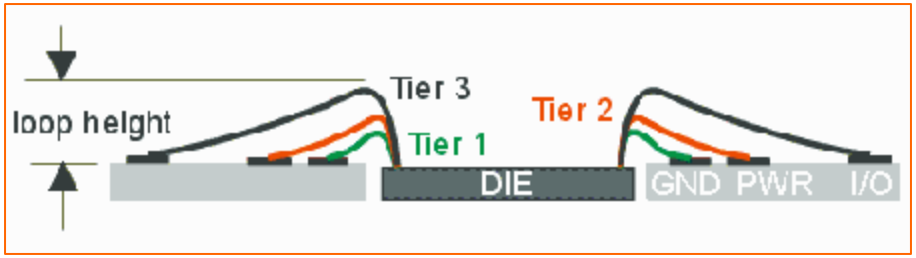


Inline

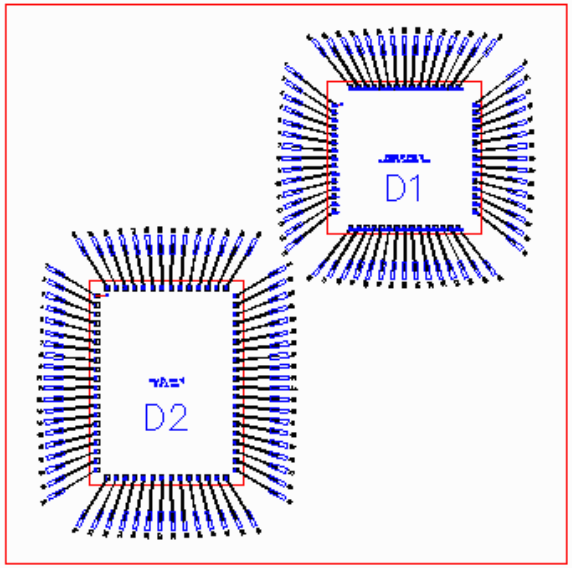


Staggered

6) Different Types of Wire Bonding

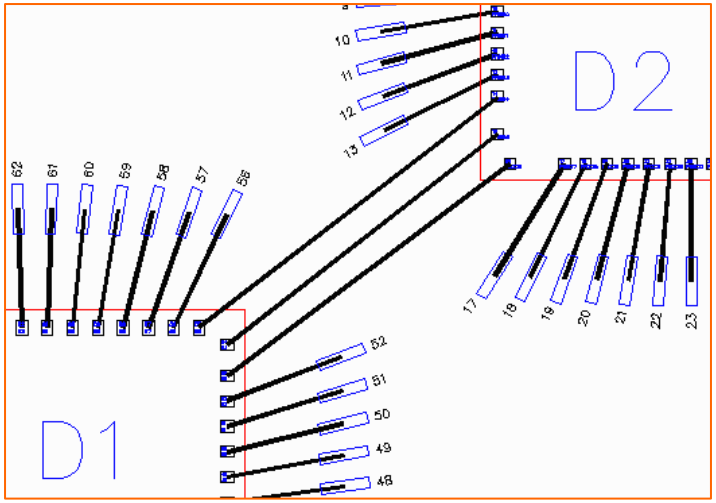


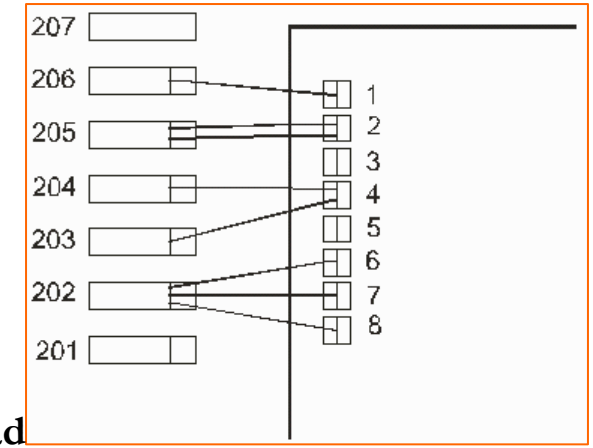
Multi Tier Bonding



Multi Chip Bonding

Die to Die Bonding





Multiple Wire
in Same Bond Pad

6) Die to Package Bonding - Wire Bonding

Wire Bonding

- *Advantages :*
  - *Enormous installed capacity*
  - *Flexible process : multiple die / package*
- *Dis-advantages :*
  - *Cost is a function of number of bonds*
  - *Wire inductance*
- *Trend :*
  - *Pad pitch shrink is possible with new technology*
  - *Multiple rails to bond on a substrate*

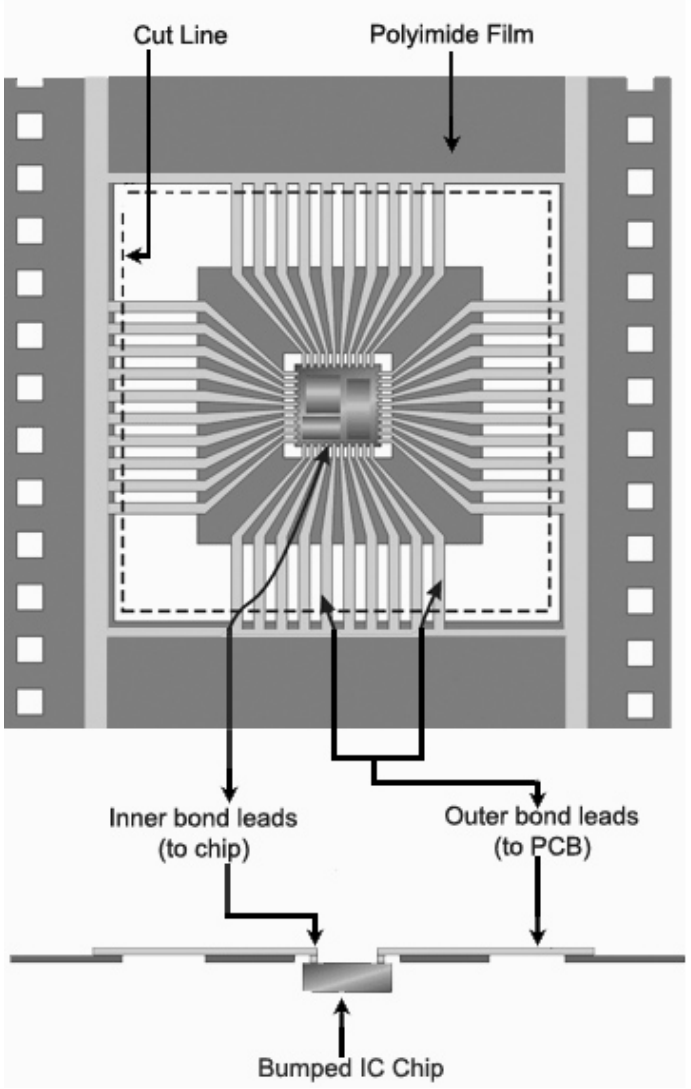
6) Die to Package Bonding - TAB

Tape Automated Bonding (TAB)

- *TAB is the process of mounting a die on a flexible tape made of polymer material, such as polyimide. This can be mounted to a package substrate or PCB.*
- *Thermo-compression bonding*
- *Patterned metal on polymer tape is bonded*
- *Advantages :*
  - *Gang bonding instead of single*
  - *Better electrical performance than a wire bond*
- *Dis-advantages :*
  - *Each silicon requires a new tape design*
  - *Special metallurgy needed at the bond pad*

6) Die to Package Bonding - TAB

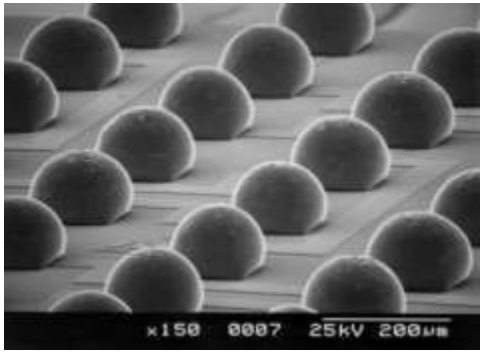
- ***Tape Automated Bonding***
  - ***Inner Lead Bonding (ILB)***
    - ***The TAB bonds connecting the die and the tape are known as inner lead bonds.***
  - ***Outer Lead Bonding (OLB)***
    - ***The TAB bonds connecting the tape to the package or to external circuits are known as outer lead bonds.***



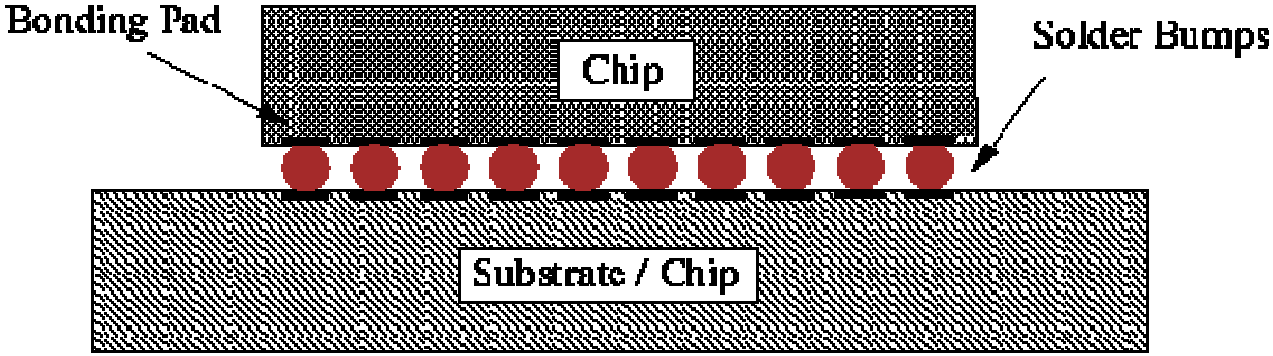
6) Die to Package Bonding – Flip Chip

Flip Chip Bonding

- *It is an interconnect technology [C4 Bump (Controlled Collapse Chip Connection)]*
- *Can be offered in any type of package but it is most suited to BGA*
- *Assembly Process :*
  - *Small bumps are grown on the die : Bumping*
  - *Die is flipped and attached to the substrate : Reflow*
  - *Underfill to minimize CTE difference between the die and the substrate.*



C4 Bump in the Die



6) Die to Package Bonding – Flip Chip

Flip Chip Bonding

- *Advantages :*
  - *Die shrink is possible compared to wire bond die*
  - *Best electrical performance*
  - *Allows for I/Os anywhere in the die*
  - *Lower inductance power planes support high frequency designs*
  - *Supports higher pin counts than wire-bond packages*
  - *Assembly cost independent of No of I/Os*

- *Dis-advantages :*
  - *Requires technology development in several areas*
  - *Required infrastructure is not there*
  - *Cost is very high for low volume applications*
  - *Expertise concentrated within certain companies*
  - *Additional fab processes - Redistribution, Bumping*

6) Die to Package Bonding – Flip Chip (RDL)

RDL (Re Distribution Layer)

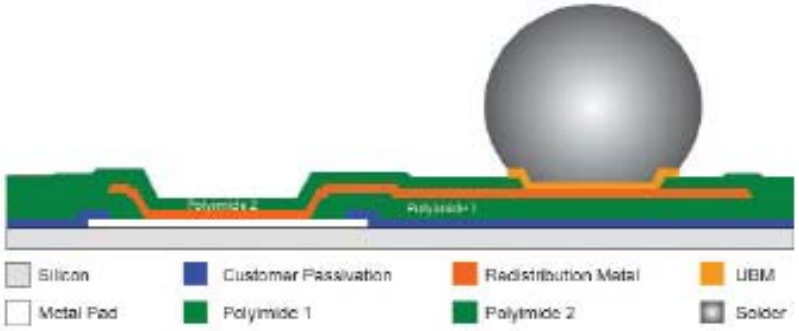
- *A redistribution layer (RDL) is a routing layer of conductive metal within an IC that connects the die or solder bump to a connection point on an I/O driver.*

RDL in Flip-chip

- *The RDL connects I/O Cells to the Bond Pad*
- *Normally it will be the top metal layer*

RDL in WLP

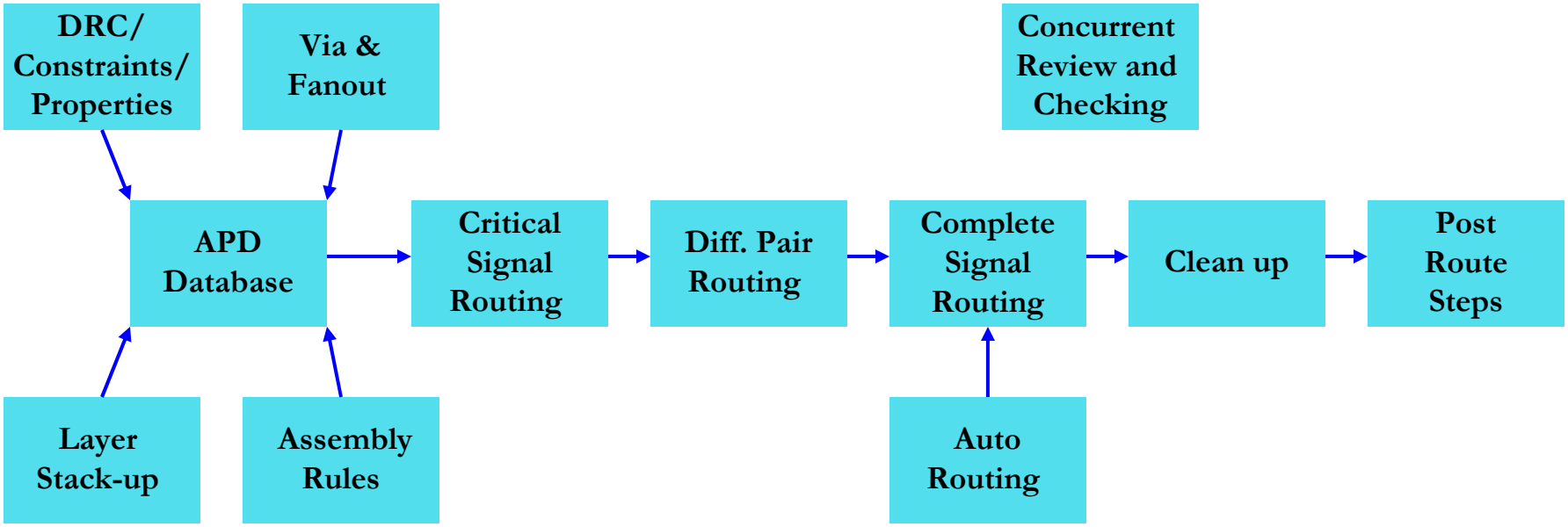
- *The RDL connects I/O Cells to the Solder ball*
- *Can be done by the Die or Package Foundry*



Back to Package Flow

7) Package Substrate Routing

❖ Substrate Routing – Flow Diagram



7) Package Substrate Routing

- *Create power/ Ground planes/ Power rings*
- *Generate fanout/ offset vias*
- *Die-to-die routing*
- *Die-to-package routing*
- *Package-to-plating bar routing*
- *Generate radial routes*
- *Route automatically*
  - *Spider Router*
  - *Specctra Router*
- *Route manually*

7) Substrate Materials (Ceramic & Organic)

Dielectric Materials

- Ceramic
  - Thick-film ceramic
  - Thin-film ceramic
  - High-Temperature Co-fired Ceramic (HTCC)
  - Low-Temperature Co-fired Ceramic (LTCC)


Ceramic Dual In-Line Package (CDIP)

Ceramic Pin Grid Array (CPGA)

Ceramic Leadless Chip Carrier (CLCC)

Ceramic Ball Grid Array (CBGA)

Ceramic Land Grid Array (CLGA)

- Organic
  - BT (Bismaleimide-Triazine)
  - FR-4

Plastic Dual In-Line Package (PDIP)

Plastic Pin Grid Array (CPGA)


Plastic Quad Flat Pack (PQFP)

Plastic Ball Grid Array (PBGA)

Conductor Materials

- Gold, Silver, Copper, Aluminium, Tin/Lead, Nickel

7) Substrate Functions

Main Functions

- Support die and components
- Insulate between tracks and layers
- Provide electrical interconnections

Desired Functions

- Mechanically strong to support die and components
- Dissipate heat and have low thermal expansion
- Drill and Punch through
- Resist degradation by heat and process chemicals
- Should not absorb excessive moisture
- Low dielectric constant
- Dielectric should receive plating

7) Substrate Stack-up

- ***Stack-up***
  - ***Routability***
  - ***Power Planes***
  - ***Controlled Impedence***

	SURFACE	AIR
WIREBOND	BONDING_WIRE	GOLD
	DIELECTRIC	AIR
TOP_COND	CONDUCTOR	COPPER
	DIELECTRIC	FR-4
VSS	PLANE	COPPER
	DIELECTRIC	FR-4
VDD	PLANE	COPPER
	DIELECTRIC	FR-4
BOT_COND	CONDUCTOR	COPPER
	SURFACE	AIR

Wire Bond

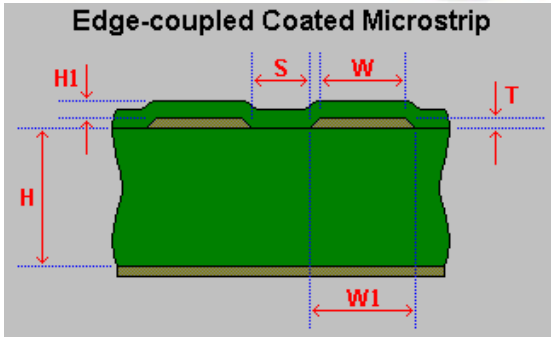
	SURFACE	AIR
TOP_COND	CONDUCTOR	COPPER
	DIELECTRIC	FR-4
GND_2	PLANE	COPPER
	DIELECTRIC	FR-4
SIG_3	CONDUCTOR	COPPER
	DIELECTRIC	FR-4
PWR_4	PLANE	COPPER
	DIELECTRIC	FR-4
SIG_5	CONDUCTOR	COPPER
	DIELECTRIC	FR-4
SIG_6	CONDUCTOR	COPPER
	DIELECTRIC	FR-4
PWR_7	PLANE	COPPER
	DIELECTRIC	FR-4
SIG_8	CONDUCTOR	COPPER
	DIELECTRIC	FR-4
GND_9	PLANE	COPPER
	DIELECTRIC	FR-4
BOT_COND	CONDUCTOR	COPPER
	SURFACE	AIR

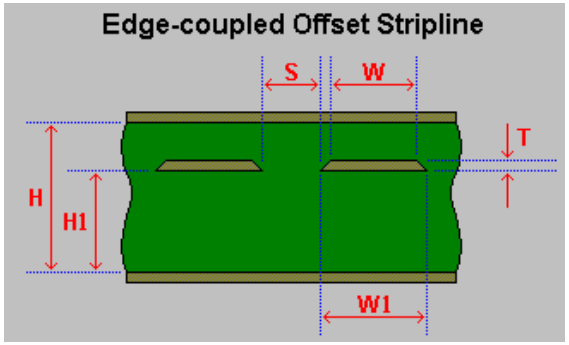
Flip Chip

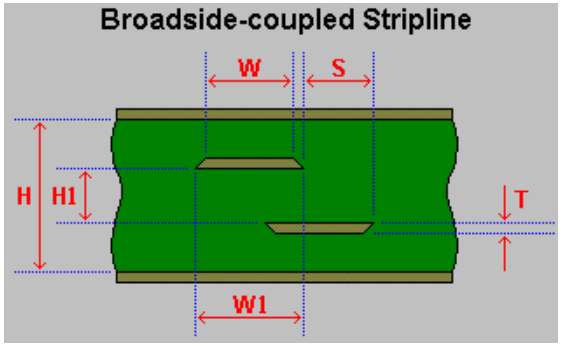
7) Substrate Trace Structure

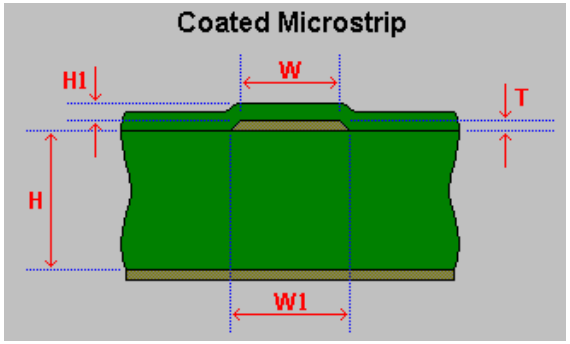
Normal Substrate Trace Structures

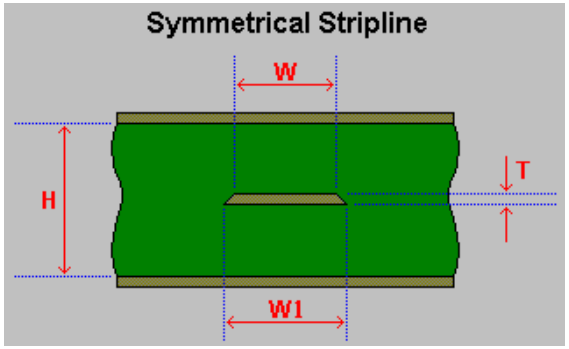
- Microstrip & Stripline
- Single ended tracks
- Differential tracks

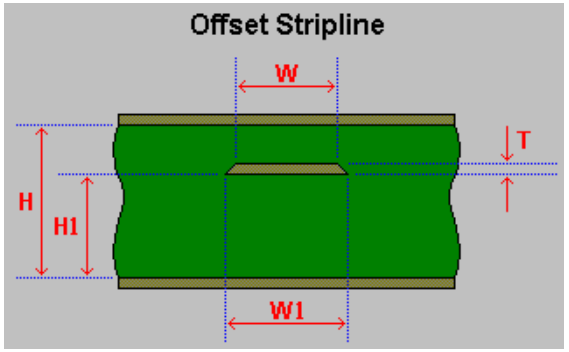




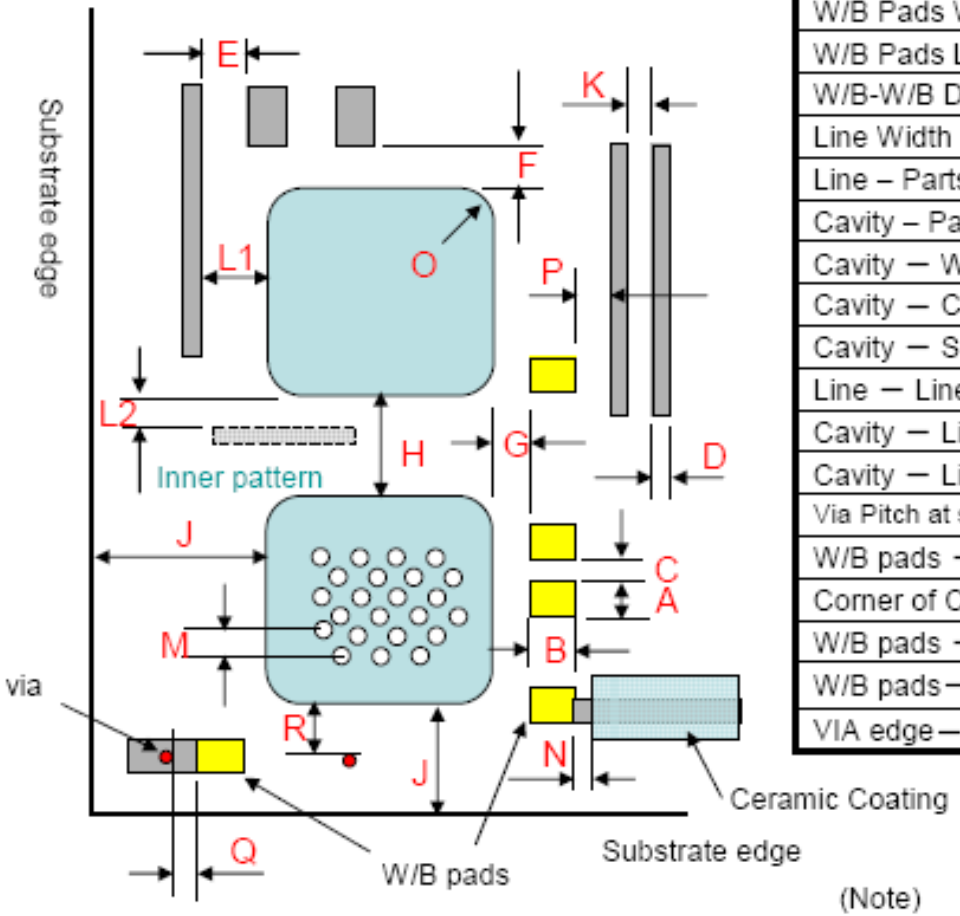








7) Substrate Design Rules (Sample)



model

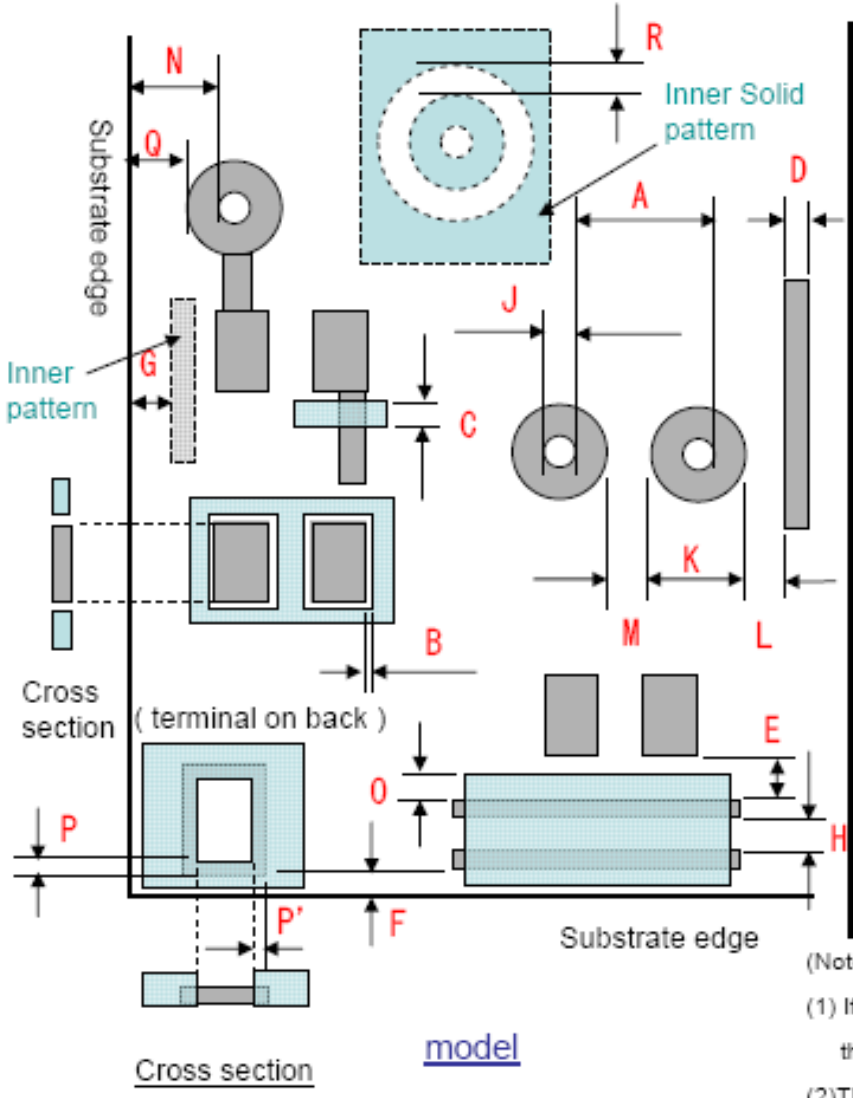
Unit : mm

items	symbol	Spec.
W/B Pads Width	A	0.150 min
W/B Pads Length	B	0.200 min
W/B-W/B Distance	C	0.100 min
Line Width	D	0.075 min
Line – Parts pads	E	0.200 min
Cavity – Parts pads	F	0.300 min
Cavity – W/B pads	G	0.150 min
Cavity – Cavity	H	1.000 min
Cavity – Substrate edge	J	1.000 min
Line – Line	K	0.075 min
Cavity – Line (surface)	L1	0.200 min
Cavity – Line (inner)	L2	0.200 min
Via Pitch at same functional trace	M	0.300 min
W/B pads – Ceramic Coating	N	0.050 min
Corner of Cavity	O	0.150 min
W/B pads – Line	P	0.150 min
W/B pads–Via edge	Q	0.500 min
VIA edge–Cavity edge	R	0.300 min

(Note)

If the module layout does not allow the design rules above, the specification shall be discussed.

7) Substrate Design Rules (Sample) Cont.



Unit : mm

items	symbol	Spec.
Pads – Ceramic Coating	B	0.050 min
Ceramic Coating dam pattern width	C	0.200 min
Line width	D	0.075 min
Pads – Line	E	0.200 min
Substrate edge – Line (Surface)	F	0.200 min
Substrate edge – Line (inner)	G	0.250 min
Line – Line	H	0.075 min
Standard: Via Dia. /Via Land Dia./Via Pitch	J/K/A	Φ0.100/Φ0.200/Φ0.350 min
Standard: Via Dia./Via Land Dia./Via Pitch	J/K/A	Φ0.050/Φ0.150/Φ0.225 min
Option(＊): Via Dia./Via Land Dia./Via Pitch	J/K/A	Φ0.050/Φ0.125/Φ0.200 min
Via Land – Line	L	0.137 min
Via Land – Via Land	M	0.150 min
Substrate edge – Via edge	N	0.300 min
Ceramic Coating – Line	O	0.150 min
Ceramic Coating overlap at Bottom pads	P	0.100 min
not to the substrate edge	P'	0.050 min
Via Land – Substrate edge	Q	0.250 min
Via Land – Inner solid pattern	R	0.150 min

(Note)

(1) If the module layout does not allow the design rules a
the specification shall be discussed.

(2)The Via pitch for 200um described above(＊) is applicable to Flip Chip area only.

Back to Package Flow

8) Package Analysis - Electrical Analysis

Electrical Analysis

- *RLC 3-D extraction*
- *Substrate impedance analysis*
- *Propagation delay report for Netlist*
- *Pre/Post route SPICE/IBIS 3-D model simulations on Nets*
- *3D package modeling and IBIS model generation*
- *Cross talk, Reflection, Over/Under Shoot analysis*
- *Timing analysis*
- *Power-Ground Bounce/SSN analysis*

☞ *Refer Package Analysis course material for details.*

8) Package Analysis - Thermal Analysis

Thermal Analysis

- Thermal modeling based on JEDEC test setup
- Thermal Resistance (Rjb, Rjc, Rja)
- Package Thermal Characterization
  - Junction temperature
  - Junction temperature reliability
  - Junction temperature functionality
  - Case temperature
  - Board temperature

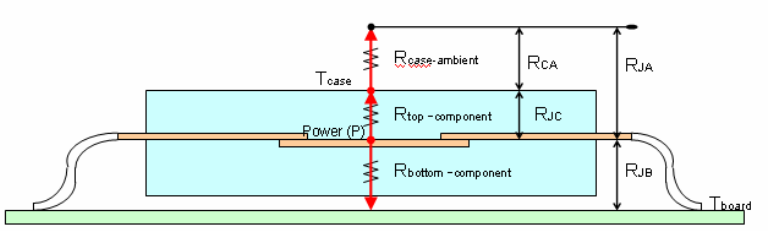
Thermal Analysis (Impact on Package Design)

- Modify die placement in case of Multi Chip Module
- Add plane layers to the stackup
- Use alternative substrate materials
- Add thermal vias
- Add heat sinks
- Experiment with alternative environmental conditions

☞ Refer Package Analysis course material for details.

8) Package Analysis - Thermal Analysis

❖ Temperature Flow in a Package



- *Rja = Rjc + Rca*

- *Package thermal performance is defined by Rja.*
- *Power = (Tj - Ta) / Rja*
  where, Tj = Junction Temperature (ex. 110 deg C)
  Ta = Ambient Temperature (ex. 50 - 70 deg C)

- *If Tj = 110, Ta = 50 & Rja = 15 ----> Power = 4 Watts*

☞ *Refer Package Analysis course material for details.*

8) Package Analysis

Mechanical Analysis

- Stress Analysis
- Bending Analysis
- Mechanical Structural Analysis
- Mechanical Shock
- Vibration Analysis
- Moisture Sensitivity Characterization
- Drop Test
- Board Level Cyclic Bending Test, etc.

☞ *Refer Package Analysis course material for details.*

Back to Package Flow

9) Design Verification

- *Check Physical Design Rules*
- *Check Electrical Rules*
- *Check Connectivity*
- *DFM/DFA Analysis*
- *Netlist with Property Output file Verification*
- *Component Compare*
- *LVS Comparison*

Back to Package Flow

10) Design Documentation

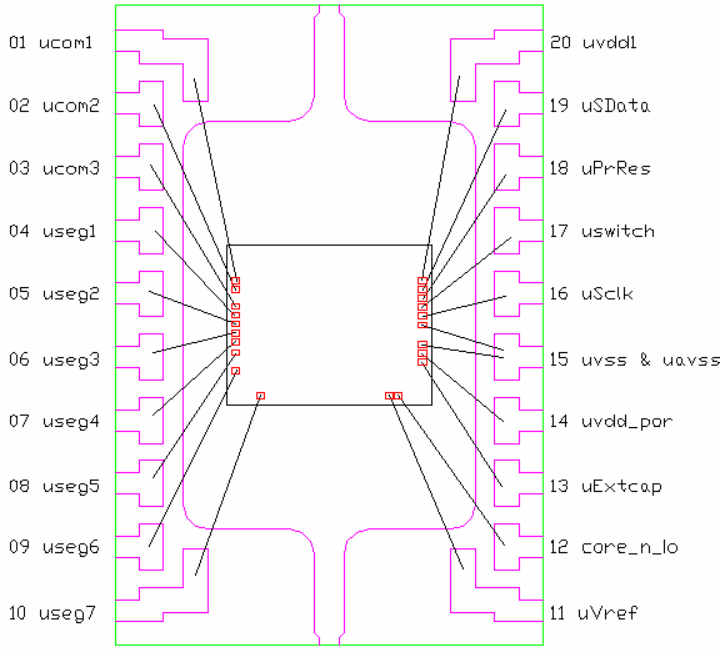
- *Create Plot/IPF Files*
- *Generate Reports*
- *Generate Dimensioning data*
- *Create Wire Bond Diagrams*
- *3-D Translation using MCAD Translators*

Back to Package Flow

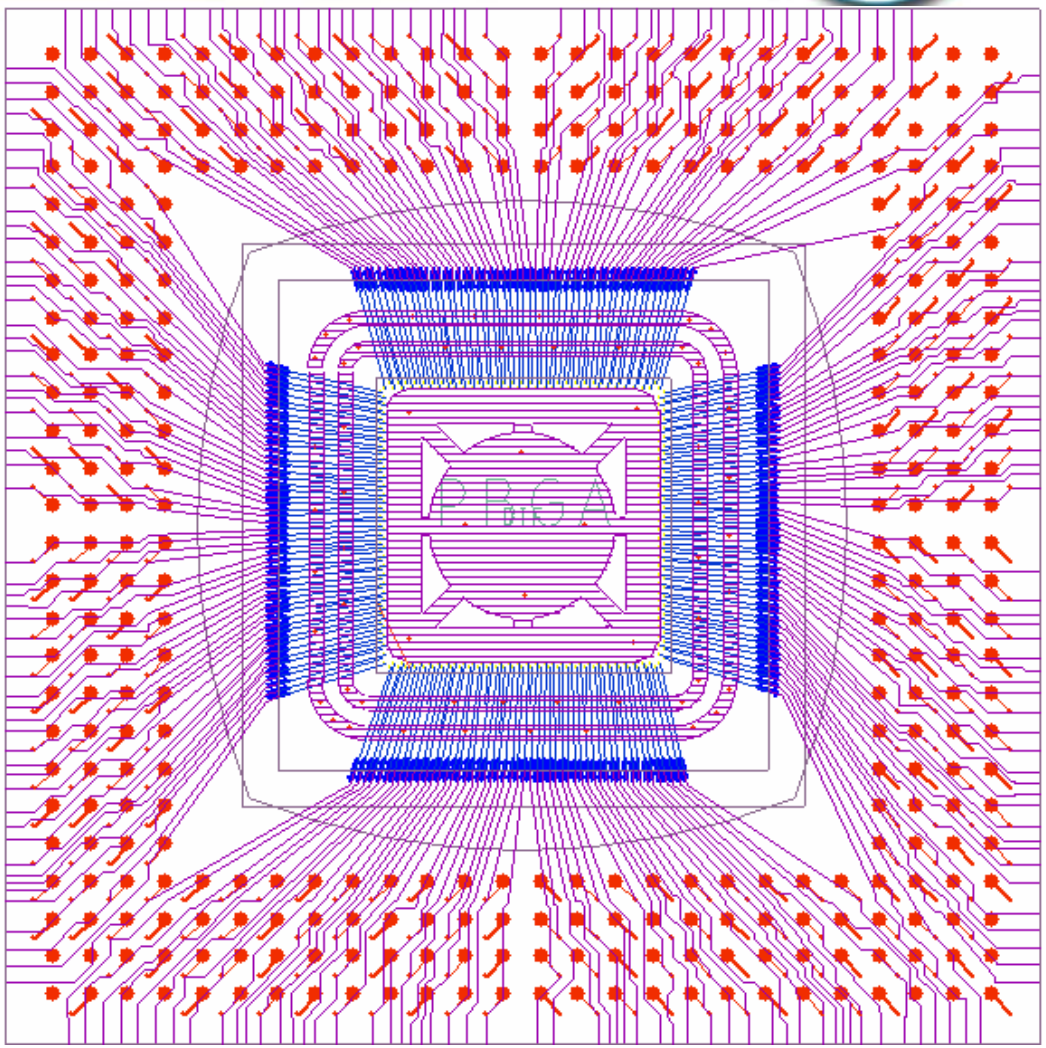
11) Output Generation

- *Gerber and NC Drill Data*
- *ODB++ Data*
- *GDSII Stream Data*
- *DXF Data*
- *Wire Bond Diagrams/ Reports*
- *PCB Symbols*
  - *PCB Schematic and Layout*
- *.mcm file (APD Database)*

11) Wipro – Sample Designs



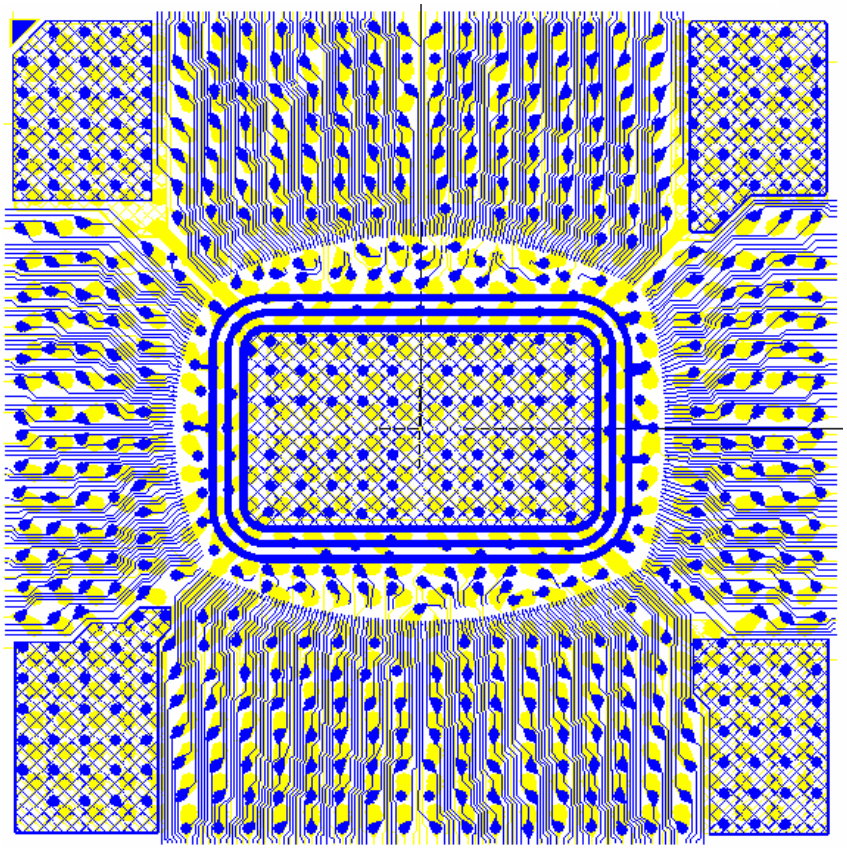
20 – Pin SOP



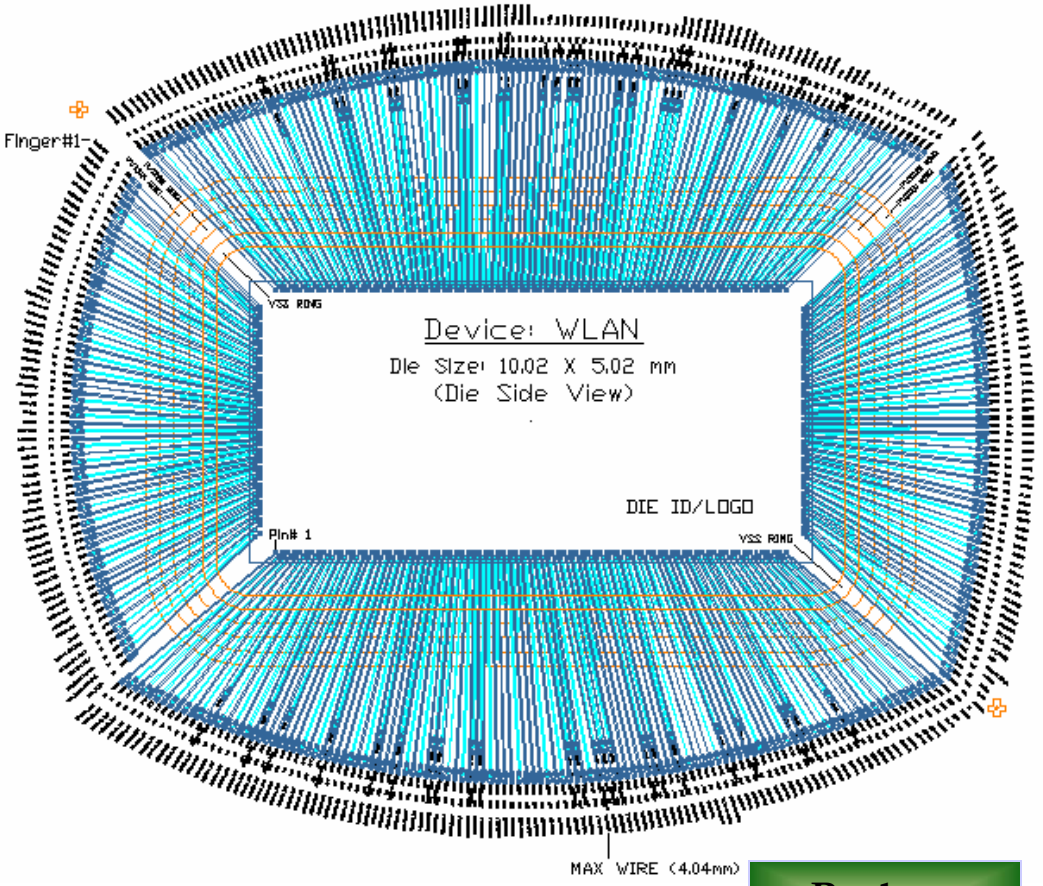
PBGA 352 Pin, 1.27 mm pitch

11) Wipro – Sample Designs

672 – Pin PBGA



Substrate Routing



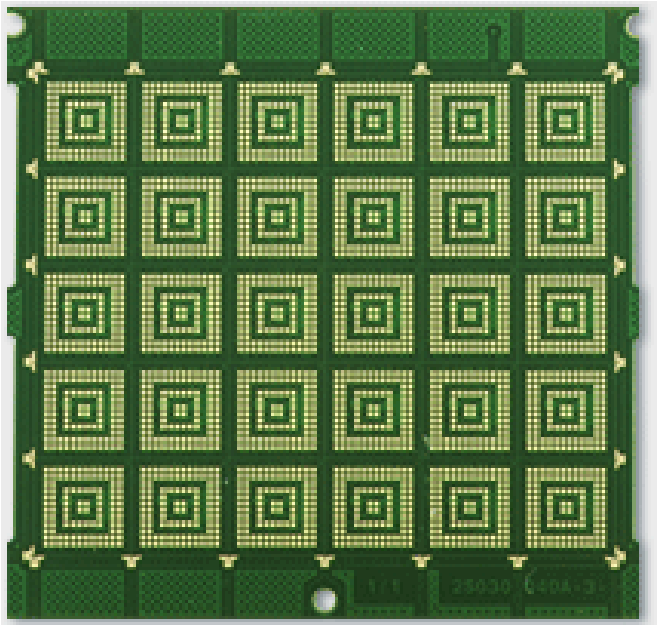
Wire Bond Diagram

Back to Package Flow

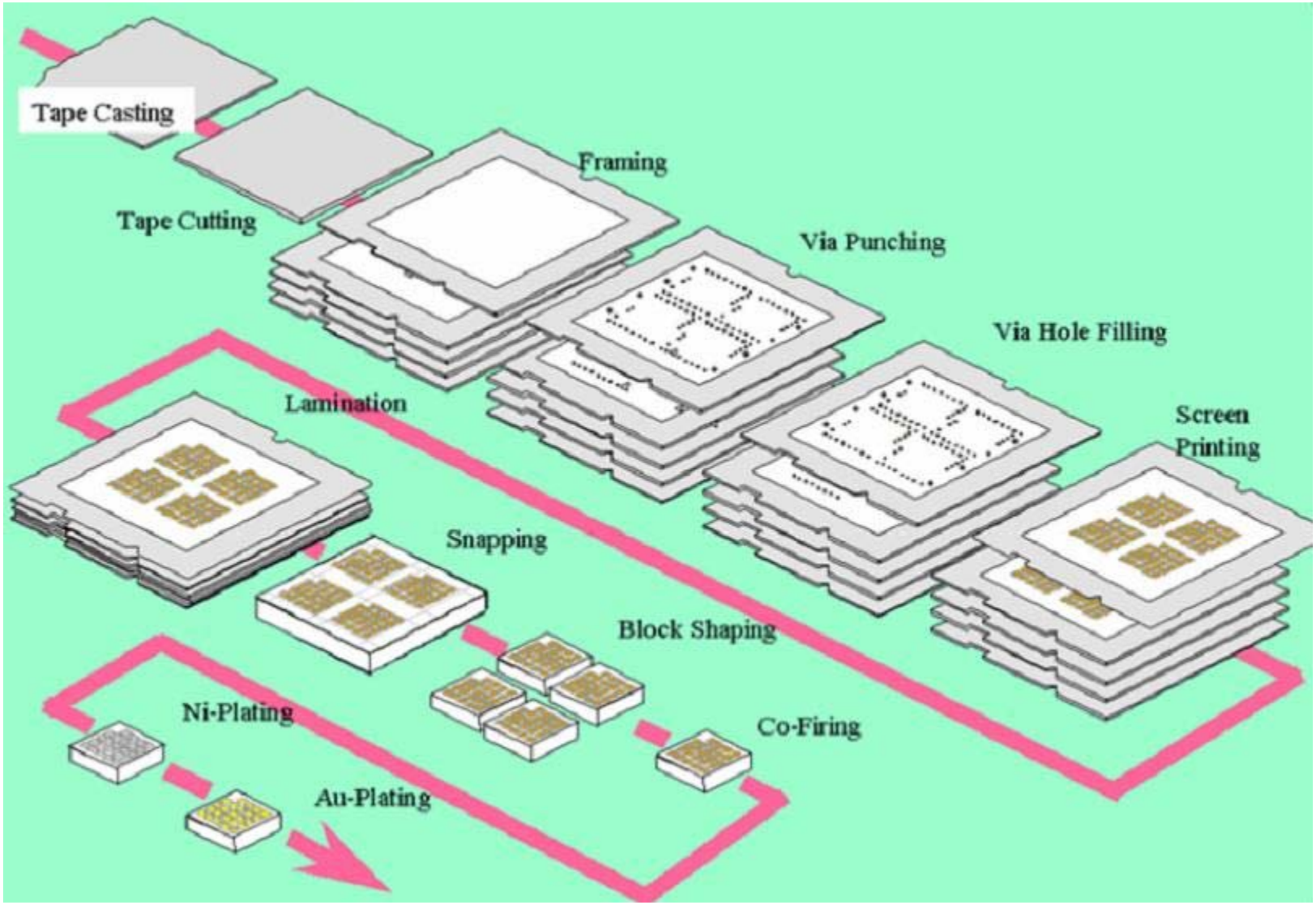
12) Fabrication & Chip Assembly

❖ Panelising Substrate

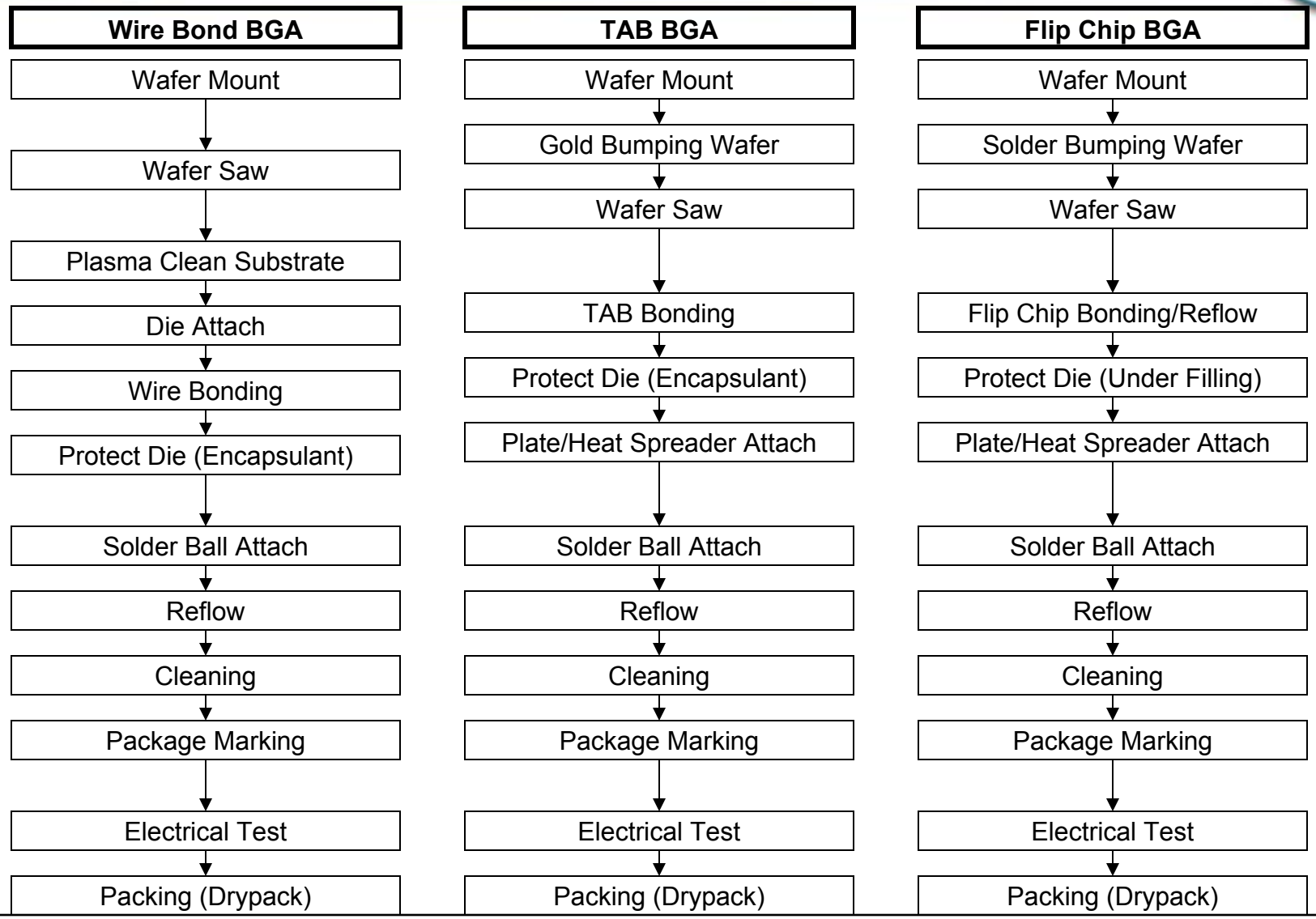
- *The substrate has to be fabricated with the Panelising rule of the assembly house*
- *This will help in assembling the chip in the substrate with proper tooling*



12) Substrate Fabrication Flow (Ceramic)



12) Typical Package Assembly Flow (BGA)



12) Some Fab and Assembly Process

Wafer Backgrind

- *It is the process of grinding the backside of the wafer to the correct wafer thickness prior to assembly. It is also referred to as 'wafer thinning'.*

Die Preparation

- *Die preparation is the process by which the wafer is processed into individual dice in preparation for assembly. Die preparation consists of two major steps, namely, wafer mounting and wafer saw.*

Wafer Saw

- *Wafer saw is the step that actually cuts the wafer into individual dice for assembly in IC packages*

12) Encapsulation

Encapsulation

- *It is the process of covering the assembled chip with a mold material for protection.*

Encapsulation – Types

- *Hermetic*
- *Non-Hermetic*

Encapsulant Properties

- *Adequate mechanical strength*
- *Adhesion to package components*
- *Manufacturing and environmental chemical resistance*
- *Electrical resistance*
- *Matched CTE to interfaces*
- *High thermal and moisture resistance*

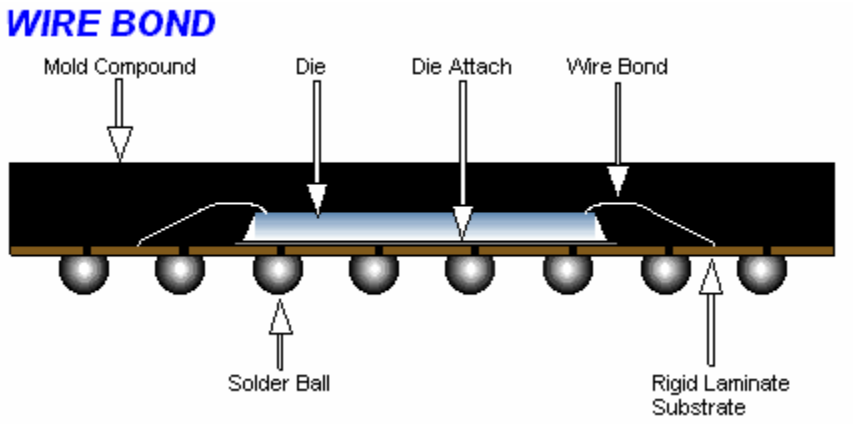
12) Encapsulation – Die Attach/Underfill/Mold

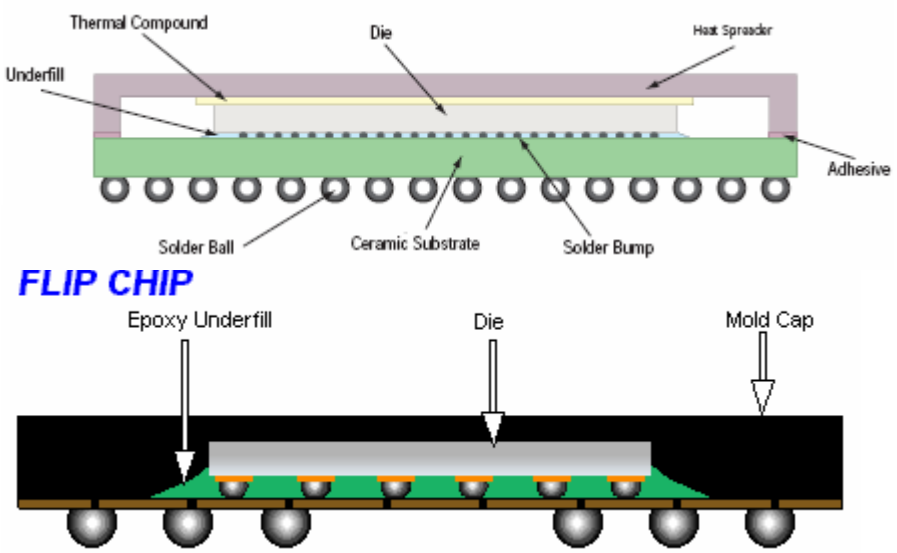
❖ Overmolding & Die attach in Wirebond Chips

- *Die attach Epoxy normally conductive*

❖ Overmolding & Under fill in Flipchip BGAs

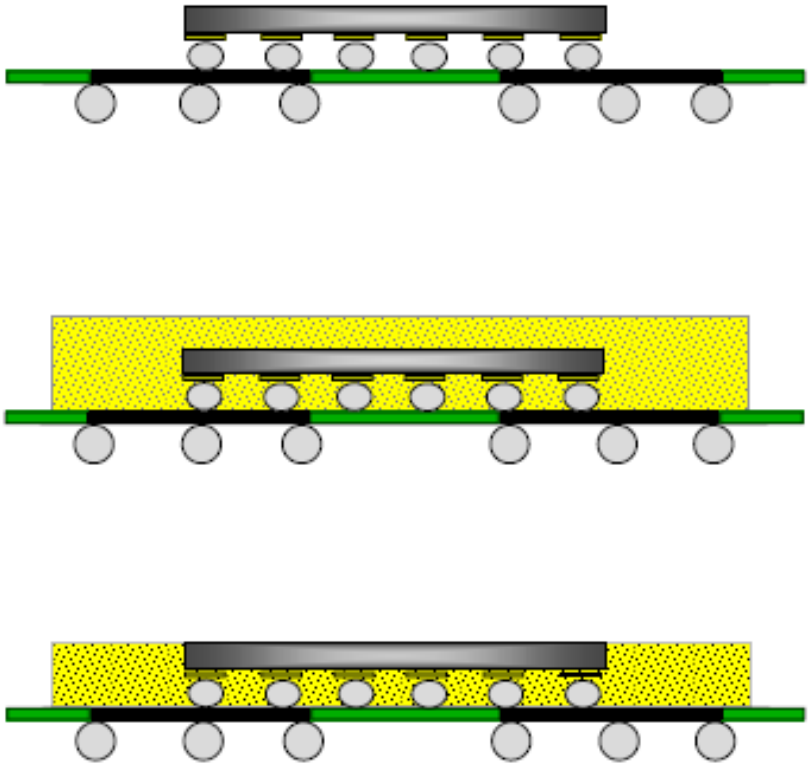
- *Underfill should be insulator*
- *Protection from shock and vibration*
- *Moisture control*



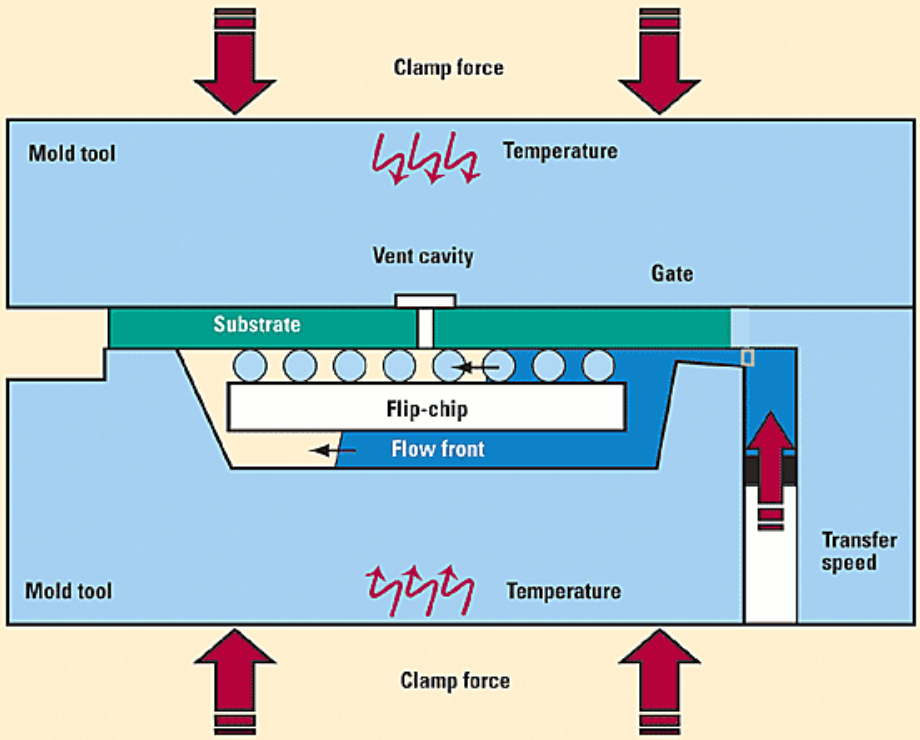


12) Encapsulation – Molded Underfill/Tooling

- ***Molded Underfill***
  - *Overmold material itself using for underfill*



Molded Underfill



Molded Underfill Tooling

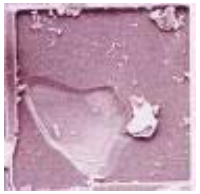
Package Related Failures

- **Bond Lifting**
  - Bond lifting refers to any of several phenomena in which a wire bond that connects the device to the outside world becomes detached from its position, resulting in loss or degradation of electrical and mechanical connection between that bond and its bonding site.

- **Bond Shorting**
  - Bond Shorting is the presence of an unintended electrical connection between two bonds.

- **Package Cracking**
  - Package cracking is the occurrence of fracture(s) anywhere in or on a semiconductor package.

- **Cratering**
  - Cratering is a partial or total fracture of the silicon material underneath the bond pad. Cratering is commonly due to excessive stresses on the bond pads from a poorly set up wire-bonding machine.

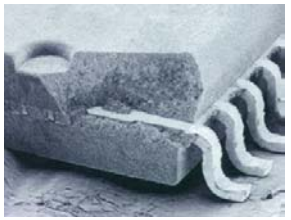


- **Die Lifting**
  - Die lifting is the dis-bonding or detachment of the die from its die pad or die cavity.

Package Related Failures

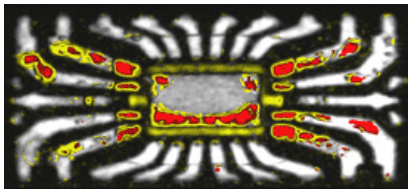
- ## Contamination
  - Contamination is the presence of a foreign material, whether attached or unattached, anywhere inside or external portions of the package and leads.

- ## Package Chip-outs
  - Package chipping is a failure mechanism wherein a part or parts of the package break away from the package itself.



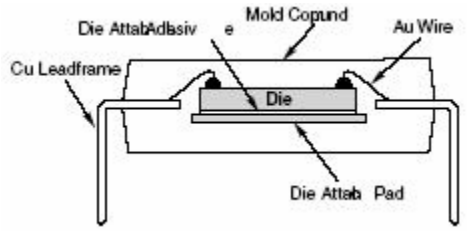
- ## Corrosion
  - Corrosion refers to the corrosion of the metal areas on the surface of the die or wire-bond or package leads.

- ## Package De-lamination
  - Package de-lamination refers to the dis-bonding between a surface of the package and that of another material.

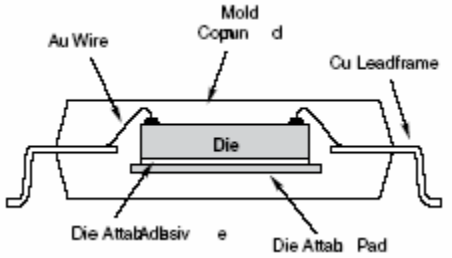


- ## Wire Depression
  - Wire depression is a condition wherein one or more wires of the device are deformed or pressed downwards. Wire depression is caused by purely mechanical means, usually by mishandling.

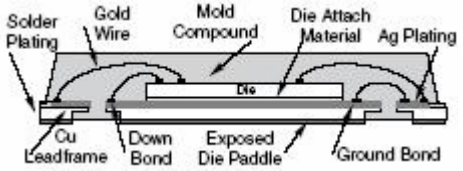
Some Package Structures (sample)



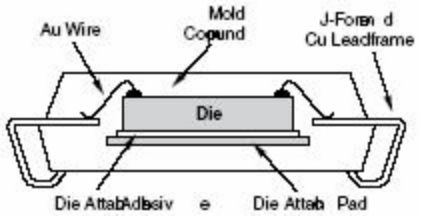
DIP



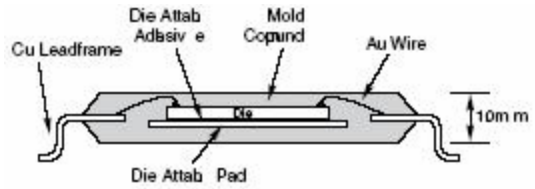
SSOP



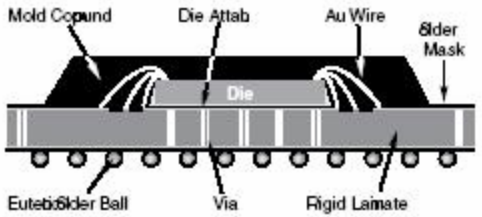
QFN



PLCC



QFP



BGA

Eco Friendly Packaging

Eco Friendly Packaging

- Eco packaging targets to use environmental friendly substances in the packaging and assembly process. It also targets to limit the hazardous substance to a minimum level in the packaging process.

Pb Free

- For Pb free Pb must be reduced below a certain level. In addition the package must survive Pb free assembly processes.

RoHS

- ROHS, which is the acronym for "Reduction of Hazardous Substances", is a directive from the European Union (EU) that restricts the use of six substances [Lead (Pb), Mercury (Hg), Cadmium (Cd), etc.] in new electrical and electronic equipment that are placed on the market by July 1, 2006.

Green Packaging

- The “Green” level packaging encompasses an even wider range of restrictions, and the requirements vary from region to region and customer to customer.

Thank You … !