

Chapter 7

Input/Output Circuitry

Input/Output circuits (**I/O pads**) are intermediate structures connecting internal signals from the **core** of the integrated circuit to the external pins of the **chip package**.

7.1 Padframes

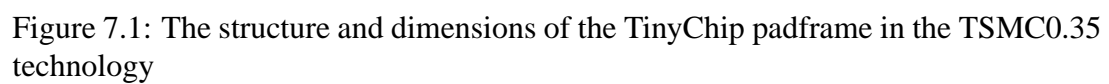
Typically I/O pads are organized into a rectangular **Padframe**.

The smallest **padframe** available for the MOSIS chip fabrication (<http://www.mosis.org/>), “TinyChip”, consists of 40 I/O pads, 10 on each side. We use such a padframe in our practical exercises.

The complete documentation of the I/O pads and resulting “TinyChip” padframe for the TSMC0.35 technology is available from <http://www.mosis.org/cell-libraries/scn035-pads-tiny/mTSMs035P.pdf>

Note that in the TSMC0.35 technology $\lambda = 0.2\mu$.

The structure and dimensions of the TinyChip padframe in the TSMC0.35 technology are given in Figure 7.1.



Note that the total size of the frame is $1.5 \times 1.5 \text{ mm}^2$. The internal space available for the core of the integrated circuit is $0.9 \times 0.9 \text{ mm}^2$ which is equivalent to $4500 \times 4500 \lambda^2$.

If we take into account that the size of an average standard cell is approximately $120 \times 40 \lambda^2$ then we can fit into the TinyChip padframe a circuit consisting of approximately **2500** standard cells (allowing 75% of the area for interconnections.)

The input/output pads are spaced with the pitch of $90 \mu\text{m} = 450 \lambda$.

The structure and dimensions of an I/O pad in the TSMC0.35 technology are given in Figure 7.2.

The size of the 40-pin padframe is $1.5 \times 1.5 \text{ mm}$, to core area being $0.9 \times 0.9 \text{ mm}$.

The total size of an **I/O pad** is $300 \times 90 \mu\text{m}^2$ ($1500 \times 450 \lambda^2$). The pad consists of

- a **bonding pad** — an area to which the bond wire is soldered.
The wire goes from the bonding pad to a chip pin.
The size of the bonding pad is $60 \times 60 \mu\text{m}^2$ ($300^2 \lambda^2$).
- ESD (electrostatic discharge) protecting circuitry consisting of a pair of big pMOS, nMOS transistors.
The ESP circuitry takes twice the area of $78 \times 78 \mu\text{m}^2$ ($390^2 \lambda^2$).
- Driving and logic circuitry for which the area of $46 \times 90 \mu\text{m}^2$ ($230 \times 450 \lambda^2$) is designated.

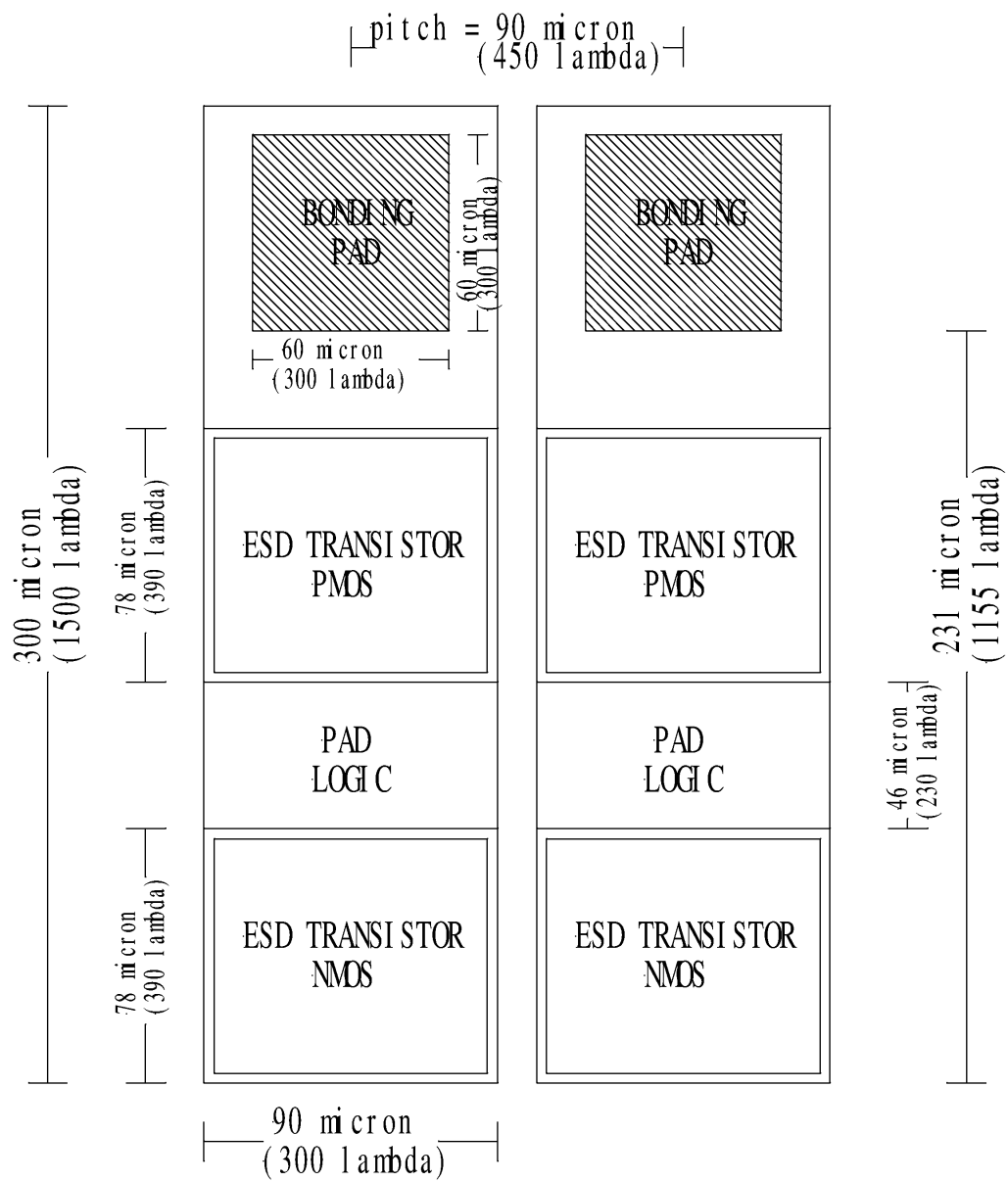


Figure 7.2: The structure and dimensions of an I/O pad in the TSMC0.35 technology

An example of the **layout of a TinyChip padframe** consisting of different I/O pads is given in Figure 7.3.

We note that in addition to different I/O pads, the padframe contains four corner pads which close the VDD and GND connections.

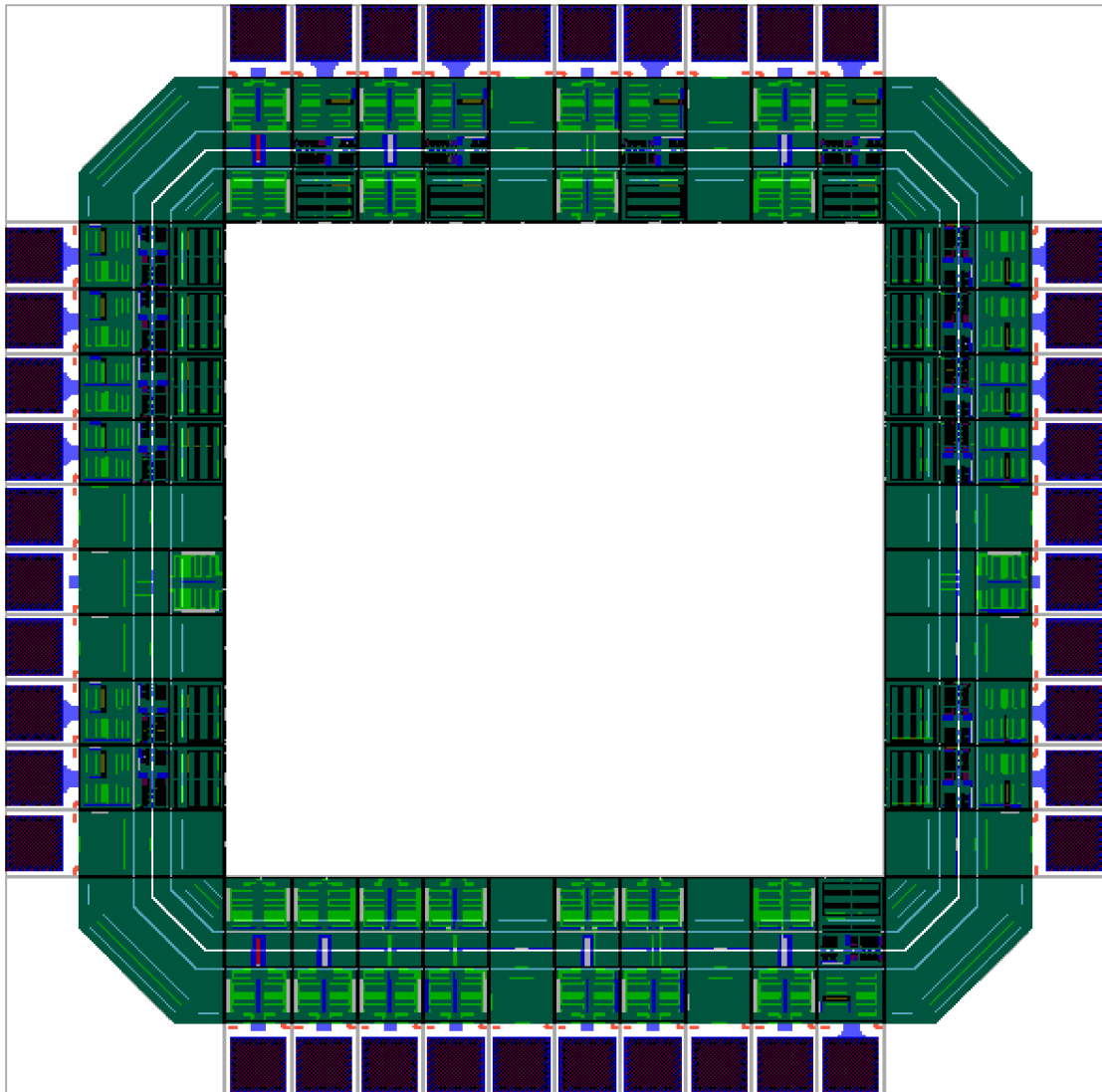


Figure 7.3: The layout of a TinyChip padframe in the TSMC0.35 technology

7.2 The simplest I/O pad

The simplest I/O pad (**PadARef**) available in the TMS035 technology consists of only

- Bonding pad, and
- ESD protection circuitry.

The schematic of the PadARef pad is given in Figure 7.4.

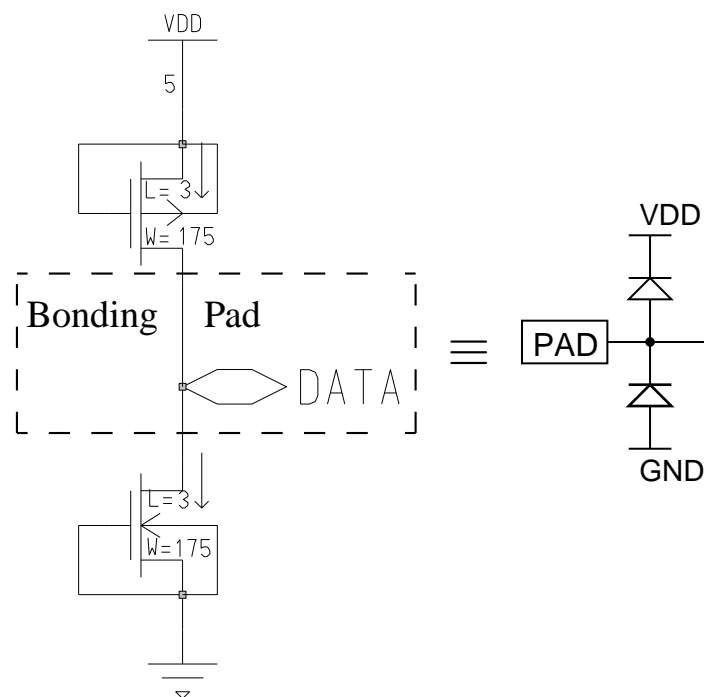


Figure 7.4: The schematic of the simplest I/O pad, PadARef, and its equivalent circuit.

It is a bidirectional pad with the DATA terminal being connected to the bonding pad. The ESD protection circuit consists of a pair of equivalent nMOS and pMOS transistors with gates tied up to the respective power supply terminals.

7.2.1 Fundamentals of the ESD protection

Electrostatic discharge (ESD) occurs when the charge stored in the human body or other devices is discharged to the gate of a MOS transistor on contact or by static induction.

If, for example, the charge on the human body is discharged as a current of $10\mu\text{A}$ flowing for $1\mu\text{s}$ to a gate capacitor of $C_g = 0.025\text{pF}$, then the voltage which will build up on the transistor gate is

$$V = \frac{10 \cdot 10^{-6} \cdot 10^{-6}}{0.025 \cdot 10^{-12}} = 400\text{V}$$

Such a voltage destroys MOS transistors, therefore, ESD protection is essential for the I/O circuitry.

A typical solution of the ESD protection problem is to use clamping diodes implemented using MOS transistors with gates tied up to either GND for nMOS transistors, or to VDD for pMOS transistors as shown in Figure 7.4.

For normal range of input voltages these transistors are in the off state. If the input voltage builds up above (or below) a certain level, one of the transistor starts to conduct clamping the input voltage at the save level.

These clamping transistors are very big structures (in the example of Figure 7.4 $L = 2\lambda$, $W = 175\lambda$) consisting of a number of transistors connected in parallel, and are able to sustain significant current.

7.2.2 The layout of the PadARef.

The layout of the PadARef together with the zoomed in the corner of the bonding pad is shown in Figure 7.5.

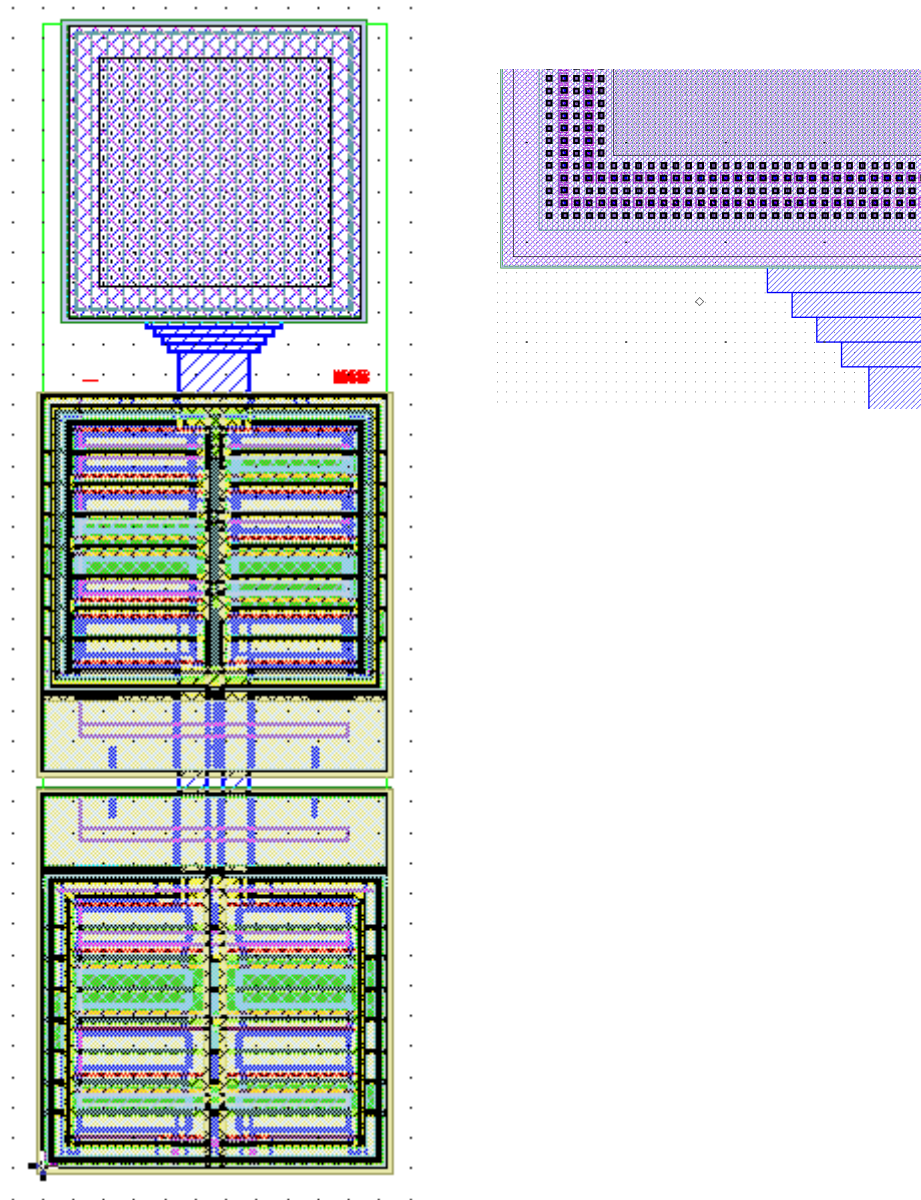


Figure 7.5: The layout of the complete PadARef (left) and a section of the corner of the bonding pad.

The bonding pad consists of three superimposed squares in metal 1, metal 2 and metal 3 joined together with respective vias (metal1-to-metal2 and metal2-to-metal3), as visible in the zoomed corner of the bonding pad shown in Figure 7.5.

The layout of the left-half of the **ESD protection** pMOS transistors are shown in Figure 7.6.

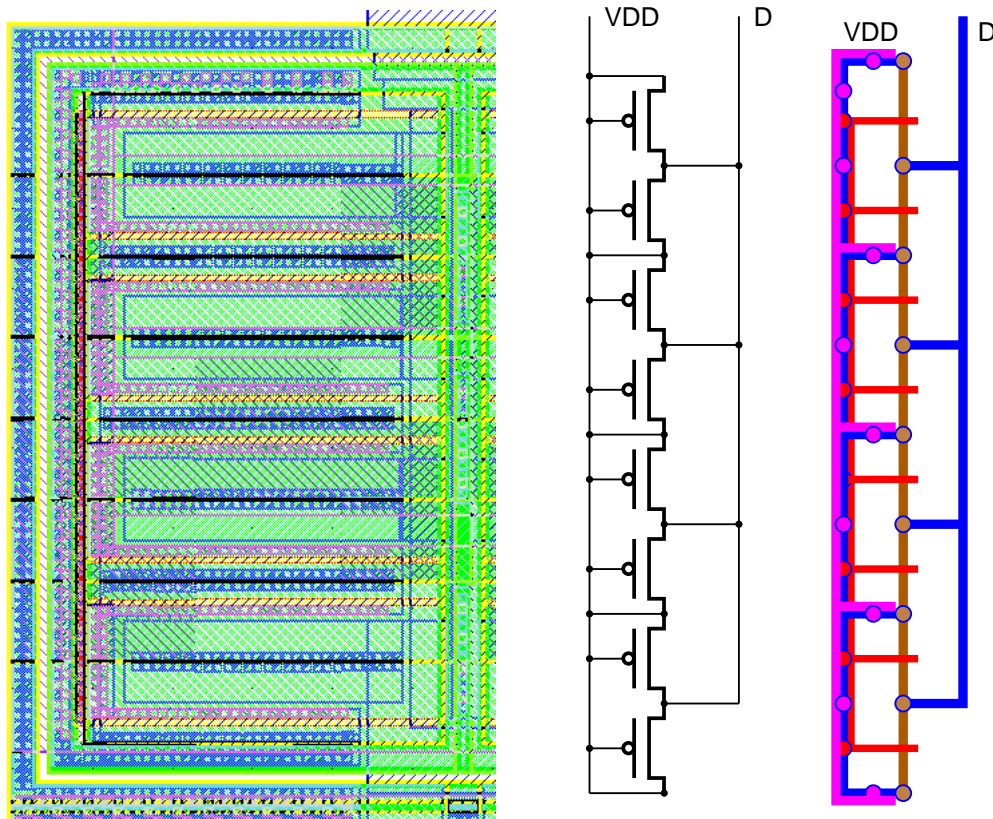


Figure 7.6: The layout of the left-half of the ESD protection pMOS transistors (left), the equivalent schematic and simplified stick diagram.

The core of the layout contains eight pMOS transistors, $3 \times 944 \lambda^2$ each, connected in parallel between the VDD and the signal terminal, D.

In Figure 7.7 we present a section of the layout with two ESD protection pMOS transistors.

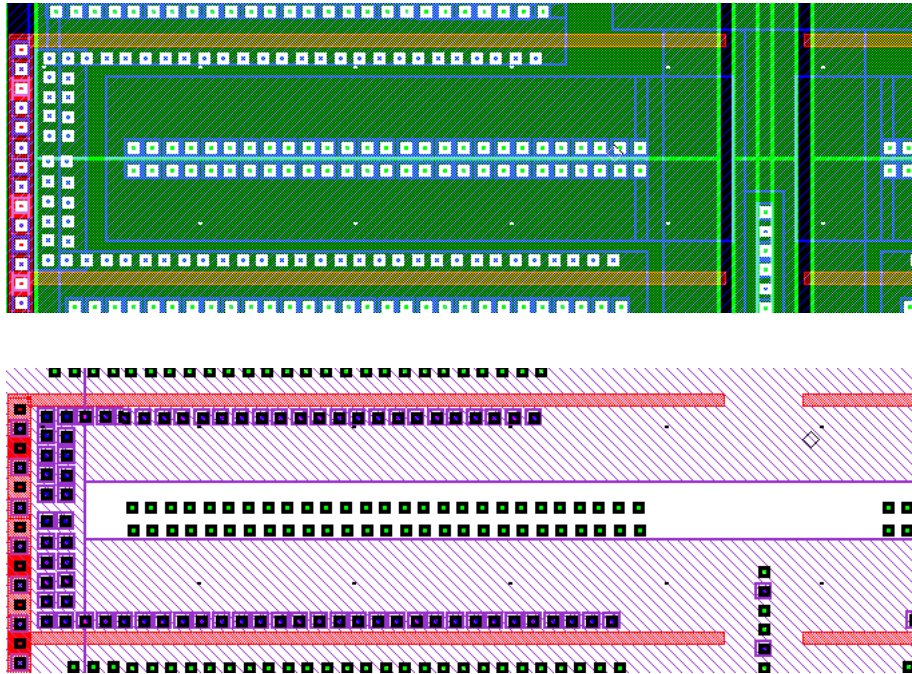


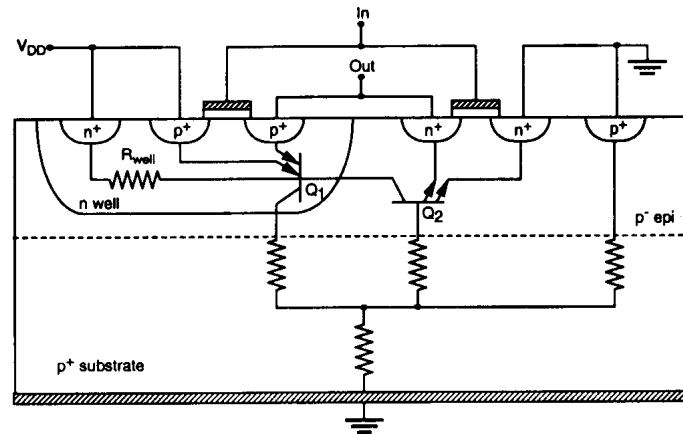
Figure 7.7: A section of the layout with two ESD protection pMOS transistors. Visible layers are: Top — polysilicon, active (p diffusion), metal 1 and contacts. Bottom — polysilicon, metal 2 and contacts.

A single ESD protection transistor has a size of $3 \times 175\lambda^2$. It can be observed that the metal 2 layer is used to distribute VDD whereas the metal 1 layer distributes the signal D. Note the contacts connecting the gates and sources of the transistors to VDD and drains to the signal terminal D.

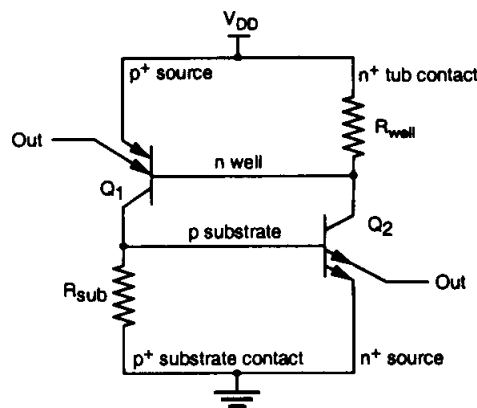
7.2.3 The Latch-up Problem and its prevention

Large MOS transistor are susceptible to the latch-up effect.

In the chip substrate, at the junctions of the p and n material, parasitic pnp and npn bipolar transistors are formed as in the following cross-sectional view:



These bipolar transistors form a silicon-controlled rectifier (SRC) with positive feedback as in the following circuit model:



The final result of the latch-up is the formation of a short-circuit (a low impedance path) between V_{DD} and GND which results in destruction of the MOS transistor.

Guidelines for Avoiding Latch-Up

(Quoted from Kang, Leblebici)

- Use p^+ **guard rings** connected to ground around nMOS transistors and n^+ guard rings connected to VDD around pMOS transistors to reduce R_w and R_{sub} and to capture injected minority carriers before they reach the base of the parasitic BJTs.
- Place substrate and well contacts as close as possible to the source connections of MOS transistors to reduce the values of R_w and R_{sub} .
- Use minimum area p-wells (in case of twin-tub technology or n-type substrate) so that the p-well photocurrent can be minimized during transient pulses.
- Source diffusion regions of pMOS transistors should be placed so that they lie along equipotential lines when currents flow between VDD and p-wells. In some n-well I/O circuits, wells are eliminated by using only nMOS transistors.
- Avoid the forward biasing of source/drain junctions so as not to inject high currents; the use of a lightly doped epitaxial layer on top of a heavily doped substrate has the effect of shunting lateral currents from the vertical transistor through the low- resistance substrate.
- Lay out n- and p-channel transistors such that all nMOS transistors are placed close to GND and pMOS transistors are placed close to VDD rails. Also maintain sufficient spacings between pMOS and nMOS transistors.

Double guard rings.

The concept of the guard rings is best explained in a simplified layout shown in Figure 7.8.

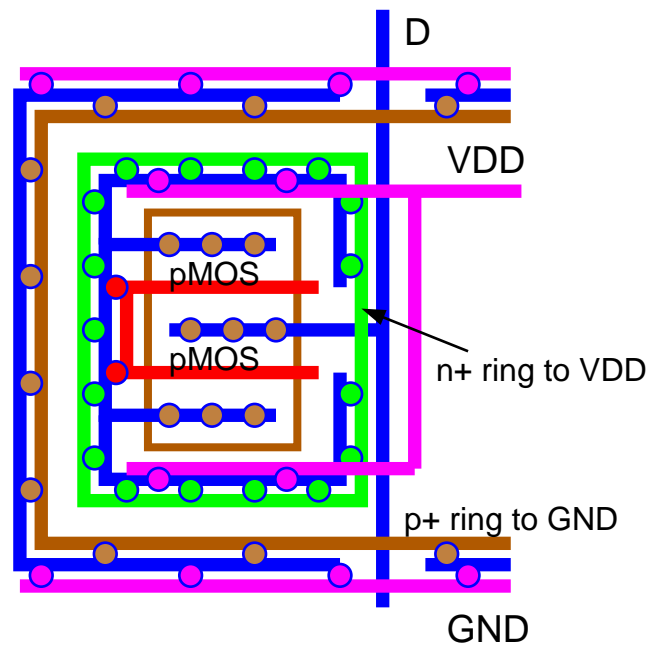


Figure 7.8: A simplified layout illustrating double guard rings.

A pair of pMOS transistors is surrounded by a n^+ guard ring (green) formed from the n diffusion. The n^+ guard ring is connected to VDD. The p^+ guard ring formed from p diffusion encircles the whole structure and is connected to GND

In Figure 7.9 a section of the layout of the PadARef is shown to demonstrate the implementation of the double guard rings.

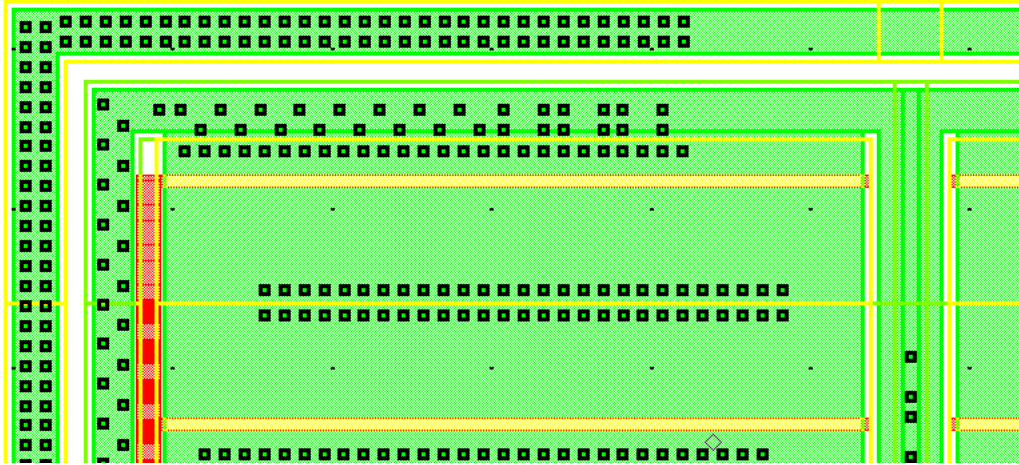
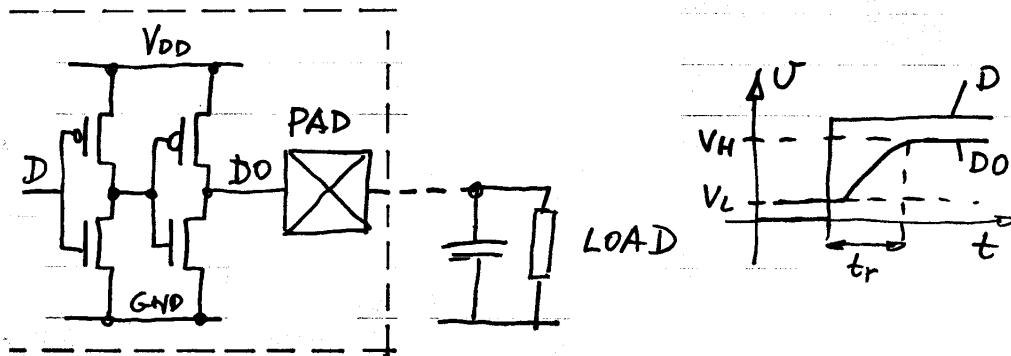


Figure 7.9: Double guard rings in the PadARef.

For clarity only the poly, active, p+, n+, and active contacts are shown. The external n^+ guard ring consists of the active layer surrounded by the n+ mask (yellow). The internal p^+ guard ring consists of the active layer surrounded by the p+ mask (light green).

7.3 Output pads

The simplest driver for the output pad consists of a pair of inverters with large transistors (in addition to the standard ESD protection circuitry).



The driver must be able to supply enough current (must have enough driving capability) to achieve satisfactory rise and fall times (t_r , t_f) for a given capacitive load.

In addition the driver must meet any required DC characteristics regarding the levels of output voltages for a given load type, namely, CMOS or TTL.

7.4 Bidirectional pads

In the TSMC0.35 pad library there is a bidirectional pad that can also be used as a **tri-state output** pad or an **input** pad.

The schematic of the **input section** of the bidirectional pad is shown in Figure 7.10.

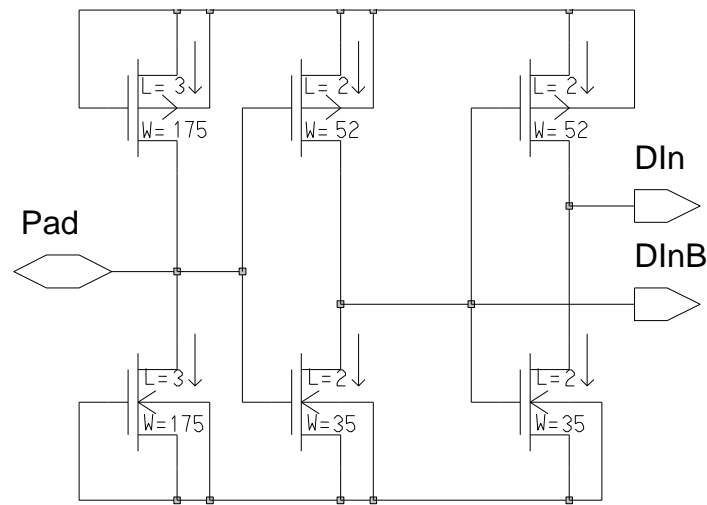


Figure 7.10: The schematic of the input section of the bidirectional pad from the TSMC0.35 pad library.

The external signal is coming through **Pad** and after double inversion is available to the core circuitry as signal **DIn**.

Note the ESD protection transistors connected to the input **Pad**.

A simplified schematic of the **tri-state output section** of the bidirectional pad is shown in Figure 7.11.

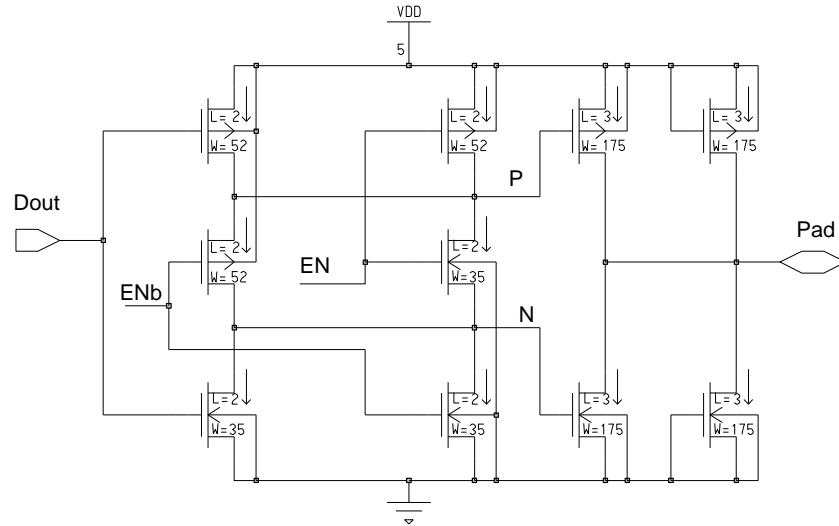


Figure 7.11: A simplified schematic of the tri-state output section of the bidirectional pad from the TSMC0.35 pad library.

The signal **Dout** is generated by the chip core circuitry together with the enable signal **EN** and its complement **ENb**.

The 3 pairs of MOS transistor generate two signals **P** and **N** which drive the pair of big output transistors forming the output signal **Pad** according to the following truth table:

EN	ENb	Dout	P	N	Pad
0	1	*	1	0	Z
1	0	0	1	1	0
1	0	1	0	0	1

$$\text{Pad} = \begin{cases} Z & \text{if } \text{EN} = 0 \\ \text{Dout} & \text{if } \text{EN} = 1 \end{cases}$$

The complete transistor level schematic of the output section of the bidirectional pad includes additional three pairs of inverters for amplify signals **EN**, **P** and **N**.

The layout of the nMOS section of the tri-state driver is shown in Figure 7.12.

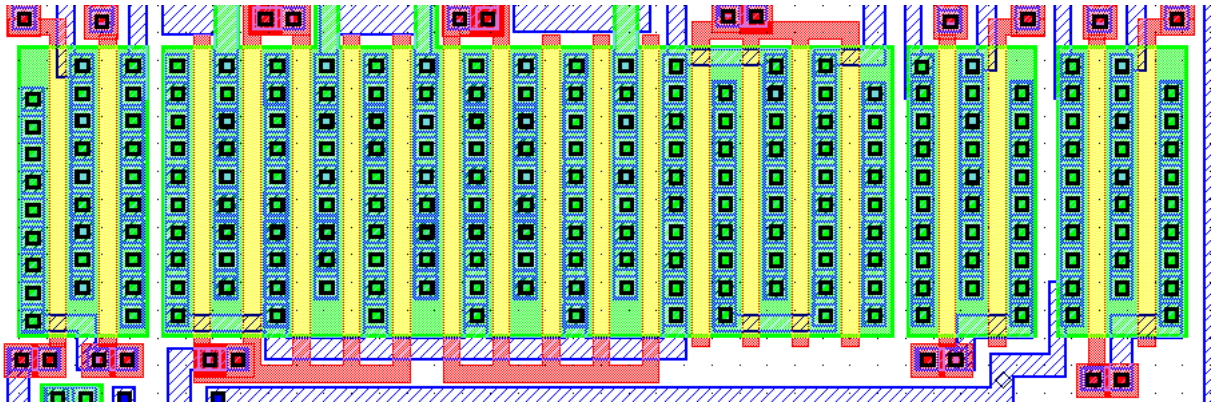


Figure 7.12: The layout of the nMOS section of the tri-state driver of the output pad. The metal 2 layer has been removed for clarity.

From the left-hand side we identify nMOS transistor belonging to:

- nMOS transistor belonging to a pair of inverters of the enable signal,
- three groups of parallel connected transistors belonging to the circuit generating signals P and N,
- nMOS transistor belonging to two pairs of inverters amplifying signals P, and N.