1. **BASIC GATES.**
2. **UNIVERSAL GATES.**
3. **EXCLUSIVE GATES.**
4. **HALF ADDER, FULL ADDER, HALF SUBTRACTOR AND FULL SUBTRACTOR.**
5. **2X1, 4X1, 8X1 AND 16X1 MULTIPLEXURE.**
6. **2 TO 4 AND 3 TO 8 DECODER.**
7. **4 TO 2 ENCODER AND 8 TO 3 ENCODER.**
8. **4 BIT ADDER.**
9. **4 BIT ADDER SUBTRACTOR COMPOSITE UNIT.**
10. **4 BIT CARRY LOOK AHEAD ADDER.**

1. FULL ADDER USING HALF ADDER AS COMPONENT.
2. FULL SUBTRACTOR USING HALF SUBTRACTOR AS COMPONENT.
3. 16X1 MUX USING 4X1 MUX AS COMPONENT.
4. SR, JK, D AND T FLIP FLOP.
5. 4 BIT BINARY UP COUNTER AND 4 BIT BINARY DOWN COUNTER.
6. JOHNSON COUNTER.
7. DECADE COUNTER.
8. RIPPLE COUNTER.
9. MOD-5 COUNTER.
10. 3 BIT UP/DOWN COUNTER.

1. Design a circuit to implement BCD Addition/Binary Addition depending on the selec

that it can perform BCD Addition of A=0011(12) AND B=0010(20) as well as Binary Add

C=1011(11) and D=1101(13) depending upon a select input. Veryfy the results with atl

inputs for each case.

2. Design a 4bit ALU to perform the following set of operations :

ALU Operation	Description
Add Signed	R = A + B : Treating A, B, and R as signed two's complement integers.
Subtract Signed	R = A - B : Treating A, B, and R as signed two's complement integers.
Bitwise AND	R(i) = A(i) AND B(i).
Bitwise NOR	R(i) = A(i) NOR B(i).
Bitwise OR	R(i) = A(i) OR B(i).
Bitwise NAND	R(i) = A(i) NAND B(i).
Bitwise XOR	R(i) = A(i) XOR B(i).
Biwise NOT	R(i) = NOT A(i).