EE560 : Reconfigurable Computing
Lab III: FPGA Experiment

Objective:

The objective of this experiment is to interface the FPGA with a clock, switches, and LED. The description of the FPGA board and other details are given below.

- Zybo Z7-10 has a clock of 125MHz, which can be accessed from the "K17" pin.
- Zybo Z7-10 has four switches, which can be accessed from pins described in the design constraints below. Switch can generate two states as logic '0' and '1'. The switch in its lower position generates logic '0' in the upper position generates logic '1'.
- Zybo Z7-10 has four buttons, which can be accessed from pins described in the design constraints below. Button can generate two states as logic '0' and '1'. By pressing a button it generates logic '1' or else in idle state it generates logic '0'.
- Zybo Z7-10 has four LEDs, which can be accessed from pins described in the design constraints below. LED can be turn ON by passing '1' to the pin.

```
##Clock signal
#set_property -dict { PACKAGE_PIN K17   IOSTANDARD LVCMOS33 } [get_ports { sysclk }];
#IO_L12P_T1_MRCC_35 Sch=sysclk

#create_clock -add -name sys_clk_pin -period 8.00 -waveform {0 4} [get_ports { sysclk }];


##Switches
#set_property -dict { PACKAGE_PIN G15   IOSTANDARD LVCMOS33 } [get_ports { sw[0] }];
#IO_L19N_T3_VREF_35 Sch=sw[0]
#set_property -dict { PACKAGE_PIN P15   IOSTANDARD LVCMOS33 } [get_ports { sw[1] }];
#IO_L24P_T3_34 Sch=sw[1]
#set_property -dict { PACKAGE_PIN W13   IOSTANDARD LVCMOS33 } [get_ports { sw[2] }];
#IO_L4N_T0_34 Sch=sw[2]
#set_property -dict { PACKAGE_PIN T16   IOSTANDARD LVCMOS33 } [get_ports { sw[3] }];
#IO_L9P_T1_DQS_34 Sch=sw[3]


##Buttons
#set_property -dict { PACKAGE_PIN K18   IOSTANDARD LVCMOS33 } [get_ports { btn[0] }];
#IO_L12N_T1_MRCC_35 Sch=btn[0]
#set_property -dict { PACKAGE_PIN P16   IOSTANDARD LVCMOS33 } [get_ports { btn[1] }];
#IO_L24N_T3_34 Sch=btn[1]
#set_property -dict { PACKAGE_PIN K19   IOSTANDARD LVCMOS33 } [get_ports { btn[2] }];
#IO_L10P_T1_AD11P_35 Sch=btn[2]
#set_property -dict { PACKAGE_PIN Y16   IOSTANDARD LVCMOS33 } [get_ports { btn[3] }];
#IO_L7P_T1_34 Sch=btn[3]


##LEDs
#set_property -dict { PACKAGE_PIN M14   IOSTANDARD LVCMOS33 } [get_ports { led[0] }];
#IO_L23P_T3_35 Sch=led[0]
#set_property -dict { PACKAGE_PIN M15   IOSTANDARD LVCMOS33 } [get_ports { led[1] }];
#IO_L23N_T3_35 Sch=led[1]
#set_property -dict { PACKAGE_PIN G14   IOSTANDARD LVCMOS33 } [get_ports { led[2] }];
#IO_0_35 Sch=led[2]
#set_property -dict { PACKAGE_PIN D18   IOSTANDARD LVCMOS33 } [get_ports { led[3] }];
#IO_L3N_T0_DQS_AD1N_35 Sch=led[3]
```

1 Assignments

FPGA on-board clock has a frequency of 125 MHz. Using the on board clock, design a real-time clock.

- The circuit should start its operation only when start='1', else the circuit is OFF.
- The rereal-timelock should have an output *sec*, which will be blinking for every second.
- The real time clock should have an output *min*, to count the minutes of the real-time clock.
- The clock should stop after reaching its maximum output (min). The clock can be started again after a reset only. A done signal can be used to indicate the timer reached its maximum value. After pressing reset *rst* only, the clock should work again.
- There should be a stop as input to the real time clock. When stop is pressed clock should stay in the idle state. The clock should stop counting the seconds upon **stop**.
- The totop modules given below.

```
module clock_Expt(clk,sec,min,done,rst, start, stop);
input clk;
input rst, stop, start;
output reg sec, done;
output reg [1:0] min;
```

Deadline:-14th Feb, 2025