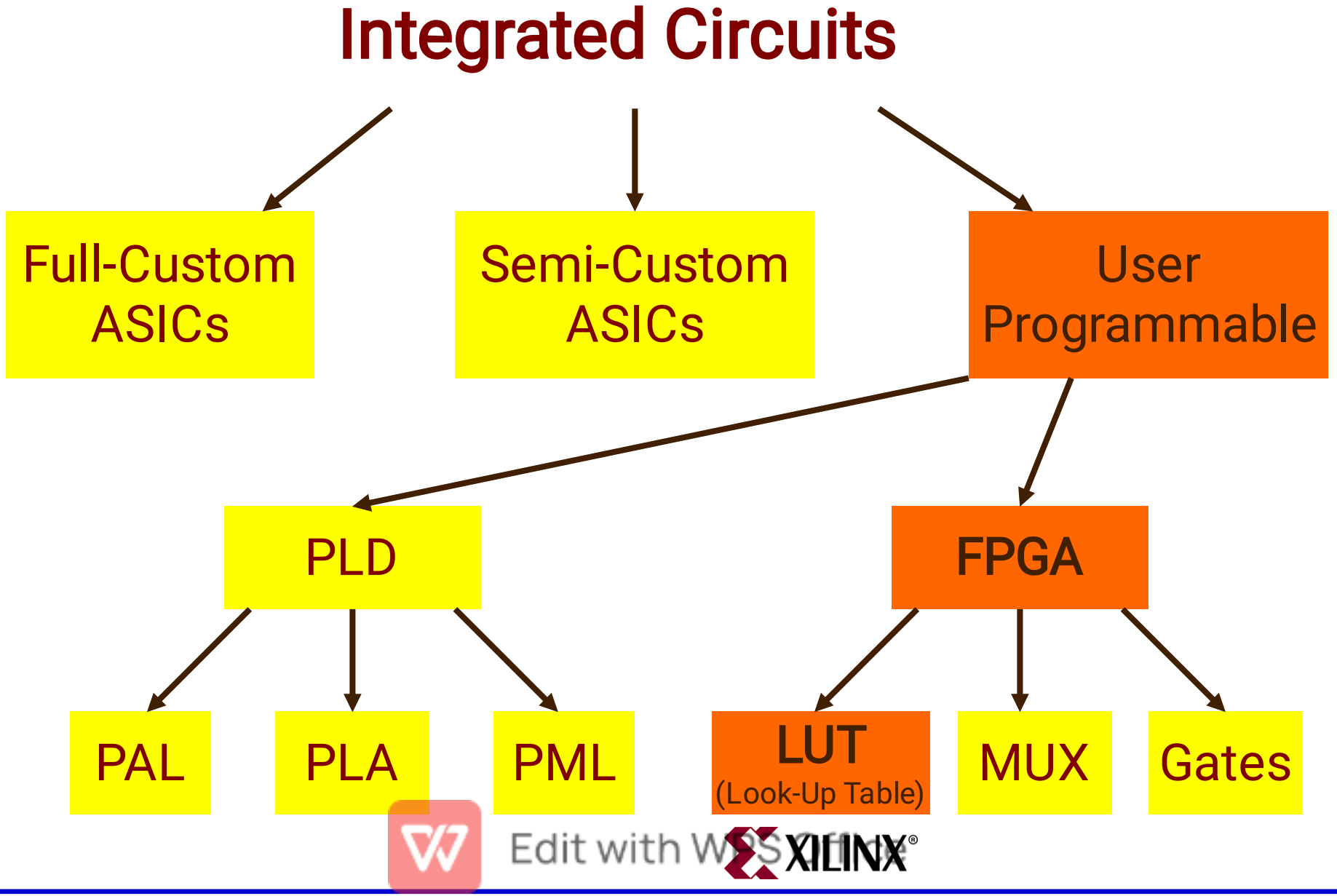
Introduction to FPGA Devices and V

Unit IV

World of Integrated Circuits



Two competing implementation approaches

ASIC
Application Specific Integrated Circuit

- designs must be sent for expensive and time consuming fabrication in semiconductor foundry
- designed all the way from behavioral description to physical layout

FPGA
Field Programmable Gate Array

- bought off the shelf and reconfigured by designers themselves
- no physical layout design; design ends with a bitstream used to configure a device

FPGA DISADVANTAGE

*High per-part costs

*High volume applications should consider ASICs

*Perhaps use FPGA for prototyping

*Lower performance than ASIC

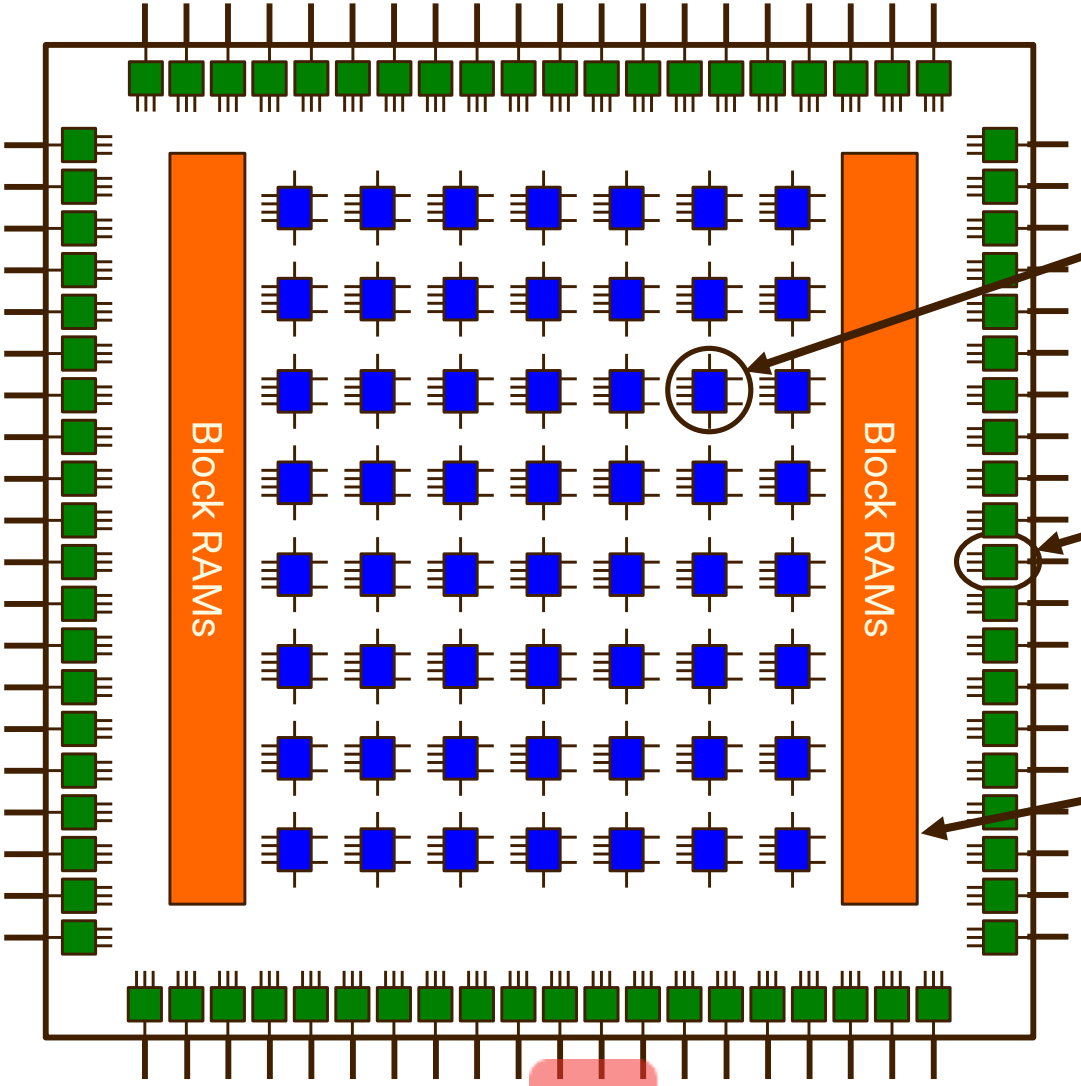
*Higher power than ASIC

*More specialized design skills than CPU

Programmable Logic Device

- Programmable Logic Device
  - Programmable Logic Array, Programmable Array Logic, Field Programmable Gate Array
- All layers already exist
  - Designers can purchase an IC
  - To implement desired functionality
    - Connections on the IC are either created or destroyed to implement
- Benefits
  - Very low NRE costs
  - Great time to market
- Drawback
  - High unit cost, bad for large volume
  - Power
    - Except special PLA
  - slower

What is an FPGA?

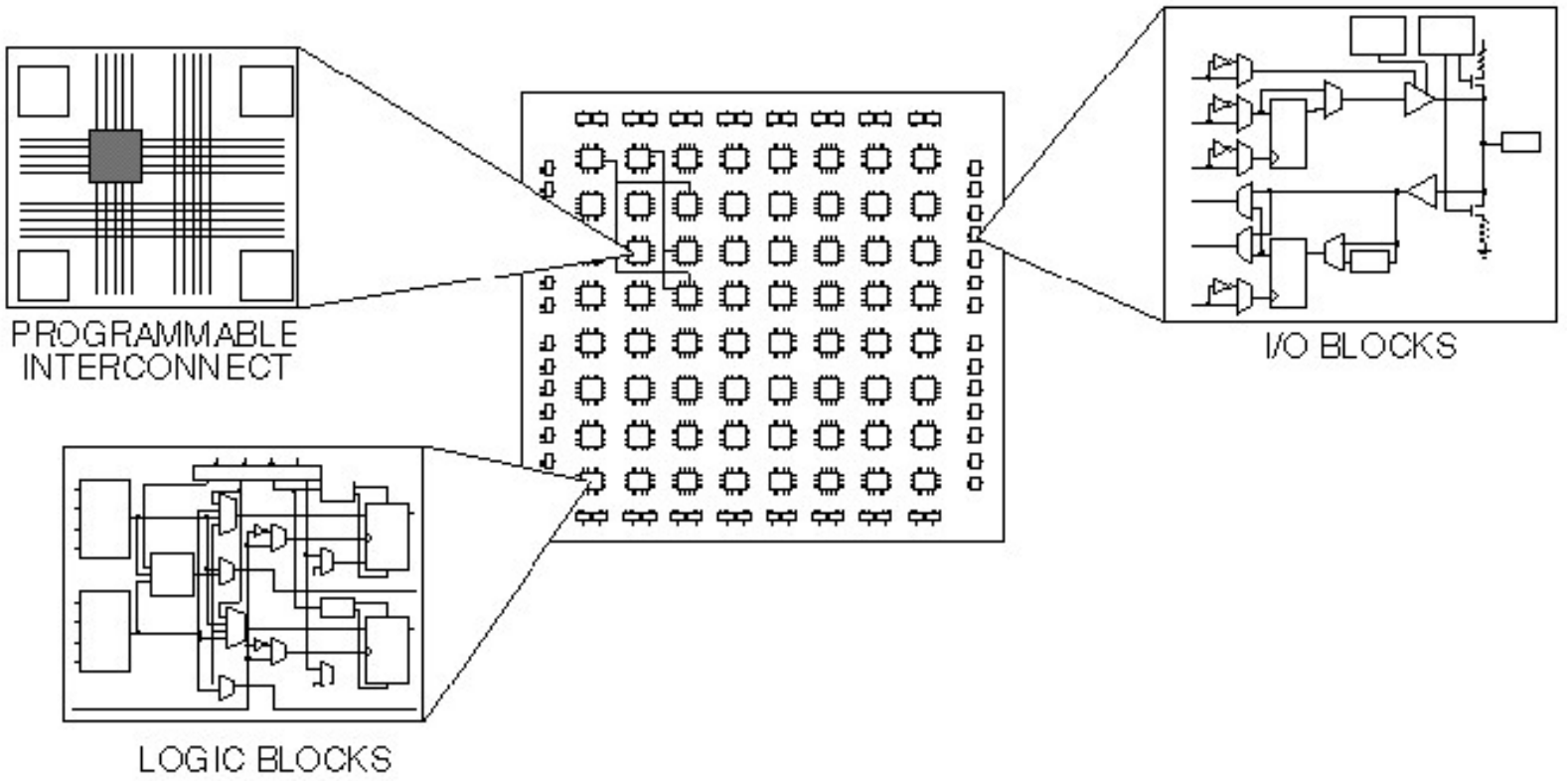


Configurable Logic Blocks

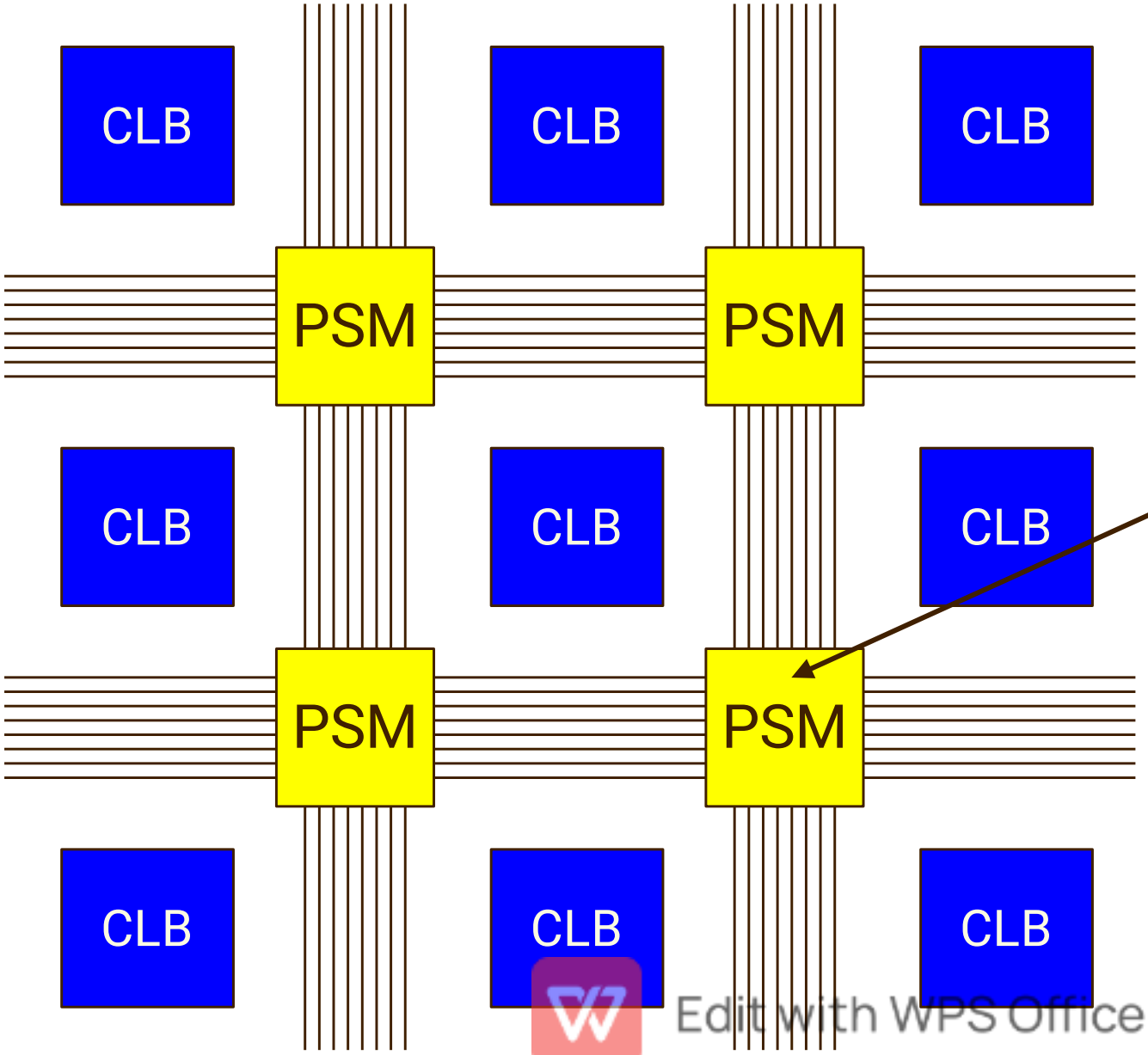
I/O Blocks

Block RAMs

Xilinx FPGA

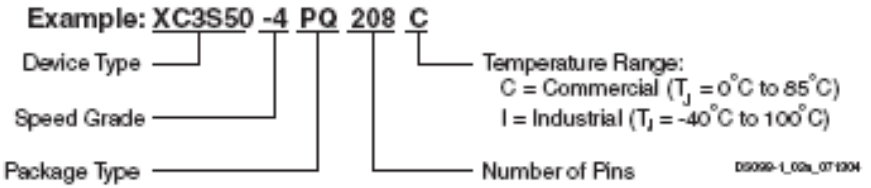


Routing Resources



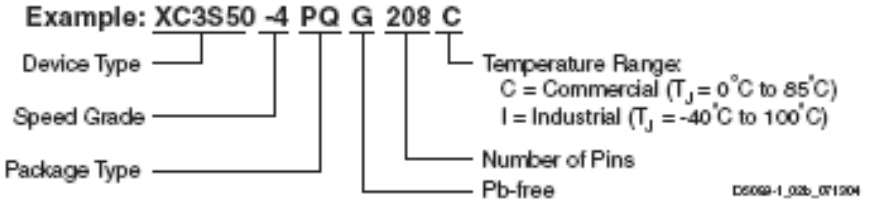
FPGA Nomenclature

Standard Packaging



Pb-Free Packaging

For additional information on Pb-free packaging, see XAPP427: "Implementation and Solder Reflow Guidelines for Pb-Free Packages".



Device
XC3S50
XC3S200
XC3S400
XC3S1000
XC3S1500
XC3S2000
XC3S4000
XC3S5000

Speed Grade	
-4	Standard Performance
-5	High Performance[1]

Package Type / Number of Pins	
VQ(G)100	100-pin Very Thin Quad Flat Pack (VQFP)
CP(G)132	132-pin Chip-Scale Package (CSP)
TQ(G)144	144-pin Thin Quad Flat Pack (TQFP)
PQ(G)208	208-pin Plastic Quad Flat Pack (PQFP)
FT(G)256	256-ball Fine-Pitch Thin Ball Grid Array (FTBGA)
FG(G)320	320-ball Fine-Pitch Ball Grid Array (FBGA)
FG(G)456	456-ball Fine-Pitch Ball Grid Array (FBGA)
FG(G)676	676-ball Fine-Pitch Ball Grid Array (FBGA)
FG(G)900	900-ball Fine-Pitch Ball Grid Array (FBGA)
FG(G)1156	1156-ball Fine-Pitch Ball Grid Array (FBGA)

Temperature Range (T_J)	
C	Commercial (0°C to 85°C)
I	Industrial (–40°C to 100°C)

Major FPGA Vendors

SRAM-based FPGAs

- **Xilinx, Inc.**
- **Altera Corp.**

} Share over 60% of the market

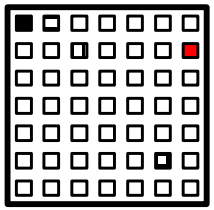
- Atmel
- Lattice Semiconductor

Flash & antifuse FPGAs

- Actel Corp.
- Quick Logic Corp.

Xilinx

- Primary products: FPGAs and the associated CAD software



Programmable
Logic Devices

ISE Alliance and Foundation
Series Design Software

- Main headquarters in San Jose, CA
- Fabless* Semiconductor and Software Company
  - UMC (Taiwan) {*Xilinx acquired an equity stake in UMC in 1996}
  - Seiko Epson (Japan)
  - TSMC (Taiwan)

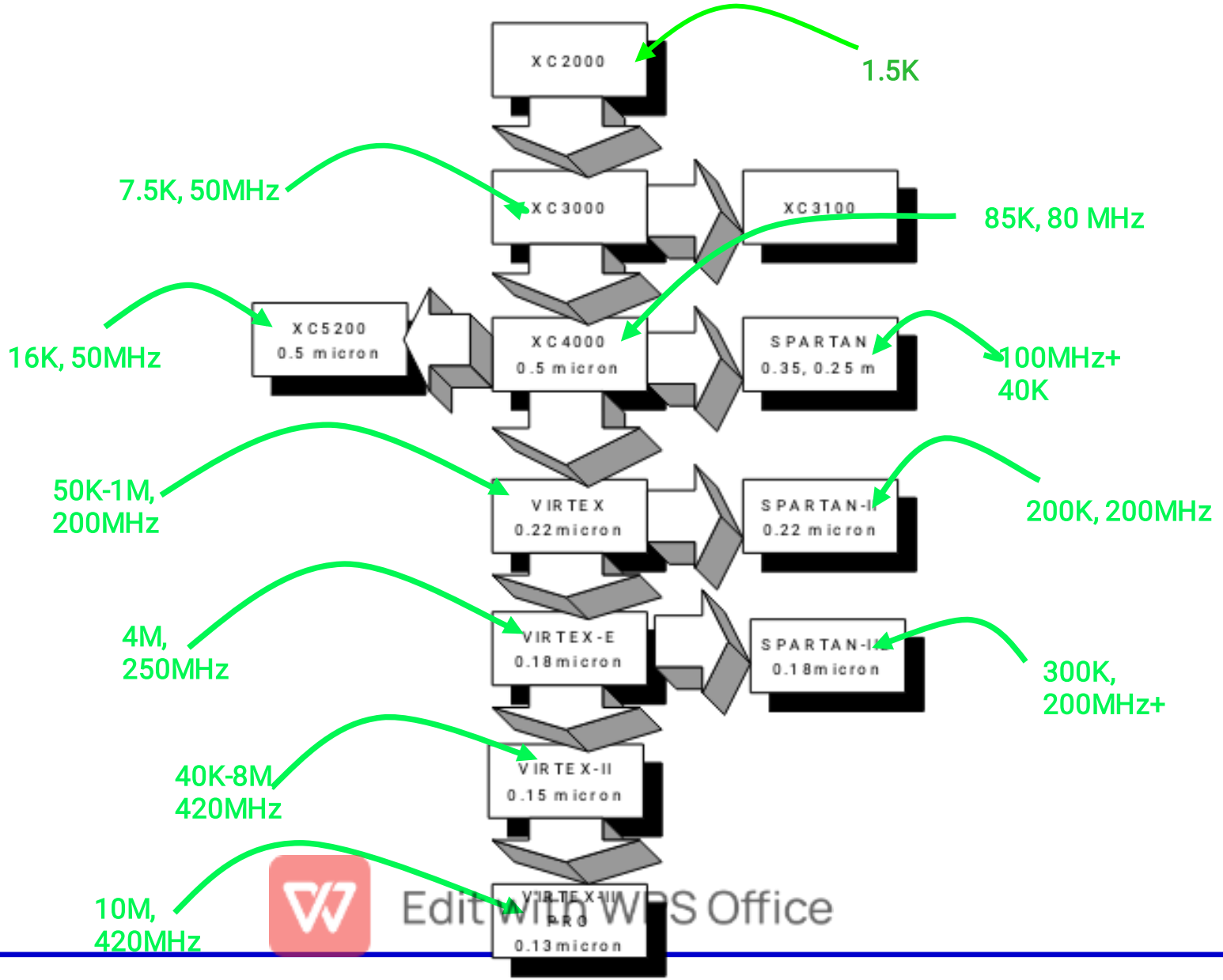
Xilinx FPGA Families

- Old families
  - XC3000, XC4000, XC5200
  - Old 0.5µm, 0.35µm and 0.25µm technology. Not recommended for modern designs.
- **High-performance families**
  - Virtex (0.22µm)
  - Virtex-E, Virtex-EM (0.18µm)
  - Virtex-II, Virtex-II PRO (0.13µm)
  - Virtex-4 (0.09µm)
- **Low Cost Family**
  - Spartan/XL – derived from XC4000
  - Spartan-II – derived from Virtex
  - Spartan-IIE – derived from Virtex-E
  - Spartan-3

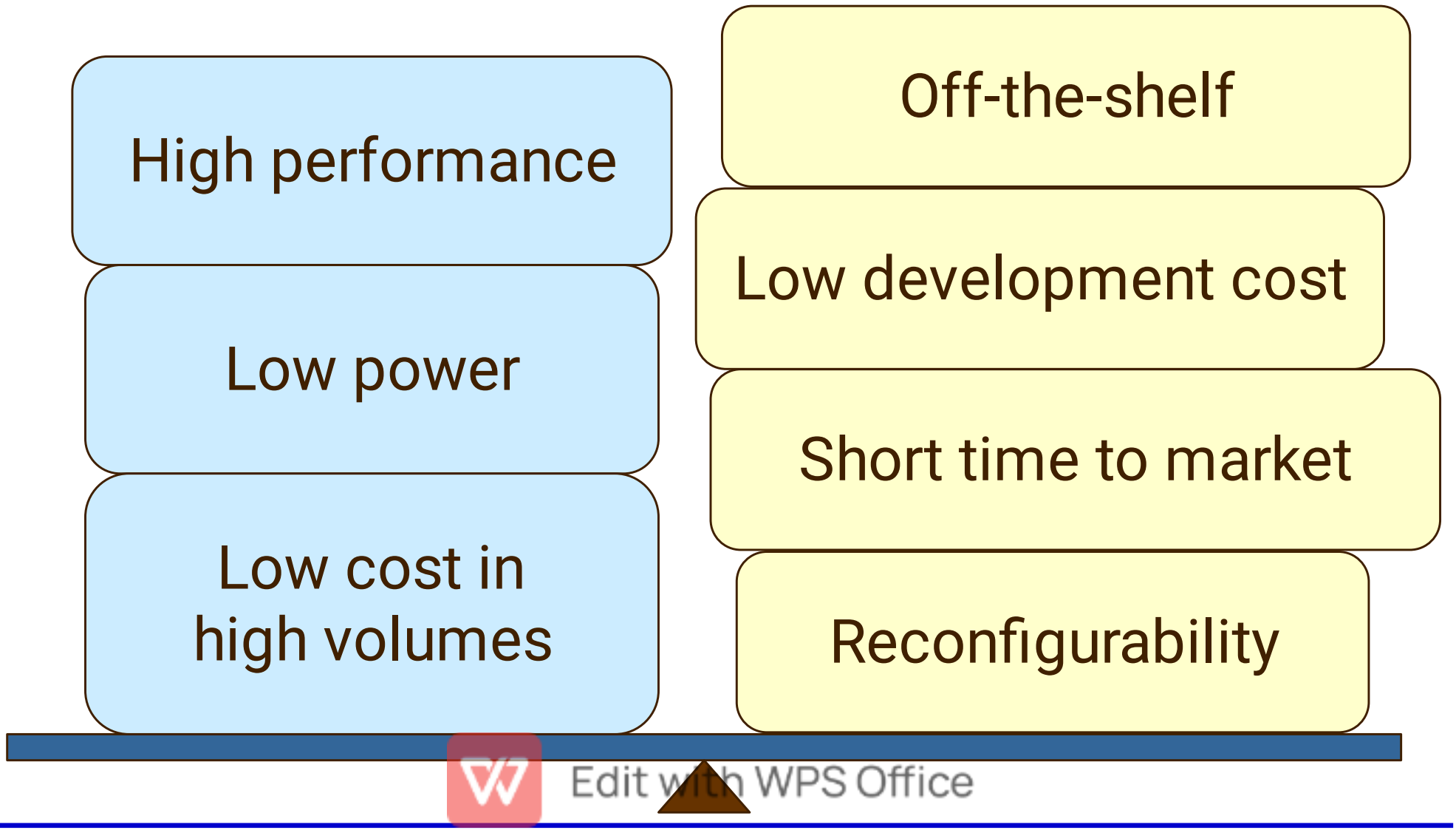
Spartan-3 FPGA Family Members

Device	System Gates	Equivalent Logic Cells	CLB Array (One CLB = Four Slices)			Distributed RAM (bits[1])	Block RAM (bits[1])	Dedicated Multipliers	DCMs	Maximum User I/O	Maximum Differential I/O Pairs
			Rows	Columns	Total CLBs						
XC3S50[2]	50K	1,728	16	12	192	12K	72K	4	2	124	56
XC3S200[2]	200K	4,320	24	20	480	30K	216K	12	4	173	76
XC3S400[2]	400K	8,064	32	28	896	56K	288K	16	4	264	116
XC3S1000[2, 3]	1M	17,280	48	40	1,920	120K	432K	24	4	391	175
XC3S1500[3]	1.5M	29,952	64	52	3,328	208K	576K	32	4	487	221
XC3S2000	2M	46,080	80	64	5,120	320K	720K	40	4	565	270
XC3S4000[3]	4M	62,208	96	72	6,912	432K	1,728K	96	4	712	312
XC3S5000	5M	74,880	104	80	8,320	520K	1,872K	104	4	784	344

Xilinx FPGAs : An Endless Journey



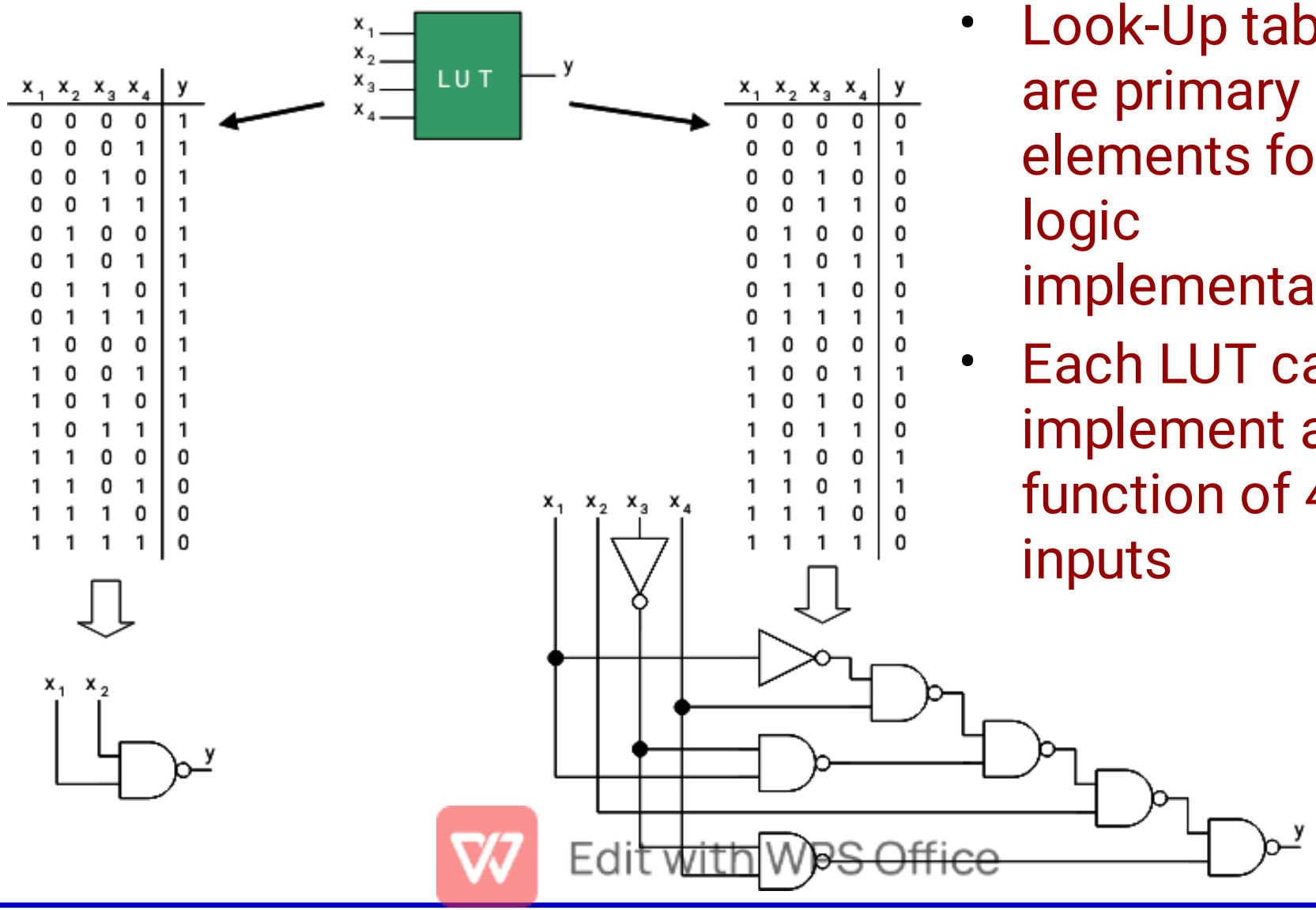
Which Way to Go?



Other FPGA Advantages

- Manufacturing cycle for ASIC is very costly, lengthy and engages lots of manpower
  - Mistakes not detected at design time have large impact on development time and cost
  - FPGAs are perfect for rapid prototyping of digital circuits
- Easy upgrades like in case of software
- Unique applications
  - reconfigurable computing

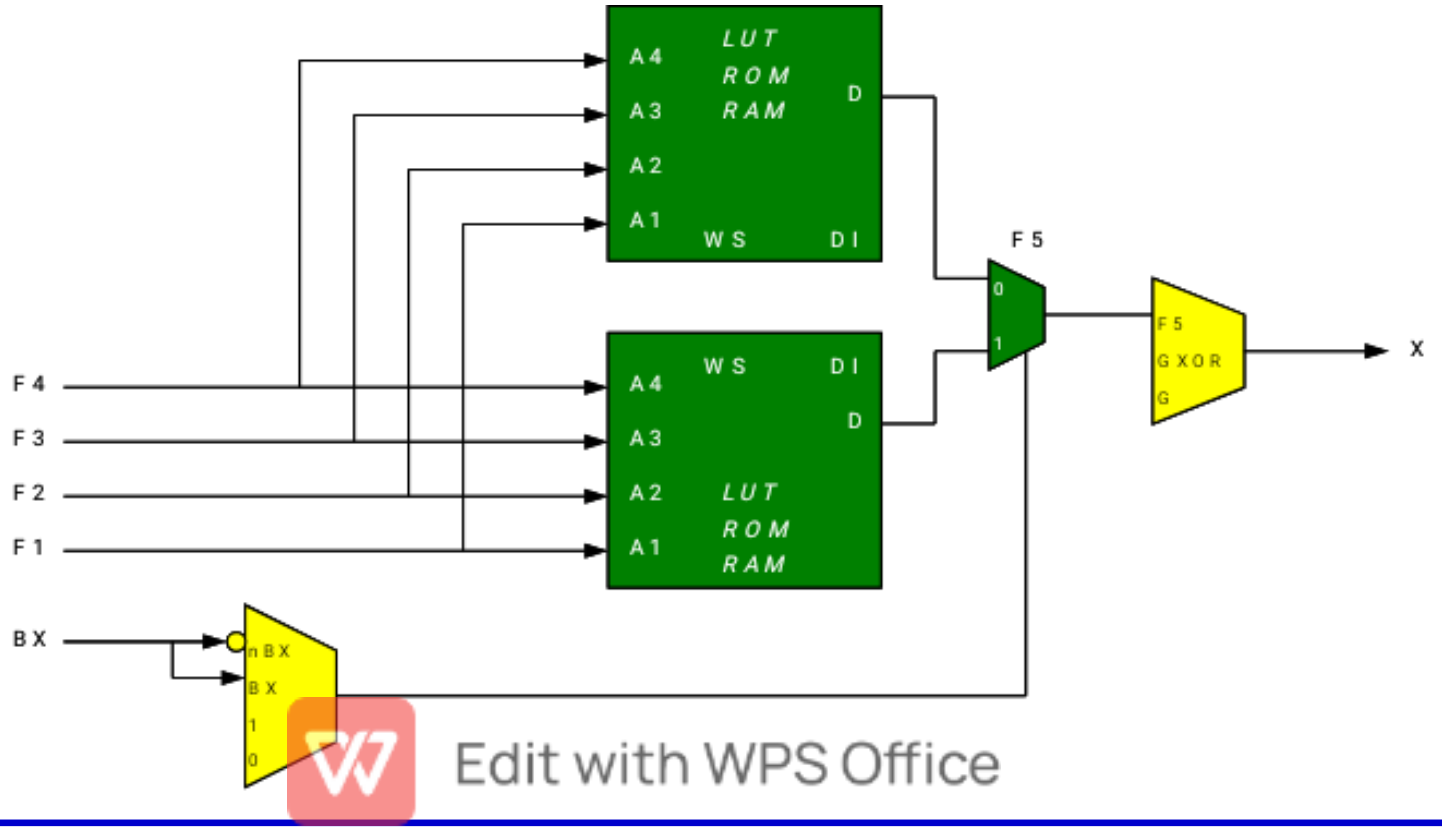
LUT (Look-Up Table) Functionality



- Look-Up tables are primary elements for logic implementation
- Each LUT can implement any function of 4 inputs

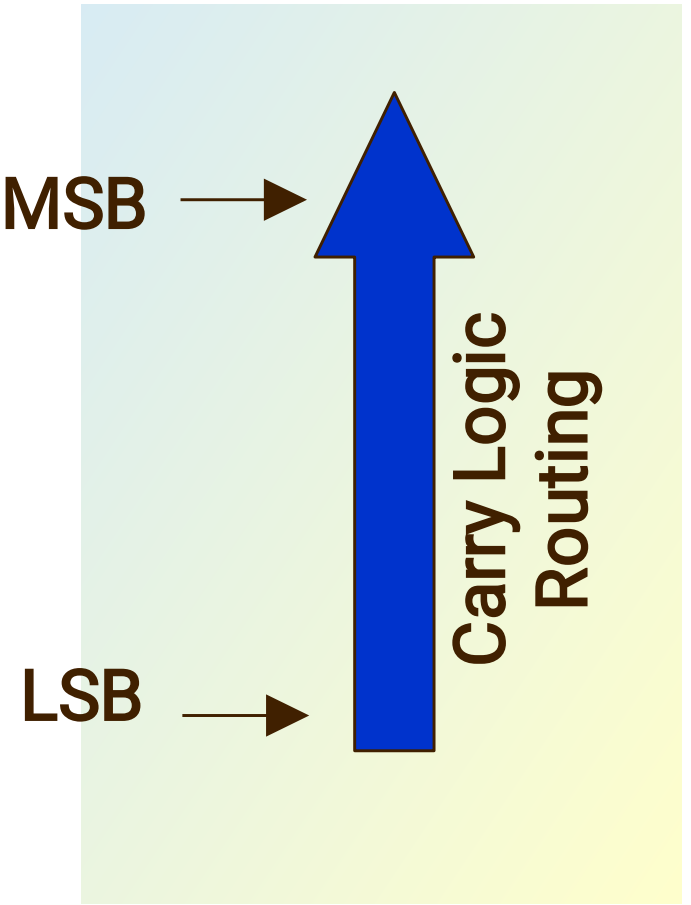
5-Input Functions implemented using two LUTs

- One CLB Slice can implement any function of 5 inputs
- Logic function is partitioned between two LUTs
- F5 multiplexer selects LUT

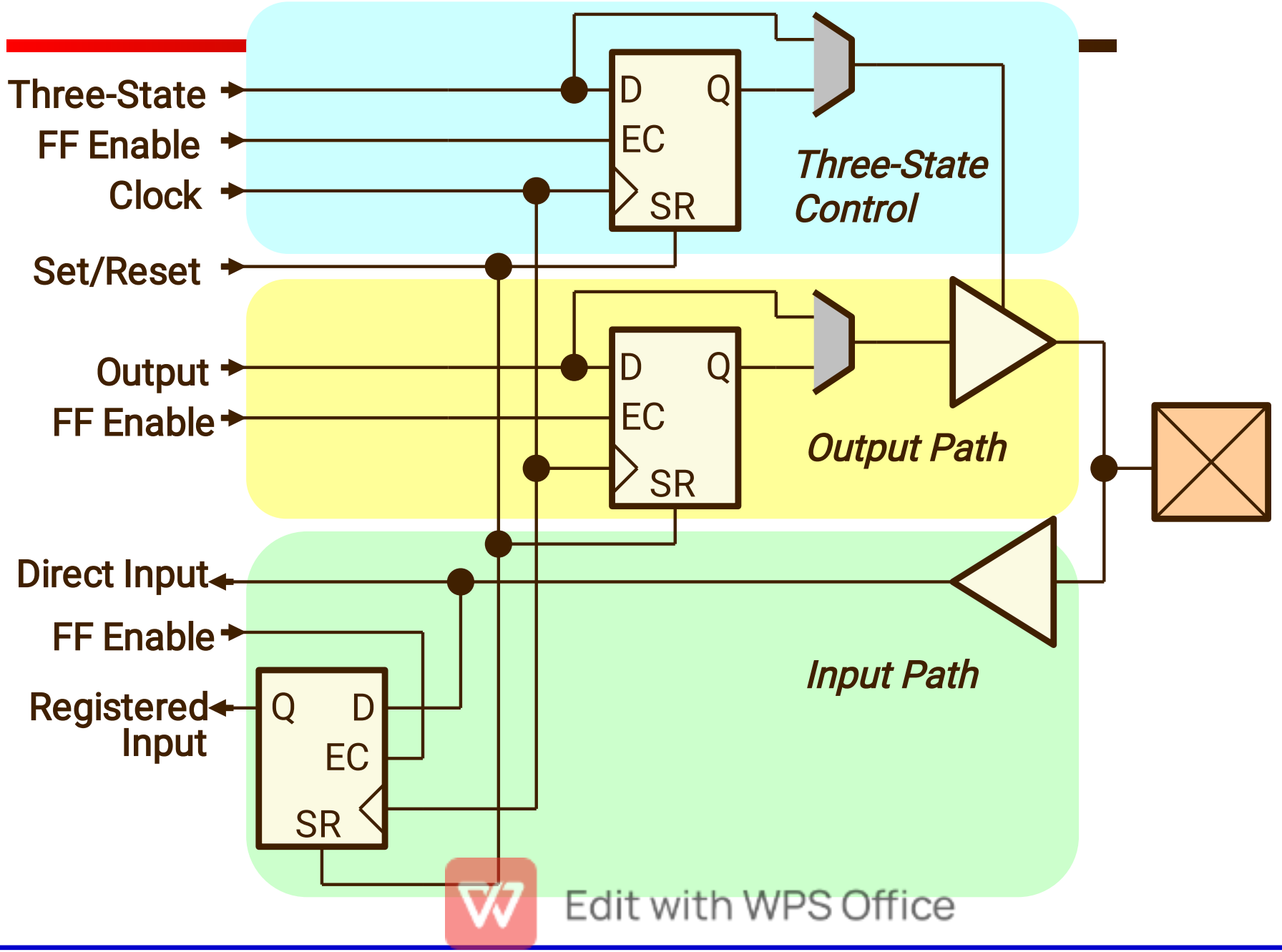


Fast Carry Logic

- Each CLB contains separate logic and routing for the fast generation of sum & carry signals
  - Increases efficiency and performance of adders, subtractors, accumulators, comparators, and counters
- Carry logic is independent of normal logic and routing resources



Basic I/O Block Structure



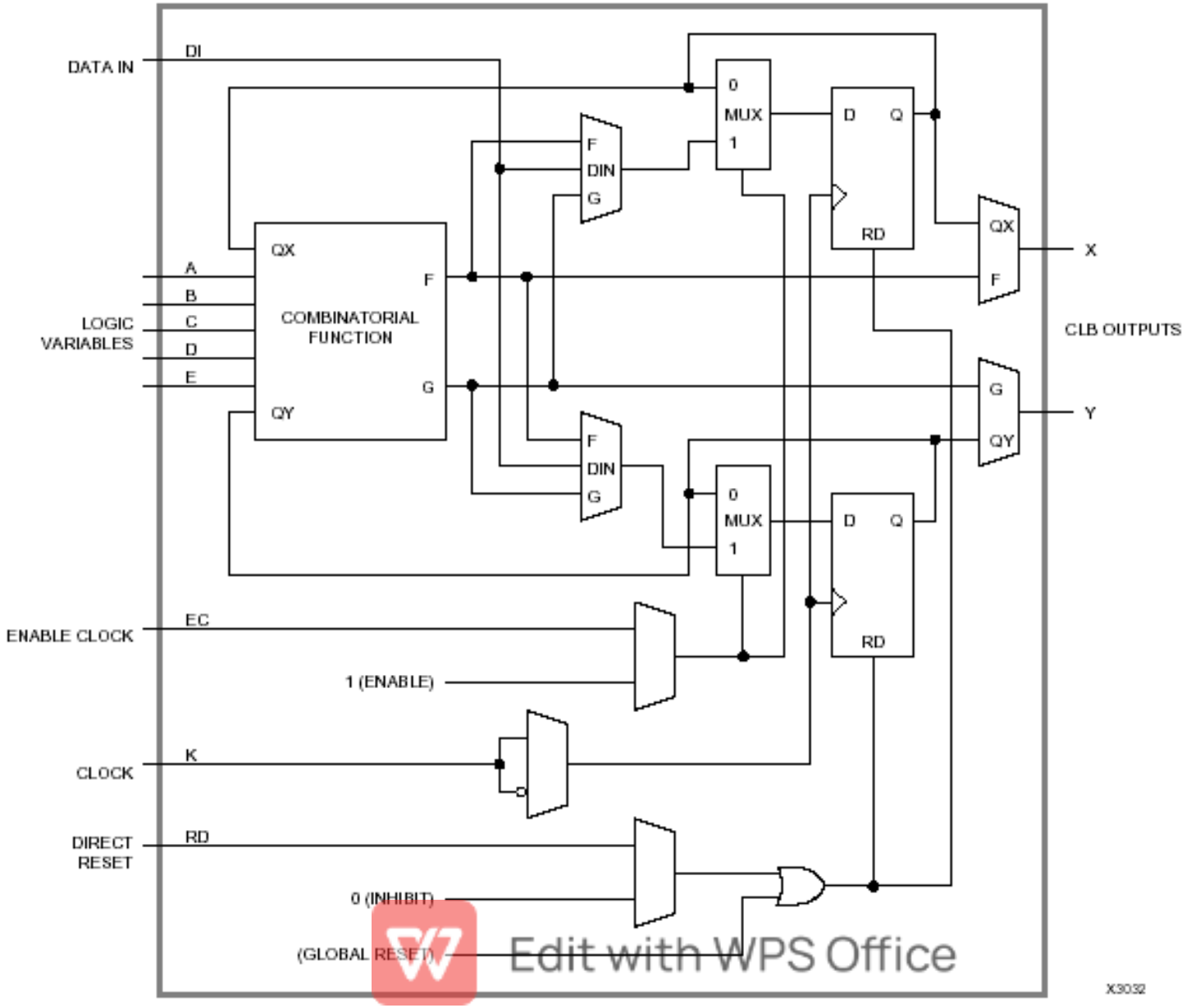
IOB Functionality

- IOB provides interface between the package pins and CLBs
- Each IOB can work as uni- or bi-directional I/O
- Outputs can be forced into High Impedance
- Inputs and outputs can be registered
  - advised for high-performance I/O
- Inputs can be delayed

XC3000

- Replaces TTL, MSI and other PLD logics.
- Integrates complete subsystem into single Package.
- System clock Speed up to 50 MHz.
- On-chip crystal Oscillator.
- Low-Skew Clock Nets.
- Over 20 different Packaging Options
- Interface to popular design Environment like Mentor, Cadence and View Logic.

XC3000 CLB



Xilinx XC3000 CLB

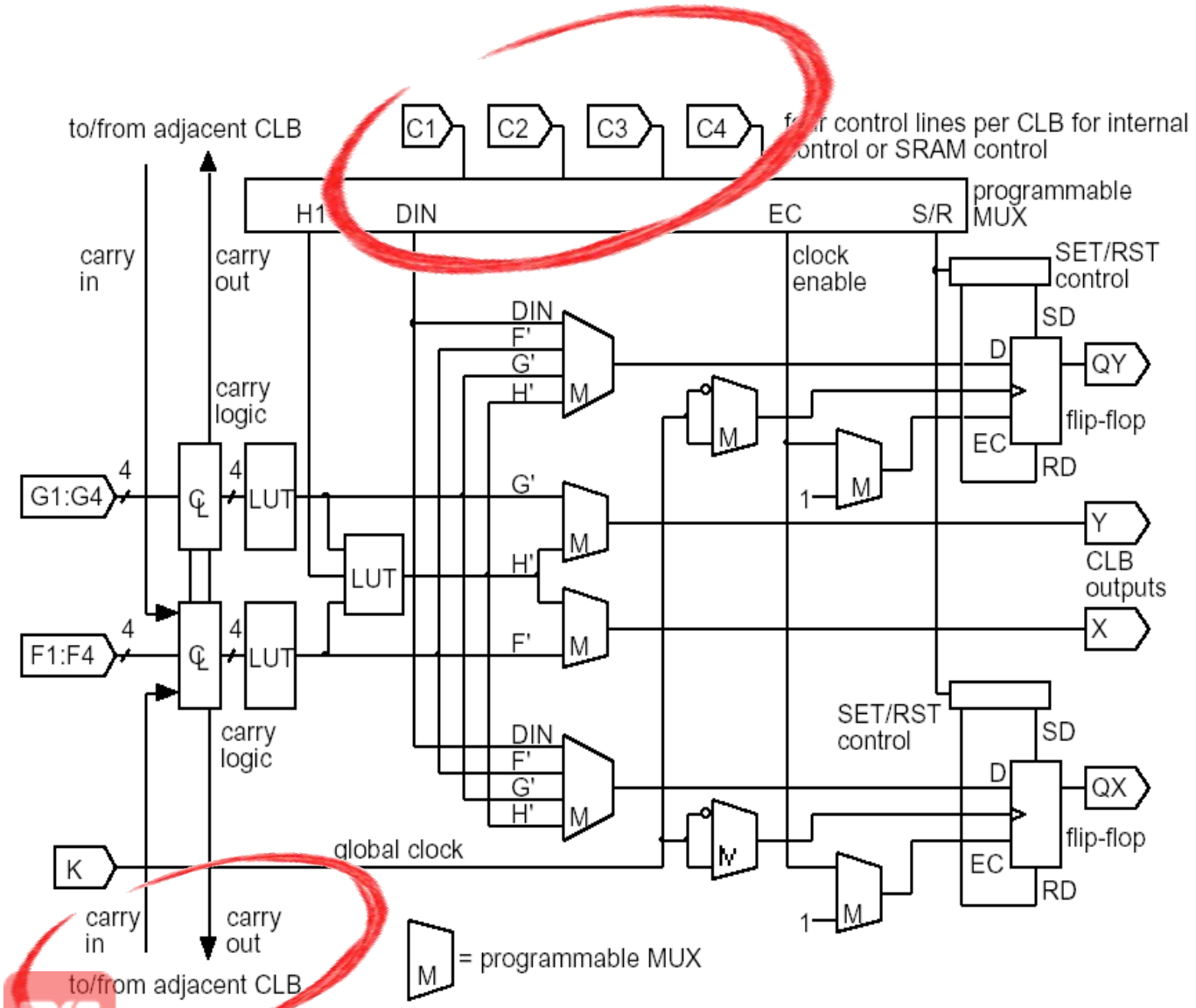
- A 32-bit look-up table (LUT)
- CLB propagation delay is fixed (the LUT access time) and independent of the logic function
- 7 inputs to the XC3000 CLB:
  - 5 CLB inputs (A–E), and
  - 2 flip-flop outputs (QX and QY)
- 2 outputs from the LUT (F and G).
- Since a 32-bit LUT requires only five variables to form a unique address ($32 = 2^5$), there are multiple ways to use the LUT

Xilinx XC3000 CLB

- Use 5 of the 7 possible inputs (A–E, QX, QY) with the entire 32-bit LUT
  - the CLB outputs (F and G) are then identical
- Split the 32-bit LUT in half to implement 2 functions of 4 variables each
  - choose 4 input variables from the 7 inputs (A–E, QX, QY).
  - you have to choose 2 of the inputs from the 5 CLB inputs (A–E); then one function output connects to F and the other output connects to G
- You can split the 32-bit LUT in half, using one of the 7 input variables as a select input to a 2:1 MUX that switches between F and G
  - to implement some functions of 6 and 7 variables

Xilinx XC4000 Family CLB

- The block diagram for the XC4000 family CLB is similar to that of the CLB of the XC3000
- Carry logic connections shown



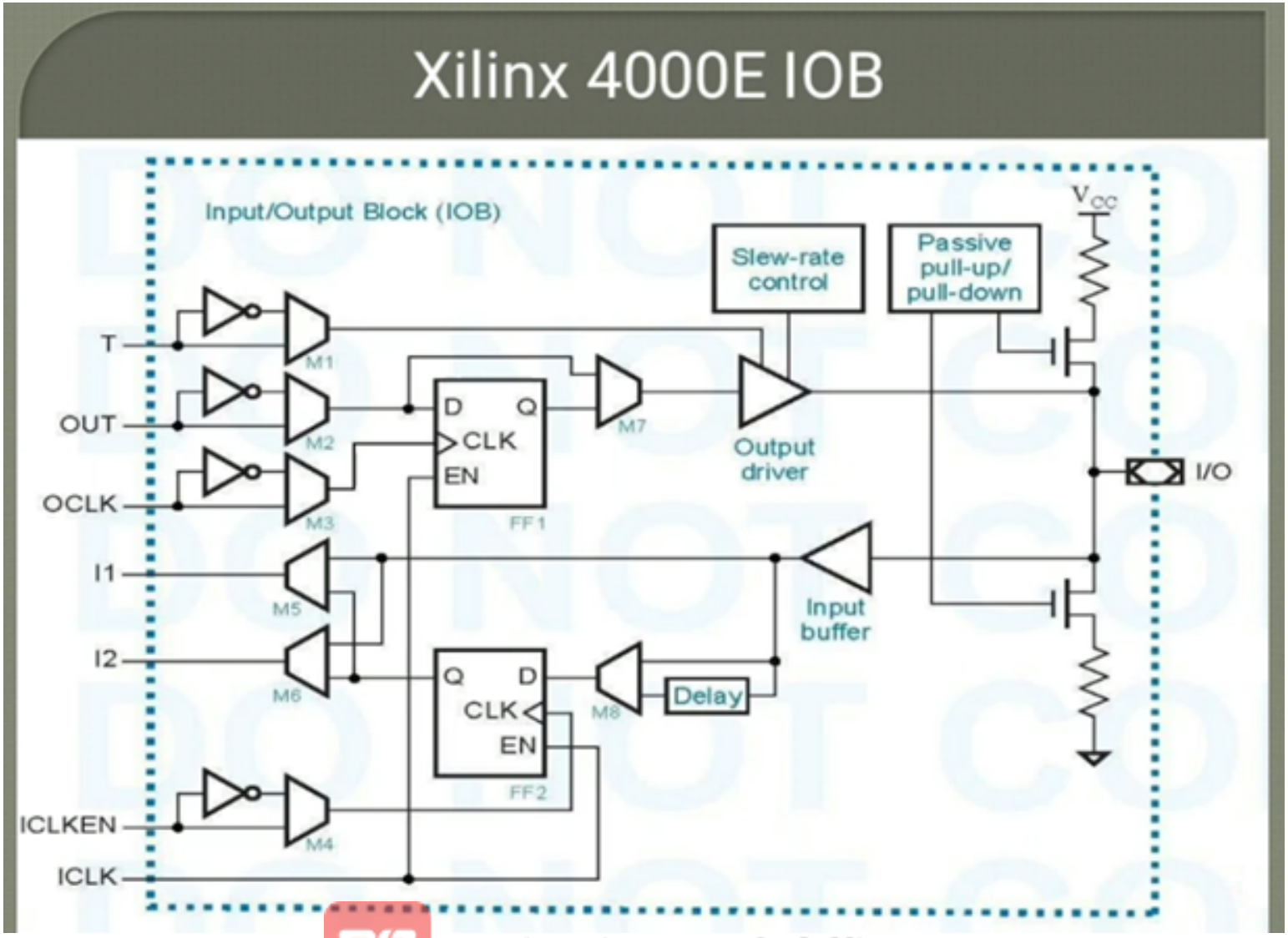
XC4000 Logic Block

- Two four-input LUTs that feed a three-input LUT
- Special fast carry logic hard-wired between CLBs
- MUX control logic maps four control inputs C1-C4 into the four inputs:
  - LUT input (H1)
  - direct in (DIN)
  - enable clock (EC)
  - set/reset control for flip-flops (S/R)
- Control inputs C1-C4 can also be used to control the use of the F’ and G’ LUTs as 32 bits of SRAM

XC4000 Family Features

- Synchronous Single and Dual-Port RAM
- Internal Three-state buffers.
- JTAG Boundary Scan
- System performance to 80 MHz
- 0.5 µ SRAM Process Technology

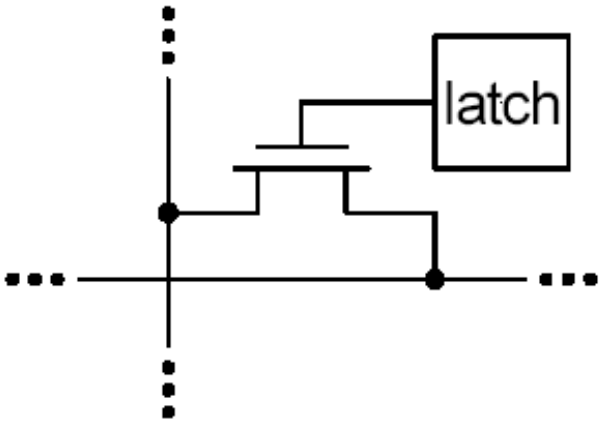
Xilinx 4000E IOB



SRAM Based Programmability

- Latches are used to:
  - make or break cross-point connections in the interconnect
  - define the function of the logic blocks
  - set user options:
    - within the logic blocks
    - in the input/output blocks
    - global reset/clock
- "Configuration bit stream" can be loaded under user control
- All latches are strung together in a shift chain

Latch-based (Xilinx, Altera, …)



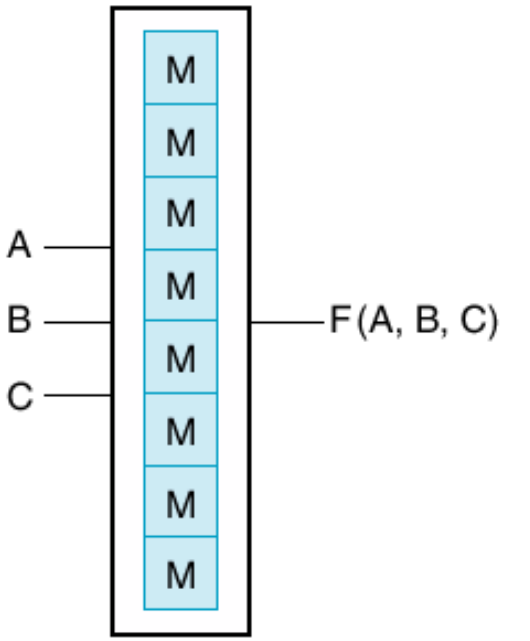
\+ reconfigurable

– volatile

– relatively large

Logic Lookup Table

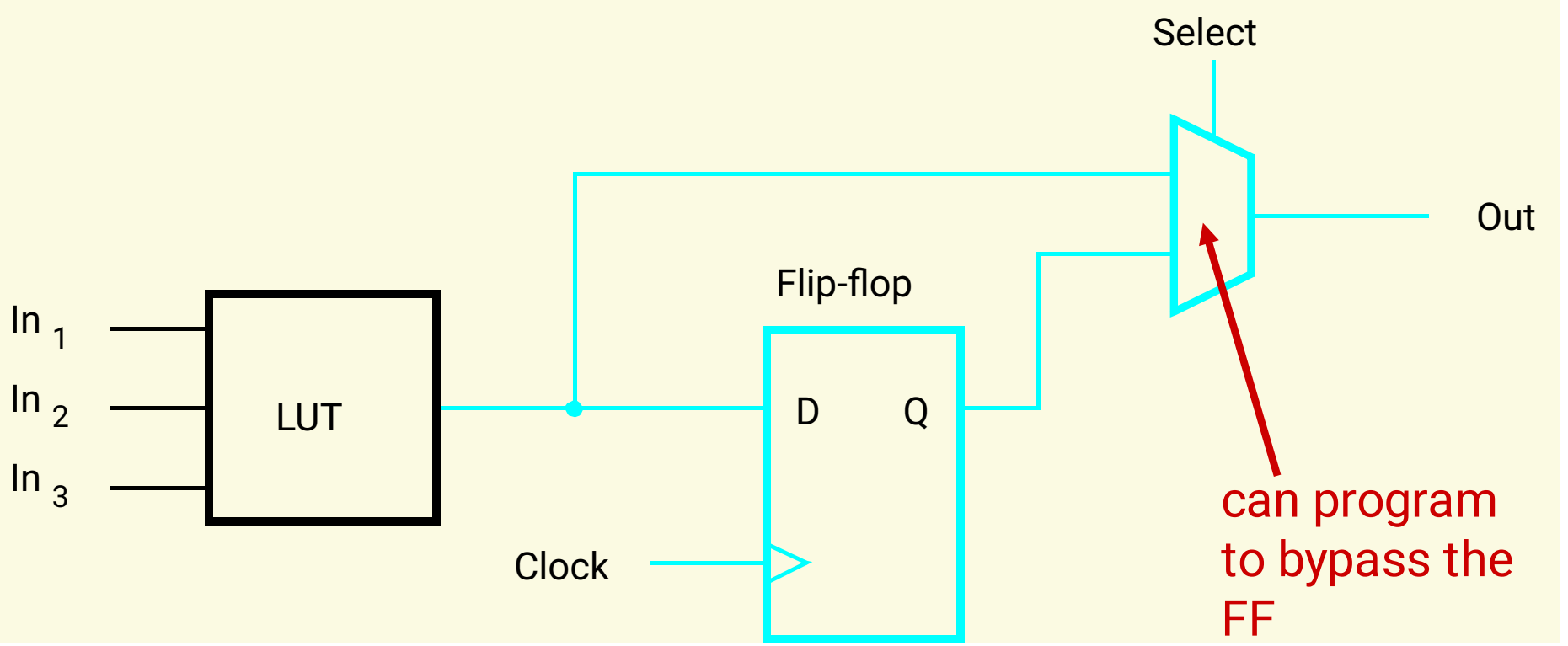
- LUT is used instead of basic gates or MUXs
- Specify logic functions to be implemented as a simple truth table
- n-input LUT can handle function of 2^n inputs
- A LUT is actually a small (1-bit) RAM
  - FPGA LUTs can be used as RAM



Look up table implementation

Inclusion of a Flip-Flop with a LUT

- A Flip-Flop can be selected for inclusion or not
- Latches the LUT output



Xilinx LUTs: Pros and Cons

- Using LUTs to implement combinational logic has both advantages and disadvantages
- Disadvantages:
  - an inverter is as slow as a five input NAND
  - routing between cells is more complex than Actel because of coarse-grain architecture
- Advantages:
  - simplifies timing
  - same delay for any function of five variables
  - can be used directly as SRAM

Field Programmability

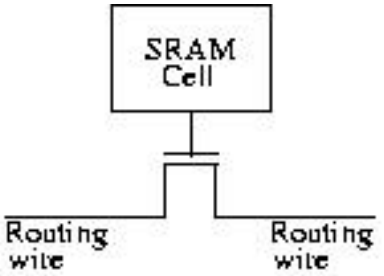
- Field programmability is achieved through switches (Transistors controlled by memory elements or fuses)
- Switches control the following aspects
  - Interconnection among wire segments
  - Configuration of logic blocks
- Distributed memory elements controlling the switches and configuration of logic blocks are together called “Configuration Memory”

Technology of Programmable Elements

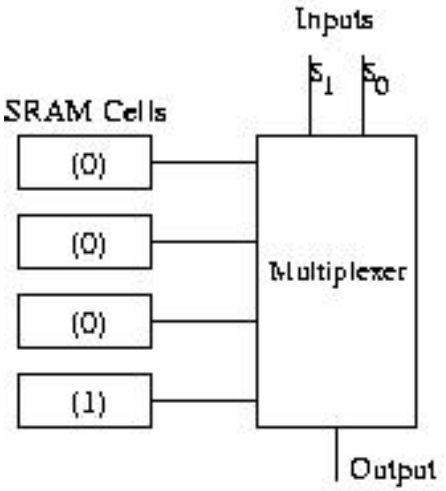
- Vary from vendor to vendor. All share the common property: Configurable in one of the two positions – 'ON' or 'OFF'
- Can be classified into three categories:
  - SRAM based
  - Fuse based
  - EPROM/EEPROM/Flash based
- Desired properties:
  - Minimum area consumption
  - Low on resistance; High off resistance
  - Low parasitic capacitance to the attached wire
  - Reliability in volume production

SRAM Programming Technology

- Employs SRAM (Static RAM) cells to control pass transistors and/or transmission gates
- SRAM cells control the configuration of logic block as well
- Volatile
  - Needs an external storage
  - Needs a power-on configuration mechanism
  - In-circuit re-programmable
- Lesser configuration time
- Occupies relatively larger area

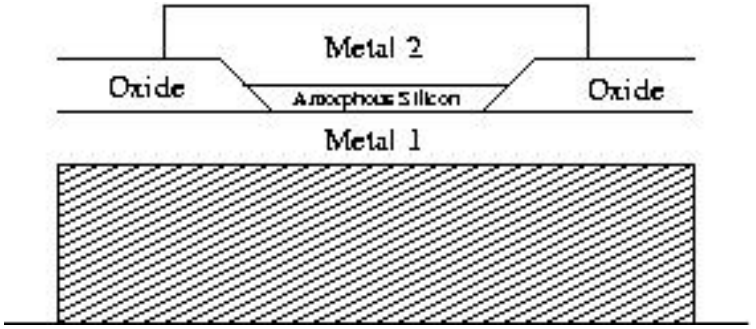


(A) pass transistor



(B) Multiplexer

Anti-fuse Programming Technology

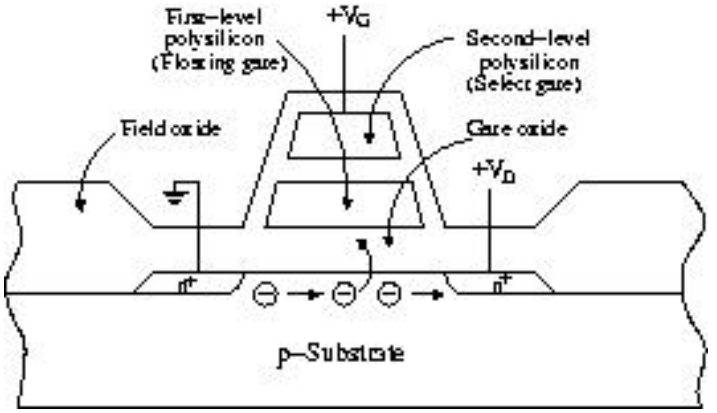


- Though implementation differ, all anti-fuse programming elements share common property
  - Uses materials which normally resides in high impedance state
  - But can be fused irreversibly into low impedance state by applying high voltage

Anti-fuse Programming Technology

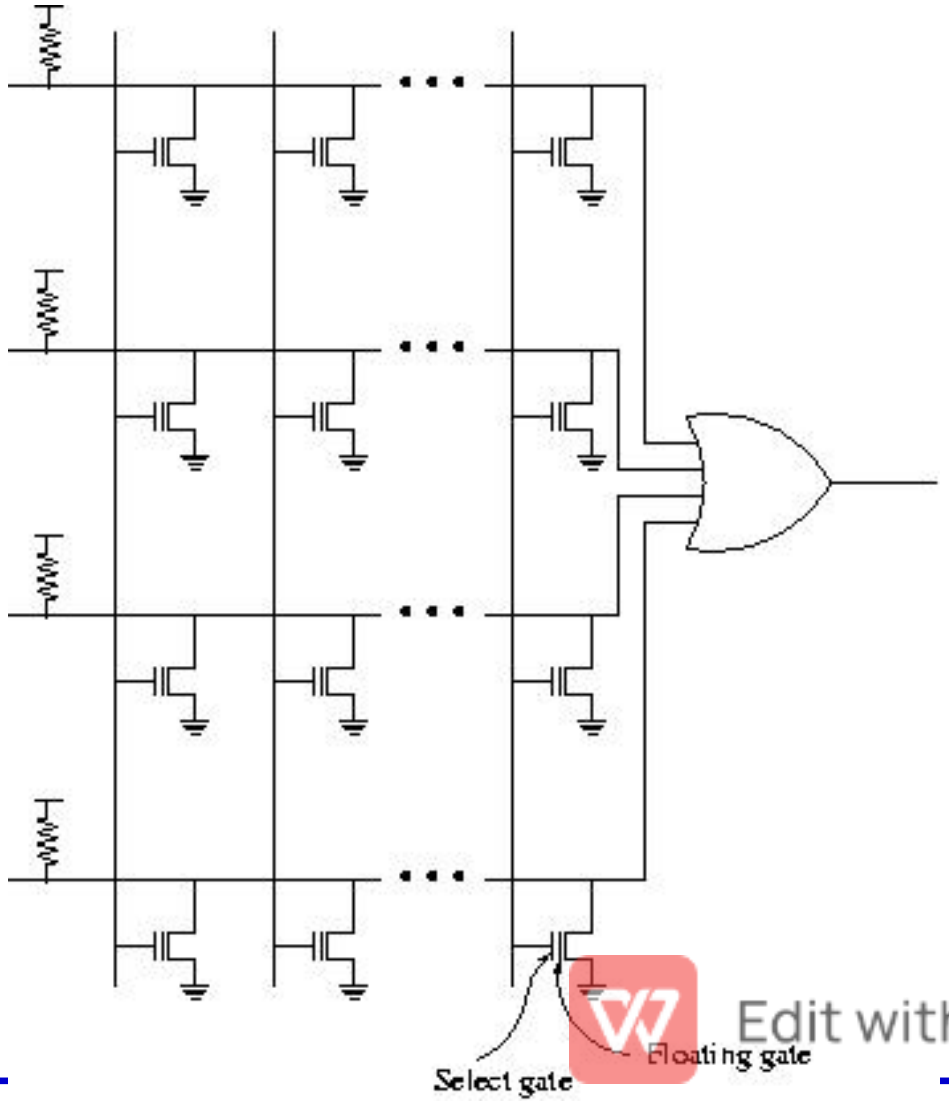
- Very low ON Resistance (Faster implementation of circuits)
- Limited size of anti-fuse elements; Interconnects occupy relatively lesser area
  - Offset : Larger transistors needed for programming
- One Time Programmable
  - Cannot be re-programmed
    - (Design changes are not possible)
  - Retain configuration after power off

EPROM, EEPROM or Flash Based Programming Technology



- EPROM Programming Technology
  - Two gates: Floating and Select
  - Normal mode:
    - No charge on floating gate
    - Transistor behaves as normal n-channel transistor
  - Floating gate charged by applying high voltage
    - Threshold of transistor (as seen by gate) increases
    - Transistor turned off permanently
  - Re-programmable by exposing to UV radiation

EPROM Programming Technology



- Used as pull-down devices
- Consumes static power

EPROM Programming Technology

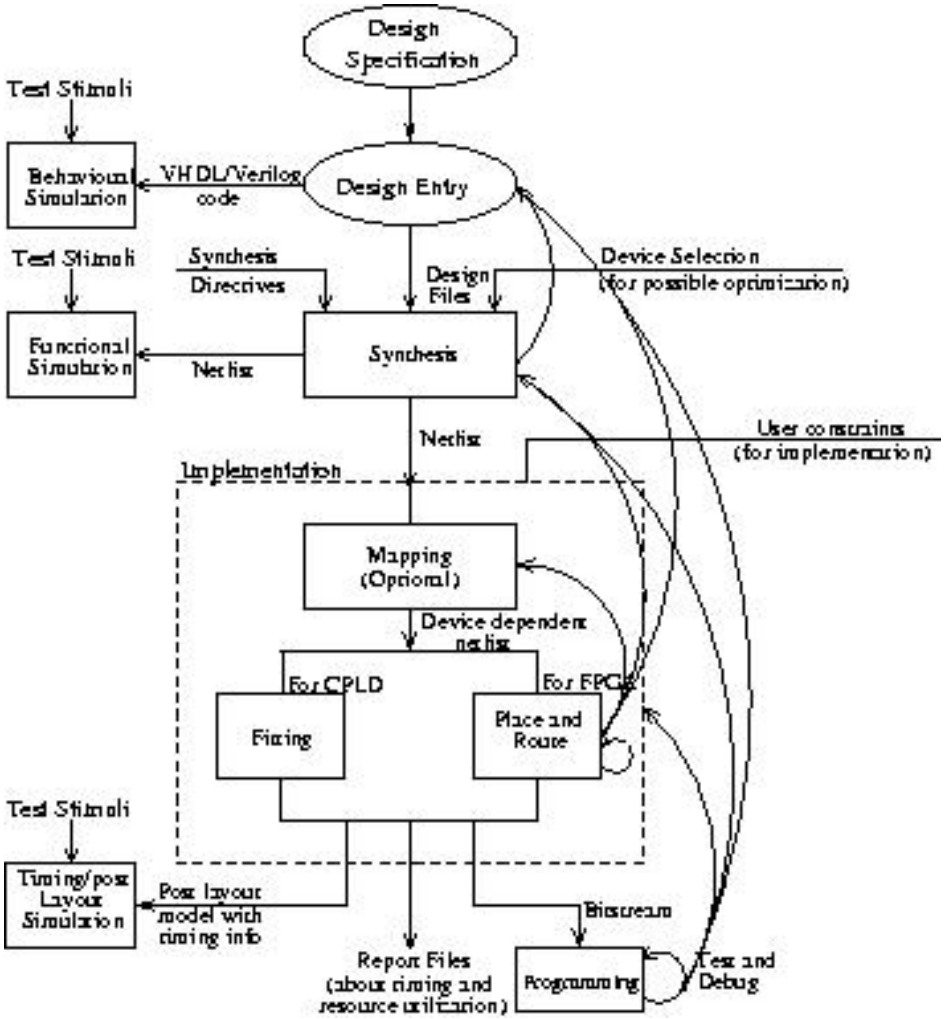
- No external storage mechanism
- Re-programmable (Not all!)
- Not in-system re-programmable
- Re-programming is a time consuming task

EEPROM Programming Technology

- Two gates: Floating and Select
- Functionally equivalent to EPROM; Construction and structure differ
- Electrically Erasable: Re-programmable by applying high voltage

  (No UV radiation expose!)
- When un-programmed, the threshold (as seen by select gate) is negative!

Design Steps Involved in Designing With FPGAs



- Understand and define design requirements
- Design description
- Behavioural simulation (Source code interpretation)
- Synthesis
- Functional or Gate level simulation
- Implementation
  - Fitting
  - Place and Route
- Timing or Post layout simulation
- Programming, Test and Debug