SRM Institute of Science and Technology
College of Engineering and Technology

SET A

DEPARTMENT OF ECE

SRM Nagar, Kattankulathur – 603203, Chengalpattu District, Tamilnadu

Academic Year: 2021-2022 (EVEN)

Test: CLAT-II **Date: 25.05.2022**
Course Code & Title: 18ECE206J Advanced Digital System Design **Duration:** 120 Min.
Year & Sem: II & IV **Max. Marks:** 50

Course Articulation Matrix:

18ECE206J / Advanced Digital System Design		Program Outcomes (POs)														
		Graduate Attributes												Program Specific Outcomes (PSO)		
S.No.	**Course Outcomes (CO):**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**1**	**2**	**3**
1	Apply advanced theorems to simplify the design aspects of various practical circuits and design Mealy and Moore models of sequential circuit.	2	-	2	-	-	-	-	-	-	-	-	-	-	-	-
2	Implement synchronous sequential circuits and write VHDL Code	-	2	2	-	-	-	-	-	-	-	-	-	-	-	-
3	Analyze asynchronous sequential circuits and write code using VHDL.	-	2	2	-	-	-	-	-	-	-	-	-	-	-	-
4	Implement Hazard free circuits and various digital circuits using Programmable Logic Devices.	-	2	2	-	-	-	-	-	-	-	-	-	-	-	-
5	Demonstrate FPGAs and Construct digital circuits using VHDL.	-	3	3	-	-	-	-	-	-	-	-	-	-	-	2
6	Design and verify the experiments in the laboratory with hardware and software.		-	-	-	3	-	-	-	2	-	-	3	3	-	2

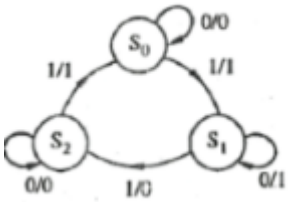
Part - A
(10 x 1 = 10 Marks)
Answer all

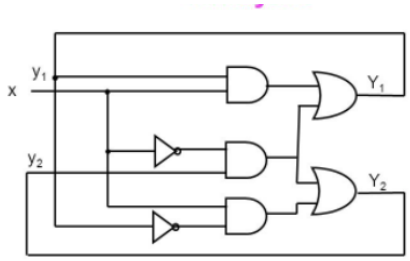
Q. No	Question	Mark	BL	CO	PO	PI Code
1	Component instantiation is done under _____ model. a). structural b). Behavioral c). Switch d). Dataflow	**1**	**1**	**2**	**2**	**2.3.1**
2	The result of the shift operation : 1001010 **srl** 2 is a). 0101000 b). 0010010 c). 1001011 d). 1111000	**1**	**2**	**2**	**3**	**3.1.1**
3	State reduction in the sequential circuit represents the reduction of a). Number of flip flops	**1**	**1**	**2**	**2**	**2.3.1**

	b). Number of OR gates c). Number of AND gates d). Number of Counters					
4	Which one of the following is not the element of the ASM Chart? a). state box b). decision box c).data box d). conditional box	**1**	**1**	**2**	**3**	**3.1.1**
5	A _____ can't be declared inside a process. a). Signal b). Variable c). Constants d). Subprograms	**1**	**1**	**2**	**2**	**2.3.1**

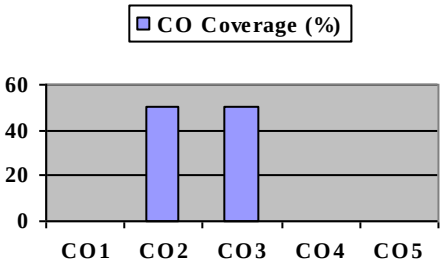
6	The following vhdl code represents
	process (A, B, S)
	begin
	if (S='1') then
	Z <= A;
	else
	Z <= B;
	end if;
	end process;
	a). 4x2 encoder
	b). 2x4 decoder
	c). 2 x1 multiplexer
	d). 1x4 demultiplexer
		1	**2**	**3**	**3**	**3.2.1**

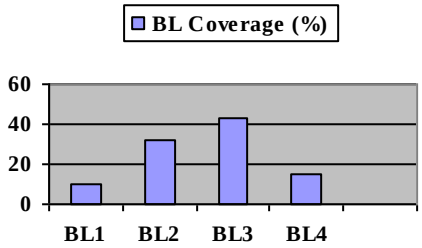
7	If the states are named by letter symbol in transition table, then it is called _____ table. a). flow b). truth c). look up d). FSM	**1**	**1**	**3**	**2**	**2.1.1**
8	If the final stable state does not depend on the change order of state variable ,then it is said to be a). critical race b). non critical race c). steady state d). hazard	**1**	**1**	**3**	**2**	**2.1.1**
9	In asynchronous sequential circuit ,the output changes occur with the change of a a). Input b). output c). clock pulse d). Time	**1**	**1**	**3**	**2**	**2.1.1**
10	Which of the following expression remove hazard from: xy+zx′ ? a). xy+zx′ b). xy+zx′+wyz c). xy+zx′+yz d). xy+zx′+wz	**1**	**2**	**3**	**3**	**3.2.1**
Section B1 (2 x 10 = 20 Marks) **Answer any two questions**						
11	i) List out sequential statement in VHDL and Explain briefly any three statement (5) ii) What is concurrent statement? Explain with one example (5)	**10**	**2**	**2**	**2**	**2.3.1**
12	i) convert the given state diagram into ASM chart (5)	**10**	**3**	**2**	**3**	**3.2.1**

<table>
<tr><td></td><td> 

ii)List out different data types in VHDL.Compare signal and variable (5)</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>13</td><td>i)Reduce the given state table using Implication chart (8)
<table>
<tr><th>Present state</th><th colspan="2">Next state</th><th>output</th></tr>
<tr><th></th><th>X=0</th><th>X=1</th><th></th></tr>
<tr><td>a</td><td>e</td><td>e</td><td>1</td></tr>
<tr><td>b</td><td>c</td><td>e</td><td>1</td></tr>
<tr><td>c</td><td>i</td><td>h</td><td>0</td></tr>
<tr><td>d</td><td>h</td><td>a</td><td>1</td></tr>
<tr><td>e</td><td>i</td><td>f</td><td>0</td></tr>
<tr><td>f</td><td>e</td><td>g</td><td>0</td></tr>
<tr><td>g</td><td>h</td><td>b</td><td>1</td></tr>
<tr><td>h</td><td>c</td><td>d</td><td>0</td></tr>
<tr><td>i</td><td>f</td><td>b</td><td>1</td></tr>
</table>
ii)Write about State assignment and its type (2)</td><td>10</td><td>2</td><td>2</td><td>3</td><td>3.1.1</td></tr>
<tr><td colspan="7">Section B2 (2 x 10 = 20 Marks)
Answer any two questions</td></tr>
<tr><td>14</td><td>i) Write about Race condition and its type in asynchronous sequential circuit with example (5)
ii) analyze the following asynchronous sequential circuit (5)
 
</td><td>10</td><td>3</td><td>3</td><td>3</td><td>3.2.1</td></tr>
<tr><td>15</td><td>Design a asynchronous sequential circuit in gated latch with inputs X and Y ,output Whenever Y is 1 input X is transferred to output when Y is 0 output remains in the same state even if X is change its value.</td><td>10</td><td>4</td><td>3</td><td>3</td><td>3.2.1</td></tr>
<tr><td>16</td><td>Write a VHDL code for a Full adder design using two half adder circuit.</td><td>10</td><td>3</td><td>3</td><td>3</td><td>3.2.1</td></tr>
</table>

Course Outcome (CO) and Bloom's level (BL) Coverage in Questions





Evaluation Sheet

Name of the Student:
Register No.:

Part- A (10x 1= 10 Marks)				
Q. No	**CO**	**PO**	**Marks Obtained**	**Total**
1	2	2		
2	2	3		
3	2	2		
4	2	3		
5	2	2		
6	3	3		
7	3	2		
8	3	3		
9	3	3		
10	3	3		
Part -B				
Section -B1 (2 x 10= 20 Marks)				
11	2	2		
12	2	3		
13	2	3		
Section -B2 (2 x 10= 20 Marks)				
14	3	3		
15	3	3		
16	3	3		

Consolidated Marks:

	Marks Scored
CO2	
CO3	
PO2	
PO3	
Total	

Signature of the Course Teacher