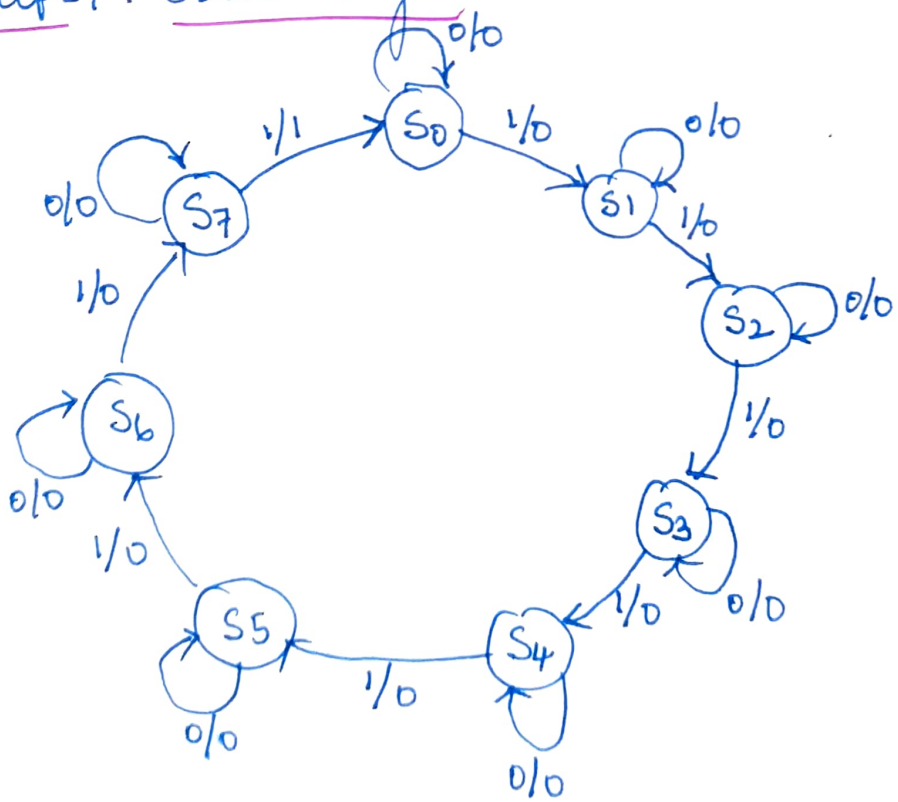
Design of a 3-bit Gray code counter using Sequential PAL

Problem Statement:

The counter is to be designed with one i/p terminal (which receives pulse signals) and one o/p terminal. It counts in the Gray system up to 7 and produces an o/p pulse for every 8 i/p pulses. After the count 7 is reached, the next pulse will reset the counter to its initial state, ie., to a count of zero.

Step-1 : State diagram



Step-2 : State Table

PS	NS		O/P, Z	
	$x=0$	$x=1$	$x=0$	$x=1$
S_0	S_0	S_1	0	0
S_1	S_1	S_2	0	0
S_2	S_2	S_3	0	0
S_3	S_3	S_4	0	0
S_4	S_4	S_5	0	0
S_5	S_5	S_6	0	0
S_6	S_6	S_7	0	0
S_7	S_7	S_0	0	1

Step-3

State Assignment

S_0	000
S_1	001
S_2	011
S_3	010
S_4	110
S_5	111
S_6	101
S_7	100

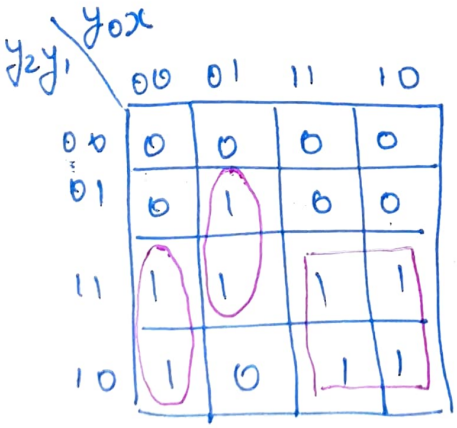
Step-4 : Transition Table

PS	I/P	NS	O/P
$y_2\ y_1\ y_0$	x	$Y_2\ Y_1\ Y_0$	Z
S_0	0	S_0	0
S_0	1	S_1	0
S_1	0	S_1	0
S_1	1	S_2	0
S_2	0	S_2	0
S_2	1	S_3	0
S_3	0	S_3	0
S_3	1	S_4	0
S_4	0	S_4	0
S_4	1	S_5	0
S_5	0	S_5	0
S_5	1	S_6	0
S_6	0	S_6	0
S_6	1	S_7	0
S_7	0	S_7	0
S_7	1	S_0	1

Step-5: Excitation Table

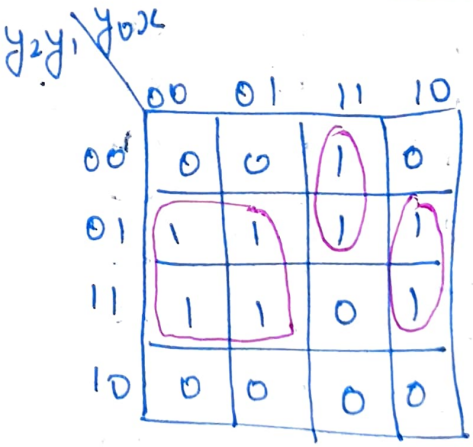
PS	I/P	NS	FF i/PS	O/P
$y_2\ y_1\ y_0$	x	$Y_2\ Y_1\ Y_0$	$D_2\ D_1\ D_0$	Z
0 0 0	0	0 0 0	0 0 0	0
0 0 0	1	0 0 1	0 0 1	0
0 0 1	0	0 0 1	0 0 1	0
0 0 1	1	0 1 1	0 1 1	0
0 1 0	0	0 1 0	0 1 0	0
0 1 0	1	1 1 0	1 1 0	0
0 1 1	0	0 1 1	0 1 1	0
0 1 1	1	0 1 0	0 1 0	0
1 0 0	0	1 0 0	1 0 0	0
1 0 0	1	0 0 0	0 0 0	1
1 0 1	0	1 0 1	1 0 1	0
1 0 1	1	1 0 0	1 0 0	0
1 1 0	0	1 1 0	1 1 0	0
1 1 0	1	1 1 1	1 1 1	0
1 1 1	0	1 1 1	1 1 1	0
1 1 1	1	1 0 1	1 0 1	0

Step-7: K-Maps and minimal expressions



~~$D_2 = \bar{y}_0\bar{x} + y_1$~~

$D_2 = y_2\bar{y}_0\bar{x} + y_1\bar{y}_0x + y_2y_0$



$D_1 = y_1\bar{y}_0 + \bar{y}_2y_0x + y_1y_0\bar{x}$

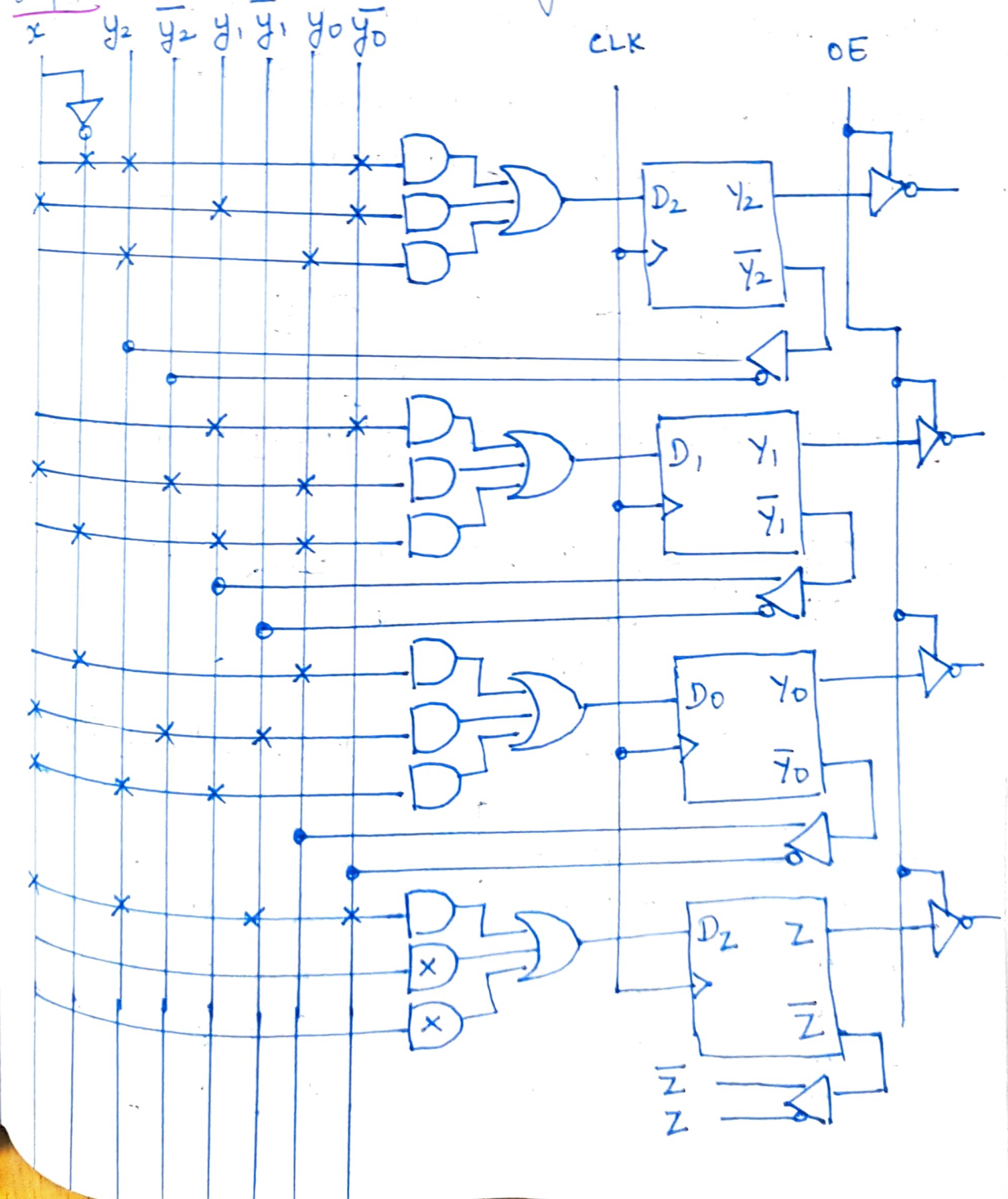
y_2y_1 \ y_0x	00	01	11	10
00	0	1	1	1
01	0	0	0	1
11	0	1	1	1
10	0	0	0	1

$$D_0 = y_0\bar{x} + \bar{y}_2\bar{y}_1x + y_2y_1x$$

y_2y_1 \ y_0x	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	0	0	0	0
10	0	1	0	0

$$Z = y_2\bar{y}_1\bar{y}_0x$$

Step-8: Implementation using Sequential PAL



Design of Sequence detector using Sequential PAL

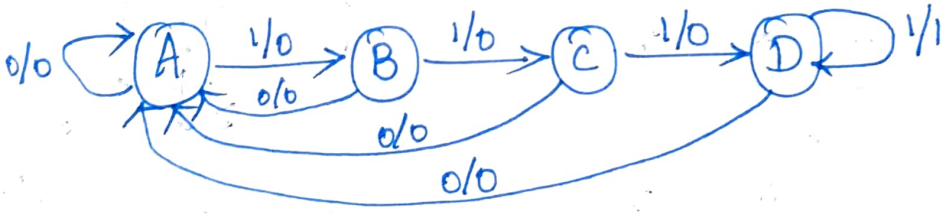
Problem Statement

A long sequence of pulses enters a synchronous sequential circuit which is required to produce an output Z = 1, whenever the sequence 1111 occurs. overlapping sequences are accepted. For example,

if the input is ⟶ 01011111

the required o/p is ⟶ 00000011

Step-1 : State diagram for sequence (1111) detector



Step-2 : State Table

PS	NS		o/p, Z	
	x=0	x=1	x=0	x=1
A	A	B	0	0
B	A	C	0	0
C	A	D	0	0
D	A	D	0	1

Step-3 : State Assignment

A	00
B	01
C	10
D	11

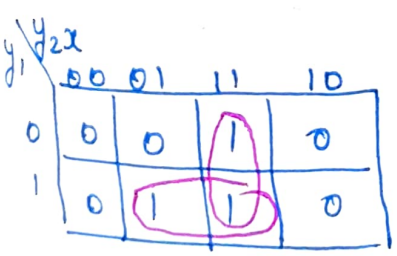
Step-4: Transition Table

PS		NS ($Y_1 Y_2$)		o/p (z)	
y_1	y_2	x = 0	x = 1	x = 0	x = 1
0	0	0 0	0 1	0	0
0	1	0 0	1 0	0	0
1	0	0 0	1 1	0	0
1	1	0 0	1 1	0	1

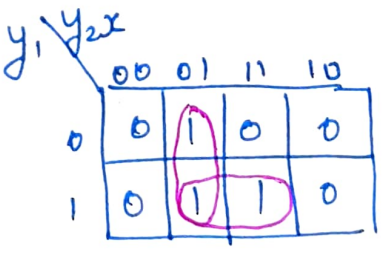
Excitation Table - Step 5

PS		I/p	NS		FF i/ps		o/p
y_1	y_2	x	Y_1	Y_2	D_1	D_2	Z
0	0	0	0	0	0	0	0
0	0	1	0	1	0	1	0
0	1	0	0	0	0	0	0
0	1	1	1	0	1	0	0
1	0	0	0	0	0	0	0
1	0	1	1	1	1	1	0
1	1	0	0	0	0	0	0
1	1	1	1	1	1	1	1

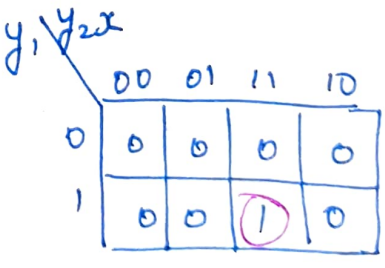
Step-6: K-Maps



$D_1 = y_2x + y_1x$



$D_2 = \overline{y_2}x + y_1x$



$Z = y_1y_2x$

Step-7: Logic diagram