Reg. No.	R	A	2	0	1	1	0	0	4	0	1	0	0	S	1

B.Tech. DEGREE EXAMINATION, DECEMBER 2022

Fifth Semester

18ECC203J – MICROPROCESSOR, MICROCONTROLLER AND INTERFACING TECHNIQUES

(For the candidates admitted from the academic year 2020-2021 to 2021-2022)

Note:

(i) **Part - A** should be answered in OMR sheet within first 40 minutes and OMR sheet should be handed over to hall invigilator at the end of 40th minute.

(ii) **Part - B** should be answered in answer booklet.

Time: 2½ Hours

Max. Marks: 75

PART – A (25 × 1 = 25 Marks)

Answer **ALL** Questions

	Marks	BL	CO	PO
1. The BIU contains FIFO register of size _____ bytes. (A) 4 (B) 6 (C) 8 (D) 12	1	1	1	2
2. What is the range of 10 addressing in 8086? (A) 256 bytes (00_H to FF_H) (B) 4kB(000_H to FFF_H) (C) 64 kB(0000_H to $FFFF_H$) (D) 1MB(00000_H to $FFFFF_H$)	1	1	1	2
3. Which signal is used to demultiplex address and data? (A) ALE (B) $MN / \overline{MX}$ (C) $M / \overline{IO}$ (D) $\overline{RD}$	1	2	1	2
4. When $\overline{s}_2 = 0$, $\overline{s}_1 = 0$ and $\overline{s}_0 = 1$ the processor is in _____ state. (A) Halt (B) Code access (C) Read I/0 port (D) Real memory	1	2	1	2
5. Calculate the physical address when the register values are $CS = 5000$ and $IP = 1020$. (A) 06020 (B) 05000 (C) 51020 (D) 01020	1	2	1	2
6. The 8086 instruction used to perform 2's complement is (A) AND (B) OR (C) NOT (D) NEG	1	1	2	2
7. _____ instruction stores the content of a register on to the stack. (A) MOV (B) PUSH (C) POP (D) XCHG	1	1	2	2
8. _____ instruction affects all condition code flags except the carry flag. (A) ADD (B) SUB (C) ADC (D) INC	1	1	2	2

9. Type 1 interrupt is reserved for _____ 1 1 2 2
   (A) Zero interrupt (B) Single step interrupt
   (C) NMI (D) Single byte instruction

10. The POP instruction will _____the _____SP value by _____ 1 1 2 2
   (A) Increment, 1 (B) Increment, 2
   (C) Decrement, 1 (D) Decrement, 2

11. Calculate the control word register format for 8255 when PORT A is input and PORT B is output in mode '0'. PORT C is not used. 1 2 3 2
   (A) 80 H (B) 90 H
   (C) AOH (D) BOH

12. Which device facilitates the generation of accurate time delay? 1 1 3 2
   (A) 8253 (B) 8255
   (C) 8251 (D) 8237

13. _____stores all the interrupt requests inorder to serve them in 8259A programmable interrupt controller. 1 1 3 2
   (A) Interrupt Request Register (IRR) (B) In-Service Register (ISR)
   (C) Interrupt Mask Register (IMR) (D) Priority resolver

14. "Transmit buffer" of 8251 is a _____shift register. 1 1 3 2
   (A) PIPO (B) PISO
   (C) SIPO (D) SISO

15. To select counter 1 in 8253 the SC_1 AND SC_0 have to be loaded with 1 1 3 2
   (A) 00 (B) 01
   (C) 10 (D) 11

16. _____register have to be used to address a data stored in a 16 bits address location. 1 1 4 2
   (A) Accumulator (B) Stack pointer
   (C) Instruction pointer (D) DPTR

17. MOV $A,@R_1$ will 1 1 4 2
   (A) Copy R_1 to accumulator (B) Copy accumulator to R_1
   (C) Copy the content of memory where address is in R_1 to the accumulator (D) Copy the accumulator content to memory pointed by R_1

18. MOV A,@A+DPTR uses 1 2 4 2
   (A) Immediate addressing mode (B) Direct addressing mode
   (C) Indirect addressing mode (D) Indexed addressing mode

19. _____instruction is an example for direct addressing mode. 1 2 4 2
   (A) MOV A, @ R_0 (B) MOV A, R_2
   (C) MOV A, 70 H (D) MOV A, #06H

20.	_____ of internal RAM are bit addressable memory.		1	1	4	2
	(A) 32 bits	(B) 64 bits				
	(C) 128 bits	(D) 16 bits				
21.	The standard frequency of the crystal for serial communication is		1	1	5	2
	(A) 11.0592 MHz	(B) 11.0592 KHz				
	(C) 11.0952 MHz	(D) 11.0952 kHz				
22.	Serial port interrupt is generated if _____ bits are set		1	1	5	2
	(A) T_1, R_1	(B) IE, TF_0				
	(C) TF_0, TF_1	(D) IE, TF_1				
23.	To configure all pins in a parallel port of 8051 as input pins _____ must be sent to the port.		1	2	5	2
	(A) 00H	(B) 55H				
	(C) AAH	(D) FFH				
24.	Which interrupt has highest priority in 8051?		1	1	5	2
	(A) TF_0	(B) TF_1				
	(C) INT_0	(D) INT_1				
25.	The alternate function of PORT 2 is _____		1	1	5	2
	(A) Multiplexed address/data	(B) Higher byte of address				
	(C) Control signals	(D) Lower byte of address				

PART – B (5 × 10 = 50 Marks)

Answer **ALL** Questions

		Marks	BL	CO	PO
26. a.	With neat diagram explain the architecture of 8085 microprocessor.	10	2	1	2
	(OR)				
b.	Describe the functional blocks of minimum mode system using 8086 microprocessor with read cycle timing diagram and block diagram.	10	3	1	2
27. a.	With suitable examples, explain any five addressing modes for sequential control how instructions in 8086 microprocessor.	10	3	2	2
	(OR)				
b.	Write an ALP for 8086 to perform sorting 'n' numbers in ascending order with neat flowchart.	10	4	2	2
28. a.	Design an interface between 8086 CPU and two chips of 16 K × 8 EPROM and two chips of 32 K × 8 RAM. Select the starting address of EPROM suitably. The RAM address must start at 00000H.	10	4	3	3
	(OR)				
b.	Explain the architecture of 8257 (DMA) with neat diagram.	10	3	3	3

29. a. Explain the interrupts in 8051 with the registers used to control the interrupts. Draw and explain the register bit formats. 10 3 4 2

(OR)

b. Write an ALP program to store the result of the equation $Y = 3x^2 + 4x + 5$ in an array for $x = 1$ through 5. 10 4 4 2

30. a. Write an assembly level program (ALP) for 8051, to generate a square wave with an ON time of 3 ms and OFF time of 7 ms on port 3 pin 4. Assume an XTAL of 11.0592 MHz. 10 4 5 3

(OR)

b. Explain with necessary diagram to interface 8051 microcontroller with an ADC. 10 3 5 3

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