SRM Institute of Science and Technology
College of Engineering and Technology
DEPARTMENT OF ECE
SRM Nagar, Kattankulathur – 603203, Chengalpattu District, Tamilnadu

Mode of Exam
OFFLINE
SET- B

Academic Year: 2021-2022 (EVEN)-Answer Key

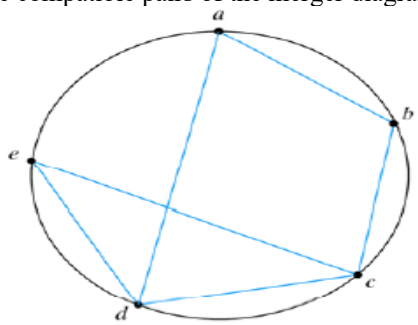
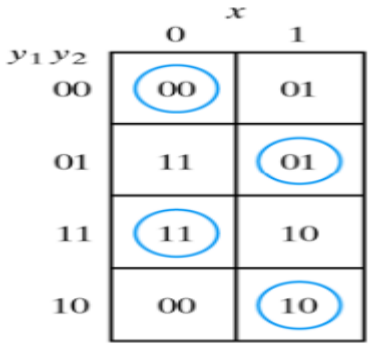
Test: CLAT-2 | **Date: 25.05.2022**
Course Code & Title: 18ECE206J Advanced Digital System Design | **Duration:** 1 Hour 40 Minutes
Year & Sem: II & IV | **Max. Marks:** 50

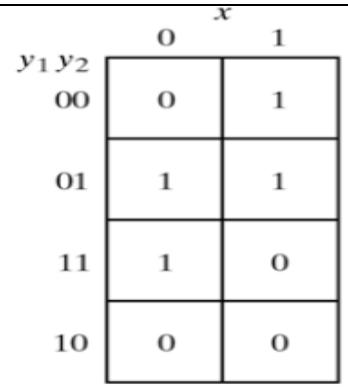
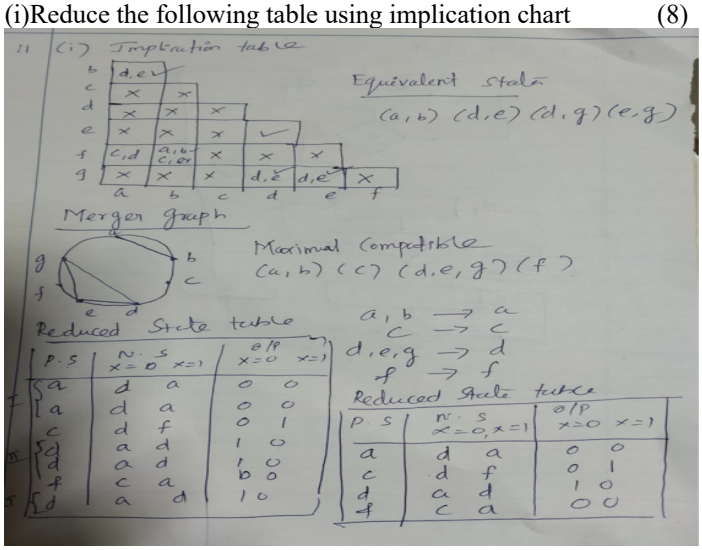
Course Articulation Matrix:

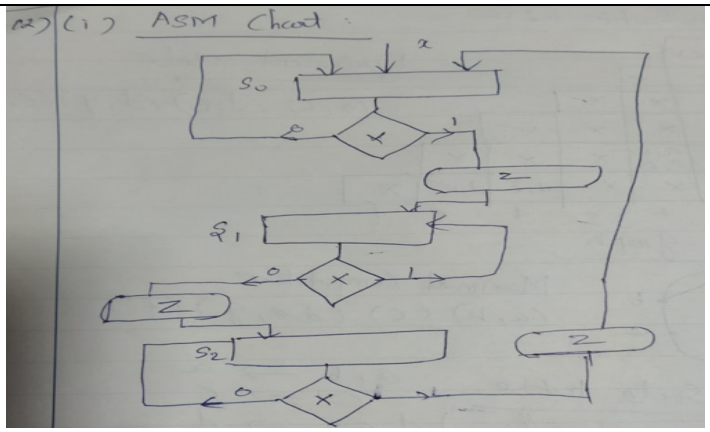
18ECE206J / Advanced Digital System Design		Program Outcomes (POs)														
		Graduate Attributes												Program Specific Outcomes (PSO)		
S.No.	**Course Outcomes (CO):**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**1**	**2**	**3**
1	Apply advanced theorems to simplify the design aspects of various practical circuits and design Mealy and Moore models of sequential circuit.	2	-	2	-	-	-	-	-	-	-	-	-	-	-	-
2	Implement synchronous sequential circuits and write VHDL Code	-	2	2	-	-	-	-	-	-	-	-	-	-	-	-
3	Analyze asynchronous sequential circuits and write code using VHDL.	-	2	2	-	-	-	-	-	-	-	-	-	-	-	-
4	Implement Hazard free circuits and various digital circuits using Programmable Logic Devices.	-	2	2	-	-	-	-	-	-	-	-	-	-	-	-
5	Demonstrate FPGAs and Construct digital circuits using VHDL.	-	3	3	-	-	-	-	-	-	-	-	-	-	-	2
6	Design and verify the experiments in the laboratory with hardware and software.		-	-	-	3	-	-	-	2	-	-	3	3	-	2

Part - A
(10 x 1 = 10 Marks)
Instructions: Answer all Questions

Q. No	Question	Marks	BL	CO	PO	PI Code
1	A signal cannot be declared inside a_____ **(a) Process** (b) Sequential (c) Concurrent (d) Wait	**1**	**1**	**2**	**2**	**2.3.1**
2	State reduction in the sequential circuit represents the reduction of (a) **Number of flip flops** (b) Number of OR gates (c) Number of AND gates (d) Number of Counters	**1**	**1**	**2**	**2**	**2.3.1**
3	Which of the following is not a Data type? (a) std_logic_vector (b) bit_vector (c) **std_bit_logic**	**1**	**1**	**2**	**2**	**2.3.1**

	(d) bit					
4	The result of the shift operation: 1001010 srl3 is (a) 0001001 (b) 0010010 (c) 1001011 (d) 1111000	**1**	**1**	**2**	**2**	**2.3.1**
5	what is wrong in the following VHDL code entity 2and is port (A, B: in BIT; Y: out BIT); end 2and; (a) port list (b) **entity name** (c) end (d)entity	**1**	**1**	**2**	**3**	**3.1.1**
6	___------- flow table has only one stable state in each row. (a) **Primitive** (b) Non-primitive (c) transition (d) FSM	**1**	**1**	**3**	**2**	**2.1.1**
7	The logic circuit causes the output to go to 0, When it should remain at 1, which produce (a) Static 0 hazard (b) Static 1 hazard (c) Dynamic hazard (d) Essential hazard	**1**	**1**	**3**	**2**	**2.1.1**
8	The compatible pairs of the merger diagram are  (a) (a,b)(b,c)(c,e)(c,d)(d,e) (b) (a,b)(b,c)(a,d)(c,e)(c,d) (c) (a,b)(b,c)(d,e) (d) **(a,b)(b,c)(a,d)(c,e)(c,d)(d,e)**	**1**	**2**	**3**	**3**	**3.2.1**
9	The total stable states in the given flow table are  (a) 001,110,101,111 **(b) 000, 011,110,101** (c) 000,111,001,101 (d) 001,010,111,100	**1**	**2**	**3**	**3**	**3.2.1**
10	Next state equation of the given transition table is	**1**	**2**	**3**	**3**	**3.2.1**

	 (a) $xy_2 + xy_1'$ (b) $x'y_2 + xy_1$ (c) $x'y_2 + x'y_1'$ **(d)** $x'y_2 + xy_1'$					
Section- B1 (2 X 10 Marks = 20 Marks) Instructions: Answer Any Two Questions						
11	(i)Reduce the following table using implication chart (8)  (ii) Write about state assignment and its types. (2) • In order to design a sequential circuit with physical components, it is necessary to assign unique coded binary values to the states. *Three Possible Binary State Assignments* **State** / **Assignment 1, Binary** / **Assignment 2, Gray Code** / **Assignment 3, One-Hot** *a* 000 000 00001 *b* 001 001 00010 *c* 010 011 00100 *d* 011 010 01000 *e* 100 110 10000	**10 (8+2)**	**2**	**2**	**3**	**3.1.1**
12	Draw the ASM for the given state diagram	**5**	**3**	**2**	**3**	**3.1.1**

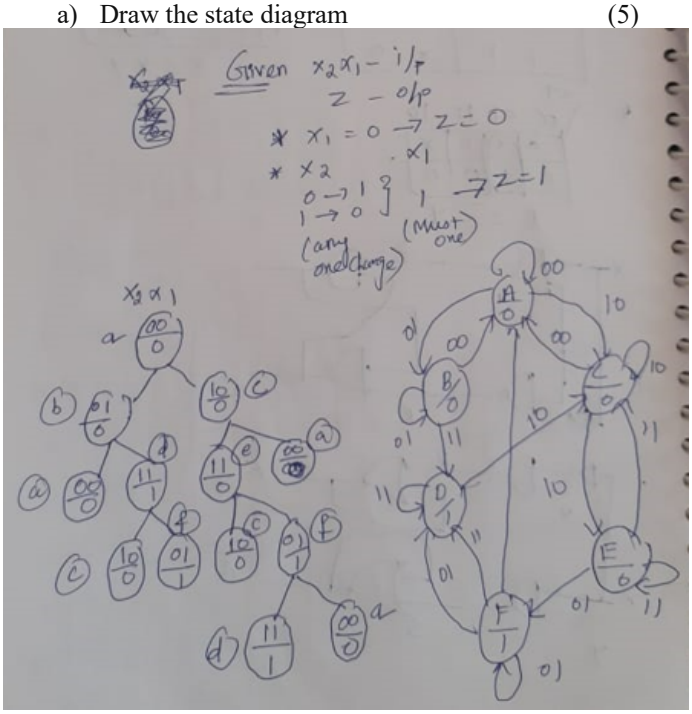
	 (ii) Explain Scalar data type in VHDL with example (5) • Integer • Minimum range for any implementation as defined by standard: -2,147,483,647 to 2,147,483,647 • Integer assignment example • Real • Minimum range for any implementation as defined by standard: -1.0E38 to 1.0E38 • Real assignment example • Enumerated • User defined range • Enumerated example • Physical • Can be user defined range • Physical type example	**5**	**2**	**2**	**3**	**3.1.1**
13	(i) Explain the VHDL operators with example? Logical Operators: and, or, not, nand, nor, xor, xnor Relational Operators: = , /=, <, <=, >, >= Shift Operators: sll, srl, sla, sra, rol,ror	**5**	**2**	**2**	**2**	**2.3.1**

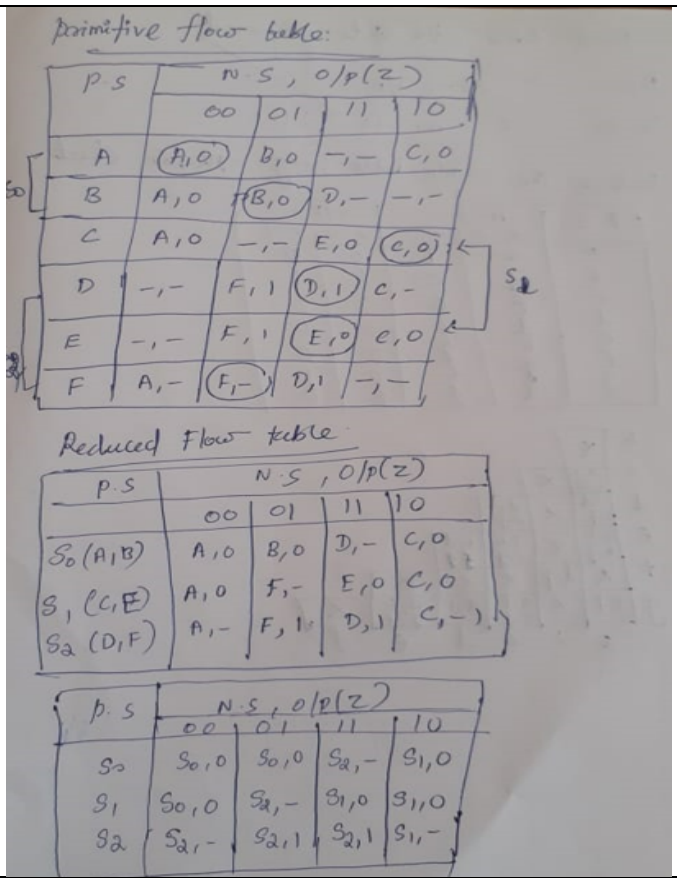
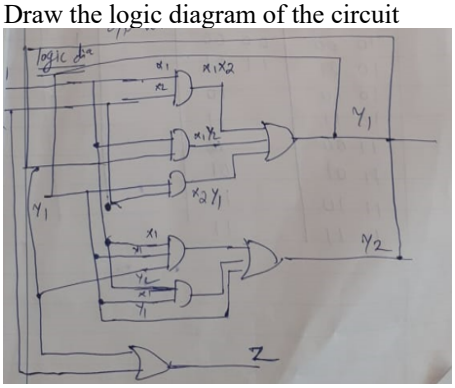
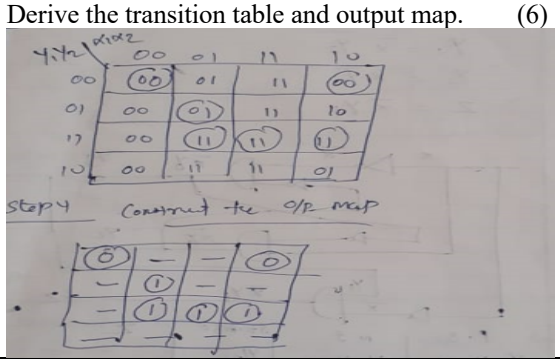
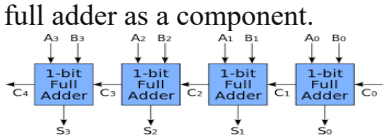
```
ARCHITECTURE test_int OF test IS
BEGIN
    PROCESS (X)
      VARIABLE a: INTEGER;
    BEGIN
      a := 1;  -- OK
      a := -1;  -- OK
      a := 1.0;  -- bad
    END PROCESS;
END TEST;
```

```
ARCHITECTURE test_real OF test IS
BEGIN
    PROCESS (X)
      VARIABLE a: REAL;
    BEGIN
      a := 1.3;  -- OK
      a := -7.5;  -- OK
      a := 1;  -- bad
      a := 1.7E13;  --OK
      a := 5.3 ns;  -- bad
    END PROCESS;
END TEST;
```

```
TYPE binary IS ( ON, OFF );
... some statements ...
ARCHITECTURE test_enum OF test IS
BEGIN
    PROCESS (X)
      VARIABLE a: binary;
    BEGIN
      a := ON;  -- OK
      ... more statements ...
      a := off;  -- OK
      ... more statements ...
    END PROCESS;
END TEST;
```

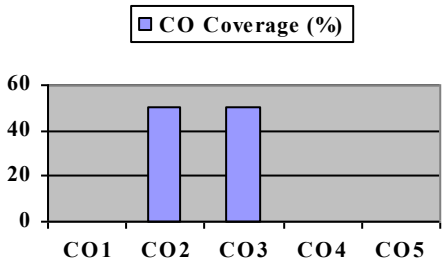
```
TYPE resistance IS RANGE 0 to 1000000

UNITS
    ohm;  -- ohm
    Kohm = 1000 ohm;  -- 1 KΩ
    Mohm = 1000 kohm;  -- 1 MΩ
END UNITS;
```

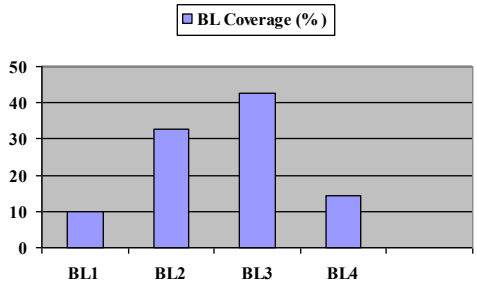
	Adding Operators: +, - , & Multiplying Operators: *, /, mod, rem (ii) Write a VHDL program for 4 X1 MUX using 'Case' statement 1 library ieee ; 2 use ieee.std_logic_1164.all ; 3 entity mux_case is 4 port(I:in std_logic_vector(0 to 3); 5 s:in std_logic_vector(1 downto 0); 6 y:out std_logic); 7 end mux_case; 8 architecture muxx of mux_case is 9 begin 10 process(I) 11 variable x:std_logic; 12 begin 13 case s is 14 when "00"=>x:=I(0); 15 when "01"=>x:=I(1); 16 when "10"=>x:=I(2); 17 when others=>x:=I(3); 18 --when others=> y<="----"; 19 end case; 20 y<=x; 21 end process; 22 end muxx;	**5**	**3**	**2**	**2**	**2.3.1**
	Section- B2 **(2 X 10 Marks = 20 Marks)** **Instructions: Answer Any Two Questions**					
14	a) Draw the state diagram (5)  b) Construct the primitive flow table (3) c) Derive the reduced flow table (2)	**10** **(5+3+2)**	**4**	**3**	**3**	**3.2.1**

	Primitive flow table: Reduced Flow table 					
15	a) Draw the logic diagram of the circuit (4)  b) Derive the transition table and output map. (6) 	**10 (4+6)**	**3**	**3**	**3**	**3.2.1**
16	Write a VHDL Program to add two four-bit numbers, use full adder as a component.  Block diagram ----1 Mark Full adder program ---2 Marks RCA program ---7 Marks	**10**	**3**	**3**	**3**	**3.2.1**

	Library ieee;
	Use ieee.std_l ogic_1164.all;
	Entity ripple_str is
	port(A:in std_logic_vector(3 downto 0);
	B:in std_logic_vector(3 downto 0);
	Cin:in std_logic;
	sum:out std_logic_vector(3 downto 0);
	Cout:out std_logic);
	End ripple_str;
	Architecture ripple_str_fa of ripple_str is
	Signal Cint:std_logic_vector(1 to 3);
	Component fa
	port(x,y,z:in std_logic; s,c:out std_logic);
	End component;
	Begin
	rip1:fa port map(A(0),B(0),Cin,sum(0),Cint(1));
	rip2:fa port map(A(1),B(1),Cint(1),sum(1),Cint(2));
	rip1:fa port map(A(2),B(2),Cint(2),sum(2),Cint(2));
	rip1:fa port map(A(3),B(3),Cint(3),sum(3),Cout);
	End ripple_str_fa;					

Course Outcome (CO) and Bloom's level (BL) Coverage in Questions





Evaluation Sheet

Name of the Student:

Register No:

Part- A (10x 1= 10 Marks)				
Q. No	**CO**	**PO**	**Marks Obtained**	**Total**
1	2	2		
2	2	2		
3	2	2		
4	2	2		
5	2	3		
6	3	2		
7	3	2		
8	3	3		
9	3	3		
10	3	3		
Part -B				
Section -B1 (2 x 10= 20 Marks)				
11	2	3		
12(i)	2	3		
12(ii)	2	3		
13(i)	2	2		

13(ii)	2	2		
Section -B2 (2 x 10= 20 Marks)				
14	3	3		
15	3	3		
16	3	3		

Consolidated Marks:

	Marks Scored
CO2	
CO3	
PO2	
PO3	
Total	

Signature of the Course Teacher