# UNIT-IV SEQUENTIAL SYSTEMS

Source: These slides contains copyrighted materials from - Digital Design with an Introduction to the Verilog HDL, M. Morris Mano, Michael D. Ciletti

- **Text book**

M. Morris Mano, Michael D. Ciletti, "Digital Design with an Introduction to the Verilog HDL", *5th edition,* Pearson education

# Overview

- Introduction- Sequential Circuit
- Flip-Flops & Latches SR latch
- Types of flip-flop
- Master-slave  flip-flop
- Registers
- Counters
- Shift Registers

# Introduction- Sequential Circuit

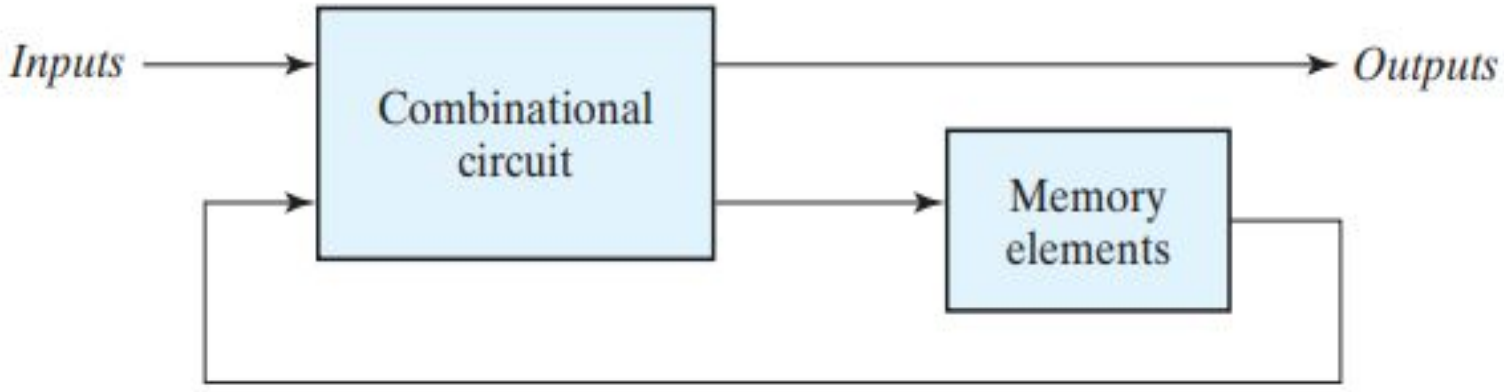



Fig.1. Block diagram of Sequential Circuits

# Sequential Circuit (contd…)

- Outputs in a sequential circuit are a function not only of the inputs, but also of the present state of the storage elements.
- Next state of the storage elements is also a function of external inputs and the present state.
- Sequential circuit is specified by a time sequence of inputs, outputs, and internal states .
- In contrast, the outputs of combinational logic depend only on the present values of the inputs.

# Sequential Circuit (contd…)

- two types of sequential circuits - classification is a function of the timing of their signals
  - Synchronous sequential circuit is a system whose behaviour can be defined from the knowledge of its signals at discrete instants of time.
  - The behaviour of an asynchronous sequential circuit depends upon the input signals at any instant of time and the order in which the inputs change

# Synchronous clocked sequential circuit

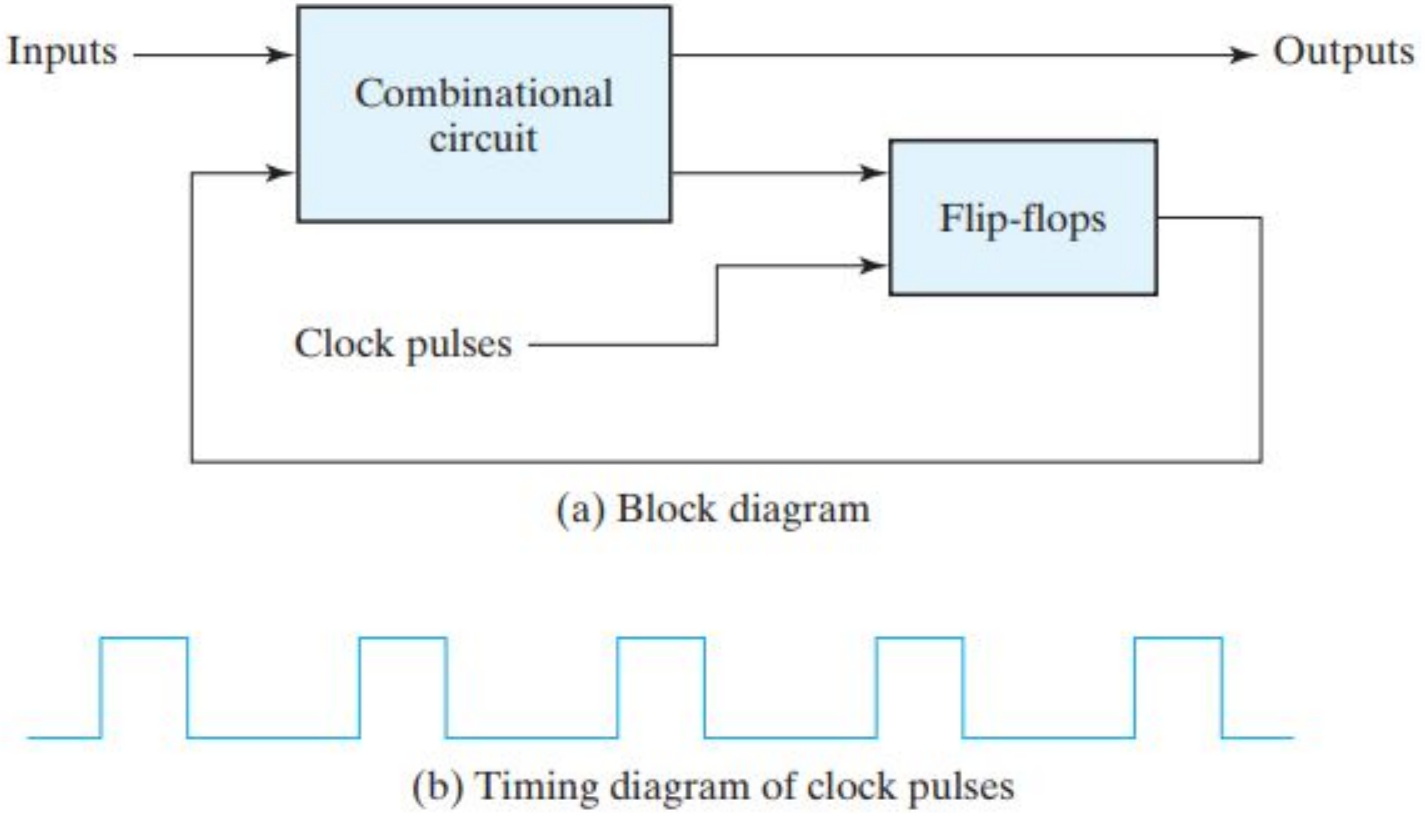
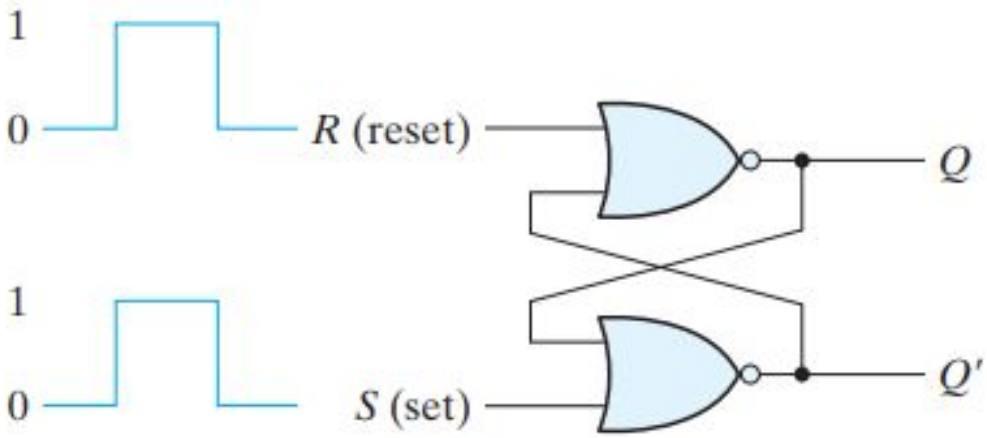



Fig.2. Synchronous clocked sequential circuit

# Storage Elements: Latches

- Storage elements that operate with signal levels (rather than signal transitions) –latches
- Latches are said to be level sensitive devices
- latches are the basic circuits from which all flip-flops are constructed
- Not practical for use as storage elements in synchronous sequential circuits

# SR latch with NOR gates



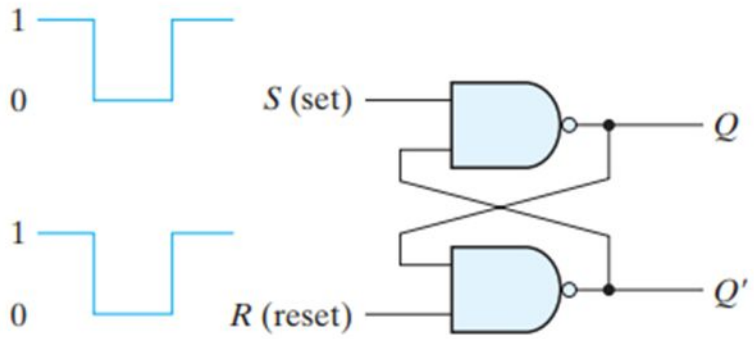

(a) Logic diagram

| $S$ | $R$ | $Q$ | $Q'$ | |
|---|---|---|---|---|
| 1 | 0 | 1 | 0 | |
| 0 | 0 | 1 | 0 | (after $S = 1, R = 0$) |
| 0 | 1 | 0 | 1 | |
| 0 | 0 | 0 | 1 | (after $S = 0, R = 1$) |
| 1 | 1 | 0 | 0 | (forbidden) |

(b) Function table

- SR latch constructed with two cross-coupled NOR gates
- When output Q = 1 and Q' = 0, the latch is said to be in the set state
- When Q = 0 and Q' = 1, , the latch is said to be in the reset state

# SR latch with NAND gates



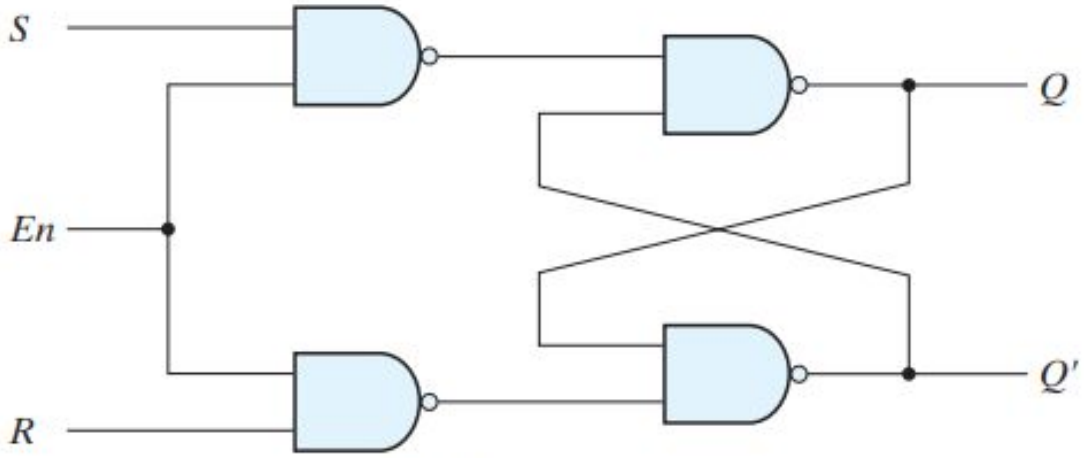

(a) Logic diagram

| $S$ | $R$ | $Q$ | $Q'$ | |
|---|---|---|---|---|
| 1 | 0 | 0 | 1 | |
| 1 | 1 | 0 | 1 | (after $S = 1, R = 0$) |
| 0 | 1 | 1 | 0 | |
| 1 | 1 | 1 | 0 | (after $S = 0, R = 1$) |
| 0 | 0 | 1 | 1 | (forbidden) |

(b) Function table

- In comparing the NAND with the NOR latch, note that the input signals for the NAND require the complement of those values used for the NOR latch.
- Because the NAND latch requires a 0 signal to change its state, it is sometimes referred to as an S'R' latch.

# SR latch with control input



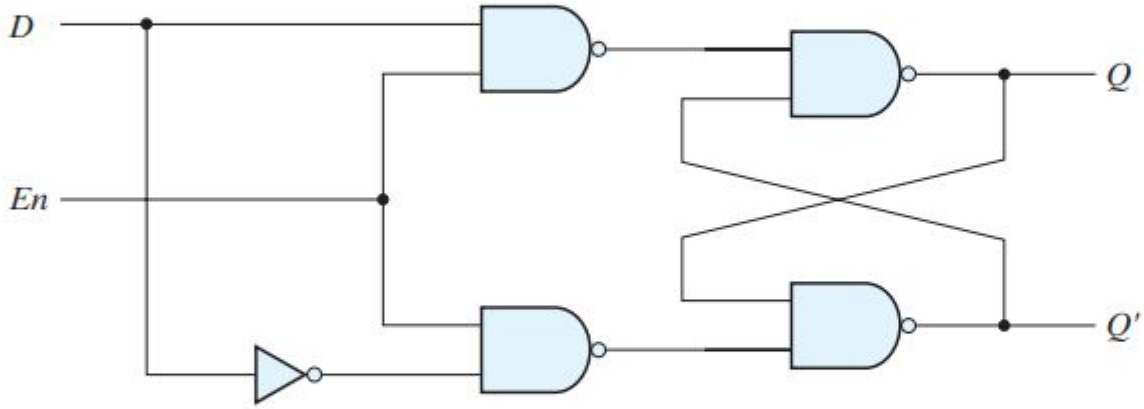

(a) Logic diagram

| *En* | *S* | *R* | Next state of *Q* |
|---|---|---|---|
| 0 | X | X | No change |
| 1 | 0 | 0 | No change |
| 1 | 0 | 1 | $Q = 0$; reset state |
| 1 | 1 | 0 | $Q = 1$; set state |
| 1 | 1 | 1 | Indeterminate |

(b) Function table

- It consists of the basic SR latch and two additional NAND gates.
- The control input E*n* acts as an enable signal for the other two inputs.
- The outputs of the NAND gates stay at the logic-1 level as long as the enable signal remains at 0
- When the enable input goes to 1, information from the S or R input is allowed to affect the latch
- Indeterminate condition makes this circuit difficult to manage

# D Latch (Transparent Latch)



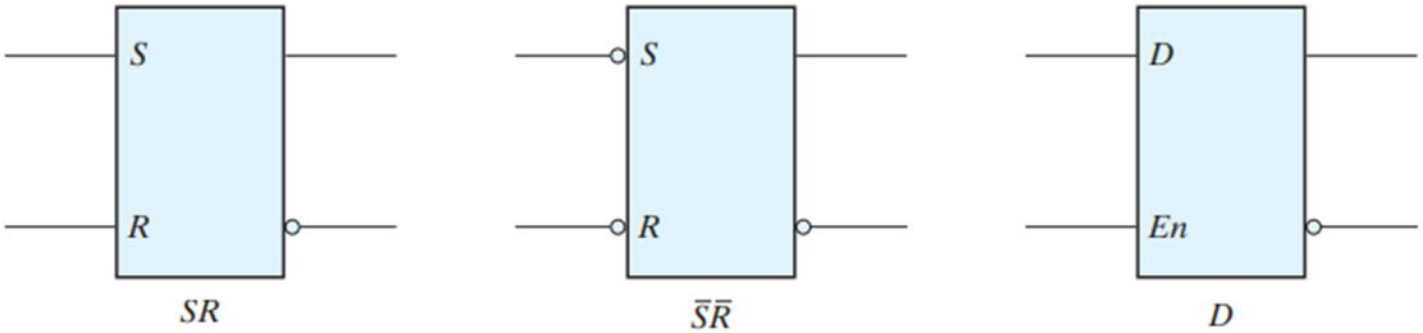

(a) Logic diagram

| *En* | *D* | Next state of *Q* |
|---|---|---|
| 0 | X | No change |
| 1 | 0 | $Q = 0$; reset state |
| 1 | 1 | $Q = 1$; set state |

(b) Function table

One way to eliminate the undesirable condition of the indeterminate state in the SR latch is to ensure that inputs S and R are never equal to 1 at the same time. This is done in the D latch

# Graphic symbols for latches



# Storage Elements: Flip-Flops

## Latches

- Output depends on clock
  - Clock high: Input passes to output
  - Clock low: Latch holds its output
- Latches are level sensitive and “transparent”

## Flip-flops

- Input sampled at clock edge
  - Rising edge: Input passes to output
  - Otherwise: Flip-flop holds its output
- Flip-flops can be rising-edge triggered or falling-edge triggered

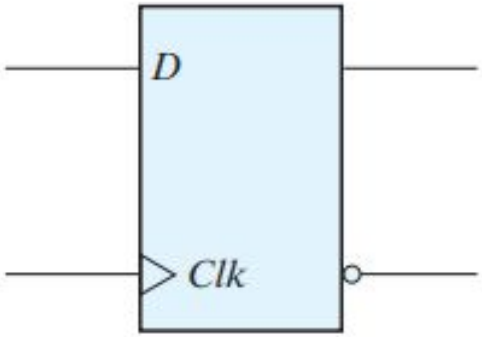
# Clock response in latches and flip-flops

(a) Response to positive level

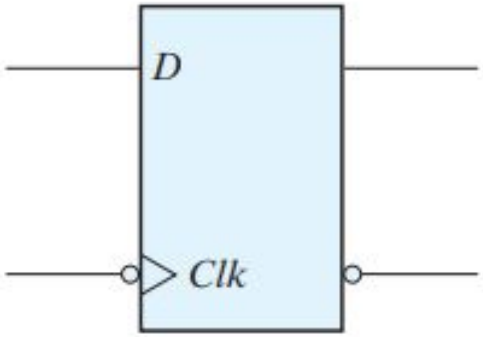
(b) Positive-edge response

(c) Negative-edge response

# Graphic symbol for edge triggered D-flip-flop




(a) Positive-edge




(a) Negative-edge

*Flip-Flop Characteristic Tables*

**D Flip-Flop**

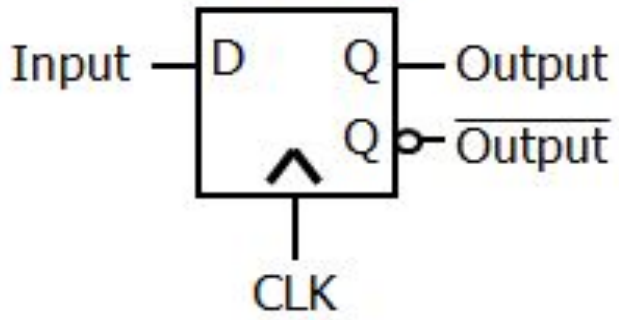
| D | Q(t + 1) | |
|---|---|---|
| 0 | 0 | Reset |
| 1 | 1 | Set |

**Characteristic Equation**

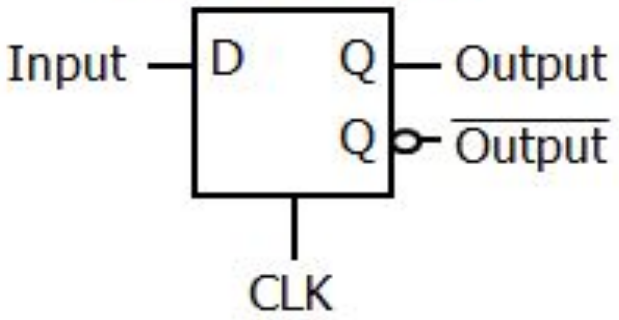
$$Q(t + 1) = D$$

# Terminology & Notation

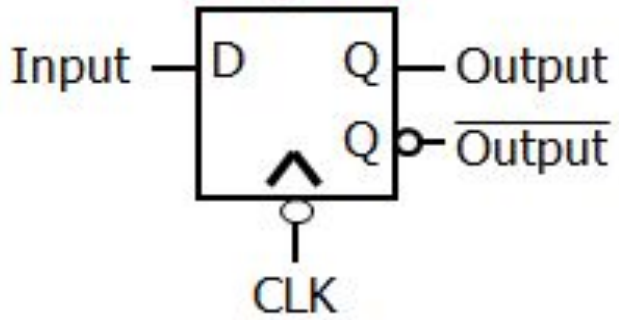
Rising-edge triggered D flip-flop



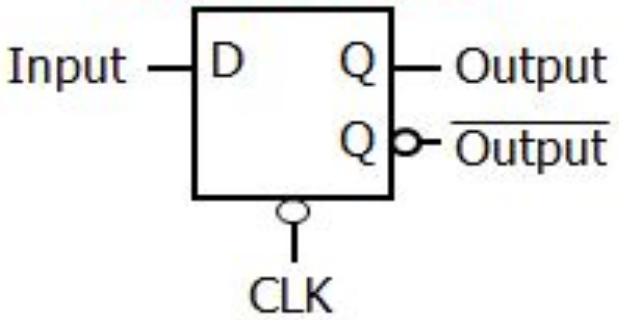

Positive D latch



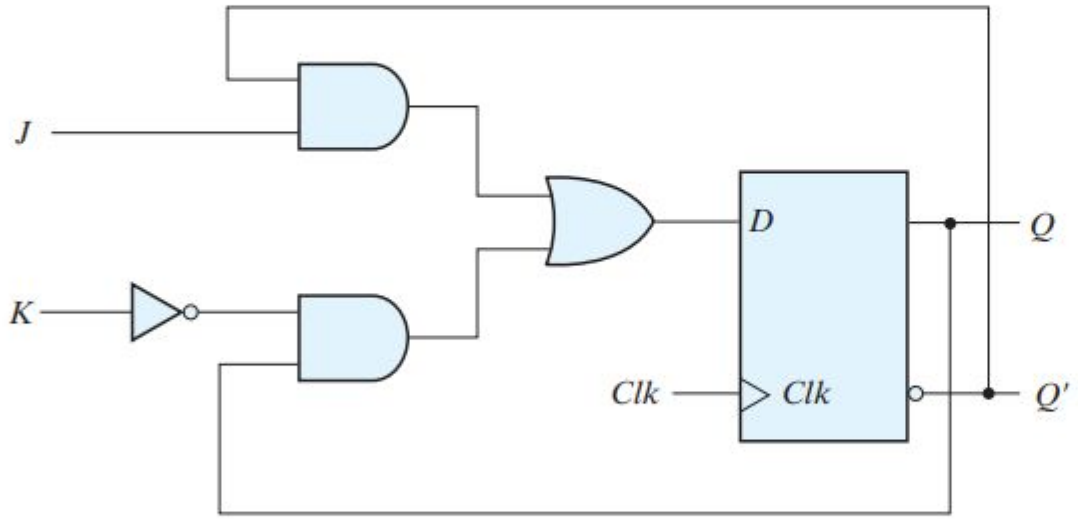

Falling-edge triggered D flip-flop



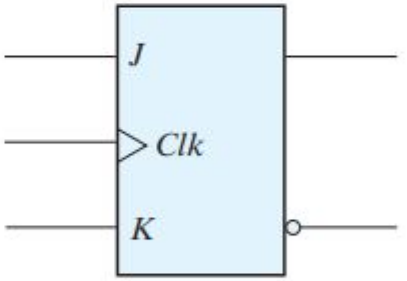

Negative D latch



# JK flip-flop




(a) Circuit diagram




(b) Graphic symbol

*Flip-Flop Characteristic Tables*

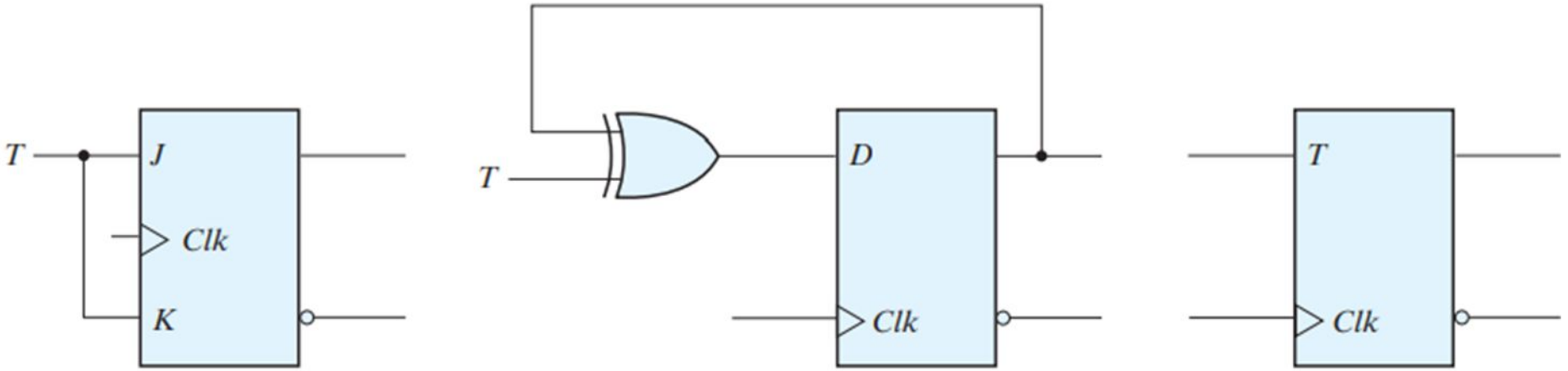
**JK Flip-Flop**

| J | K | Q(t + 1) | |
|---|---|---|---|
| 0 | 0 | $Q(t)$ | No change |
| 0 | 1 | 0 | Reset |
| 1 | 0 | 1 | Set |
| 1 | 1 | $Q'(t)$ | Complement |

**Characteristic Equation**

$$Q(t + 1) = JQ' + K'Q$$

# T flip flop (Toggle flip-flop)




(a) From *JK* flip-flop (b) From *D* flip-flop (c) Graphic symbol

*Flip-Flop Characteristic Tables*

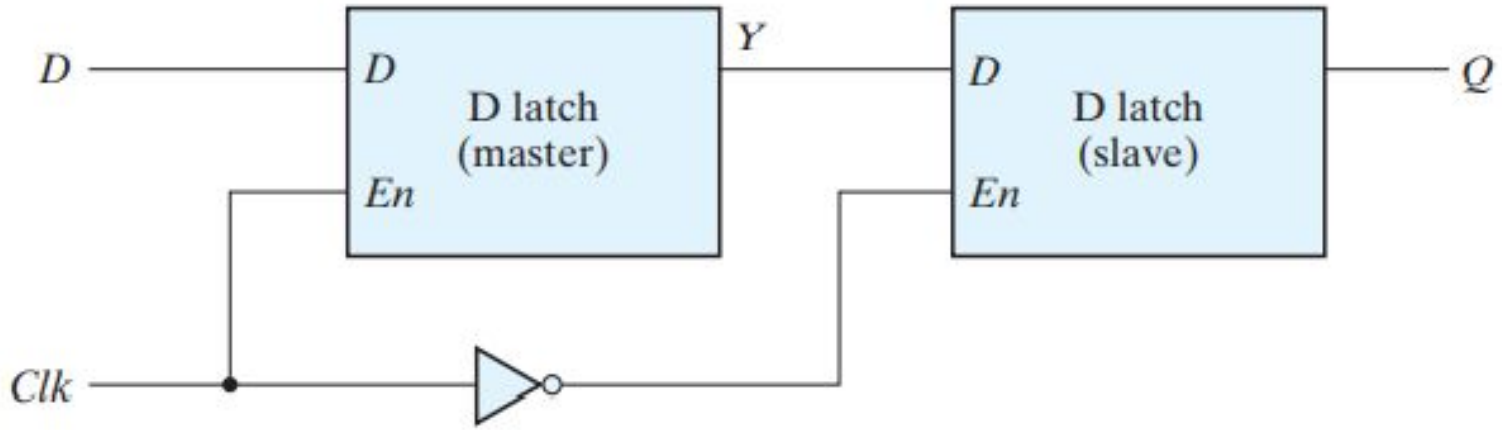
**T Flip-Flop**

| T | Q(t + 1) | |
|---|---|---|
| 0 | $Q(t)$ | No change |
| 1 | $Q'(t)$ | Complement |

**Characteristic Equation**

$$Q(t+1) = T \oplus Q = TQ' + T'Q$$

# Master-slave D flip-flop




- The construction of a D flip-flop with two D latches and an inverter
- The first latch is called the master and the second the slave
- a change in the output of the flip-flop can be triggered only by and during the transition of the clock from 1 to 0

# Behaviour of the master–slave flip-flop

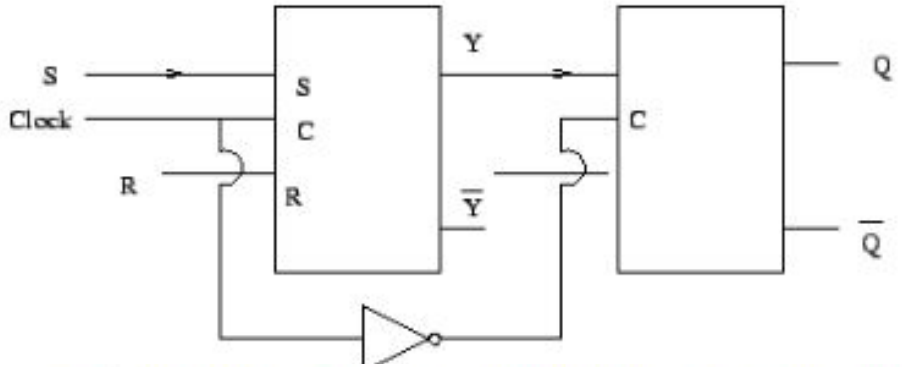
(1) the output may change only once,

(2) a change in the output is triggered by the negative edge of the clock

(3) the change may occur only during the clock's negative level.

- The value that is produced at the output of the flip-flop is the value that was stored in the master stage immediately before the negative edge occurred .

# Master-slave SR flip-flop




*When $S = 1$, $R = 1$, $Q$ and $\overline{Q}$ are both 1. Therefore, it is an undefined condition. This can be eliminated by proper feedback.*

# Master-slave JK flip-flop

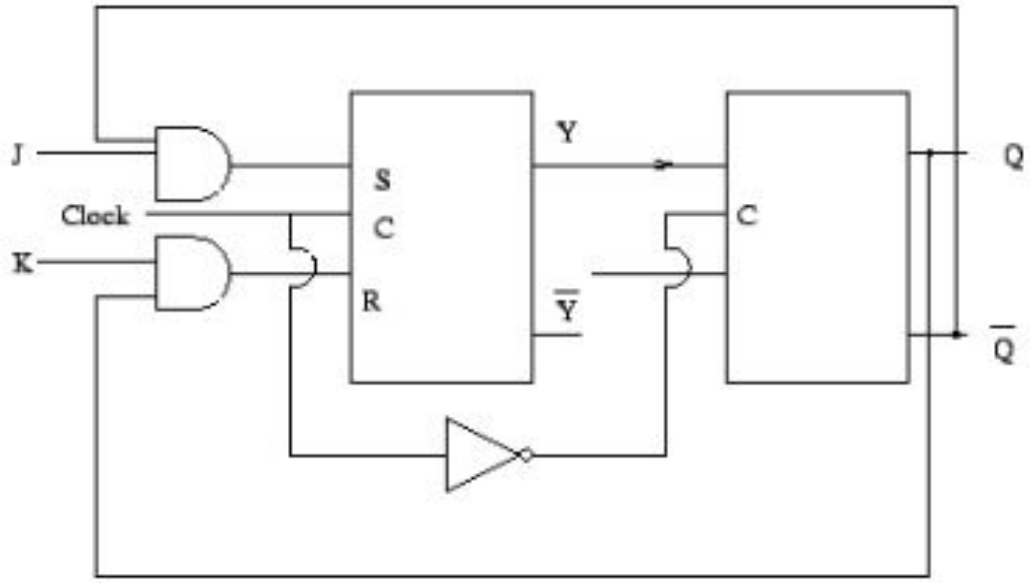


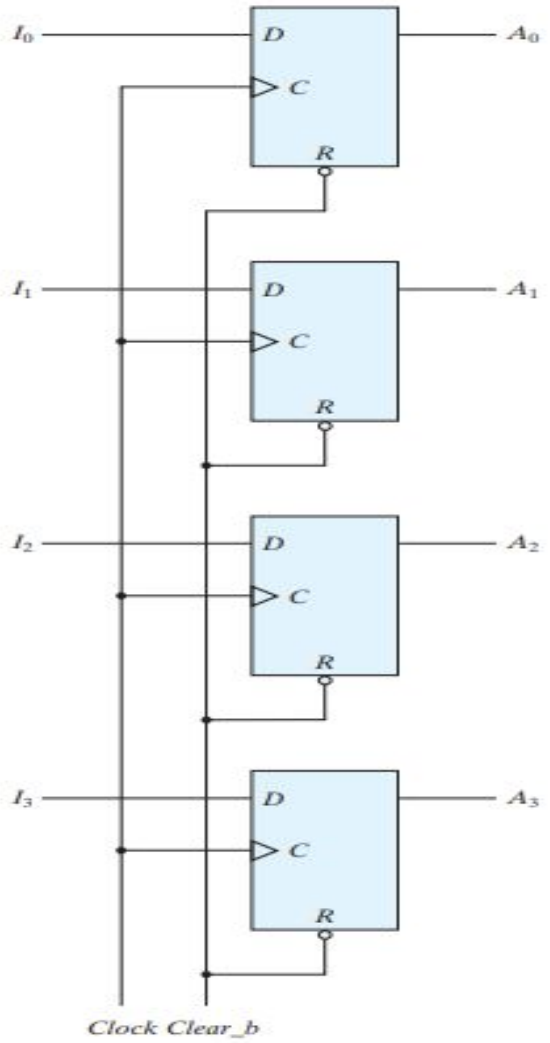

Fig. a. Circuit diagram

| $J$ | $K$ | $Q_{n+1}$ |
|---|---|---|
| 1 | 1 | $\overline{Q_n}$ |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 0 | 0 | $Q_n$ |

Fig. b. Truth table

# 4 bit Registers

- A register is a group of flip-flops, each one of which shares a common clock and is capable of storing one bit of information
- n -bit register consists of a group of n-flip-flops capable of storing n bits of binary information
- A register constructed with four D -type flip-flops to form a four-bit data storage register
- “Clock” triggers all flipfolps on the positive edge of each pulse.
- “Clear” is useful for clearing the register to all 0’s prior to its clocked operation.



# Counters

- Counter is essentially a register
  - special type of register
- Goes through a predetermined sequence of binary states.
- Gates in the counter are connected to produce the prescribed sequence of states.
- Types
  - Synchronous Counter
  - Asynchronous Counter

# Shift Registers

- A register capable of shifting its binary information in one or both directions is called a shift register
- Logical configuration - chain of flip-flops in cascade, with the output of one flip-flop connected to the input of the next flip-flop.
- All flip-flops receive common clock pulses that initiate the shift from one stage to the next stage

# Capabilities of shift registers

- 1. An input for clock pulses to synchronize all operations.
- 2. A shift-right operation and a serial input line associated with the shift right.
- 3. A shift-left operation and a serial input line associated with the shift-left.
- 4. A parallel load operation and n input lines associated with the parallel transfer.
- 5. n parallel output lines.
- 6. A control state that leaves the information in the register unchanged even though clock pulses are applied continuously.

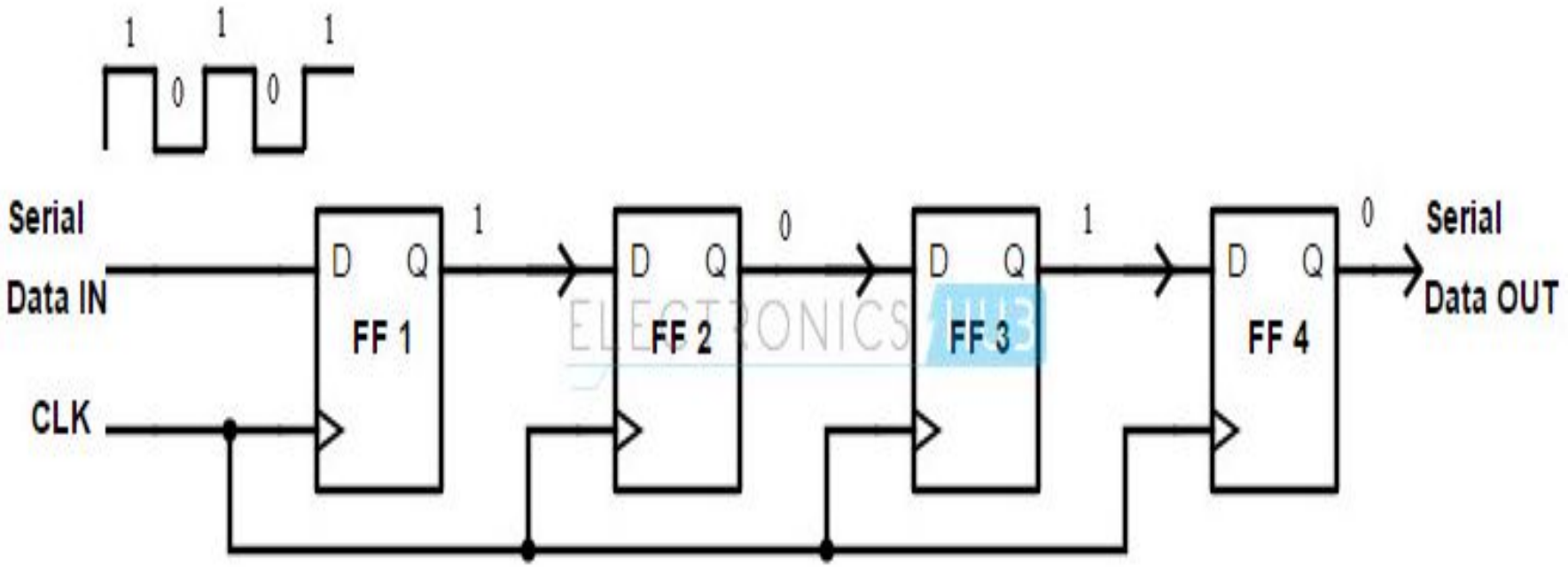
# Universal Shift Register

- If the register has both shifts and parallel load capabilities, it is referred to as a universal shift register.
- Shift registers are often used to interface digital system situated remotely from each other.
- If the distance is far, it will be expensive to use n-lines to transmit the n- bits in parallel.
- Transmitter performs a parallel-to-serial conversion of data and the receiver does a serial-to-parallel conversion.

# Types

- Serial in serial out (SISO)
- Serial in parallel out (SIPO)
- Parallel in serial out (PISO)
- Parallel in parallel out (PIPO)

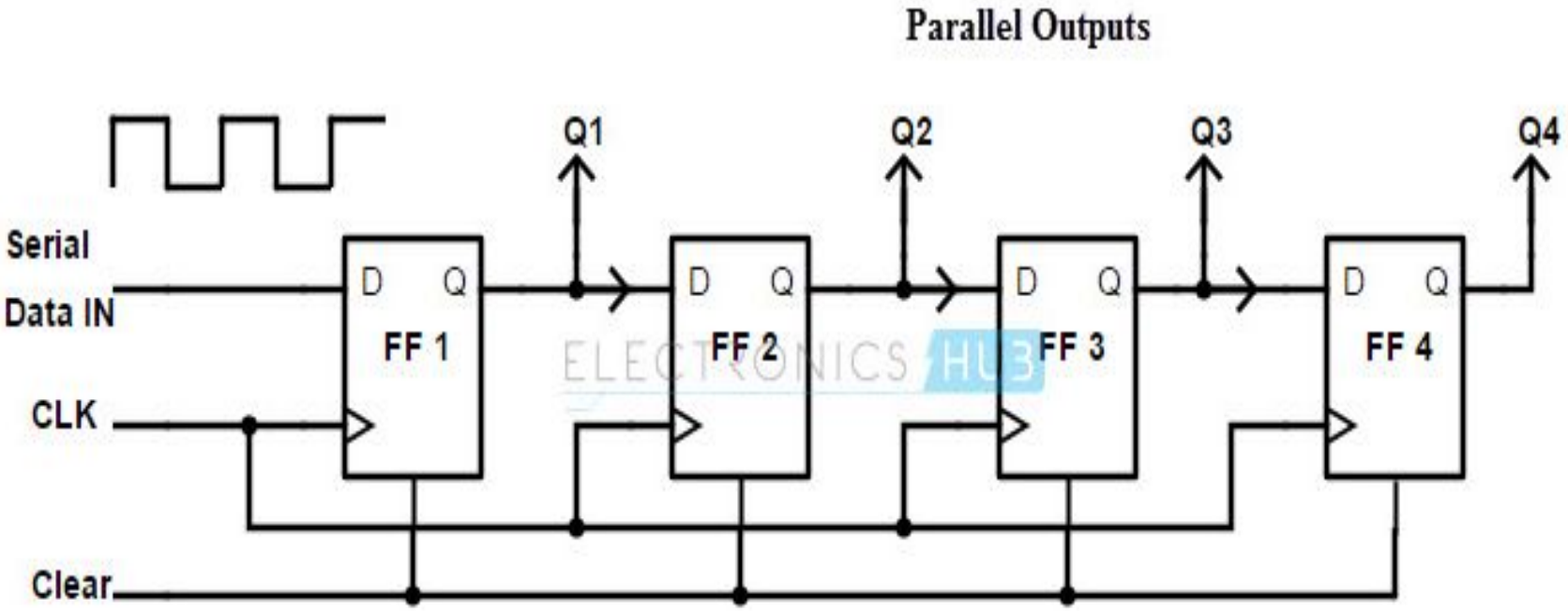
# SISO


1
1
1
0
0
Serial
Data IN
CLK
D
Q
FF 1
FF 2
FF 3
FF 4
1
0
1
0
Serial
Data OUT

# SISO

- The input to this register is given in serial and the output is collected in serial
- The output of the first flip flop is connected to the input of the next flip flop and so on. The final output of the shift register is collected at the outmost flip flop.
- In this shift register, when the clock signal is applied and the serial data is given
- only one bit will be available at output at a time in the order of the input data.
- Use - temporary data storage device.
- Application - act as a delay element.

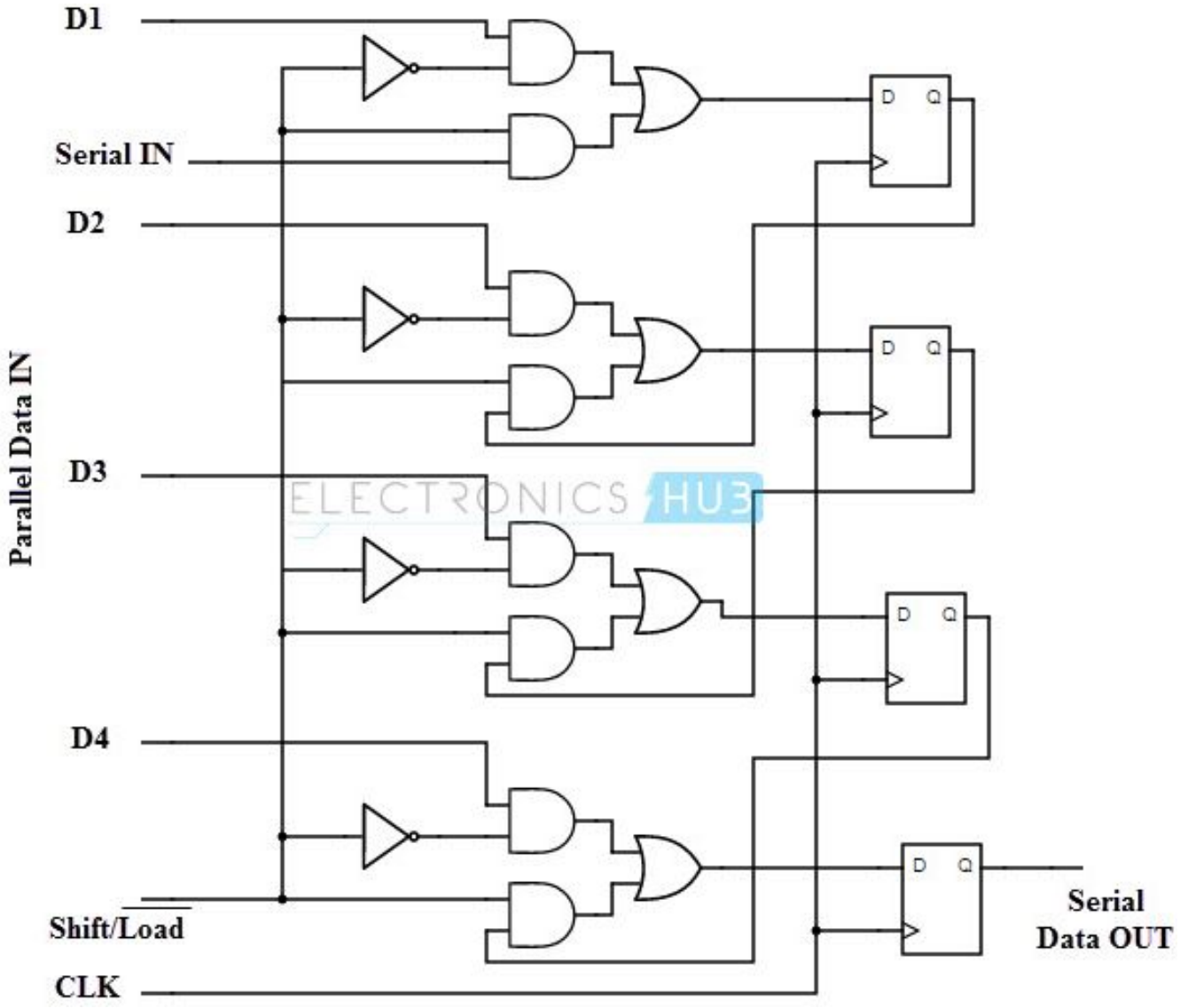
# SIPO


Parallel Outputs
Q1
Q2
Q3
Q4
Serial
Data IN
CLK
Clear
D
Q
FF 1
FF 2
FF 3
FF 4
ELECTRONICS HUB

# SIPO

- The input to this register is given in serial and the output is collected in parallel
- The clear (CLR) signal is connected in addition to clock signal to all the 4 flip flops in order to RESET them and the serial data is connected to the flip flop at either end (depending on shift left register or shift right register).
- The output of the first flip flop is connected to the input of the next flip flop and so on. All the flip flops are connected with a common clock.
- Unlike the SISO shift registers, the output of Serial in Parallel out (SIPO) shift register is collected at each flip flop.
- Q1, Q2, Q3 and Q4 are the outputs of first, second, third and fourth flip flops, respectively.
- Application - to convert serial data into parallel data. Hence they are used in communication lines where demultiplexing of a data line into several parallel line is required.

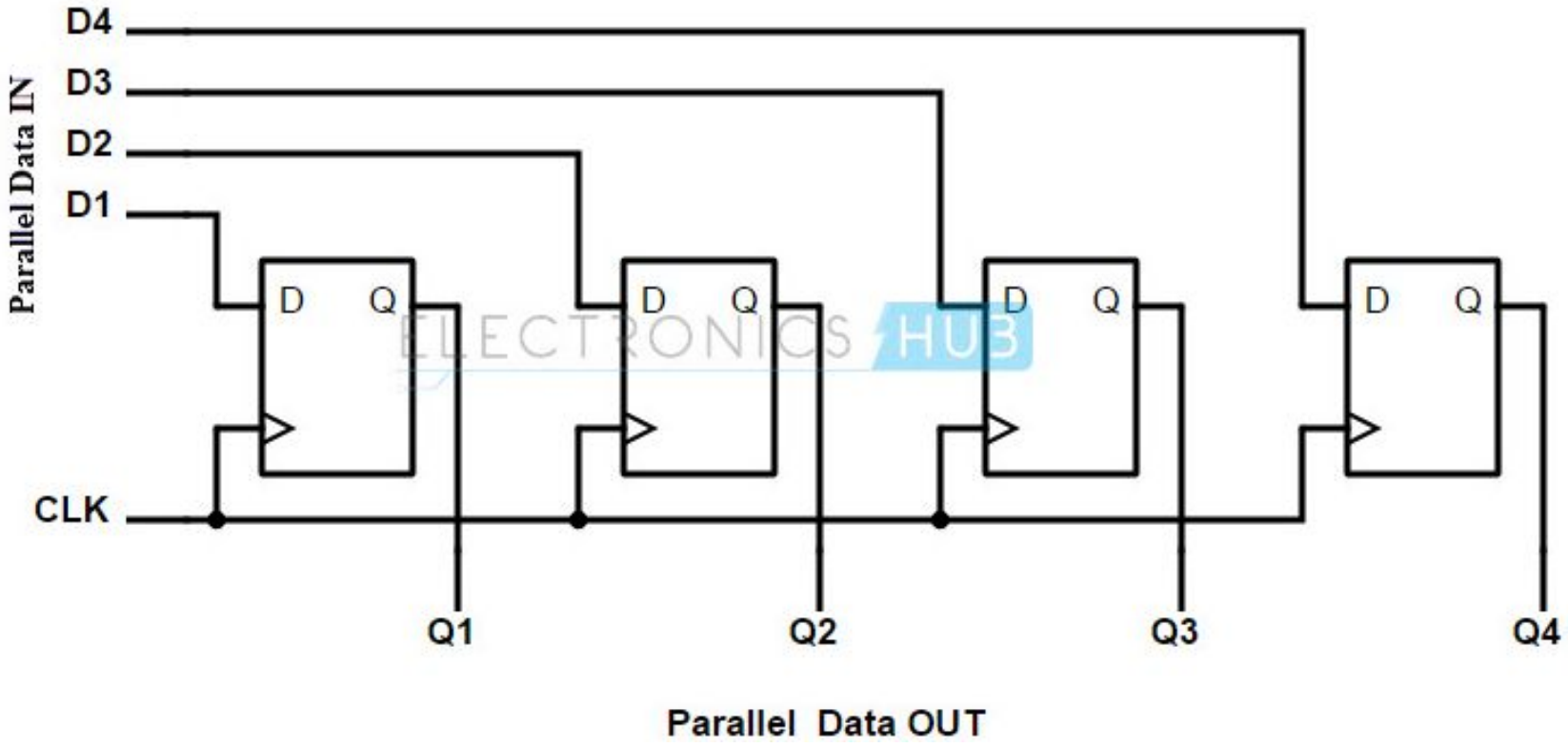
# PISO


D1
Serial IN
D2
Parallel Data IN
D3
D4
Shift/Load
CLK
D Q
D Q
D Q
D Q
Serial
Data OUT
ELECTRONICS HUB

# PISO

- The input to this register is given in parallel i.e. data is given separately to each flip flop and the output is collected in serial at the output of the end flip flop.
- The clock input is directly connected to all the flip flops but the input data is connected individually to each flip flop through a mux (multiplexer) at input of every flip flop.
- D1, D2, D3 and D4 are the individual parallel inputs to the shift register.
- The output of the previous flip flop and parallel data input are connected to the input of the MUX and the output of MUX is connected to the next flip flop.
- PISO shift register converts parallel data to serial data.
- Application - used in communication lines where a number of data lines are multiplexed into single serial data line.

# PIPO


D4
D3
D2
D1
Parallel Data IN
D Q
D Q
D Q
D Q
CLK
Q1
Q2
Q3
Q4
Parallel Data OUT

# PIPO

- In this register, the input is given in parallel and the output also collected in parallel.
- Clock signals are connected to all the 4 flip flops.
- Data is given as input separately for each flip flop and in the same way, output also collected individually from each flip flop.
- There are no interconnections between any of the four flip flops.
- A Parallel in Parallel out (PIPO) shift register is used as a temporary storage device and also as a delay element similar to a SISO shift register.

# Summary

- ✔ Sequential Circuits & its types
- ✔ Flip-Flops & Latches
  - ✔ Definition
  - ✔ Types , Construction, Characteristic table & equations
- ✔ Master-slave - D FF, JK FF, SR FF
- ✔ Registers
- ✔ Counters
- ✔ Shift Registers
  - ✔ Capabilities, Types, Applications & Universal shift register