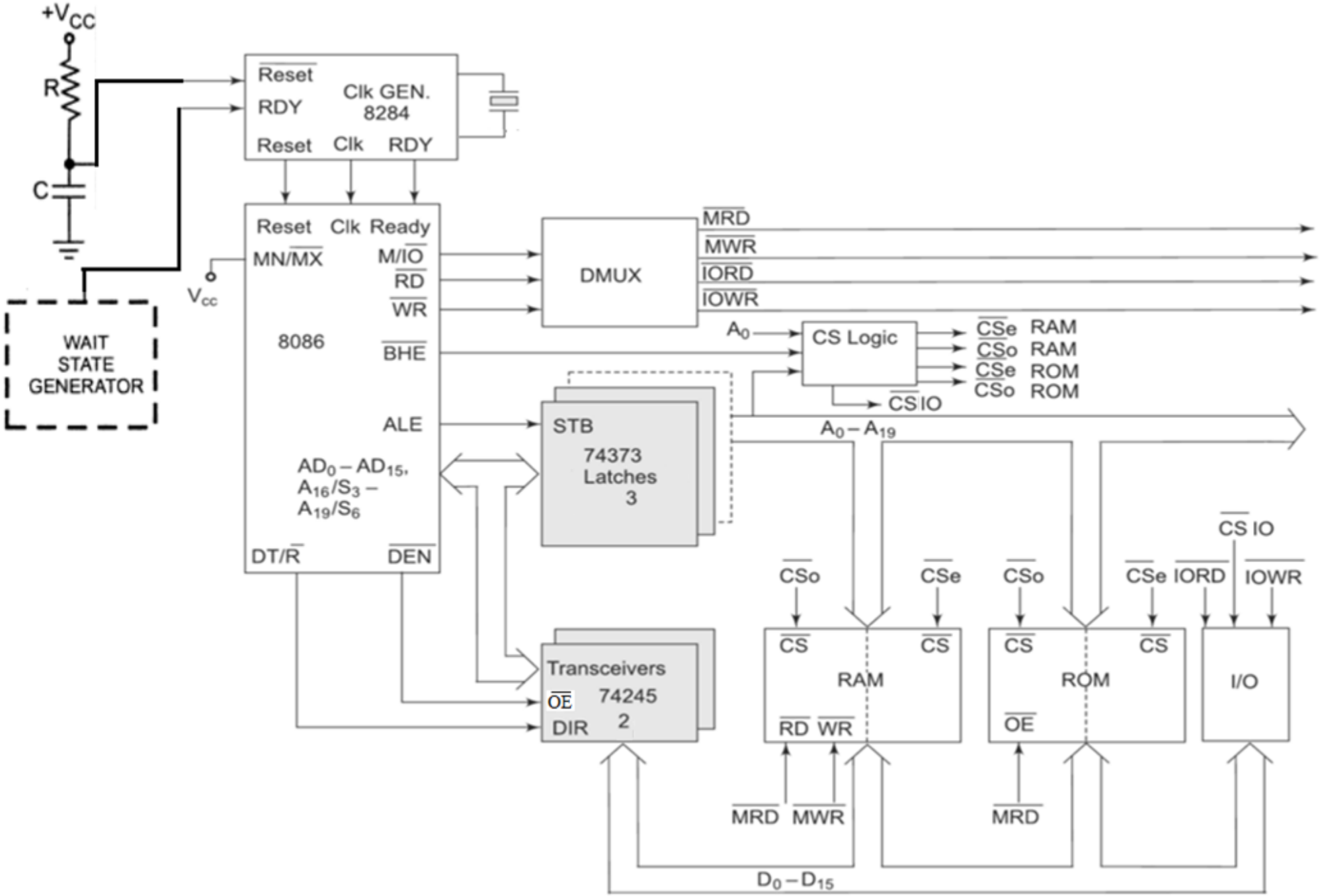
18ECC203J – Unit – 1 – Part - 2

Minimum Mode 8086 System

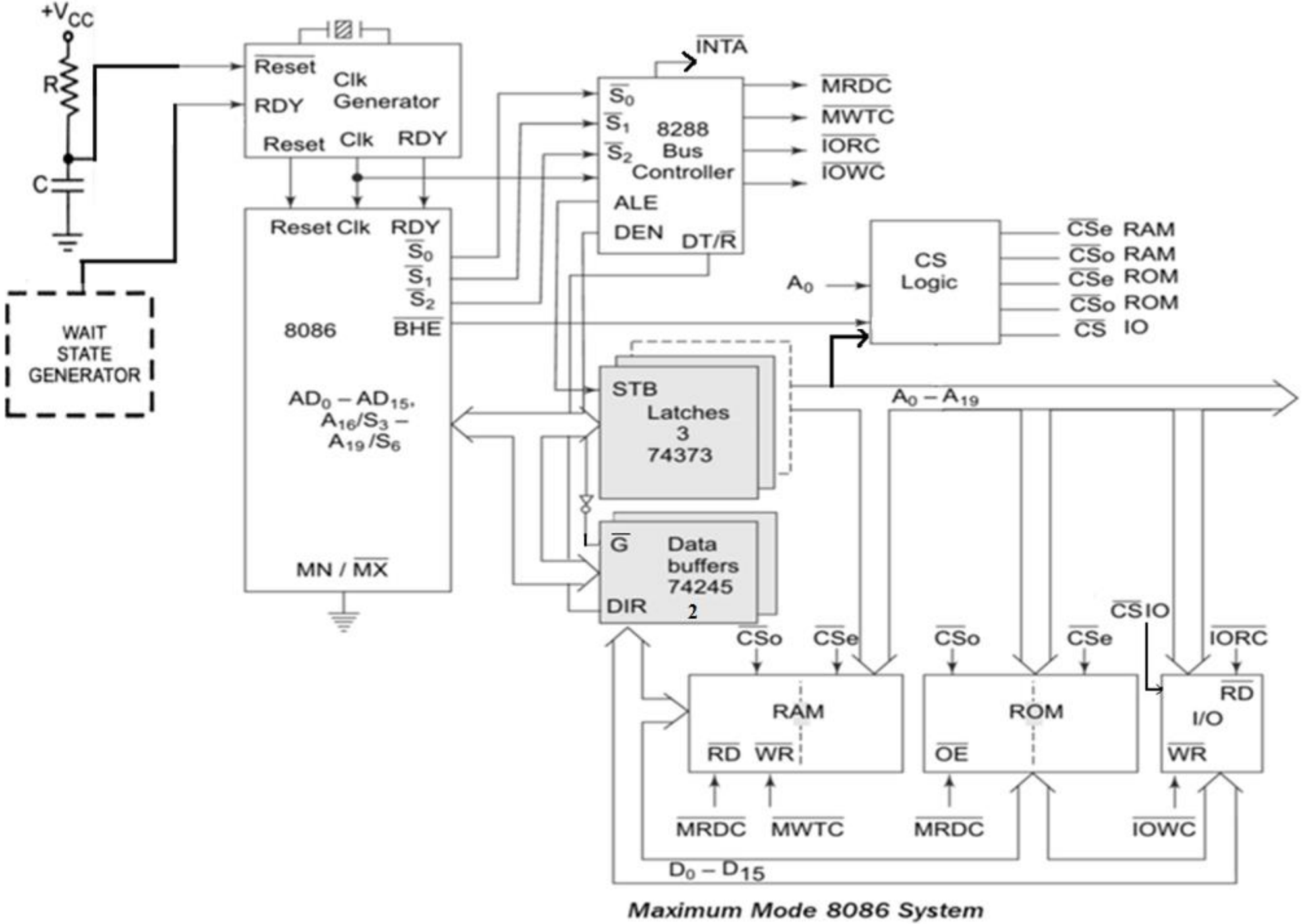


Minimum Mode 8086 System

Cont.

$M/\overline{IO}$	$\overline{RD}$	$\overline{WR}$	*Transfer Type*
0	0	1	I/O read
0	1	0	I/O write
1	0	1	Memory read
1	1	0	Memory write

Maximum Mode 8086 System



Maximum Mode 8086 System

Status Signals ($\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$) during various Machine Cycles

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Processor state	8288 command
0	0	0	Interrupt Acknowledge	$\overline{INTA}$
0	0	1	Read I/O Port	$\overline{IORC}$
0	1	0	Write I/O Port	$\overline{IOWC}$, $\overline{AIOWC}$
0	1	1	Halt	None
1	0	0	Code Access	$\overline{MRDC}$
1	0	1	Read Memory	$\overline{MRDC}$
1	1	0	Write Memory	$\overline{MWTC}$, $\overline{AMWC}$
1	1	1	Passive	None

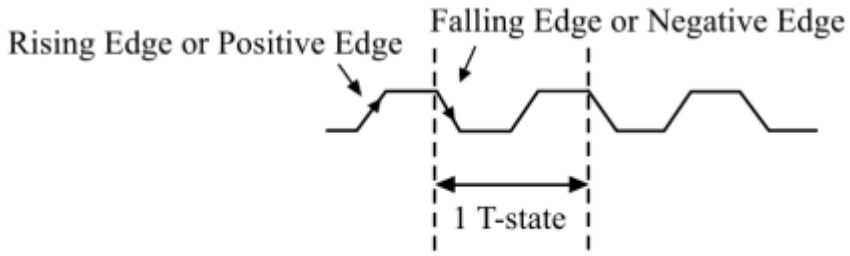
Signals of the 8288

- $\overline{\text{IORC}}$ – I/O Read Command
- $\overline{\text{IOWC}}$ – I/O Write Command
- $\overline{\text{MRDC}}$ – Memory Read Command
- $\overline{\text{MWTC}}$ – Memory Write Command
- $\overline{\text{AIOWC}}$ – Advance I/O Write Command
- $\overline{\text{AMWTC}}$ – Advance Memory Write Command
- $\overline{\text{INTA}}$ – Interrupt Acknowledge
- DEN, ALE, DT/$\overline{\text{R}}$

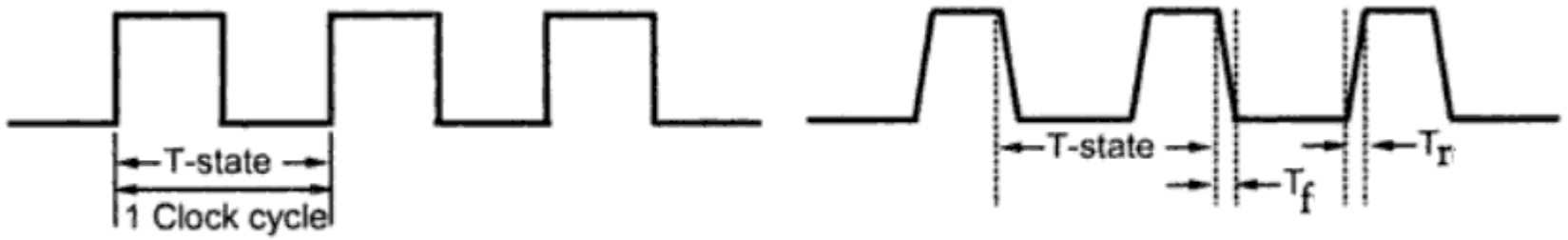
Timing Diagram

- **Timing Diagram** is a graphical representation.
- It represents the execution time taken by each instruction in a graphical format.
- The execution time is represented in T-states.
- **Instruction Cycle**: The time required to execute an instruction
- **Machine Cycle**: The time required to access the memory or input/output devices
- **T-State**: A portion of an operation carried out in one system clock period

T-State



Clock Signal.



(a) Ideal **(b) Practical**

Clock signal representation

Timing Diagram

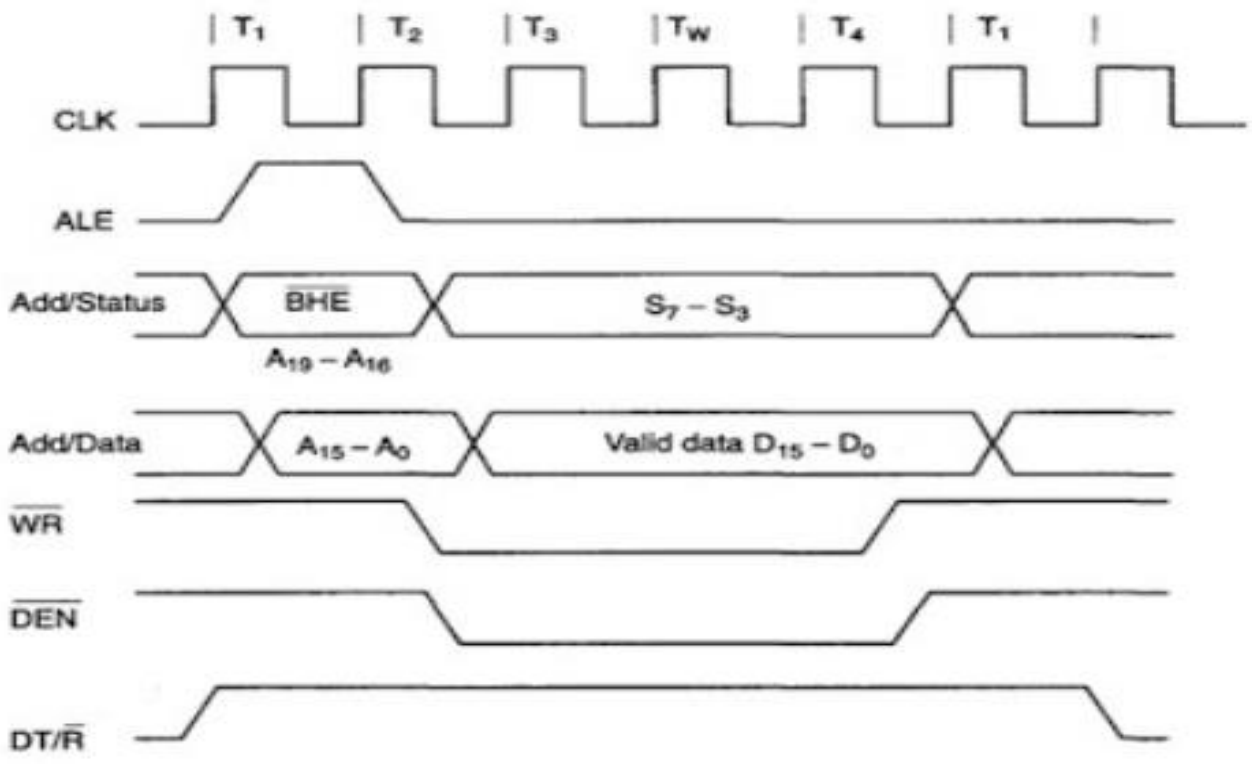
- Timing diagram provides information about the various conditions of the signals while a machine cycle is executed.
- In other words, it is the representation of various control signals generated during execution of an instruction
- Following Buses and Control signals must be shown in a Timing diagram:

✓**Higher Order Address Bus**, **Lower Address/Data bus**, **ALE**, $\overline{RD}$, $\overline{WR}$, IO/$\overline{M}$

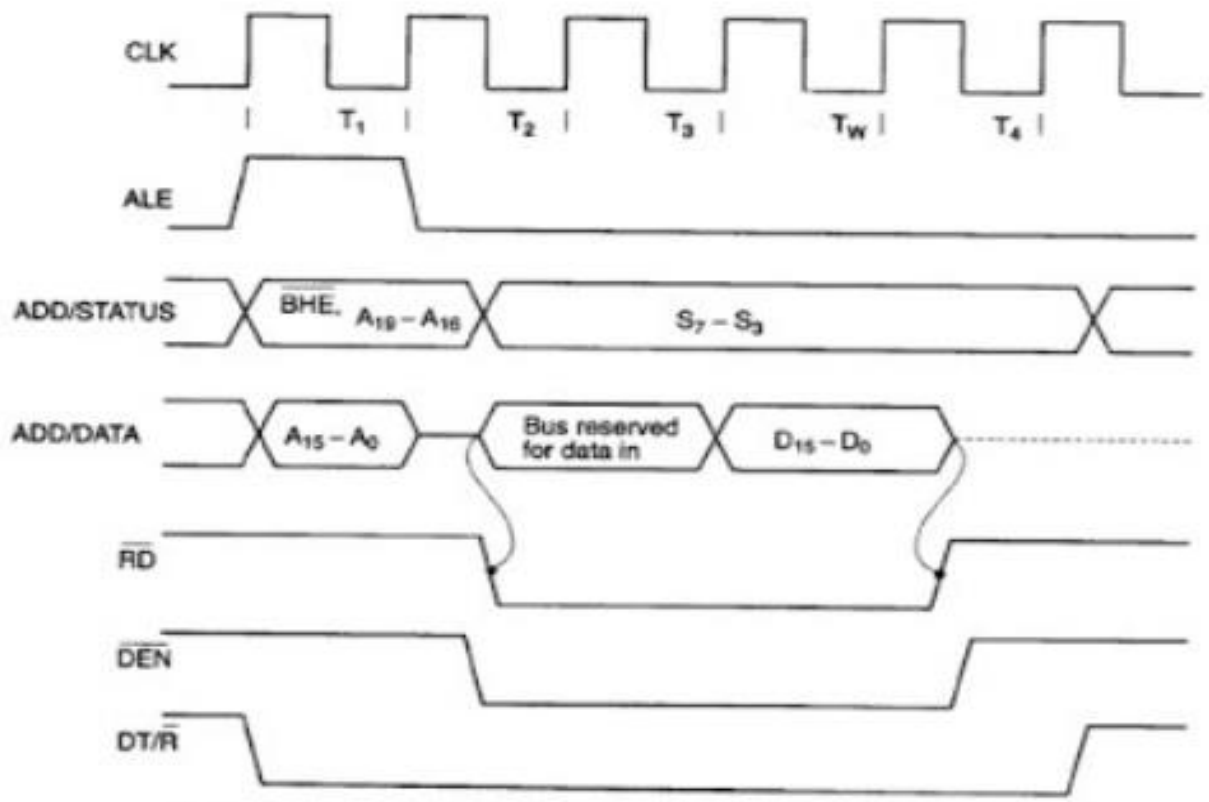
Bus cycle and T states

- A bus cycle defines the basic operation that a microprocessor performs to communicate with external devices
- Examples of bus cycles are memory read, memory write, input/output read and input/output write.
- A bus cycle corresponds to a sequence of events that starts with an address being output on the system bus followed by a read or write data transfer
- During these operations, a series of control signals are also produced by the MPU to control the direction and timing of the bus.
- Bus cycle consists of at least four clock periods, T1, T2, T3, and T4.
  - During T1 the MPU puts the address on the address bus
  - For a write memory cycle, data are put on the bus during state T2 and maintained thru T3 and T4.
  - When a read cycle is performed, the bus is first put in the high-Z state during T2 and data to be read must be available on the bus during T3 and T4.
  - Bus cycle duration of 125 ns x 4 = 500 ns in an 8 mhz 8088 system

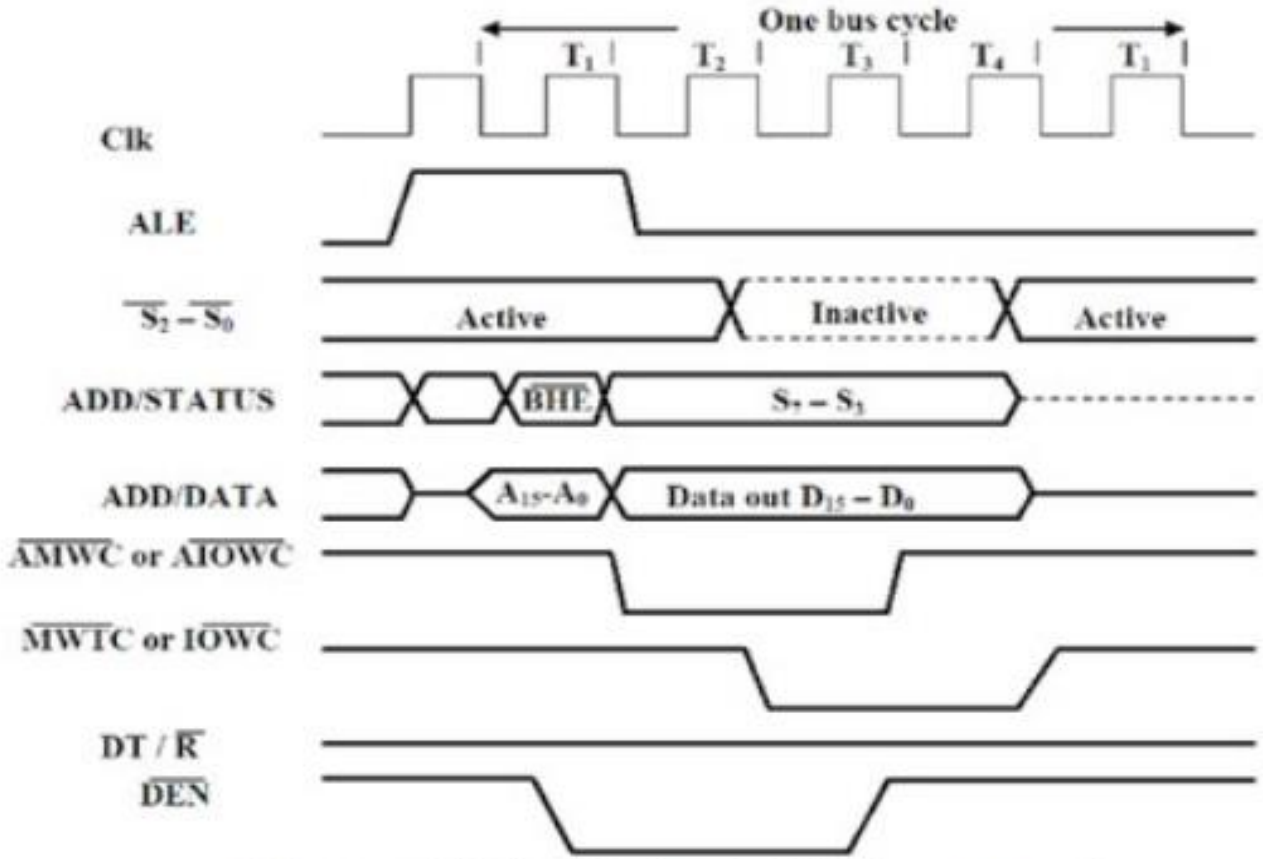
Timing Diagram : Write cycle – Minimum mode



Timing Diagram : Read cycle – Minimum mode

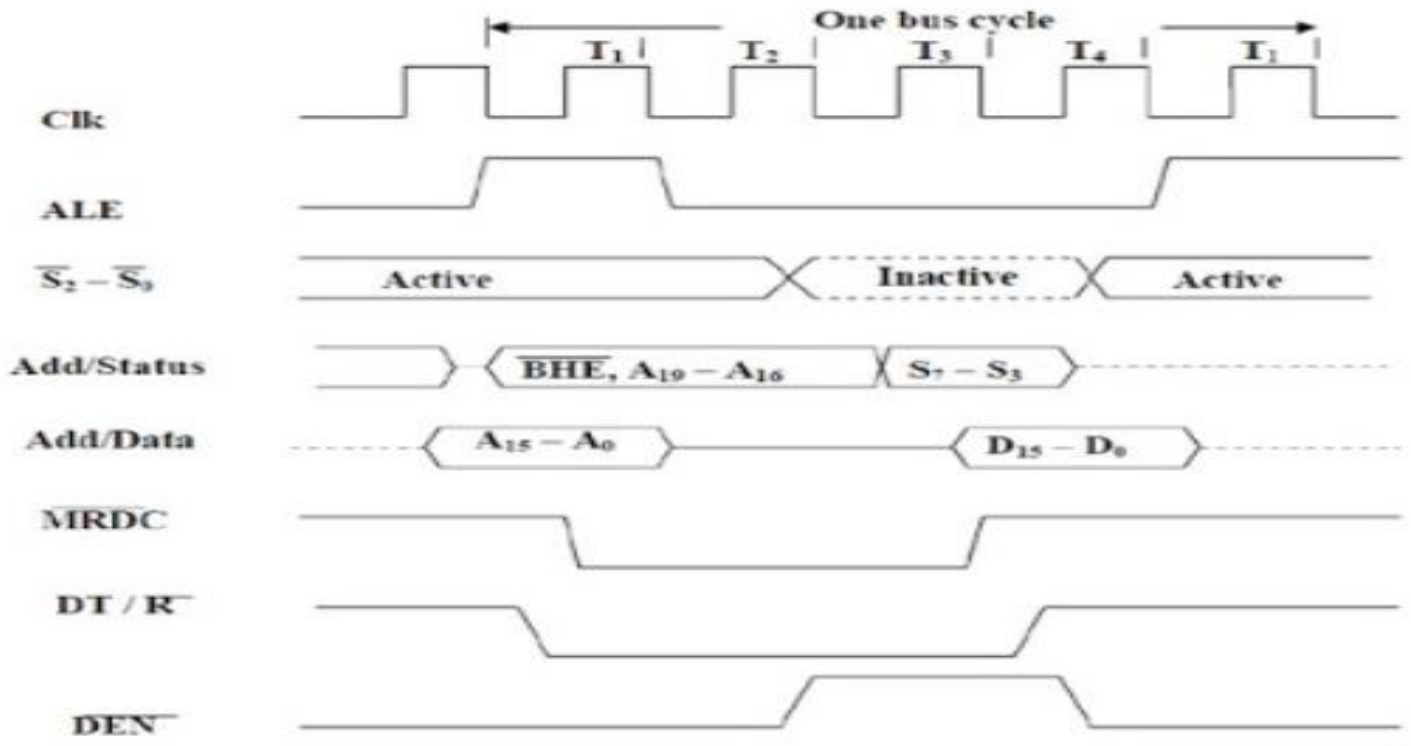


Timing Diagram : Write cycle – Maximum mode



Memory Write Timing in Maximum mode.

Timing Diagram : Read cycle – Maximum mode

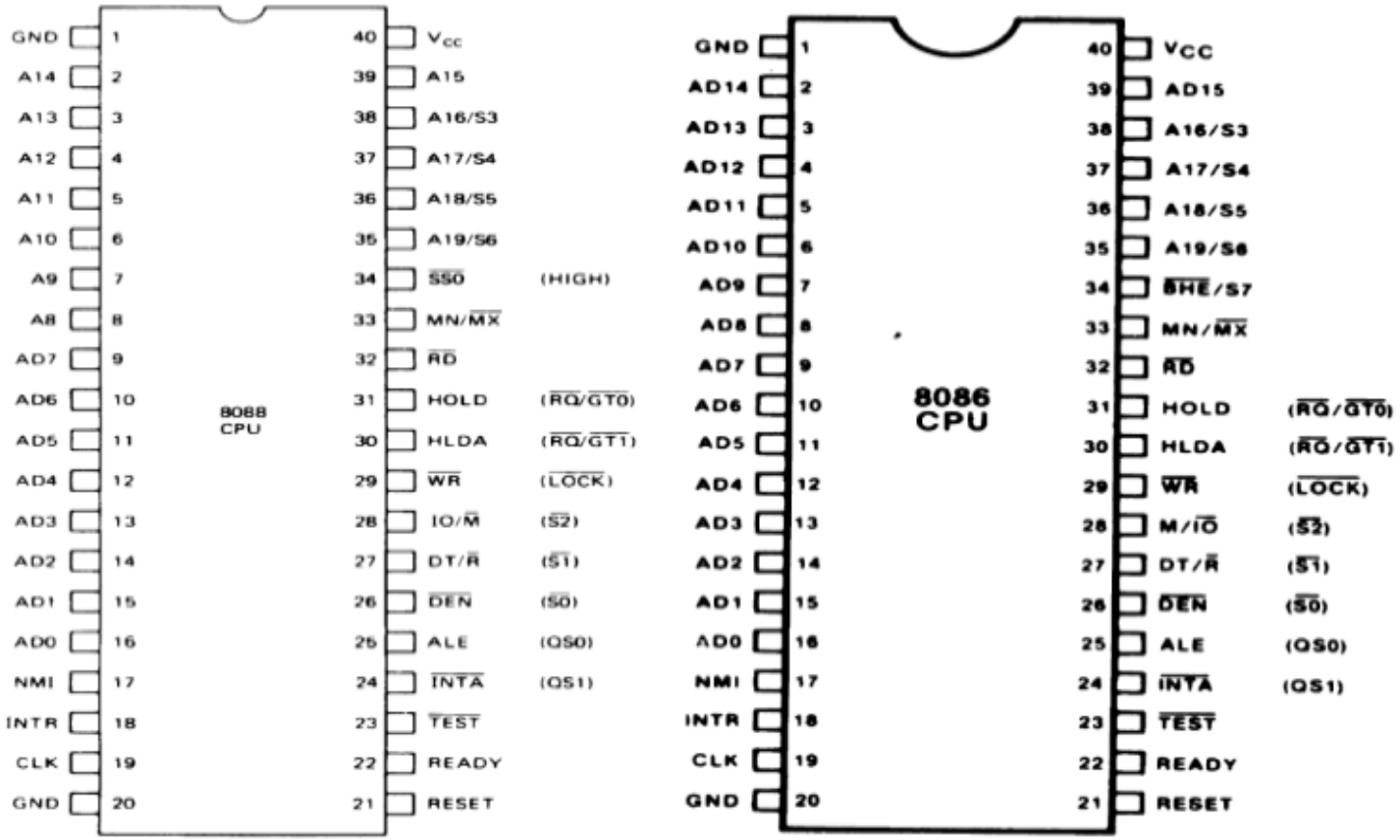


Memory Read Timing in Maximum Mode

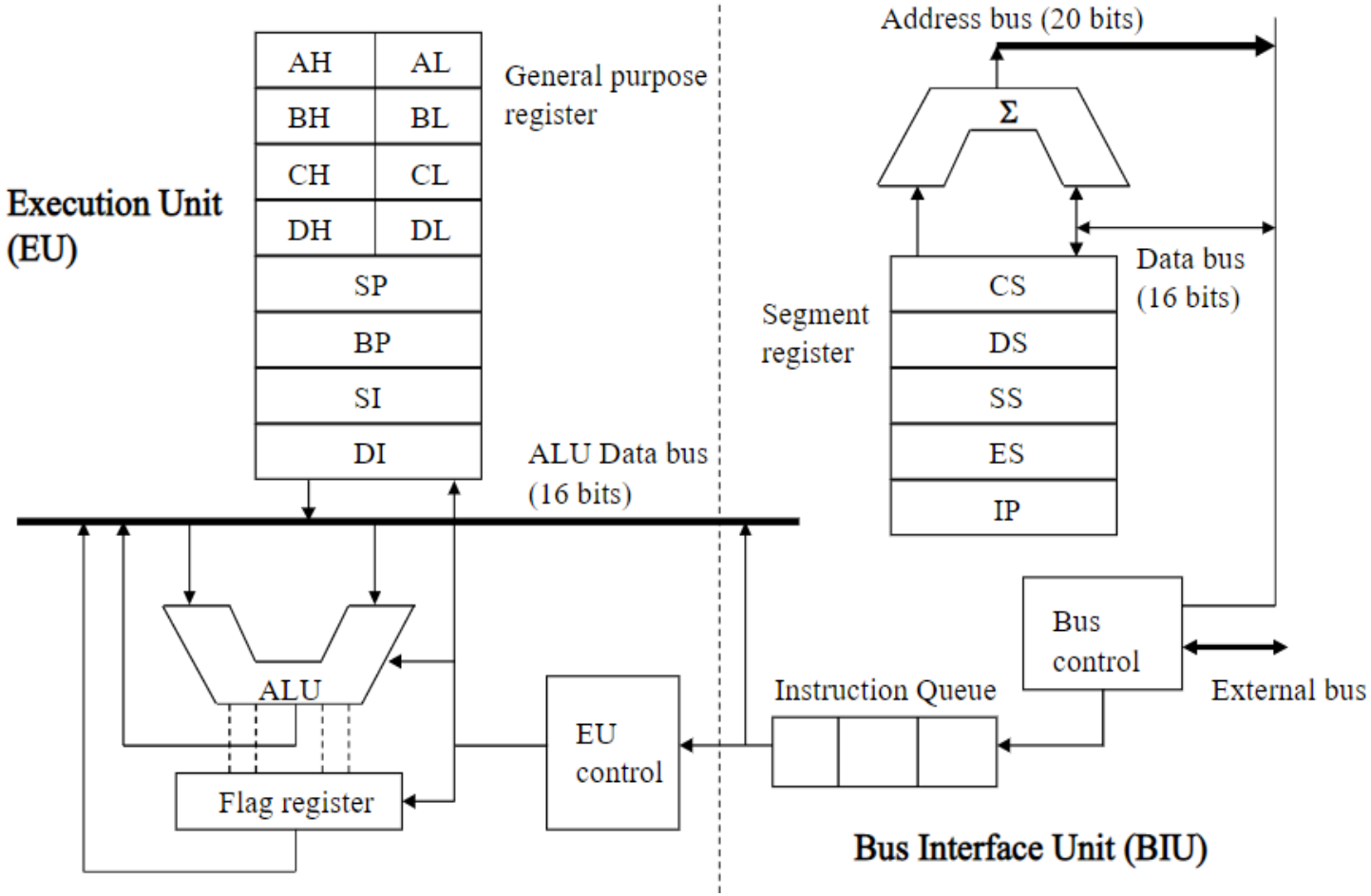
8086 and 8088 Microprocessors

- 8086 announced in 1978; 8086 is a 16 bit microprocessor with a 16 bit data bus
- 8088 announced in 1979; 8088 is a 16 bit microprocessor with an 8 bit data bus
- Both manufactured using High-performance Metal Oxide Semiconductor (HMOS) technology
- Both contain about 29000 transistors
- Both are packaged in 40 pin dual-in-line package (DIP)
- Address lines A0-A7 and Data lines D0-D7 are multiplexed in 8088 –By multiplexed we mean that the same physical pin carries an address bit at one time and the data bit another time
- Address lines A0-A15 and Data lines D0-D15 are multiplexed in 8086

8088 and 8086 Microprocessors



Architecture of 8088



Differences between 8086 and 8088 Microprocessor

8086	8088
The instruction Queue is 6 byte long.	The instruction Queue is 4 byte long.
In 8086, memory divides into two banks -even or lower bank -odd or higher bank	The memory in 8088 does not divide into two banks.
The data bus of 8086 is 16-bit wide	The data bus of 8088 is 8-bit wide.
It has BHE (bar) signal on pin no. 34 & there is no SSO (bar) signal.	It does not have BHE (bar) signal on pin no. 34 & has only SSO (bar) signal. It has no S7 pin.
Control pin in 8086 is M/IO (bar).	Control pin in 8088 is IO/M (bar).
It needs one machine cycle to R/W signal if it is at even location otherwise it needs two.	It needs one machine cycle to R/W signal if it is at even location otherwise it needs two.
In 8086, all address & data Buses are multiplexed.	In 8088, address bus; AD_7- AD_0 buses are multiplexed.
It needs two IC 74343 for de-multiplexing AD_0-AD_{19}.	It needs one IC 74343 for de-multiplexing AD_0-AD_7.
Maximum supply current 360mA.	Maximum supply current 340mA.
Three clock speed: 5, 8, 10 MHz	Two clock speed: 5, 8 MHz

8088

- The complete memory is homogeneously addressed as a bank of 1 Mbyte memory locations using the segmented memory scheme.
- The 8088 can access only a byte at a time. This fact reduces the speed of operation of 8088 as compared to 8086.