Unit -V : Digital Electronics Principles

Design of Counters

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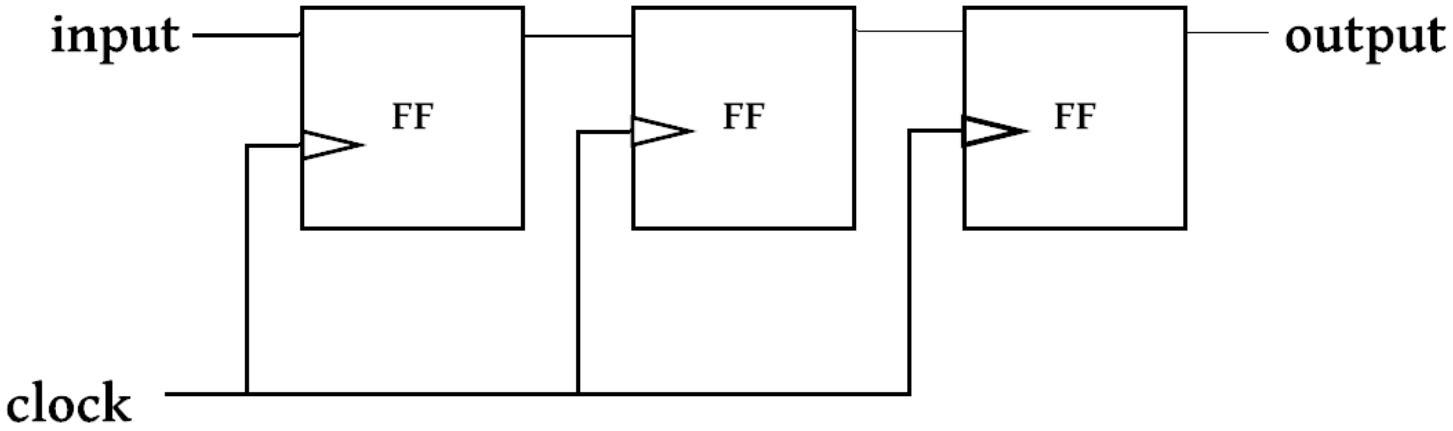
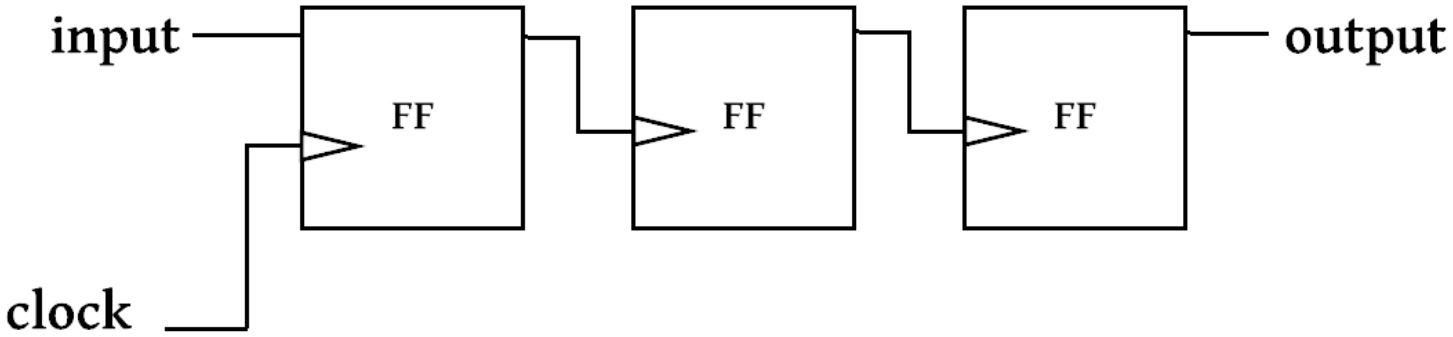
Introduction

- Counters are the basic elements of a digital circuit.
- For every clock pulse, it counts in two different ways, namely
  - *Up count:* 0, 1, 2, 3, ...14, 15.
  - *Down count:* 15, 14, 13, 12, 11, 10, ...2,1,0.
- Designing a counter requires flip flops as it need to record every bit in each clock pulse.
- Two types of counter designs:
  - Asynchronous
  - Synchronous

Types of counter designs



(a) Synchronous design



(b) Asynchronous design

Difference: Asynchronous and Synchronous designs

Asynchronous:

- In this type of design, flip-flops are connected in such a way that output of first flip-flop drives the clock for the next flip-flop.
- All the flip-flops are not clocked simultaneously.
- Logic circuit is very simple even for more number of states.
- *Low speed*: The clock is propagated through number of flip-flops before it reaches last flip-flop.

Synchronous:

- In this type of design, no connection between the output of first flip-flops and the clock input of next flip-flop.
- All the flip-flops are clocked simultaneously.
- Design involves complex logic circuit as the number of states increases.
- *High speed*: The clock is propagated uniformly to all the flip-flops.

Waveform

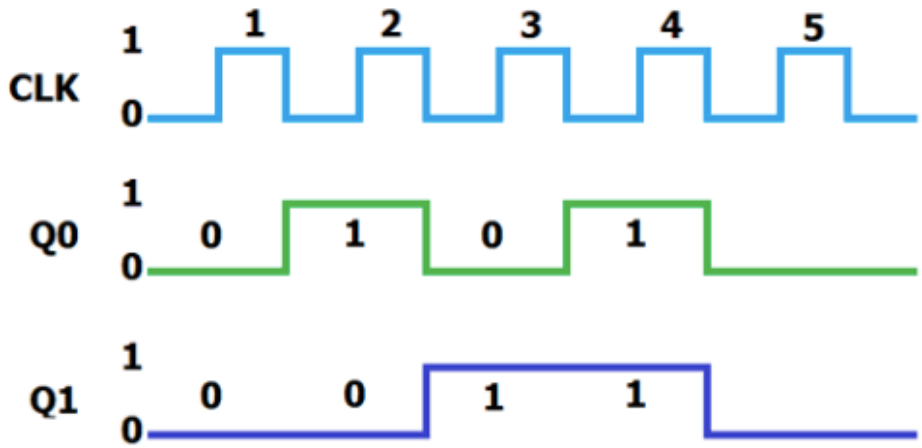


Figure 2: Asynchronous waveform

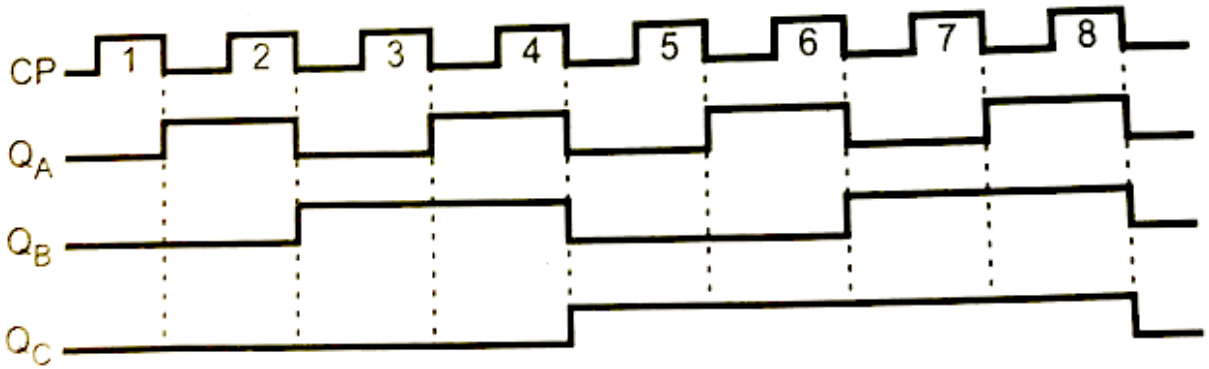


Figure 3: Synchronous waveform

Up/Down Counter

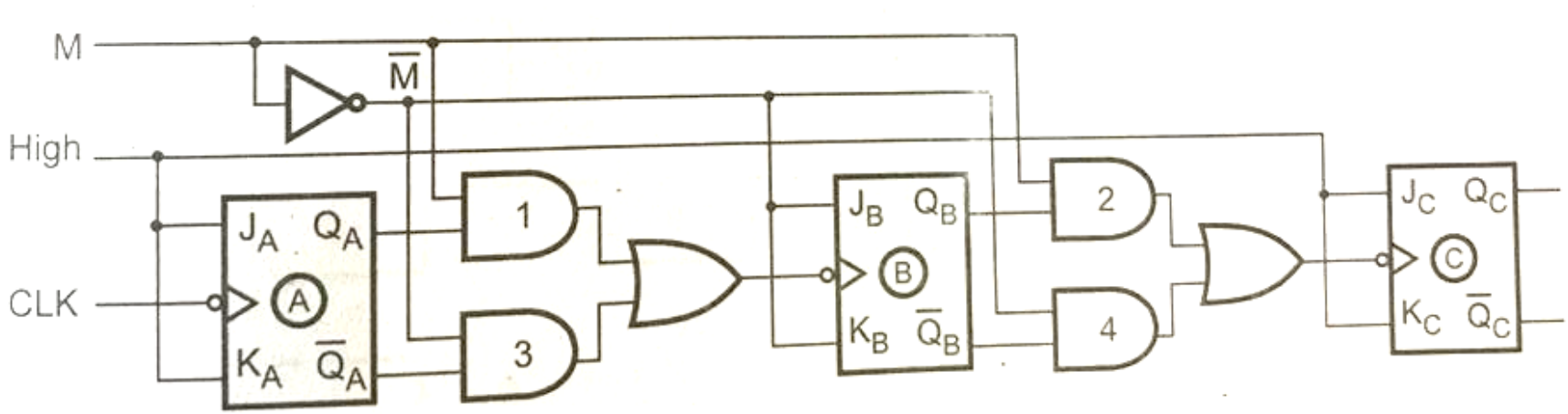


Figure 4: Logic Diagram

Up/Down Counter

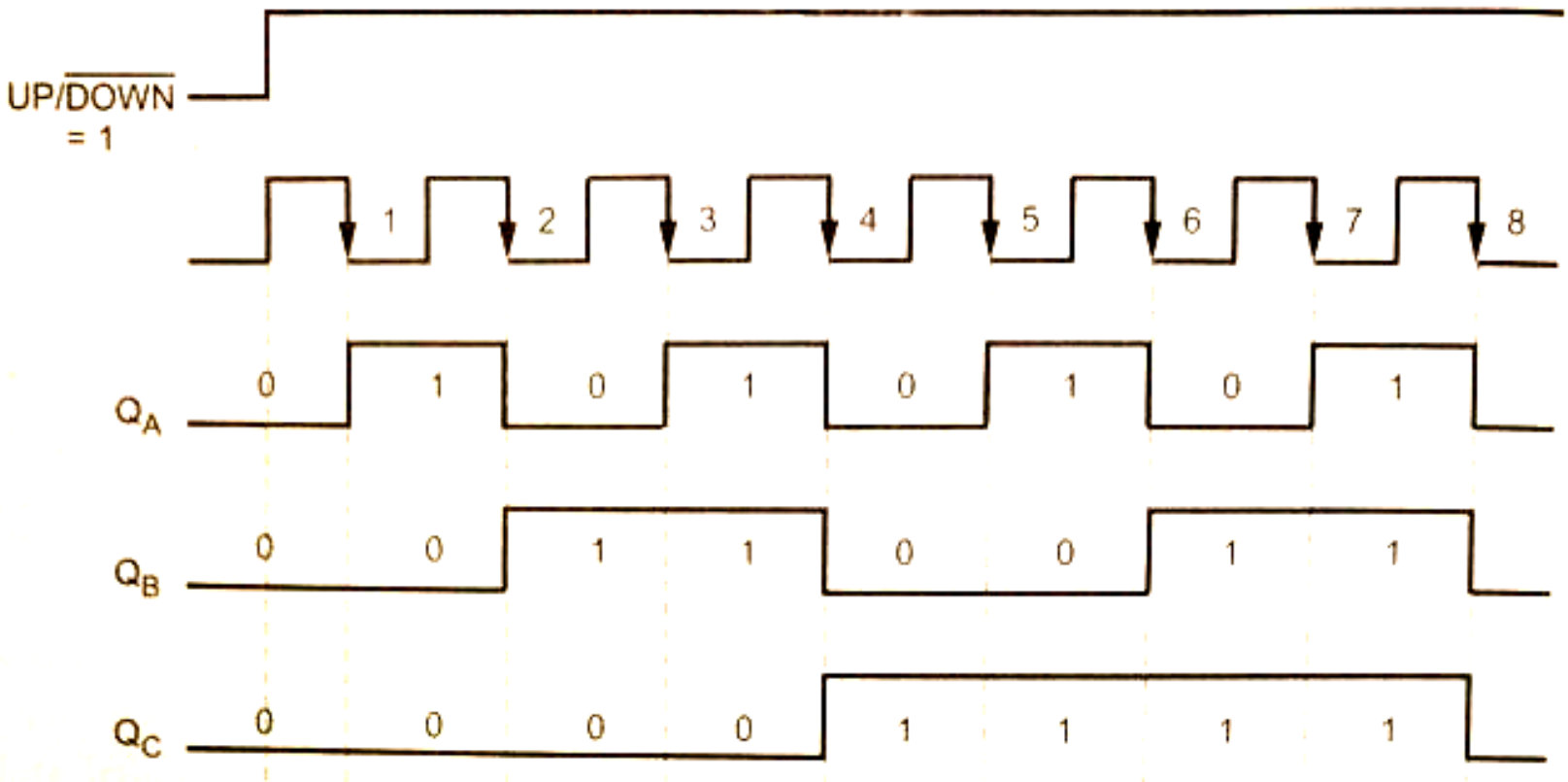
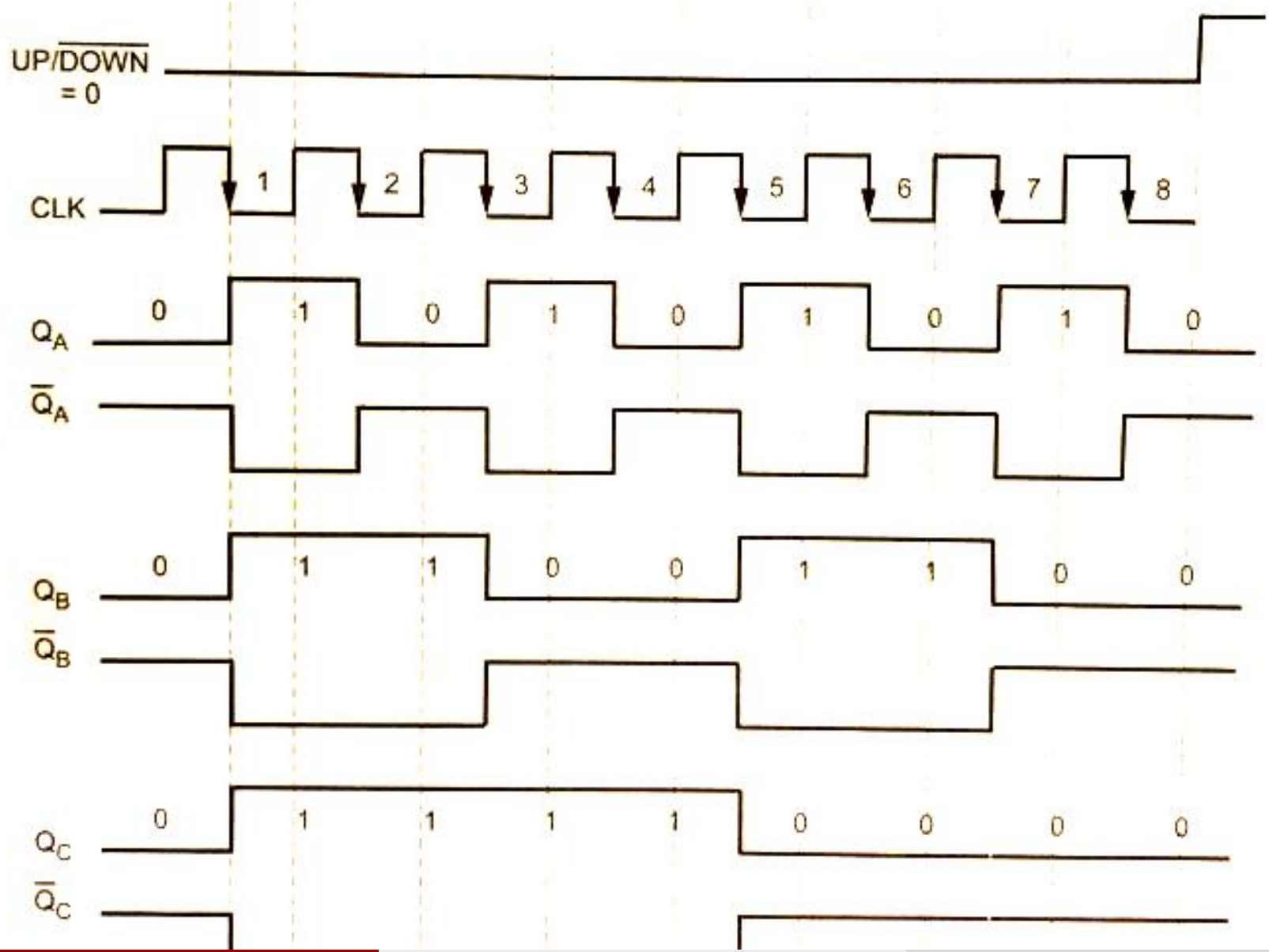


Figure 5: Up-count waveform

Up/Down Counter



Steps to design a Synchronous counter

- It is necessary to first obtain the stable table from the given circuit information.
- Assign binary values to each state in the state table.
- Determine the number of flip flops needed and assign a letter symbol to each state.
- Choose the type of flip flop to be used.
- From the state table , derive the circuit excitation and output tables.
- Using K-map or any other simplification method, derive the circuit output functions and the flip-flop input functions.
- Draw the logic diagram.

Synchronous: Sequence counter

- Design a Synchronous counter using JK flip flop to count the sequence $4 \rightarrow 6 \rightarrow 7 \rightarrow 3 \rightarrow 1 \rightarrow 4...$
- According to $2^n \geq N$. Here, N =7 therefor n =3 flip-flops.

Present state			Next state			Flip flop inputs					
A	B	C	A_{+1}	B_{+1}	C_{+1}	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	1	0	0	1	X	0	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	0	0	1	0	X	X	1	X	0
1	0	0	1	1	0	X	0	1	X	0	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	0	1	1	X	1	X	0	X	0

K -map

	$\overline{B}\,\overline{C}$	$\overline{B}\,C$	B C	B $\overline{C}$
$\overline{A}$	0	1	0	0
A	X	X	X	X

Table 1: $J_A = \overline{B}C$

	$\overline{B}\,\overline{C}$	$\overline{B}\,C$	B C	B $\overline{C}$
$\overline{A}$	X	X	X	X
A	0	0	1	0

Table 2: $K_A = BC$

	$\overline{B}\,\overline{C}$	$\overline{B}\,C$	B C	B $\overline{C}$
$\overline{A}$	0	0	X	X
A	1	1	X	X

Table 3: $J_A = A$

	$\overline{B}\,\overline{C}$	$\overline{B}\,C$	B C	B $\overline{C}$
$\overline{A}$	X	X	1	0
A	X	X	0	0

Table 4: $K_B = \overline{A}C$

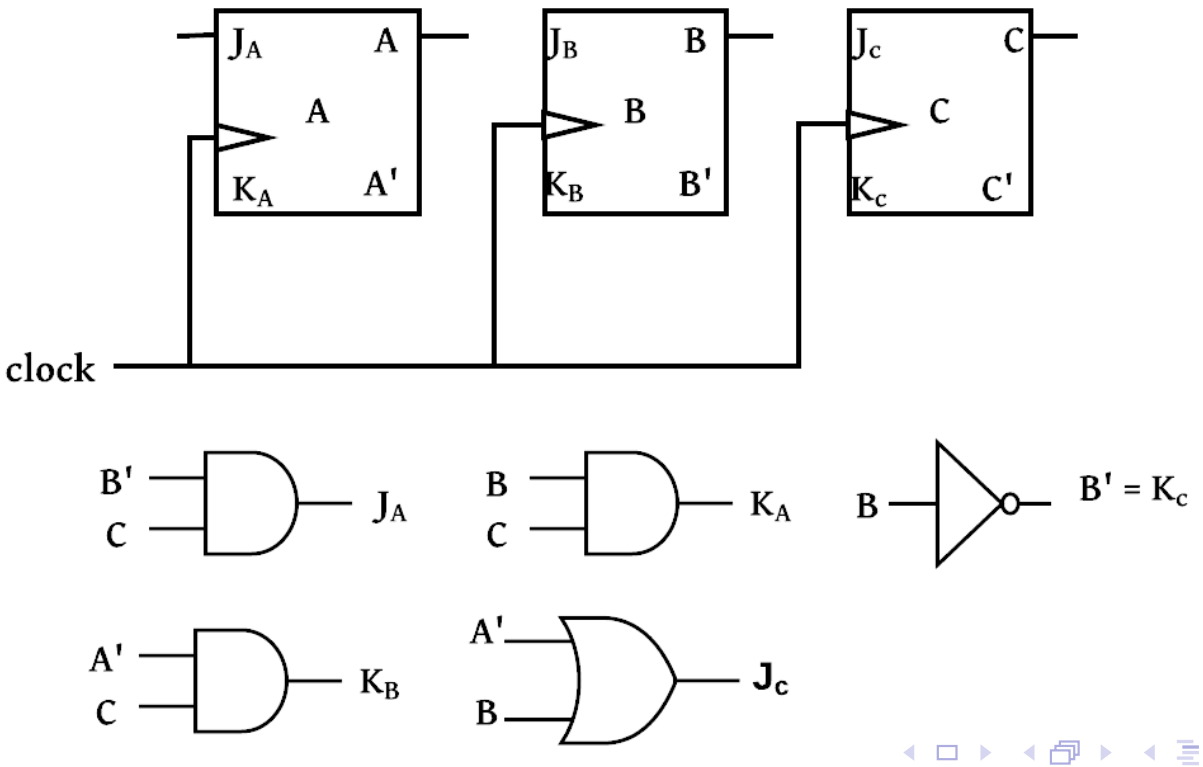
contin..

	$\overline{B}\,\overline{C}$	$\overline{B}\,C$	B C	B $\overline{C}$
$\overline{A}$	1	X	X	1
A	0	X	X	1

Table 5: $J_C = A$

	$\overline{B}\,\overline{C}$	$\overline{B}\,C$	B C	B $\overline{C}$
$\overline{A}$	X	1	0	X
A	X	1	0	X

Table 6: $K_C = \overline{A}C$



Synchronous: Decade counter

- Design a synchronous decade (count till 10 states) counter using D flip-flop.
- According to $2^n \geq N$. Here, N =10 therefor n =4 flip-flops.

Present state				Next state				Flip flop inputs			
A	B	C	D	D_{+1}	C_{+1}	B_{+1}	A_{+1}	D_D	D_C	D_B	D_A
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	0
0	0	1	0	0	0	1	1	0	0	1	1
0	0	1	1	0	1	0	0	0	1	0	0
0	1	0	0	0	1	0	1	0	1	0	1
0	1	0	1	0	1	1	0	0	1	1	0
0	1	1	0	0	1	1	1	0	1	1	1
0	1	1	1	1	0	0	0	1	0	0	0
1	0	0	1	0	0	0	0	0	0	0	0

Decade K-map

For Q_{D+1}

$Q_D Q_C$ \ $Q_B Q_A$	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	X	X	X	X
10	1	0	X	X

$$Q_{D+1} = Q_D\overline{Q}_A + Q_CQ_BQ_A$$

For Q_{C+1}

$Q_D Q_C$ \ $Q_B Q_A$	00	01	11	10
00	0	0	1	0
01	1	1	0	1
11	X	X	X	X
10	0	0	X	X

$$Q_{C+1} = Q_C\overline{Q}_B + Q_C\overline{Q}_A + \overline{Q}_CQ_BQ_A$$

For Q_{B+1}

$Q_D Q_C$ \ $Q_B Q_A$	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	X	X	X	X
10	0	0	X	X

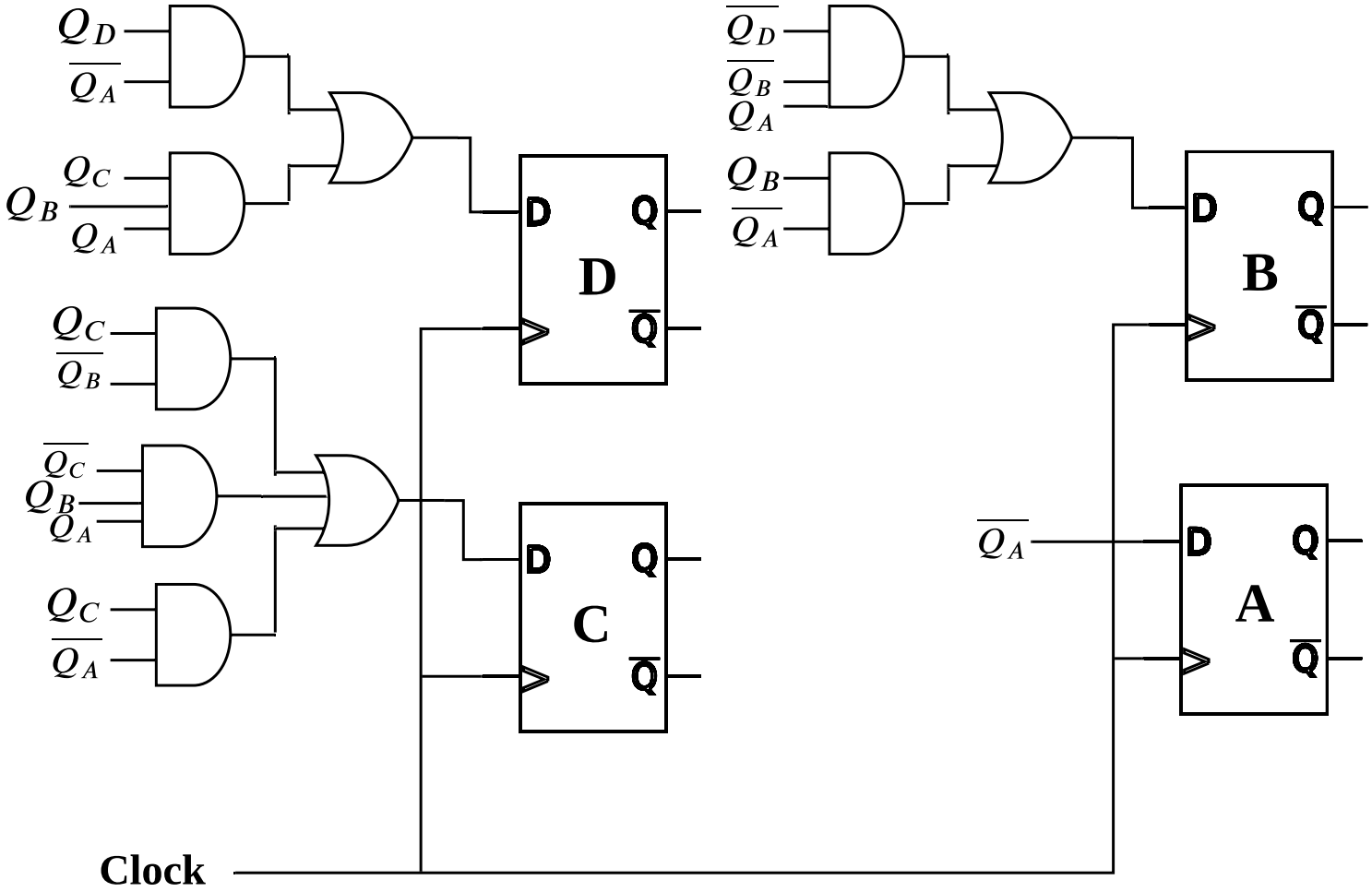
$$Q_{B+1} = \overline{Q}_D\overline{Q}_BQ_A + Q_B\overline{Q}_A$$

For Q_{A+1}

$Q_D Q_C$ \ $Q_B Q_A$	00	01	11	10
00	1	0	0	1
01	1	0	0	1
11	X	X	X	X
10	1	0	X	X

$$Q_{A+1} = \overline{Q}_A$$

Logic diagram



Steps to design a Asynchronous counter

- Determine the number of flip-flops needed.
- Choose the flip-flop to be used.
- Write the truth table for the counter.
- Derive the reset logic by K-map simplification.
- Draw the logic diagram.

Asynchronous: BCD ripple counter using JK Flip flop

- BCD counter goes through states 0-9, i.e. total 10 states. Thus, N = 10, and for $2^n \geq N$, w need n = 4 i.e. 4 flip-flops.

CLK	A	B	C	D	Y
1	0	0	0	0	1
1	0	0	0	1	1
1	0	0	1	0	1
1	0	0	1	1	1
1	0	1	0	0	1
1	0	1	0	1	1
1	0	1	1	0	1
1	0	1	1	1	1
1	1	0	0	0	1
1	1	0	0	1	1

CLK	A	B	C	D	Y
0	1	0	1	0	0
0	1	0	1	1	0
0	1	1	0	0	0
0	1	1	0	1	0
0	1	1	1	0	0
0	1	1	1	1	0

$*Y$ is the output port of the BCD ripple counter

Contin..

- Derive the reset logic expression.

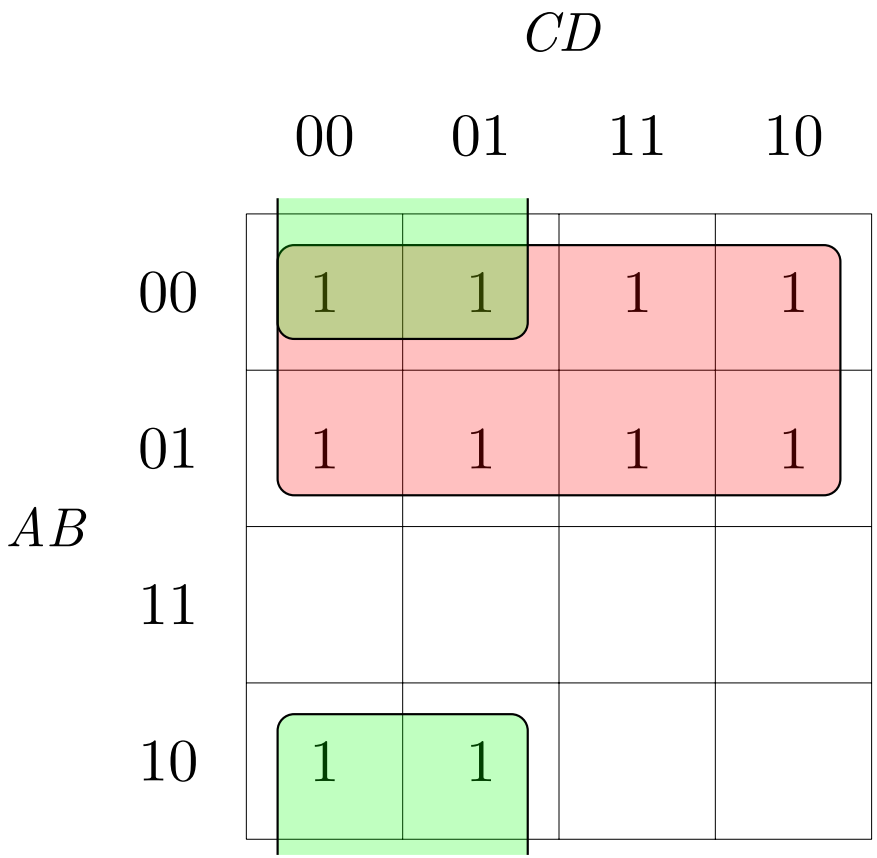
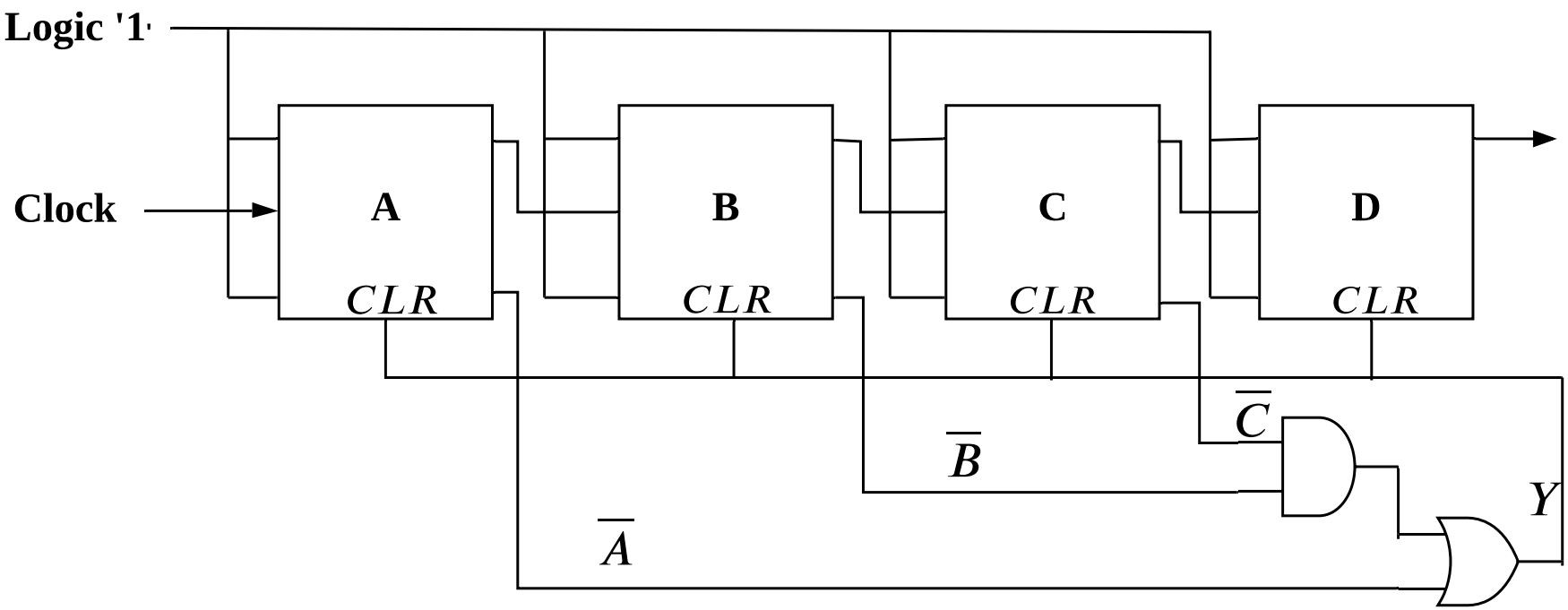


Figure 8: $Y = \overline{A} + \overline{B}\,\overline{C}$


Logic '1'
Clock
A
CLR
B
CLR
C
CLR
D
CLR
$\overline{C}$
$\overline{B}$
$\overline{A}$
Y

Mod-6 ripple counter using T flip-flop

- 0 - 5 states.
- According to $2^n \geq N$. Here, N = 6 therefore n = 3 flip-flops.

Clk	A	B	C	Y
0	0	0	0	1
1	0	0	1	1
2	0	1	0	1
3	0	1	1	1
4	1	0	0	1
5	1	0	1	1
-	1	1	0	0
-	1	1	1	0

K-map

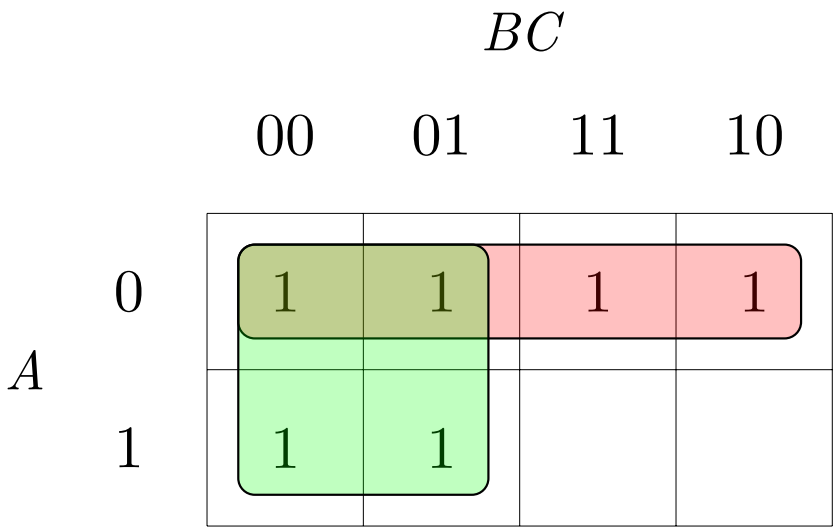


Figure 9: $Y = \overline{A} + \overline{B}$

Logic diagram

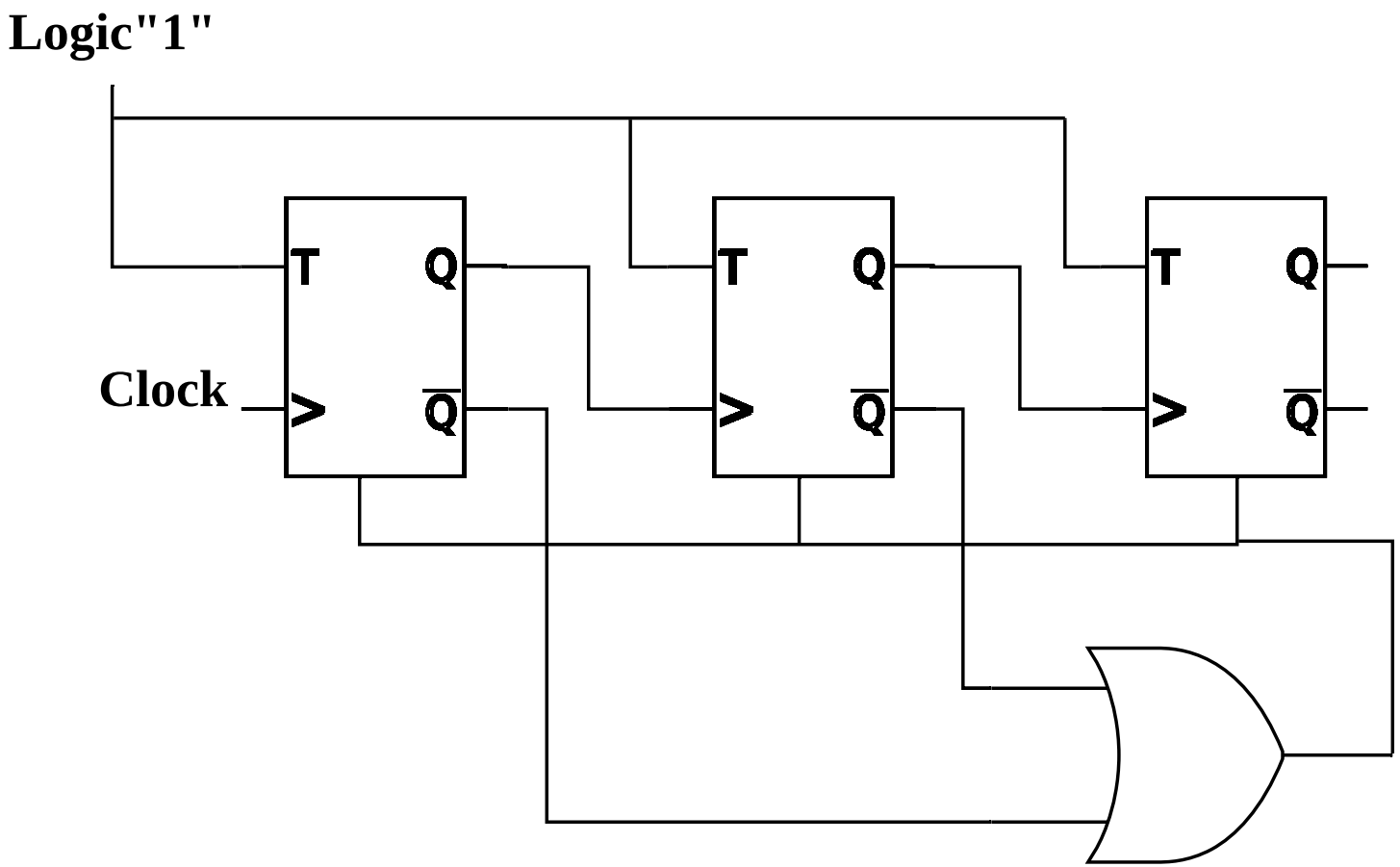


Figure 10: Logic diagram

Ring Counter

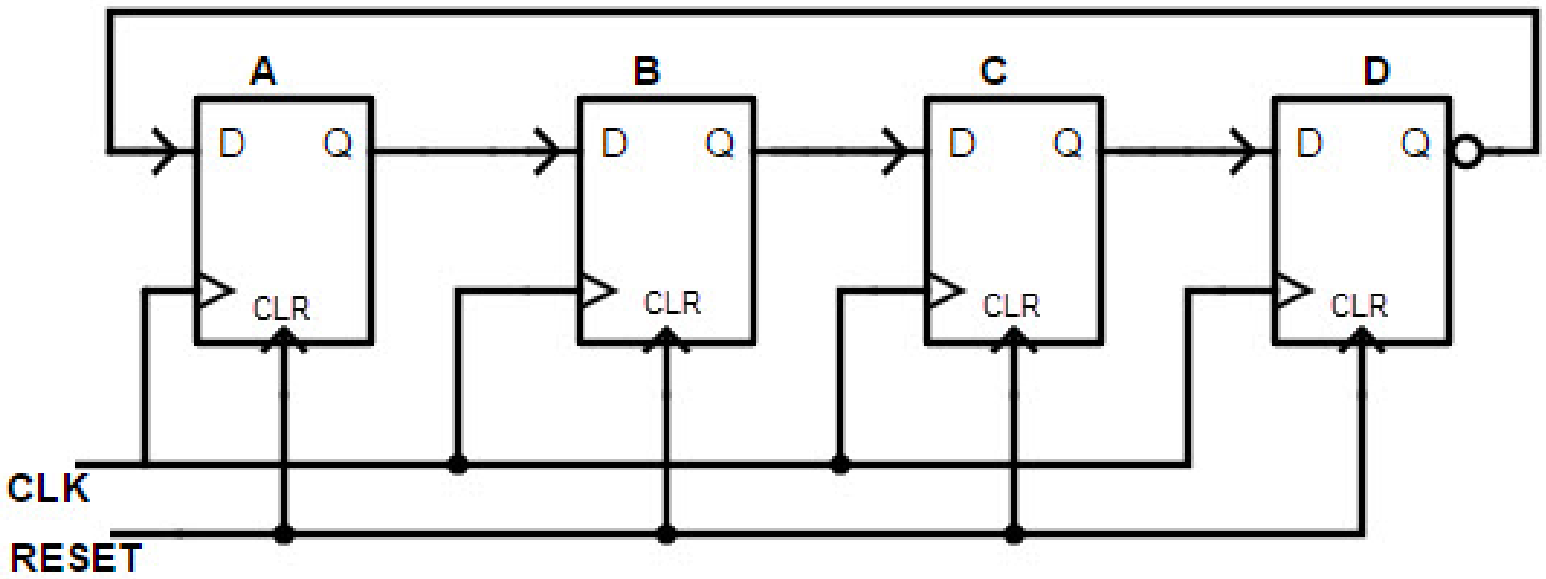


Figure 11: Ring Counter

Johnson Counter

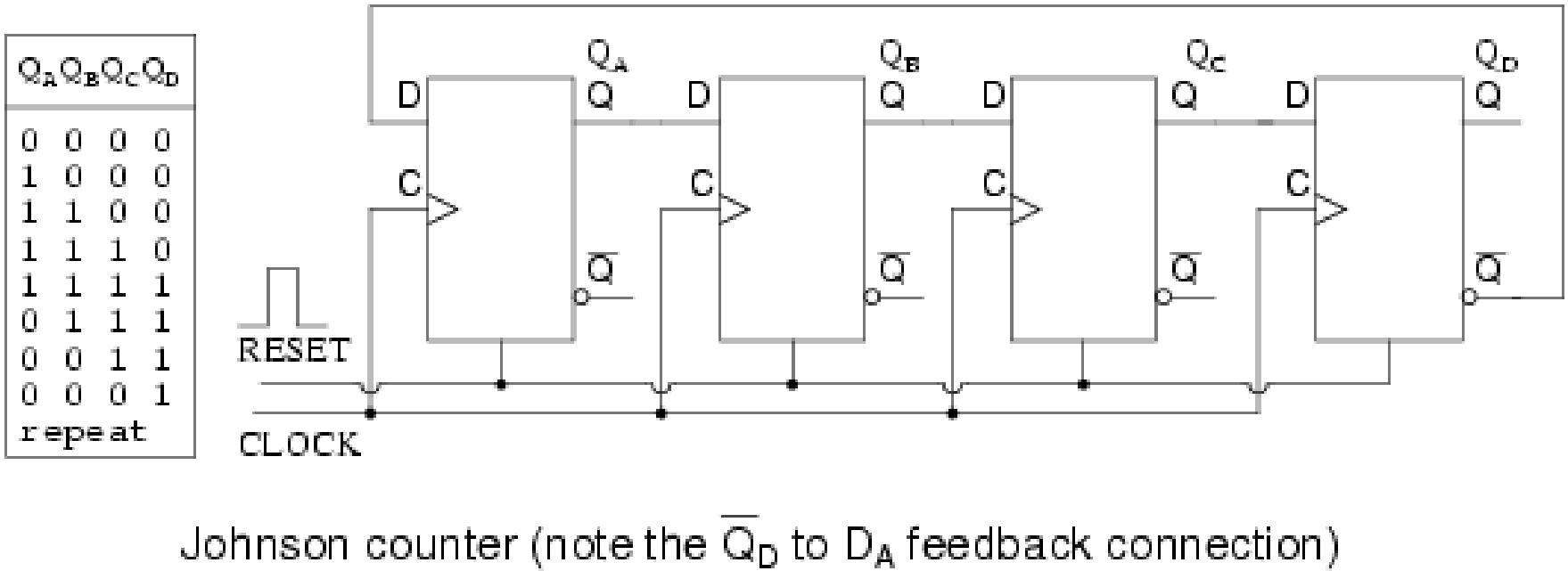


Figure 12: Johnson Counter