SRM Institute of Science and Technology
College of Engineering and Technology

DEPARTMENT OF ECE

SRM Nagar, Kattankulathur – 603203, Chengalpattu District, Tamilnadu

SET A

Academic Year: 2021-2022 (EVEN)

Test: CLAT- 3 **Date: 16-11-2022**
Course Code & Title: 18ECC203J – Microprocessors, Microcontrollers and Interfacing Techniques
Duration: 2 periods
Year & Sem: III/ V **Max. Marks:** 50

Course Articulation Matrix:

	18ECC203J - Microprocessor, Microcontroller and Interfacing Techniques	**Program Outcomes (POs)**														
		Graduate Attributes												**PSO**		
COs	**Course Outcomes (COs)**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**1**	**2**	**3**
CO-1	Apply a basic concept of digital fundamentals to Microprocessor based personal computer system	-	2	-	-	-	-	-	-	-	-	-	-	-	-	-
CO-2	Demonstrate programming proficiency using the various addressing modes of the 8086 microprocessor	-	3	-	-	2	-	-	-	-	-	-	2	-	-	-
CO-3	Develop interfacing techniques using various peripheral chips with microprocessor	-	2	3	-	3	-	-	-	-	-	-	-	-	-	1
CO-4	Evaluate programming proficiency using the various addressing modes of the 8051 microcontroller	-	3	-	-	2	-	-	-	-	-	-	2	-	-	-
CO-5	Construct a system to interface various peripheral chips with microcontroller	-	2	3	-	3	-	-	-	-	-	-	-	-	-	3
CO-6	Implement the practical knowledge through laboratory experiments using microprocessor and microcontroller	-	-	3	-	3	-	-	-	-	-	-	2	1	-	2

Part - A
(10 x 1 = 10 Marks)

Q. No	**Question**	**Marks**	**BL**	**CO**	**PO**
1.	8051 has_____interrupts. a. 3 b. 2 **c. 5** d. 6	**1**	**1**	**4**	**2**
2.	8051 has _____special function register a. 10 b. 15 c. 12 **d. 21**	**1**	**1**	**4**	**2**
3.	Identify an invalid instruction given below. a. MOV A,B **b. MOV R1,R2** c. MOV 40H,A d. MOV A,#05H	**1**	**2**	**4**	**2**
4.	When the 8051 is powered up, the SP register contains _____value. a. 00H b. FFH c. 06H **d. 07H**	**1**	**1**	**4**	**2**
5.	_____ Bytes of locations are set aside for bit-addressable memory. a. 10 **b. 16** c. 13 d. 11	**1**	**1**	**4**	**2**
6.	Timer 0 operates in _____modes. a. 1 b. 3 c. 5 **d. 4**	**1**	**1**	**5**	**3**
7.	SBUF register is _____register. a. 4-bit b. 16-bit	**1**	**1**	**5**	**3**

	c. 12-bit **d. 8-bit**				
8.	PCON register is related to_____. a. Timer b. Counter c. Interrupts **d. Serial port**	**1**	**2**	**5**	**3**
9.	The roll over value of Timer 1 in mode 2 is_____ **a. FFFFH-0000H** b. 1FFFH-0000H c. FFH-00H d. 1FH-00H	**1**	**2**	**5**	**3**
10	To control the timer by software, the _____is set to zero **a. Gate** b. TRx c. TFx d. INT	**1**	**2**	**5**	**3**
	Part – B **(4 x 10 = 40 Marks)**				
	SECTION B1 **Instructions: Answer ANY 2 Questions**				
11	a. Draw the bit pattern of program status word register and explain.	**5**	**2**	**4**	**2**

CY	AC	F0	RS1	RS0	OV	--	P

CY	PSW.7	Carry Flag.
AC	PSW.6	Auxiliary carry flag.
F0	PSW.5	Available to the user for general purpose.
RS1	PSW.4	Register bank selector bit 1.
RS0	PSW.3	Register bank selector bit 0.
OV	PSW.2	Overflow flag.
--	PSW.1	User- definable bit.
P	PSW.0	Parity flag. Set/cleared by hardware each instruction cycle to indicate and Odd/ even number of 1 bit in the accumulator.

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1. CY: the carry flag.

- This flag is set whenever there is a carry out from the D7 bit.
- The flag bit is affected after an 8 bit addition or subtraction.
- It can also be set to 1 or 0 directly by an instruction such as —SETB C and CLR C where SETB C stands for - set bit carry and CLR C for - clear carry.

2. AC: the auxiliary carry flag

- If there is a carry from D3 and D4 during an ADD or SUB operation, this bit is set; it is cleared. This flag is used by instructions that perform BCD (binary coded decimal) arithmetic.

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3. F0: Available to the user for general purposes.

4. RS0, RS1: register bank selects bits

- These two bits are used to select one of the four register banks n internal RAM in the table. By writing zeroes and ones to these bits, a group of registers R0- R7 can be used out of four registers banks in internal RAM.

RS1	RS0	Space in RAM
0	0	Bank 0 (00H- 07H)
0	1	Bank 1 (08H-0FH)
1	0	Bank2 (10H-17H)
1	1	Bank3 (18H-1FH)

5. OV: the overflow flag

- This flag is set whenever the result of a signed number operation is too large, causing the high-order bit to overflow into the sign bit. In general, the carry flag is used to detect errors in unsigned arithmetic operations. The overflow flag is only used to detect errors in signed arithmetic operations.

6. P: Parity flag

- The parity flag reflects the number of 1s in the A (accumulator) register only. If the A register contains an odd number of 1's, then P=1, P=0 if A has an even number of 1's.

	b. Explain in detail about 8051 stack.	**5**	**2**	**4**	**2**

	Stack: The stack is a section of RAM used by the CPU to store information temporarily information could be data or an address. 1. The register used to access the stack is called stack pointer register. 2. Stack is used to store data temporary during any program execution. 3. The 8 bit stack pointer is used to hold an internal RAM address which is called the top of stack. 4. Generally 8051 used bank1 of internal RAM as the stack so the default stack pointer is 07H. 5. The stack pointer in the 8051 only 8 bit wide which means that it can take value of 00 to FFH. 6. When the 8051 is powered up the sp register contain value 07H. 7. RAM location 08H is the first location begin used for the stack by the 8051. 8. When data is retrieved from the stack the byte is read from the stack and then sp register increment. 9. The stack is used during PUSH, POP, CALL, RET instruction. . 10. Stack pointer work on the principal of last ID first output (LIFO).	**5M**			
12	a. Write the single instruction to perform the following operations. **i.** To change the contents of accumulator from 85H in to 58H--------**SWAP A,** ii. To set the carry flag------**SETB C** **iii.** To set any bit---------**SETB BIT** **iv.** Logical instruction to copy the content FFH into accumulator-----**ORL A,FFH**	**4** **Each 1M**	**3**	**4**	**2**

	b. Show the code to push R5 and A on to the stack and pop back them into R2 and B, Where B=A and R2=R5. Also show the stack and SP value after pushing content on to stack. Assume the default stack area.
	`PUSH 05 ;push R5 onto stack`
	`PUSH 0E0H ;push register A onto stack`
	`POP 0F0H ;pop top of stack into B`
	`;now register B = register A`
	`POP 02 ;pop top of stack into R2`
	`;now R2=R6`
		6
		3M
			4	**4**	**2**

	Stack / **PUSH 05** / **PUSH 0E0** OB / 0B / 0B 0A / 0A / 0A 09 / 09 / 09 08 / 08 / 08 Start SP=07 / SP=08 / SP=09	**3M**			
13	a. Identify the addressing modes and comment on it. i. MOV A,B----**Register addressing mode** Uses registers to hold the data(operand) to be manipulated ii. MOVC A,@A+PC----**Indexed addressing** The MOVC instruction moves a byte from the code or program memory to the accumulator. The address of an operand is specified in PC and A. **iii.** MOV 40H,40H--------**Direct addressing**	**10** **Each 2M**	**3**	**4**	**2**

		The address of an operand to be manipulated is directly given as operand in an instruction. iv. MOV A,#05H-----**Immediate addressing** Operand to be manipulated is directly specified as constant or immediate number in an instruction. **v.** MOVX A,@DPTR----**External Direct/Indexed Addressing** The MOVX instruction moves a byte from the external data memory to the accumulator. The address of an operand is specified in DPTR.				
SECTION B2 **Instructions: Answer ANY 2 Questions**						
14	Interface an EPROM of size 4kB and RAM size of 8kB with 8051. The EPROM address starts at 0000H and RAM address starts at 8000H.		**10**	**3**	**5**	**3**

Determination of Address lines for EPROM and ROM

Solution

Available EPROM–4 KB = 2^{12}
Address lines with EPROM chip = 12 i.e. A_0–A_{11}
Available RAM–8 KB = 2^{13}
Address lines with RAM chip = 13 i.e. A_0–A_{12}

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Address map for EPROM and RAM

EPROM Address Map

Hex Address	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	size
0000H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4 KB
0FFFH	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	

RAM Address Map

Hex Address	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
8000H	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9FFFH	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1

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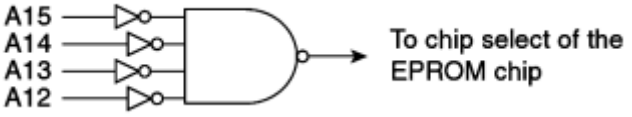
Chip Select of the EPROM



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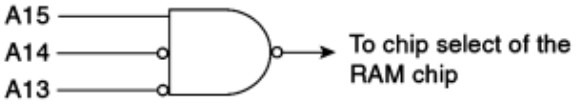
Chip select of the RAM



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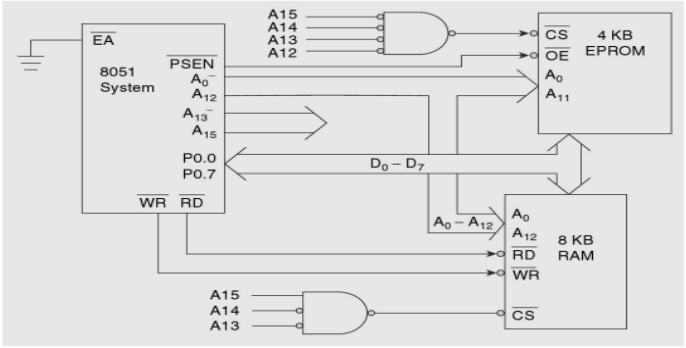
Interfacing Diagram



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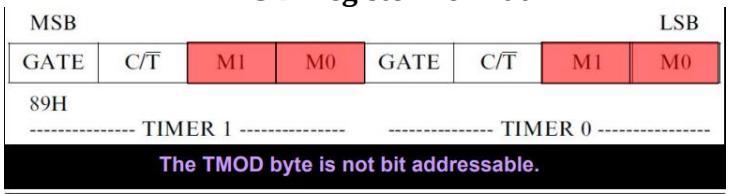
15	a. Indicate which mode and which timer is selected for the following. i. MOV TMOD,#01H ii. MOV TMOD,#20H iii. MOV TMOD,#12H **TMOD Register Format**  The TMOD byte is not bit addressable. M1 M0 Operation 0 0 8048 8-bit timer TLx serves as 5-bit prescaler 0 1 16-bit timer/counter. THx and TLx are cascaded. No prescaler 1 0 8-bit autoreload timer/counter. THx contents loaded into TLx when it overflows 1 1 TL0 is 8-bit counter controlled by timer 0 control bits. TH0 is 8-bit timer controlled by timer 1 control bits 1 1 Timer 1 off **Convert the given TMOD value from hex to binary. Use TMOD register format to determine mode of operation and Timer.** i. TMOD=00000001, Mode 1 of Timer 0 is selected. ii. TMOD=00100000, Mode 2 of Timer 1 is selected. iii. TMOD=00010010, Mode 2 of Timer 0, and Mode 1 of Timer 1 are selected. b. Explain the function of SBUF register. SBUF is an 8-bit register used solely for serial communication. For a byte data to be transferred via the TxD line, it must be placed in the SBUF register. The moment a byte is written into SBUF, it is framed with the start and stop bits and transferred serially via the TxD line. SBUF holds the byte of data when it is received by 8051 RxD line. When the bits are received serially via RxD, the 8051 deframes it by eliminating the stop and start bits, making a byte out of the data received, and then placing it in SBUF.	**6** **2M** **4M** **4** **4M**	**3** **2**	**5** **5**	**3** **3**
16	a. Write the programming steps to transmit and receive the data for serial communication. **Programming the 8051 to transfer data serially** In programming the 8051 to transfer character bytes serially, the following steps must be taken. 1. The TMOD register is loaded with the value 20H, indicating the use of Timer 1 in mode 2 to set the baud rate. 2. The TH1 is loaded with one of the values in Table (2) to set the baud rate for serial data transfer. 3. The SCON register is loaded wit the value 50H, indicating serial mode 1, where an 8-bit data is framed with start and stop bits. 4. TR1 is set to 1 to start Timer 1.	**10** **5M**	**3**	**5**	**3**

	5. TI is cleared by the "CLR TI" instruction . 6. The character byte to be transferred serially is written into the SBUF register. 7. The TI flag bit is monitored with the use of the instruction "JNB TI, xx" to see if the character has been transferred completely. 8. To transfer the next character, go to Step 5. **Programming the 8051 to receive data serially** In programming the 8051 to transfer character bytes serially, the following steps must be taken. 1. The TMOD register is loaded with the value 20H, indicating the use of Timer 1 in mode 2 to set the baud rate. 2. TH1 is loaded with one of the values in Table(2) to set the baud rate. 3. The SCON register is loaded with the value 50H, indicating serial mode 1, where 8-bit data is framed with start and stop bits and receive enable is turned on. 4. TR1 is set to 1 to start Timer 1. 5. RI is cleared with the "CLR RI" instruction. 6. The RI flag bit is monitored with the use of the instruction "JNB RI, xx" to see if an entire character has been received yet. 7. When RI is raised, SBUF has the byte. Its contents are moved into safe place. 8. To receive the next character, go to Step 5.	**5M**			