18ECC203J – Module 3

8086 Interfacing with Memory and Programmable Devices

S – 11, 12, 13

S – 11

Programmable Keyboard / Display Controller 8279 & Interfacing 8279 with 8086 and programming

Why 8279?

- Interfacing keyboards and displays can be done using 8255.
- ISSUE is processor has to refresh the display and check the status of the keyboard periodically using polling technique.
- DISADVANTAGE: A considerable amount of CPU time is wasted, reducing the system operating speed.
- Intel's 8279 is a general purpose keyboard display
- 8279 controller can simultaneously drives the display of a system and interfaces a keyboard with the CPU.
- ADVANTAGE: CPU left free for its routine task (computing).

Components of 8279

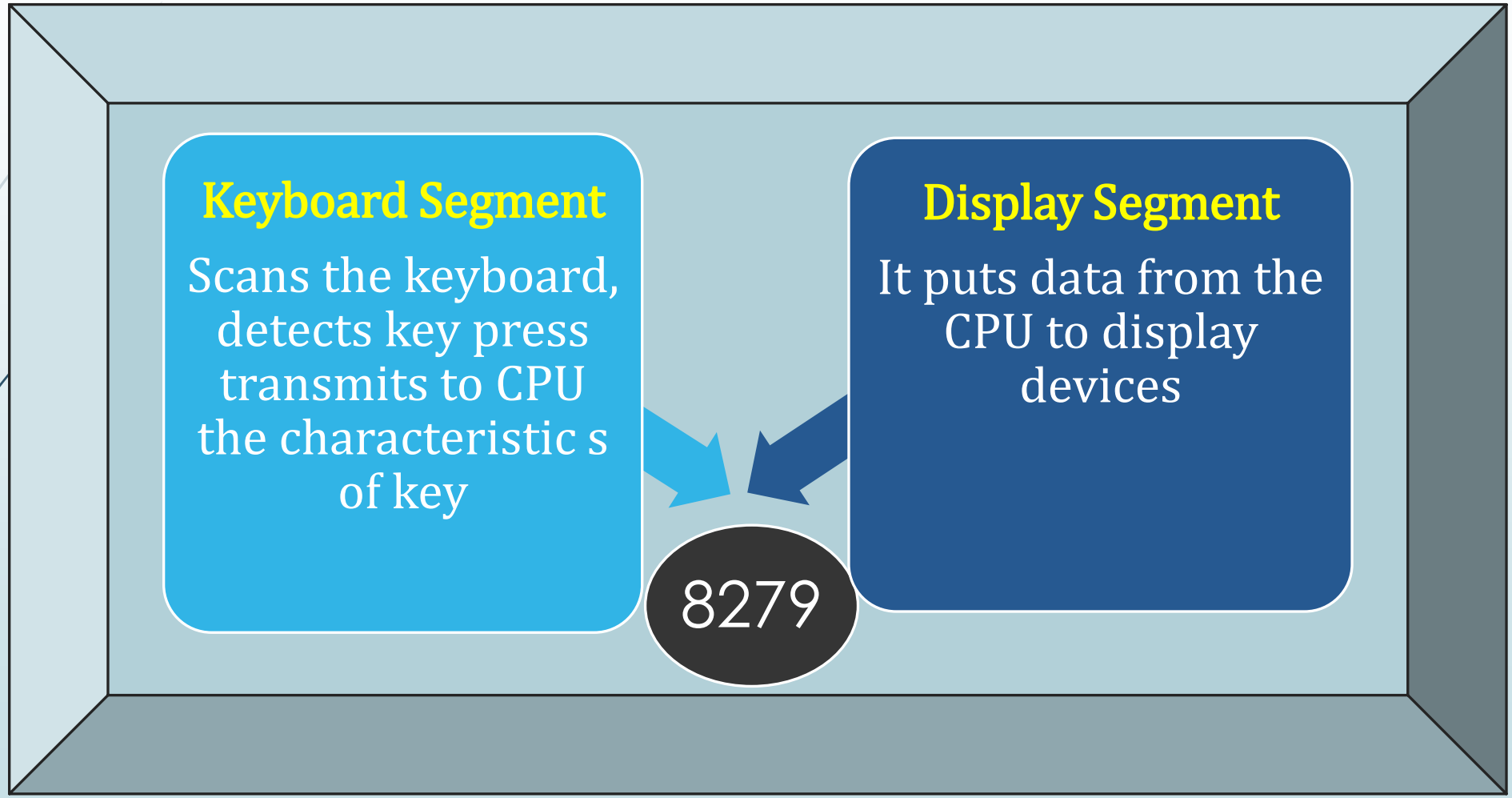


Image Courtesy: Google

Functions of 8279

Keyboard segment

- Connected to a 64 contact key matrix
- Keyboard entries and debounced and stored in FIFO
- Interrupt signal is generated with each entry

Display segment

- 16 character scanned display
- 16x8 R/W memory (RAM)
- Right entry or left entry

Image Courtesy: Google

8279 interface

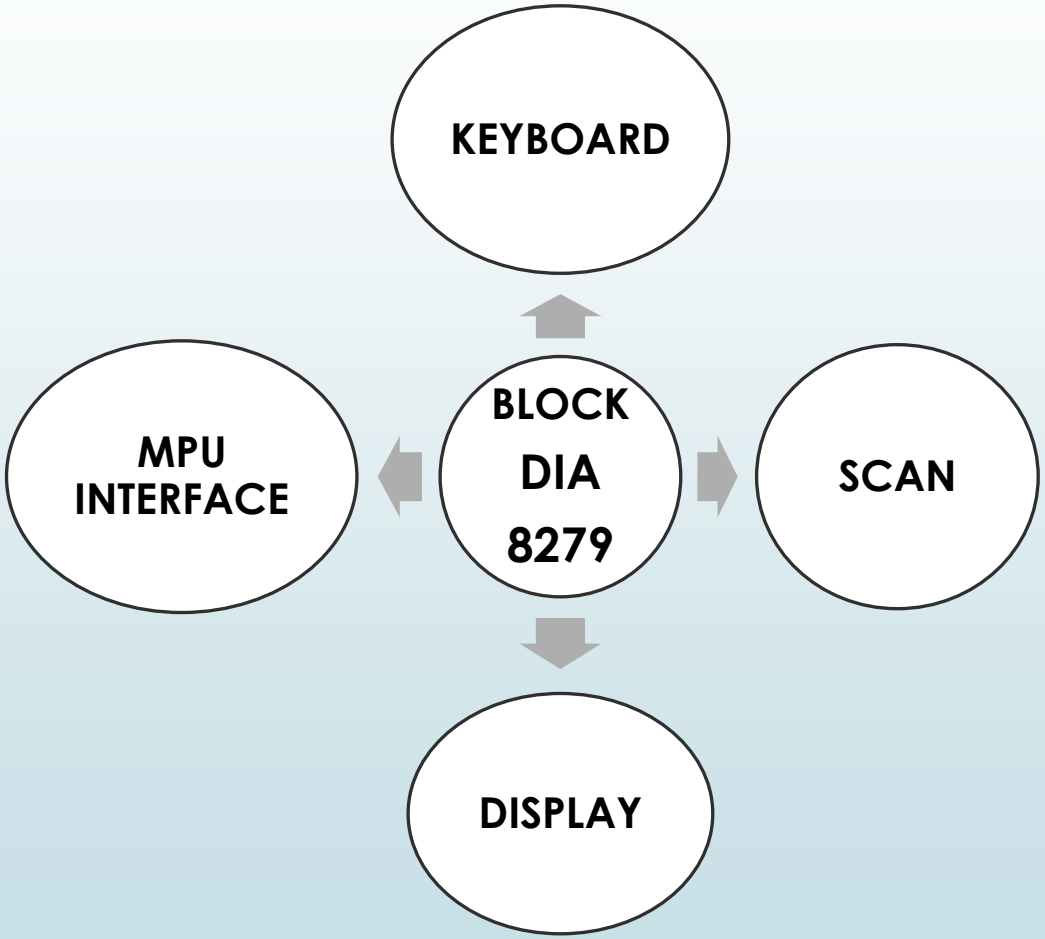


Image Courtesy: Google

8279 Block Diagram

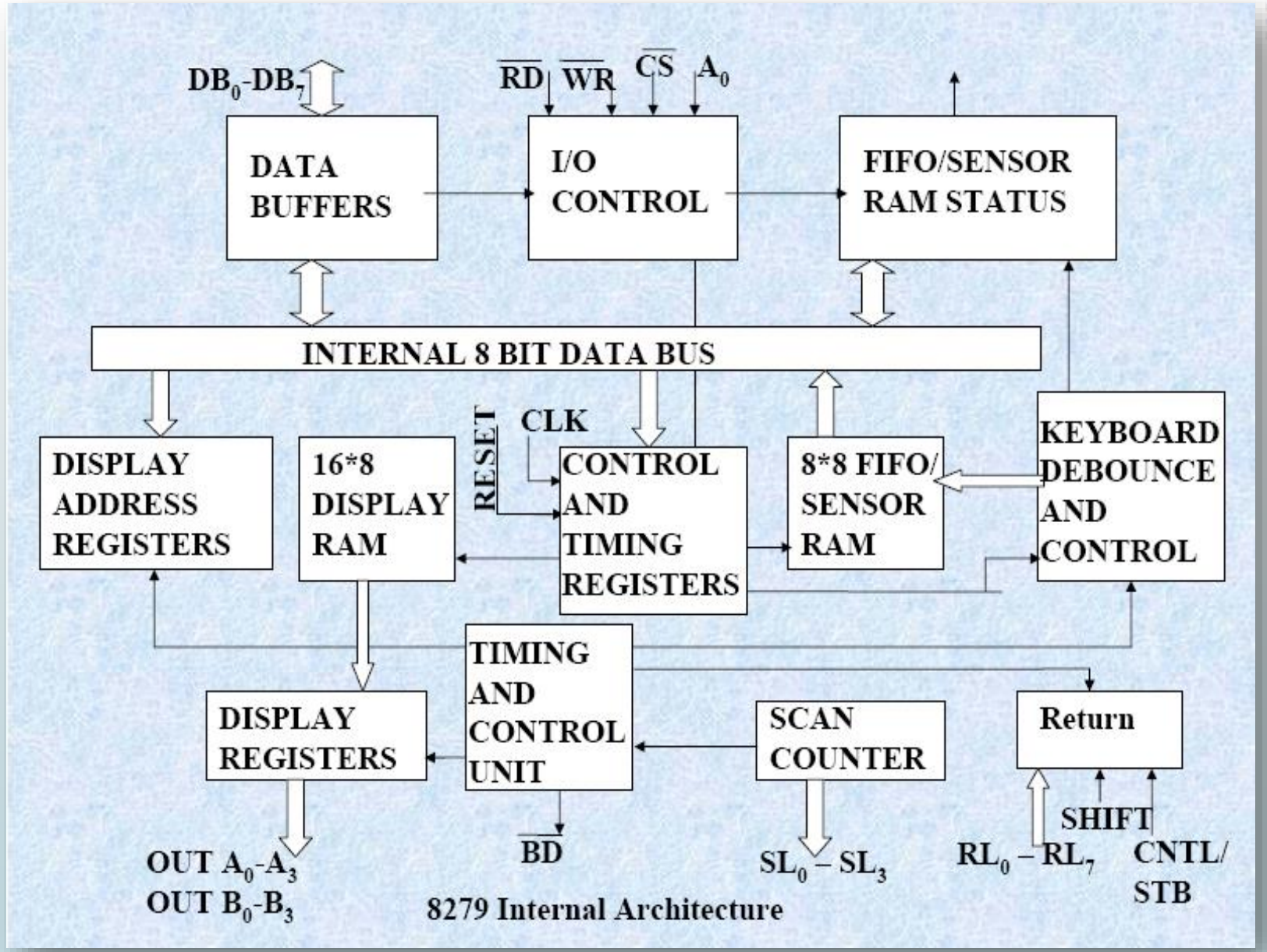


Image Courtesy: Google

Architecture of 8279

- The keyboard display controller chip 8279 provides following lines
- A set of 4 scan lines and 8 return lines for interfacing keyboard
- A set of 8 output lines for interfacing display

Image Courtesy: Google

8279 – Control lines

I/O Control and Data Buffers

- The I/O control section controls the flow of data to/from the 8279
- The I/O section is enabled only if CS is low.
- The pins A0, RD and WR select the command, status or data read/write operations carried out by the CPU with 8279.
- The data buffers interface the external bus of the system with internal bus of 8279.

Control and Timing Register and Timing Control :

- These registers store the keyboard and display modes and other operating conditions programmed by CPU.
- The registers are written with A0=1 and WR=0. The Timing and control unit controls the basic timings for the operation of the circuit.
- Scan counter divide down the operating frequency of 8279 to derive scan keyboard and scan display frequencies.

Scan Counter

- The scan counter has **two modes** to scan the key matrix and refresh the display.
- In the **encoded mode**, the counter provides binary count that is to be externally decoded to provide the scan lines for keyboard and display
- Four externally decoded scan lines may drive upto 16 displays.
- In the **decode scan mode**, the counter internally decodes the least significant 2 bits and provides a decoded 1 out of 4 scan on SL0-SL3
- Four internally decoded scan lines may drive upto 4 displays.
- The keyboard and display both are in the same mode at a time.

Return Buffers and Display RAM

Return Buffers and Keyboard De-bounce and Control:

- This section scans for a key closure row wise. If a key closer is detected, the keyboard debounce unit debounces the key entry (i.e. wait for 10 ms).
- After the debounce period, if the key continues to be detected, The code of key is directly transferred to the sensor RAM along with SHIFT and CONTROL key status.

Display Address Registers and Display RAM :

- The display address register holds the address of the word currently being written or read by the CPU to or from the display RAM.
- The contents of the registers are automatically updated by 8279 to accept the next data entry by CPU.

FIFO/Sensor RAM and Status Logic

In keyboard or strobed input mode, this block acts as 8-byte first-in-first out (FIFO) RAM

- Each key code of the pressed key is entered in the order of the entry and in the mean time read by the CPU, till the RAM become empty.
- The status logic generates an interrupt after each FIFO read operation till the FIFO is empty.

In scanned sensor matrix mode, this unit acts as sensor RAM.

- Each row of the sensor RAM is loaded with the status of the corresponding row of sensors in the matrix.
- If a sensor changes its state, the IRQ line goes high to interrupt the CPU.

.

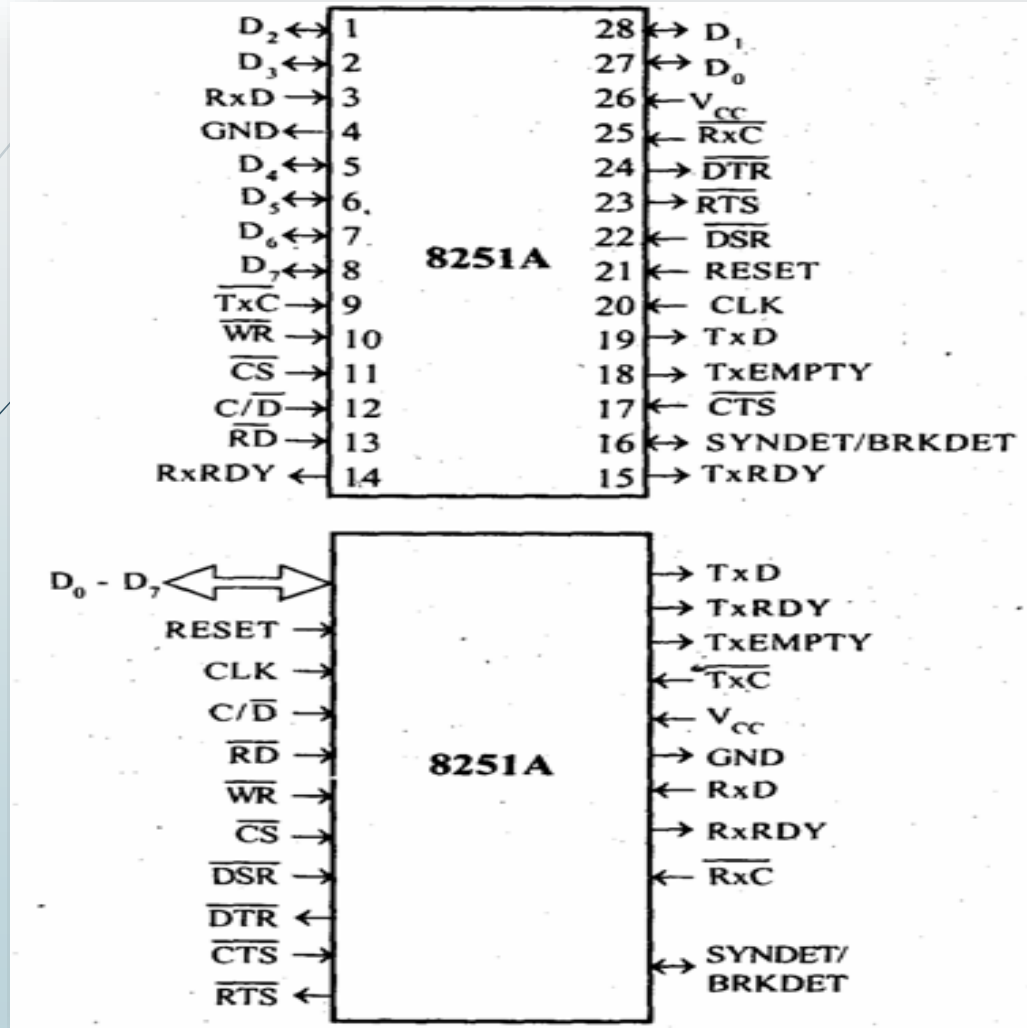
S – 12

Programmable Communication Interface 8251 USART & Interfacing 8251 with 8086 and programming

8251

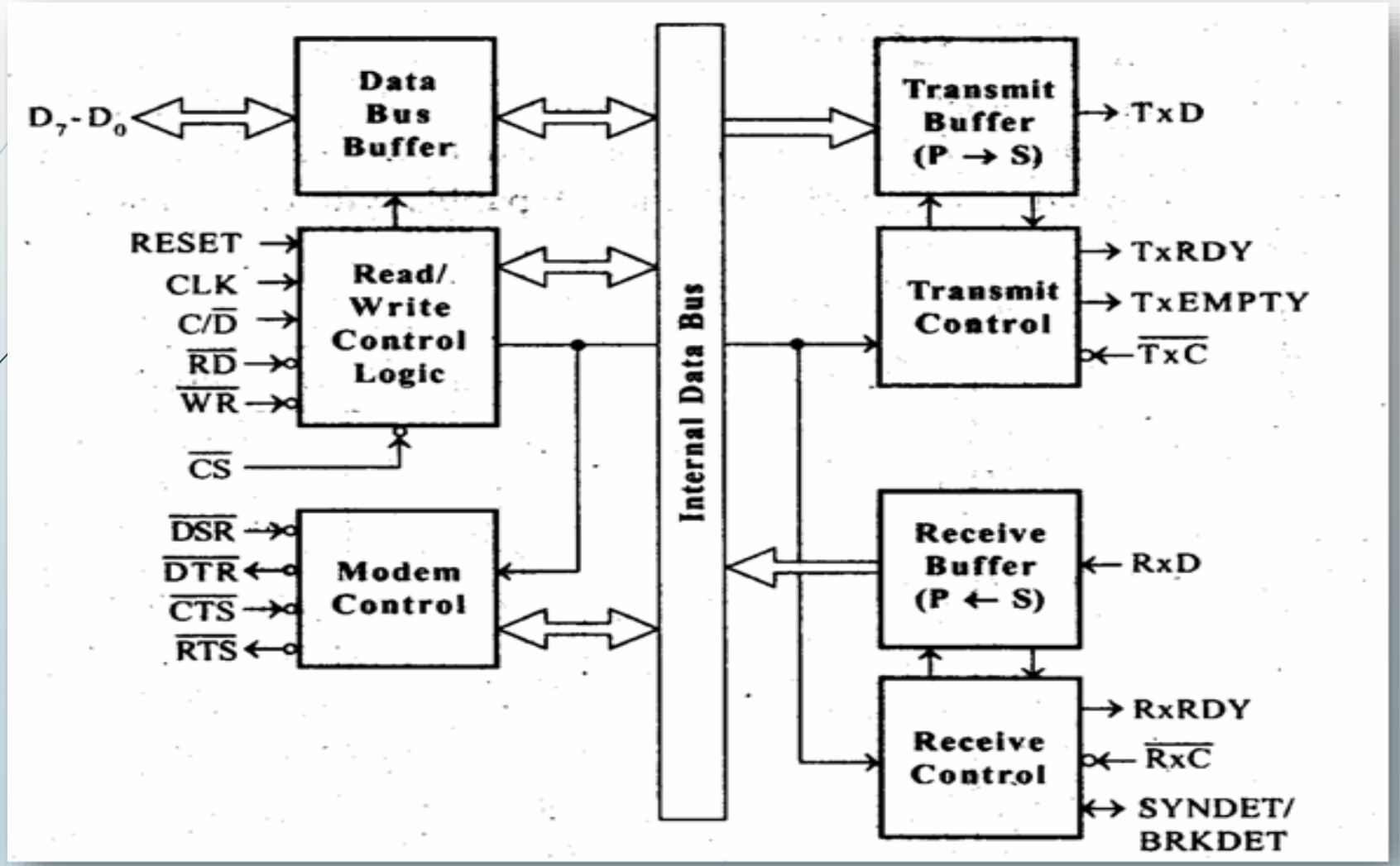
- The 8251A is a programmable serial communication interface chip designed for synchronous and asynchronous serial data communication.
- It supports the serial transmission of data.
- It is packed in a 28 pin DIP.

8251 – Pin Details



Pin	Description
D_0-D_7	Parallel data
C/$\overline{D}$	Control register or Data buffer select
$\overline{RD}$	Read control
$\overline{WR}$	Write control
$\overline{CS}$	Chip Select
CLK	Clock pulse (TTL)
RESET	Reset
$\overline{TxC}$	Transmitter Clock
TxD	Transmitter Data
$\overline{RxC}$	Receiver Clock
RxD	Receiver Data
RxRDY	Receiver Ready
TxRDY	Transmitter Ready
$\overline{DSR}$	Data Set Ready
$\overline{DTR}$	Data Terminal Ready
SYNDET/ BRKDET	Synchronous Detect / Break Detect
$\overline{RTS}$	Request To Send Data
$\overline{CTS}$	Clear To Send Data
TxEMPTY	Transmitter Empty
V_{CC}	Supply (+5V)
GND	Ground (0 V)

8251 – Architecture



8251 Architecture - Explanation

- The functional block diagram of 825 1A consists five sections.

They are:

- Read/Write control logic
- Transmitter
- Receiver
- Data bus buffer
- Modem control.

Read/Write control logic

- The Read/Write Control logic interfaces the 8251A with CPU, determines the functions of the 8251A according to the control word written into its control register.
- It monitors the data flow.
- This section has three registers and they are control register, status register and data buffer.
- The active low signals RD, WR, CS and C/D(Low) are used for read/write operations with these three registers.

Read/Write control logic (2)

- When C/D(low) is high, the control register is selected for writing control word or reading status word.
- When C/D(low) is low, the data buffer is selected for read/write operation.
- When the reset is high, it forces 8251A into the idle mode.
- The clock input is necessary for 8251A for communication with CPU and this clock does not control either the serial transmission or the reception rate.

Transmitter

- The transmitter section accepts parallel data from CPU and converts them into serial data.
- The transmitter section is double buffered, i.e., it has a buffer register to hold an 8-bit parallel data and another register called output register to convert the parallel data into serial bits.
- When output register is empty, the data is transferred from buffer to output register. Now the processor can again load another data in buffer register. If buffer register is empty, then TxRDY is goes to high.
- If output register is empty then TxEMPTY goes to high.
- The clock signal, TxC (low) controls the rate at which the bits are transmitted by the USART.
- The clock frequency can be 1,16 or 64 times the baud rate.

Receiver

- The receiver section accepts serial data and convert them into parallel data
- The receiver section is double buffered, i.e., it has an input register to receive serial data and convert to parallel, and a buffer register to hold the parallel data.
- When the RxD line goes low, the control logic assumes it as a START bit, waits for half a bit time and samples the line again.
- If the line is still low, then the input register accepts the following bits, forms a character and loads it into the buffer register.

Receiver (2)

- The CPU reads the parallel data from the buffer register.
- When the input register loads a parallel data to buffer register, the RxRDY line goes high.
- The clock signal RxC (low) controls the rate at which bits are received by the USART.
- During asynchronous mode, the signal SYNDET/BRKDET will indicate the break in the data transmission.
- During synchronous mode, the signal SYNDET/BRKDET will indicate the reception of synchronous character.

Modem Control

- The MODEM control unit allows to interface a MODEM to 8251A and to establish data communication through MODEM over telephone lines.
- This unit takes care of handshake signals for MODEM interface.
- The 8251A can be memory mapped (OR) I/O mapped
- Using a 3-to-8 decoder generates the chip select signals for I/O mapped devices.
- The address lines A4, A5 and A6 are decoded to generate eight chip select signals (IOCS-0 to IOCS-7) and in this, the chip select signal IOCS-2 is used to select 8251A.

Modem control (2)

- The address line A7 and the control signal IO / M(low) are used as enable for decoder.
- The address line A0 of 8085 is connected to C/D(low) of 8251A to provide the internal addresses.
- The data lines D0 - D7 are connected to D0 - D7 of the processor to achieve parallel data transfer.
- The RESET and clock signals are supplied by the processor. Here the processor clock is directly connected to 8251A. This clock controls the parallel data transfer between the processor and 8251A.
- The output clock signal of 8085 is divided by suitable clock dividers like programmable timer 8254 and then used as clock for serial transmission and reception.

Modem Control (3)

- The TTL logic levels of the serial data lines and the control signals necessary for serial transmission and reception are converted to RS232 logic levels using MAX232 and then terminated on a standard 9-pin D-.type connector.
- In 8251A the transmission and reception baud rates can be different or same.
- The device which requires serial communication with processor can be connected to this 9-pin D-type connector using 9-core cable
- The signals TxEMPTY, TxRDY and RxRDY can be used as interrupt signals to initiate interrupt driven data transfer scheme between processor and 8251

Modem Control (4)

- The CPU reads the parallel data from the buffer register.
- When the input register loads a parallel data to buffer register, the RxRDY line goes high.
- The clock signal RxC (low) controls the rate at which bits are received by the USART.
- During asynchronous mode, the signal SYNDET/BRKDET will indicate the break in the data transmission.
- During synchronous mode, the signal SYNDET/BRKDET will indicate the reception of synchronous character.

S – 13

DMA Controller 8257 & Interfacing 8257 with 8086 and programming

Direct Memory Access (DMA)

- An I/O technique used for high data transfer
- Between memory and peripheral
- MPU releases the control of Buses
- DMA controller manages data transfer

8257 DMA Controller

- Programmable DMA controller
- Primary function: a sequential memory access which allow the peripheral **to read or write data** directly **to or from memory**
- Has 4 independent channels each capable of transferring 64 Kbytes of data
- Must be interfaced with MPU and peripherals
- HOLD
- HLDA (Hold Acknowledge)

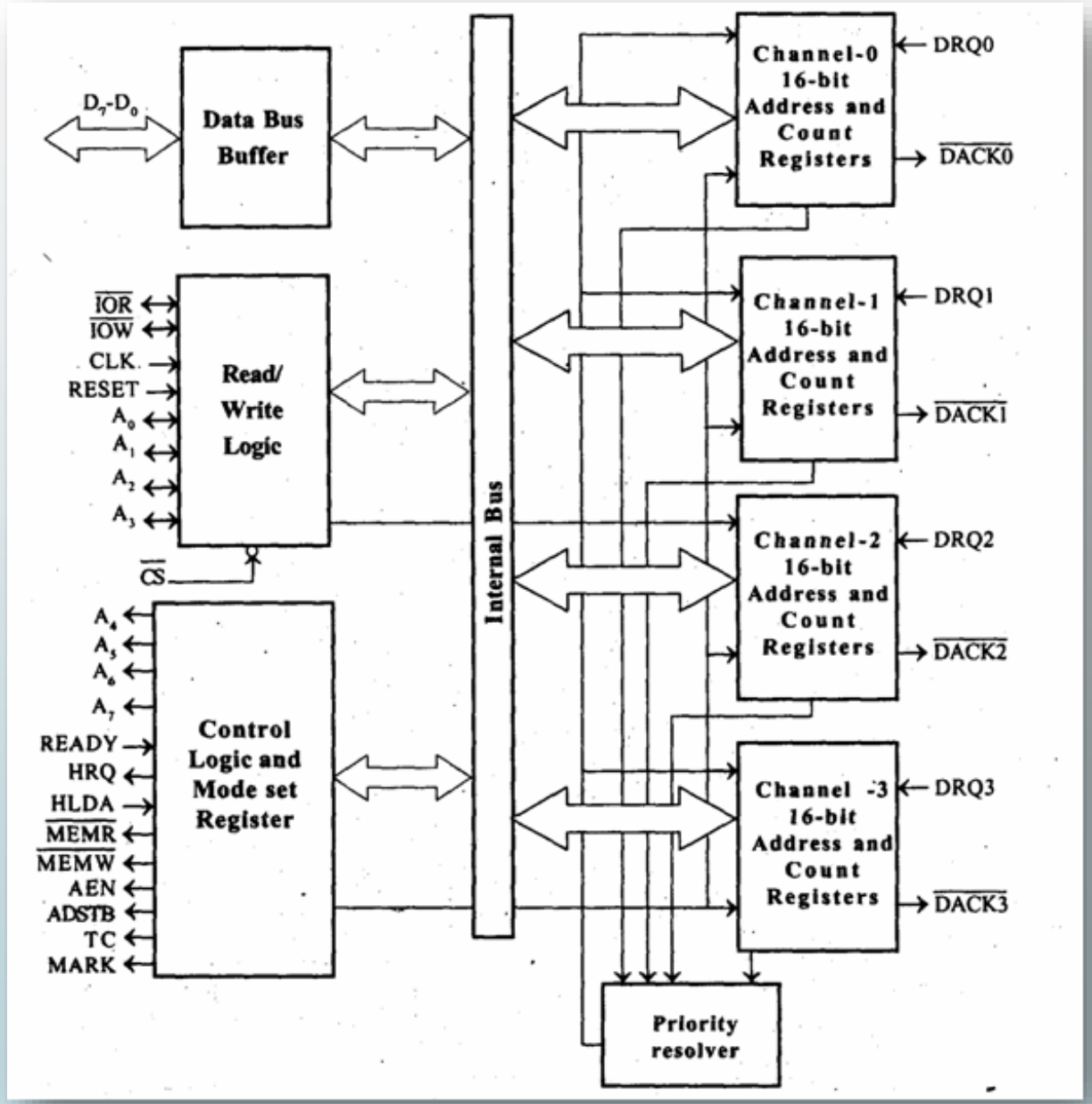
8257 DMA Controller

- Plays two role:
  - I/O to Microprocessor (**Slave mode**)
  - Data transfer processor to peripherals (**Master mode**)
- Has priority DMA request logic

8257 Architecture

BLOCKS

1. DMA Channels
2. Data Bus Buffer
3. Read/Write Logic
4. Control Logic



1. DMA Channels contd...

- Four separate DMA channels (CH-0 to CH-3)
- Each channel includes two 16 bit registers
  1. DMA address register
  2. Terminal count register
- 14 bit count (N-1) is loaded into TC reg
  - 2 msb's give the type of DMA operation
- Signals DRQ0 to DRQ3, $\overline{DACK0}$ to $\overline{DACK3}$

1. DMA Channels (Types of DMA Operation)

Bit 15	Bit 14	Type of DMA Operation
0	0	Verify DMA Cycle
0	1	Write DMA Cycle
1	0	Read DMA Cycle
1	1	(Illegal)

2. Data Bus Buffer

- This three-state, bi-directional, eight bit buffer interfaces the 8257 to the system data bus
- $D_0 – D_7$

3. Read/Write Logic

- $A_0 - A_3$
- $\overline{\mathbf{IOR}}$, $\overline{\mathbf{IOW}}$
  - Input signals in slave mode
  - Output signals in master mode
- RESET
- CLK
- $\overline{\mathbf{CS}}$

4. Control Logic

- ADSTB (Address Strobe):
- This output strobes the most significant byte of the memory address into the 8212 device from the data bus
- AEN (Address Enable):
- Used to disable the system buses
- TC (Terminal Count)
- MARK (Modulo 128 Mark)

Learning Resource

[1] K. M. Bhurchandi and A. K. Ray, "Advanced Microprocessors and Peripherals – with ARM and an Introduction to Microcontrollers and Interfacing", Tata McGraw Hill, 3rd ed., 2015.

Thank You