Dillo2 ps

Tost - CLATZ - Answer Key

Course code: MUCCOOIJ- Analog Electronic

Yearlsem: 11/1

Max marks : 50

SET-A

Parl-A: (10x1 = 10) Marks.

7 p) 1.730/0

2. a) mobility decreases

2. c) - gmRo/(1+gm Pi)

4. c) Common gate

5. a) coupling Capacitor Most Circuit and Load Capacitor Open Circuit

6. b) Error Signal

y. b) invuerses

g. a) Distortion

q. c) High, high

10. b) Oscillator

Part-B: (d1x10 = 40) Marks.

11. Common Cade Configuration

18 3/00 /20 x

Sol! 
$$\int_{R} = \int_{DR} = K_{n} \left( V_{GNS} Q - V_{FN} \right)^{2}$$

$$\int_{I=1}^{2} \left( V_{GNS} Q - I \right)^{2}$$

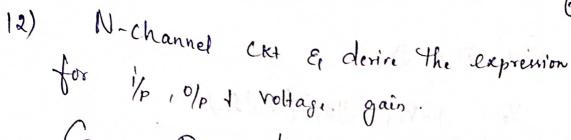
$$\int_{V_{GN}} = 2V$$

$$\int_{I=1}^{2} \left( V_{GNS} Q - I \right)^{2}$$

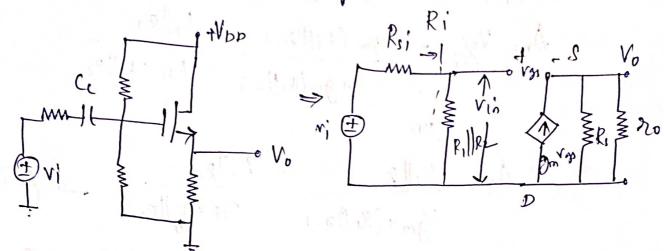
$$\int_{I=1}^{2} \left( V_{GNS} Q - I \right)$$

$$\int_{I=1}^{2} \left($$

117 1 2 1 2 1 2 1



Common Drain Amplifuis



Sub is Vo

Explanation - (2m)

Circuit & Equivalent Circuit - 2m)

Circuit & Equivalent Circuit (2m)
Vollege gain Av = Vo/vi
= - gmRp - (1m)

b) Small Signal Voltage gais of Common Source with Source bypass Capacitor.

Sol!

Too = Io = Kn ( Vasa - VTN)

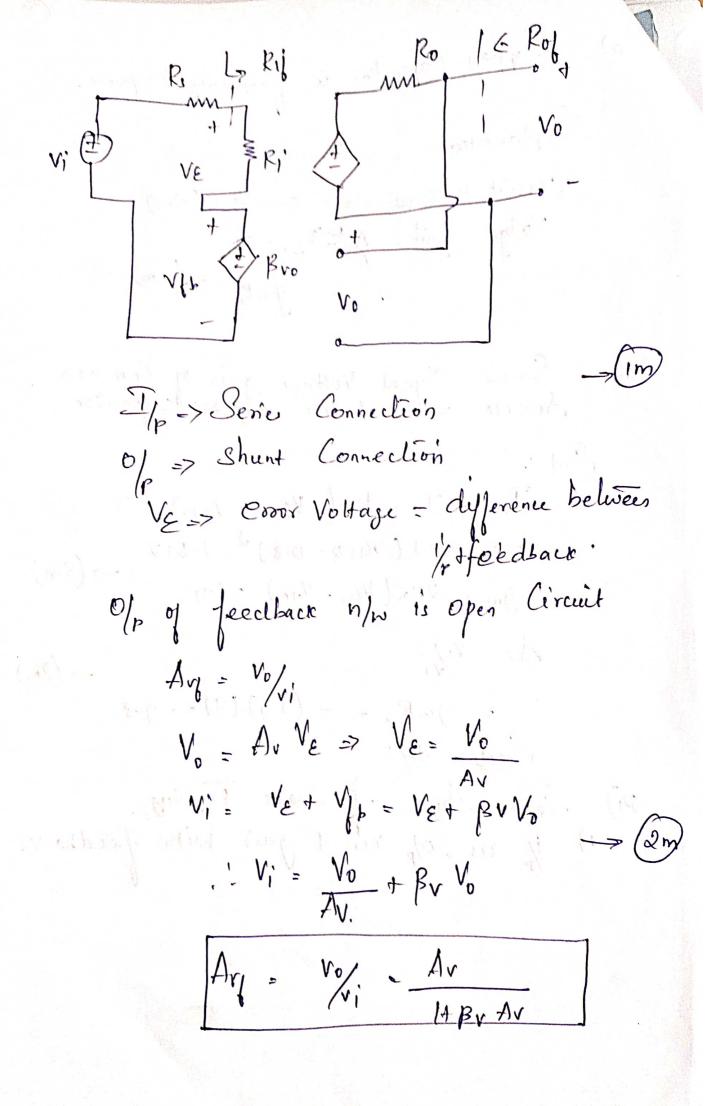
0.5 = (1) ( Vasa - 0.8) = 1.5) V

gm = 2 Kn ( Vas - VTN) = 1.4

3m)

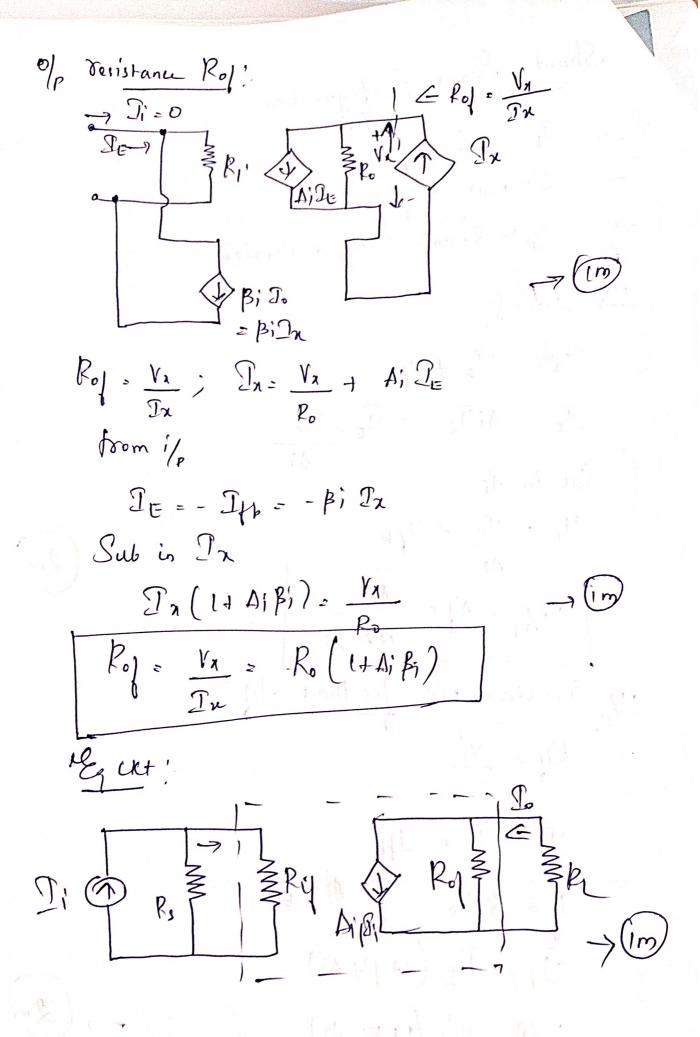
 $Ar = V_0/1$   $= -g_m R_p = -(1-q)[7] = -q.8$ Section -B2:

14) Series Shunt feedback Topology.
a) 1/2 res, 0/2 res + gais with feedback.



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Shunt Series Configuration



Chapperse, Diagram 
$$\rightarrow$$
 (2m) Chipperse, Diagram  $\rightarrow$  (2m) Chipperse, Ceq =  $\frac{1}{1} + \frac{1}{12} + \frac{1$ 

- Cach Re n/w provide a phase shift of 6.
Three Re stages are carcaded to provide
Three Re stages are carcaded to provide a phone shift of 100.
- Value of Re components determine the
frequency of Re components determine the
No no of stages
No no of stayer
1 JURY5
The amplifier gain AZ29, B=1/29.
Advantage: - Simple to design
Advantage: Simple to denign  - produces Sineware - Dr
Disadvantage - frequency + stability
Pool