Unit -III : Digital Electronics Principles

Sequential circuits

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Introduction

- Sequential circuits output is also depend on the previous output.
- It takes the history of output.

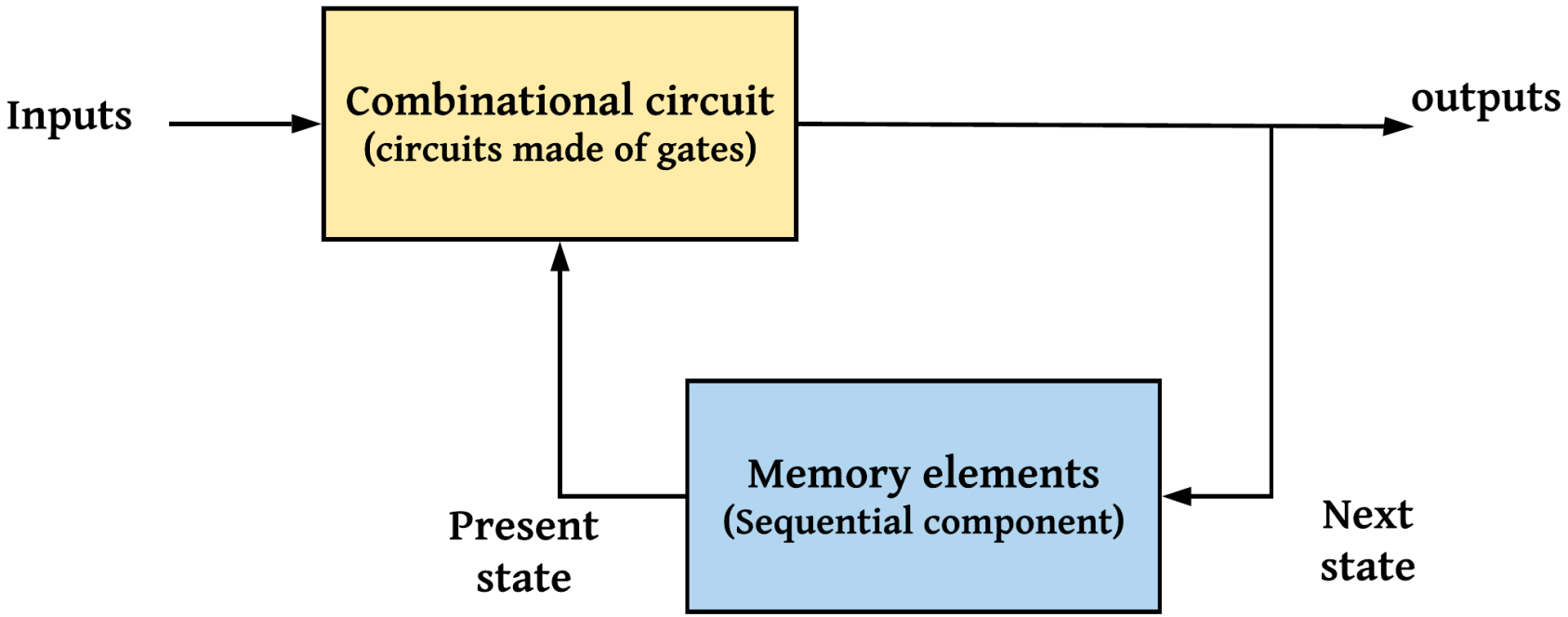

Figure 1: Block diagram of sequential circuit

Latch

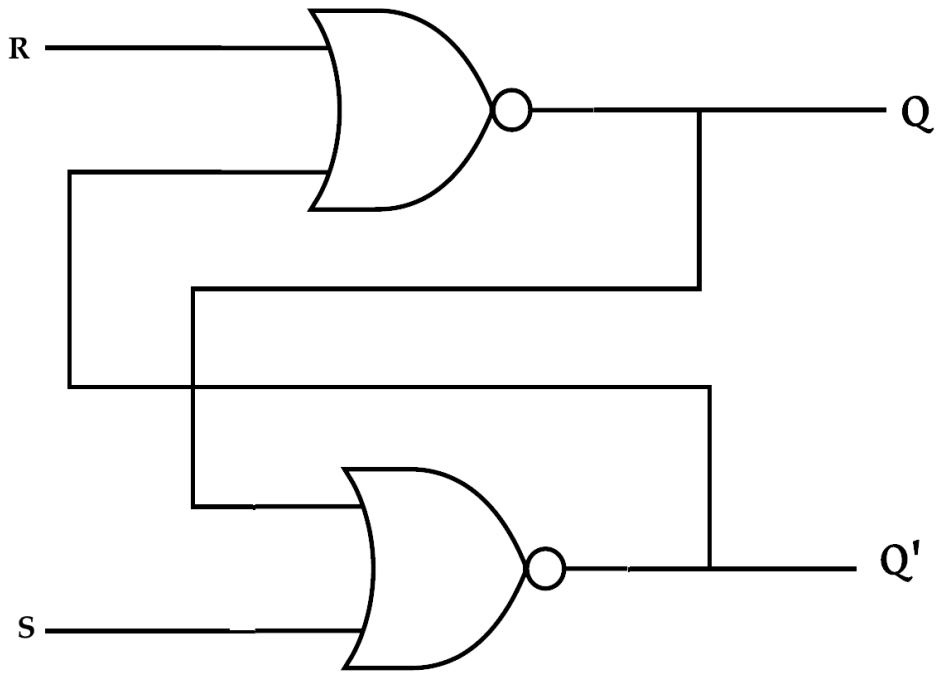

Figure 2: One bit cell

S	R	Q	Q'	State
0	1	1	0	
0	0	1	0	memory
1	0	0	1	
0	0	0	1	memory
1	1	0	0	not used
0	0	1	0	un-reliable
0	0	0	1	un-reliable

Table 1: One bit cell

Operation

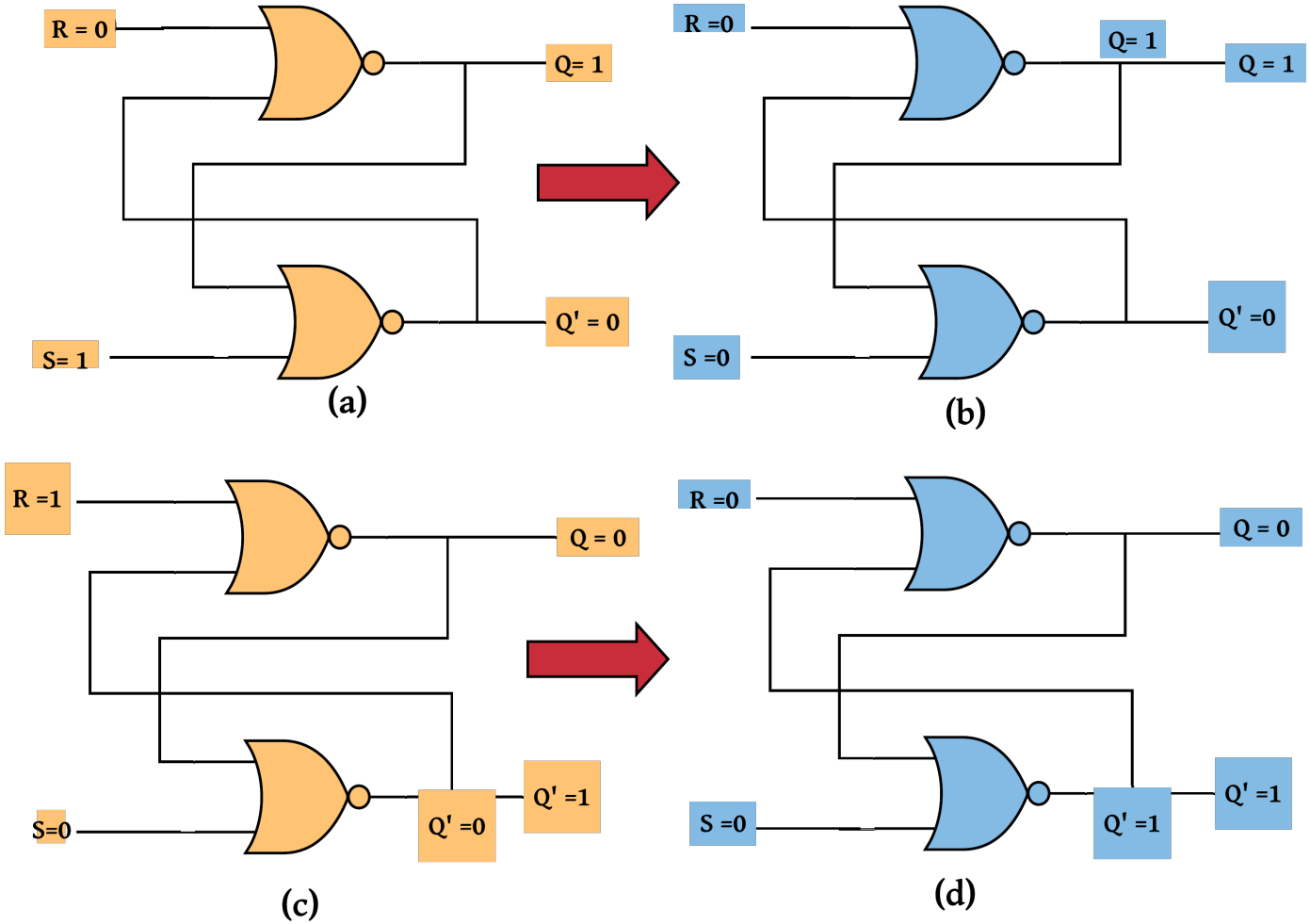

Figure 3: Characteristics of a SR Latch

Operation contin..

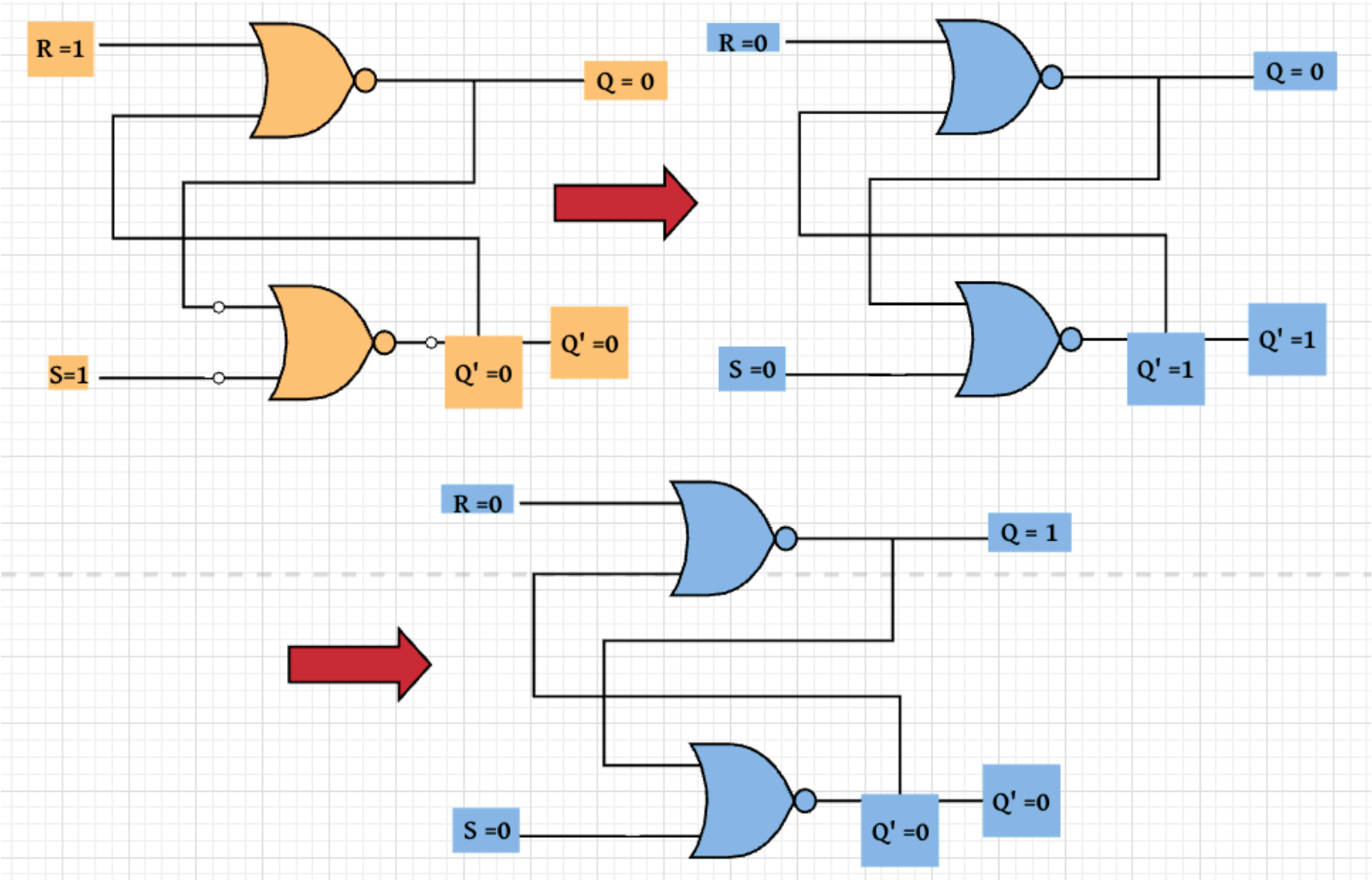

Figure 4: Characteristics of a SR Latch

Summary of characteristic of SR latch

S	R	Q	Q'
0	0	memory	
0	1	0	1
1	0	1	0
1	1	not used	

Table 2: SR latch summary

Exercise:

- Analyse the operation of following sequential circuit given below:

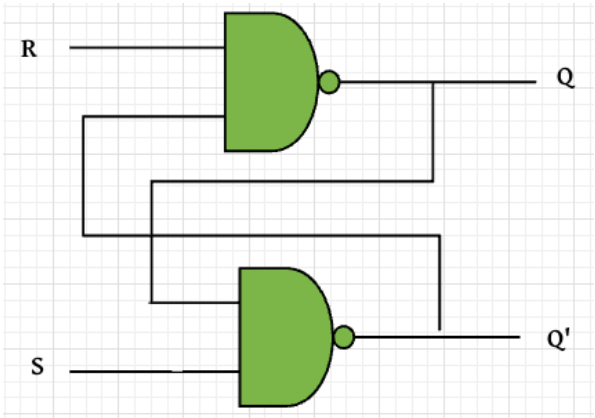

Figure 5: SR latch using NAND gates

Clocks

- It controls the storage value.
- It is a enable signal to decide when to take the new value of input and store in the latch.
- Mostly, it is a square wave that goes either high to low or low to high.

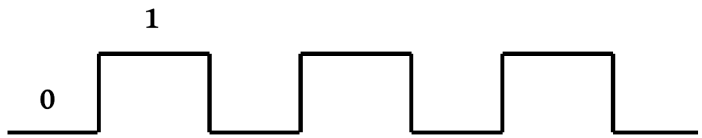

Figure 6: Clock signal

- Latches constructed using this clock signal are called as *Flip-flops*.
- Types :
  - SR flip flop
  - D flip flop
  - T flip flop
  - JK flip flop

SR flip flop

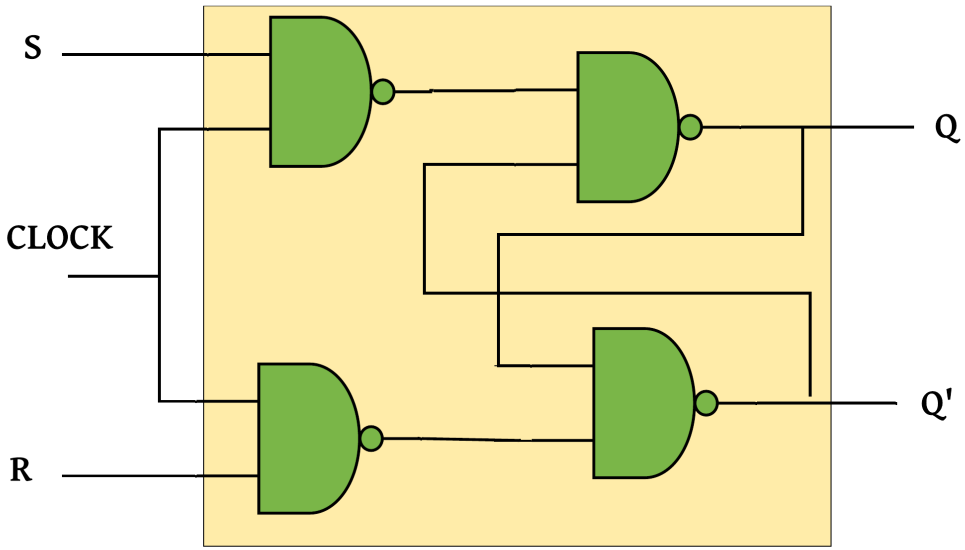

Figure 7: SR flip flop

Clock	S	R	Q	Q'
0	X	X	memory	
1	0	0	memory	
1	0	1	0	1
1	1	0	1	0
1	1	1	not used	

Table 3: SR FF truth table

D flip flop

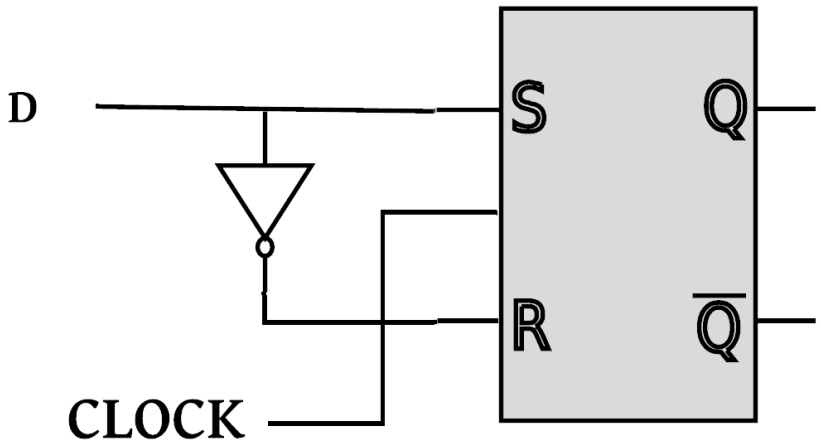

Figure 8: D flip flop

Clock	D	Q	Q'
0	X	memory	
1	1	1	0
1	0	0	1

Table 4: D flip flop summary

JK flip flop

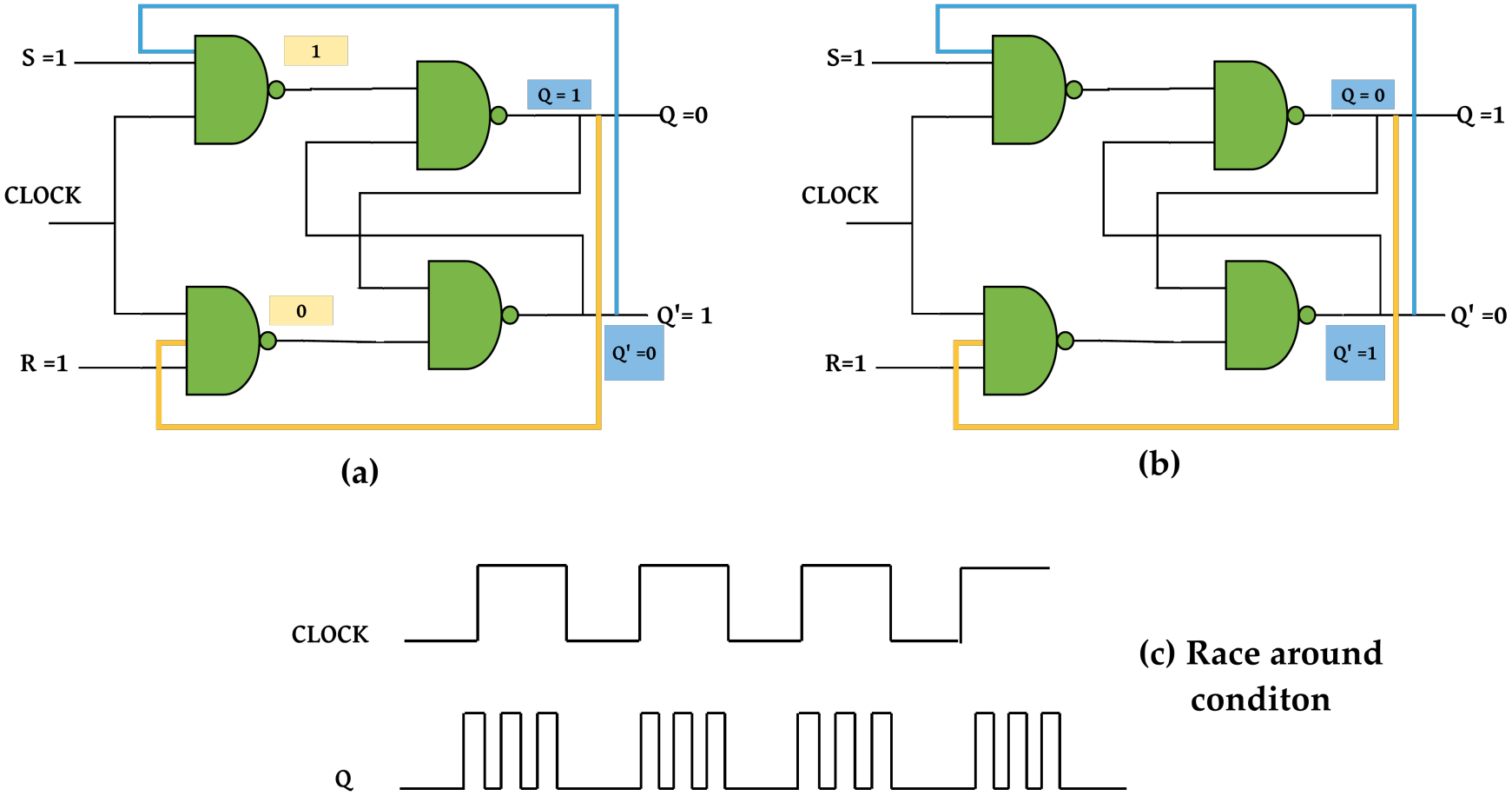

Figure 9: JK flip flop and its race around condition

Summary of JK flip flop and Exercise

Clock	J	K	Q	Q'
0	X	X	memory	
1	0	0	memory	
1	0	1	0	1
1	1	0	1	0
1	1	1	Toggle	

Table 5: JK FF truth table

Exercise: Obtain the truth table and characteristic table of T flip flop.

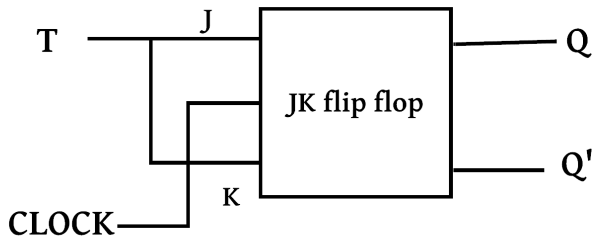

Figure 10: T flip flop

Excitation table from Truth table

SR flip flop

CP	S	R	Q_n	Q_{n+1}
1	0	0	0	0
1			1	1
1	0	1	0	0
1			1	0
1	1	0	0	1
1			1	1
1	1	1	0	X
1			1	X

Table 6: Truth table

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Table 7: Excitation table

Q_n - previous state; Q_{n+1} - next state; CP - clock pulse

Excitation table from Truth table

D flip flop

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Table 8: Excitation table of D FF

JK flip flop

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Table 9: Excitation table of JK FF

T flip flop

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Table 10: Excitation table of T FF