Analysis of Clocked Sequential Circuits

Sequential Circuit Analysis

- The behavior of a clocked sequential circuit is determined from
  - The inputs
  - The outputs
  - The state of its flip-flops
- The outputs and the next state are both a function of the inputs and the present state
- To analyze a sequential circuit, we can use
  - State equations
  - State table
  - State diagram
  - Flip-Flop input equations

State Equations

- Specify the next state as a function of the present state and inputs
  - Also called transition equation
- Analyze the combinational part directly
- EX:

$A(t+1) = A(t)x(t) + B(t)x(t)$

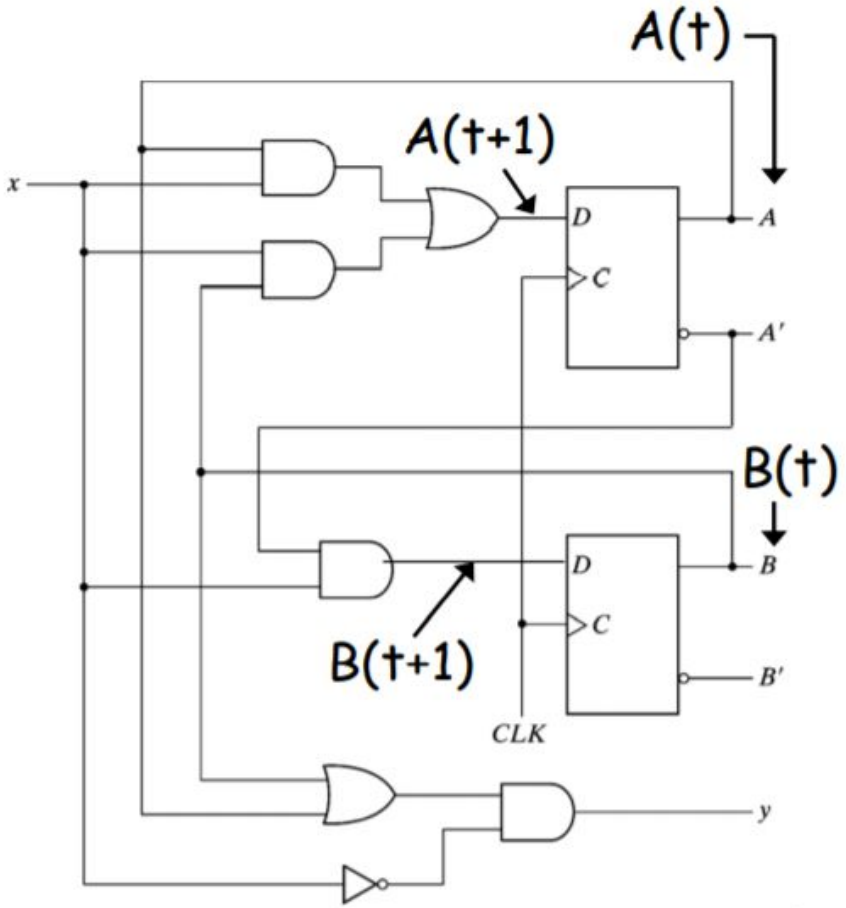
$\Rightarrow A(t+1) = Ax + Bx$

$B(t+1) = A'(t)\,x(t)$

$\Rightarrow B(t+1) = A'x$

$y(t)=[A(t)+B(t)]\,x(t)$

$\Rightarrow y=(A+B)x'$



State Table

- Enumerate the time sequence of inputs, outputs, and flip-flop states
  - Also called transition table
  - Similar to list the truth table of state equations
- Consist of four sections
  - Present state, input, next state, and output
- A sequential circuit with m flip-flops and n inputs need 2^{m+n} rows in the state table

Present state		input	Next state		output
A	B	x	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

Second Form of State Table

- The state table has only three section: present state, next state, and output
- The input conditions are enumerated under next state and output sections

Present State		Next State				Output	
		X=0		X=1		X=0	X=1
A	B	A	B	A	B	Y	Y
0	0	0	0	0	1	0	0
0	1	0	0	1	1	1	0
1	0	0	0	1	0	1	0
1	1	0	0	1	0	1	0

State Diagram

- Graphically represent the information in a state table
  - Circle: a state (with its state value inside)
  - Directed lines: state transitions (with inputs/outputs above)
- Ex: starting from state 00
  - If the input is 0, it stays at state 00 with output=0
  - If the input is 1, it goes to state 01 with output=0
- The state table is easier to derive from a given logic diagram and state equations
- The state diagram is suitable for human interpretation

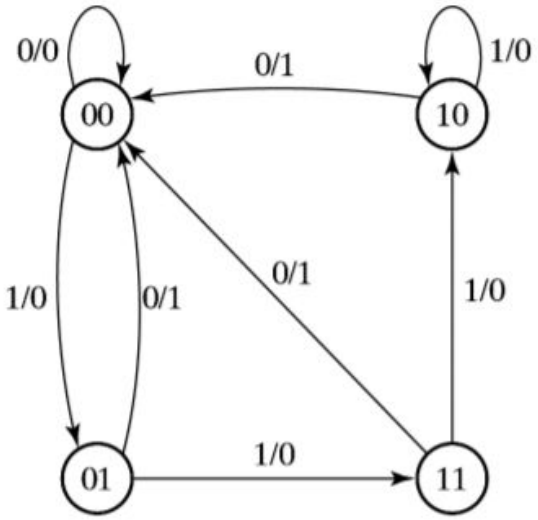


Fig. 5-16 State Diagram of the Circuit of Fig. 5-15

Flip-Flop Input Equations

- To draw the logic diagram of a sequential circuit, we need
  - The type of flip-flops
  - A list of Boolean expressions of the combinational circuits
- The Boolean functions for the circuit that generates external outputs is called output equations
- The Boolean functions for the circuit that generates the inputs to flip-flops is flip-flop input equations
  - Sometimes called excitation equations
- The flip-flop input equations provide a convenient form for specifying the logic diagram of a sequential circuit
- Ex: (Fig. 5-15)

Input:

$D_A = Ax + Bx$

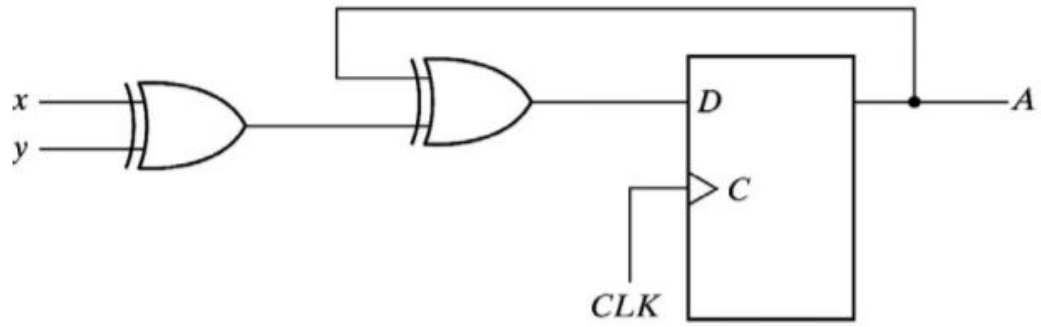
$D_B = A'x$

Output:

$y = (A+B)x'$

Analysis with D Flip-Flop

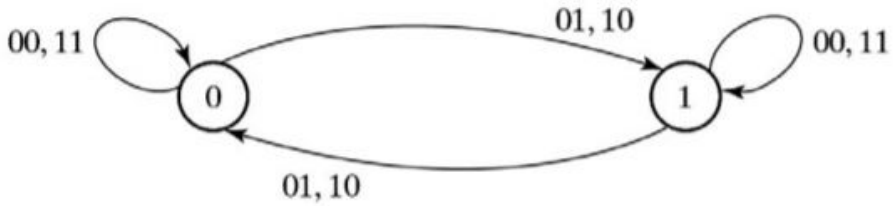
- Input equation: $D_A = A \oplus x \oplus y$



(a) Circuit diagram

Present state	Inputs		Next state
A	*x*	*y*	*A*
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

(b) State table



(c) State diagram

Fig. 5-17 Sequential Circuit with *D* Flip-Flop

Analysis with Other Flip-Flops

- The sequential circuit using other flip-flops such as JK or T type can be analyzed as follows
  - Determine the flip-flop input equations in terms of the present state and input variables
  - List the binary values of each input equation
  - Use the corresponding flip-flop characteristic table to determine the next state values in the state table

Analysis with JK Flip-Flops (1/2)

Step 1: input equations

$J_A=B \quad K_A=Bx' \quad J_B=x' \quad K_B=A \oplus x'$

Step 2: state equations

$A(t+1)= JA' + K'A$

$= BA' + (Bx')'A$

$= A'B + AB' + Ax$

$B(t+1)= JB' + K'B$

$= x'B' + (A \oplus x)'B$

$= B'x' + ABx + A'Bx'$

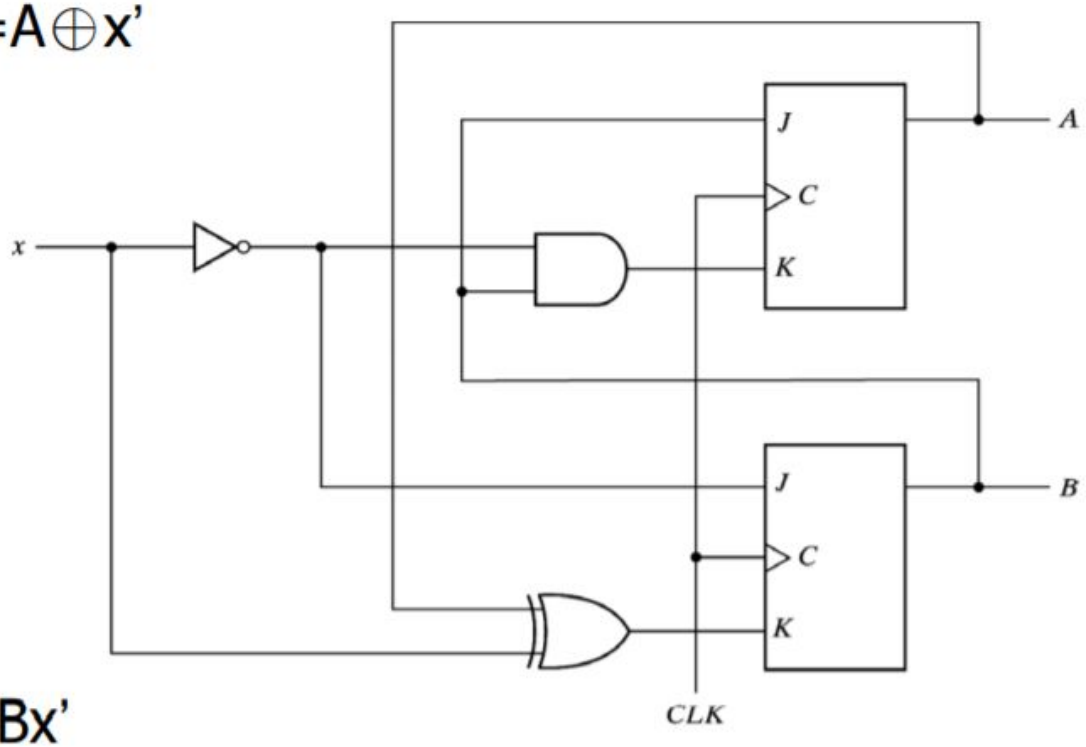


Fig. 5-18 Sequential Circuit with *JK* Flip-Flop

Analysis with JK Flip-Flops (2/2)

Step 3: state table

Present state		Input	Next state		Flip-Flop Inputs			
A	B	X	A	B	J_A	K_A	J_B	K_B
0	0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	0	1
0	1	0	1	1	1	1	1	0
0	1	1	1	0	1	0	0	1
1	0	0	1	1	0	0	1	1
1	0	1	1	0	0	0	0	0
1	1	0	0	0	1	1	1	1
1	1	1	1	1	1	0	0	0

Step 4: state diagram

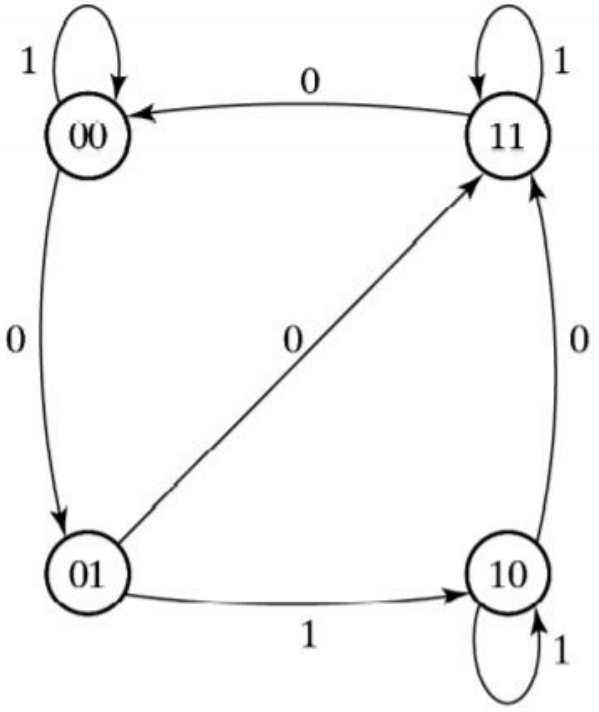
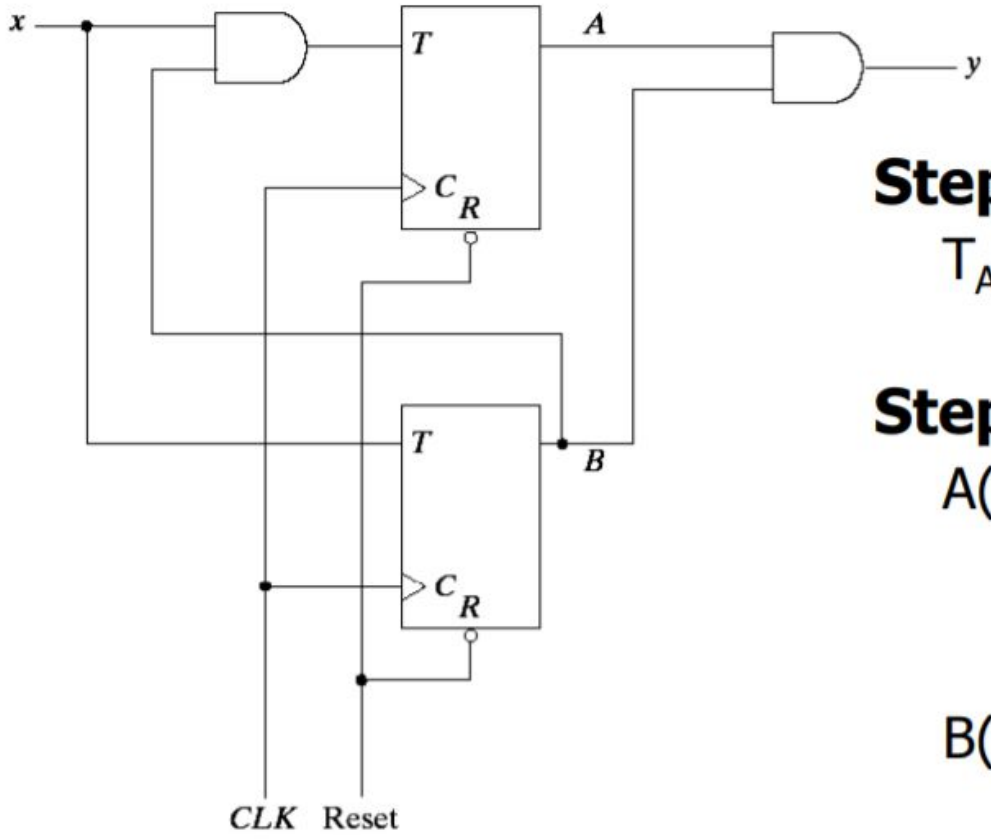


Fig. 5-19 State Diagram of the Circuit of Fig. 5-18

Analysis with T Flip-Flops (1/2)



(a) Circuit diagram

Step 1: input equations

$T_A = Bx \quad T_B = x \quad y = AB$

Step 2: state equations

$A(t+1) = T'A + TA'$

$= (Bx)'A + (Bx)A'$

$= AB' + Ax' + A'Bx$

$B(t+1) = T'B + TB'$

$= x'B + xB'$

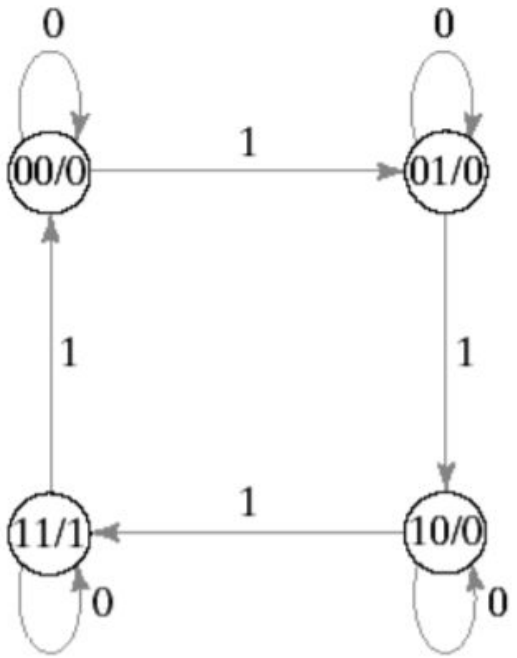
$= x \oplus B$

Analysis with T Flip-Flops (2/2)

Step 3: state table

Present state		Input	Next state		Output
A	B	X	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	1

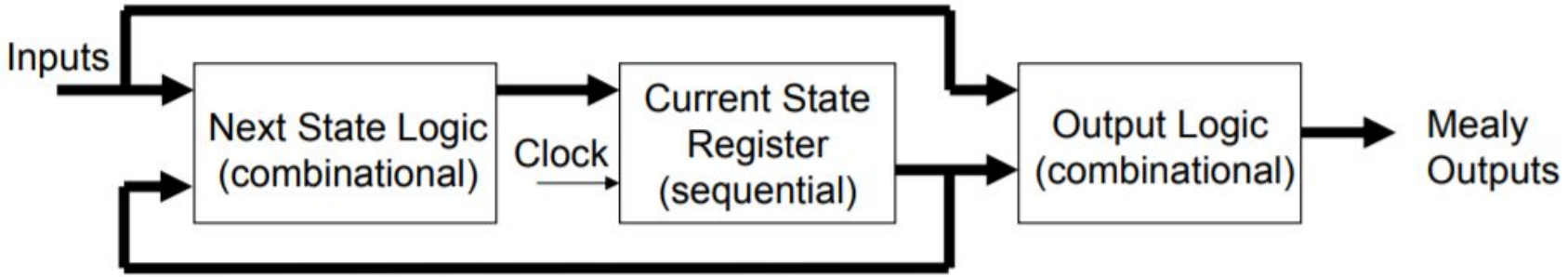
Step 4: state diagram



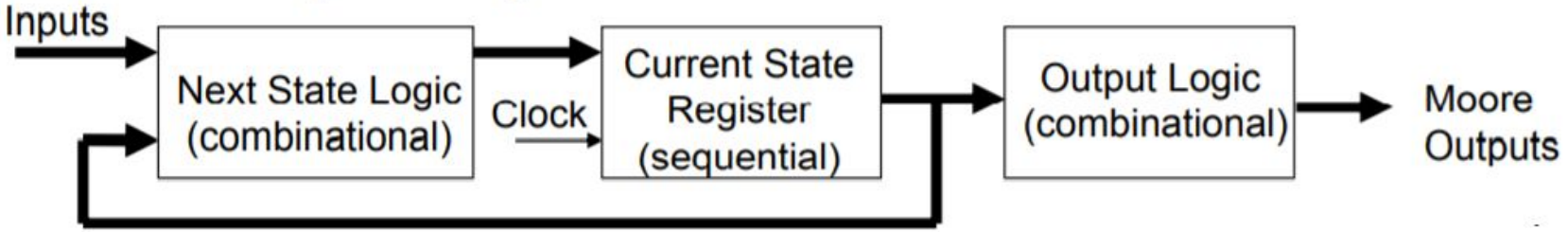
(b) State diagram

Mealy and Moore Model

- Mealy model :
  - The output is a function of **both** the present state and input
  - The output may change if the inputs change during a clock cycle



- Moore model :
  - The output is a function of the **present state only**
  - The output are **synchronized** with the clock



State Reduction

State Reduction

- Reducing the number of states in a state table, while keeping the external input-output requirements unchanged
- Example:
  - Total 7 states
  - A sequence as follows

state	a	a	b	c	d	e	f	f	g	f	g	a
input	0	1	0	1	0	1	1	0	1	0	0	
output	0	0	0	0	0	1	1	0	1	0	0	

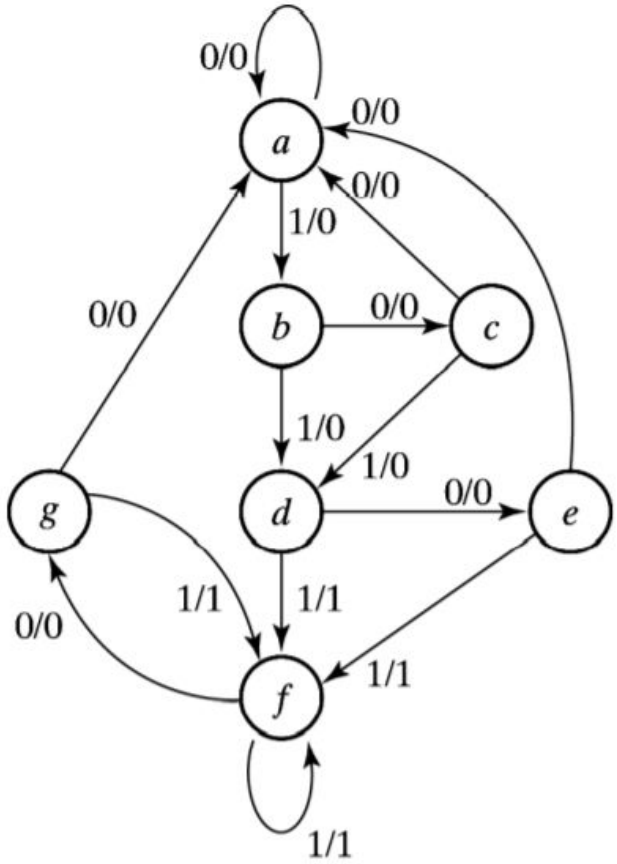


Fig. 5-22 State Diagram

State Reduction Rules

- Two states are said to be equivalent if, for every possible inputs, they give exactly the same output and have equivalent next state

Present State	Next State X=0	Next State X=1	Output X=0	Output X=1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

Present State	Next State X=0	Next State X=1	Output X=0	Output X=1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	e	f	0	1

delete state g and replaced with state e

Further State Reduction

- After the first reduction, we can see that state d and state f will have the same output and next state for both x=0 and x=1
  - Further reduce one state

Present State	Next State X=0	Next State X=1	Output X=0	Output X=1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	e	f	0	1

Present State	Next State X=0	Next State X=1	Output X=0	Output X=1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	d	0	1
e	a	d	0	1

delete state f and replaced with state d

Reduced State Diagram

- After reduction, the circuit has only 5 states with same input/output requirements
- Original output sequence:

state	a	a	b	c	d	e	f	f	g	f	g	a
input	0	1	0	1	0	1	1	0	1	0	0	
output	0	0	0	0	0	1	1	0	1	0	0	

- Reduced output sequence:

state	a	a	b	c	d	e	d	d	e	d	e	a
input	0	1	0	1	0	1	1	0	1	0	0	
output	0	0	0	0	0	1	1	0	1	0	0	

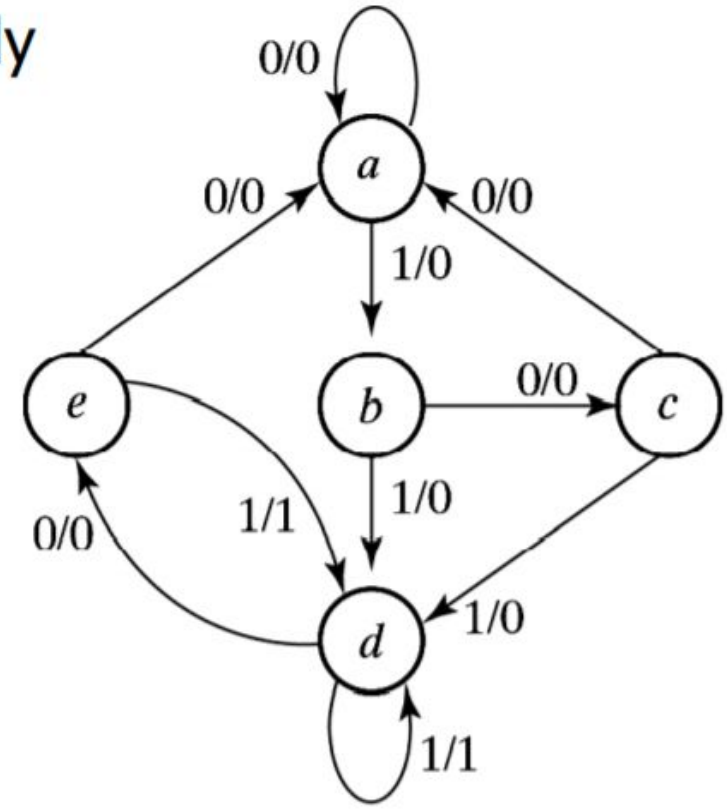


Fig. 5-23 Reduced State Diagram