Laboratory Report Cover Sheet

SRM Institute of Science and Technology Faculty of Engineering and Technology Department of Electronics and Communication Engineering
15EC203J Digital Systems **Third Semester, 2018-19 (odd semester)**

Name :

Register No. :

Day / Session :

Venue :

Title of Experiment :

Date of Conduction :

Date of Submission :

Particulars	Max. Marks	Marks Obtained
Pre-lab questions	10	
In-lab experiment	20	
Post-lab questions	10	
Total	40	

REPORT VERIFICATION

Date :

Staff Name :

Signature :

Lab 5: Design and implementation of Multiplexer and De-multiplexer using logic gates.

4:1 MUTIPLEXER

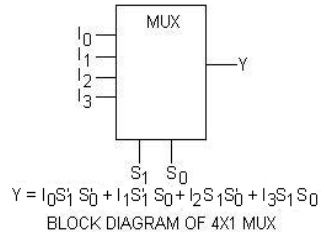

Figure 4.1: Block Schematic of 4x1 MUX

Truth Table of 4x1 MUX

Select Inputs		Output
S1	S0	Y
0	0	I0
0	1	I1
1	0	I2
1	1	I3

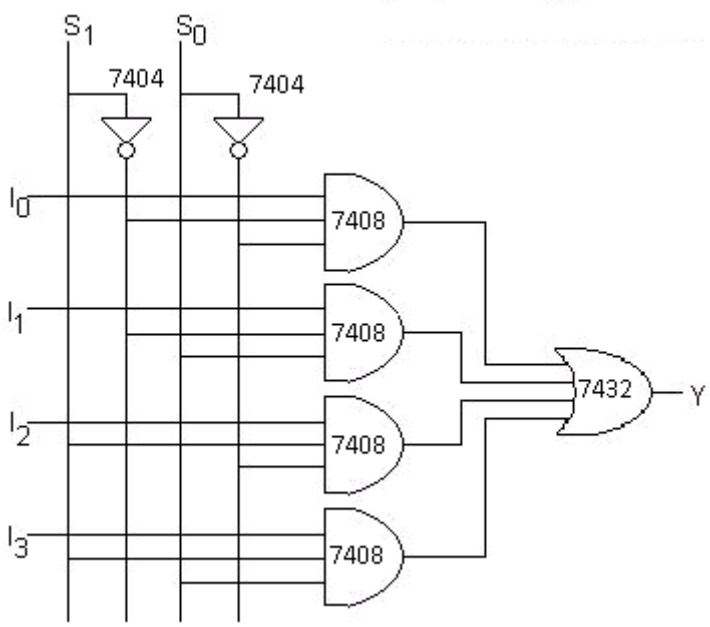

Figure 4.2: Realization of 4x1 MUX using logic gates

Lab 5: Design and implementation of Multiplexer and De-multiplexer using logic gates.

Aim

To implement and verify the functional table of 4:1 Multiplexer and 1:4 De-multiplexer using logic gates.

Hardware Requirement

a. Equipments - Digital IC Trainer Kit

b. Discrete Components - 74LS04 Hex 1-Input NOT gate
74LS08 Quad 2-Input AND gate
74LS11 Triple 3-Input AND gate
74LS32 Quad 2-Input OR gate

Theory

Multiplexer

The *multiplexer*, shortened to "MUX" or "MPX", is a combinational logic circuit designed to switch one of several input lines through to a single common output line by the application of a control signal. Multiplexers operate like very fast acting multiple position rotary switches connecting or controlling multiple input lines called "channels" one at a time to the output.

Multiplexers, or MUX's, can be either digital circuits made from high speed logic gates used to switch digital or binary data or they can be analogue types using transistors, MOSFET's or relays to switch one of the voltage or current inputs through to a single output.

In digital electronics, multiplexers are also known as data selectors because they can "select" each input line, are constructed from individual Analogue switches encased in a single IC package as opposed to the "mechanical" type selectors such as normal conventional switches and relays.

Generally, the selection of each input line in a multiplexer is controlled by an additional set of inputs called *control lines* and according to the binary condition of these control inputs, either "HIGH" or "LOW" the appropriate data input is connected directly to the output. Normally, a multiplexer has an even number of 2^n data input lines and a number of "control" inputs ' n' that correspond with the number of data inputs.

A ***multiplexer implementation table*** is used to determine the input connections for the multiplexer.

The Boolean expression for this 4-to-1 **Multiplexer** with inputs I_0 to I_3 and data select lines S_0 & S1 is given as:

$$Y = \overline{S_1}S_0I_0 + \overline{S}_1S_0I_1 + S_1\overline{S}_0I_2 + S_1S_0I_3$$

De-Multiplexers

The data distributor, known more commonly as a **Demultiplexer** or "Demux" for short, is the exact opposite of the Multiplexer, which has one single input data line and then switch it to any one of their individual multiple output lines one at a time. **The De-multiplexer** converts the serial data signal at the input to a parallel data at its output lines.

1:4 DEMULTIPLEXER

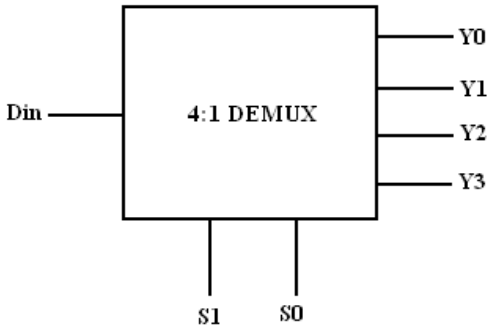

Figure 4.3: Block Schematic of 1x4 De-MUX

Truth Table of 1x4 De-MUX

Select Inputs		Data Outputs			
S_1	S_0	Y_0	Y_1	Y_2	Y_3
0	0	D_{in}	0	0	0
0	1	0	D_{in}	0	0
1	0	0	0	D_{in}	0
1	1	0	0	0	D_{in}

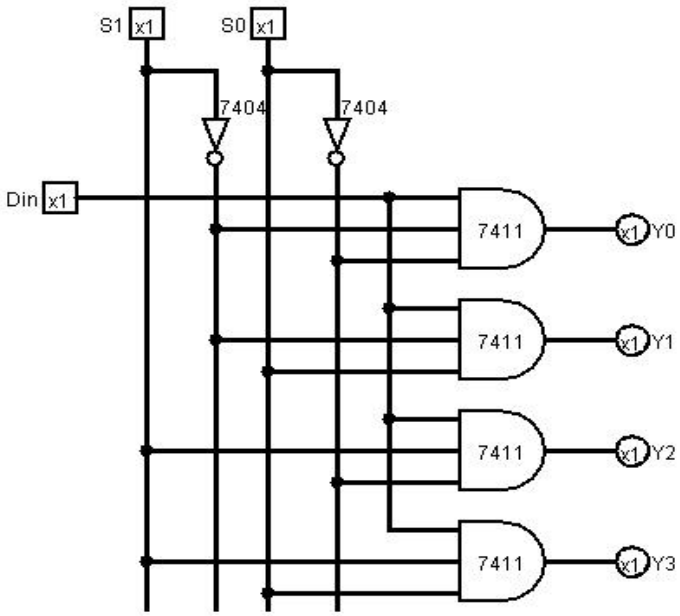

Figure 4.4: Realization of 1x4 De-MUX

They are digital switches which connect data from one input source to one of n outputs. Usually implemented by using n-to-2n binary decoders where the decoder enable line is used for data input of the de-multiplexer. The figure below shows a de-multiplexer block diagram which has got 's'-bits-wide select input, one b-bits-wide data input ' D_{in}' and 'n' outputs.

Lab Procedure

MUX

1. Write the Functional table for 4: 1 MUX.
2. From the functional table, derive the logical expression for the output in terms of the data input and the select inputs.
3. Using the derived expression, implement 4: 1 Mux using logic gates and verifies its functional table.

DEMUX

1. Write the functional table for 1: 4 De- MUX
2. From the functional table, derive the logical expression for the output in terms of the data input and the select inputs.
3. Using the derived expression, implement 1: 4 De- MUX using logic gates and verify its functional table.

Pre-lab Questions

1. Multiplexer is also called a data selector. Why?
2. Justify, Demultiplexer is a data distributor.
3. A certain multiplexer can switch one of 32 data inputs to its output. How many select inputs does this MUX have?
4. Implement a 4:1 using 2:1 MUX only.
5. Implement a 16:1 multiplexer using two 8:1 multiplexer.

Post Lab questions

1. Implement the following Boolean expression using 8:1 multiplexers :
   $F(A,B,C,D)= \Sigma(0,1,3,4,8,9,15)$
2. Draw the block diagram of 1x4 DeMUX using 1x2 DeMUX. Draw its truth table.
3. Implement a Full Adder using two 8-to-1 MUX.
4. Implement a Full Adder using two 4-to-1 MUX and one inverter.
5. Show how two 4-to-1 and one 2-to-1 MUX could be connected to form an 8-to-1 MUX.
6. Show how two 2-to-1 MUX (with no added gates) could be connected to form a 3-to-1 MUX. Input selection should be as follows.
   If AB=00, Select I_0
   If AB=01, Select I_1
   If AB=1X, Select I_2
7. How can a decoder be used as a demultiplexer?
8. What are the applications of MUX and DEMUX?

Result: