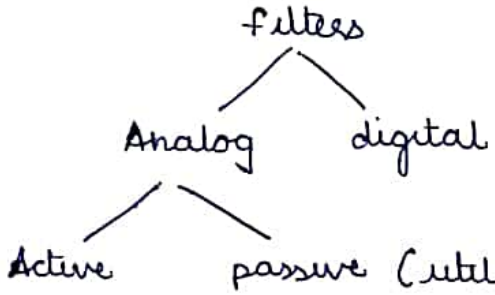
UNIT- IV ACTIVE FILTERS & VOLTAGE REGULATORS

filter is frequency selective circuit that allows only desired frequency band to pass through and attenuates undesired frequency components.



Active n/w interconnects passive elements (R, C) & Active elements (Transistor, tunnel diodes & operational amplifiers)

COMPARISON BETWEEN PASSIVE & ACTIVE NETWORKS:

Limitations of passive RLC Networks over Active RC n/w:

(i) In RLC n/w, practical inductors tend to deviate from the inductance realized.

(ii) There is power loss because of the dissipation in resistive and inductive elt.

(iii) Q factor, $Q = \frac{\omega L}{r_L}$; for ideal inducta $r_L = 0$ & $Q = \infty$ but for practical inductor $r_L \neq 0$; therefore $Q \neq \infty$

(iv) for practical inductors, total dissipative loss ↑ as f↑ as a result Q does not ↑ linearly.

(v) magnetic coupling creates unwanted stray fields which is harmful for applications like Satellite instrumentation

(vi) for low freq application such as control s/m inductors of reasonable Q becomes bulky & expensive.

(vii) dissipation losses starts increasing when indust. is miniaturized

Advantage of Active filters over passive filters

(i) gain > unity

(ii) loading effect is minimal

iii) They do not exhibit insertion loss.

(iv) complex filters can be realized with out indust.

(v) Stable & economical design

(vi) easily tuneable, flexible gain & frequency adjustm

viii) Active filtes uses op-amp. hence it has high input impedance & low output impedance. hence th do not cause loading effect

Limitation of Active filter over passive filter

(i) Slew rate of op amps leads to lower bandwidth than the designed B/W

(ii) design is costly for high freq.

(iii) Active filters require dual polarity dc power supply.

(iv) sensitive to temperature and parameter variations

ACTIVE NETWORK DESIGN

A filter is a linear two port n/w with transfer function $H(s) = V_o(s)/V_i(s)$. This response is also expressed as $H(j\omega) = |H(j\omega)| e^{j\varphi(\omega)}$

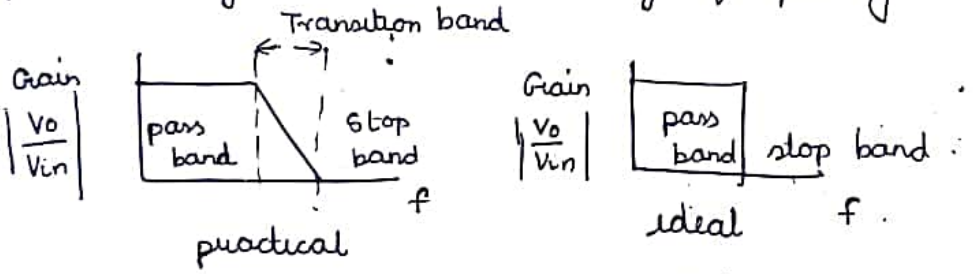
$H(j\omega) \rightarrow$ magnitude response.

$\varphi(\omega) \rightarrow$ phase response.

filter can be realized in one of the following four basic response types.

(i) LOW PASS FILTER (LPF)

LPF allows only low frequency signal to pass through & suppresses high frequency components

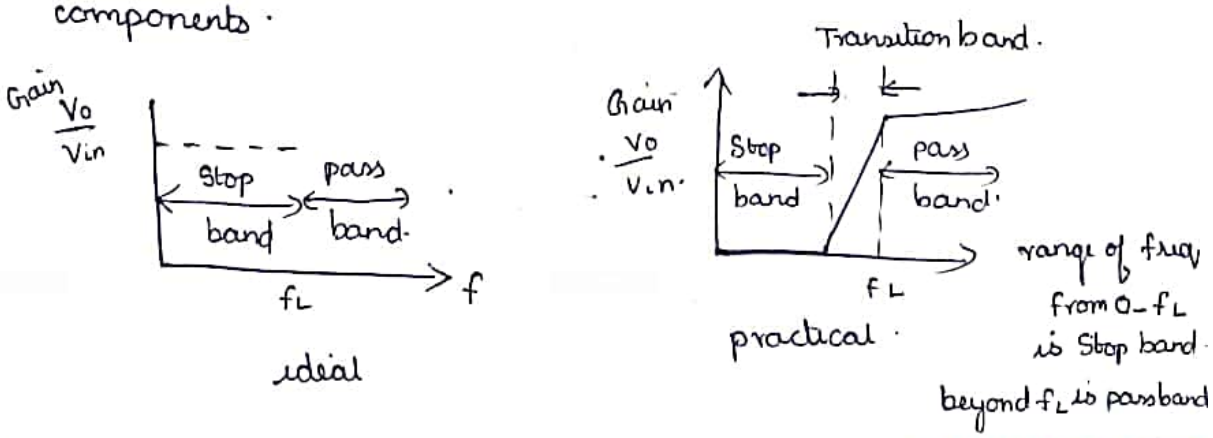


range of freq from 0 to higher cut off freq f_H is pass band.

range of freq beyond f_H is stop band

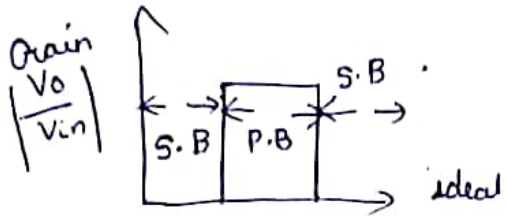
(ii) HIGH PASS FILTER (HPF)

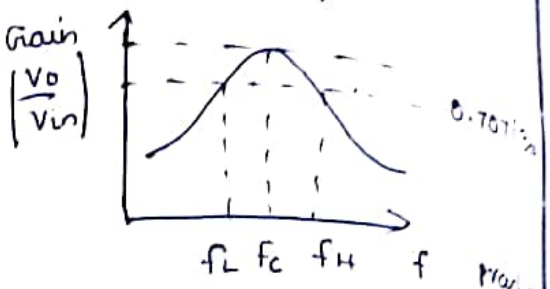
HPF allows only frequencies above a certain breakpoint to pass through and attenuates low freq components.



(iii) BAND PASS FILTER (BPF).

combination of HPF & LPF & this allows specified range of frequencies to pass through





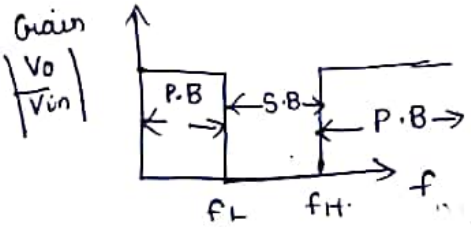
2 Stop bands & 1 pass band (band b/w f_L & f_H)

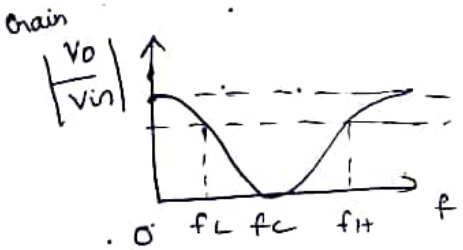
↓

(0 - f_L) & beyond f_H

(iv) BAND REJECT FILTER. (BRF)

inverse of BPF which does not allow specific range of frequency to pass through.



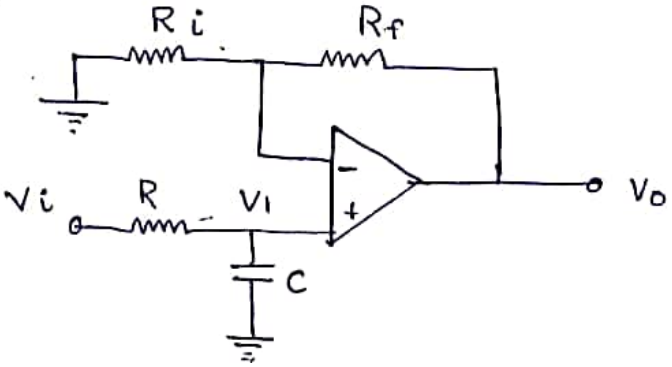


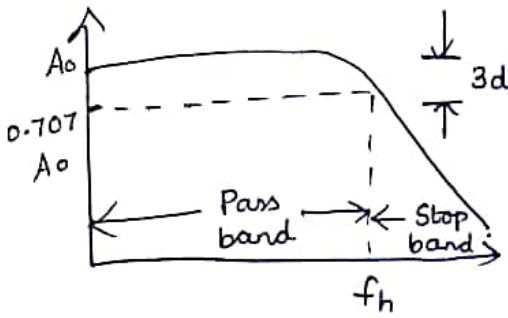
(f_L - f_H) → Stop band.

(0 - f_L) & beyond f_H - pass band.

FIRST ORDER LOW PASS FILTER.

First order low pass filter consists of single RC network connected to (+) input terminal of non inverting op-amp. R_1 & R_f determine gain of filter in pass band.





The voltage V_1 across capacitor C in S-domain is

$$V_1(S) = \frac{1/SC}{R + 1/SC} V_i(S) \quad -(1)$$

$$\therefore \boxed{\frac{V_1(S)}{V_i(S)} = \frac{1}{1 + RCS}}$$

where V(S) is laplace transform of V in time domain

W.K.T → close loop gain A_o of op-amp is

$$A_o = \frac{V_o(S)}{V_1(S)} = \left(1 + \frac{R_f}{R_1}\right) \quad -(2)$$

∴ overall Transfer function is

$$H(S) = \frac{V_o(S)}{V_i(S)} = \frac{V_o(S)}{V_1(S)} \cdot \frac{V_1(S)}{V_i(S)} = \frac{A_o}{RCS + 1} \quad -(3)$$

Let $\omega_H = 1/RC$

Therefore, $$H(S) = \frac{V_o(S)}{V_i(S)} = \frac{A_o}{\frac{S}{\omega_H} + 1} = \frac{A_o \omega_H}{S + \omega_H} \quad -(4)$$

This is standard form of transfer function of first order LPF.

To determine frequency response put $S = j\omega$ in (3)

$$H(j\omega) = \frac{A_o}{1 + j\omega RC} = -\frac{A_o}{1 + j(f/f_H)} \quad \text{where } f_H = \frac{1}{2\pi RC}$$

At low frequency i.e. $f << f_H$

$$|H(j\omega)| \simeq A_o$$

At $f = f_H$

$$|H(j\omega)| = \frac{A_0}{\sqrt{2}} = 0.707\, A_0$$

At high frequency ie $f >> f_H$

$$|H(j\omega)| << A_0 \simeq 0$$

from dia At $f = 0$, it has max gain A_0

At f_H, gain falls to 0.707 times (-3dB down) the max gain.

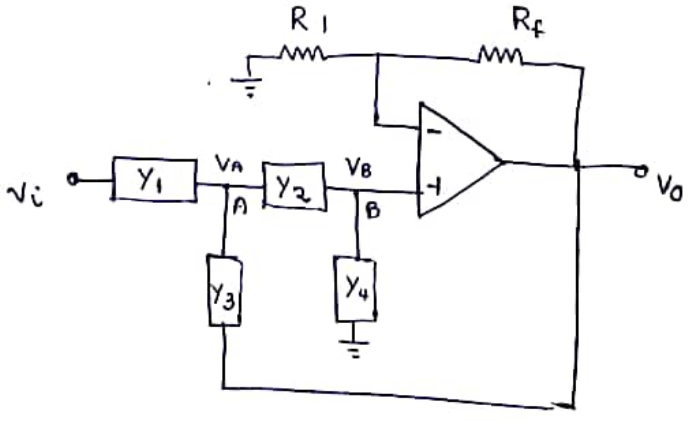
At $f > f_h$, the gain ↓ at -20 dB/decade

∵ [when freq is ↑ ten times, voltage gain is divided by ten in terms of dBs. Therefore gain decreases by 20 dB)

SECOND ORDER ACTIVE FILTER

Improved filter response can be obtained by using second order filter. Second order filter has two RC pairs & has roll off rate of -40 dB/dec

General Second order filter is shown below



$$V_o = \left(1 + \frac{R_F}{R_i}\right) V_B = A_0 V_B$$

$$A_0 = 1 + \frac{R_F}{R_i}$$

V_B → voltage at node B

KCL at node A

$$V_i Y_1 = V_A (Y_1 + Y_2 + Y_3) - V_o Y_3 - V_B Y_2$$

$$= V_A(Y_1+Y_2+Y_3) - V_0Y_3 - \frac{V_0Y_2}{A_0}$$

$V_A \rightarrow$ voltage at node A

KCL at node B give — (1)

$$V_AY_2 = V_B(Y_2+Y_4)$$

$$= \frac{V_0}{A_0}(Y_2+Y_4) \quad ; \quad V_A = \frac{V_0(Y_2+Y_4)}{A_0Y_2} \quad - (2)$$

on simplification of (1) & (2), we get

$$\frac{V_0}{V_i} = \frac{A_0Y_1Y_2}{Y_1Y_2 + Y_4(Y_1+Y_2+Y_3) + Y_2Y_3(1-A_0)}$$

To make LPF, $Y_1 = Y_2 = 1/R$ and $Y_3 = Y_4 = SC$

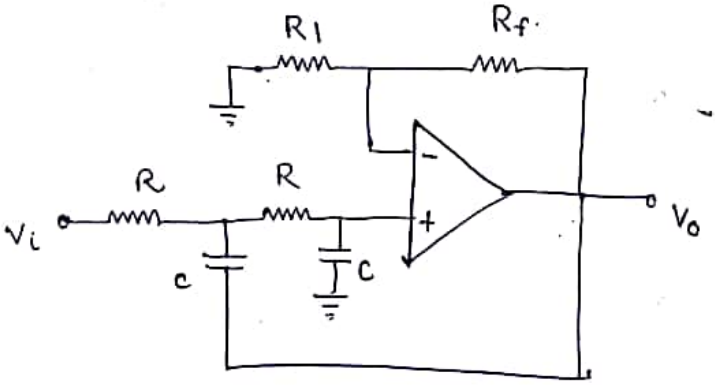
we get T.F of LPF as

$$H(S) = \frac{A_0}{S^2C^2R^2 + SCR(3-A_0) + 1}$$

$H(0) = A_0$; for $S = 0$

$H(\infty) = 0$; for $S = \infty$

} So this is obviously LPF.



$$H(S) = \frac{A_0\omega_h^2}{S^2 + \alpha\omega_hS + \omega_h^2}$$

Taking $\omega_h = 1/RC$

A_0 = gain, ω_h = upper cut off freq, α = damping co-efficient

$\alpha = (3-A_0)$.

↓

damping co-efficient

put $S = j\omega$, we get

$$H(j\omega) = \frac{A_0 \omega_h^2}{\left(\frac{j\omega}{\omega_h}\right)^2 + \alpha \omega_h (j\omega) + \omega_h^2}$$

* by ω_h^2 on num & denom

$$= \frac{A_0}{(j\omega/\omega_h)^2 + j\alpha(\omega/\omega_h) + 1}$$

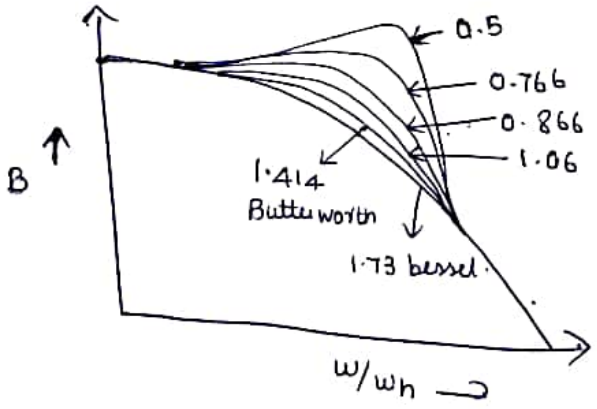
Normalized expression for LPF is

$$H(j\omega) = \frac{A_0}{S_n^2 + \alpha S_n + 1} \quad ; \quad S_n = j\left(\omega/\omega_h\right)$$

expression of magnitude in dB fa T.F is

$$20 \log |H(j\omega)| = 20 \log \left| \frac{A_0}{1 + j\alpha(\omega/\omega_h) + (j\omega/\omega_h)^2} \right|$$

$$= 20 \log \frac{A_0}{\sqrt{\left(1 - \frac{\omega^2}{\omega_h^2}\right)^2 + \left(\frac{\alpha\omega}{\omega_h}\right)^2}}$$



chebyshev

only fa $\alpha > 1.7$ response is stable.

If α is reduced, response exhibits overshoot & ripple begins to appear.

If α is reduced further, the filter becomes oscillatory.

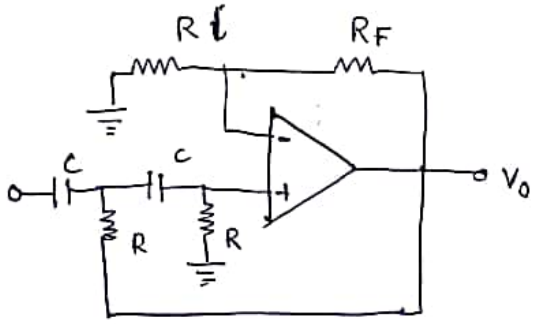
HIGHER ORDER LPF

Second order LPF provides - 40 dB/ decade roll off rate. roll off rate increases by increasing order of filter. Each increase in order produces - 20 dB/decade additional increase in roll off rate.

BUTTER WORTH POLYNOMIAL

1	$S_n + 1$
2	$S_n^2 + 1.414 S_n + 1$
3	$(S_n + 1)(S_n^2 + S_n + 1)$
4	$(S_n^2 + 0.765 S_n + 1)(S_n^2 + 1.618 S_n + 1)$

HIGH PASS ACTIVE FILTER



complement of LPF

HPF configuration is obtained by simply interchanging R & C in LPF

put $Y_1 = Y_2 = SC$; $Y_3 = Y_4 = G = 1/R$

The Transfer fn is written as

$$H(S) = \frac{A_0 S^2}{S^2 + (3 - A_0)\omega_l S + \omega_l^2}$$

where $\omega_l = 1/RC$

(or)

$$H(S) = \frac{A_0}{1 + (3 - A_0)\frac{\omega_l}{S} + \left(\frac{\omega_l}{S}\right)^2}$$

If $S = 0$, $H = 0$

$S = \infty$; $H = A_0$

The circuit acts as HPF

put $S = j\omega$ in above eqn

$$H(j\omega) = \frac{A_0}{1 + \frac{\omega_l}{j\omega}(3 - A_0) + \left(\frac{\omega_l}{j\omega}\right)^2}$$

Magnitude eqn of HPF is gvn by

$$|H(j\omega)| = \frac{A_0}{\sqrt{1 + \left(\frac{f_l}{f}\right)^4}}$$

BAND PASS FILTER

There are two types of BPF

(i) Narrow band pass filter ($Q > 10$)

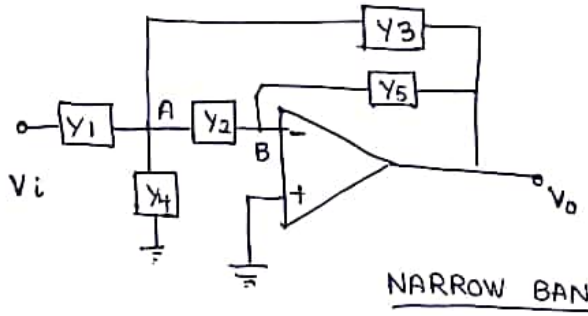
(ii) wide band pass filter ($Q < 10$).

$$Q = \frac{f_0}{BW} = \frac{f_0}{(f_H - f_l)} \quad \text{where } f_0 = \sqrt{f_h \cdot f_l}$$

f_h = upper cut off freq f_l = lower cut-off freq

f_0 = central freq.

Band pass configuration



op-amp is in inverting mode of operation.

NARROW BAND PASS FILTER

node voltage eqn at node A is

$$V_i Y_1 + V_0 Y_3 = V_A (Y_1 + Y_2 + Y_3 + Y_4). \quad \text{—(1)}$$

$V_B = 0$ (virtual ground), node voltage eqn at node B is

$$V_A Y_2 = -V_0 Y_5$$

$V_n = -V_o(Y_5/Y_2)$ sub in ①

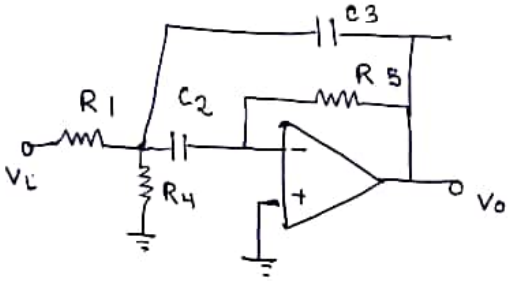
we get

$$V_i Y_1 + V_o Y_3 = -\frac{V_o Y_5 (Y_1+Y_2+Y_3+Y_4)}{Y_2}$$

$$V_i Y_1 = V_o \left[-\frac{Y_2Y_3 + Y_1Y_5 + Y_2Y_5 + Y_3Y_5 + Y_4Y_5}{Y_2} \right]$$

$$\frac{V_o}{V_i} = \frac{-Y_1Y_2}{Y_2Y_3 + Y_1Y_5 + Y_2Y_5 + Y_3Y_5 + Y_4Y_5}.$$

put $Y_1 = G_1$, $Y_2 = SC_2$, $Y_3 = SC_3$, $Y_4 = G_4$ & $Y_5 = G_5$



$$H(S) = \frac{V_o(S)}{V_i(S)} = \frac{-SG_1C_2}{S^2C_2C_3 + S(C_2+C_3)G_5 + SG_5(G_1+G_4)}$$

This Transfer function is equivalent to gain expression of parallel RLC circuit given by.

$$\frac{V_o(S)}{V_i(S)} = -\frac{G'}{Y} = -\frac{G'}{SC + G_1 + 1/SL}$$ comparing we get

$G' = G_1$

$L = \frac{C_2}{G_5(G_1+G_4)}$

$G_1 = \frac{G_5(C_2+C_3)}{C_2}$

$C = C_3$

resonance freq.

$$\omega_0^2 = 1/LC = \frac{G_5(G_1+G_4)}{C_2C_3}$$

At resonance, imaginary part is zero.

∴ gain at resonance is

$$\left.\frac{V_0}{V_i}\right|_{\omega=\omega_0} = -\frac{G_1'}{G_1} = -\frac{(G_1/G_5)C_2}{C_2+C_3}$$

$$= -\frac{(R_5/R_1)C_2}{C_2+C_3}$$

Q factor at resonance is $Q_0 = \frac{\omega_0 L}{R} = \omega_0 RC = \frac{\omega_0 C}{G_1} = \frac{\omega_0 C_2 C_3}{(C_2+C_3)G_1}$

B.W is given by $B.W = f_h - f_l = \frac{f_0}{Q_0} = \frac{\omega_0}{2\pi Q_0}$

$$= \frac{\omega_0}{2\pi R \omega_0 C} = \frac{1}{2\pi RC} = \frac{G_1}{2\pi C}$$

$$= \frac{G_5(C_2+C_3)}{2\pi C_2 C_3}$$

centre frequency $f_0 = \sqrt{f_h \cdot f_l}$

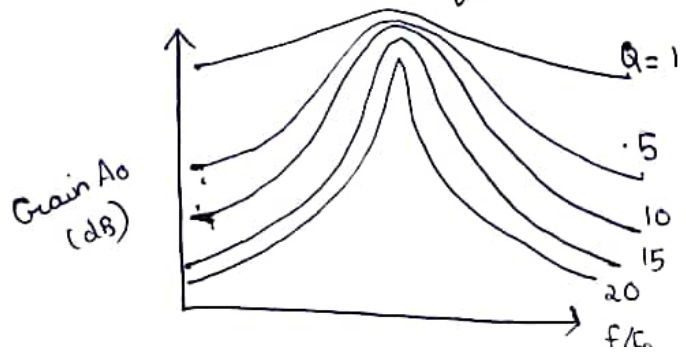
If $C_2 = C_3 = C$, then $\left.\frac{V_0}{V_i}\right|_{\omega=\omega_0} = -\frac{R_5}{2R_1} = -A_0$

$$\omega_0 = \frac{\sqrt{G_5(G_1+G_4)}}{C}$$

$$BW = \frac{G_5}{\pi C} = \frac{1}{\pi R_5 C}$$

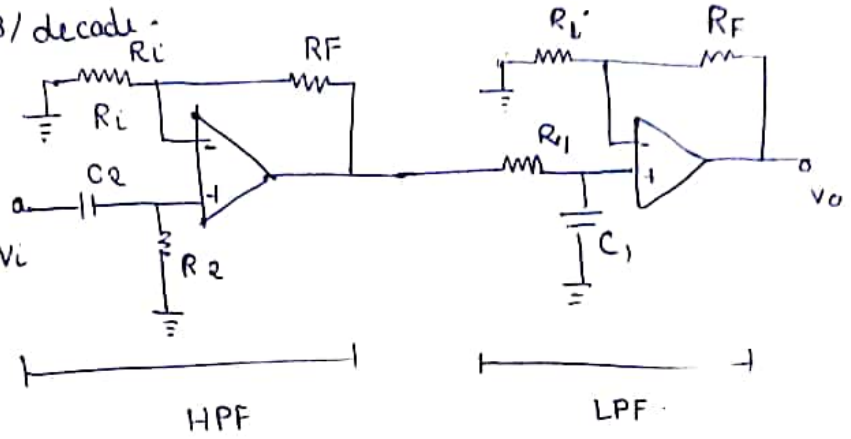
choose one parameter arbitrarily among C, G_1, G_4 & G_5

higher the Q, sharper the filter



WIDE - BAND PASS FILTER

It is formed by cascading HPF & LPF Section. If LPF & HPF are of first order, BPF will have roll off rate of -20 dB/decade.



↳ 1st order HPF, but previously we derived H(jω) for 2nd order HPF

For HP Section, magnitude of gain is

$$|H_{HP}| = \frac{A_{01}\,(f/f_\ell)}{\sqrt{1+(f/f_\ell)^2}} \quad \text{where } f_\ell = \frac{1}{2\pi R_2 C_2}$$

For LP section, magnitude of gain is

$$|H_{LP}| = \frac{A_{02}}{\sqrt{1+(f/f_h)^2}} \quad \text{where } f_H = \frac{1}{2\pi R_1 C_1}$$

magnitude gain of BPF is product of that of LPF & HPF.

$$|H_{BP}| = \left| \frac{A_0\,(f/f_\ell)}{\sqrt{\left(1+(f/f_\ell)^2\right)\left[1+(f/f_h)^2\right]}} \right|$$

where $A_0 = A_{01} \times A_{02}$

In similar fashion Second order HPF & LPF are cascaded to get -40 dB/decade fall-off rate

BAND REJECT FILTER

A band reject filter can be either

(i) Narrow band reject (ii) wide band reject.

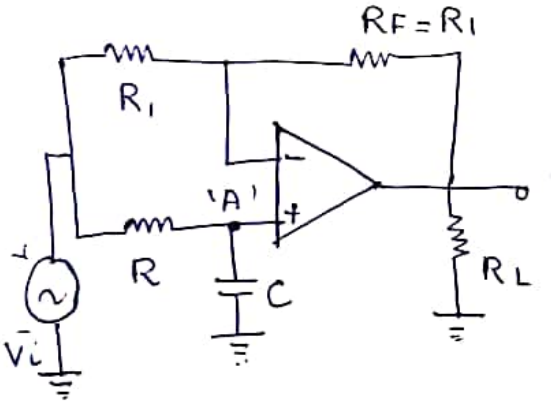
Narrow band reject filter is called notch filter. It rejects a single frequency.

There are several ways to make notch filter. one way is to subtract band pass output from its i/p. other way is to use a twin-T network cascaded with voltage follower

ALL PASS FILTER

passes all frequencies of input signal with out attenuation and provides desired phase shifts at diffrn frequencies of input signal

when signals are transmitted over transmission lines such as telephone wires, they undergo change in phase. These phase changes are compensated by all pass filter. So they are called as delay equalizers or phase correctors



here $R_F = R_1$

V_o is obtained by using superposition theorem

$$V_o = -\frac{R_F}{R_1} V_i + \left(1 + \frac{R_F}{R_1}\right) V_a \quad ; \; V_a \rightarrow \text{voltage at node 'A'} \quad \text{— (1)}$$

But $R_F = R_1$

$$\boxed{V_o = -V_i + 2V_a} \quad \text{— (2)}$$

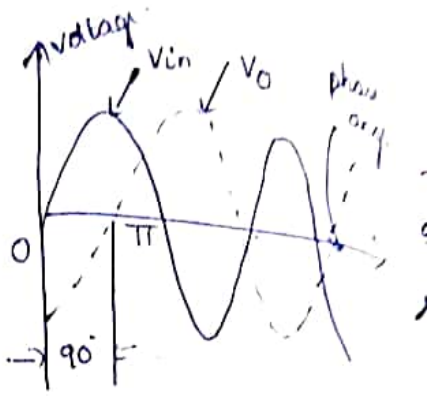
where $V_a = \left(\frac{-jX_c}{R - jX_c}\right) V_i$

$$V_o = -V_i + 2\left(\frac{-jX_c}{R - jX_c}\right) V_i$$

$\therefore$ num & den by $-jX_C$

$$= V_i\left(-1 + \frac{2}{1+j2\pi fRC}\right)$$

$$\therefore \frac{V_o}{V_i} = \left(\frac{1-j2\pi fRC}{1+j2\pi fRC}\right)$$



magnitude of $\frac{V_o}{V_i}$ is given by

$$\frac{|V_o|}{|V_i|} = \frac{\sqrt{1+(2\pi fRC)^2}}{\sqrt{1+(2\pi fRC)^2}} = 1$$

$\therefore |V_o| = |V_i|$ for all frequencies

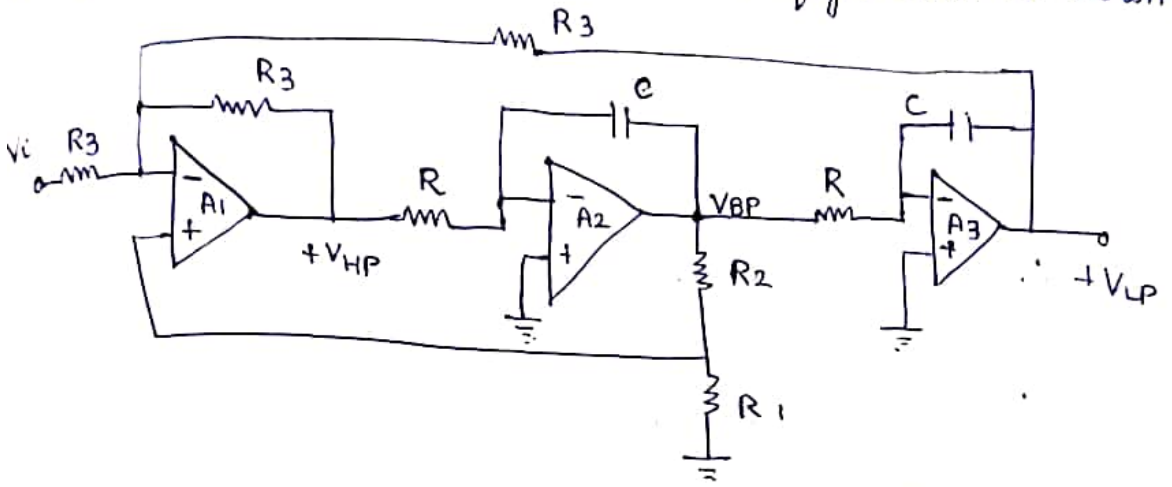
$$\varphi = -\tan^{-1} 2\pi fRC - \tan^{-1} 2\pi fRC$$

$$= -2\tan^{-1}(2\pi fRC).$$

φ can be varied with frequency for given R and C, and can be varied from 0 to -180° as freq varied from 0 to ∞. As phase shift is -ve, V_o lags V_i phase shift can be made +ve by interchanging R and C

STATE VARIABLE FILTER

State variable configuration uses two op amp integrators and one op-amp adder to provide simultaneous second order low pass, band pass & high pass filter responses. Simple state variable configuration is shown below



It uses two op-amp integrators [A2, A3] and one op amp summer [A1]. outputs V_{HP}, V_{BP}, V_{LP} of high pass, band-pass and low-pass filters are obtained at o/p of A_1, A_2 & A_3

V → laplace Transform of v in time domain.

A_2 works as inverting integrator, laplace tranformed output V_{BP} is given by

$$V_{BP} = -\frac{1}{RCs} V_{HP}$$ if $R = 1M\Omega$; $C = 1\mu F$; $RC = 1$, we get,

$$V_{BP} = -\frac{1}{s} V_{HP}$$

A_3 is also inverting integrata A_3;

$$V_{LP} = -\frac{1}{s} V_{BP} = \frac{1}{s^2} V_{HP}$$

op-amp A_1 is three input summer. o/p V_{HP} can be

written using superposition theorem

$$V_{HP} = -\left(\frac{R_3}{R_3}\right)V_i - \left(\frac{R_3}{R_3}\right)V_{LP} + \left(1 + \frac{R_3}{R_3 \| R_3}\right)\left(\frac{R_1}{R_1+R_2}\right)V_{BP}$$

$$= -V_i - V_{LP} + 3\left(\frac{R_1}{R_1+R_2}\right)V_{BP}$$

put $\alpha = 3\left(\frac{R_1}{R_1+R_2}\right)$

$$\therefore V_{HP} = -V_i - V_{LP} + \alpha V_{BP} \quad \left[\text{Sub } V_{LP} = \frac{1}{S^2}V_{HP} \text{ \& } V_{BP} = \frac{1}{S}V_{HP}\right]$$

$$\therefore \boxed{V_{HP} = -V_i - \frac{V_{HP}}{S^2} - \frac{1}{S}\alpha V_{HP}}$$

$$V_{HP}\left(1 + \frac{\alpha}{S} + \frac{1}{S^2}\right) = -V_i$$

high pass Transfer function H_{HP} is

$$H_{HP} = \frac{V_{HP}}{V_i} = \frac{-S^2}{S^2+\alpha S+1}$$

$\alpha \rightarrow$ damping factor

comparing this eqn with std HP Transfer fn $\frac{A_0 S^2}{S^2+\alpha\omega_l S+1}$

we have $\boxed{A_0 = -1}$ & $\boxed{\omega_l = 1}$

From Transfer fn eqn of LPF we have TF $= \frac{A_0}{S^2+\alpha\omega_h S+\omega_l}$

$$\therefore H_{LP} = \frac{V_{LP}}{V_i} = \frac{-1}{S^2+\alpha S+1}$$

where $A_0 = -1$

$\omega_h = 1$

Finally Band - pass impulse response is obtained by eliminating V_{HP} & V_{LP}.

$$H_{BP} = \frac{V_{BP}}{V_i} = \frac{S}{S^2 + \alpha S + 1}$$

Standard BPF T.F is given by $\frac{A_0 \alpha \omega_0 S}{S^2 + \alpha \omega_0 S + \omega_0^2}$

comparing we get $A_0 \alpha \omega_0 = 1$;

$$\omega_0 = 1/RC = 1$$

$$\therefore A_0 = 1/\alpha = \frac{R_1 + R_2}{3R_1}$$

from analysis, W.F.T BPF response is obtained by integrating HP response & L.P is generated by integrating band pass.

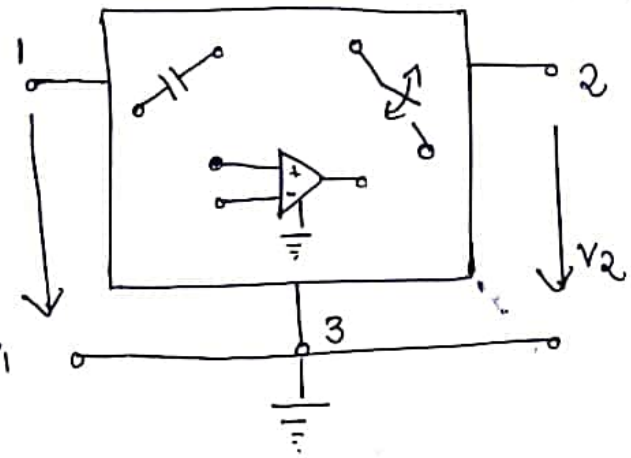
SWITCHED CAPACITOR FILTERS

(i) The resistor value needed for RC filters are generally too large

(ii) Large value resistors occupies large amount of chip area & have poor linearity characteristics

(iii) This is the reason for not using active filters in MOS technology.

(iv) Switched capacitor filter offers an attractive alternative to RC active filter.



(iv) This is a three terminal element with capacitor, switches & op amps.

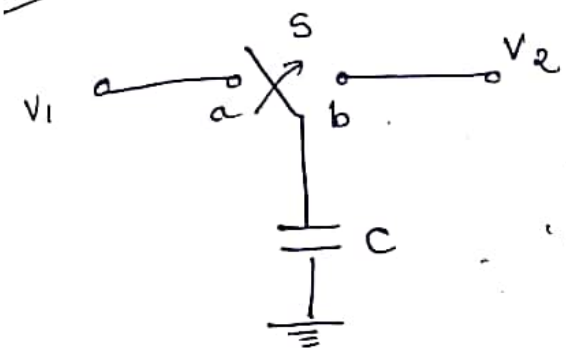
(vi) not possible to achieve desired RC products of sufficient magnitude & accuracy unless switched capacitor filter is used.

(vii) In switched capacitor filter it is achieved by setting capacitor ratios & switch periods

(viii) large resistor values required for active filter are achieved by combination of small value capacitors (Say 10PF) & MOS switching transistors

(vii) Thus even a filter of high order becomes an integrated circuit of very small size with low power consumption. It is more reliable & low price.

Realization of Resistor by Single capacitor



Initially switch is in position 'a'. capacitor is charged to V_1

Then switch is thrown to position 'b'. capacitor is discharged to V_2

$V_2 < V_1$

amount of charge $Q = C(V_1 - V_2)$

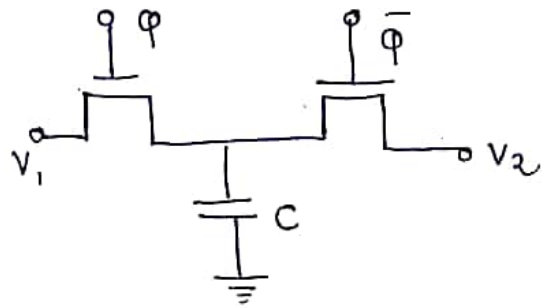
S is thrown back every T_{CK} second, then i that flows through is gvn by

$$i = \frac{Q}{T_{CK}} = \frac{C(V_1 - V_2)}{T_{CK}} = f_{CK}\, C\, (V_1 - V_2)$$

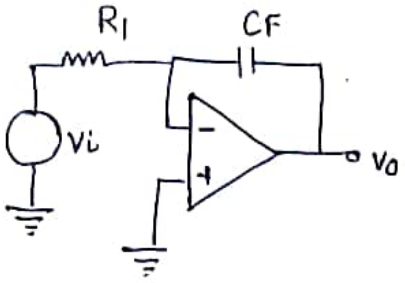
$T_{CK} \rightarrow$ clock period

$f_{CK} = 1/T_{CK}$.

Resistance R is gvn by $R = \frac{T_{CK}}{C} = \frac{1}{f_{CK} \cdot C}$.



SWITCHED CAPACITOR INTEGRATOR



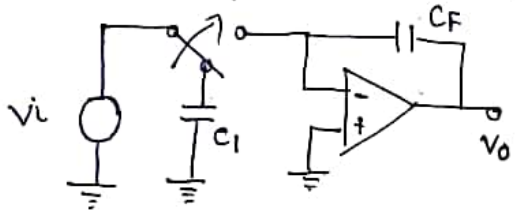
ordinary integrata

Transfer function is

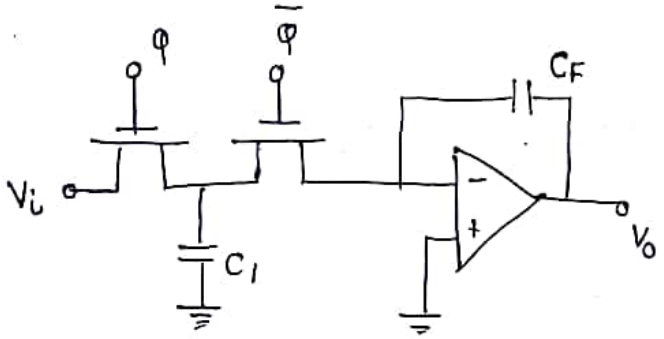
$$H = -\frac{1}{sR_1C_F} = -\frac{1}{j(f/f_0)}$$

where $f_0 = \frac{1}{2\pi R_1 C_F}$

R_1 replaced by Switched capacita C_1



The MOS version.



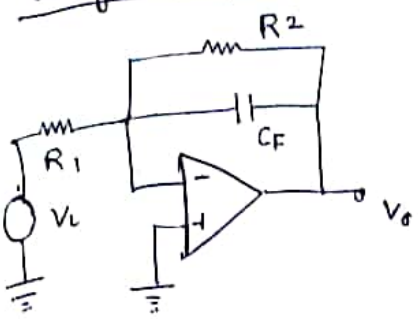
here $R_1 = \frac{1}{C_1 f_{ck}}$

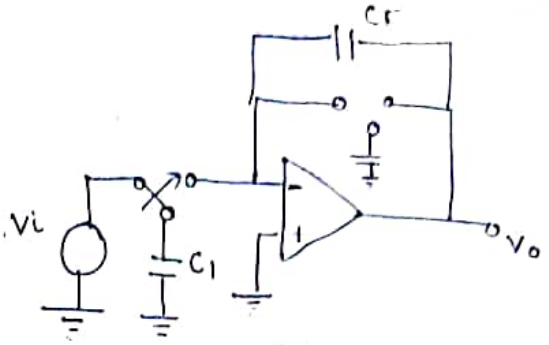
f_{ck} → clock frequency.

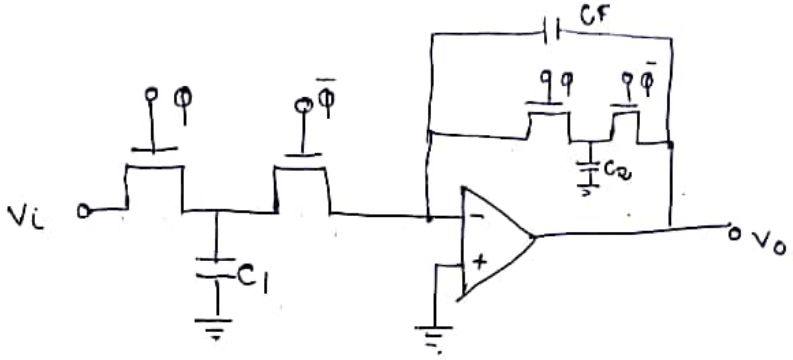
f_0 is given by $f_0 = \frac{C_1}{2\pi C_f} f_{CK}$

By proper choice of f_{CK} and C_1/C_F, it is possible to avoid use of high capacitance value even if low values of f_0 are desired.

Lossy integrator







$$R_2 = \frac{1}{f_{ck} C_2} \quad ; \quad R_1 = \frac{1}{f_{ck} C_1}$$

$$\frac{R_2}{R_1} = \frac{C_1}{C_2}$$

$$f_h = \frac{1}{2\pi C_F R_2} = \frac{1}{2\pi} \frac{C_2}{C_F} f_{ck}$$

SWITCHED CAPACITOR FILTER ICS

MF5 - Universal second order filter

MF6 - Unity gain Sixth order Butterworth LP filter

MF8 - Two second order BP filter.

MF10 - State variable filter IC.

VOLTAGE REGULATOR

provides stable dc voltage for powering electronic circuits.

voltage regulators are classified as.

(i) Series regulator

(ii) switching regulator

Series regulator

It uses a power transistor connected in series between unregulated dc i/p & load. O/p voltage is controlled by voltage drop taking place across series pass transistor. Since Transistor operates in linear region, it is called linear regulator

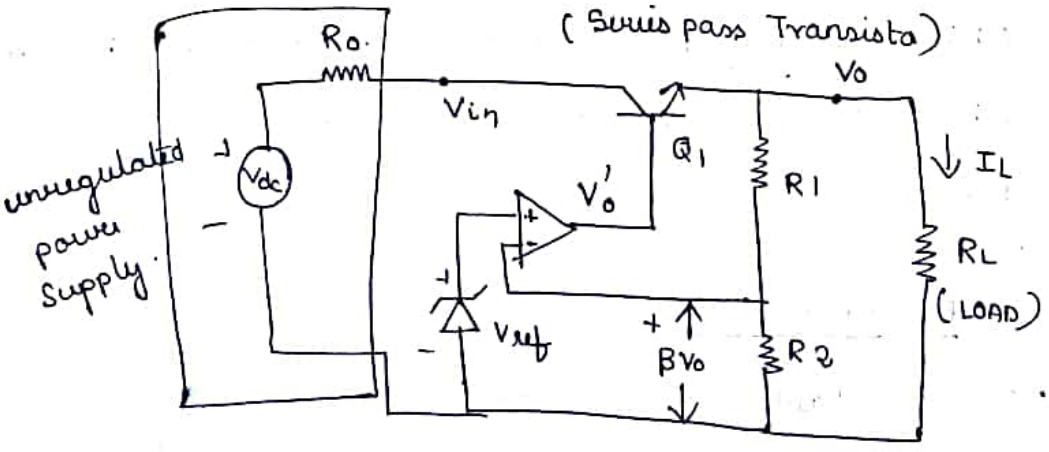
Switching regulators

They operate power transistor as high freq on/off switch, so that power transistor does not conduct current continuously. This has improved efficiency

SERIES OP-AMP REGULATOR - LINEAR VOLTAGE REGULATOR

circuit consists of four parts

(i) Reference voltage circuit
(ii) Error amplifier
(iii) Series pass transistor
(iv) feedback network



Q_1 is in series with unregulated dc voltage V_{in} & regulated output voltage V_o.

So it must absorb the difference between these two voltage whenever fluctuation in V_o occurs

Q_1 is also connected as emitter follower. Therefore it provides sufficient current gain to drive the load

o/p voltage is sampled by $R_1 - R_2$ divider & feedback to (-) terminal of op amp error amplifier

This sampled voltage is compared with reference voltage V_{ref}.

o/p V_o' drives the Q_1

If o/p voltage ↑ due to variation in load current the sampled voltage βV_o increases where

$$\beta = \frac{R_2}{R_1 + R_2}$$

This reduces o/p voltage V_o' due to 180° phase difference provided by op-amp amplifier

V_o' is applied to base of Q_1, which is used as emitter follower. V_o follows V_o', so V_o also reduces. hence increase in V_o is nullified, i.e. reduction in o/p voltage also gets regulated.

IC VOLTAGE REGULATORS

IC voltage regulators are versatile, relatively inexpensive and available with features such as programmable o/p, current/ voltage boosting & floating operation for high voltage application.

Types:

(i) fixed positive / negative o/p voltage regulators

(ii) adjustable o/p voltage regulato

fixed voltage regulators:

78XX series are three terminal positive fixed voltage regulators.

78XX
↳ used to identify o/p voltage of regulator

79XX series are negative fixed voltage regulators.

ADJUSTABLE O/P VOLTAGE REGULATOR:

These are regulated voltage sources which are variable.

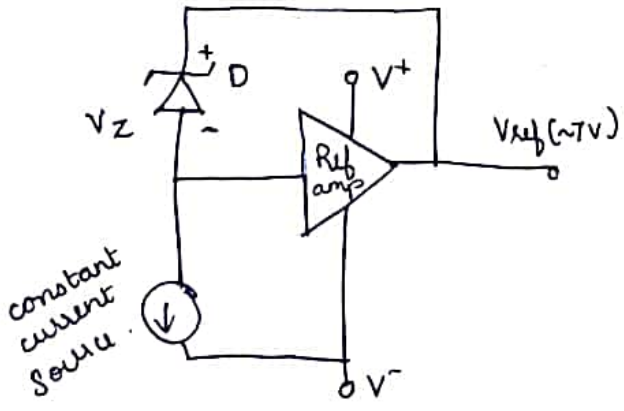
Adjustable positive voltage regulator: LM117, LM317
Adjustable negative voltage regulator: LM137, LM337

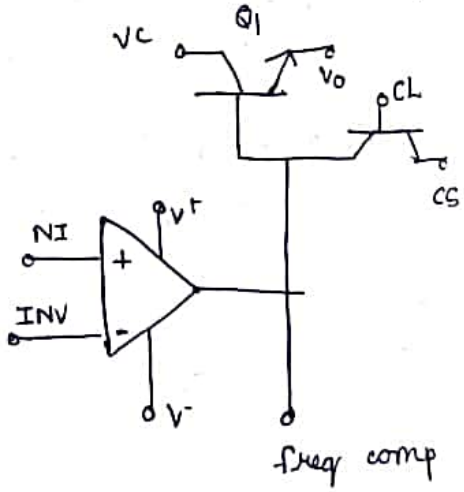
723 GENERAL PURPOSE REGULATOR

The regulators discussed earlier have following limitations

(i) No short circuit protection.

This limitation is overcome in 723, which can be adjusted over wide range of both positive or negative regulated voltage.





(Section 1)

limitation is no - inbuilt thermal protection.

It has two seperate Sections.

Zener diode, a constant current Source and reference amplifier produces fixed voltage of 7 volts at terminal Vref.

constant current source forces the zener to operate at fixed points. So zener outputs a fixed voltage.

other section consists of an error amplifier, series pass transistor Q_1 and current limit transistor Q_2. error amp. compares sample of o/p voltage applied at INV input terminal to reference voltage. Vref applied at NI terminal

error signal controls conduction of Q_2.

These sections are not internally connected. but various points are brough out on IC package.

IC 723 can be used to realize both

(i) Low voltage regulator.

(ii) high voltage regulator.

SWITCHING REGULATOR:

disadvantage of Series regulator

(i) To give unregulated dc voltage as i/p, Step down transformer is used which is bulky & expensive

(ii) large values of filter capacitors are required

(iii) i/p voltage must be greater than o/p voltage. greater the difference in i/p - o/p voltage, more will be the power dissipated as series pass transistor is always in active region

(iv) one dc Supply voltage is enough for TTL but where as for op-amp ±15V is needed

In switched mode regulator, pass transistor acts as control switch and operates in either cut-off or saturated state

power transmitted is discrete, rather than steady current when pass device is cutoff, no current & dissipates no power when pass device is in saturation - max current is given to load & power wasted is little hence effecency is high.

bridge rectifier & capacitor filter - converts ac to unregulated dc.

Thermistor Rt - limits high initial capacitor charging current

reference voltage regulator - is series pass regulator & provides power supply voltage for all other circuits

[power loss in series pass reg is very less, hence it do not affect

over all efficiency

Q_1 & Q_2 are alternatively switched ON or OFF so they dissipate very little power. They drive primary of Transformer.

Secondary is centre tapped & full wave rectification is achieved by D_1 & D_2

V_o is sampled by $R_1 R_2$ divider and fraction is compared with V_{ref} in comparator 1.

o/p of voltage comparison is $V_{control}$ which is applied to (-) input terminal of comparator 2 & Δ^{lar} wave form is applied to +ve terminal

comparator 2 acts as Pulse width modulator & o/p is square wave V_A

width of V_A varies with $V_{control}$ which in turn varies with V_o

40KHz OSC cascaded with F.F. to produce V_Q & $\bar{V}_Q$.

V_{A1} and V_{A2} are o/p of AND gates A_1 and A_2.

They are applied to base of Q_1 and Q_2.

depending on whether Q_1 or Q_2 is on, waveform at i/p of transformer will be Square wave.

If $V_o \uparrow$, $V_{control} \uparrow$, which decreases T_1 in turn decreases pulse width driving main power transform...

SWITCHING REGULATOR!

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UNIT-V

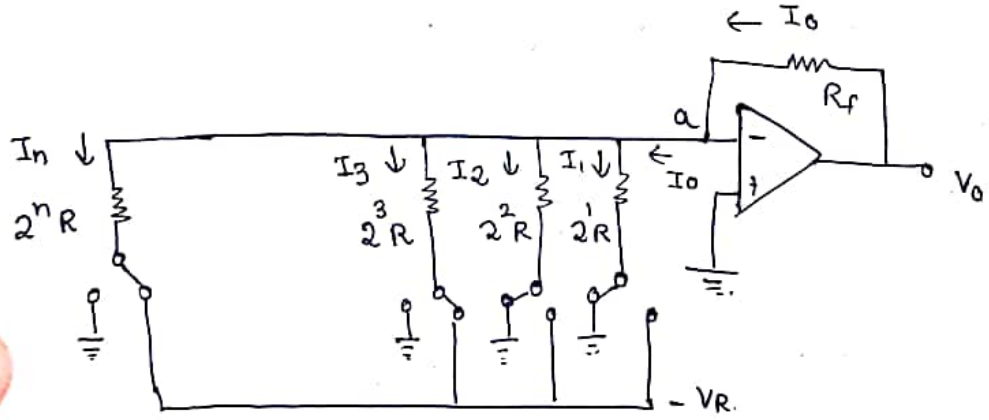
DATA CONVERSION DEVICES

for processing, transmission & storage, it is often convenient to express analog values in digital form because it gives better accuracy and reduces noise

DAC Types

(i) weighted resista DAC
(ii) R-2R ladder
(iii) Inverted R-2R ladder.

WEIGHTED RESISTOR DAC



Summing amplifier with binary weighted resistor network. It has n-electronic switches $d_1, d_2 \ldots d_n$ connected by binary input word. They are Single pole double throw (SPDT) type. If binary i/p is 1, it connects resistance to reference voltage ($-V_R$) And if input bit is 0, switch connects resistor to ground

$$I_0 = I_1 + I_2 + \cdots + I_n$$

$$= \frac{V_R}{2R} d_1 + \frac{V_R}{2^2 R} d_2 + \cdots + \frac{V_R}{2^n R} d_n$$

$d_1 d_2 \cdots d_n$ - n bit binary word.

$$\therefore = \frac{V_R}{R}\left[d_1 2^{-1} + d_2 2^{-2} + \cdots d_n 2^{-n}\right].$$

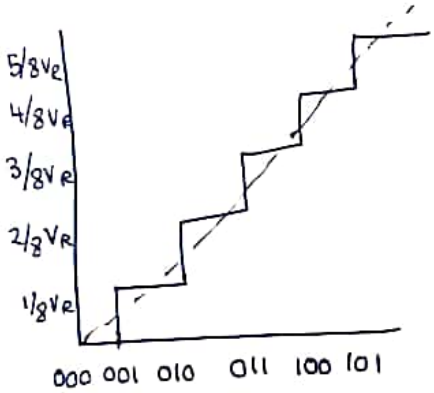
output voltage

$$V_0 = I_0 R_f$$

$$= V_R \frac{R_f}{R}\left[d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{-n}\right].$$

reference voltage is -ve

∴ positive staircase is obtained



circuit shown is connected in inverting mode.

It can also be connected in non inverting mode.

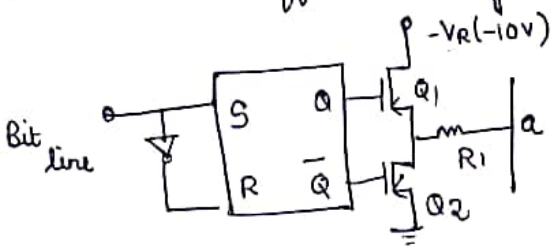
op-amp acts as I to V converter.

Accuracy & Stability of DAC depends on accuracy of resistors

disadv (i) wide range of resistors used.

(ii) for better resolution binary word length should be large.

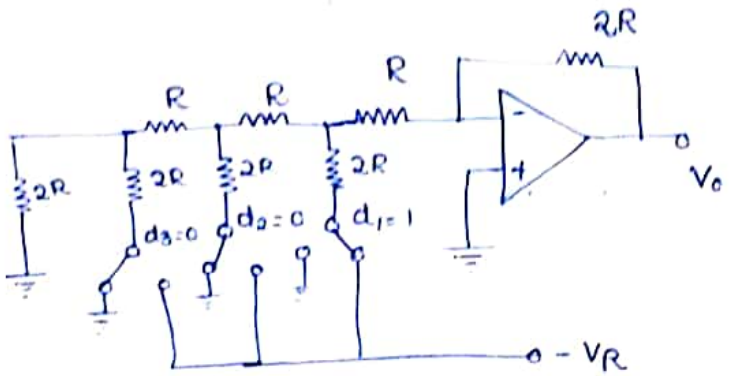
Bipolar transistor donot perform well as voltage switches hence by using totem pole MOSFET SWITCH low ON resistance & zero offset voltage can be achieved



R - 2R LADDER DAC

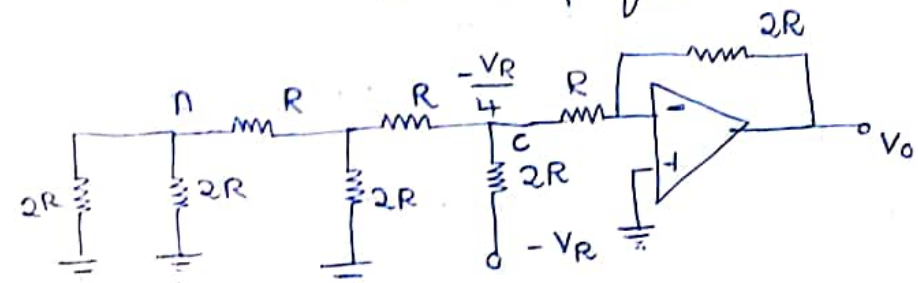
wide range of resistors are required in binary weighted resistor type DAC. Thus is, avoided by using R-2R ladder type DAC where only two values of resistors are required.

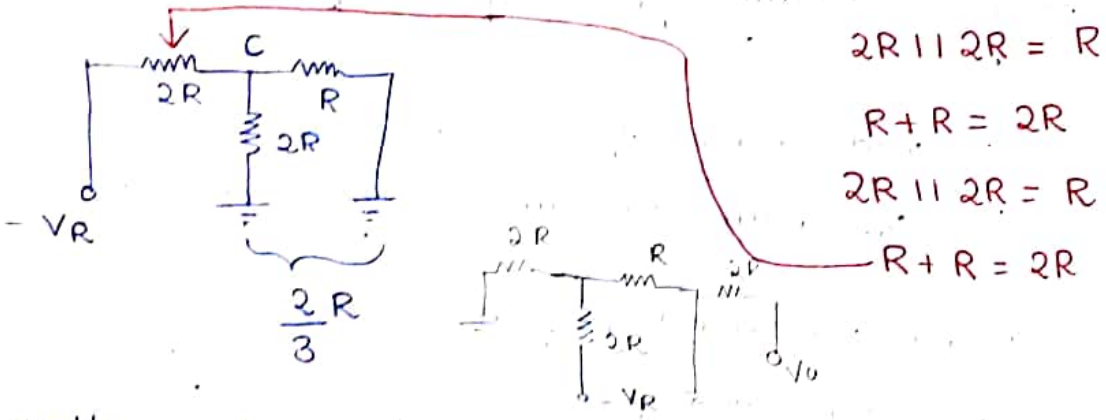
consider 3 bit DAC as shown below



Switch position $d_1 d_2 d_3$ corresponds to binary word 100

The circuit can be simplified as shown below





$2R \parallel 2R = R$

$R + R = 2R$

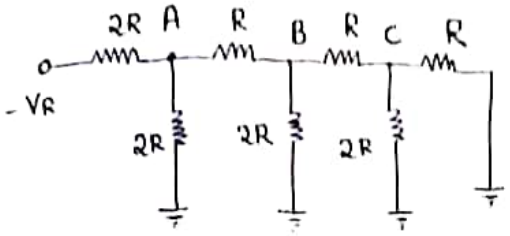
$2R \parallel 2R = R$

$R + R = 2R$

voltage at node C can be calculated as

$$\frac{-V_R\left(\frac{2R}{3}\right)}{2R + \frac{2R}{3}} = -\frac{V_R}{4}$$

The output voltage $V_0 = \frac{-2R}{D}\left(\frac{-V_R}{1}\right) = V_R = V_{FS}$



At A

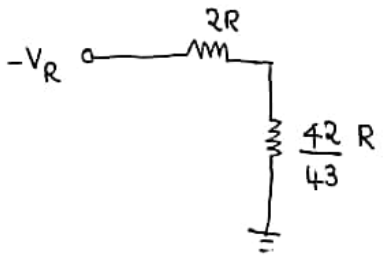
$(R \parallel 2R) = \frac{2R^2}{3R} = \frac{2}{3}R$; series with R

$\frac{2}{3}R + R = \frac{5R}{3}$; $\parallel^l$ with 2R

$$\frac{\left(\frac{5R}{3}\right)2R}{\frac{5R}{3}+2R} = \frac{10R}{11}$$

series with R ; $\frac{10R}{11} + R = \frac{21R}{11}$

$\parallel^l$ to 2R ; $\frac{\left(\frac{21R}{11}\right)2R}{\frac{21}{11}R+2R} = \frac{42}{43}R$

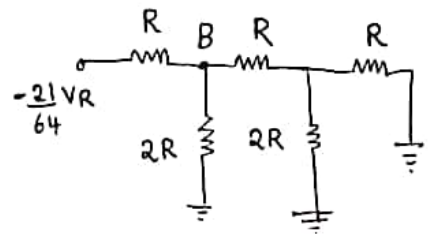


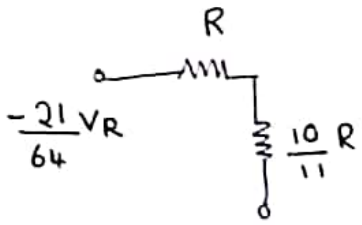
voltage at A $= -V_R \times \frac{\frac{42}{43}R}{\frac{42}{43}R+2R}$

$= -V_R \times \frac{21}{64}$

$V_A = -\frac{21}{64}V_R$

At B

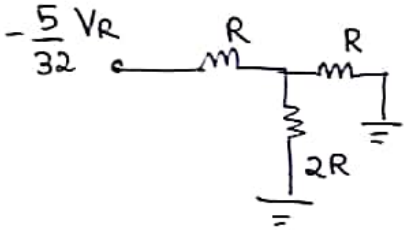




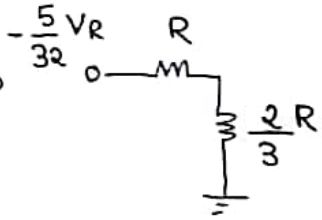
$$V_B = \frac{-\frac{21}{64}V_R \times \frac{10}{11}R}{\frac{10}{11}R + R}$$

$$= \frac{-\frac{21}{64}V_R \times \frac{10}{11}R}{\frac{21}{11}R}$$

$$= -\frac{10V_R}{64} = -\frac{5}{32}V_R$$



$\Rightarrow$

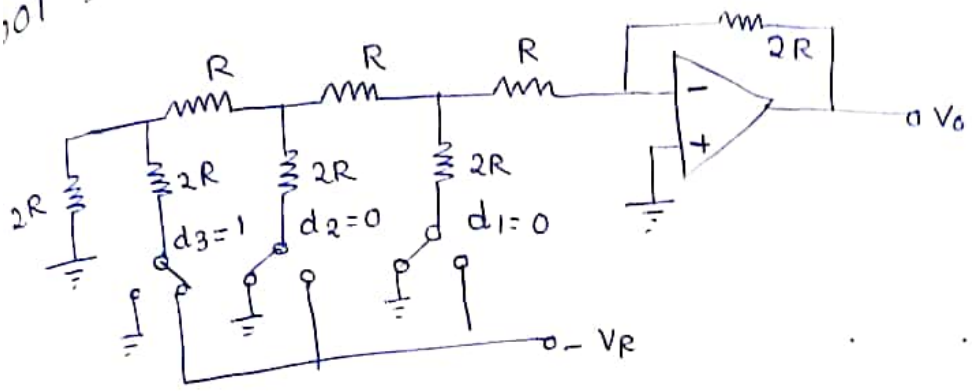


$$\Rightarrow V_C = \frac{-\frac{5}{32} \times \frac{2}{3}R}{\frac{2}{3}R + R} = \frac{-\frac{5}{32} \times 2R}{5R}$$

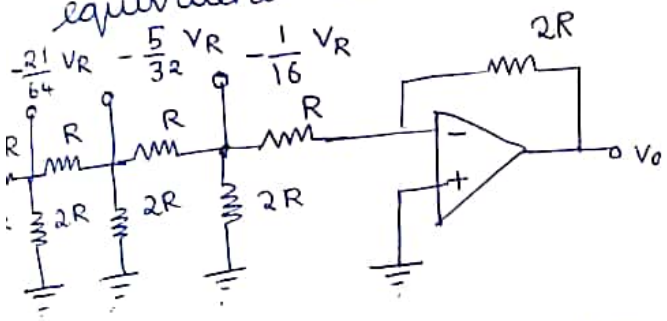
$$V_C = -\frac{1}{16}V_R$$

The output voltage $V_o = \frac{-2R}{R}\left(\frac{-V_R}{4}\right) = \frac{V_R}{2} = \frac{V_{FS}}{2}$

The switch position corresponding to binary word 101 in 3 bit DAC is shown in circuit below



equivalent circuit is



The output voltage eqn for this circuit is given by.

$$V_o = \frac{-2R}{R}\left(\frac{-V_R}{16}\right) = \frac{V_R}{8} = \frac{V_{FS}}{8}$$

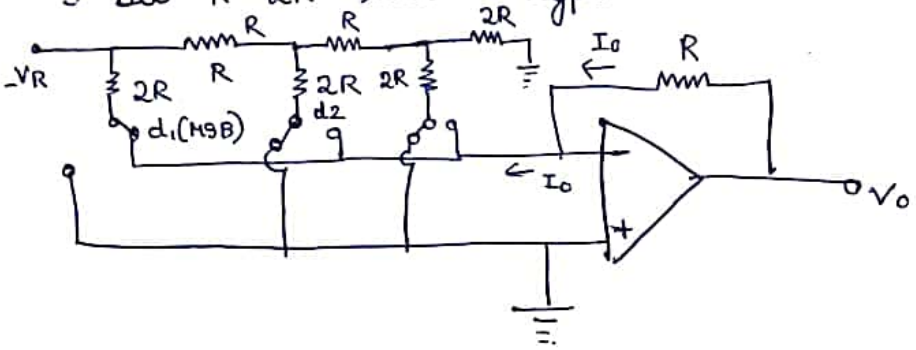
In similar fashion, output voltage for R-2R ladder type DAC corresponding to other 3 bit binary words can be calculated.

INVERTED R-2R LADDER

In weighted resistor type DAC and R-2R ladder type DAC, current flowing in resistor changes as input data changes

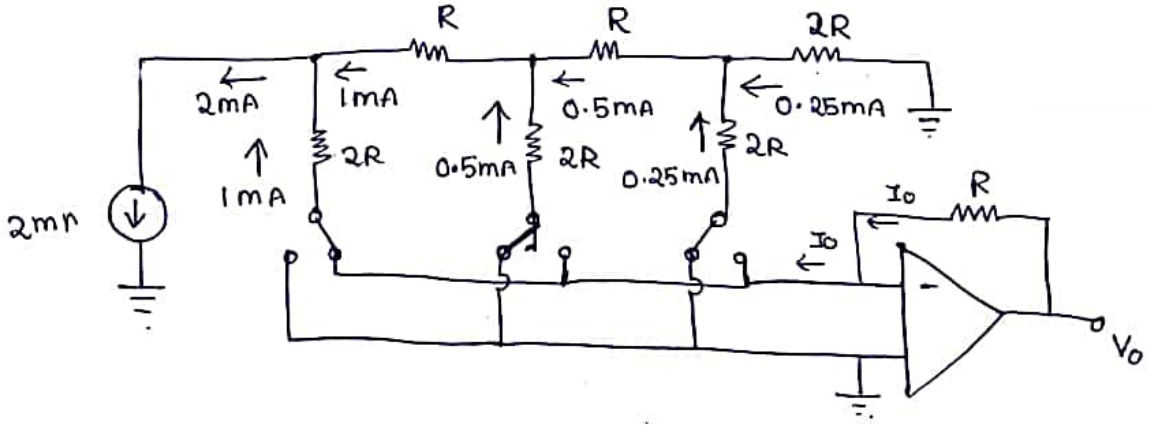
More power dissipation causes heating, which in turn creates non linearity in DAC.

3 bit R-2R ladder type DAC is shown below



each input binary word corresponds switch either to ground or to inverting input terminal of opamp which is at virtual ground.

Since both terminals of switches d_i are at ground potential, current flowing in the resistances is constant and independent of switch position (or) independent of input binary word.



The circuit has important property that the current divides equally at each of the nodes. This is because equivalent resistance to the right or to the left of any node is exactly 2R

equal division of current in successive nodes remains the same in Inverted R-2R ladder irrespective of input binary word

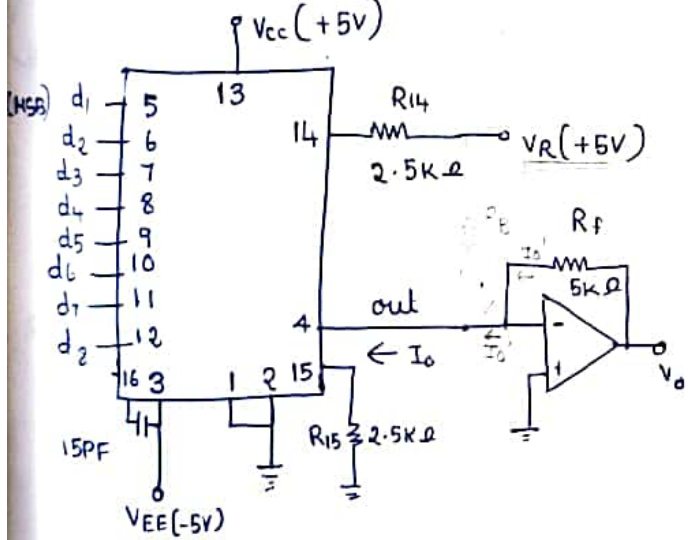
constant current implies constant voltage. The ladder node voltages remains constant at $\frac{V_R}{2^0}, \frac{V_R}{2^1}, \frac{V_R}{2^2}$

Most important advantage is that since ladder node voltage remains constant, the stray capacitance are not able to produce slow down effects on performance of circuit

Switches are SPDT Switches

MONOLITHIC DAC

Monolithic DAC consist of R-2R ladder, Switches & feedback resistors. 8, 10, 12, 14 & 16 bit resolution are available for various manufacturers.



It has 8 data lines d_1 to d_8

It requires 2mA reference current for full scale i/p & two power Supplies $V_{CC} = +5V$ & $V_{EE} = -5V$

Reference current is determined by resista R_{14} & V_R

$$\& \quad I_R = \frac{V_R}{R_{14}} = \frac{5V}{2.5K} = 2mA$$

$R_{15} = R_{14}$ match i/p impedance of reference Source.

$$I_0 = \frac{V_R}{R_4}\left(\sum_{i=1}^{8} d_i\, 2^{-i}\right); \quad d_i = 0 \text{ a } 1$$

fa full Scale i/p d_8 through $d_1 = 1$

$$\therefore I_0 = \frac{5V}{2.5K\Omega}\left(\sum_{i=1}^{8} 1\times 2^{-i}\right) = 2mA\left(\frac{255}{256}\right) = 1.992_{,}$$

O/p voltage for full scale i/p is

$$V_0 = 2mA(255/256)\times 5K\Omega$$

$$V_0 = 9.961\ V$$

In general O/p voltag is gvn by

$$V_0 = \frac{V_R}{R_{14}} R_f\left[\frac{d_1}{2}+\frac{d_2}{4}+\cdots\frac{d_8}{256}\right]$$

The DAC can be calibrated for bipolar range from -5V to +5V by adding R_B between V_R & o/p pin 4. $R_B = 5K\Omega$;. current applied $(= V_R/R_B = 1mA)$ in opposite direction of current generated by i/p signal.

$$\therefore I_0' = I_0 - (V_R/R_B) = (V_R/R_{14})\left(\sum_{i=1}^{8} d_i 2^{-i}\right) - (V_R/R_B$$

for binary i/p word = 00000000

O/p voltage

$$V_0 = I_0' R_f = (I_0 - V_R/R_B)R_f = \left(0 - \frac{5V}{5K\Omega}\right)\times 5K\Omega$$

$$= -5V$$

for binary i/p word = 10000000

$$V_0 = (I_0 - V_R/R_B)R_f = \left[\left(V_R/R_{14}\right)\left(d_1/2\right) - \left(V_R/R_B\right)\right]R_f$$

$$= \left(\frac{5V}{2.5K\Omega}\right)\left(\frac{1}{2}\right) - \left(\frac{5V}{5K\Omega}\right)\Big] 5K\Omega$$

$$= [1mA - 1mA]\ 5K\Omega = 0V$$

for binary input word = 11111111

$$V_0 = \left[\left(\frac{V_R}{R_{14}}\right)\left(\frac{255}{256}\right) - \left(\frac{V_R}{R_B}\right)\right] R_f$$

$$= [1.9992\,mA - 1mA]\, 5k\Omega$$

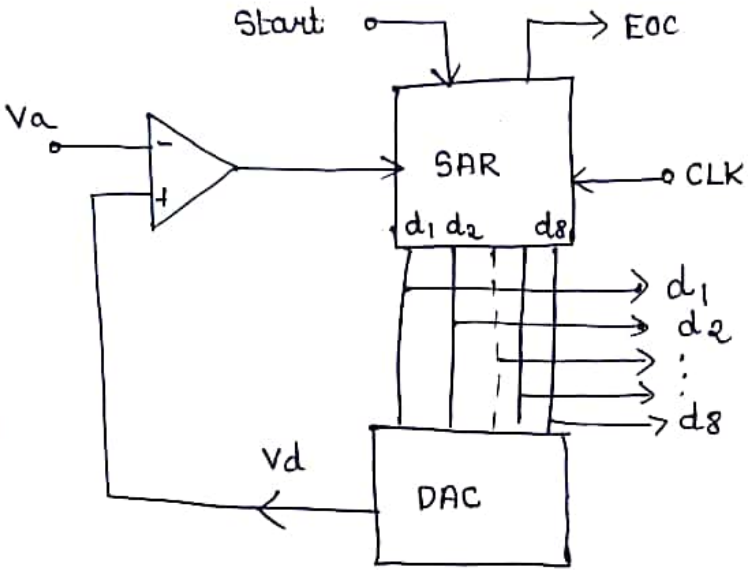
$$= 0.992\,mA \times 5k\Omega$$

$$= +4.960\,V$$

SUCCESSIVE APPROXIMATION ADC

Successive approximation technique uses a very efficient code search strategy to complete n-bit conversion in n-clock periods.

eight bit converter requires eight clock pulses to obtain a digital o/p



circuit uses SAR (Successive approximation register) to find the required value of each bit by trial & error.

With the arrival of "Start" command, SAR sets MSB $d_1 = 1$ with all other bits zero so that the trial code is 10000000.

o/p Vd of DAC is now compared with analog i/p Va

If Va > Vd, then 10000000 is less than correct digital representation

MSB is left at '1' and next MSB is made '1' & further tested

If Va < Vd, then 10000000 is greater than correct digital representation.

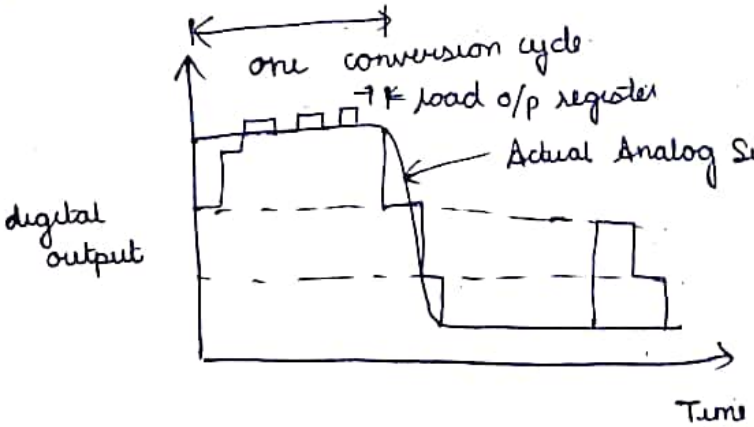
So reset MSB to '0' & go to next lower significant bit

The procedure is repeated for all subsequent bits one at a time, until all bit positions have been tested

correct digital representation	SAR o/p at different Stages in conversion (Vd)	comparator o/p
11010100	10000000	1
	11000000	1
	11100000	0
	11010000	1
	11011000	0
	11010100	1
	11010110	0
	11010101	0
	11010100	

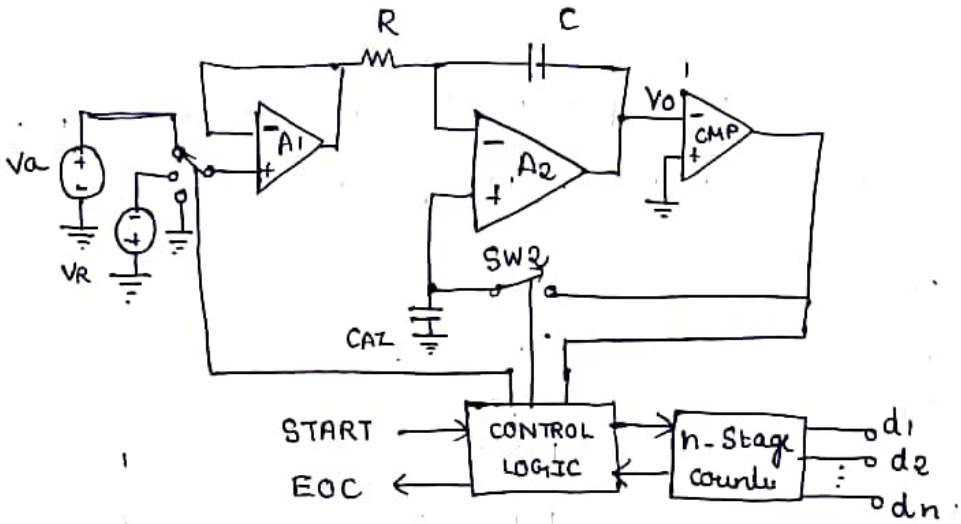
It requires eight pulses to establish the accurate output regardless of the value of analog input

one additional clock is used to load the output register and reinitialize the circuit



DUAL SLOPE ADC

- Integrating type ADC



$A_1 \rightarrow$ high input impedance buffer

$A_2 \rightarrow$ precision integrator

CMP - voltage comparator

The converter first integrates the analog input signal Va for fixed duration of 2^n clock periods.

Then it integrates an internal reference voltage V_R of opposite polarity until integrator output is zero.

The Number of clock cycles N required to return the integrator to zero is proportional to value of Va averaged over the integration period.

Hence N represents desired O/P code.

Before START command arrives, SW1 is connected to ground & SW_2 is closed.

Any offset voltage present in A_1, A_2, comparator loop after integration, appears across C_{AZ} till the threshold of the comparator is achieved

Thus CAZ provides automatic compensation for input offset voltages of all the three amplifiers.

Later when SW_2 opens, C_{AZ} acts as memory to hold the voltage required to keep the offset null.

At arrival of START, at $t=t_1$, control logic opens SW_2 and connects SW_1 to V_a and enables counter starting from Zero.

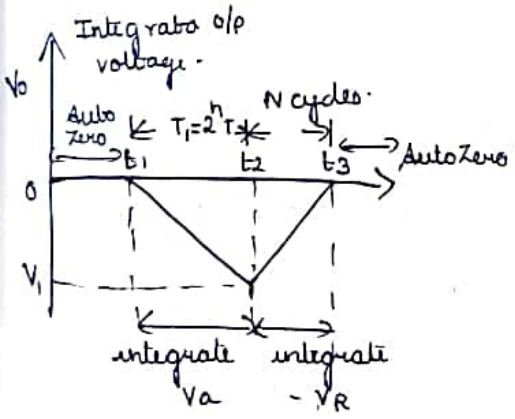
n-Stage counter is used, therefore counter resets to zero after counting 2^n pulses.

V_a is integrated for fixed number 2^n counts of clock pulses after which the counter resets to Zero.

If clock period is T, integration takes place for time $T_1 = 2^n \times T$ and o/p is ramp going downwards.

counter resets after T_1 & SW_1 is connected to reference voltage V_R

The output voltage V_o will now have a positive slope.



As long as V_o is -ve, o/p of comparator is +ve and control logic allows the clock pulse to be counted.

$V_o = 0$ at $t = t_3$, the control logic issues 'EOC' & no further clock pulse enter the counter.

Reading of counter at t_3 is proportional to analog input voltage V_a

$$T_1 = t_2 - t_1 = \frac{2^n \text{ counts}}{\text{clock rate}}$$

$$t_3 - t_2 = \frac{\text{digital count } N}{\text{clock rate}}$$

for integrator,

$$\Delta V_o = \left(-\frac{1}{RC}\right) V(\Delta t)$$

$V_o = V_1$ at t_2 & can be written as

$$v_1 = (-1/RC)\ V_a(t_2 - t_1)$$

voltage v_1 is also given by

$$v_1 = (-1/RC)(-V_R)(t_2 - t_3)$$

So; $V_a(t_2 - t_1) = V_R(t_3 - t_2)$

put $t_2 - t_1 = 2^n$; $t_3 - t_2 = N$

$\therefore V_a(2^n) = V_R(N)$

$$V_a = V_R\left(N/2^n\right).$$

(i) V_R & n are constant; $V_a \propto$ count reading N & is independent of R, C and T :

(ii) dual slope ADC integrates input signal to fixed time, hence it provides excellent noise rejection.

(iii) <u>disadvantage</u> : long conversion time

applications

(i) accurate measurement of slowly varying signals. such as thermocouples & weighing scales.