SRM
INSTITUTE OF SCIENCE & TECHNOLOGY
(Deemed to be University u/s 3 of UGC Act, 1956)

SRM Institute of Science and Technology
College of Engineering and Technology
DEPARTMENT OF ECE

SRM Nagar, Kattankulathur – 603203, Chengalpattu District, Tamilnadu

Academic Year: 2021-2022 (EVEN)

SET A

Test: CLAT-II
Course Code & Title: 18ECE206J Advanced Digital System Design
Year & Sem: II & IV
Max. Marks: 50

Answer Key

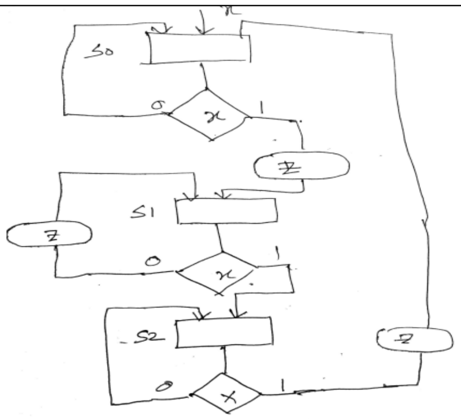
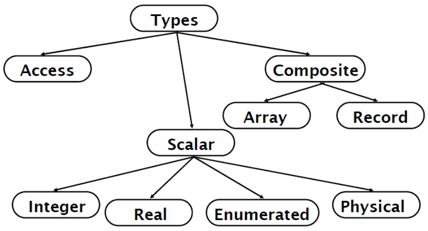
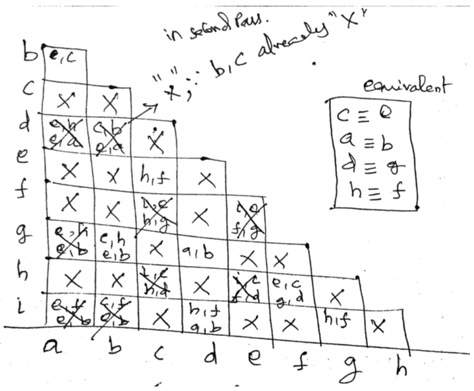
Part - A
(10 x 1 = 10 Marks)
Answer all

Q. No	Question	Mark	BL	CO	PO	PI Code
1	Component instantiation is done under ______ model. **a) Structural** b) Behavioral c)Switch d)Dataflow	1	1	2	2	2.3.1
2	The result of the shift operation : 1001010 **srl** 2 is a)0101000 **b) 0010010** c) 1001011 d)1111000	1	2	2	3	3.1.1
3	State reduction in the sequential circuit represents the reduction of **a)Number of flip flops** b) Number of OR gates c) Number of AND gates d)Number of Counters	1	1	2	2	2.3.1
4	Which one of the following is not the element of the ASM Chart? a)State box b)Decision box **c)Data box** d)Conditional box	1	1	2	3	3.1.1
5	A __________ can't be declared inside a process. **a)Signal** b)Variable c)Constants d)Subprograms	1	1	2	2	2.3.1

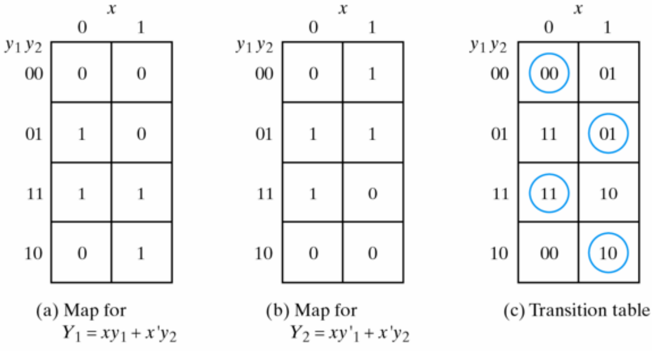
6	The following VHDL code represents
	process (A, B, S)
	begin
	if (S='1') then
	Z <= A;
	else
	Z <= B;
	end if;
	end process;
	a)4x2 encoder
	b)2x4 decoder
	c)2 x1 multiplexer
	d)1x4 demultiplexer
		1	2	3	3	3.2.1

7	If the states are named by letter symbol in transition table, then it is called _______ table. **a)Flow** b)Truth	1	1	3	2	2.1.1

	c)Look up d) FSM					
8	If the final stable state does not depend on the change order of state variable ,then it is said to be a)Critical race **b)Non critical race** c)Steady state d)Hazard	**1**	**1**	**3**	**2**	**2.1.1**
9	In asynchronous sequential circuit ,the output changes occur with the change of a **a)Input** b)Output c)Clock pulse d)Time	**1**	**1**	**3**	**2**	**2.1.1**
10	Which of the following expression remove hazard from: xy+zx′ ? a)xy+zx′ b)xy+zx′+wyz **c)xy+zx′+yz** d)xy+zx′+wz	**1**	**2**	**3**	**3**	**3.2.1**
Section B1 (2 x 10 = 20 Marks) Answer any two questions						
11	**i)List of sequential statements:** wait statement assertion statement report statement signal assignment statement variable assignment statement procedure call statement if statement case statement loop statement next statement exit statement return statement null statement **Explanation in any three statements** **ii) concurrent statement:** The operations in real systems are executed concurrently. The VHDL language models real systems as a set of operation that operate concurrently **Any one example for concurrent statements**	**2** **3** **1** **4**	**2**	**2**	**2**	**2.3.1**
12	**i) ASM chart**	**5**	**3**	**2**	**3**	**3.2.1**

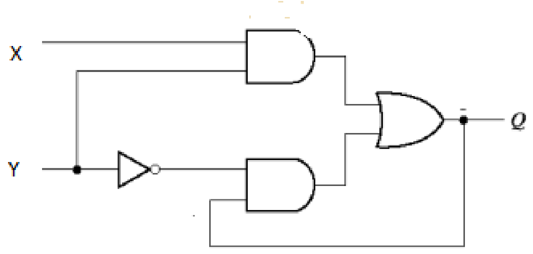
	 x S0 0 x 1 Z S1 Z 0 x 1 S2 Z 0 x 1 **ii)VHDL Data types:**  Types Access Composite Array Record Scalar Integer Real Enumerated Physical (2) **Compare signal and variable: (any three) (3)** • Variables can only be used inside processes, signals can be used inside or outside processes. • Variables need to be defined after the keyword process but before the keyword begin. Signals are defined in the architecture before the begin statement. • Variables are assigned using the := assignment symbol. Signals are assigned using the <= assignment symbol. • Variables that are assigned immediately take the value of the assignment. Signals depend on if it's combinational or sequential code to know when the signal takes the value of the assignment.(3)					
13	i) **Implication chart**  in second pass. " " X ; : b,c already "X" equivalent c ≡ e a ≡ b d ≡ g h ≡ f b c d e f g h i a b c d e f g h **Reduced State Table:** **Present Next state output**	**4**	**2**	**2**	**3**	**3.1.1**

	state X=0 X=1 **a c c 1** **c i f 0** **d f a 1** **f c d 0** **i f b 1** ii) **State assignment and its type** State assignment :to assign unique coded binary values to the states.(1) Types : (1) - Binary - Gray - One hot assignment	**4** **1** **1**				
	Section B2 (2 x 10 = 20 Marks) **Answer any two questions**					

14	**(i)Race condition and its type :**
	A race condition exists in an asynchronous circuit when two or more binary state variables change value in response to a change in an input variable. When unequal delays are encountered, a race condition may cause the state variable to change in an unpredictable manner
	Type 1: Noncritical race
	If the final stable state that the circuit reaches does not depend on the order in which the state variables change, the race is called a noncritical race
	Type 2: Critical race
	If the final stable state that the circuit reaches does depend on the order on which the state variables change, the race is called a critical race
	
	Any example:
	
	ii) analyze the following asynchronous sequential circuit
	
	y_1y_2 \ x: 0 1
	00: 0 0
	01: 1 0
	11: 1 1
	10: 0 1
	(a) Map for $Y_1 = xy_1 + x'y_2$
	
	y_1y_2 \ x: 0 1
	00: 0 1
	01: 1 1
	11: 1 0
	10: 0 0
	(b) Map for $Y_2 = xy'_1 + x'y_2$
	
	y_1y_2 \ x: 0 1
	00: 00 01
	01: 11 01
	11: 11 10
	10: 00 10
	(c) Transition table
		3
		
		2
		
		1(for a)
		1(for b)
		3(for c)
			3	**3**	**3**	**3.2.1**

15	**Primitive flow table:**	**5**	**4**	**3**	**3**	**3.2.1**

<table>
<tr>
<td></td>
<td>
<table>
<tr><td></td><td>00</td><td>xy
01</td><td>11</td><td>10</td></tr>
<tr><td>a</td><td>c , –</td><td>ⓐ , 0</td><td>b , –</td><td>– , –</td></tr>
<tr><td>b</td><td>– , –</td><td>a , –</td><td>ⓑ , 1</td><td>e , –</td></tr>
<tr><td>c</td><td>ⓒ , 0</td><td>a , –</td><td>– , –</td><td>d , –</td></tr>
<tr><td>d</td><td>c , –</td><td>– , –</td><td>b , –</td><td>ⓓ , 0</td></tr>
<tr><td>e</td><td>f , –</td><td>– , –</td><td>b , –</td><td>ⓔ , 1</td></tr>
<tr><td>f</td><td>ⓕ , 1</td><td>a , –</td><td>– , –</td><td>e , –</td></tr>
</table>
(4)

Reduced table (2)
<table>
<tr><td></td><td>00</td><td>01</td><td>11</td><td>10</td></tr>
<tr><td>a,b,c</td><td>ⓒ, 0</td><td>ⓐ, 0</td><td>b , –</td><td>ⓓ, 0</td></tr>
<tr><td>d,e,f</td><td>ⓕ, 1</td><td>a , –</td><td>ⓑ, 1</td><td>ⓔ, 1</td></tr>
</table>
Transition Table: (2)
<table>
<tr><td></td><td colspan="4">XY</td></tr>
<tr><td>q</td><td>00</td><td>01</td><td>11</td><td>10</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td></tr>
</table>
<b>Logic Diagram: (2)</b>


<b>Q=XY+Q Y’</b>
</td>
<td></td><td></td><td></td><td></td><td></td>
</tr>
<tr>
<td><b>16</b></td>
<td>Full adder design using two half adder circuit:

Circuit Diagram

Half adder program (any model) and or gate

Full adder using half adder
library IEEE;
Use IEEE. STD_LOGIC_1164.all;
entity fulladder IS
port (a,b,cin :in STD_LOGIC;
    sum,carry : out STD_LOGIC);
end fulladder;
architecture FA_arch of fulladder is</td>
<td><b>2</b>

<b>4</b>

<b>4</b></td>
<td><b>3</b></td>
<td><b>3</b></td>
<td><b>3</b></td>
<td><b>3.2.1</b></td>
</tr>
</table>

	component half_adder is
	port (p,q :in STD_LOGIC;
	s,cy: out STD_LOGIC);
	end component;
	component or_gate is
	port (p1,q1 :in STD_LOGIC;
	r1: out STD_LOGIC);
	end component;
	signal s1,c1,c2 : STD_LOGIC;
	begin
	w1: half_adder port map (a,b,s1,c1);
	w2: half_adder port map (s1,cin,sum,c2);
	w3: or_gate port map (c1,c2,carry);
	end FA_arch;					