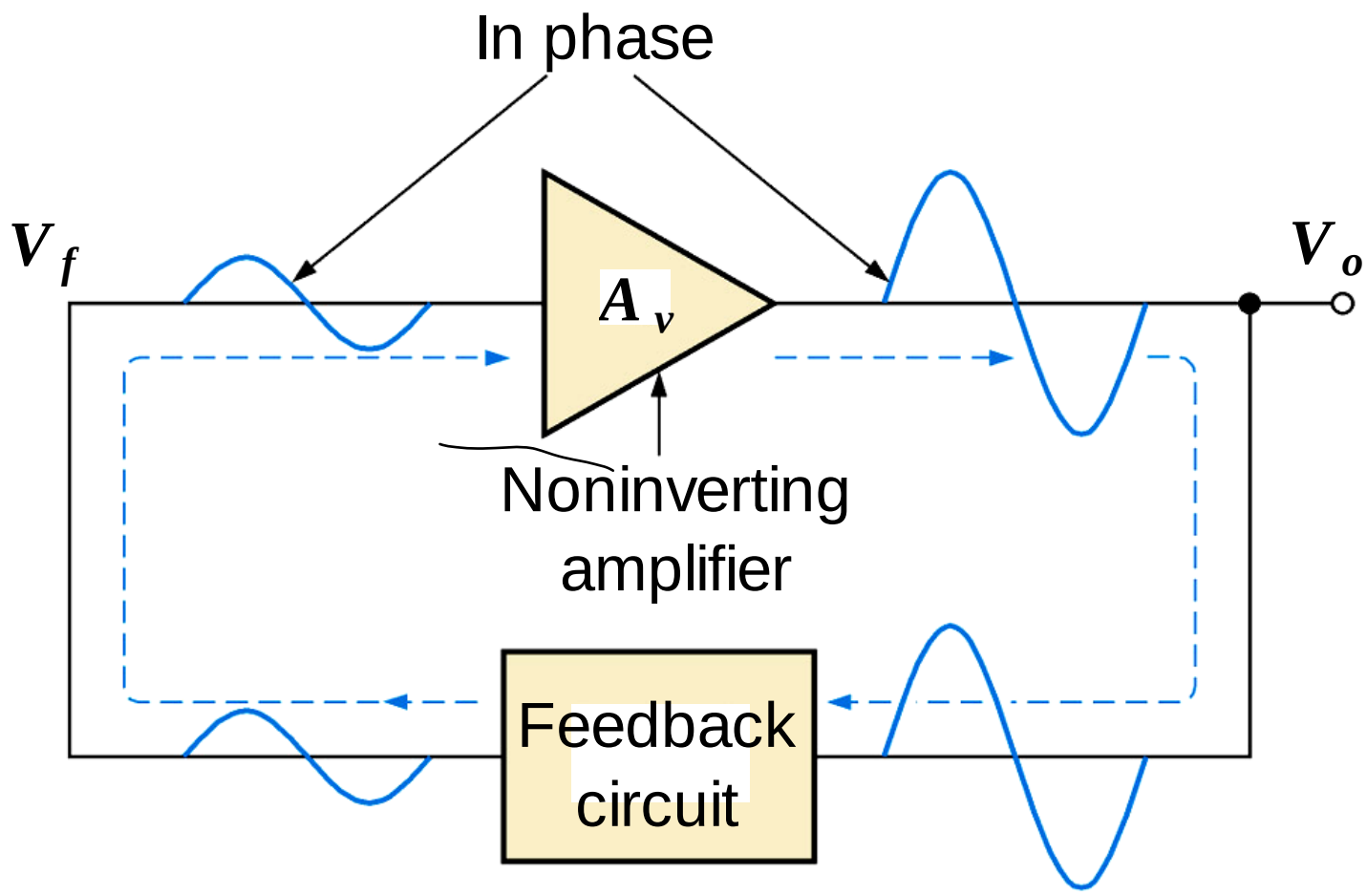
UNIT-III
Oscillators

Basic principles for oscillation

- The feedback oscillator is widely used for generation of sine wave signals.
- The positive (in phase) feedback arrangement maintains the oscillations.
- The feedback gain must be kept to unity to keep the output from distorting.

Basic principles for oscillation



Design Criteria for Oscillators

1. The magnitude of the loop gain must be unity or slightly larger

   – Barkhaussen criterion

$$\left|A\beta\right| = 1$$

2. Total phase shift, ϕ of the loop gain must be Nx360°

   where N=0, 1, 2, …

RC-Phase Shift Oscillator

- The circuit of an RC phase shift oscillator is shown in fig 1(a). The op-amp is used in the inverting mode and therefore provides 180 degree phase shift. The additional phase of 180 degree is provided by the RC feedback network to obtain a total phase shift of 360°.
- The feedback Network consists of three identical RC stages. Each of the RC stage provides a 60° phase shift so that the total phase shift due to feedback network is 180°.
- It is not necessary that all the three RC sections are identical so long the total phase shift is 180°.
- However, if we use non-identical stages, it is possible that the total phase shift is 180° for more than one frequency. This phenomenon can lead to undesirable inter-modal oscillations.
- The feedback factor B of the RC network can be calculated by writing the KVL equations from Fig 1 b).

RC-Phase Shift Oscillator

$$I_1\left(1+\frac{1}{sC}\right)-I_2R=V_O \qquad (1)$$

$$I_1R+I_2\left(2R+\frac{1}{sC}\right)-I_3R=0 \qquad (2)$$

$$0-I_2R+I_3\left(2R+\frac{1}{sC}\right)=6 \qquad (3)$$

$$V_f=I_3R \qquad (4)$$

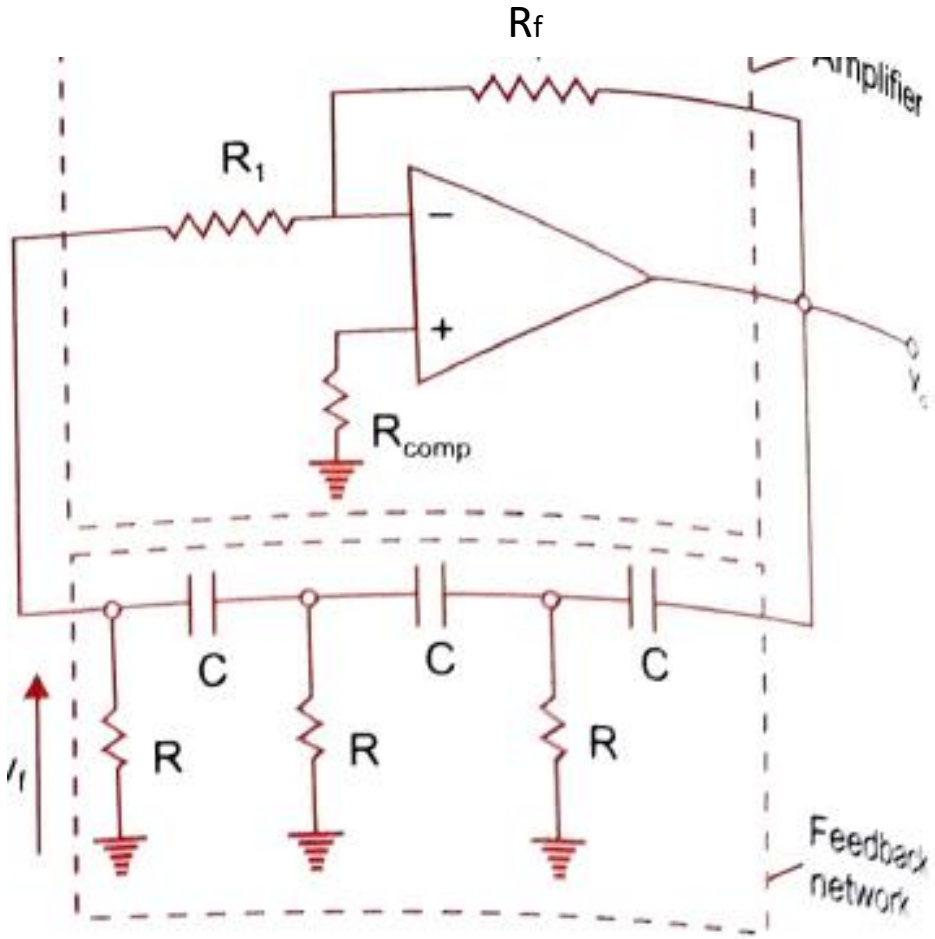


Fig :1 a) Phase shift oscillator

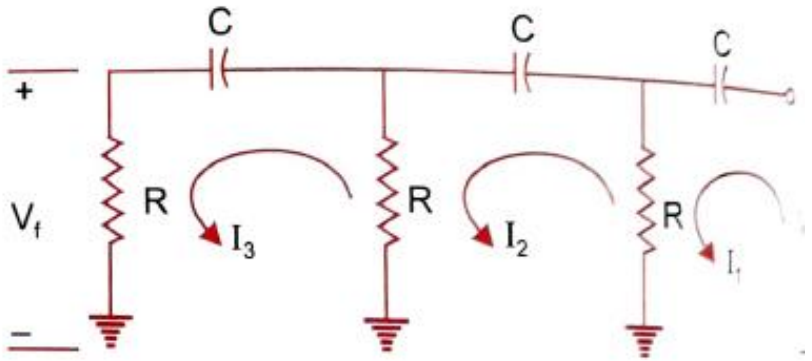


Fig :1 b) Calculating ß from the phase shift network

Solving equation (1), (2) and (3) for I3 , we get

$$I_3 = \frac{V_0 R^2 s^3 C^3}{1+5sRC+6s^2C^2R^2+s^3C^3R^3} \qquad (5)$$

$$V_f = I_3 R = \frac{V_0 R^3 s^3 C^3}{1+5sRC+6s^2C^2R^2+s^3C^3R^3} \qquad (6)$$

$$V_f = \frac{1}{1+\frac{6}{sRC}+\frac{5}{s^2C^2R^2}+\frac{1}{s^3C^3R^3}} \qquad (7)$$

Replace:

S = jw, $S^2 = -w^2$ and $S^3 = -jw^3$

$$\beta = \frac{1}{1-\frac{6}{jwRC}-\frac{5}{w^2C^2R^2}+\frac{1}{jw^3C^3R^3}} \qquad (8)$$

$$\beta = \frac{1}{(1-5\,\alpha^2)+j\alpha(6-\alpha^2)} \qquad (9)$$

$$\alpha = \frac{1}{wRC} \qquad (10)$$

For Aβ=1, β should be real, that is the imaginary term in eg.(9) must be zero. Thus

$$\alpha\left(6 - \alpha^2\right) \qquad (11)$$

$$\alpha^2 = 6$$
$$\alpha = \sqrt{6}$$
$$\frac{1}{wRC} = \sqrt{6}$$

The frequency of oscillation

$$f_0 = \frac{1}{2\pi RC\sqrt{6}}$$

$$\beta = -\frac{1}{29} \qquad (12)$$

- The negative sign indicates that the feedback network produces a phase shift of 180°.

So, $$|\beta| = \frac{1}{29}$$

Since $$|A\beta| \geq 1$$

Therefore, for sustained oscillations,

$$|A| \geq 29$$

- Gain of the inverting op – amp should be atleast 29, or Rf = 29 R1. The gain A is kept greater than 29 to ensure that variations in circuit parameters will not make < 1, otherwise oscillations will die out.
- For low frequencies (< 1kHz), op-amp 741 may be used, however, for high frequencies.
- LM 318 or LF 351 should be used.

Wien bridge oscillator

•Another commonly used audio frequency oscillator is a Wien bridge oscillator. The circuit is shown in Fig. 1.

•It may be noted that the feedback signal in this circuit is connected to the non-inverting (+) input terminal so that the op-amp is working as a non-inverting amplifier. Therefore, the feedback network need not provide any phase shift.

•The circuit can be viewed as a Wien bridge with a series RC network in one arm R and a parallel RC network in the adjoining arm. Resistors R and Rf are connected in the remaining two arms. The condition of zero phase shift around the circuit is achieved by balancing the bridge.

•The circuit has been redrawn to show the bridge network in Fig.2. The output ac signal of the op-amp amplifier is fed back to point A of the bridge. The feedback signal, Vf across the parallel combination R2,C2 is applied to the non-inverting input terminal of the o-pamp.

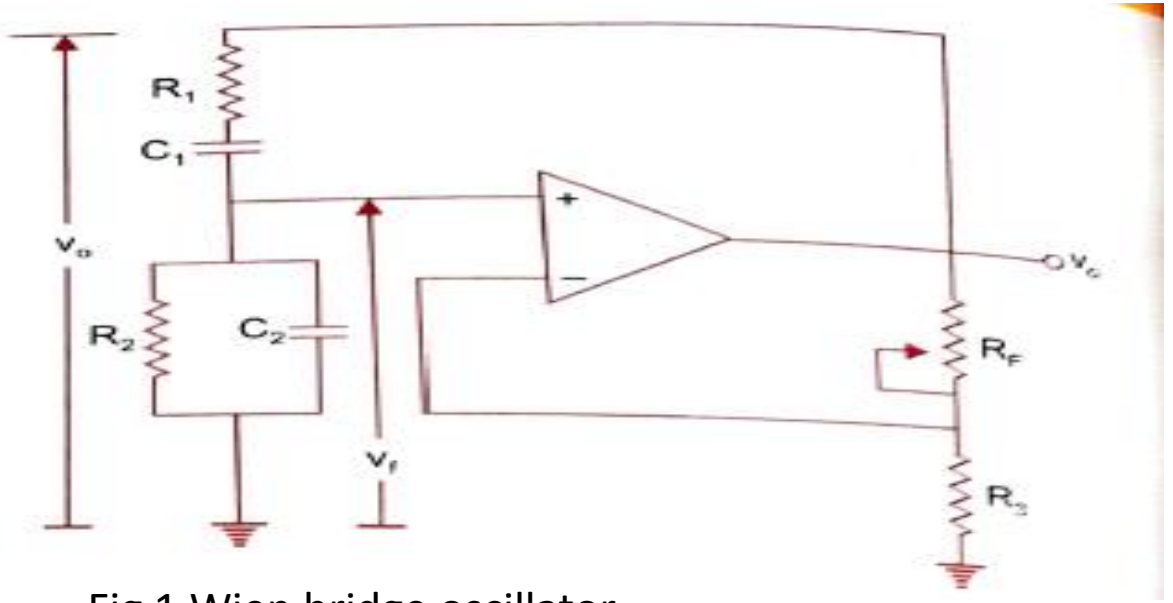


Fig 1 Wien bridge oscillator

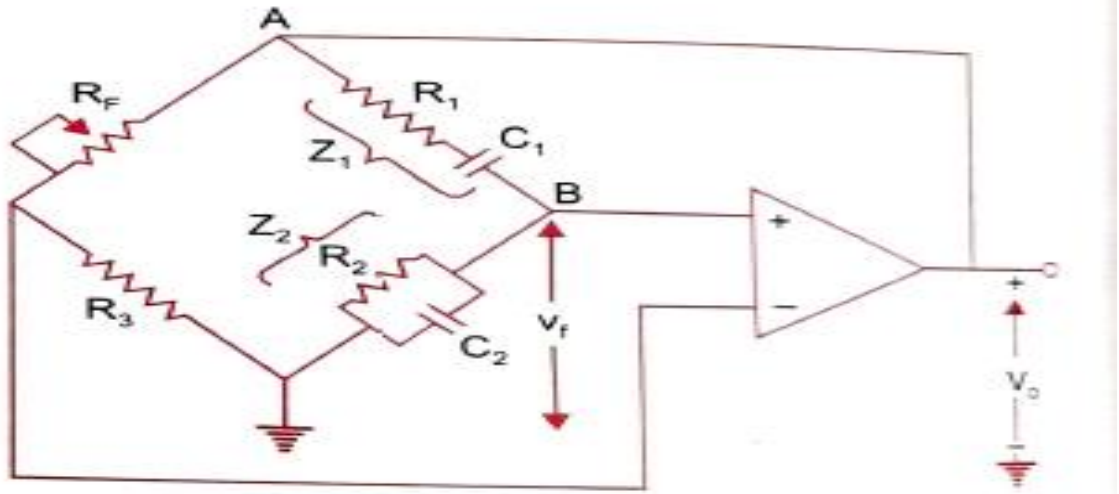


Fig 2 Wien bridge oscillator showing the bridge network

The gain of the op-amp amplifier is

$$A = 1 + \frac{R_F}{R_3} \qquad \text{.....(1)}$$

and feedback factor, B from Fig. 2 is

$$\beta = \frac{V_f}{V_o} = \frac{Z_2}{Z_1 + Z_2} \qquad \text{.....(2)}$$

where

$$Z_1 = R_1 + \frac{1}{sC_1} = \frac{sR_1C_1 + 1}{sC_1} \qquad \text{.....(3)}$$

$$Z_2 = \frac{R_2}{1 + sR_2C_2} \qquad \text{.....(4)}$$

Putting the values of Z_1 and Z_2 in equation (2) we get

$$\beta = \frac{R_2/(1 + R_2C_2s)}{\frac{1 + sR_1C_1}{sC_1} + \frac{R_2}{1 + sR_2C_2}}$$

$$\beta = \frac{jwR_3C_1}{1 + jw\left(R_1C_1 + R_2C_2 + R_2C_1\right) - w^2R_1C_1R_2C_2}$$

In order β to be a real quality

$$1 - \omega^2 R_1 R_2 C_1 C_2 = 0$$

The frequency of oscillation :

$$f_o = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}} \qquad \beta = \frac{R_2C_1}{R_1C_1 + R_2C_2 + R_2C_1}$$

For $R_1 = R_2 = R$ and $C_1 = C_2 = C$,

$$f_o = \frac{1}{2\pi RC}$$

$$\beta = \frac{1}{3}$$

$|A\beta| \geq 1$ for sustained oscillations,

$|A| \geq 3$

$$A = 1 + \frac{R_f}{R_f}$$

$$3 = 1 + \frac{R_f}{R_f} \qquad R_f = 2\,R_s$$

•If the gain |A| > 3, sometimes oscillations Keep growing and it may clip the output Sine wave. This problem is eliminated by a practical Wien bridge oscillator with adaptive negative feedback as shown in Fig. 3.

• In this circuit, resistor R, is initially adjusted to give a gain so that oscillations start.

•The output signal grows in amplitude until the voltage across R3 approaches the cut-in voltage of the diode.

•As the diode begin to turn-on (one for the positive half cycle and the other for the negative half cycle), the effective feed back resistance Rf decreses because the diode is in parallel with the resistor R3.

• This will reduce the gain of the amplifier which in turn lowers the output amplitude. Hence the sustained oscillations can be obtained.

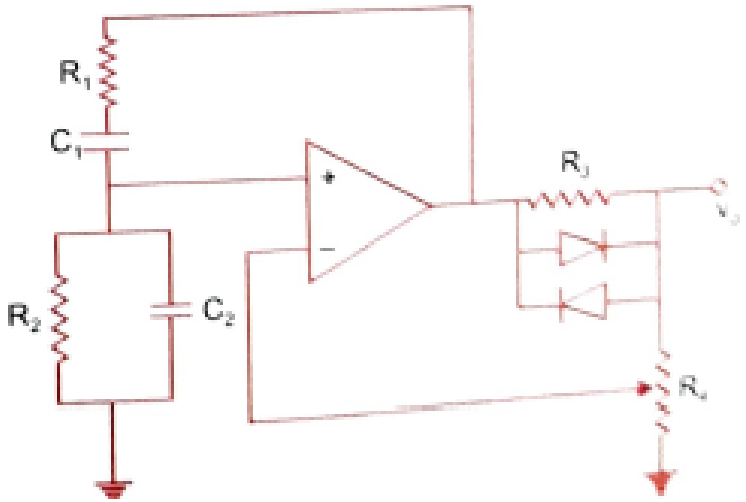


Fig 3 Practical Wien bridge oscillator with adaptive negative feedback

•Further, if the output signal falls, the diodes would begin to turn-off thereby increasing R which in turn increases gain.

•The two op-amp RC oscillator circuits studied are suitable tor the frequency 10 Hz to 100 kHz (maximum 1 MHz).

• The size of R and C components becomes very large for generating low frequencies.

•Thus, the low frequency limit is dictated by the size of passive components required.

•The upper frequency limit is governed by the frequency response and slew rate limit of the op-amp used.

•For generating high frequencies in the RF range the oscillator circuits are usually designed using BJT and LC tuned circuits or crystal oscillators.

SQUARE WAVE GENERATOR

- A simple op-amp square wave generator is also called a free oscillator.

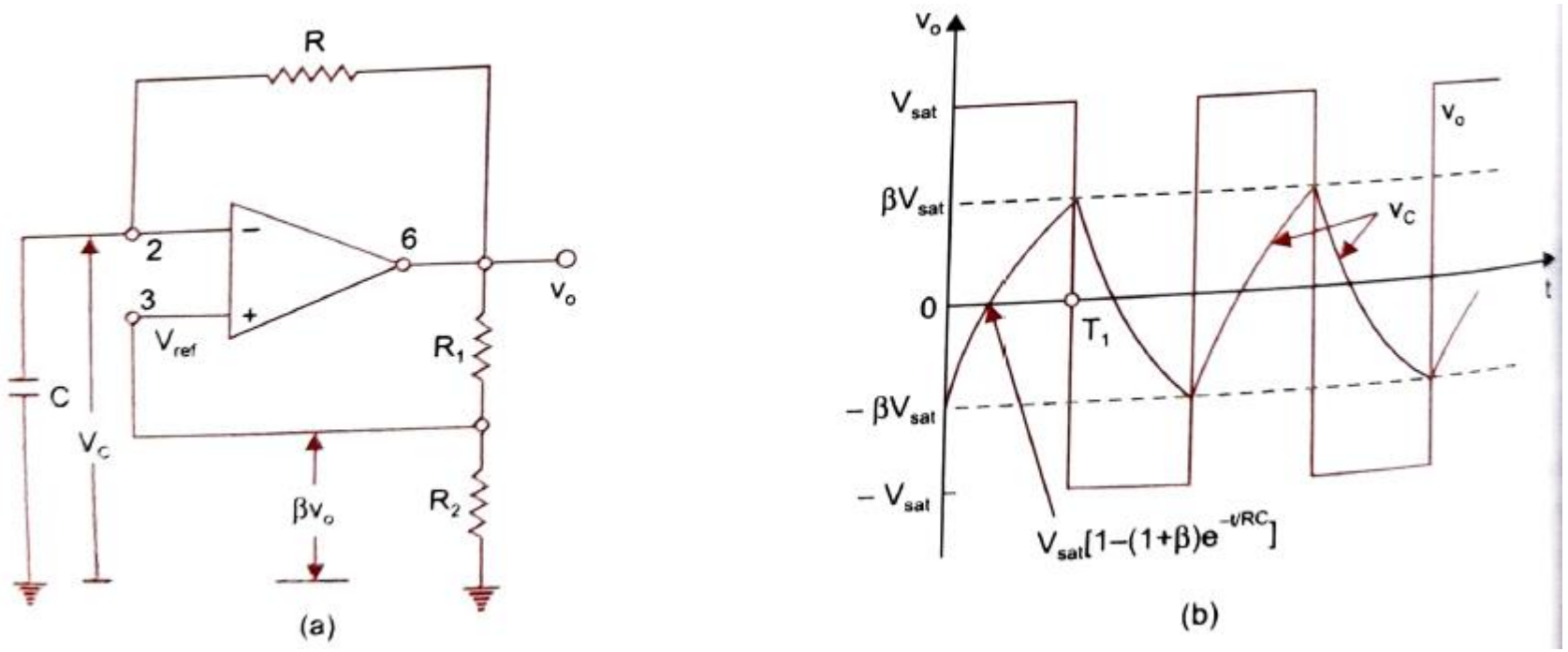


Fig. 1 (a) Simple op-amp square *wave generator (b) Waveforms*

SQUARE WAVE GENERATOR

- The principle of generation of square wave output is to force an op-amp to operate in the saturation region.
- In Fig. 1 (a) fraction $\beta = R2/(R1 + R2)$ *of the output is fed back* to the (+) input terminal.
- Thus the reference voltage *Vref is* βVo *and may take values as* $+\beta$ Vsat or $-\beta$ Vsat .
- The output is also fed back to the (-) input terminal after integrating by a low-pass RC combination.
- Whenever input at the (-) input terminal just exceeds Vref switching takes place resulting in a square wave output.
- In astable multivibrator, both the states are quasi stable.

SQUARE WAVE GENERATOR

- Consider an instant of time when the output is +Vsat. The capacitor now starts charging towards +Vat through resistance R, as shown in Fig. 1 (b).
- The voltage at the (+) input terminal is held at + βVsat by R1 and R2 combination.
- This condition continues as the charge on C rises, until it has just exceeded + βVsat, the reference voltage.
- When the voltage at the (-) input terminal becomes just greater than this reference voltage, the output is driven to - Vsat .
- At this instant, the voltage on the capacitor is + β Vsat . It begins to discharge through R that is, charges toward - Vsat .

SQUARE WAVE GENERATOR

- At this instant, the voltage on the capacitor is +βVsat· It begins to discharge through R that is, charges toward - Vsat·
- When the output voltage switches to – Vsat, the capacitor *charges more and more negatively until its voltage just exceeds* - β Vsat · *The output switches back to* + Vsat.

The cycle repeats itself as shown in Fig. 1 (b).

- The frequency is determined by the time it takes the capacitor to charge from - βVsat *to* +βVsat
- *The voltage across the capacitor as a function of time is given by,*

$$v_c(t) = V_f + (V_i - V_f)e^{-t/RC}$$

SQUARE WAVE GENERATOR

$$V_f = +V_{sat}$$
$$V_i = -\beta V_{sat}$$

$$v_c(t) = V_{sat} + (-\beta V_{sat} - V_{sat})\, e^{-t/RC}$$
$$v_c(t) = V_{sat} - V_{sat}\,(1 + \beta)\, e^{-t/RC}$$

At $t = T1$, voltage across the capacitor reaches βsat and switching takes place.

$$v_c(T_1) = \beta V_{sat} = V_{sat} - V_{sat}\,(1+\beta) e^{-T_1/RC}$$

After algebraic manipulation, we get,

$$T_1 = RC \ln \frac{1+\beta}{1-\beta}$$

This gives only one half of the period.

Total time period

$$T = 2T_1 = 2RC \ln \frac{1+\beta}{1-\beta}$$

and the output wave form is symmetrical.

If $R_1 = R_2$, then $\beta = 0.5$, and $T = 2RC \ln 3$. And for $R_1 = 1.16R_2$, $T = 2\ RC$

or

$$f_0 = \frac{1}{2RC}$$

The output swings from $+V_{sat}$ to $-V_{sat}$, so,

v_o peak-to-peak $= 2\ V_{sat}$

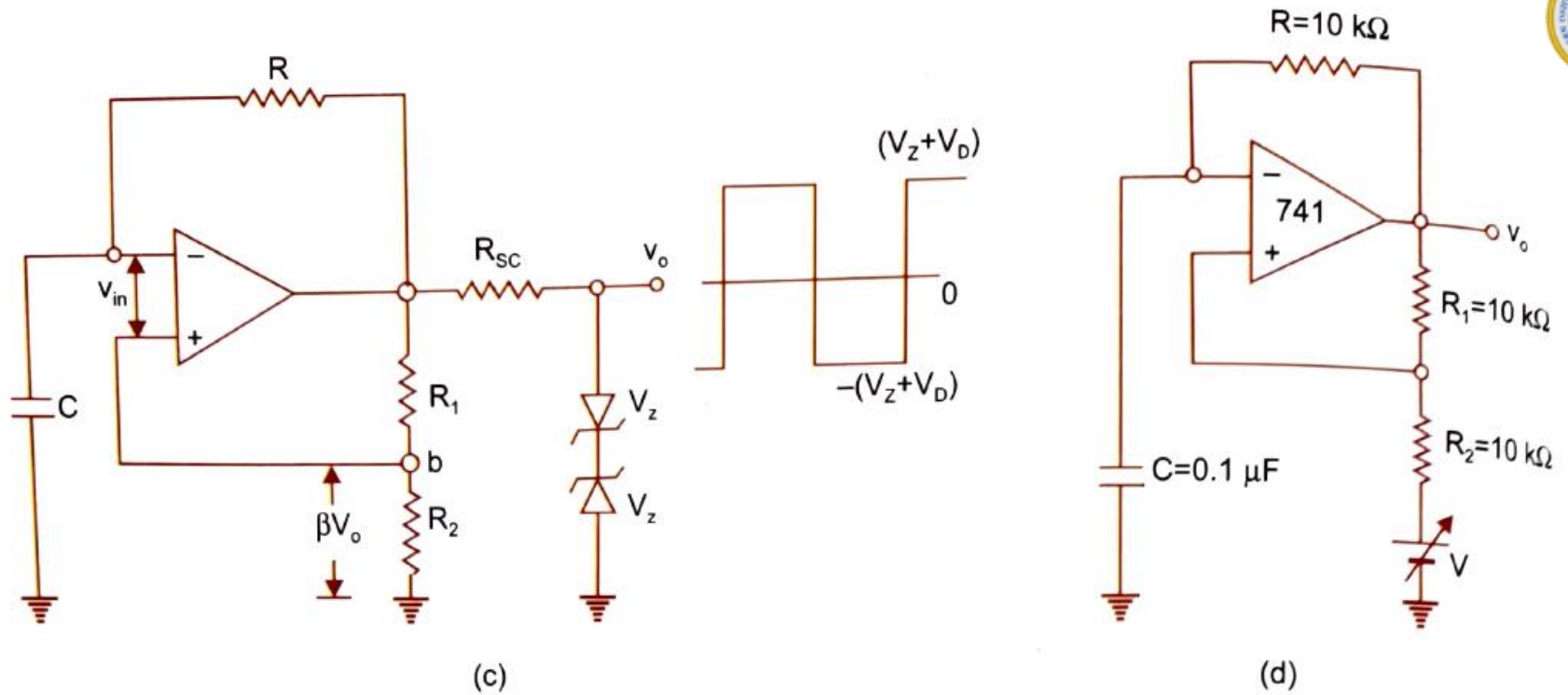


Fig. 1 (c) Use of back to back zener diodes. (d) Asymmetric square wave generator

- The peak to peak output amplitude can be varied by varying the power supply voltage.
- However, a better technique is to use back to back zener liodes as shown in Fig. 1(c).
- The output voltage is regulated to (Vz + VD) by the zener diodes.
- Vo peak-to-peak = 2 (Vz + VD)
- Resistor Rs limits the currents drawn from the op-amp to $I_{sc} = \frac{V_{sat} - V_Z}{R_{sc}}$

- This circuit works reasonably well at audio frequencies. At higher frequencies, however, slew-rate of the op-amp limits the slope of the output square wave.
- If an asymmetric square wave is desired, then zener diodes with different break down voltages V_{z1} and V_{z2} may be used.
- Then the output is either Vo1 or Vo2, where $V_{o1} = V_{z1} + V_D$ and $V_{o2} = V_{z2} + V_D$.
- It can be easily shown that the V_{z1} positive section is given by,

$$T_1 = RC \ln \frac{1 + \beta V_{o2}/V_{o1}}{1 - \beta} \qquad \text{....(1)}$$

- The duration of negative section T2 will be the same as given by Eq. (1) with V_{o1} and V_{o2} interchanged.
- An alternative method to get asymmetric square wave output is to add a dc voltage source V in series R2 as shown in Fig. 1 (d).
- Now the capacitor C swings between the voltage levels (β Vat + V) and (- β Vsat + V). If the voltage source V is made variable, voltage to frequency conversion can be achieved through the variation will not be linear.

TRIANGULAR WAVE GENERATOR

- A triangular wave can be simply obtained by integrating a square wave as shown in Fig.1(a). It is obvious that the frequency of the square wave and triangular wave is the same as shown in Fig.1 (b).
- Although the amplitude of the square wave is constant at $\pm Vsat$, the amplitude of the triangular wave will decrease as the frequency increases.
- This is because the reactance of the capacitor C_2in the feedback circuit decreases at high frequencies.
- A resistance *R4 is connected across* C_2 *to avoid the saturation problem at low frequencies as* in the case of practical integrator.

TRIANGULAR WAVE GENERATOR

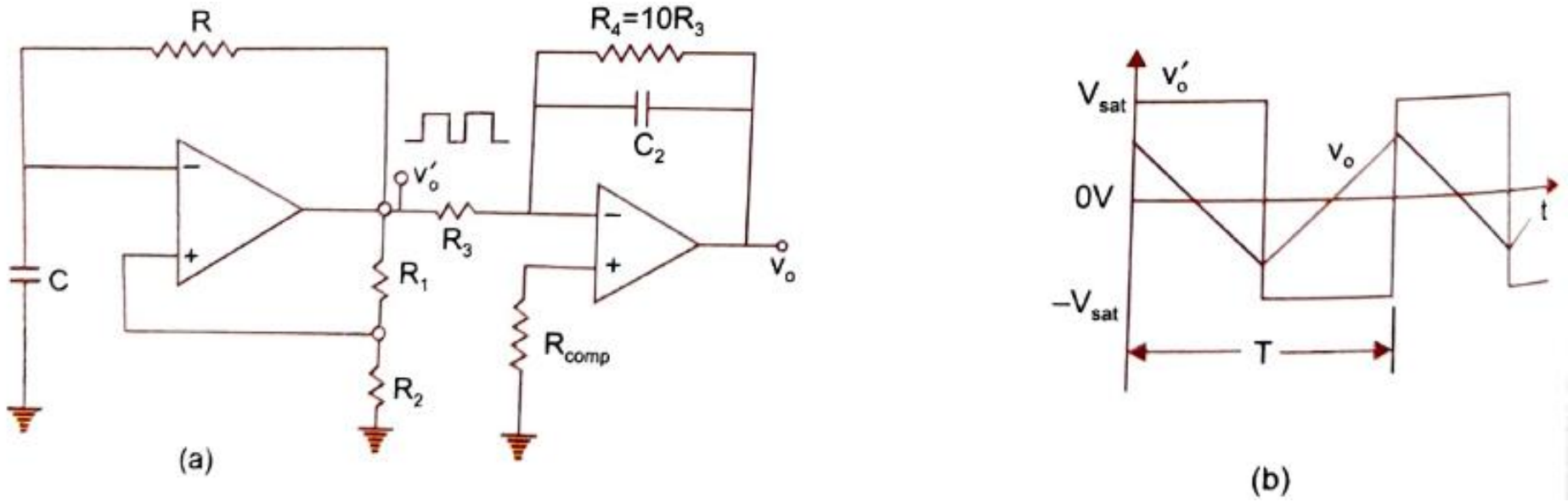


Fig 1 a) Triangular waveform generator b) Output waveform

TRIANGULAR WAVE GENERATOR

- Another triangular wave generator using lesser number of components is shown in Fig 2.
- It consists of a two level comparator followed by an integrator.
- The output of the comparator A1 is a square wave of amplitude ±Vsat and is applied to the (-) input terminal of the integrator A2 producing a triangular wave.
- This triangular wave is fed back as input to the comparator A1 through a voltage divider R2R3.

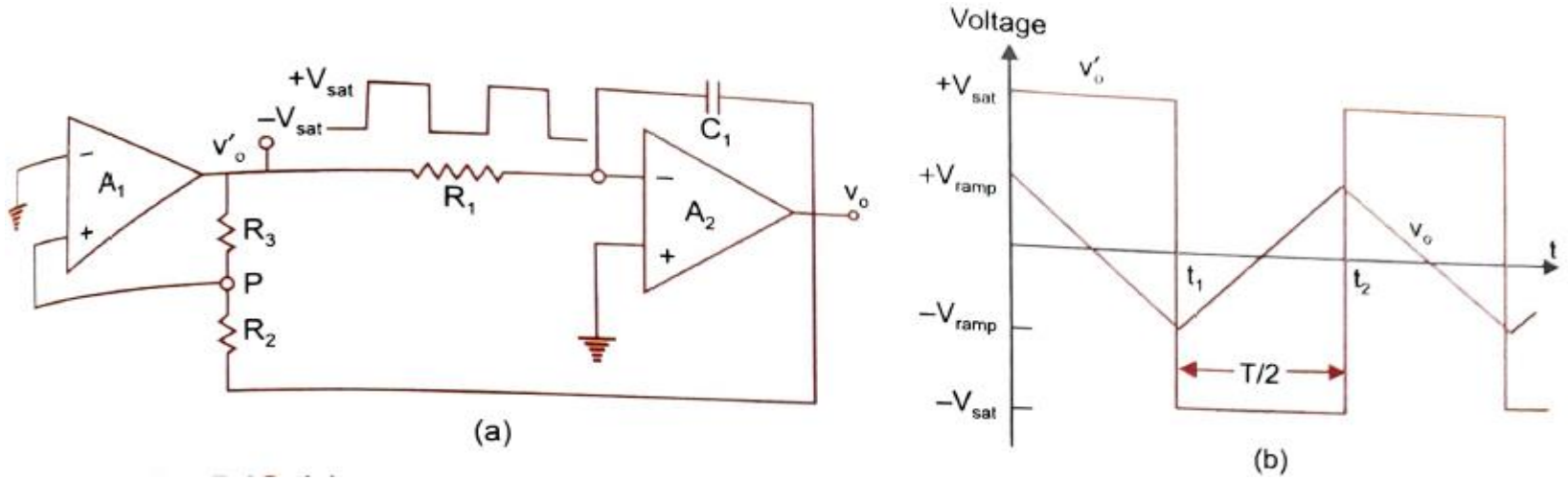


Fig 2 a) Triangular waveform generator using lesser components b) Waveforms

TRIANGULAR WAVE GENERATOR

- Initially, let us consider that the output of comparator *A1 is at +Vsat. The output of the integrator A2 will be a negative* going ramp as shown in Fig. 2 (b).
- Thus one end of the voltage divider *R2R3 is at a voltage + Vsat and the other at the negative going ramp of A2.*
- At a time *t = t1, when the negative going ramp attains a value of*

  -Vramp the effective voltage at the point P becomes slightly less than 0V. This switches the output of A1 from positive saturation to negative saturation level -Vsat·
- During the time when the output of A1 is at -Vsat, the output of A2 increases in the positive direction. And at the instant *t = t2, the volt*age at point *P becomes just above 0V, thereby switching the output of A1 from -Vsat to* +Vsat · The cycle repeats and generates a triangular waveform.
- It can be seen that the frequency of the square wave and triangular wave will be the same. The amplitude of the triangular wave depends upon the *RC value of the integrator A2 and the output* voltage level of A1 .
- The output voltage of A1 can be set to desired level by using appropriate zener diodes.

The frequency of the triangular waveform can be calculated as follows: .
The effective voltage at point *p during the time when output of A1 is at +Vsat level is given by*

$$-V_{ramp} + \frac{R_2}{R_2 + R_3} I_2 \left(-V_{sat} - (-V_{ramp})\right) \quad (1)$$

At $t = t1$ *the voltage at point p becomes equal to zero. Therefore , from Eq (1).*

$$-V_{ramp} = -\frac{R_2}{R_2} \left(+V_{sat}\right)$$

Similarly at t = $-t_2$ *when the output of* A_1 *switches from* $-V_{sat}$ to V_{sat}

$$V_{ramp} = \frac{R_2}{R_2} \left(+V_{sat}\right)$$

Therefore peak to peak amplitude of Triangular wave is

$$V_0(pp) = V_{ramp} - \left(-V_{ramp}\right) = 2\frac{R_2}{R_3} V_{sat}$$

The output switches from $-V_{ramp}$ *to* V_{ramp} in half the time period

$$v_o = -\frac{1}{RC}\int v_i\,dt$$

$$v_o(\text{pp}) = -\frac{1}{R_1C_1}\int_0^{T/2}(-V_{sat})dt = \frac{V_{sat}}{R_1C_1}\left(\frac{T}{2}\right)$$

or,
$$T = 2\,R_1C_1\frac{v_o\,(\text{pp})}{V_{sat}}$$

Putting the value of V0(pp) from equation (2), we get

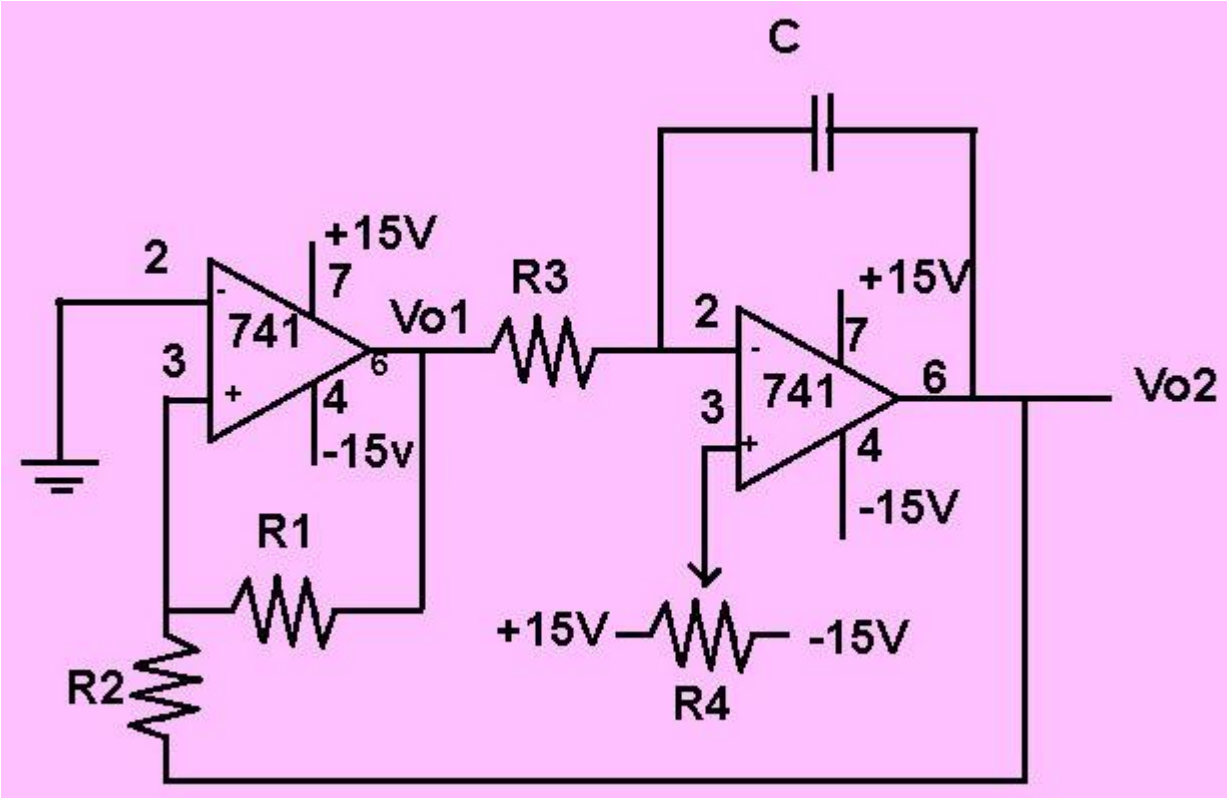
$$T = \frac{4R_1C_1R_2}{R_3}$$

Hence the frequency of oscillation f_o is,

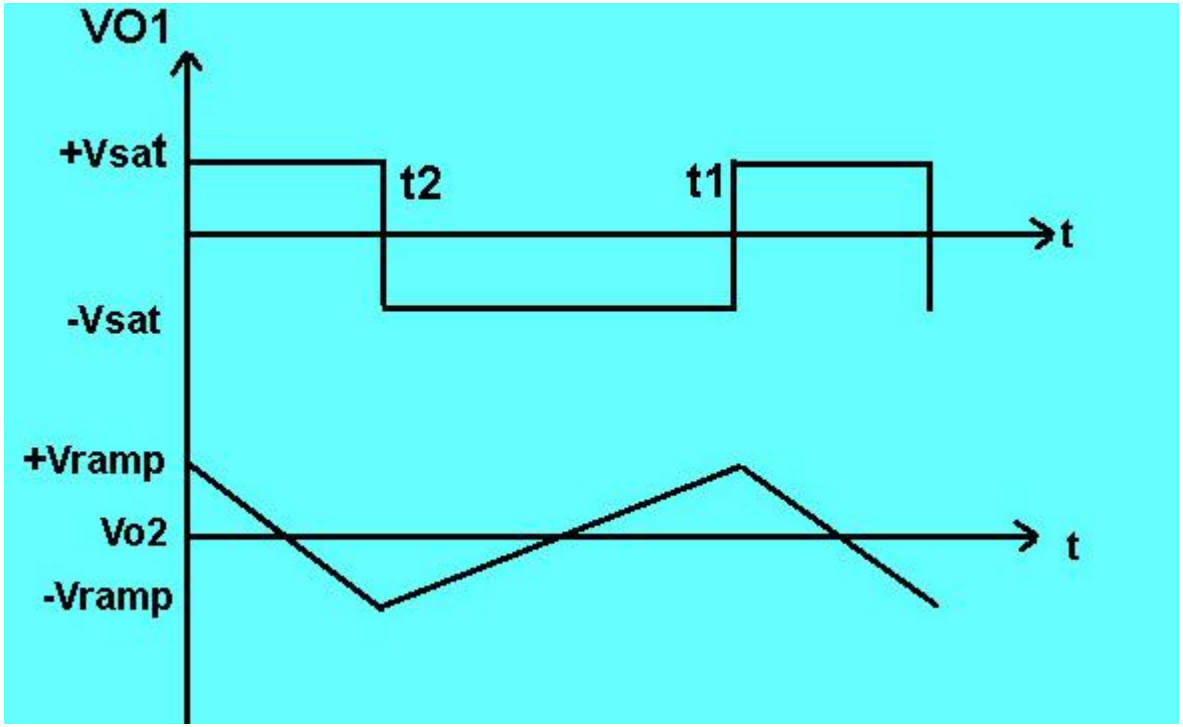
$$f_o = \frac{1}{T} = \frac{R_3}{4R_1C_1R_2}$$

Sawtooth waveform generator

- A sawtooth waveform is used in pulse width modulation circuits and time-base generators. A potentiometer is used when the wiper moves toward negative voltage(-V); then the rise time becomes more than the fall time. When the wiper moves towards positive voltage(+V), then the rise time becomes less than the fall time.



When the comparator output goes negative saturation, a negative voltage is added to the inverting terminal, thereby the wiper moves to a negative supply. This causes a decrease in the potential difference across R1 and hence current through the capacitor and resistor decreases.



Then the slope decreases and rise time also decrease. When the comparator output is under positive saturation, the potential difference across the R1 increases and current through the capacitor resistor also increases. This is due to the presence of a negative voltage at the inverting terminal. Then the slope increases and fall time decreases. And the output is obtained as a saw tooth waveform.

Introduction to the 555 Timer

- The 555 Timer is one of the most popular and versatile integrated circuits ever produced!
- It was first introduced by Hans R. Camenzind in 1970 and brought to market in 1971 by Signetics (later acquired by Philips).
- It is 30 years old and still being used!
- It is a combination of digital and analog circuits.

555 Timer

- It has been claimed that the 555 gets its name from the three 5 kΩ resistors used in typical early implementations.
- Typically it has 8 pins, but it has various versions.
- Ultra-low power versions of the 555 are also available.
- It is known as the "time machine" as it performs a wide variety of timing tasks.
- Variant IC's available include the 556 (a 14-pin DIP combining two 555s on one chip), and the 558 (a 16-pin DIP combining four slightly modified 555s .

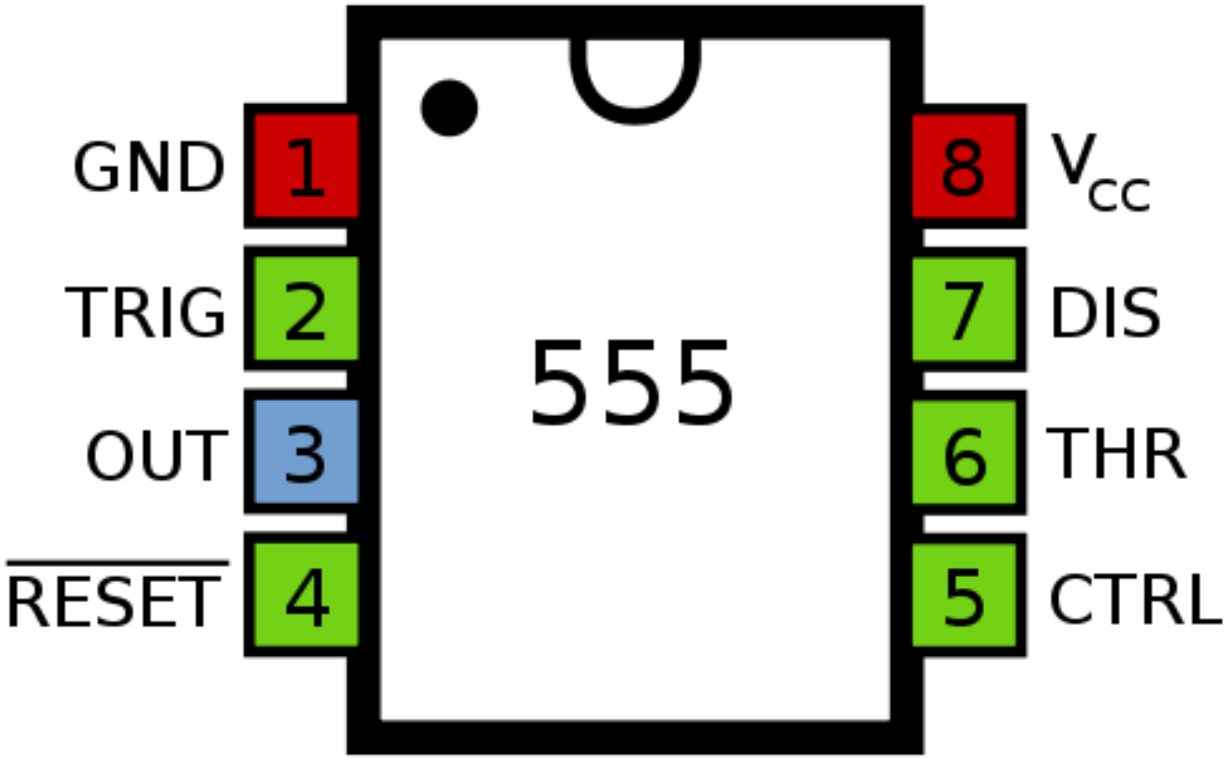
Application's for the 555 Timer include:

- Bounce-free switches and Cascaded timers.
- Frequency dividers.
- Voltage-controlled oscillators.
- Pulse generators and LED flashers.
- Sawtooth (linear ramp) generator.
- Pulse width modulator.
- Pulse position modulator.
- Frequency divider.

555 Timer

- Missing pulse detector.
- Metronome.
- Bicycle light.
- Sweeping frequency siren.
- Voltage inverter.
- Voltage doubler.
- Running/rotating light generator.
- Infrared remote control.
- Frequency to voltage converter.
- Power alarm.
- Dark detector.

555 Timer IC Pin Configuration:



Pin Details:

1.GND(Ground)

2.TRIG(Trigger voltage)

3.OUT(Output)

4.RESET(Reset)

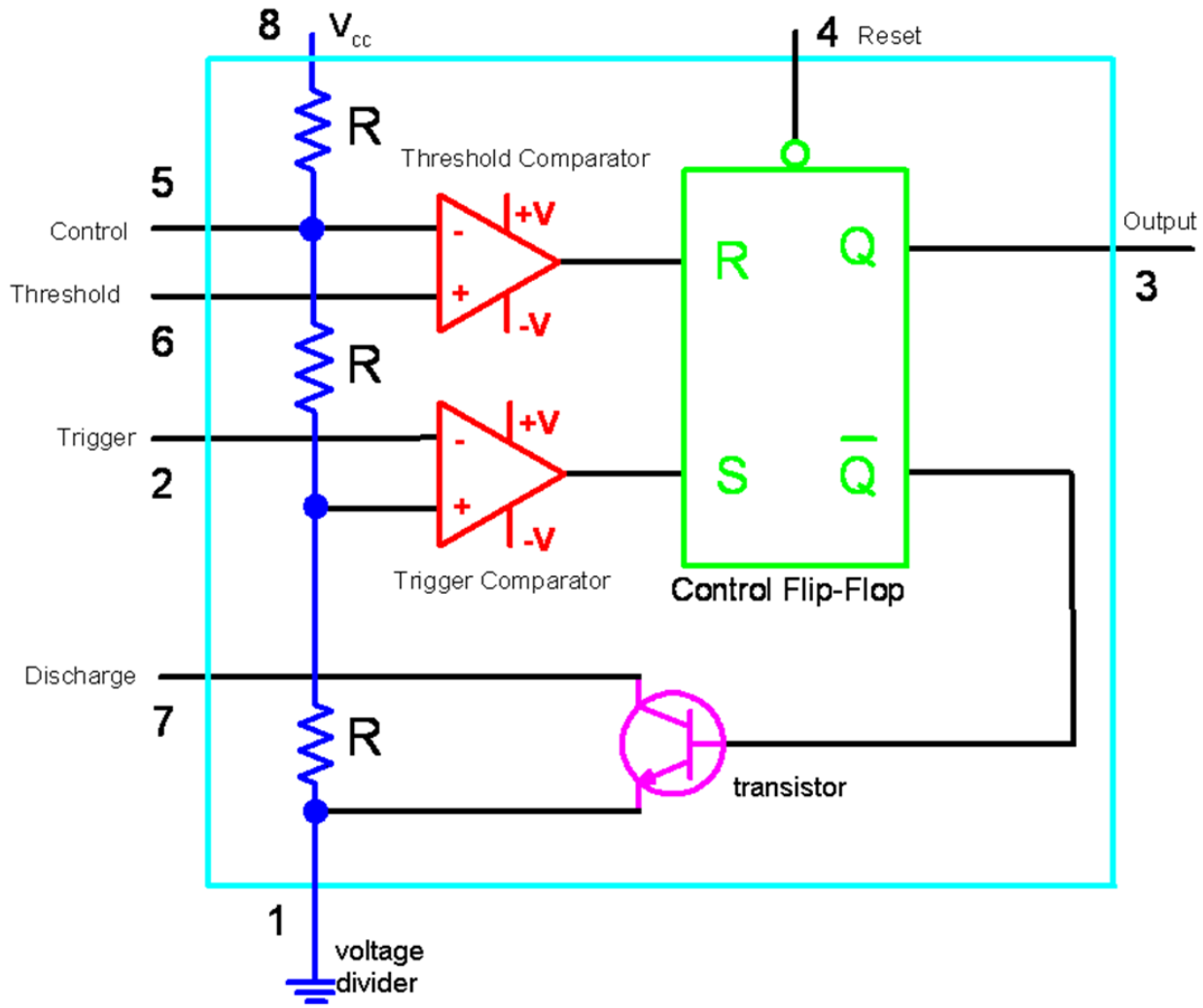
5.CTRL(Control Voltage)

6.THR(Threshold)

7.DIS(Discharge)

8.Vcc(Supply Voltage)

Inside 555 Timer IC:



Description of internal circuit:

❖The voltage divider (blue) has three equal 5K resistors. It divides the input voltage (Vcc) into three equal parts.

❖The two comparators (red) are op-amps that compare the voltages at their inputs and saturate depending upon which is greater.

- The Threshold Comparator (upper)saturates when the voltage at the Threshold pin (pin 6) is greater than (2/3)Vcc.
- The Trigger Comparator(lower) saturates when the voltage at the Trigger pin (pin 2) is less than (1/3)Vcc

Description of internal circuit:

❖The flip-flop (green) is a bi-stable device. It generates two values, a “high” value equal to Vcc and a “low” value equal to 0V.

- When the Threshold comparator saturates, the flip flop is Reset (R) and it outputs a low signal at pin 3.
- When the Trigger comparator saturates, the flip flop is Set (S) and it outputs a high signal at pin 3.

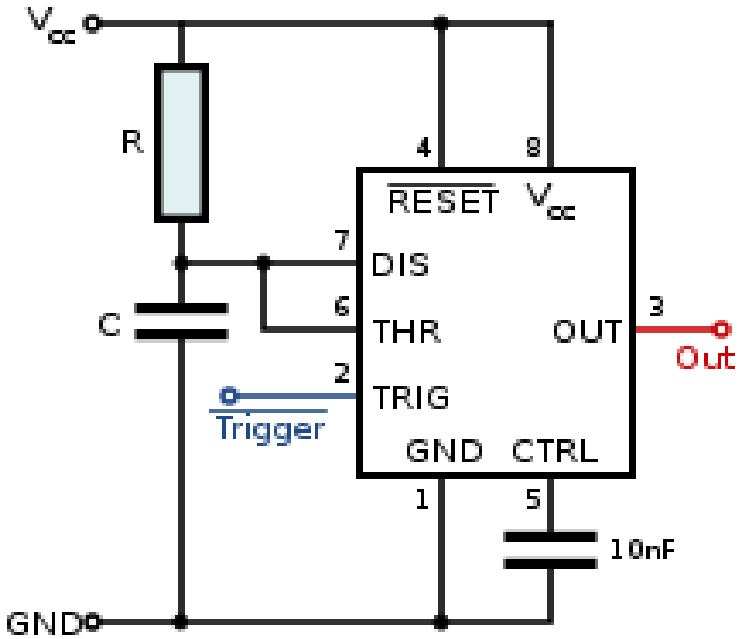
❖The transistor (purple) is being used as a switch, it connects pin 7 (discharge) to ground when it is closed.

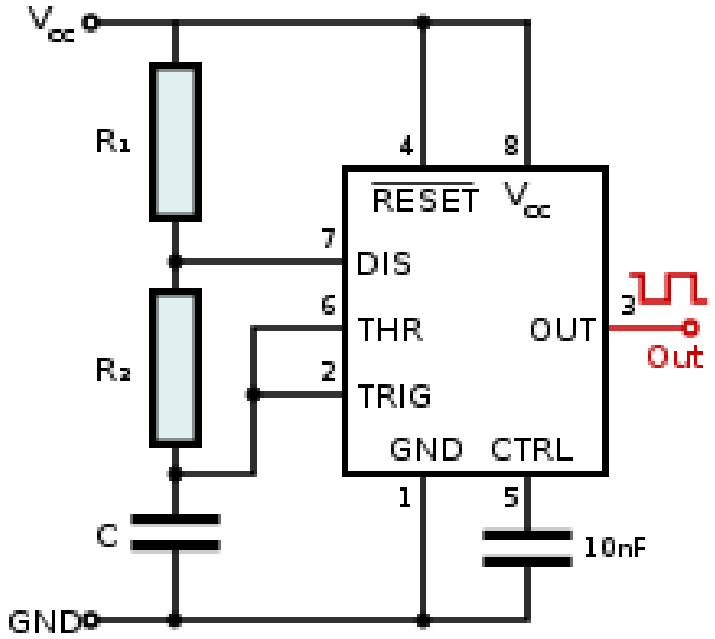
- When Q is low, Q-bar is high. This closes the transistor switch and attaches pin 7 to ground.
- When Q is high, Q-bar is low. This open the switch and pin 7 is no longer grounded.

Types of 555-Timer circuits:

❖There are three types of 555-Timer circuits:-

- Monostable Multivibrator.
- Astable Multivibrator.
- Bistable Multivibrator.

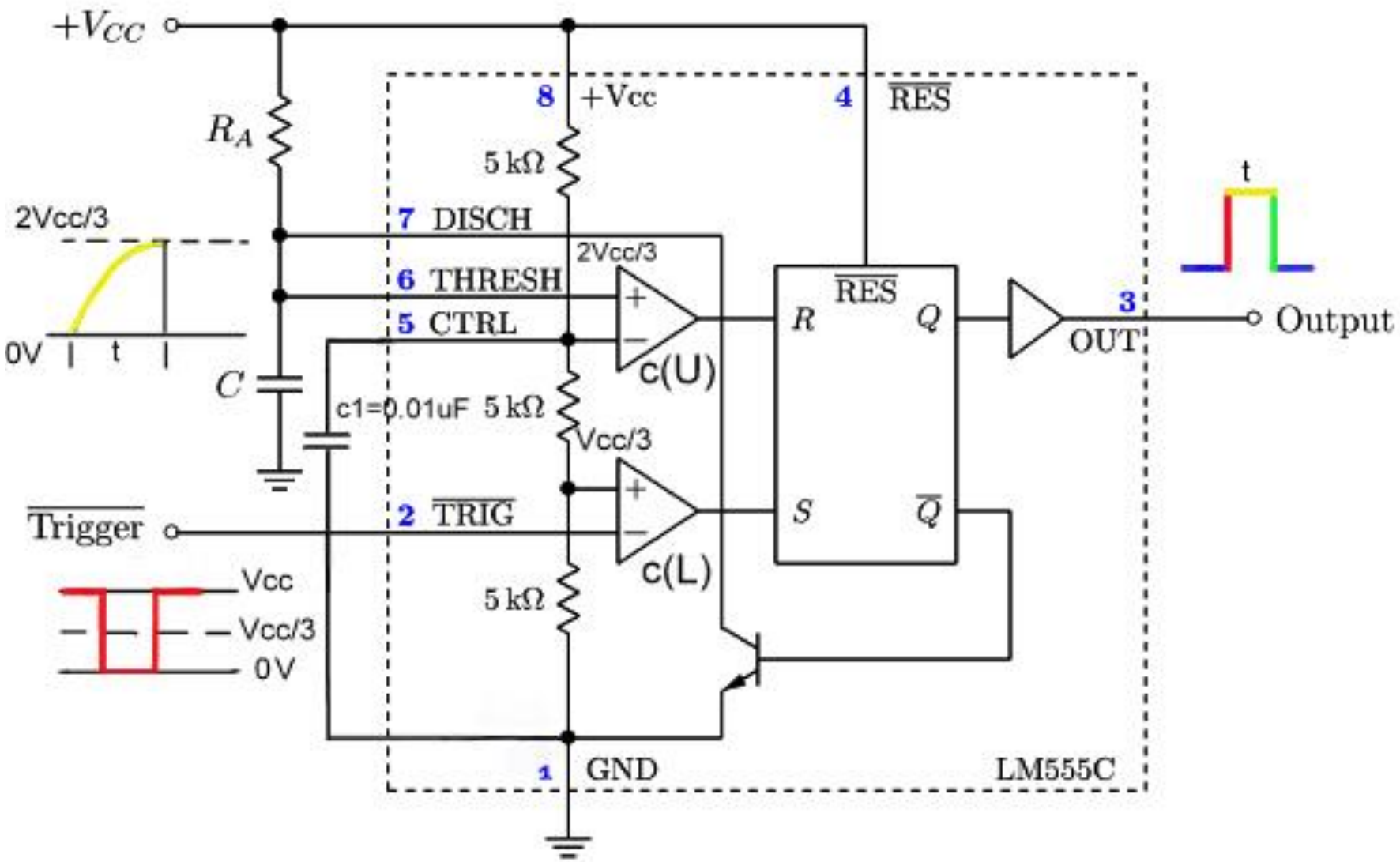




Monostable Multivibrator (or one-shot) puts out one pulse each time the switch is connected

Astable Multivibrator puts out a continuous sequence of pulses

Monostable Multivibrator (One shot):



Circuit

1. In the diagram you can see that we have connected a resistor “Ra” between the Supply Voltage(Pin 8) and Threshold Voltage (Pin 6).Also Threshold And Discharge (Pin 7) is shorted.
2. A capacitor of capacitance “C” is connected between Threshold (Pin 6) and Ground . the function of this capacitor is to suppress noise and deliver energy during the transition time of the output.
3. Between Control Voltage (Pin 5) and Ground (Pin 1) a Capacitor of capacitance 0.01uF is connected.

Operation:

1) We know that if we leave a capacitor alone then the capacitor will discharge gradually, so initially we can consider the voltage of capacitor “C” as 0Volt.
2) Now to start the sequence, we apply a negative trigger voltage shown in red color in left side.
3) When the trigger voltage goes below Vcc/3 voltage level, at that time in the lower comparator c(L) +ve pin voltage becomes > -ve pin voltage, as +ve pin is fixed with Vcc/3 in 555 resistor network and –ve is connected with trigger voltage. So the output of the comparator c(L) become high.

Operation:

4) Now you can see that the output of the comparator c(L) is connected with the “S” terminal of SR Flip Flop .So we know that if we give S=1 and R=0 in SR Flip Flop the out put becomes Q=1 and Q-bar=0,which starts the output signal (connected with Q) portion shown in red and it becomes high as shown in the out put graph at right side of the picture.

5) At the same time the capacitor “C” starts to become charged through resistor “Ra” from. Vcc(shown in the upper left side of the picture), and continues upto voltage level 2Vcc/3.

6) Suppose the capacitor takes time “t” to reach the voltage level 2Vcc/3, so the output remains high during this time period “t” shown in “yellow” at output .And during this period any trigger voltage applied in the trigger pin will have no effect on the output.

7) Now the capacitor Reaches to voltage level 2Vcc/3 and exceeds the voltage, at that time in the comparator c(U) the +ve pin voltage becomes > the –ve voltage level, as +ve pin is connected with capacitor and –ve pin is fixed with 2Vcc/3 voltage Level in 555 resistor network.

Operation:

7) Here you can see that the R pin in SR flip flop is connected with the output of the comparator c(U).So the input of SR flip flop is S=0 and R=1 and output is Q=0 and Q-bar=1.

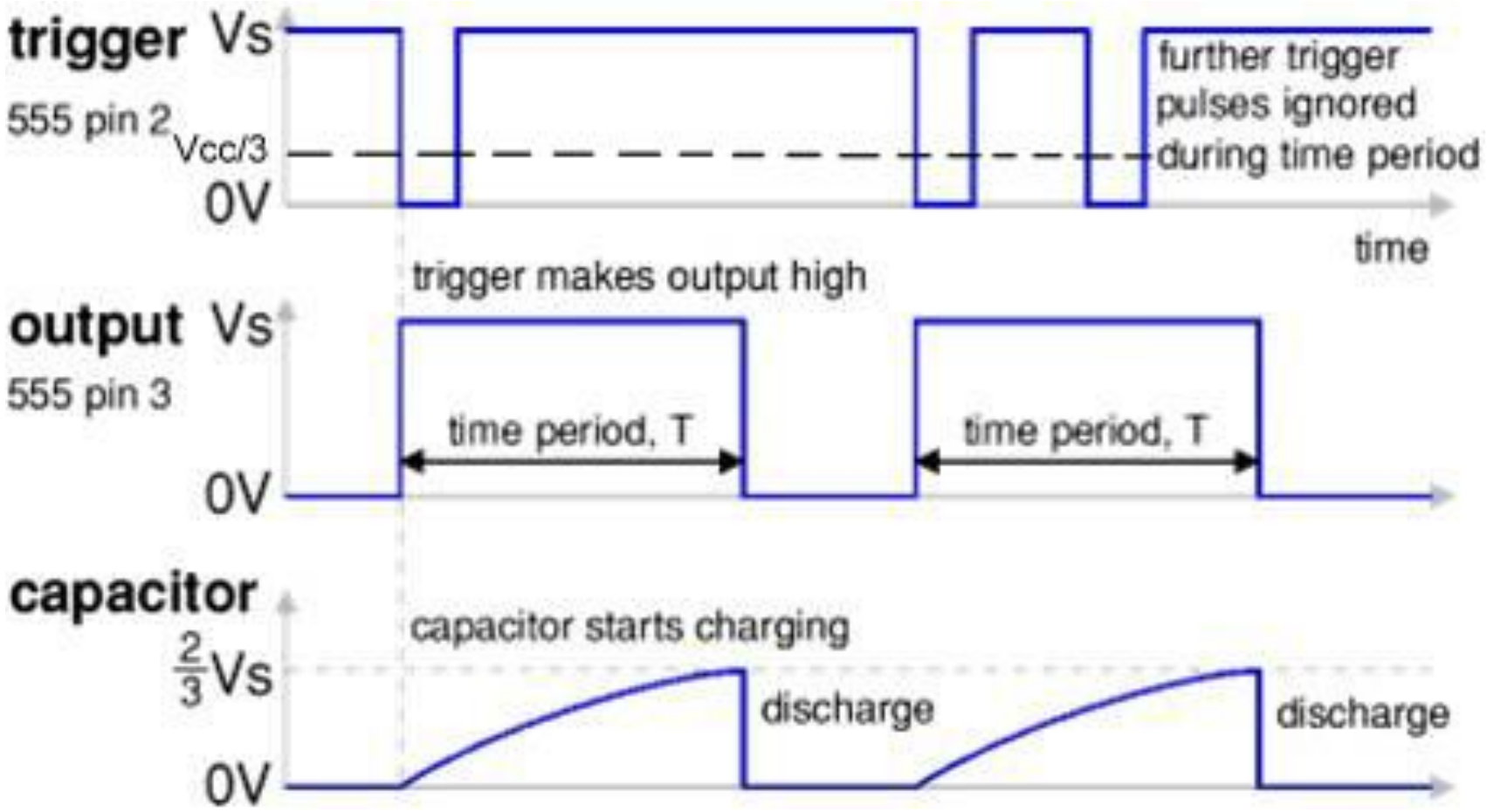
8) As shown in picture Q ia connected with the output so, output becomes low shown in green color in output graph.

9) Again we can see that Q-bar is connected with the gate of the discharge BJT, whose collector is connected with the capacitor “C” and emitter is grounded. So if the Gate voltage is “1” then the gate opens and the capacitor discharges through the capacitor and becomes oV as it was initially, shown in capacitor charactaristics graph.

10) Now the whole circuit is in the stage as it was initially. Now if we give another trigger pulse at trigger pin then the whole sequence starts again.

By this way the 555 Timer works as monostable multivibrator in which we get a regulated time output pulse for each trigger voltage.

Graphical Representation:



Mathematical Calculation:

Equation for charging capacitor is:

$$e = E\{1-e^{(-t/Ra*C)}\}$$

Here,
e=capacitor voltage.
E=Supply Voltage.
e=Base of Natural Logarithm.

Now,

The voltage across the external capacitor changes exponentially from 0 to (2/3)Vcc, is given by

$$Vc=Vcc\ \{1-e^{(-t/Ra*C)}\}$$

At time t=T, Vc=(2/3)Vcc;

Mathematical Calculation:

Therefore,

$$(2/3)Vcc=Vcc\ \{1-e^{(-T/Ra*C)}\}$$

$$\text{or, } (2/3)= \{1-e^{(-t/Ra*C)}\};$$

$$\text{or, } T=1.1Ra*C.$$

Therefore, when the output is high, the time interval becomes, thigh = T.

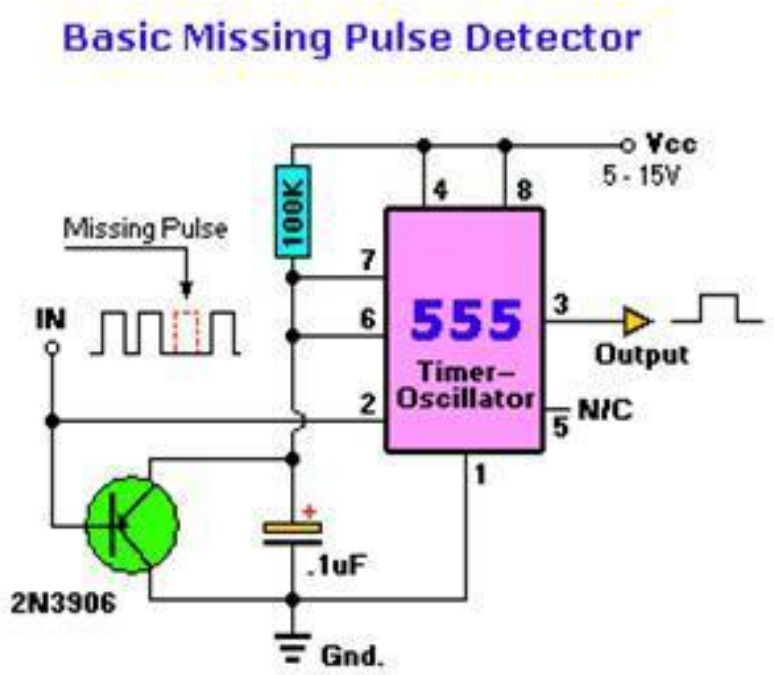
Practical Circuits:

Some of the frequently used practical circuits are.

- Missing Pulse Detector.
- Pulse Width Modulator.
- Linear Ramp Generator.
- Frequency Divider.

Practical Circuits:

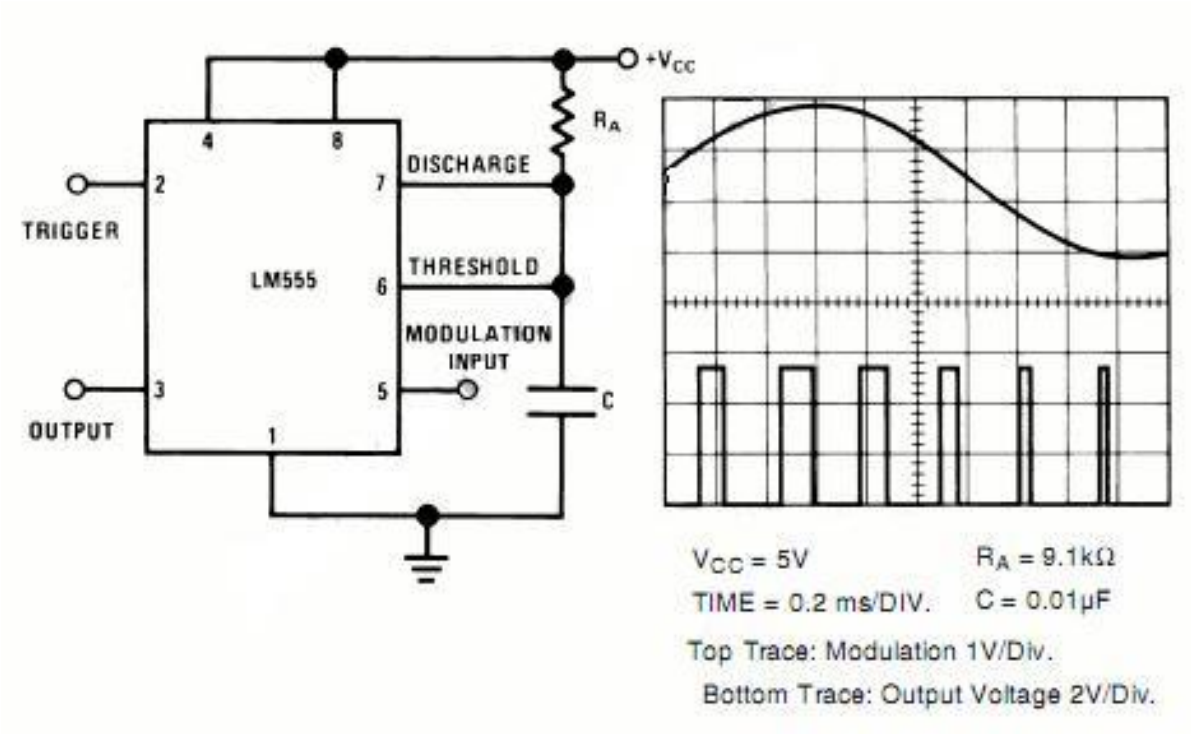
- **Missing Pulse Detector (Basic):** This transistor can be replaced with a ECG or NTE159. This is just a basic model but works. Experiment with the values of Resistor and Capacitor. A good example would be the **'Crashed Aircraft Locator'** beacon used in radio control. If there is no signal it sees it as a missing pulse and sounds buzzer.



Practical Circuits:

- **Pulse width modulator :**Pulse width modulator produce a PWM signal, a pulse with a constant frequency but with the duty cycle vary according to a modulating signal.
- Here is the schematic diagram of pulse width modulator circuit using 555 IC as the active component.
- This pulse width modulator circuit need external pulse train input to trigger the the 555 monostable circuit.
- This trigger input sould be a square wave signal with a fixed frequency.
- The output of this pulse width modulator circuit will have same frequency with the trigger input, but with its pulse width proportional to the modulating input signal at pin 5.

Circuit


+VCC
RA
4
8
DISCHARGE
7
2
TRIGGER
LM555
THRESHOLD
6
MODULATION
INPUT
3
5
C
OUTPUT
1
VCC = 5V
RA = 9.1kΩ
TIME = 0.2 ms/DIV.
C = 0.01μF
Top Trace: Modulation 1V/Div.
Bottom Trace: Output Voltage 2V/Div.

Linear Ramp Generator

- Linear ramp can be generated by the circuit shown in Fig.1 The resistor R of the monostable circuit is replaced by a constant current source. The capacitor is charged linearly by the constant current source formed by the transistor Q3. The capacitor voltage Vc can be written as

$$v_c = \frac{1}{C}\int_0^t i\,dt \qquad \text{.....(1)}$$

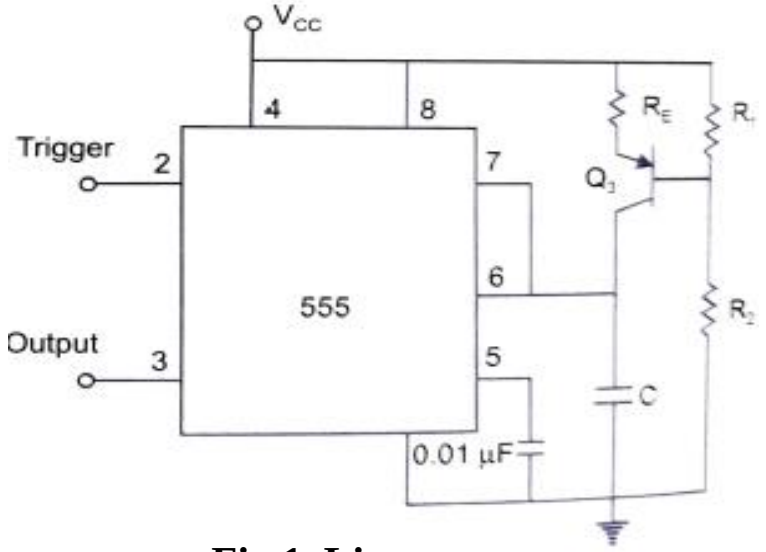


Fig 1. Linear ramp generator

Where ' i' is the current supplied by the constant current source. Further, the KVL equation can be written as

$$\frac{R_1}{R_1+R_2}\,V_{CC} - V_{BE} = (\beta+1)I_B R_E \approx \beta I_B R_E = I_C R_E = iR_E$$

where Ig, lc are the base current and collector current respectively, β is the current amplification factor in CE-mode and is very high.

- Therefore,

$$i = \frac{R_1 V_{CC} - V_{BE}(R_1 + R_2)}{R_E (R_1 + R_2)}$$

Now putting the value of the current i in Eq. (1), we get

$$v_c = \frac{R_1 V_{CC} - V_{BE}(R_1 + R_2)}{C\, R_E (R_1 + R_2)} \times t$$

At time t = T, the capacitor voltage Vc becomes (2/3) Vo: Then we get

$$\frac{2}{3} V_{CC} = \frac{R_1 V_{CC} - V_{BE}(R_1 + R_2)}{R_E (R_1 + R_2) C} \times T$$

which gives the time period of the linear ramp generator as

$$T = \frac{(2/3) V_{CC} R_E (R_1 + R_2) C}{R_1 V_{CC} - V_{BE} (R_1 + R_2)}$$

The capacitor discharges as soon as its voltage reaches (2/3) Voc which is the threshold of the upper comparator in the monostable circuit functional diagram. The capacitor voltage remains zero till another trigger is applied. The various waveforms are show in fig 2.

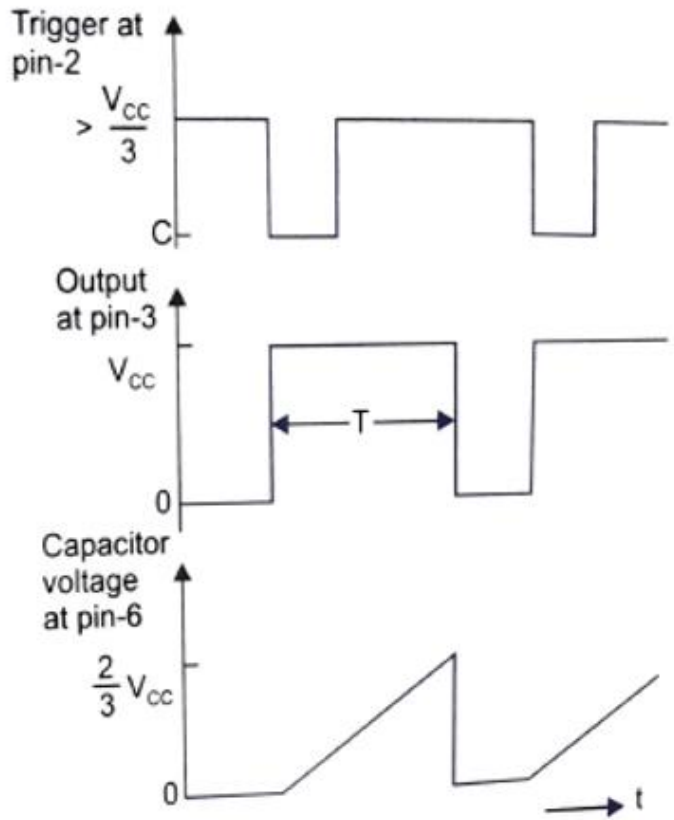


Fig 2. Linear ramp generator output

Frequency Divider

- A continuously triggered monostable circuit when triggered by a square wave generator can be used as a frequency divider, if the timing interval is adjusted to be longer than the period or the triggering square wave input signal.
- The monostable multivibrator will be triggered by the first negative going edge of the square wave input but the output will remain HIGH. (because of greater timing interval) for next negative going edge of the input square wave as shown in Fig. 1.
- The mono-shot will however be triggered on the third negative going input, depending on the choice of the time delay. In this way, the output can be made integral fractions of the frequency of the input trigger wave.

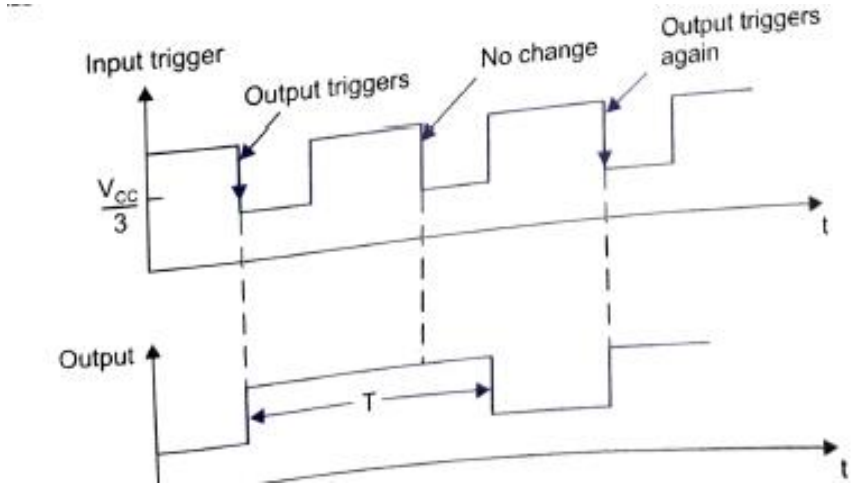
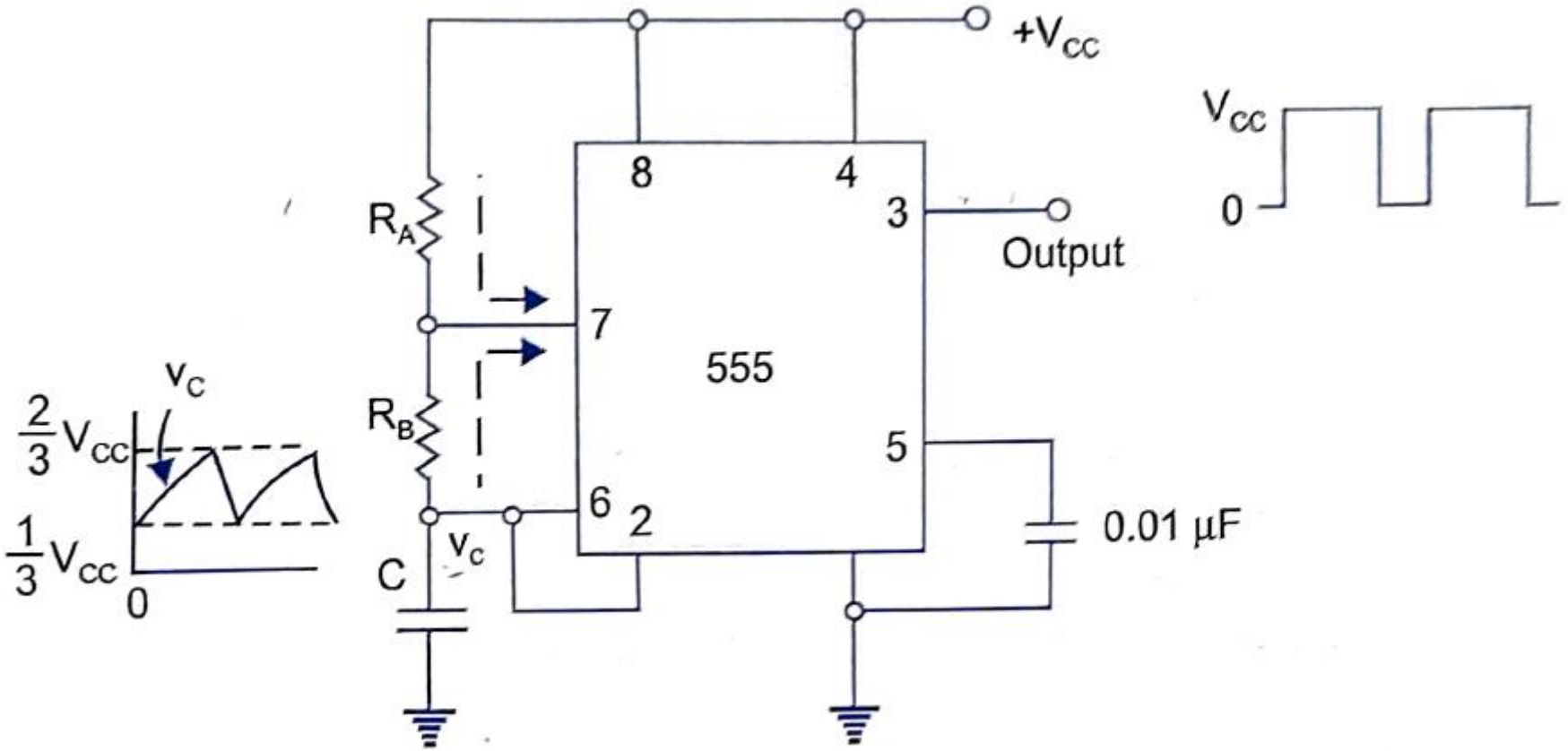
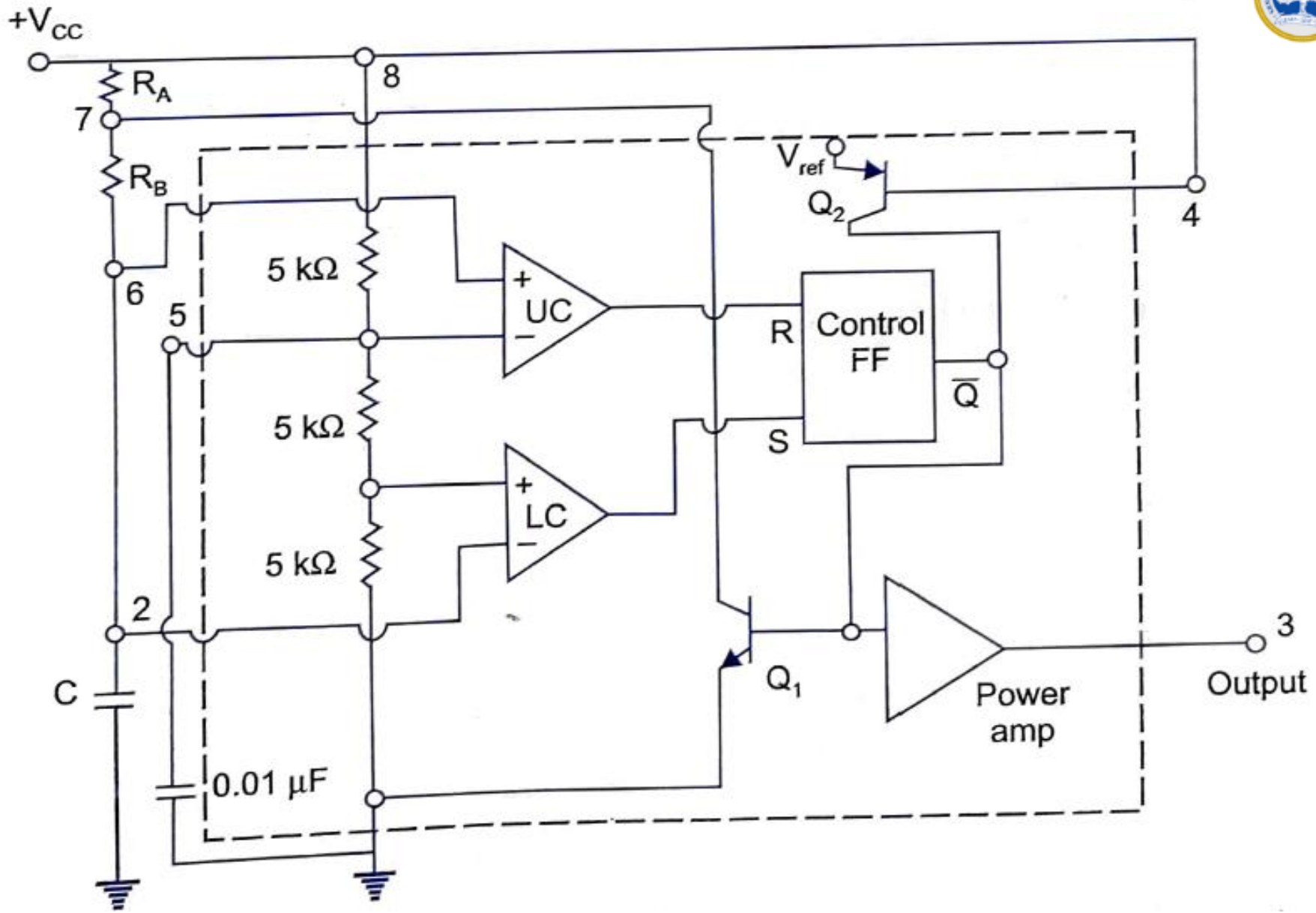


Fig 1. Frequency divider circuit

IC 555 ASTABLE OPERATION



Astable multivibrator using 555 timer

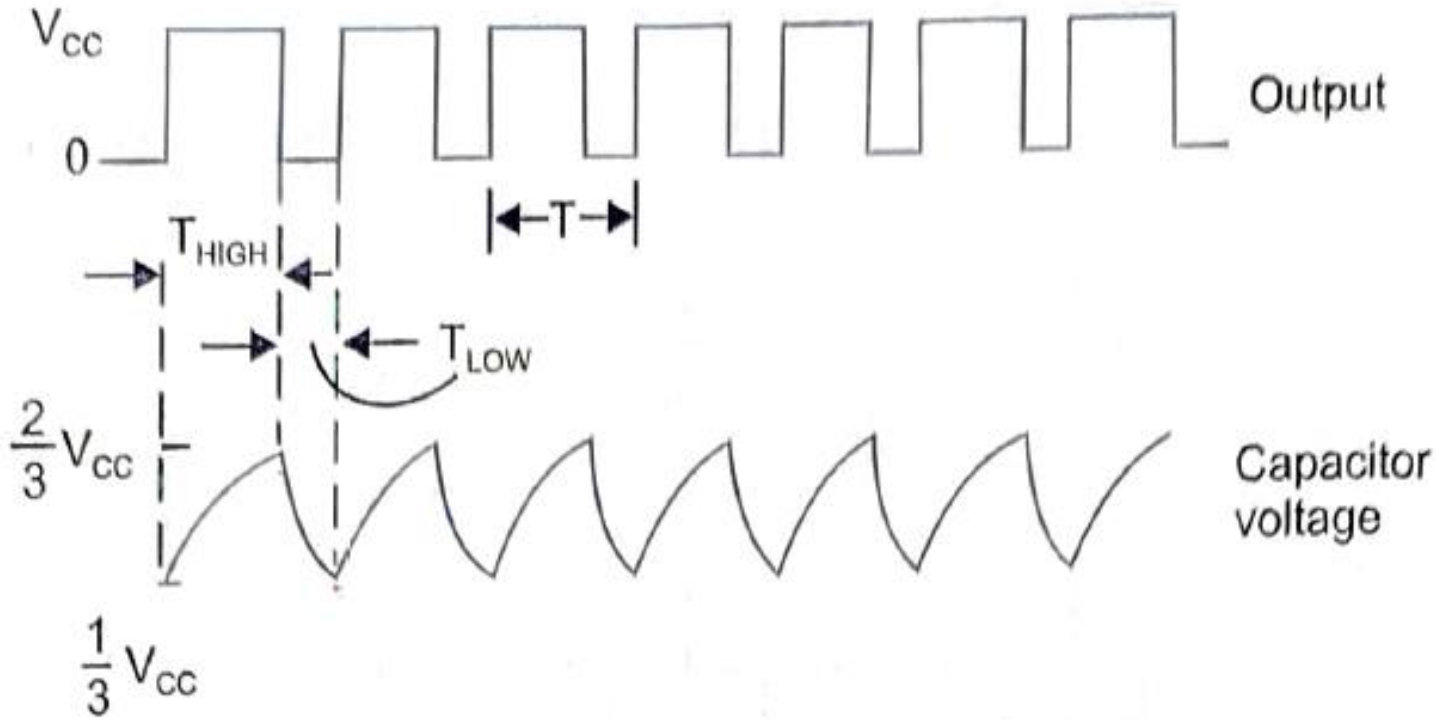


Functional diagram of astable multivibrator using 555 timer

- Tuning resistor is split into two sections R_A and R_B.
- Discharging transistor Q_1 is connected to junction of R_A and R_B.
- When the power supply V_{cc} is connected, external capacitor C charges towards Vcc with time constant $(R_A + R_B)C$
- During this time, the output is high(equals V_{cc}) as reset R=0, set S=1 and this combination makes $\bar{Q} = 0$.
- When capacitor voltage equals $(\frac{2}{3})\ Vcc$, the upper comparator triggers Flip flop and $\bar{Q} = 1$.

[V_{in}>V_{ref}; for +ve comparator Vout=+ve and resets]

- Output at pin 3 is zero. This makes Q_1 on and C discharges.
- During discharge of capacitor C, as it reaches less than $(\frac{1}{3})\ Vcc$, lower comparator is triggered and at this stage S=1,R=0 which turns $\bar{Q} = 0$.
- Now Q_1 is off and C charges [V_{in}< $(\frac{1}{3})\ Vcc$; for -ve comparator Vout=+ve and sets].
- Thus the capacitor is periodically charged and discharged between $(\frac{2}{3})\ Vcc$ and $(\frac{1}{3})\ Vcc$.



Timing sequence of astable multivibrator

The capacitor voltage for a low pass RC circuit subjected to a step input of V_{CC} volts is given by

$$v_c = V_{CC}(1 - e^{-t/RC})$$

The time t_1 taken by the circuit to charge from 0 to (2/3) V_{CC} is,

$$(2/3)\,V_{CC} = V_{CC}(1 - e^{-t_1/RC})$$

or, $$t_1 = 1.09\,RC$$

and the time t_2 to charge from 0 to (1/3) V_{CC} is,

$$(1/3)\,V_{CC} = V_{CC}(1 - e^{-t_2/RC})$$

or, $$t_2 = 0.405\,RC$$

So the time to charge from (1/3) V_{CC} to (2/3) V_{CC} is

$$t_{HIGH} = t_1 - t_2$$
$$t_{HIGH} = 1.09\,RC - 0.405\,RC = 0.69\,RC$$

So, for the given circuit,

$$t_{HIGH} = 0.69\,(R_A + R_B)C$$

The output is low while the capacitor discharges from (2/3) V_{CC} to (1/3) V_{CC} and the voltage across the capacitor is given by

$$(1/3)\,V_{CC} = (2/3)V_{CC}\,e^{-t/RC}$$

Solving, we get $t = 0.69\,RC$

So, for the given circuit, $t_{LOW} = 0.69\,R_BC$

Notice that both R_A and R_B are in the charge path, but only R_B is in the discharge path. Therefore, total time,

$$T = t_{HIGH} + t_{LOW}$$

or,

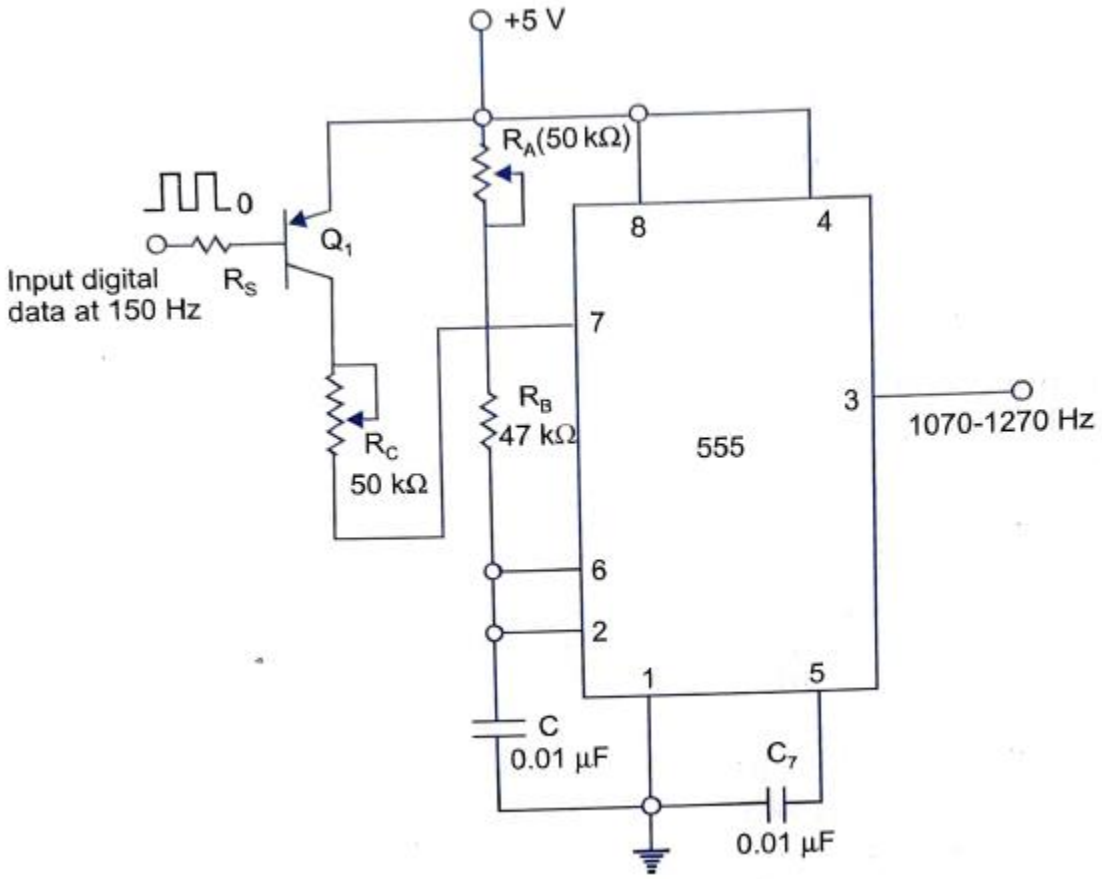
$$T = 0.69\,(R_A + 2R_B)\,C$$

So,

$$f = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C}$$

Applications in Astable mode

FSK generator:



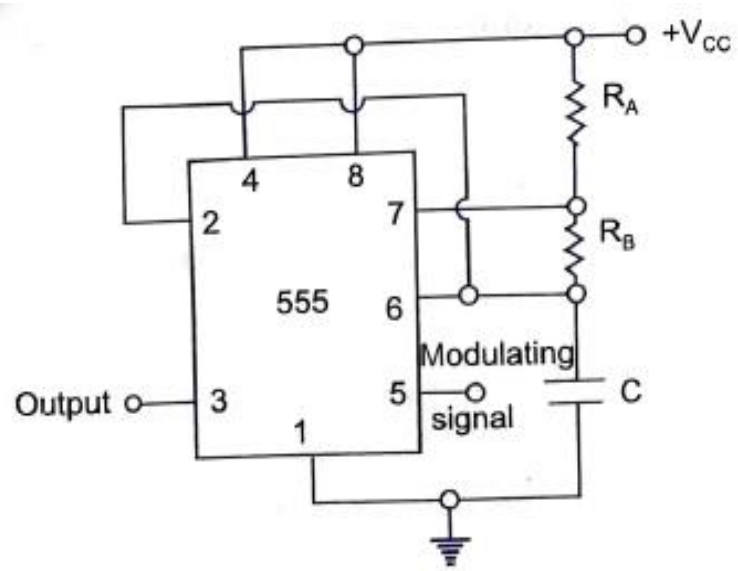
- Binary code is transmitted by shifting a carrier frequency between two preset frequencies.
- 555 timer in astable mode is used to generate FSK signal.
- When input is high, Q1 is off and 555 timer works in normal astable mode of operation.
- Frequency of operation is given by

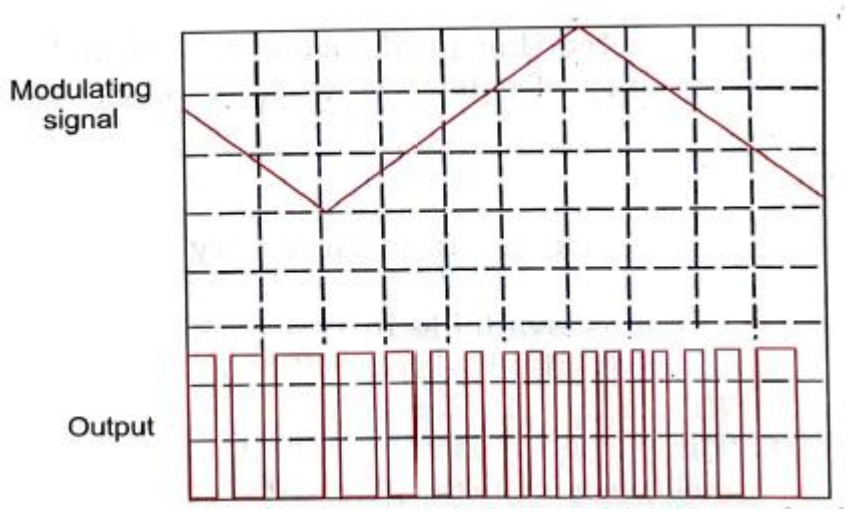
$$f_0 = \frac{1.45}{(R_A + 2R_B)C}$$

- When the input is low, Q1 is on and connects Rc across RA. The output frequency is now given by

$$f_0 = \frac{1.45}{(R_A || R_C) + 2R_B}$$

Pulse position modulator





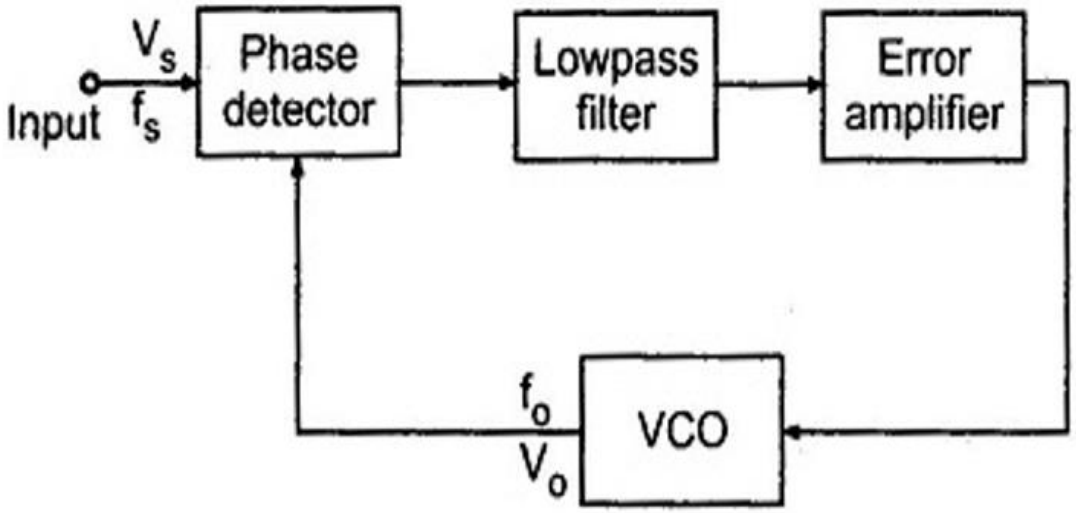
- Here the modulating signal is triangular wave. It is applied to pin 5 of 555 timer connected for astable operation
- Output pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied.

PHASE LOCKED LOOP

Operation of Basic PLL

PLL consists of

1. Phase detector / comparator
2. A low pass filter
3. An error amplifier
4. A Voltage Controlled Oscillator (VCO)



PHASE LOCKED LOOP

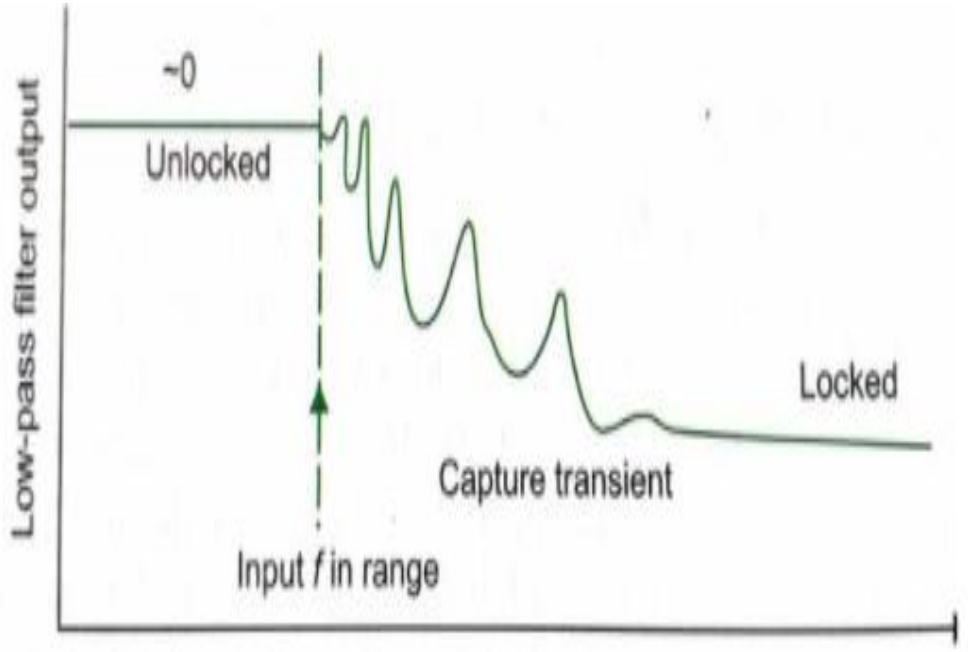
- VCO – a free running Multivibrator
- It operates at a set frequency f_o called free running frequency.
- This frequency is determined by an external timing capacitor and an external resistor.
- It can be shifted to either side by applying a dc control voltage v_c
- The frequency deviation is directly proportional to the dc control voltage and hence it is called a voltage controlled oscillator (VCO)
- If an input signal v_s of frequency f_s is applied to the PLL, the phase detector compares the phase and frequency of the incoming signal to that of the output v_o of VCO.
- If the two signals differ in frequency and/or phase, an error voltage v_e is generated.

PHASE LOCKED LOOP

- Phase detector is basically a multiplier and produces the sum (f_s + f_o) and difference (f_s - f_o) at its output.
- The high frequency component (f_s + f_o) is removed by LPF & difference component (f_s - f_o) is amplified and then applied as control voltage v_e to VCO.
- The signal v_c shifts the VCO frequency in a direction to reduce the frequency difference between f_s and f_o .
- Once this action starts, we say that the signal is in the capture range.
- VCO continues to change frequency till its output frequency is exactly same as input signal frequency.
- Then circuit is said to be locked.

PHASE LOCKED LOOP

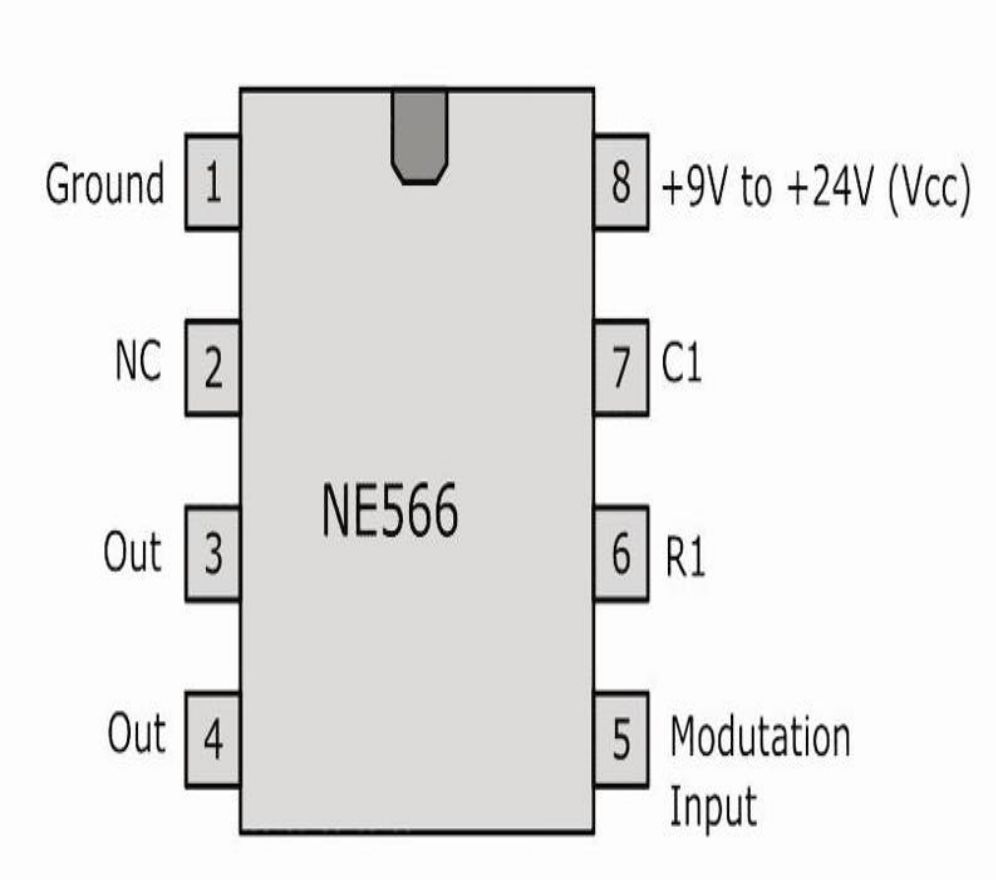
- Once locked, the output frequency f_o of VCO is identical to f_s except for a finite phase difference φ.
- This phase difference φ generates a corrective control voltage v_c to shift the VCO frequency from f_o to f_s and thereby maintain the lock.
- Once locked, PLL tracks the frequency changes of the input signal.
- Thus, a PLL goes through three stages:
- (i) free running
- (ii) capture
- (iii) locked or tracking
- As capture starts, a small sine wave appears. This is due to the difference frequency between the VCO and the input signal.
- Each successive cycle causes the VCO frequency to move closer to the input signal frequency. If VCO frequency is far away, the beat frequency will be too high to pass through the filter and the PLL will not respond.



PHASE LOCKED LOOP

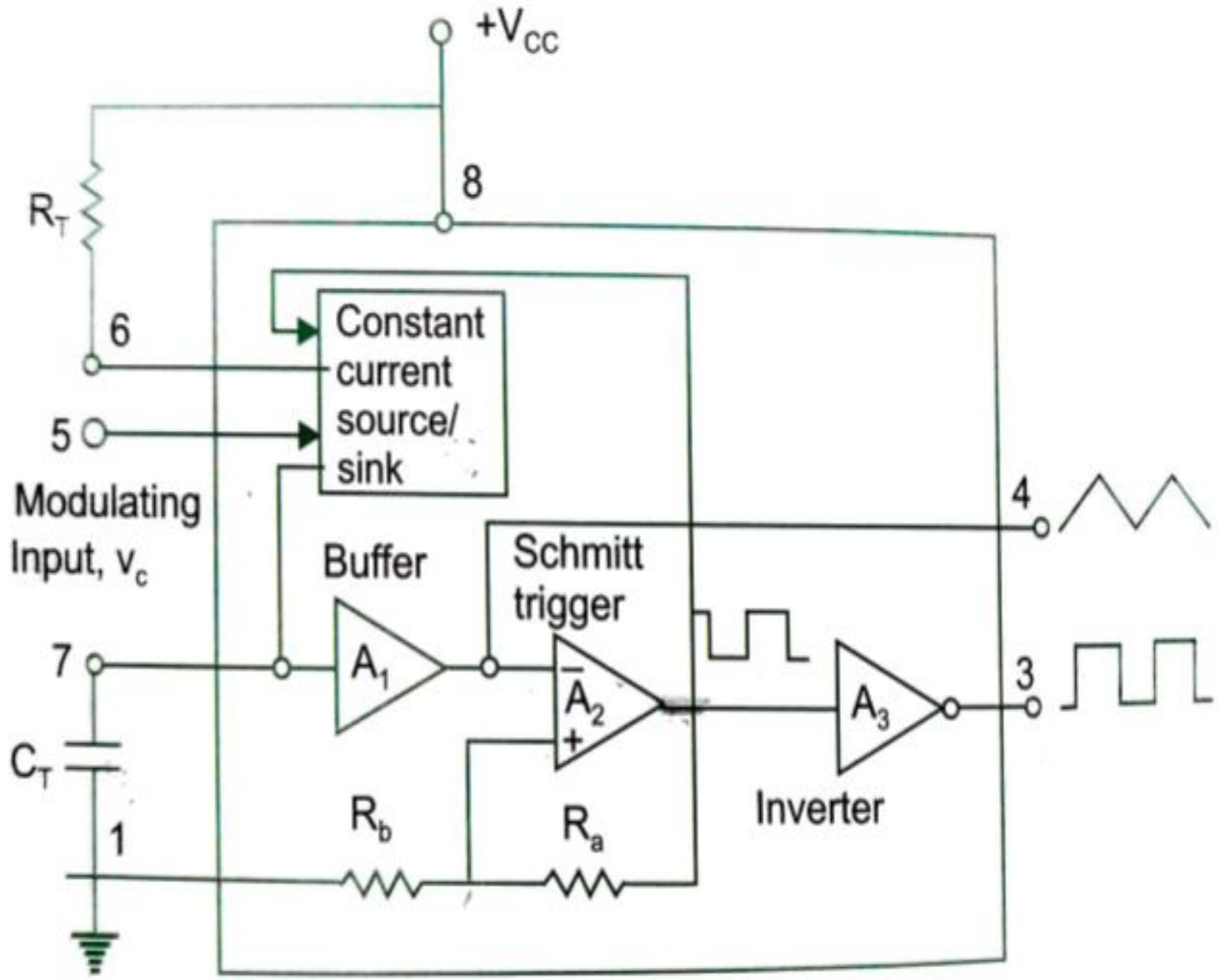
- **Lock in Range:** The range of frequency over which PLL can maintain lock with the incoming signal is called the lock-in range or tracking range. It is expressed as a percentage of f_o, the VCO frequency.
- **Capture range:** The range of frequency over which PLL can acquire lock with an input signal is called the capture range. It is also expressed as a percentage of f_o, the VCO frequency.
- **Pull-in time:** The total time taken by PLL to establish lock is called Pull-in time.

VOLTAGE CONTROLLED OSCILLATOR



- VCO is a type of oscillator where frequency of output oscillation can be varied by varying amplitude of input voltage.
- Timing capacitor is linearly charged or discharged by a constant current source or sink.
- Amount of current can be controlled by changing the voltage applied voltage at the modulating input or by changing the timing resistor.
- Voltage at Pin 6 is same as that of Pin 5.

Block Diagram

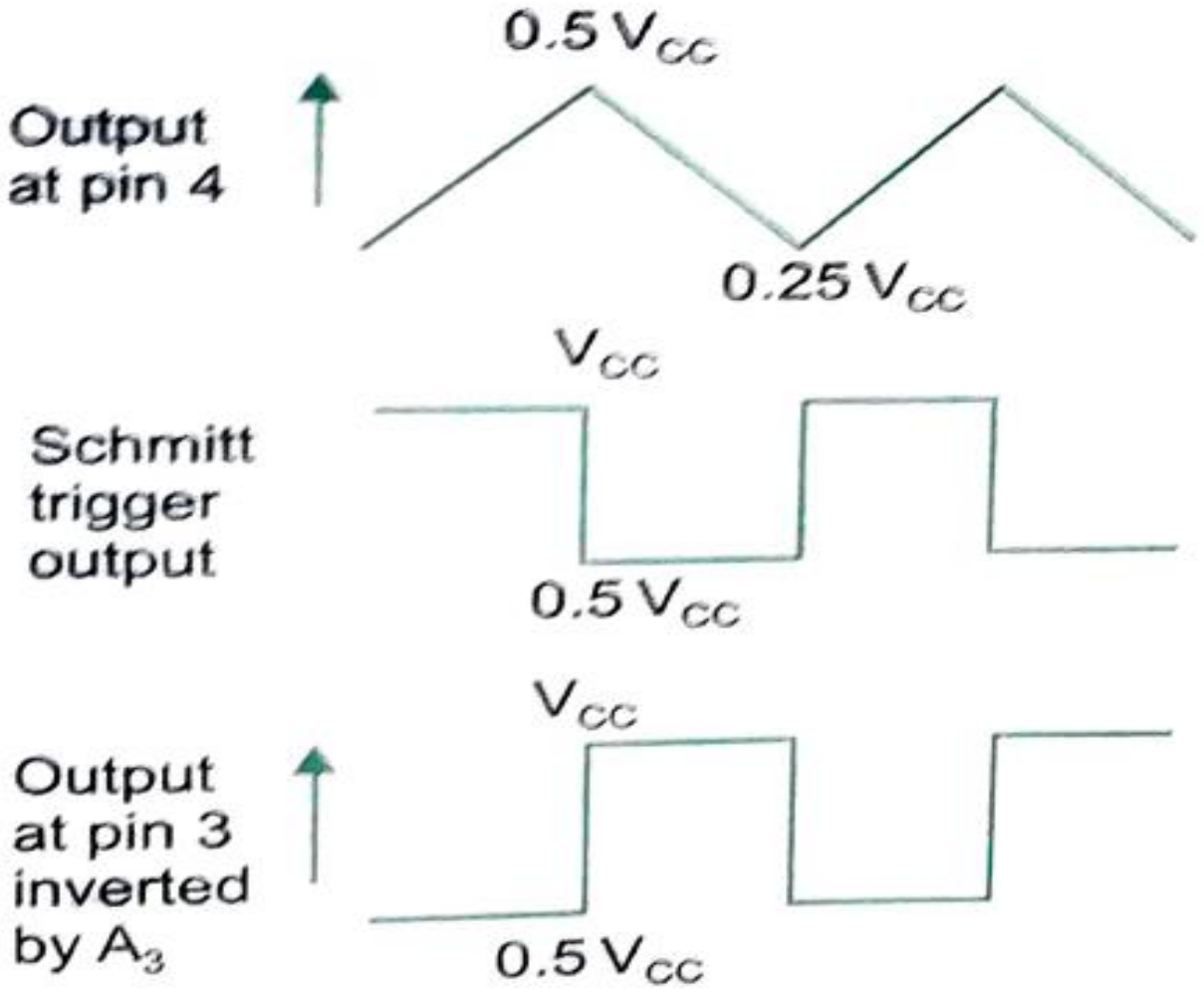


VCO

- Thus if the modulating voltage at pin 5 is increased, the output at pin 6 also increases, resulting in less voltage across R_T and thereby decreasing the charging current.
- The voltage across the capacitor C_T is applied to the inverting input terminal of Schmitt trigger A_2 via buffer amplifier A_1.
- The output voltage swing of the Schmitt trigger is designed to V_{cc} and 0.5 V_{cc}.
- If $R_a = R_b$ in the positive feedback loop, the voltage at the non- inverting input terminal of A_2 swings from 0.5 V_{cc} to 0.25 V_{cc}

VCO

- When the voltage on the capacitor C_T exceeds 0.5 V_{cc} during charging, the output of the Schmitt trigger goes LOW.
- The capacitor now discharges and when it is at 0.25 V_{cc} the output of Schmitt trigger goes HIGH.
- Since the source and sink currents are equal, capacitor charges and discharges for the same amount of time.
- This gives a triangular voltage waveform across C_T which is also available at pin 4.
- The square wave output of the Schmitt trigger is inverted by inverter A_3 and is available at pin 3.



Input and Output Waveform

Output Frequency of VCO

$$i\Delta t = C_T \, \Delta V$$

$$\frac{\Delta V}{\Delta t} = \frac{i}{C_T} \qquad (1)$$

The total voltage of capacitor changes from $0.25\ V_{cc}$ to $0.5\ V_{cc}$

$$\Delta V = 0.5V_{cc} - 0.25V_{cc}$$

$$\Delta V = 0.25V_{cc}$$

Sub in (1)

$$\frac{0.25V_{cc}}{\Delta t} = \frac{i}{C_T}$$

$$\Delta t = \frac{0.25V_{cc}\ C_T}{i} \qquad (2)$$

Output Frequency of VCO

The time period T of a triangular waveform = 2 Δt. The frequency of oscillator f_0 is,

$$f_0 = \frac{1}{T} = 2\,\Delta t$$

$$f_0 = \frac{i}{0.5\,V_{cc}\,C_T}$$

But

$$i = \frac{V_{cc} - V_c}{V_\infty\,C_T\,R_T}$$

$$f_0 = \frac{2\,(V_\infty - V_c)}{V_\infty\,C_T\,R_T}$$

The output frequency of VCO can be changed by

(i) R_T

(ii) C_T

(iii) V_c

If the modulating input at pin 5 is biased $\frac{7}{8}\,V_{cc}$

$$f_0 = \frac{2\,(V_{CC} - (\frac{7}{8})V_{CC}\,)}{V_{CC}\ C_T\ R_T} = \frac{0.25}{C_T\ R_T} \qquad (4)$$

Voltage to frequency conversion factor:

- Important parameter for V_{C0} is frequency conversion and is defined as

$$K_v = \frac{\Delta f_0}{\Delta V_c} \qquad (5)$$

Let original frequency be f_0 $and\ new\ frequency\ be f_1$

$$\Delta f_0 = f_1 - f_0$$

$$\Delta f_0 = \frac{2\,(V_{cc} - V_c + \Delta V_c)}{C_T\ R_T\ V_{cc}} - \frac{2\,(V_{cc} - V_c)}{C_T\ R_T\ V_{cc}}$$

$$= \frac{2(\Delta V_c)}{C_T\ R_T\ V_{cc}}$$

$$\Delta V_c = \frac{(V_{cc}\ \Delta f_0)C_T\ R_T}{2} \qquad (6)$$

Sub $C_T\ R_T$ from (4)

$$\Delta V_c = \frac{\Delta f_0)\ (0.25)\ V_{cc}}{2}$$

$$k_v = \frac{\Delta f_0}{\Delta V_c}$$

$$k_v = \frac{8\,\Delta f_0}{V_{cc}}$$

PLL APPLICATIONS

- The output from a PLL system can be obtained either as
  - ➢ the voltage signal $v_c(t)$ corresponding to the error voltage in the feedback loop or as
  - ➢ a frequency signal at VCO output terminal.
- Voltage output used in frequency discriminator application
- Frequency output used in signal conditioning, frequency synthesis or clock recovery applications.

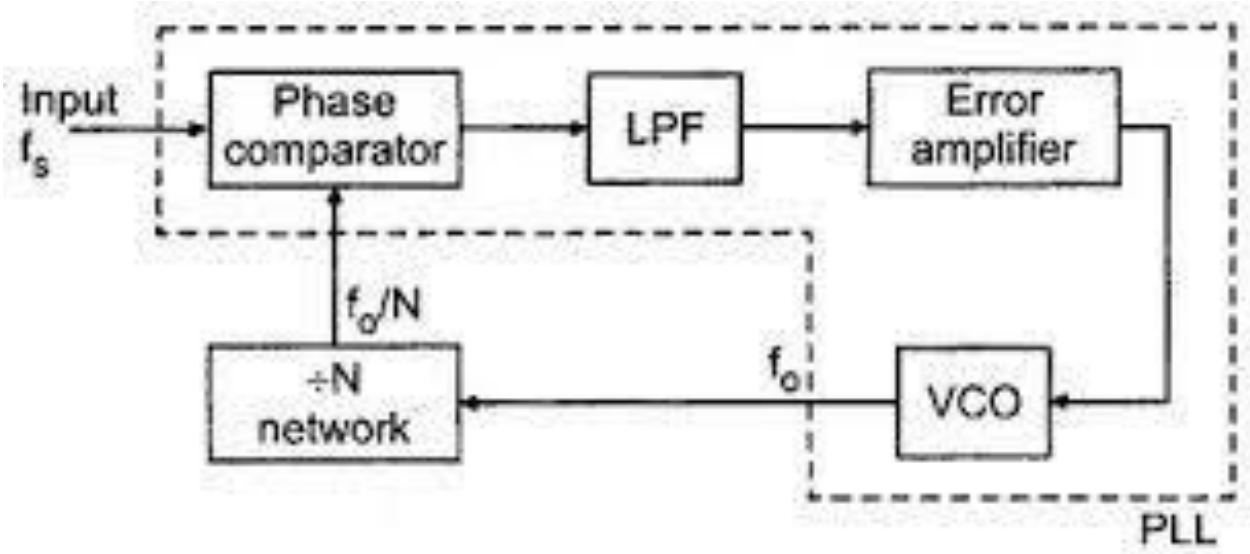
feedback loop or as
➢ a frequency signal at VCO output terminal.
• Voltage output used in frequency discriminator application
• Frequency output used in signal conditioning, frequency synthesis or clock recovery applications.

PLL Applications cont…

- **Voltage output:** when PLL is locked to input frequency, error voltage $v_c(t)$ is proportional to (f_s - f_o). If f_s is varied, v_c will also vary to maintain lock.
- **Frequency output:** If input signal comprises of many frequencies (including noise & other disturbances), the PLL can be made to lock, selectively on one particular frequency.
- The output of VCO would regenerate that particular frequency and attenuate other frequencies.
- This used for regenerating or reconditioning a desired frequency signal out of many undesirable frequency signals.

Frequency Multiplication/Division

- A divide by N network is inserted between output of VCO and phase comparator.
- In the locked state, the VCO output frequency f_o is given by, $f_o = N f_s$
- The multiplication factor can be obtained by selecting a proper scaling factor N of the counter.
- Frequency multiplication can also be obtained by using PLL in its harmonic locking mode.

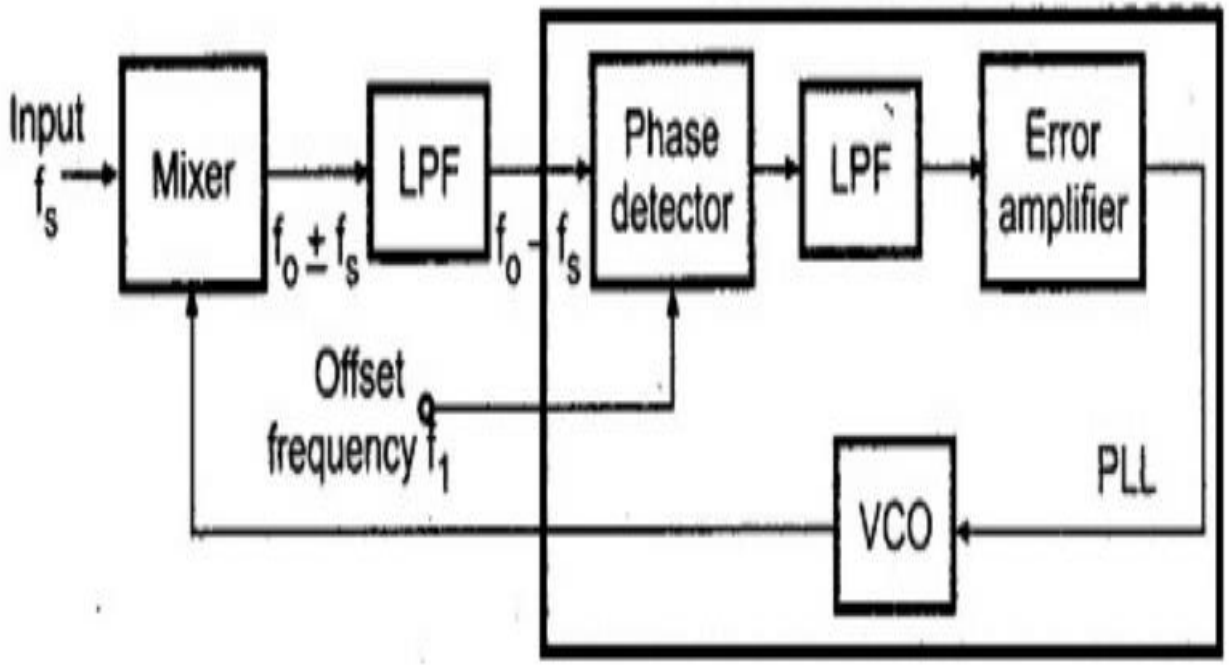


Frequency Multiplication/Division

- Frequency divider is inserted between output of VCO and phase comparator so that loop signal to PC is F_s while output of VCO is NF_0.
- Output is multiple of input frequency as long as the loop in the lock.
- Desired amount of multiplication can be obtained by selecting proper divide by N network where N is an integer.
- Frequency multiplication can also be obtained using PLL in harmonic locking mode.
- If input signal is rich in harmonics VCO can be directly locked to nth harmonic of the input signal with out connecting to any frequency divider in between.
- Effective locking may not take place if amplitude of high order harmonics are less.

Frequency Translation

- Multiplexer and low pass filter is connected externally to PLL.
- Signal f_s which has to shifted and output frequency f_0 of VCO are applied as input to mixer.

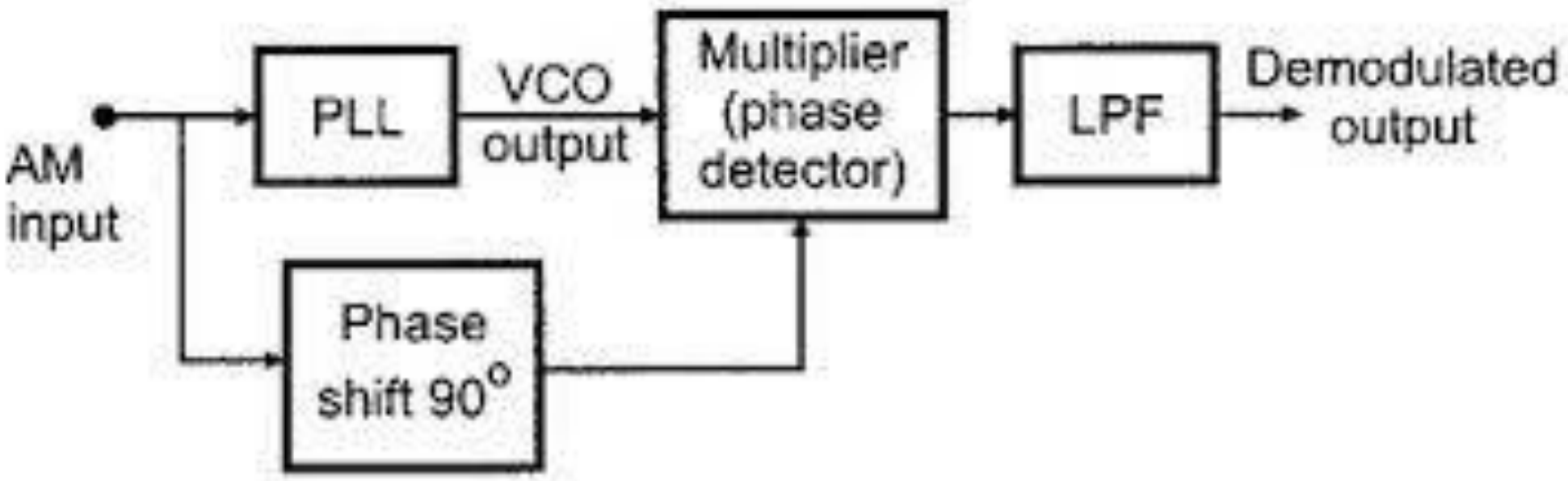


Frequency Translation

- Output of mixer contains sum and difference of the signals f_s and f_0
- The output of low pass filter contains only the difference signal between f_s and f_0
- Translation or offset frequency is applied to the phase comparator.
- When PLL is in lock state

$$f_0 - f_s = f_1$$
$$f_0 = f_s + f_1$$

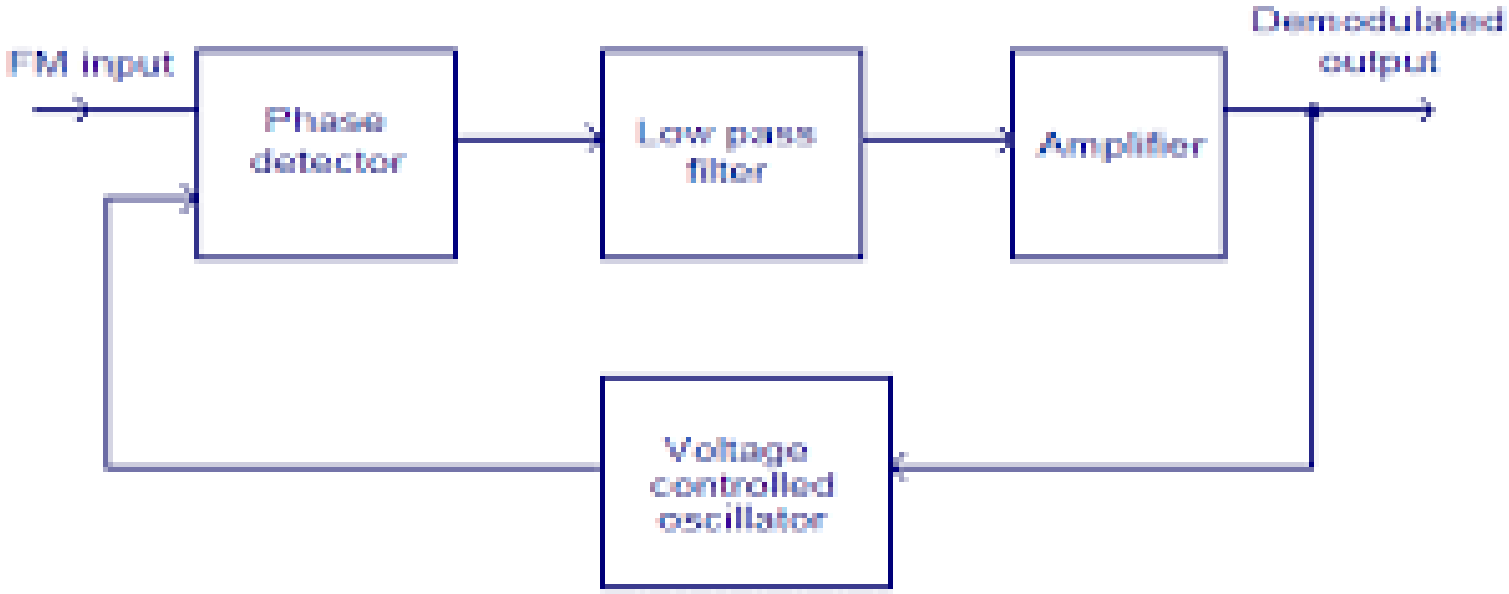
AM Detector


AM
input
PLL
VCO
output
Multiplier
(phase
detector)
LPF
Demodulated
output
Phase
shift 90°

AM Detection

- A PLL is used to demodulate the AM signal.
- PLL is locked to the carrier frequency of the incoming AM signal.
- The output of VCO that has the same frequency as the carrier, but unmodulated is fed to the multiplier.
- VCO output is always 90 degree out of phase with the incoming AM signal under the locked condition, the AM signal is also shifted in phase by 90 degree before being fed by the multiplier.
- This in turn makes both the signal applied to the multiplier is in same phase.
- The output of the multiplier has both the sum and the difference signal, the demodulated signal is obtained after filtering high frequency component by the LPF.
- AM detector exhibits high degree of selectivity and noise immunity which is not possible with conventional peak detector type AM modulators.

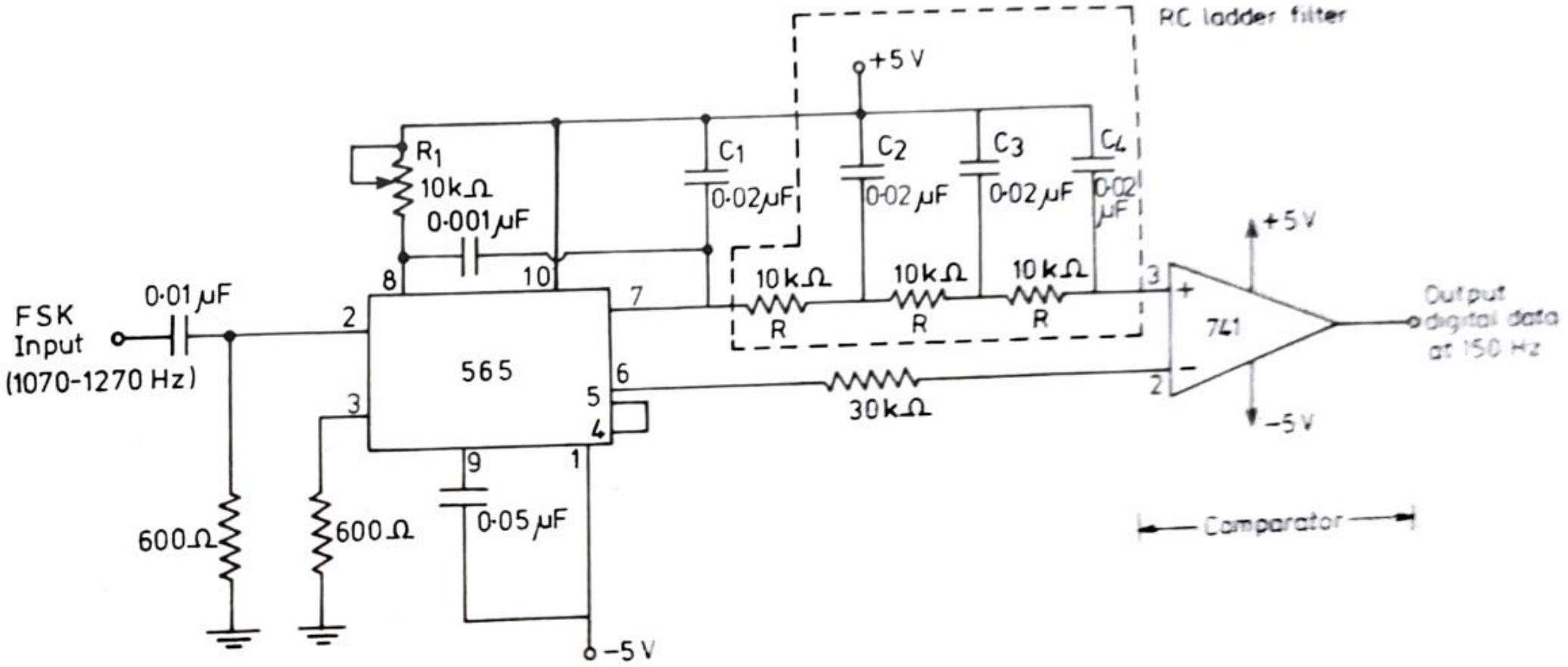
FM Demodulation



FM Demodulation

- If PLL is locked to an FM signal, the VCO tracks the instantaneous frequency of the input signal.
- The filtered error voltage which controls the VCO and maintains lock with the input signal is the demodulated FM output.
- The VCO transfer characteristics determines the linearity of the demodulated output.
- Since VCO used in the IC PLL is highly linear, it is possible to realize highly linear FM demodulators.

FSK Demodulation



FSK Demodulation

- If PLL is locked to an FM signal, the VCO tracks the instantaneous frequency of the input signal.
- The filtered error voltage which controls the VCO and maintained lock with the input signal is demodulated FM output.
- The VCO transfer characteristics determines the linearity of the demodulated output.
- Since, VCO used in IC PLL is highly linear, it is possible to realize highly linear FM demodulation.
- In digital data communication and computer peripheral, binary data is transmitted by means of carrier frequency which is shifted between two preset frequencies.
- This type of data transmission is called Frequency Shift Keying (FSK).

FSK Demodulation

- The binary data can be retried using the FSK demodulator at the receiving end.
- As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding dc shift at the output.
- A three stage filter removes the carrier component and the output signal is made logic compatible by a voltage comparator.