Laboratory Report Cover Sheet

SRM Institute of Science and Technology Faculty of Engineering and Technology Department of Electronics and Communication Engineering
15EC203J Digital Systems **Third Semester, 2018-19 (odd semester)**

Name :

Register No. :

Day / Session :

Venue :

Title of Experiment :

Date of Conduction :

Date of Submission :

Particulars	Max. Marks	Marks Obtained
Pre-lab questions	10	
In-lab experiment	20	
Post-lab questions	10	
Total	40	

REPORT VERIFICATION

Date :

Staff Name :

Signature :

Lab 4: Design of Encoder & Decoder

8:3 ENCODER

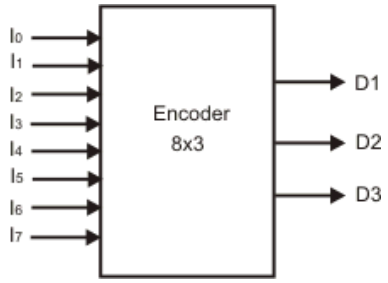

Figure 3.1: Block Schematic of 8x3 Encoder

Truth Table of 8x3 Encoder

Inputs								Outputs		
I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	D_3	D_2	D_1
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

The output equations of the encoder 8X3 are the following:

D3 = I4 +I5 +I6 +I7

D2 = I2 +I3 +I6 +I7

D1 = I1 +I3 +I5 +I7

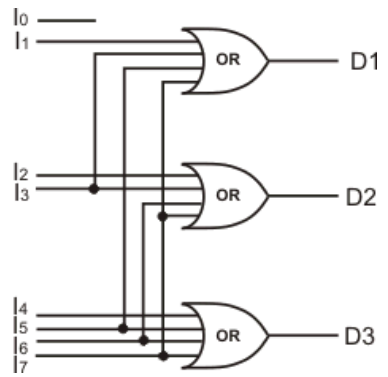

Figure 3.2: Realization of 8x3 Encoder

Lab 4: Design of Encoder & Decoder

Aim

To design and verify the truth table for 8-3 Encoder & 3-8 Decoder logic circuit.

Hardware Requirement

Equipment	:	Digital IC Trainer Kit
Software	:	Logicsim (Optional-TinkerCAD/LTspice)
Discrete Components	:	74LS08 Quad 2 input AND gate
		74LS32Quad 2 input OR gate
		74LS04 Hex 1 input NOT gate

Theory

(i) Encoder: Encoder takes all the data inputs one at a time and converts them to a single encoded output, it is a multi-input data line, combinational logic circuit that converts the logic level 1 data at its input to an equivalent binary code at its output. Encoder has 2^n input lines with common types that include 4 to 2,8 to 3 & 16 to 4 line configuration. Encoders are available to encode either a decimal or hexadecimal input pattern to typically binary or BCD output code.

(ii)Decoder: A decoder is a multiple-input, multiple-output logic circuit that converts coded inputs into coded outputs, where the input and output codes are different; e.g. n-to-2n, BCD decoders. Decoding is necessary in applications such as data multiplexing, 7 segment display and memory address decoding. Any n-variable logic function, in canonical sum-of-minterms form can be implemented using a single n-to-2^n decoder to generate the minterms, and an OR gate to form the sum. The output lines of the decoder corresponding to the minterms of the function are used as inputs to the or gate. Any combinational circuit with n inputs and m outputs can be implemented with an n-to-2^n decoder with m OR gates. Suitable when a circuit has many outputs, and each output function is expressed with few minterms.

Pre lab Questions

1. What is an encoder?
2. What is a decoder?
3. List the difference between Multiplexer & Encoder?
4. Draw 4-2 encoder circuit?

Procedure

1. The truth table and a design of 8 to 3 Encoder, 3 to 8 decoder are given.
2. Realize this circuit on your board by using logic circuit.
3. Connect three inputs x,y,z to the switches & eight outputs vice-versa.
4. Connect the functions outputs to LEDs.
5. Verify input/output relation (Truth table) of this converter.

3:8 DECODER

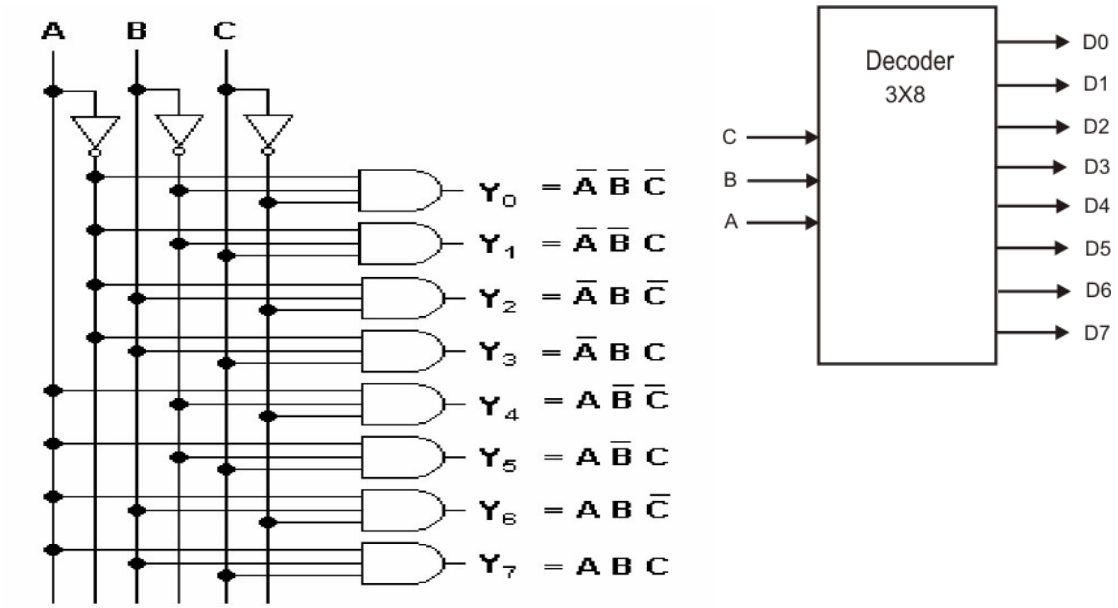

Figure 3.3: Block Schematic of 3x8 Decoder

Truth Table of 3x8 Decoder

Inputs			Outputs							
A	B	C	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Post lab Questions

1. Draw the logic symbol of 3x8 Decoder using two 2x4 decoder?
2. Implement the following expression using decoder F=XY+YZ.
3. Write the truth table for 3-input priority encoder.
4. Realize a Half Adder using a 2-to-4 line decoder.
5. Realize a Full Adder using a 3-to-8 line decoder.
6. Realize a Full Subtractor using 3-to-8 line decoder with inverting outputs.

Result: