

18ECE206J - Answer key
Advanced digital
System design

Set C

CT1 - C

PART-A (5x1 = 5 Marks) (Answer all)

1. (B) Shannon
2. (C) $(A+C+D)$
3. (b) 5
4. (b) $Z=0$
5. (b) State diagram.

PART-B (2x10 = 20 Marks)

(Answer any two)

6. i)
$$f(w, x, y) = wx + \bar{w}y + \bar{x}\bar{y}$$

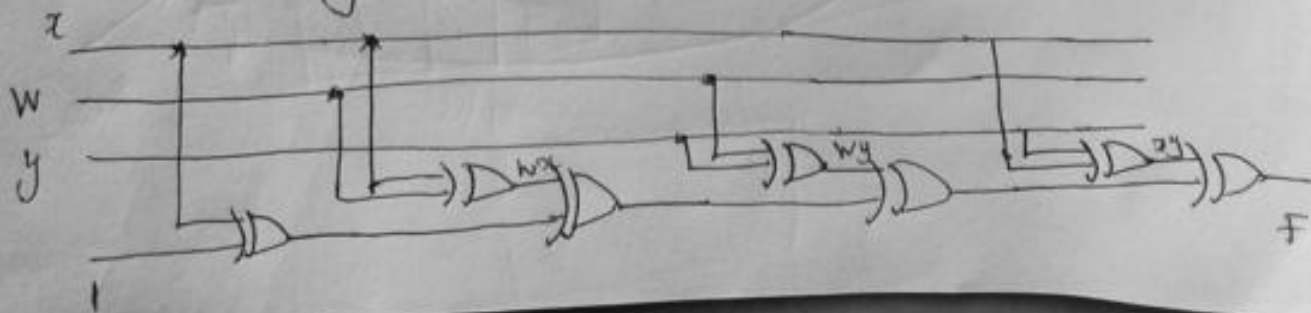
$$= wx \oplus (1 \oplus w)y \oplus (1 \oplus x)(1 \oplus y)$$

$$= wx \oplus y \oplus wy \oplus 1 \oplus x \oplus y \oplus xy$$

$$= \underbrace{1 \oplus x \oplus y \oplus y}_0 \oplus wx \oplus wy \oplus xy$$

$$= 1 \oplus x \oplus wx \oplus wy \oplus xy \quad (3m)$$

Logic diagram (2m)



(ii)

$$F(A, B, C) = \bar{A}\bar{C} + AB + AC$$

using 4:1 Mux.

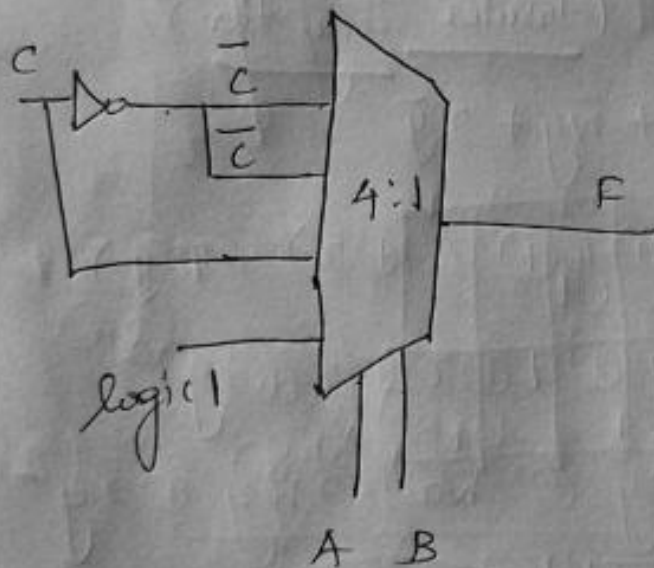
$$= \bar{A}\bar{B}(\bar{C} + 0 + 0) + \bar{A}B(\bar{C} + 0 + 0) \\ + A\bar{B}(0 + 0 + C) + AB(0 + 1 + \underline{C})$$

$$1 + C = 1$$

$$= \bar{A}\bar{B}(\bar{C}) + \bar{A}B(\bar{C}) + A\bar{B}(C) + AB(1)$$

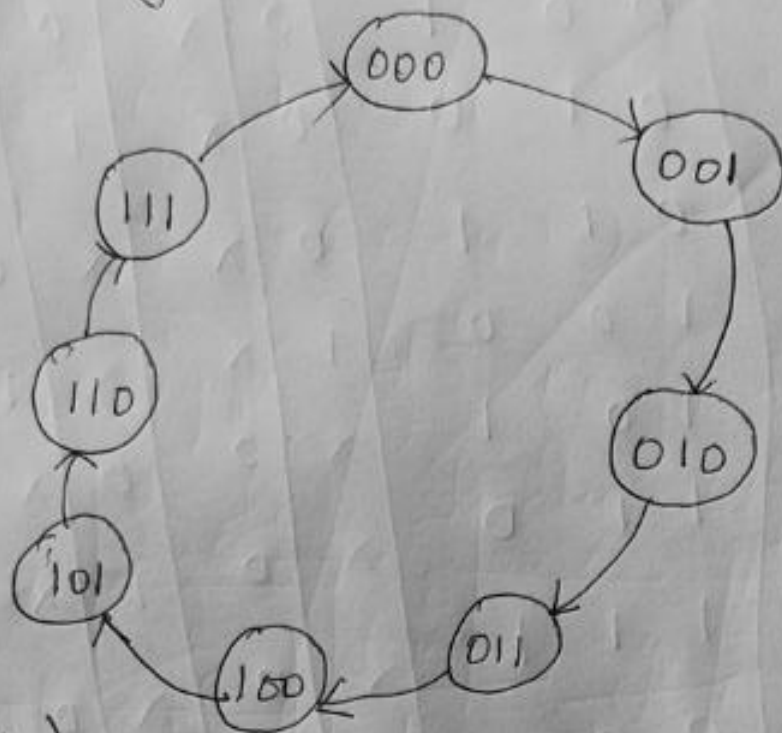
(3m)

logic function (2m)



⑦. Design 3-bit synchronous up Counter.

Step 1 State diagram: (1m)



Step 2 (1m)
State table:

Present State	Next State
000	001
001	010
010	011
011	100
100	101
101	110
110	111
111	000

Step 3

Excitation table for Counter (3 m)

Present State			Next State			Flipflop Inputs					
Q_2	Q_1	Q_0	Q_2^*	Q_1^*	Q_0^*	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	0	0	0	X	1	X	1	X	1

Step 4 k-map simplification

J_1

Q_2	$Q_1 Q_0$	00	01	11	10
0	0	1	X	X	X
1	0	1	X	X	X

$J_1 = Q_0$

K_1

Q_2	$Q_1 Q_0$	00	01	11	10
0	X	X	1	0	0
1	X	X	1	0	0

$K_1 = Q_0$

J_2

Q_2	$Q_1 Q_0$	00	01	11	10
0	0	0	1	0	0
1	X	X	X	X	X

$J_2 = Q_1 Q_0$

J_0

Q_2	$Q_1 Q_0$	00	01	11	10
0	1	X	X	1	0
1	1	X	X	1	0

$J_0 = 1$

K_0

Q_2	$Q_1 Q_0$	00	01	11	10
0	X	1	1	X	0
1	X	1	1	X	0

$K_0 = 1$

K_2

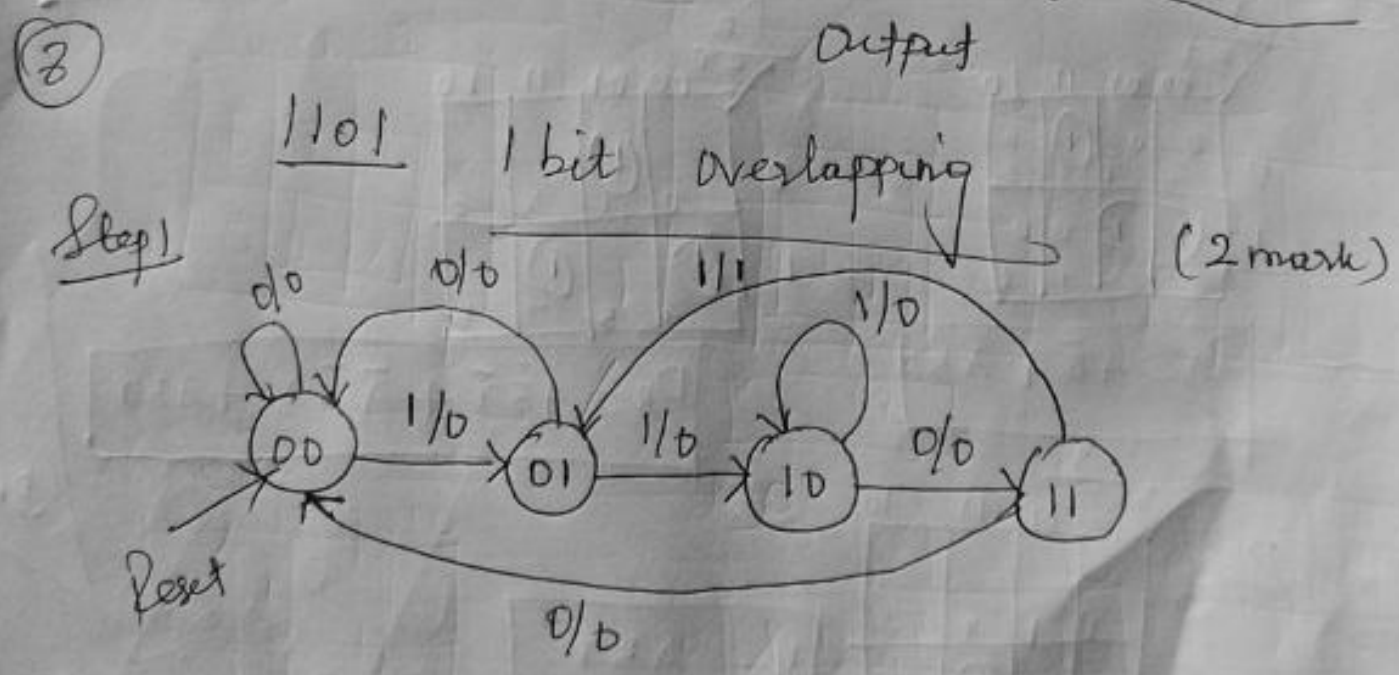
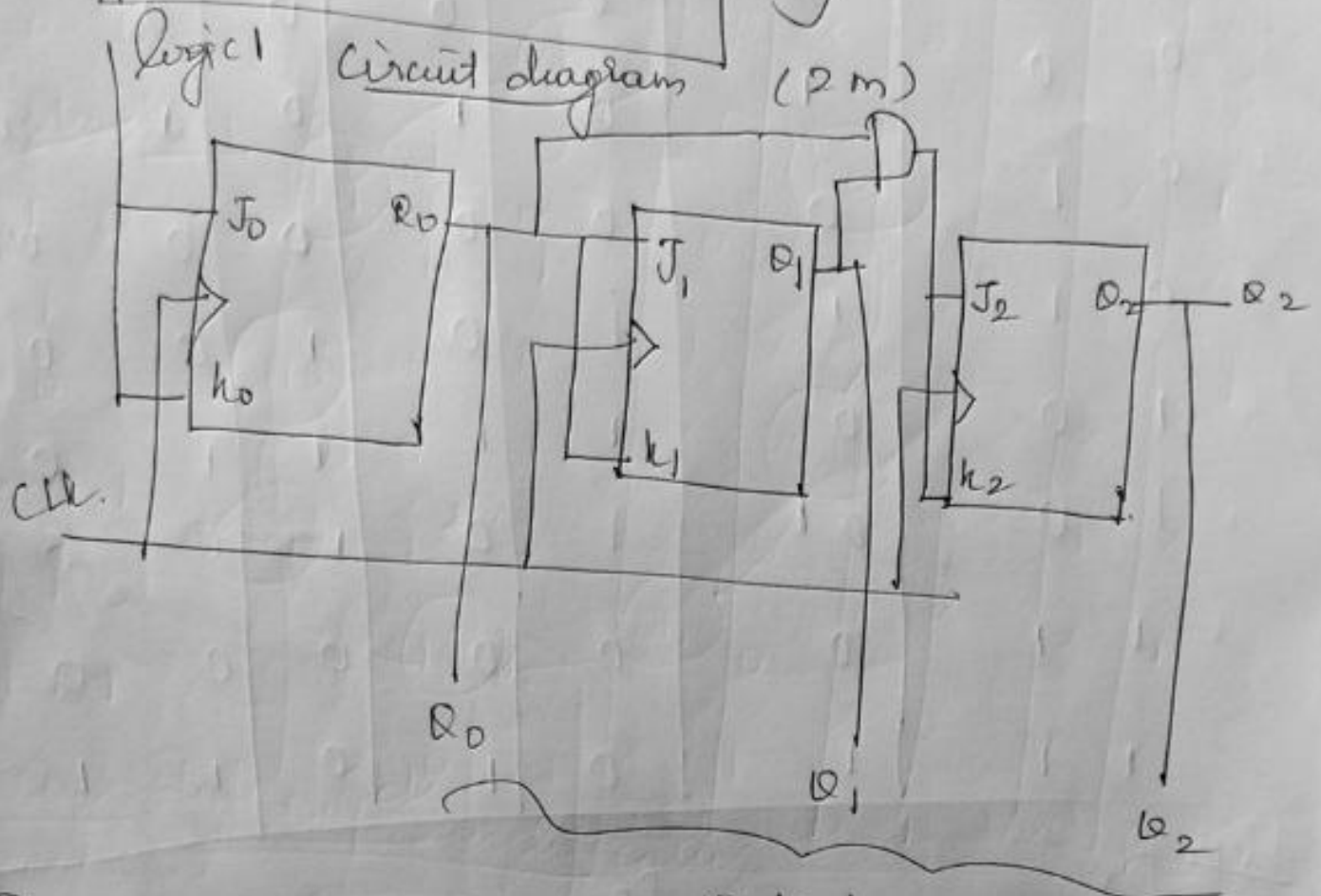
Q_2	$Q_1 Q_0$	00	01	11	10
0	X	X	X	X	0
1	0	0	1	0	0

$K_2 = Q_1 Q_0$

$$\begin{aligned} J_0 &= 1 & k_0 &= 1 \\ J_1 &= Q_0 & k_1 &= Q_0 \\ J_2 &= Q_0 Q_1 & k_2 &= Q_0 Q_1 \end{aligned}$$

}

(3 m)



Step 2 (3m)

Present State		Input	Next State		Flipflop T/P		O/P
A	B	α	$A_{(t+1)}$	$B_{(t+1)}$	D_A	D_B	y
0	0	0	0	0	0	0	0
1	0	1	0	1	0	1	0
2	0	0	0	0	0	0	0
3	0	1	1	0	1	0	0
4	1	0	1	1	1	1	0
5	1	0	1	0	1	0	0
6	1	1	0	0	0	0	0
7	1	1	0	1	0	1	1

Step 3

D_A

A	$B\alpha$			
	00	01	11	10
0	0	0	1	0
1	1	1	0	0

$$D_A = A\bar{B} + \bar{A}B\alpha$$

D_B

A	$B\alpha$			
	00	01	11	10
0		1		
1	1		1	

$$D_B = A\bar{B}\bar{\alpha} + \bar{A}\bar{B}\alpha + AB\alpha$$

A	$B\alpha$			
	00	01	11	10
0		1	3	2
1			1	

$$y = AB\alpha$$

Circuit diagrams
(2m)

(3m)