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B.Tech. DEGREE EXAMINATION, JULY 2022

Fourth Semester

18ECE206J – ADVANCED DIGITAL SYSTEM DESIGN

(For the candidates admitted from the academic year 2020-2021 to 2021-2022)

Note:

(i) **Part - A** should be answered in OMR sheet within first 40 minutes and OMR sheet should be handed over to hall invigilator at the end of 40th minute.

(ii) **Part - B** should be answered in answer booklet.

Time: 2½ Hours | Max. Marks: 75

PART – A (25 × 1 = 25 Marks) | Marks | BL | CO | PO

Answer **ALL** Questions

1. How many select lines are required to make a 64×1 multiplexer? | 1 | 2 | 1 | 1

   (A) 2 (B) 4
   (C) 6 (D) 8

2. Flip flop is used as | 1 | 1 | 1 | 1

   (A) Converter element (B) Storage element
   (C) Delay element (D) Inverter element

3. How many states will be present while detecting the sequence 1101 using Moore machine? | 1 | 2 | 1 | 1

   (A) 4 (B) 5
   (C) 6 (D) 7

4. _____can be used to decompose functions with a large number of variables into functions with less number of variables | 1 | 1 | 1 | 1

   (A) Shannon's expansion theorem (B) Consensus theorem
   (C) De-Morgan's theorem (D) Reed-Muller theorem

5. Dual consensus theorem of $(X+Y)(\bar{X}+Z)(Y+Z)$ is | 1 | 2 | 1 | 1

   (A) $(X+Y)(Y+Z)$ (B) $(X+Y)(\bar{X}+Z)$
   (C) $(\bar{X}+Z)(Y+Z)$ (D) $(X+Y)(\bar{X}+\bar{Z})$

6. Which types of memory elements are used in synchronous sequential circuits? | 1 | 1 | 2 | 2

   (A) Unclocked flip-flops (B) Clocked flip-flops
   (C) Time delay elements (D) ROM

7. The operation of the logic function is defined in the _____ | 1 | 2 | 2 | 2

   (A) Entity section (B) Architecture section
   (C) Component section (D) Port declaration

8. Which of the following statement is a concurrent statement? 1 1 2 2
   (A) Begin (B) End
   (C) Process (D) Case

9. "ROL" is a _____operator. 1 1 2 2
   (A) Shift (B) Logical
   (C) Arithmetic (D) Relational

10. ASM chart has _____ 1 1 2 2
   (A) 1 entry (B) 2 entries
   (C) 3 entries (D) 4 entries

11. _____flow table has only one stable state in each row. 1 1 3 2
   (A) Primitive (B) Non-primitive
   (C) Transition (D) FSM

12. Two or more binary state variables will change value when one input variable changes is called as _____ 1 1 3 2
   (A) Glitches (B) Hazards
   (C) Race (D) Don't care condition

13. A flow table with 4 rows required a minimum of _____state variable. 1 2 3 2
   (A) 1 (B) 2
   (C) 3 (D) 4

14. Implication table is used to find _____states 1 1 3 2
   (A) Compatible (B) Non-compatible
   (C) Unknown (D) Unequivalent

15. What would a wait statement do? 1 1 3 2
   (A) Performs looping execution (B) Performs unequal execution
   (C) Performs execution only on the rise time (D) Suspends after execution of last statement

16. Programmable array logic (PAL) consists of _____AND gates and _____OR gates. 1 1 4 2
   (A) Fixed, programmable (B) Programmable, fixed
   (C) Fixed, fixed (D) Programmable, programmable

17. PLA connected with _____ to becomes PAL. 1 1 4 2
   (A) AND gate (B) OR gate
   (C) XOR gate (D) Flip gate

18. Dynamic hazard occurs in _____ 1 1 4 2
   (A) Sequential circuit (B) Combinational circuit
   (C) Clocked circuit (D) Un clocked circuit

19. In PROM all the _____are decoded. 1 2 4 2
   (A) Maxterms (B) Min terms
   (C) Logics (D) Array elements

20.	FPGA refers to (A) Field Programmable Gate Array (B) Field Problem Gate Array (C) First Programmable Gate Array (D) First Programmable Gate Arithmetic	1	1	4	2
21.	What is the use of LUT in the CLB block? (A) Function generator (B) Storage (C) READ (D) Write	1	1	5	2
22.	How many single length lines are available in XILINX 4000 interconnections? (A) 4 (B) 8 (C) 12 (D) 16	1	1	5	2
23.	How many logic inputs are available in XILINX 3000 FPGA? (A) 5 (B) 6 (C) 4 (D) 7	1	1	5	2
24.	PORT map is used in _____ modelling. (A) Behavioural (B) Structural (C) Data flow (D) Circuit level	1	1	5	2
25.	Identify the modelling of the following program, architecture ar of find is begin $x <= a$ and b; end ar; (A) Behavioural (B) Structural (C) Data flow (D) Switch level	1	2	5	2

PART – B (5 × 10 = 50 Marks)

Answer **ALL** Questions

		Marks	BL	CO	PO
26. a.	A sequential circuit has an input (X) and one output (Z). The circuit produces an output Z=1, for the input sequence 101. Find the mealy state graph and design the circuit using D-flip flop. $X = 0011,011,001,010,100$ $Z = 0000010000010100$	10	3	1	3
	(OR)				
b.i.	State Shannon's expansion theorem and implement the following function using 4×1 MUX. $F = \overline{w_1}\,\overline{w_3} + w_1 w_2 + w_1 w_3$	5	3	1	3
ii.	Prove $\overline{A}B\overline{D} + BCD + A\overline{B}\overline{C} + A\overline{B}D = B\overline{CD} + AD + \overline{A}BC$ using Consensus theorem.	5	3	1	3

27. a. Reduce the following state table using implication chart method and use appropriate state assignment rules on the reduced states. 10 3 2 3

Present state	Next state		Output z
	$x=0$	$x=1$	
a	e	e	1
b	c	e	1
c	i	h	0
d	h	a	1
e	i	f	0
f	e	g	0
g	h	b	1
h	c	d	0
i	f	b	1

(OR)

b. Explain VHDL data types and operators with an example. 10 3 2 3

28. a. An asynchronous sequential circuit with two inputs X and Y and with one output Z. whenever Y is 1, input X is transferred to Z. when Y is 0, the output does not change for any change in X. Draw the state diagram and mention its reduced flow table. 10 3 3 3

(OR)

b. An asynchronous sequential circuit is described by the excitation and output function $Y = X_1\bar{X}_2 + \left(X_1 + \bar{X}_2\right)Y$ and $Z = Y$. Where Y and Z are excitation and output functions respectively. 10 3 3 3

(i) Draw the logic diagram
(ii) Derive the transition table and output map
(iii) Obtain a two-state flow table
(iv) Describe the behavior of the circuit

29. a. Define hazards and explain various types of hazards with suitable example. 10 3 4 3

(OR)

b. Illustrate how a PLA can be used for combinational logic design with reference to the functions 10 3 4 3

$f_1(a,b,c) = \sum m(0,1,3,4)$

$f_2(a,b,c) = \sum m(1,2,3,4,5)$

Realize the same assuming that a 3×4×2 PLA is available.

30. a. With a neat diagram, explain the architecture of Xilinx 3000 series FPGA. 10 3 5 3

(OR)

b. Write a VHDL code to implement 4-bit binary adder using structural design approach. 10 3 5 3

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