Laboratory Report Cover Sheet

SRM Institute of Science and Technology Faculty of Engineering and Technology Department of Electronics and Communication Engineering
15EC203J Digital Systems **Third Semester, 2018-19 (odd semester)**

Name :

Register No. :

Day / Session :

Venue :

Title of Experiment :

Date of Conduction :

Date of Submission :

Particulars	Max. Marks	Marks Obtained
Pre-lab questions	10	
In-lab experiment	20	
Post-lab questions	10	
Total	40	

REPORT VERIFICATION

Date :

Staff Name :

Signature :

Lab 10: Design of 3-bit Synchronous Counters

3 BIT SYNCHRONOUS COUNTERS

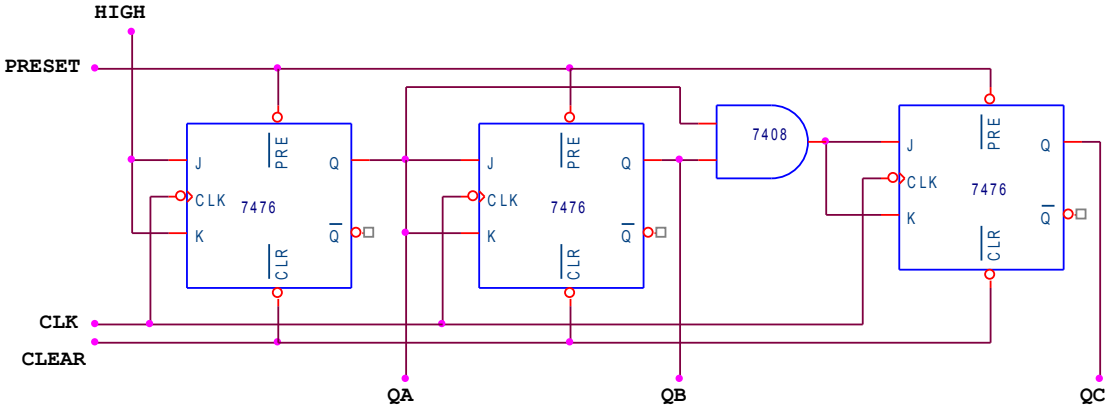

Figure 9.1: Logic diagram of 3-bit Synchronous counter

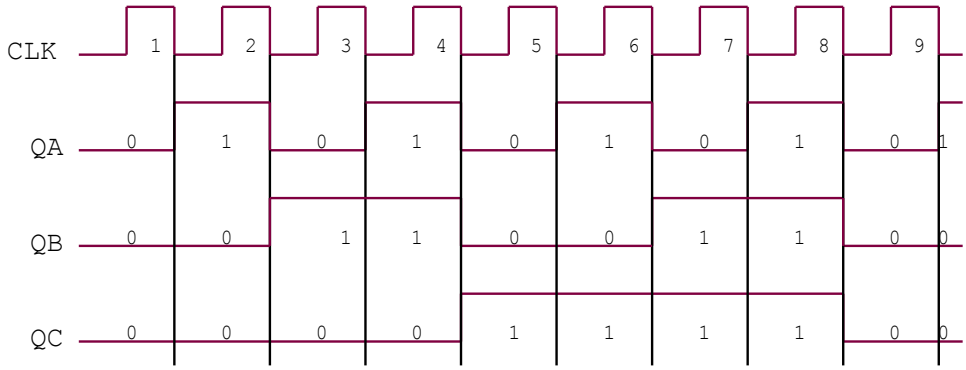

Figure 9.2: Timing Diagram of 3-bit Counter

Lab 10: Design of 3-bit Synchronous Counters

Aim

To design and verify the truth table for 3-bit synchronous up/down counter.

Hardware Requirement

Equipment	:	Digital IC Trainer Kit
Discrete Components	:	IC 7473 Dual JK Flip Flop 74LS08 Quad 2 input AND gate 74LS32Quad 2 input OR gate 74LS04 Hex 1 input NOT gate

Theory

Circuits for counting events are frequently used in computers and other digital systems. Since a counter circuit must remember its past states, it has to possess memory. The number of flip flops used and how they are connected determine the number of states and the sequence of the states that the counter goes through in each complete cycle. Counters can be classified into two broad categories according to the way they are clocked:

a. Asynchronous (Ripple) Counters - the first flip-flop is clocked by the external clock pulse, and then each successive flip -flop is clocked by the Q or Q' output of the previous flip -flop.
b. Synchronous Counters - all memory elements are simultaneously triggered by the same clock.

Synchronous Counters

In *synchronous counters*, the clock inputs of all the flip-flops are connected together and are triggered by the input pulses. Thus, all the flip-flops change state simultaneously (in parallel). The circuit below is a 3-bit synchronous counter. The J and K inputs of FF0 are connected to HIGH. FF1 has its J and K inputs connected to the output of FF0, and the J and K inputs of FF2 are connected to the output of an AND gate that is fed by the outputs of FF0 and FF1. After the 3rd clock pulse both outputs of FF0 and FF1 are HIGH. The positive edge of the 4th clock pulse will cause FF2 to change its state due to the AND gate.

The most important advantage of synchronous counters is that there is no cumulative time delay because all flip -flops are triggered in parallel. Thus, the maximum operating frequency for this counter will be significantly higher than for the corresponding ripple counter.

Pre Lab questions

1. How does synchronous counter differ from asynchronous counter?
2. What is the difference between the latch, flip-flop and master –slave Flip-flop?
3. A 4-bit up/down binary counter is in the DOWN mode and in the 1010 state. On the next clock pulse, to what state does the counter go?
4. How many flip-flops do you require to design Mod-7 counter.
5. Give the Transition table and excitation table of JK Flip flop.

Lab Procedure

1. Construct the logic circuit as shown in figure 9.1.
2. Apply clock pulses.
3. Verify the count sequence as given in figure 9.2.

PostLab questions

1. Deign a 3-bit Up/Down Gray Code Counter using D Flip-flop
2. What are the differences in Master-Slave JK Flip-flop, a +ve edge triggered JK Flip-flop and a -ve edge triggered JK Flip-flop.
3. When does a JK Flip-flop act as a divide –by- 2 circuits?
4. What are the advantages of an edge-triggered Flip-flop over a level-triggered device?
5. A negative edge triggered Flip-flop has the following timing parameters t_{SU}=15ns, t_{hold}=5ns, minimum positive clock pulse width=2.Sketch the clock, data input and data output waveforms showing these timing relationship.
6. A 4-bit binary synchronous counter uses Flip-flops with propagation delay time of 25ns each. The maximum possible time required for change state will be ----------.
7. A 4-bit pre-settable up-counter has preset input 0101.The preset operation takes place as soon as the counter becomes maximum i.e 1111.The modulus of this counter-------.
8. Convert D Flip-flop to JK Flip-flop
9. Convert T Flip-flop to D Flip-flop

Result: