Laboratory Report Cover Sheet

SRM Institute of Science and Technology Faculty of Engineering and Technology Department of Electronics and Communication Engineering
15EC203J Digital Systems **Third Semester, 2018-19 (odd semester)**

Name :

Register No. :

Day / Session :

Venue :

Title of Experiment :

Date of Conduction :

Date of Submission :

Particulars	Max. Marks	Marks Obtained
Pre-lab questions	10	
In-lab experiment	20	
Post-lab questions	10	
Total	40	

REPORT VERIFICATION

Date :

Staff Name :

Signature :

Lab 9: Design of 4-bit Ripple Counters and MOD-10 counters

4 BIT RIPPLE COUNTERS

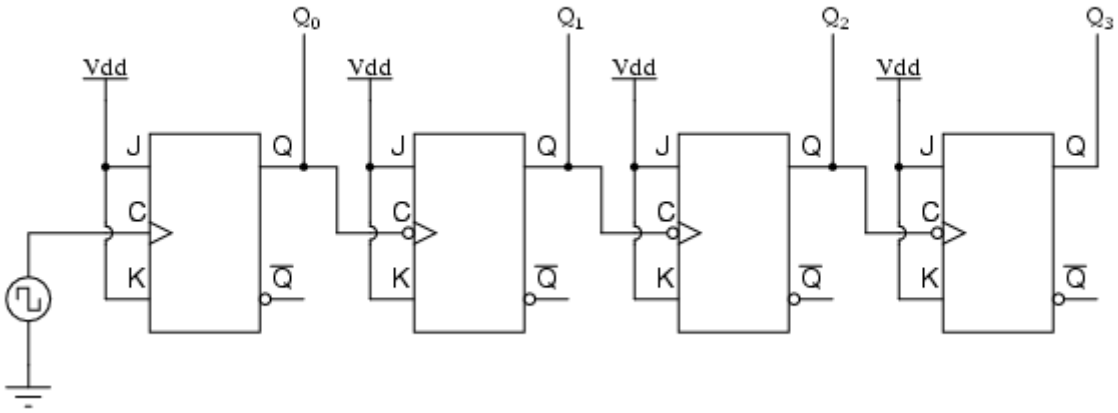

Figure 8.1: 4-bit Asynchronous Counter

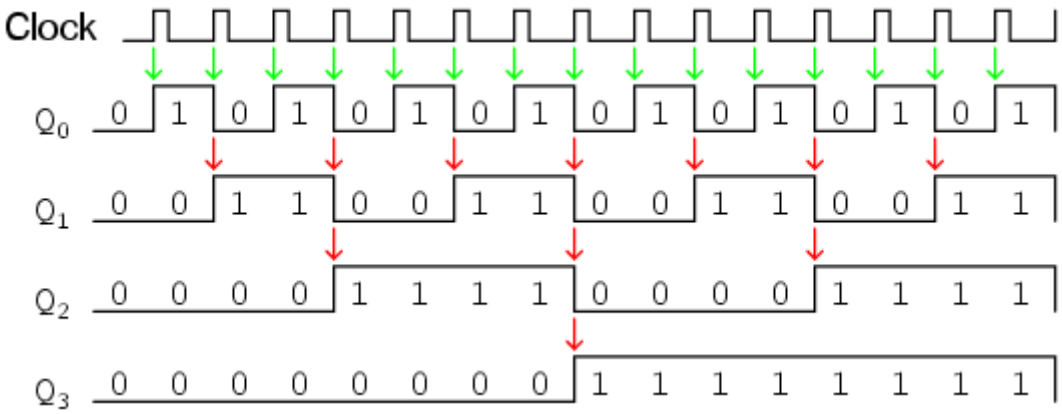

Figure 8.2: Count Sequence

Lab 9: Design of 4-bit Ripple Counters and MOD-10 counters

Aim

To design and verify the timing diagram of 4 bit Ripple Counter

Hardware Requirement

a. Equipments	- Digital IC Trainer Kit
b. Discrete Components	- IC7473 Dual JK Flip-flop
	IC 7400 NAND Gate

Theory

Asynchronous Counter is sequential circuit that is used to count the number of clock input signal. The output of one flip flop is given as a clock input to another flip-flop, so it is called as Serial Counter. A ripple counter is an asynchronous counter where only the first flip-flop is clocked by an external clock. All subsequent flip-flops are clocked by the output of the preceding flip-flop. Asynchronous counters are also called ripple-counters because of the way the clock pulse ripples it way through the flip-flops.

The MOD of the ripple counter or asynchronous counter is 2^n if n flip-flops are used. A three-bit asynchronous counter is shown on the below figure. The external clock is connected to the clock input of the first flip-flop (FF0) only. So, FF0 changes state at the falling edge of each clock pulse, but FF1 changes only when triggered by the falling edge of the Q output of FF0 similarly FF2 changes only when triggered by the falling edge of the Q output of FF1. Because of the inherent propagation delay through a flip-flop, the transition of the input clock pulse and a transition of the Q output of FF0 can never occur at exactly the same time. Therefore, the flip-flops cannot be triggered simultaneously, producing an asynchronous operation. Usually, all the CLEAR inputs are connected together, so that a single pulse can clear all the flip-flops before counting starts. The clock pulse fed into FF0 is rippled through the other counters after propagation delays, like a ripple on water, hence the name Ripple Counter.

Mod 10 Counters

Circuits for counting events are frequently used in computers and other digital systems. Since a counter circuit must remember its past states, it has to possess memory. The number of flip flops used and how they are connected determine the number of states and the sequence of the states that the counter goes through in each complete cycle.

Counters can be classified into two broad categories according to the way they are clocked:

1. Asynchronous (Ripple) Counters - the first flip-flop is clocked by the external clock pulse, and then each successive flip -flop is clocked by the Q or Q' output of the previous flip -flop.
2. Synchronous Counters - all memory elements are simultaneously triggered by the same clock.

A mod N counter is a counter that has N states. Its output frequency is f/N. A counter which is reset at the tenth clock pulse is called Mod 10 counter or Divide by 10 counter. The circuit diagram of Mod 10 counter is shown in the figure. This counter contains three JKMS flip-flop.

A 3 bit binary counter is normally counting from 000 to 111. The actual output of a 3 bit binary counter at the tenth clock pulse is 1010. A two input NAND gate is used to make a Mod 10 counter. The outputs Q_B and Q_D are connected to the input of the give NAND gate,

MOD 10 ASYNCHRONOUS COUNTER

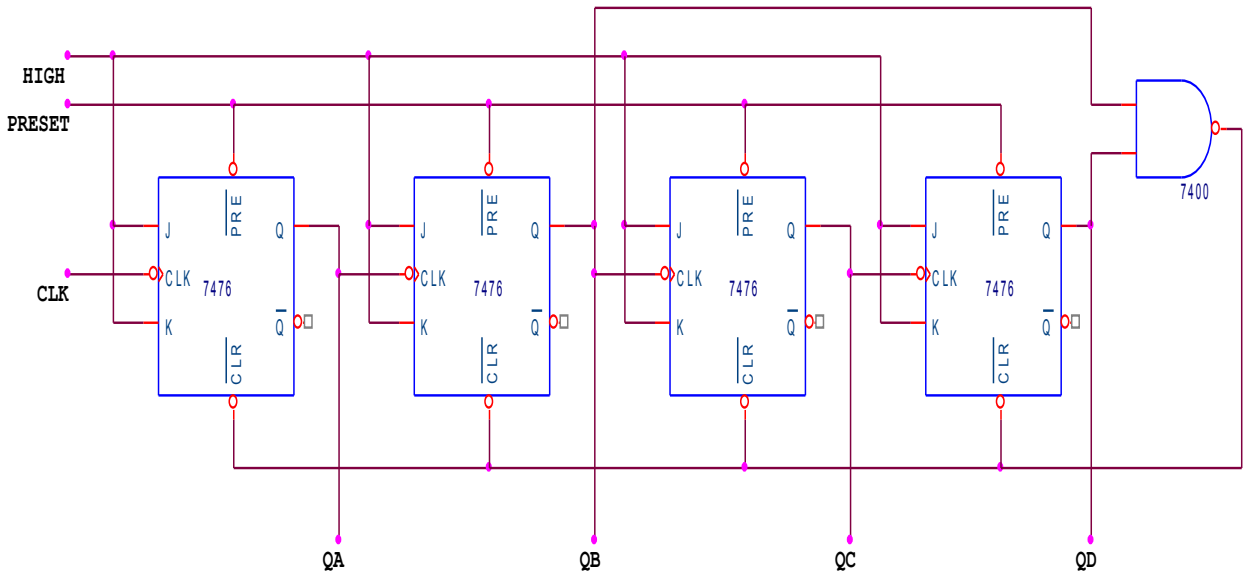

Figure 8.3: Mod 10 Asynchronous Counter

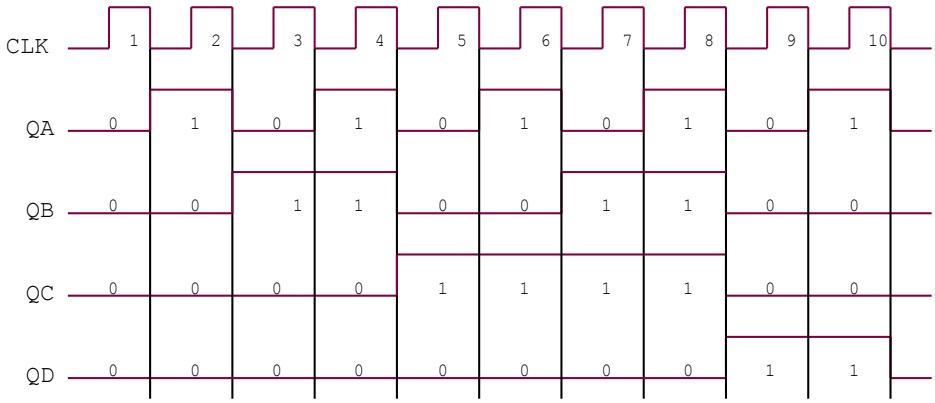

Figure 8.4: Timing Diagram

and its output is connected to the RESET terminal of the counter. Hence, the counter is reset at the tenth clock pulse, which produces the output Q_D, Q_C, Q_B, Q_A as 0000.

Pre lab questions

1. What do you mean by Glitch?
2. How many flip-flops are required to produce a divide-by-64 device?
3. Why Asynchronous counter is called as Ripple Counter?
4. What do you mean by synchronous reset and asynchronous reset?
5. What is the use of Preset input?
6. What is use of Ring and Johnson's Counter?
7. Which flip-flop is suitable for counter? Why?
8. Draw the timing diagrams for mod 6 counter.

Lab Procedure

1. Connections are made as per circuit diagram.
2. Clock pulses are applied one by one at the clock I/P and the O/P is observed at Q_A, Q_B & Q_C, Q_D.

Post lab questions

1. Design a 4-bit frequency divider.
2. Design a sequential circuit that is used to generate the timing signals with a combination of Shift register and a decoder.
3. What is state table?
4. How many states a 6-bit ripple counter can have?
5. A 4-bit binary ripple counter uses Flip-flops with propagation delay time of 25ns each. The maximum possible time required for change state will be ----------.
6. How many Flip-flops a decade counter will require?
7. What is the maximum number that can be obtained by a ripple counter using 5 Flip-flop?
8. Draw the state Diagram, state table and Timing Diagram of a 2-bit synchronous counter.
9. Design a modulus seven synchronous counter using D flip-flop.
10. A mod-5 synchronous counter is designed using JK Flip-flops. What is the number of counts it will skip?
11. The output frequency of a Modulus-16 counter, clocked from a 20kHz clock input signal is----------.

Result: