Lab 8: Characteristic table verification of flip-flops.

FLIP FLOP

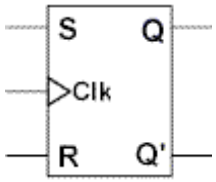
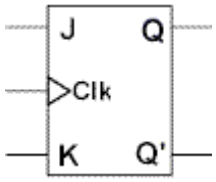
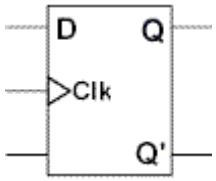
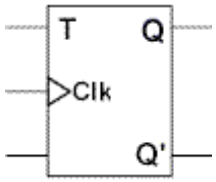
Flip-Flop Name	Flip-Flop Symbol	Characteristic Table	Characteristic Equation	Excitation Table
SR		S R Q(next) 0 0 Q 0 1 0 1 0 1 1 1 ?	Q(next) = S + R'Q SR = 0	Q Q(next) S R 0 0 0 X 0 1 1 0 1 0 0 1 1 1 X 0
JK		J K Q(next) 0 0 Q 0 1 0 1 0 1 1 1 Q'	Q(next) = JQ' + K'Q	Q Q(next) J K 0 0 0 X 0 1 1 X 1 0 X 1 1 1 X 0
D		D Q(next) 0 0 1 1	Q(next) = D	Q Q(next) D 0 0 0 0 1 1 1 0 0 1 1 1
T		T Q(next) 0 Q 1 Q'	Q(next) = TQ' + T'Q	Q Q(next) T 0 0 0 0 1 1 1 0 1 1 1 0

Table 7.1 Flip-flops and their properties

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Aim

To familiarize with circuit implementations using ICs and test the behavior of different Flip-flops.

Hardware Requirement

a. Equipments - Digital IC Trainer Kit
b. Discrete Components - 74LS73 JK-Flip flop
74LS74 D Flip flop

Theory:

Digital electronic circuit is classified into combinational logic and sequential logic. Combinational logic output depends on the inputs levels, whereas sequential logic output depends on stored levels and also the input levels.

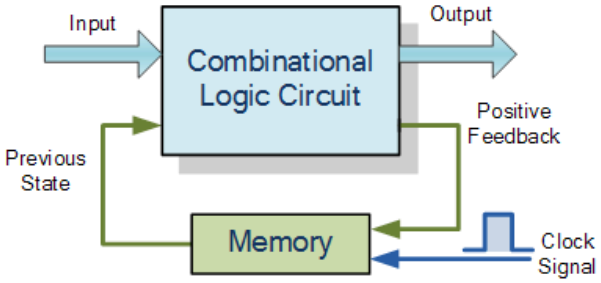


Figure 7.1: Sequential logic representation

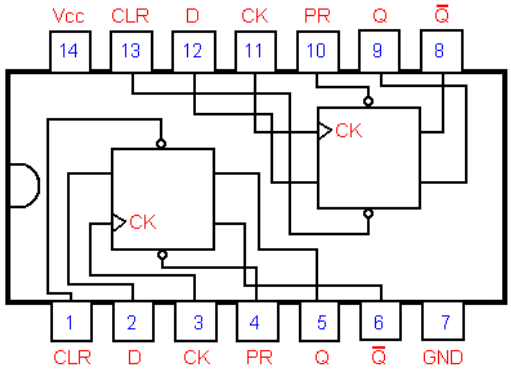
The storage elements (Flip -flops) are devices capable of storing 1-bit binary info. The binary info stored in the memory elements at any given time defines the state of the Sequential circuit. The input and the present state of the memory element determines the output. Storage elements next state is also a function of external inputs and present state.

Flip-Flops and their properties

Flip-flops are synchronous bistable devices. The term synchronous means the output changes state only when the clock input is triggered. That is, changes in the output occur in synchronization with the clock. A flip-flop circuit has two outputs, one for the normal value and one for the complement value of the stored bit. Since memory elements in sequential circuits are usually flip-flops, it is worth summarizing the behavior of various flip-flop types before proceeding further. All flip -flops can be divided into four basic types: **SR**, **JK**, **D** and **T**. They differ in the number of inputs and in the response invoked by different value of input signals. The four types of flip -flops are defined in the Table 7.1.

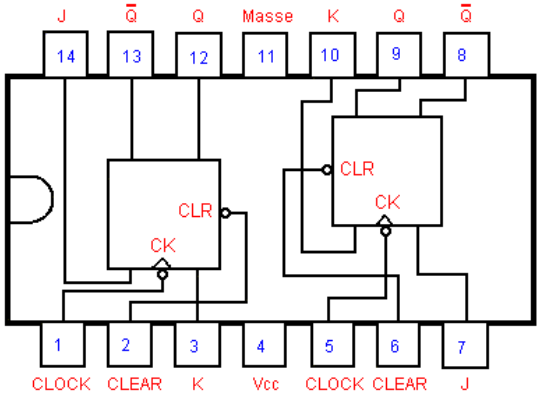
The ***characteristic table*** in the third column of Table 7.1 defines the state of each flip-flop as a function of its inputs and previous state. **Q** refers to the present state and **Q(next)** refers to the next state after the occurrence of the clock pulse**.**

FLIP FLOP PIN DIAGRAM:



PRESET	CLEAR	CLOCK	D	Q	$\bar{Q}$
0	1	X	X	1	0
1	0	X	X	0	1
0	0	X	X	1	1
1	1	↑	1	1	0
1	1	↑	0	0	1
1	1	0	X	Q0	$\bar{Q}$0
1	1	1	X	Q0	$\bar{Q}$0

Figure 7.2: IC7474 D Flip-flop connection diagram



CLEAR	CLOCK	J	K	Q	$\bar{Q}$
0	X	X	X	0	1
1	↓	0	0	Q0	$\bar{Q}$0
1	↓	1	0	1	0
1	↓	0	1	0	1
1	↓	1	1	TOGGLE	
1	1	X	X	Q0	$\bar{Q}$0
1	0	X	X	Q0	$\bar{Q}$0

Figure 7.3: IC7473 J-K Flip-flop connection diagram

Pre lab Questions

1. What is Flip flop?

2.How is a J-K flip –flop made to to toggle?

a)J=0,K=0 b)J=1,K=0 C) J=0,K=1 d)J=1,K=1

3.How many flip-flops are in the 7474 IC----------

4.What is one disadvantage of an S-R flip-flops?

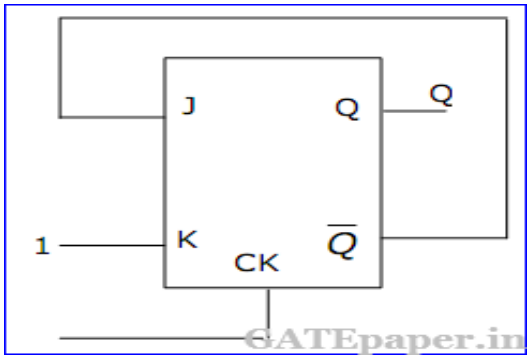
5.An S-R flip-flop can be converted into a T-flip flop by connecting ---------to Q bar and ---------- Q.

Lab Procedure

1. Refer datasheet for the input and output pin numbers of the IC.
2. Connect the particular input pins to the logic input section using a connecting wire.
3. Similarly connect the output pin to the logic output section of the trainer kit.
4. Verify the functionality of ,JK Flip flop and D Flip flop.
5. Write the truth-table for each.

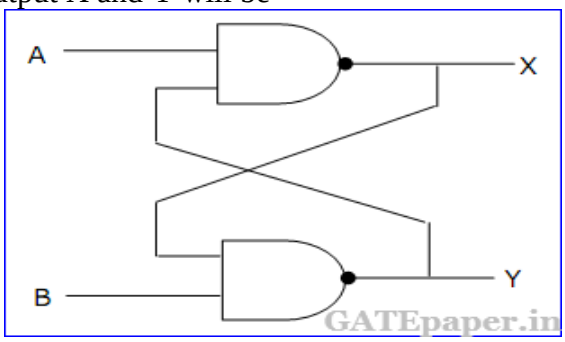
Post lab Questions

1. What is the Difference between Combinational circuits and Flip-flop?
2. In a JK flip flop, we have J = Q' and K = 1. Assume the flip flop was initially cleared and then clocked for 6 pulses, the sequence at the Q output will be



a. 010000 b. 011001 c. 010010 d. 010101

3. In the figure shown is A = 1 and B = 1, the input B is now replaced with a sequence 101010....., the output X and Y will be



a. Fixed at 0 and 1 respectively b. X = 1010... while Y = 0101....
c. X = 1010.... and Y = 1010.... d. Fixed at 1 and 0 respectively

4. The present output Q_n of an edge triggered JK flip-flop is logic '0'. If j = 1, then Q_{n+1} is--------
5. what are the applications of flip-flop?

Result: