SRM Institute of Science and Technology
College of Engineering and Technology

SET A

DEPARTMENT OF ECE

SRM Nagar, Kattankulathur – 603203, Chengalpattu District, Tamilnadu

Academic Year: 2021-2022 (EVEN)

Test: CLAT-1 **Date: 08.04.2022**
Course Code & Title: 18ECE206J Advanced Digital System Design **Duration:** 60 Minutes
Year & Sem: II & IV **Max. Marks:** 25

Course Articulation Matrix:

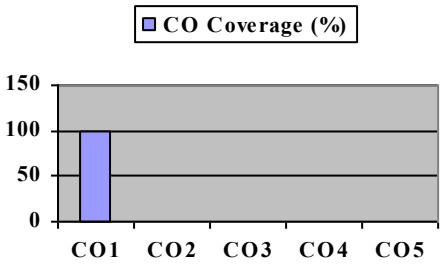
18ECE206J / Advanced Digital System Design		Program Outcomes (POs)														
		Graduate Attributes												Program Specific Outcomes (PSO)		
S. No.	**Course Outcomes (CO):**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**1**	**2**	**3**
1	Apply advanced theorems to simplify the design aspects of various practical circuits	2	-	2	-	-	-	-	-	-	-	-	-	-	-	-
2	Analyze synchronous sequential circuits and write VHDL Code	-	2	2	-	-	-	-	-	-	-	-	-	-	-	-
3	Analyze Asynchronous sequential circuits and construct circuit using VHDL	-	2	2	-	-	-	-	-	-	-	-	-	-	-	-
4	Implement various digital circuits using Programmable Logic Devices	-	2	2	-	-	-	-	-	-	-	-	-	-	-	-
5	Demonstrate FPGAs and Construct digital circuits using VHDL.	-	3	3	-	3	-	-	-	-	-	-	-	-	-	2
6	Perform experiments in the laboratory with hardware and software to simulate and verify the design	-	-	-	-	3	-	-	-	2	-	-	3	3	-	2

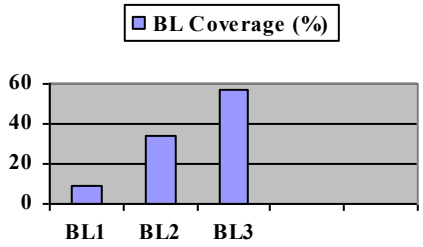
Part - A
(5 x 1 = 5 Marks)
Answer all

Q. No	Question	Marks	BL	CO	PO	PI Code
1	For Minimizing Multiple Output Logic Circuits, to use (a) Shannon's theorem (b) K-Map (c) Consensus theorem (d) Reed Muller Expansion	**1**	**1**	**1**	**1,3**	**1.1.1** **3.1.1**
2	How many states and flip flops required for Moore model of the given sequence "101011"? (a) 6,3 (b) 7,3 (c) 7,7 (d) 6,6	**1**	**2**	**1**	**1,3**	**1.1.1** **3.1.1**
3	Which among the following constraint/s is/are involved in a state-machine description? (a) State variable & clock (b) State transitions & output specifications	**1**	**1**	**1**	**1,3**	**1.1.1** **3.1.1**

	(c) Reset condition (d) a,b and c					
4	The elements used in the State diagram are (a) Transition (b) Condition (c) Iteration (d) Optional	**1**	**1**	**1**	**1,3**	**1.1.1** **3.1.1**
5	One of the Reed muller rule A+B=? (a) A⊕ B⊕AB (b) A'⊕ B⊕AB (c) A⊕ A'B (d) Both (a) and (c)	**1**	**2**	**1**	**1,3**	**1.1.1** **3.1.1**
Part – B (2 x 10 = 20 Marks) **Answer any two**						
6	Design a circuit to detect the sequence pattern "1110" using Mealy Non overlapping and D flip flop.	**10**	**3**	**1**	**1,3**	**1.1.1** **3.1.1**
7	Design a sequential circuit for the following state using T flip flop. 0-1-2-3-4-5-6-7-0	**10**	**3**	**1**	**1,3**	**1.1.1** **3.1.1**
8	(i) Implement full adder using 4 to 1 MUX (ii) What is Reed Muller expansion theorem? Expand the following expression using it and draw the circuit diagram F=A'B' + AB	**5** **5**	**2**	**1**	**1,3**	**1.1.1** **3.1.1**

Course Outcome (CO) and Bloom's level (BL) Coverage in Questions





Evaluation Sheet

Name of the Student:
Register No.:

Part- A (5x 1= 5 Marks)			
Q. No	**CO**	**Marks Obtained**	**Total**
1	**1**		
2	**1**		
3	**1**		
4	**1**		
5	**1**		
Part- B (2 x 10= 20 Marks)			
6	**1**		
7	**1**		
8	**1**		

Consolidated Marks:

CO	Marks Scored
CO1	
Total	

Approved by the Course Coordinator

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SET B

DEPARTMENT OF ECE

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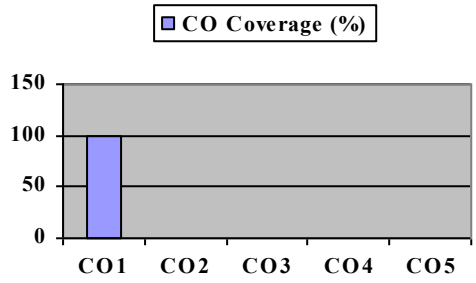
S. No.	Course Outcomes (CO):	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
1	Apply advanced theorems to simplify the design aspects of various practical circuits	2	-	2	-	-	-	-	-	-	-	-	-	-	-	-
2	Analyze synchronous sequential circuits and write VHDL Code	-	2	2	-	-	-	-	-	-	-	-	-	-	-	-
3	Analyze Asynchronous sequential circuits and construct circuit using VHDL	-	2	2	-	-	-	-	-	-	-	-	-	-	-	-
4	Implement various digital circuits using Programmable Logic Devices	-	2	2	-	-	-	-	-	-	-	-	-	-	-	-
5	Demonstrate FPGAs and Construct digital circuits using VHDL.	-	3	3	-	3	-	-	-	-	-	-	-	-	-	2
6	Perform experiments in the laboratory with hardware and software to simulate and verify the design	-	-	-	-	3	-	-	-	2	-	-	3	3	-	2

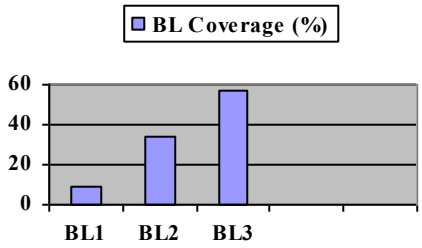
Part - A
(5 x 1 = 5 Marks)
Answer all

Q. No	Question	Marks	BL	CO	PO	PI Code
1	Which theorem is used for eliminating the complement term? (a) Shannon's (b) Reed Muller (c) Consensus (d) De Margon's	1	1	1	1,3	1.1.1 3.1.1
2	How many states and flip flop required for Mealey model of the given sequence "10011" (a) 5,3 (b) 5,5 (c) 6,3 (d) 6,5	1	2	1	1,3	1.1.1 3.1.1
3	A 2 to 1 MUX can be used to realize which of the following (a) only AND,NOT (b) only OR (c) only NOT	1	1	1	1,3	1.1.1 3.1.1

	(d) AND,OR ,NOT					
4	In a sequence detector, if the required bit is at its input while checking the sequence bit by bit, the detector moves to _____ (a) Previous state (b) Next state (c) Remains in the same state (present state) (d) Null state	**1**	**1**	**1**	**1,3**	**1.1.1** **3.1.1**
5	A⊕ B⊕BA ⊕B⊕=? (a) A⊕ AB (b) A (c) A⊕ B (d) B	**1**	**2**	**1**	**1,3**	**1.1.1** **3.1.1**
	Part – B (2 x 10 = 20 Marks) **Instructions: Answer any two**					
6	Design a circuit to detect the sequence pattern "1110" using Moore Non overlapping and D flip flop.	**10**	**3**	**1**	**1,3**	**1.1.1** **3.1.1**
7	Design a sequential circuit for the following state using T flip flop. 7-6-5-4-3-2-1-0-7	**10**	**3**	**1**	**1,3**	**1.1.1** **3.1.1**
8	(i)Simplified the following expressing using Reed Muller expansion and draw the circuit. F (A, B, C) =∑ (1,3,5,6) (ii) Implement full subtractor using 4 to 1 MUX	**5** **5**	**2**	**1**	**1,3**	**1.1.1** **3.1.1**

Course Outcome (CO) and Bloom's level (BL) Coverage in Questions





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Q. No	**CO**	**Marks Obtained**	**Total**
1	**1**		
2	**1**		
3	**1**		
4	**1**		
5	**1**		
Part- B (2 x 10= 20 Marks)			
6	**1**		
7	**1**		
8	**1**		

Consolidated Marks:

CO	Marks Scored
CO1	
Total	

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