SRM Institute of Science and Technology
College of Engineering and Technology

SET A

DEPARTMENT OF ECE

SRM Nagar, Kattankulathur – 603203, Chengalpattu District, Tamilnadu

Academic Year: 2021-2022 (EVEN)

Answer key

Test: CLAT-III **Date: 21.06.2022**
Course Code & Title: 18ECE206J Advanced Digital System Design **Duration:** 100 Min.
Year & Sem: II & IV **Max. Marks:** 50

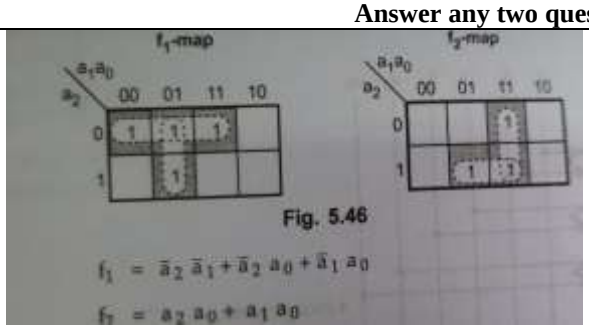
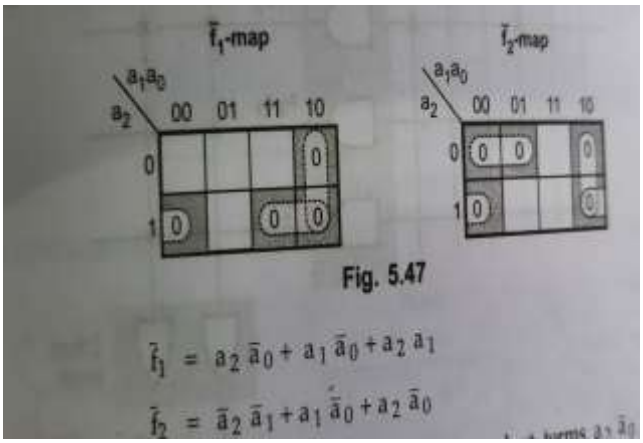
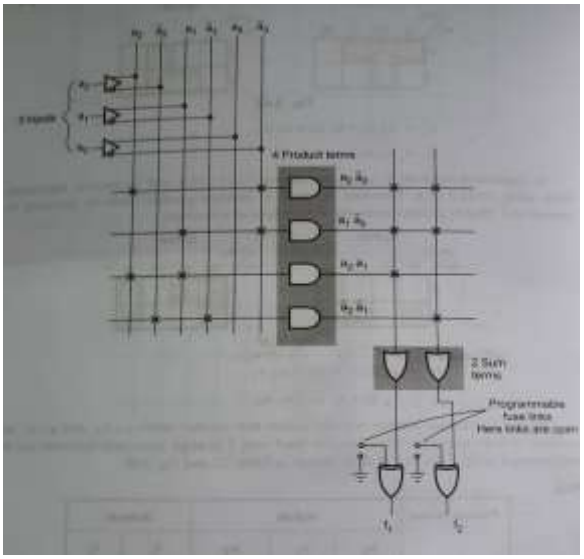
Course Articulation Matrix:

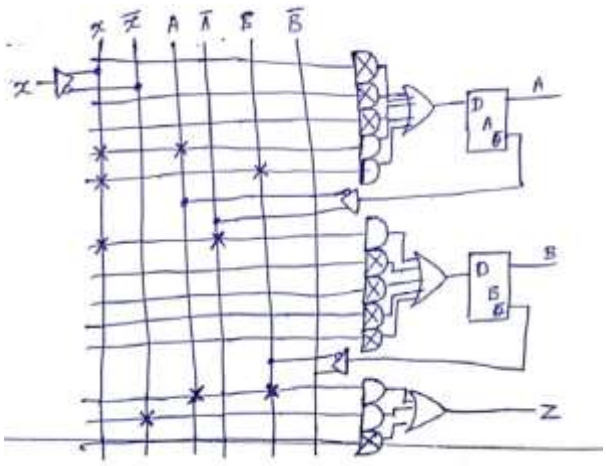
18ECE206J / Advanced Digital System Design		Program Outcomes (POs)														
		Graduate Attributes												Program Specific Outcomes (PSO)		
S.No.	**Course Outcomes (CO):**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**1**	**2**	**3**
1	Apply advanced theorems to simplify the design aspects of various practical circuits and design Mealy and Moore models of sequential circuit.	2	-	2	-	-	-	-	-	-	-	-	-	-	-	-
2	Implement synchronous sequential circuits and write VHDL Code	-	2	2	-	-	-	-	-	-	-	-	-	-	-	-
3	Analyze asynchronous sequential circuits and write code using VHDL.	-	2	2	-	-	-	-	-	-	-	-	-	-	-	-
4	Implement Hazard free circuits and various digital circuits using Programmable Logic Devices.	-	2	2	-	-	-	-	-	-	-	-	-	-	-	-
5	Demonstrate FPGAs and Construct digital circuits using VHDL.	-	3	3	-	-	-	-	-	-	-	-	-	-	-	2
6	Design and verify the experiments in the laboratory with hardware and software.		-	-	-	3	-	-	-	2	-	-	3	3	-	2

Part - A
(10 x 1 = 10 Marks)
Answer all Questions

Q. No	Question	Mark	BL	CO	PO	PI Code
1	The input to a PLD is _____ gate. A. AND B. OR C. XOR D. XNOR	**1**	**1**	**4**	**2**	**2.2.1**
2	PAL consists of _____ AND gates and _____ OR gates. A.fixed, Programmable B. Programmable, fixed C. programmable, programmable D. fixed, fixed	**1**	**1**	**4**	**2**	**2.2.1**
3	FPGA refers to _____ A. Field Programmable Gate Array	**1**	**1**	**4**	**2**	**2.2.1**

	B. Field Program Gate Array C. First Programmable Gate Array D. First Programmed Gate Array					
4	Which is used in PAL for reducing the loading on inputs? A. Output buffers B. OR Matrix C. Input buffers D. Latch	**1**	**2**	**4**	**3**	**3.2.2**
5	Which one of the following is the best way to detect hazards in circuit? A. K-map B. Boolean expansion C. Reed-muller expansion D. logical reduction technique	**1**	**1**	**4**	**2**	**2.2.1**
6	How does a layout of FPGA look? A. Matrix B. Rubik C. Square D. Net list	**1**	**1**	**5**	**3**	**3.2.3**
7	1:entity and1 is 2:port(A,B : in std_logic; Y : out std_logic); 3:end and1; 4:architecture andlogic of and1 is 5:begin 6:Y <= A AND B; 7:end and1; Find the syntax error in the above code. A. No error B. Line 7 “and1” should be “andlogic” C. It is a two input and gate line 1,3,7 it should be “and2” D. “;” is missing in line 5	**1**	**2**	**5**	**3**	**3.2.3**
8	Port map is used in _____ modelling A. behavioural B. structural C. data flow D. circuit level	**1**	**2**	**5**	**3**	**3.2.3**
9	How many logic inputs are available in Xilinx 3000 FPGA? A.5 B.6 C.7 D.4	**1**	**1**	**5**	**2**	**2.2.2**
10	If a and b are two STD_LOGIC_VECTOR input signals, then legal assignment for a and b is? A. x<= a.b B. x<= a or b C. x<= a+b D. x<= a&&b	**1**	**2**	**5**	**3**	**3.2.3**

	Section B1 (2 x 10 = 20 Marks) **Answer any two questions**					
11	 (2Marks)  (2Marks) Table (2Marks)  (4Marks)	**10**	**3**	**4**	**2**	**2.2.1**

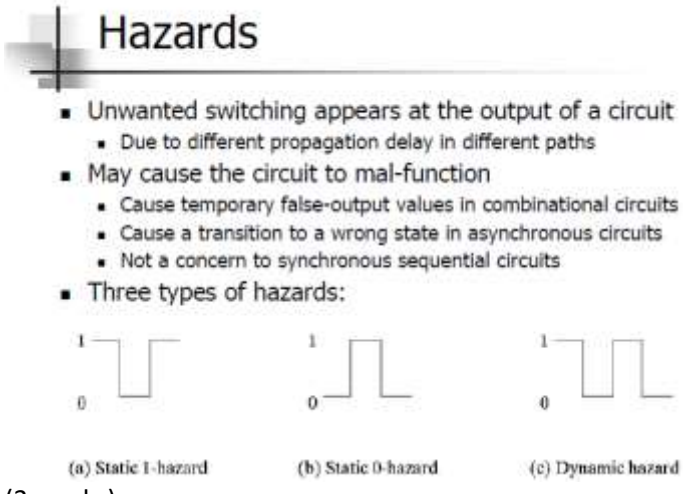
<table>
<tr>
<td>12</td>
<td>(i)
 
(7 marks)
(ii)
Explanation with example ICs
The PAL16R8 is representative of the first generation of sequential PLDs, which used bipolar (TTL) technology. This device has eight primary inputs, eight outputs, and common clock and output-enable inputs, and fits in a 20 pin package.
<table>
<tr><th rowspan="2">Part number</th><th rowspan="2">Package pins</th><th rowspan="2">AND-gate inputs</th><th colspan="3">Inputs to AND array</th></tr>
<tr><th>Primary inputs</th><th>Bidirectional combinational outputs</th><th>Registered outputs</th><th>Combinational outputs</th></tr>
<tr><td>PAL16L8</td><td>20</td><td>16</td><td>10</td><td>6</td><td>0</td><td>2</td></tr>
<tr><td>PAL16R4</td><td>20</td><td>16</td><td>8</td><td>4</td><td>4</td><td>0</td></tr>
<tr><td>PAL16R6</td><td>20</td><td>16</td><td>8</td><td>2</td><td>6</td><td>0</td></tr>
<tr><td>PAL16R8</td><td>20</td><td>16</td><td>8</td><td>0</td><td>8</td><td>0</td></tr>
<tr><td>PAL20L8</td><td>24</td><td>20</td><td>14</td><td>6</td><td>0</td><td>2</td></tr>
<tr><td>PAL20R4</td><td>24</td><td>20</td><td>12</td><td>4</td><td>4</td><td>0</td></tr>
<tr><td>PAL20R6</td><td>24</td><td>20</td><td>12</td><td>2</td><td>6</td><td>0</td></tr>
<tr><td>PAL20R8</td><td>24</td><td>20</td><td>12</td><td>0</td><td>8</td><td>0</td></tr>
</table>
(3 marks)</td>
<td>7

3</td>
<td>3

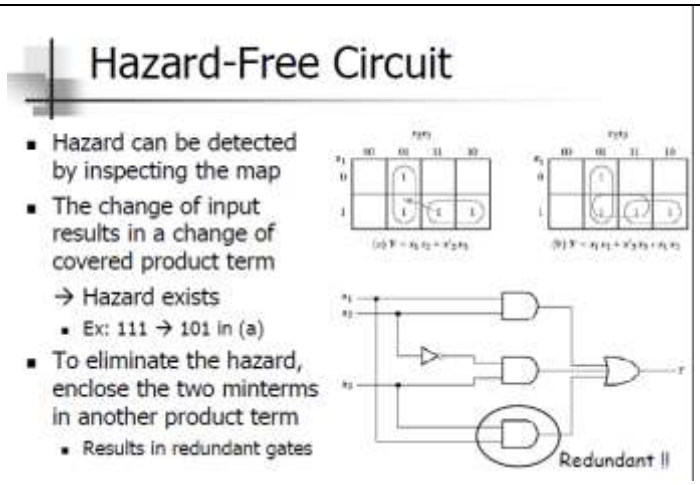
2</td>
<td>4

4</td>
<td>3

3</td>
<td>3.2.2

3.2.2</td>
</tr>
<tr>
<td>13</td>
<td> 

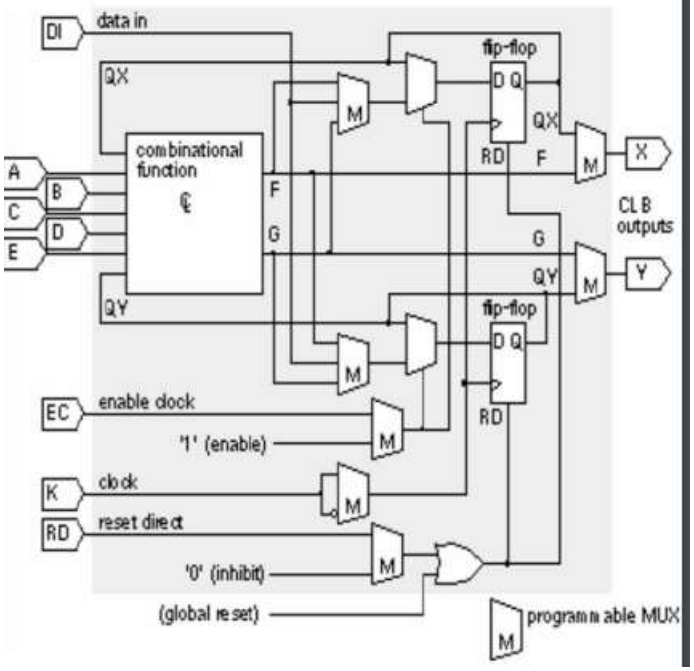
(3 marks)</td>
<td>10</td>
<td>3</td>
<td>4</td>
<td>2</td>
<td>2.2.1</td>
</tr>
</table>



(3 marks)
types explanation (each 1 marks= 4marks)

Section B2 (2 x 10 = 20 Marks)
Answer any two questions

14



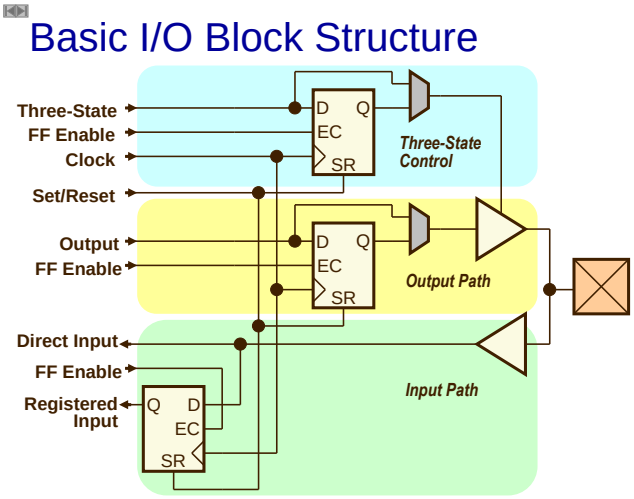
10	**3**	**5**	**3**	**3.2.3**

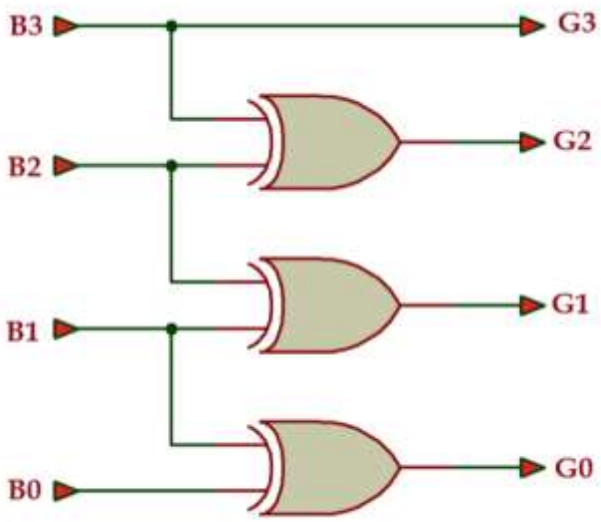
(6 marks)

Explanation (4 marks)

- A 32-bit look-up table (LUT)
- CLB propagation delay is fixed (the LUT access time) and independent of the logic function
- 7 inputs to the XC3000 CLB:
  - 5 CLB inputs (A–E), and
  - 2 flip-flop outputs (QX and QY)
- 2 outputs from the LUT (F and G).
- Since a 32-bit LUT requires only five variables to form a unique address ($32 = 2^5$), there are multiple

	ways to use the LUT • Use 5 of the 7 possible inputs (A–E, QX, QY) with the entire 32-bit LUT • Split the 32-bit LUT in half to implement 2 functions of 4 variables each					

15	(i)
	 
	
	(3 marks)
	Explanation (2 marks)
	(ii)
	library IEEE;
	use IEEE.STD_LOGIC_1164.all;
	
	entity ckt is
	port(
	clk : in STD_LOGIC;
	Q0, Q1, Q2 : inout STD_LOGIC;
	);
	end ckt;
	
	architecture seq ckt of ckt is
	
	component dff is
	port(D,CLK : in std_logic; Q: out std_logic);
	end component dff;
	
	signal s : std_logic;
	
	begin
	s <= not Q0;
	u0 : dff port map (s, clk, Q2);
	u1 : dff port map (Q2, clk, Q1);
	u3 : dff port map (Q1, clk, Q0);
	
	end seq ckt;
		5
		5
			2
			4
				5
				5
					3
					3
						3.2.3
						3.2.3

16	
	(2 marks)
	library IEEE;
	use IEEE.STD_LOGIC_1164.ALL;
	entity B_G is
	Port (bin: in std_logic_vector (1 downto 0);
	gray: out std_logic_vector (3 downto 0);
	end B_G;
	architecture Behavioral_BG of B_G is
	component xor_1 is
	Port (o,p : in STD_LOGIC;
	q : out STD_LOGIC);
	end component;
	begin
	l1: xor_1 port map (bin(3), 0, gray(3));
	l2: xor_1 port map (bin(3), bin(2),gray(2));
	l3: xor_1 port map (bin(2), bin(1),gray(1));
	l4: xor_1 port map (bin(1), bin(0),gray(0));
	end Behavioral_BG; (6 marks)
	sub program – xor gate (2marks)
		10	**4**	**5**	**3**	**3.2.3**