18ECC103J- Digital Electronic Principles

Assignment - II

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ECE-A

1. Design a 4-bit magnitude comparator to compare two four-bit number.

Soln. A Comparator used to compare two binary numbers each of four bit numbers is called a 4-bit magnitude Comparator. It consists of eight inputs each for two four bit numbers and three outputs, $A<B$, $A=B$ and $A>B$.

For $A>B$, can be possible in four cases.

a) If $A_3 = 1$ and $B_3 = 0$.

b) If $A_3 = B_3$ and $A_2 = 1$ and $B_2 = 0$.

c) If $A_3 = B_3$ and $A_2 = B_2$ and $A_1 = 1$ and $B_1 = 0$.

d) If $A_3 = B_3$, $A_2 = B_2$, $A_1 = B_1$ and $A_0 = 1$ and $B_0 = 0$.

Similarly for $A<B$, there are four cases.

a) If $A_3 = 0$ and $B_3 = 1$

b) If $A_3 = B_3$, and $A_2 = 0$ and $B_2 = 1$

c) If $A_2 = B_3$, $A_2 = B_2$ and $A_1 = 0$ and $B_1 = 1$

d) If $A_3 = B_3$, $A_2 = B_2$, $A_1 = B_1$ and $A_0 = 0$ and $B_0 = 1$

The condition of $A=B$ is only possible when all the individual bits are either 1 or 0.

From the above conditions, we get.

For $A>B$;

$$F_{(A>B)} = A_3B_3' + A_2B_2' + A_1B_1' + A_0B_0'$$

For $A<B$;

$$F_{(A<B)} = A_3'B_3 + A_2'B_2 + A_1'B_1 + A_0'B_0.$$

For $A=B$;

$$F_{(A=B)} = (A_3 \odot B_3)(A_2 \odot B_2)(A_1 \odot B_1)(A_0 \odot B_0)$$

For $A > B$;

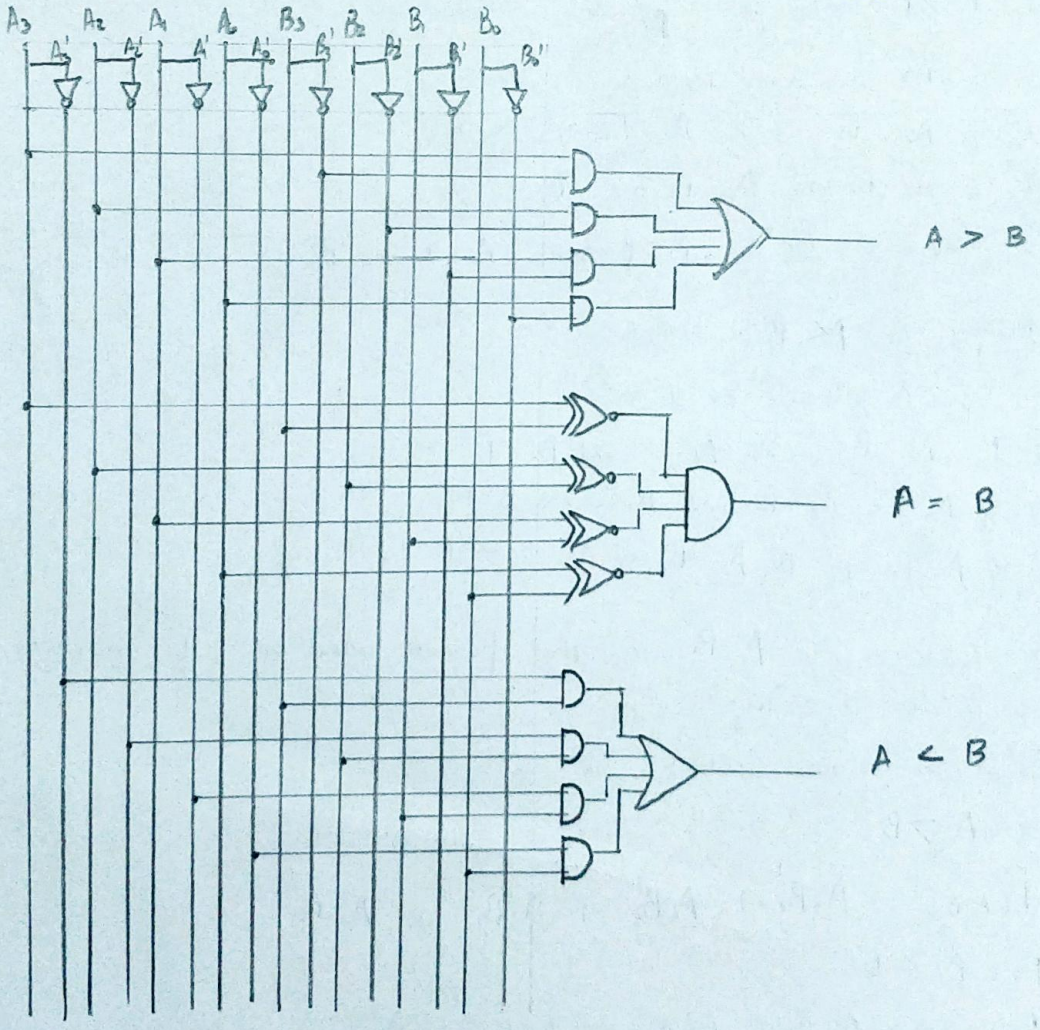
$$A>B = A_3B_3' + A_2B_2' + A_1B_1' + A_0B_0'$$

For $A < B$;

$$A<B = A_3' B_3 + A_2' B_2 + A_1' B_1 + A_0' B_0$$

For $A = B$;

$$A=B = (A_3 \odot A_3)(A_2 \odot B_2)(A_1 \odot B_1)(A_0 \odot B_0)$$

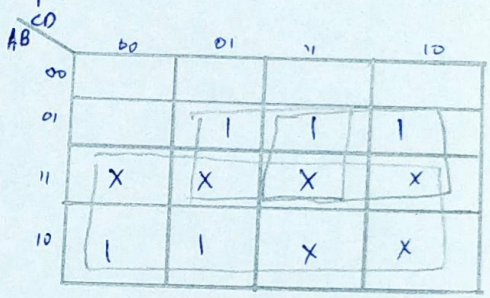


2. Construct a logic circuit for BCD to Excess - 3 Converter.

Soln. Truth Table for BCD to Excess - 3:

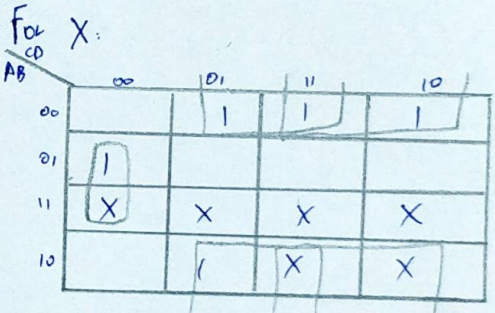
Decimal	BCD				Excess - 3			
	A	B	C	D	W	X	Y	Z
0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	1	0	0	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	0
8	1	0	0	0	1	0	1	1
9	1	0	0	1	1	1	0	0
10	X	X	X	X	X	X	X	X
11	X	X	X	X	X	X	X	X
12	X	X	X	X	X	X	X	X
13	X	X	X	X	X	X	X	X
14	X	X	X	X	X	X	X	X
15	X	X	X	X	X	X	X	X

For W:



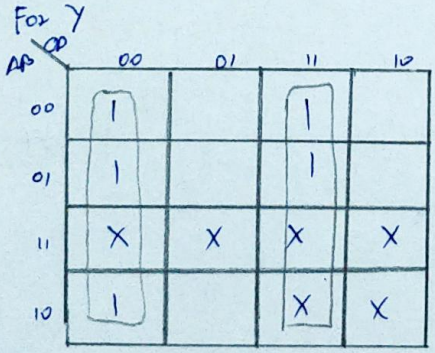
W = A + BD + BC

For X:



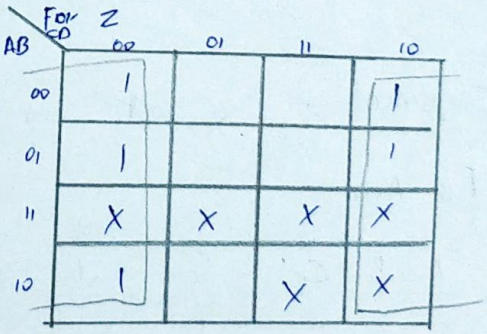
X = BC'D' + B'D + B'C

For Y



Y = C'D' + CD

For Z



Z = D'

The expressions are,

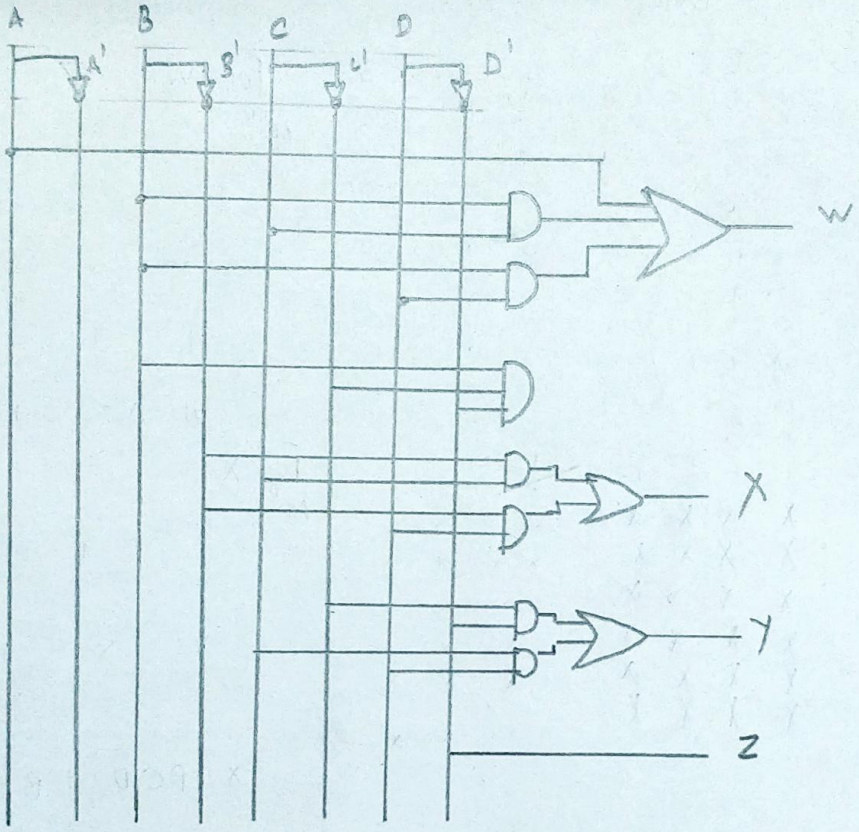
W = A + BD + BC.

X = BC'D' + B'D + B'C.

Y = C'D' + CD

Z = D'

Circuit Diagram:

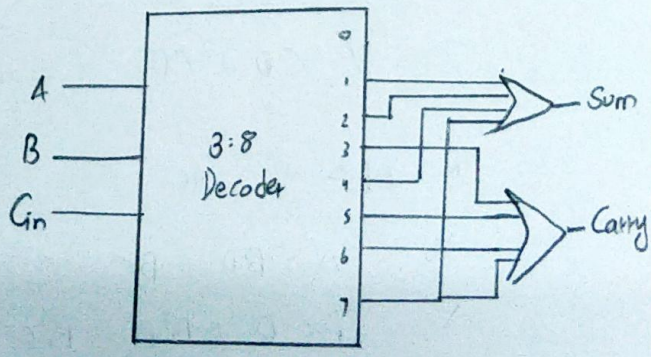


3. Implement a full adder and full subtractor using decoder.

Soln.

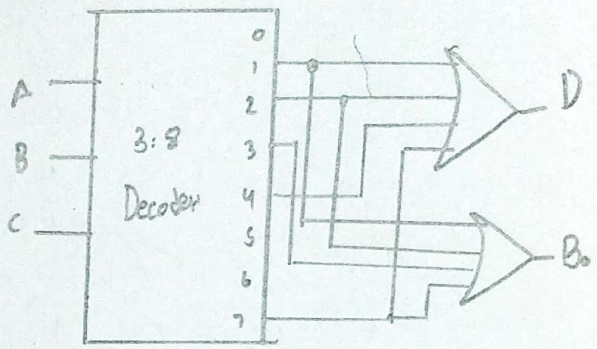
Full Adder.

A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



Full Subtractor.

A	B	Cin	D	B_o
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1



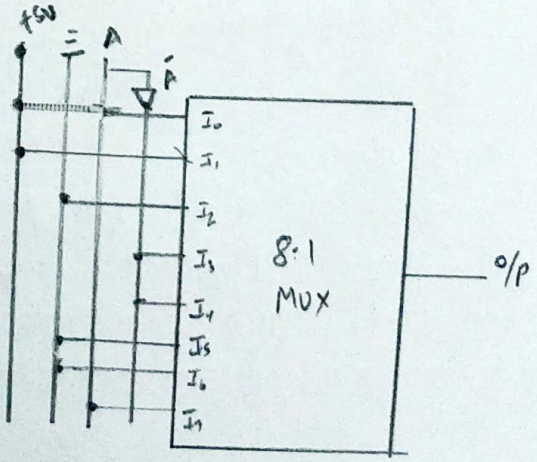
4. Implement the boolean Expression $F(A,B,C,D) = \Sigma(0,1,3,4,8,9,15)$ Using MUX.

Soln Truth Table.

Input				Output
A	B	C	D	
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
$\bar{A}$	0	1	2	3	4	5	6	7
A	8	9	10	11	12	13	14	15
	1	1	0	$\bar{A}$	$\bar{A}$	0	0	A

Appropriate 8:1 MUX



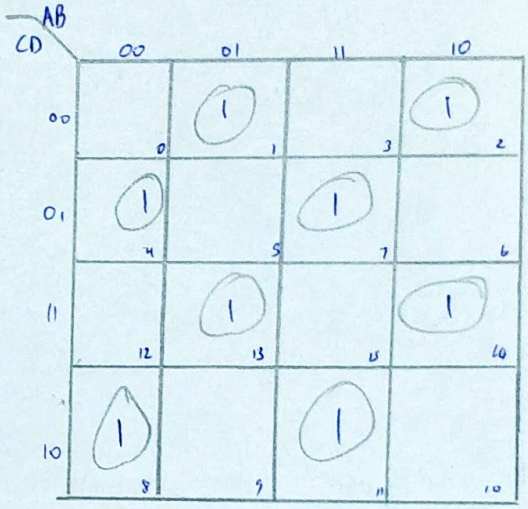
5. Design a 4-bit even parity generator and checker Circuit.

Soln

Parity Generator Truth Table

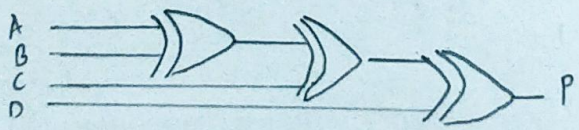
Input				Output
A	B	C	D	P
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

K-Map for P.



$P = \bar{A}\bar{B}(\bar{C}D + C\bar{D}) + \bar{A}BC\bar{D} + CD) + A\bar{B}(CD + \bar{C}\bar{D}) + A\bar{B}(CD + \bar{C}\bar{D})$

$= A \oplus B \oplus C \oplus D$



Even Parity Generator.

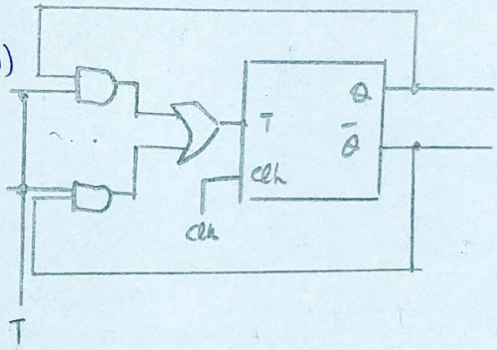
The logic for 4-bit even parity checker is similar to that of the generator. Difference being that, the Parity bit is passed as I/p with 3 bit inputs to check for error in 3 XOR Gates.

6. Construct SR flip-flop using T- flip flop.

Soln.

Inputs		Outputs		
S	R	Q	$\bar{Q}$	
0	0	0	1	(No change)
0	1	0	1	(Reset)
1	0	1	0	(Set)
1	1	X	X	(undefined)

Input	Output	
T	Q	$\bar{Q}$
0	0	1
1	1	0

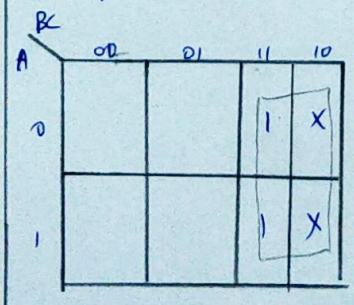


7. Design a Synchronous Counter for sequence $0 \to 1 \to 3 \to 4 \to 5 \to 7 \to 0$

Soln.

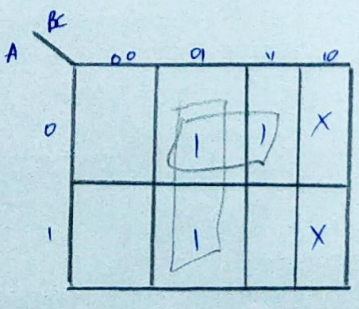
Present State			Next State			Excitation i/p		
A	B	C	A^+	B^+	C^+	T_A	T_B	T_C
0	0	0	0	0	1	0	0	1
0	0	1	0	1	1	0	1	0
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1	1

For T_A



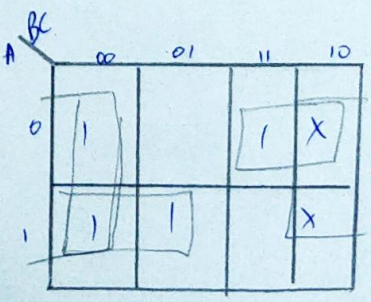
$T_A = B$

For T_B

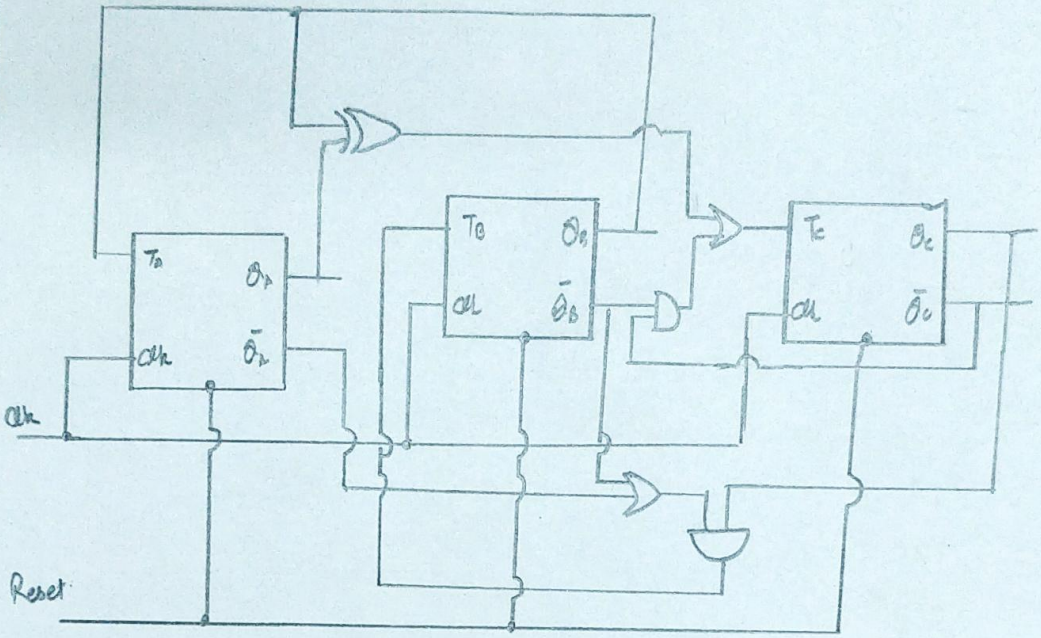


$T_B = \bar{B}C + \bar{A}C$

For T_C



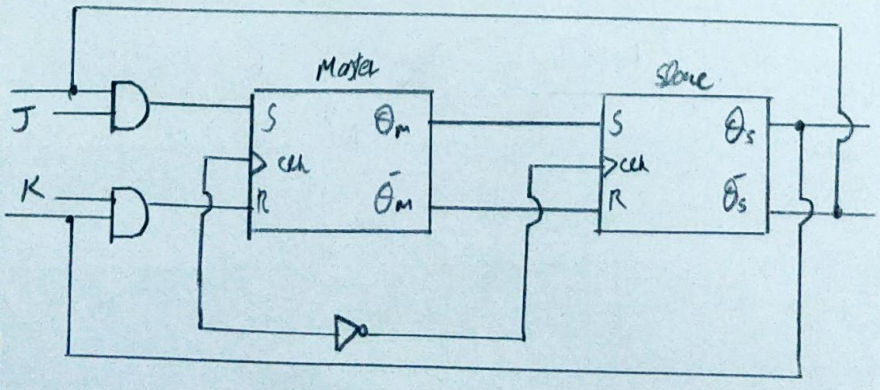
$T_C = \bar{B}\bar{C} + (A \oplus B)$

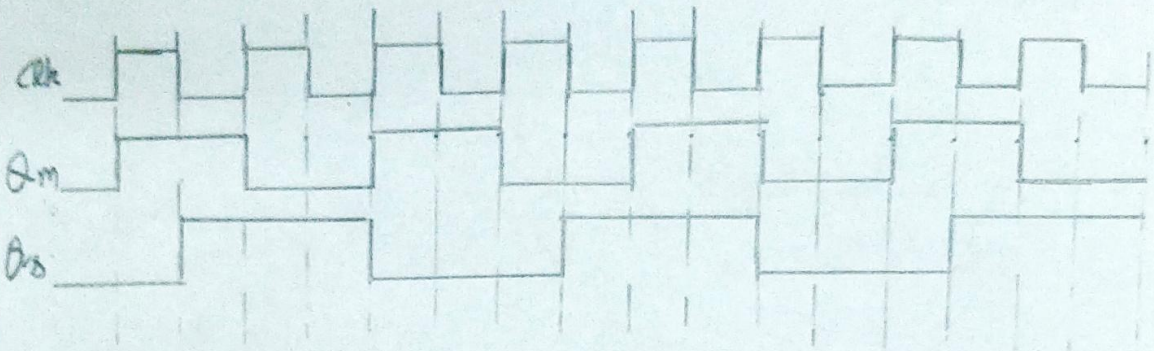


8. What is Race around Condition in JK flip flop? Explain how it is rectified and also draw the timing diagram.

Soln. For a JK flip flop, if J = K = 1, and Clk = 1, for a long time then Q output will toggle as long as Clock is high, which means the output of the flip-flop is unstable or uncertain. This is known as the race around Condition.

It is rectified using Master-Slave JK-flipflop. Here the Clock input will be 1 for a very short time. Here 2 flip flops are used of which one is called as Master and the other as Slave.

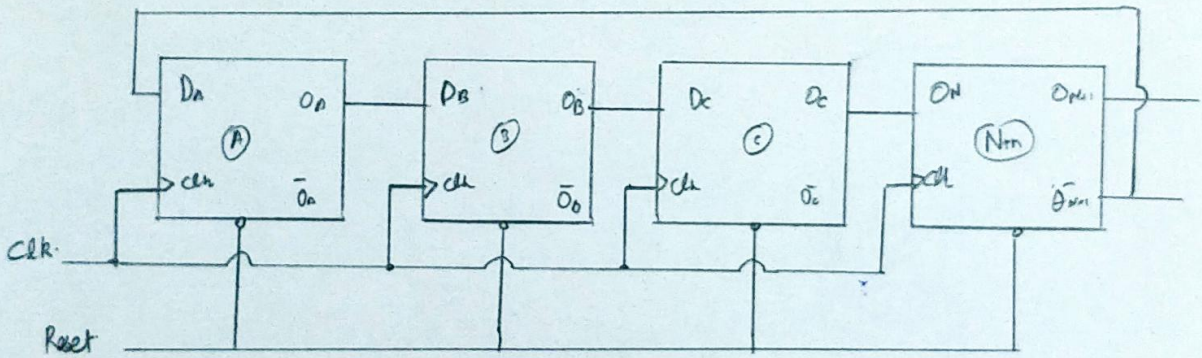




10. Explain n-bit Johnson Counter with the following

(i) Total numbe of used and unused state in n-bit Johnson Counter.

Soln n-bit Johnson Counter is a type of Counter where the Qinverted output of the last flip flop i.e, the Complemented output of the nth flip flop is Connected to the input of the first flip flop.



(a) Used State = $2n$, (b) Unused State = $(2^4 - 2n)$.

(ii) Advantages

1. The Johnson Counter Can be implemented using D and Jk Flip Flop
2. Johnson Counte is used to Count data in Continous loop.
3. It is a self decoding Circuit

(iii) Disadvantages

1. It doesnt Count in a binary sequence.
2. In this, more states remain unutilized.
3. It Can be Corrected for any number of binary sequence.

(iii) Applications.

1. It is used as a Synchronous decade Counter.
2. It is used in ASIC and FPGA designing.
3. It is used to divide the frequency of clock signal by varying their feed back.