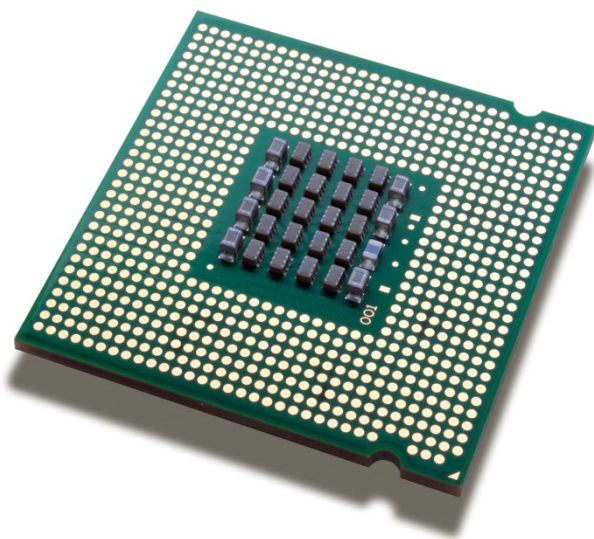
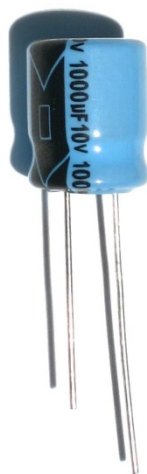


18ECC102J
ELECTRONIC
DEVICES



Syllabus

Course Code	18ECC102J	Course Name	ELECTRONIC DEVICES	Course Category	C	Professional Core			
						L	T	P	C
						3	0	2	4

Pre-requisite Courses	18EE5101J	Co-requisite Courses	Nil	Progressive Courses	18ECC201J, 18ECC202J, 18ECE203T, 18ECE303T, 18ECE3217, 18ECE3227
Course Offering Department	Electronics and Communication Engineering			Data Book / Codes/Standards	Nil

Course Learning Rationale (CLR):	The purpose of learning this course is to:
CLR-1 :	Provide a basis for understanding semiconductor material, how a pn junction is formed and its principle of operation
CLR-2 :	Explain the importance of diode in electronic circuits by presenting appropriate diode applications
CLR-3 :	Discuss the basic characteristics of several other types of diodes that are designed for specific applications
CLR-4 :	Describe the basic structure, operation and characteristics of BJT, and discuss its use as a switch and an amplifier.
CLR-5 :	Describe the basic structure, operation and characteristics of MOSFET, and discuss its use as a switch and an amplifier.
CLR-6 :	Use modern engineering tools such as PSPICE to carry out design experiments and gain experience with instruments and methods used by technicians and electronic engineers

Course Learning Outcomes (CLO):	At the end of this course, learners will be able to:
CLO-1 :	Understand the operation, characteristics, parameters and specifications of semiconductor diodes and special diodes
CLO-2 :	Demonstrate important applications of semiconductor diodes and special diodes.
CLO-3 :	Review bipolar transistor construction, operation, characteristics and parameters, as well as its application in amplification and switching.
CLO-4 :	Review field-effect transistor construction, operation, characteristics and parameters, as well as its application in amplification and switching.
CLO-5 :	Build a circuit, then make functional measurements to understand the operating characteristics of the device / circuit.
CLO-6 :	Solve specific design problem, which after completion will be verified using modern engineering tools such as PSPICE.

Learning		
1	2	3
Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)
1	90	80
2	80	75
1	90	80
1	80	75
3	80	75
3	90	75

Program Learning Outcomes (PLO)														
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Engineering Knowledge	Problem Analysis	Design & Development	Analysis, Design, Research	Modern Tool Usage	Society & Culture	Environment & Sustainability	Ethics	Individual & Team Work	Communication	Project Mgt. & Finance	Life-Long Learning	PLO-1 Professional Advancement	PLO-2 Project Management Techniques	PLO-3 Analyse & Research
H	-	-	-	-	-	-	-	-	-	-	M	-	-	-
-	-	-	-	-	-	-	-	-	-	-	M	-	-	-
H	-	-	-	-	-	-	-	-	-	-	M	-	-	-
H	-	-	-	-	-	-	-	-	-	-	M	-	L	-
-	-	-	-	H	-	-	-	-	-	-	-	L	L	-
-	-	-	-	H	-	-	L	H	M	-	M	-	-	-

Duration (hour)		Semiconductor Diodes	Diode Circuits	Special Diodes	Bipolar Junction Transistors	MOS Field-Effect Transistors
		15	15	15	15	15
S-1	SLO-1	Basic semiconductor theory: Intrinsic & extrinsic semiconductors	HWR operation, Efficiency and ripple factor	Backward diode	Physical structure	Physical structure
	SLO-2	Current flow in semiconductors	Problem solving	Varactor diode	Device operation of BJT	Device operation of E-MOSFET & D-MOSFET
S-2	SLO-1	PN junction theory: Equilibrium PN junction	Center-Tapped Transformer FWR operation, Efficiency and ripple factor	Step recovery diode	Current-Voltage characteristics of CE BJT configuration	I-V characteristics of E-MOSFET
	SLO-2	Forward biased PN junction	Problem solving	Point-contact diode	Current-Voltage characteristics of CE BJT configuration	Problem solving
S-3	SLO-1	Reverse biased PN junction	Bridge FWR operation, Efficiency and ripple factor	Metal-semiconductor junction: Structure, Energy band diagram	Current-Voltage characteristics of CB BJT configuration	Derive drain current
	SLO-2	Relation between Current and Voltage	Problem solving	Forward & Reverse Characteristics of Schottky Diode	Current-Voltage characteristics of CB BJT configuration	Problem solving
S-4-5	SLO-1	Lab 1: PN Junction Diode Characteristics	Lab 4: Diode clipping and clamping circuits	Lab 7: Series and Shunt Regulators	Lab 10: BJT and MOSFET Switching Circuits	Lab 13: Repeat Experiments
	SLO-2					
S-6	SLO-1	Calculate depletion width	Filters: Inductor & Capacitor Filters	Tunnel Diode	Current-Voltage characteristics of CC BJT configuration	Derive transconductance
	SLO-2	Calculate barrier potential	Problem solving	Tunnel Diode	Current-Voltage characteristics of CC BJT configuration	Problem solving
S-7	SLO-1	Derive diode current equation	Filters: LC & CLC Filters	Gun Diode	BJT as an amplifier	CMOS FET

	SLO-2	Derive diode current equation	Problem solving	German Diode	BJT as a switch	MOSFET as an amplifier
S-8	SLO-1	Effect of Capacitance in PN junction: Transition Capacitance	Diode Clippers	IMPATT Diode	BJT circuit models – h -parameter	MOSFET as a switch
	SLO-2	Diffusion Capacitance	Problem solving	IMPATT Diode	BJT circuit models – hybrid- π parameter	Problem solving
S-9-10	SLO-1	Lab 2: Zener diode characteristics	Lab 5: BJT Characteristics	Lab 8: MOSFET Characteristics	Lab 11: Photoconductive Cell, LED, and Solar Cell Characteristics	Lab-14: Model Examination
S-11	SLO-1	Energy band structure of PN Junction Diode	Diode Clippers	PN Diode	BJT biasing circuits and stability analysis: Base bias and emitter bias	Biasing Circuits for MOSFET: Gate Bias
	SLO-2	Ideal diode and its current-voltage characteristics	Problem solving	PN Photodiode	Problem solving	Problem Solving
S-12	SLO-1	Terminal characteristics & parameters	Voltage Multipliers	Avalanche photodiode	Voltage-divider bias	Self-bias
	SLO-2	Diode modeling	Zener diode: Characteristics, breakdown mechanisms	Laser diode	Problem solving	Problem Solving
S-13	SLO-1	DC load line and analysis	Zener resistances and temperature effects Zener diode as voltage regulator	Problem solving	Collector-feedback bias	Voltage-divider bias
	SLO-2	Problem solving	Problem solving	Problem solving	Problem solving	Problem Solving
S-14-15	SLO-1	Lab 3: Diode rectifier circuits	Lab 6: BJT Biasing Circuits	Lab 9: MOSFET Biasing Circuits	Lab 12: Simulation experiments using PSpice	Lab-15: End-Semester Practical Examination

Learning Resources	1. David A. Bell, <i>Electronic Devices and Circuits</i> , 5 th ed., Oxford University Press, 2015	5. Robert L. Boylestad, Louis Nashelsky, <i>Electronic Devices and Circuit Theory</i> , 11 th ed., Pearson Education, 2013
	2. Donald Neuman, <i>Electronic Circuits: Analysis and Design</i> , 3 rd ed., McGraw-Hill Education, 2011	6. Muhammad Rashid, <i>Microelectronic Circuits: Analysis & Design</i> , 2 nd ed., Cengage Learning, 2010
	3. Adel S. Sedra, Kenneth C. Smith, <i>Microelectronic Circuits: Theory and Applications</i> , OUP, 2014	7. Muhammad H Rashid, <i>Introduction to Pspice using OrCAD for circuits and electronics</i> , 3 rd ed., Pearson, 2004
	4. Thomas L. Floyd, <i>Electronic Devices</i> , 9 th ed., Pearson Education, 2013	8. Laboratory Manual, Department of ECE, SRM University

Learning Assessment											
	Bloom's Level of Thinking	Continuous Learning Assessment (50% weightage)								Final Examination (50% weightage)	
		CLA – 1 (10%)		CLA – 2 (15%)		CLA – 3 (15%)		CLA – 4 (10%)#			
		Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	20%	20%	15%	15%	15%	15%	15%	15%	15%	15%
	Understand										
Level 2	Apply	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	Analyze										
Level 3	Evaluate	10%	10%	15%	15%	15%	15%	15%	15%	15%	15%
	Create										
	Total	100 %		100 %		100 %		100 %		-	

CLA – 4 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, MOOCs, Certifications, Conf. Paper etc.,

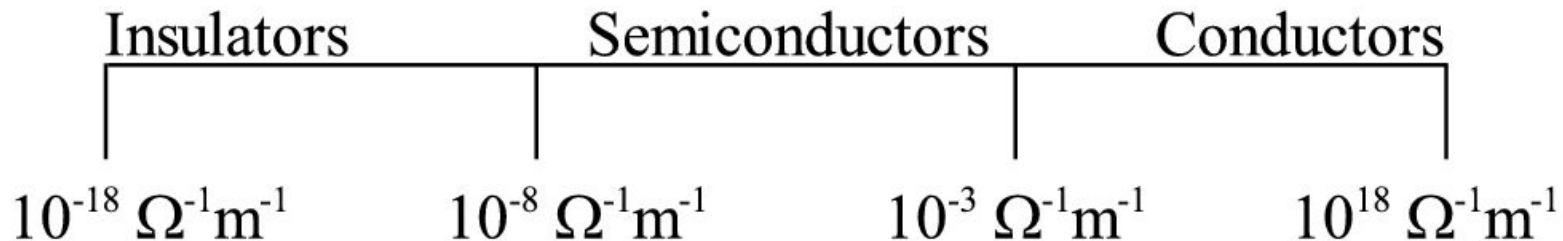
Course Designers		
Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr. Anuj Kumar, Bombardier Transportation, Ahmedabad, anujkumar.ans@gmail.com	1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meenakshi@annauniv.edu	1. Mr. Manikandan AVM, SRMIST
2. Mr. Hartharasaudhan – Johnson Controls, Pune, hartharasaudhan.v@gmail.com	2. Dr. Venkatesan, Sr. Scientist, NIOT, Chennai, venkat@niot.res.in	2. Dr. Divakar R Marur, SRMIST

UNIT I

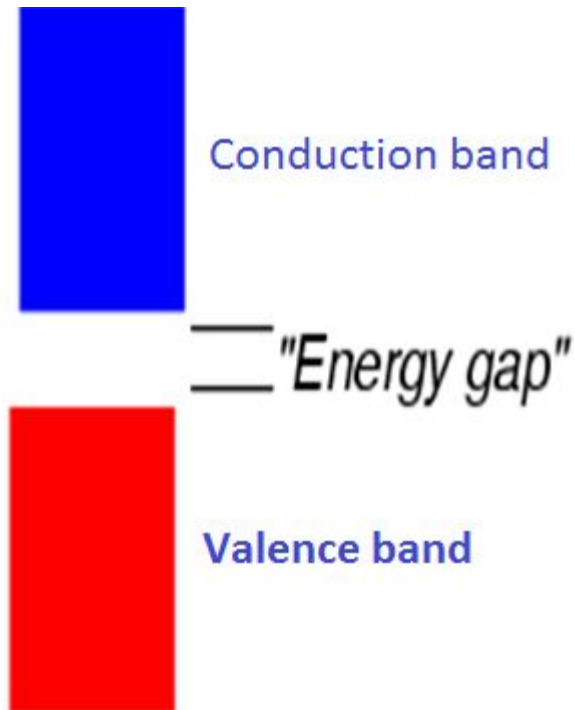
SEMICONDUCTOR DIODES

Semiconductors

- Materials having an **electrical conductivity** value falling **between that of a conductor**, such as metallic copper, and **an insulator**, such as glass.

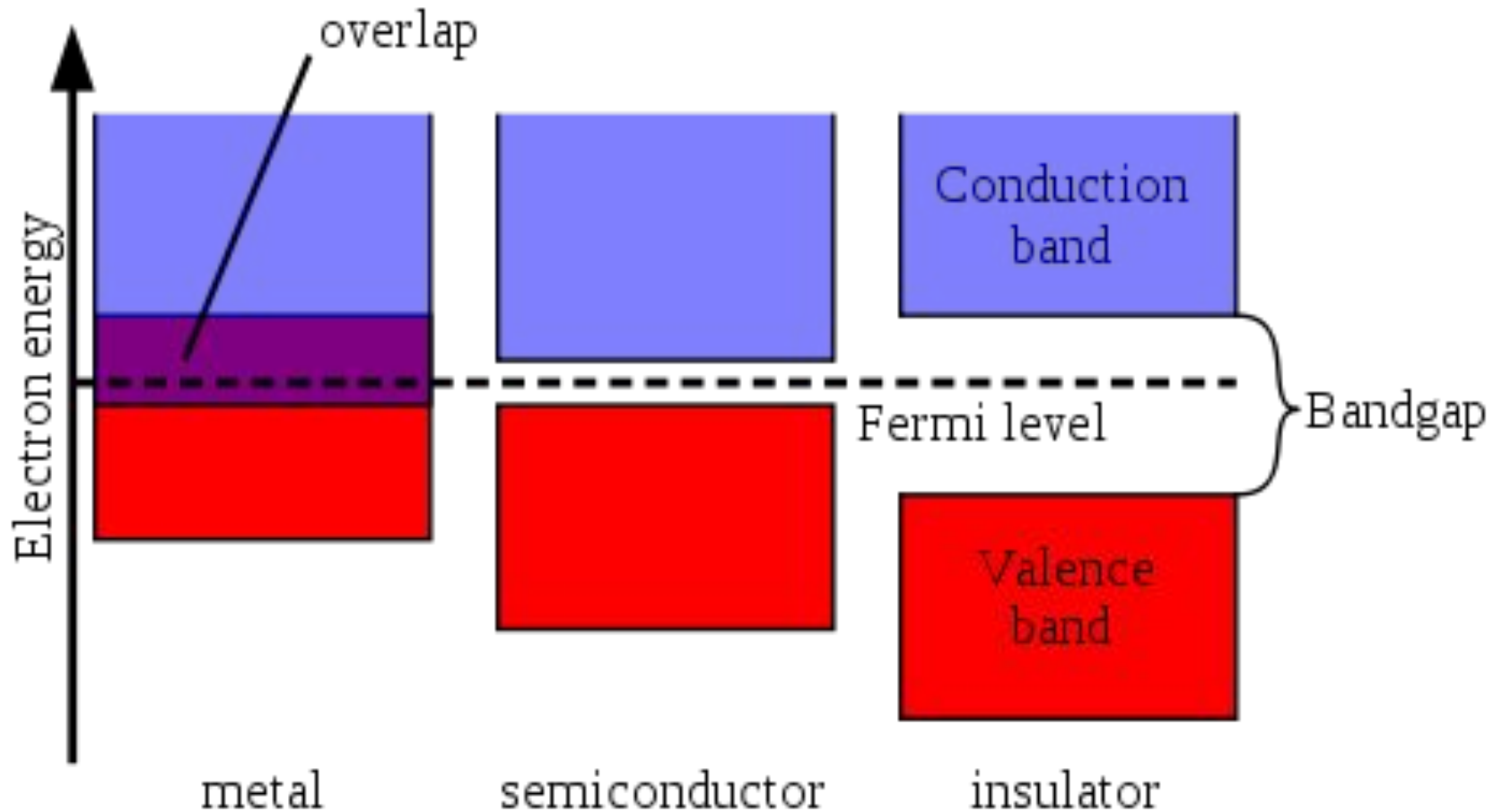


Electrical conductivity

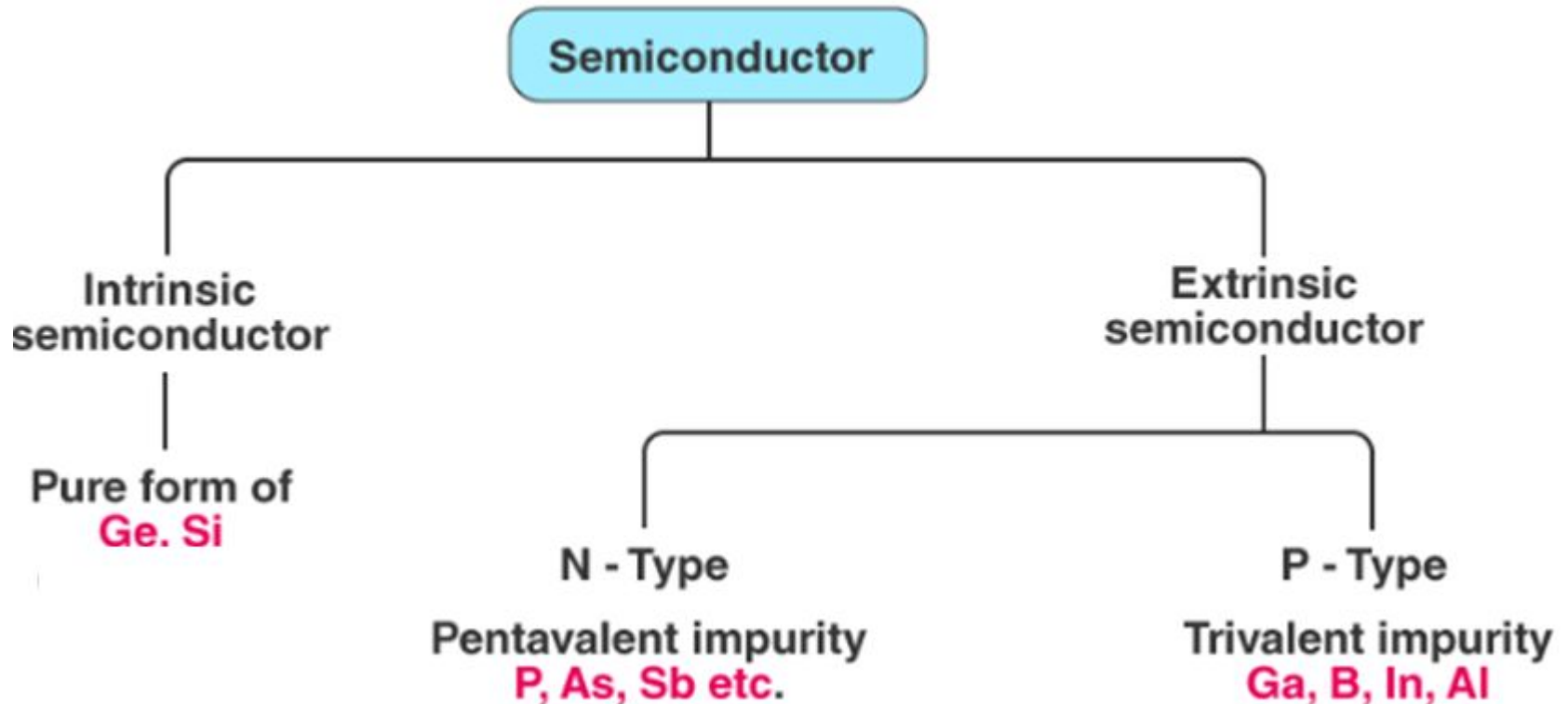


- *The highest occupied energy band is called the valence band.*
- *Most electrons remain bound to the atoms in this band.*
- *The conduction band is the band of orbitals that are high in energy and are generally empty.*
- *It is the band that accepts the electrons from the valence band*
- *The “leap” required for electrons from the Valence Band to enter the Conduction Band.*

Energy band Diagram

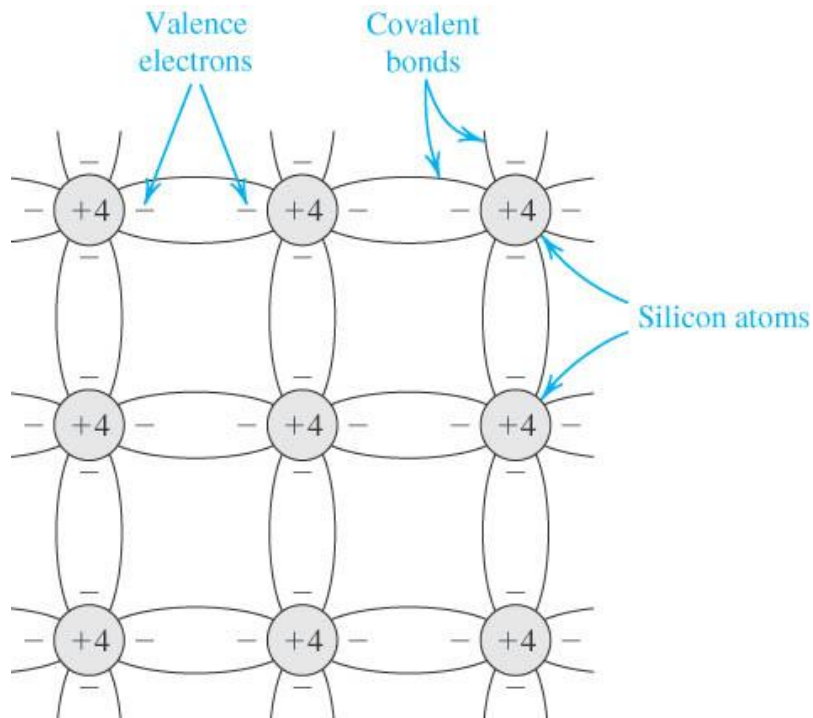


Types of semiconductors



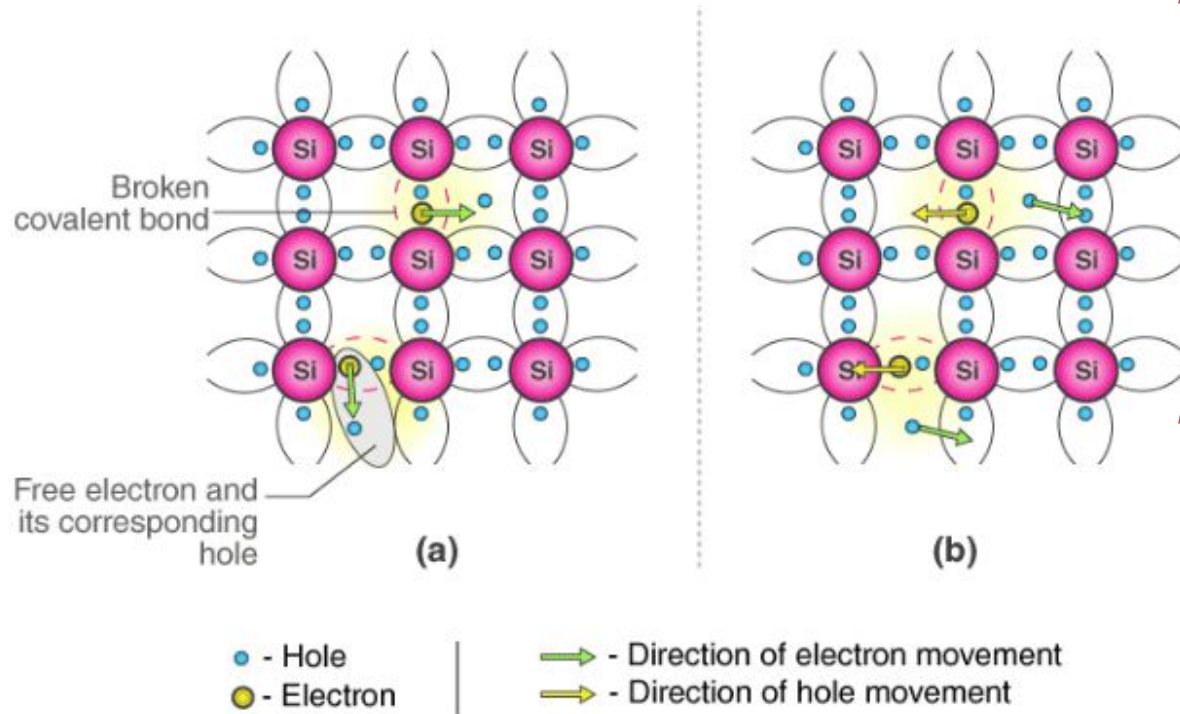
Intrinsic Semiconductor

- *A crystal of pure and regular lattice structure is called intrinsic semiconductor.*



- each silicon atom has four valence electrons
- two valence electrons from two silicon atoms form the covalent bond
- Be intact at sufficiently low temperature
- Be broken at room temperature

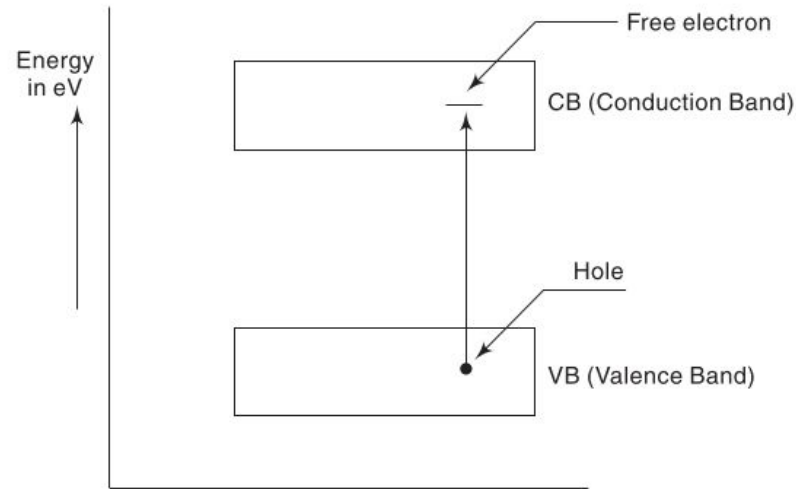
Free Electrons and Holes



□ **Free electrons** are produced by thermal ionization, which can move freely in the lattice structure.

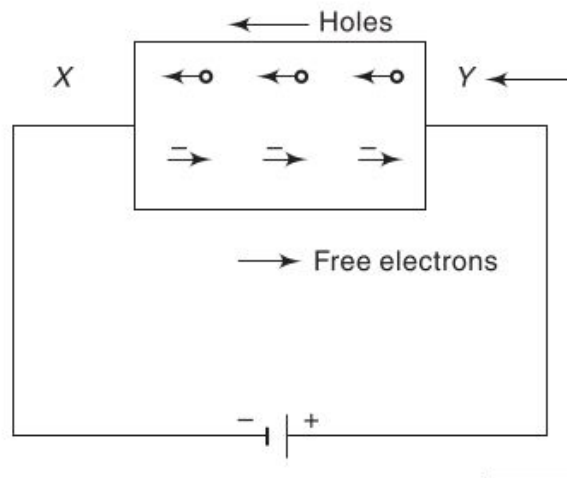
□ **Holes** are empty position in broken covalent bond, which can be filled by free electron, positive charge

Creation of Electron and hole in a semiconductor



Creation of electron-hole pair in a semiconductor

Current Conduction in semiconductor



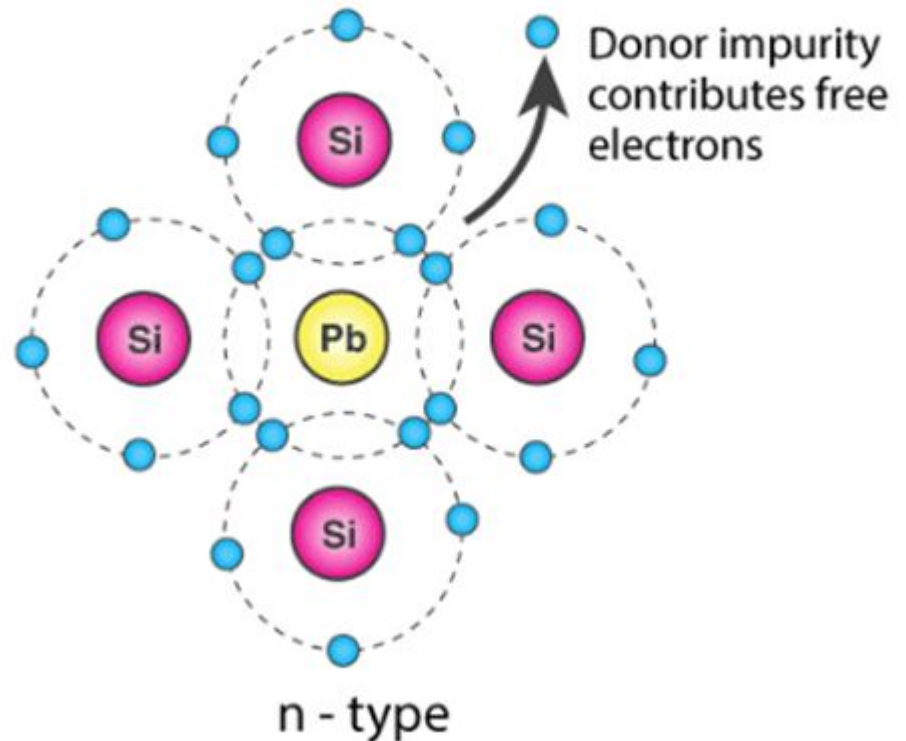
Current conduction in semiconductor

Extrinsic Semiconductor

- The conductivity of semiconductors improved by introducing a small number of suitable replacement atoms called **IMPURITIES**.
- The process of adding impurity atoms to the pure semiconductor is called **DOPING**.
- Usually, only 1 atom in 10^7 is replaced by a dopant atom in the doped semiconductor.
- An extrinsic semiconductor can be further classified into:
 - **N-type Semiconductor**
 - **P-type Semiconductor**

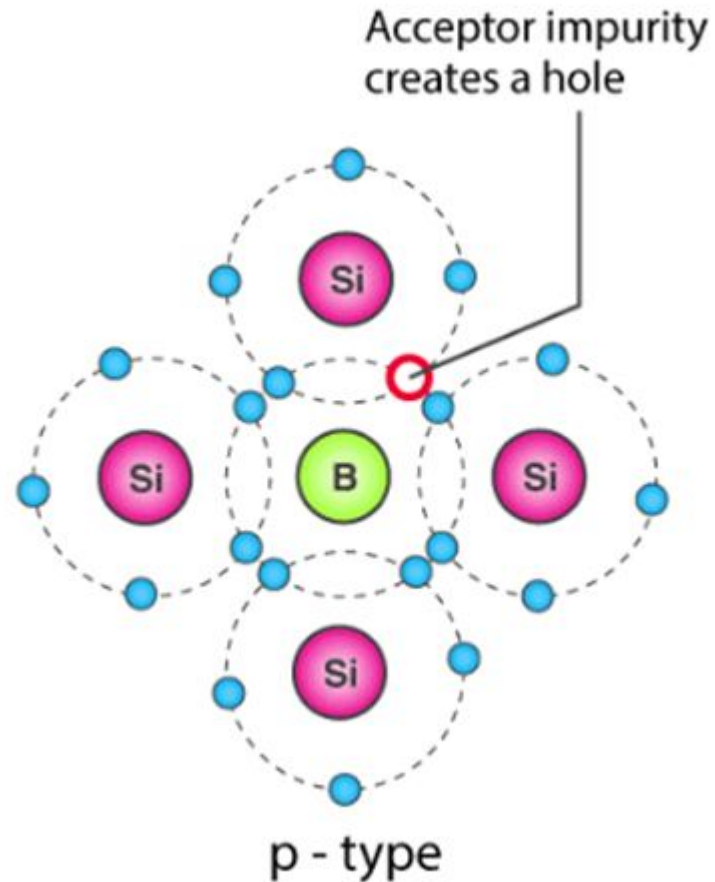
N-type Semiconductor

- A silicon crystal doped by a pentavalent element. (*phosphorus or arsenic*)
- Each dopant atom donates a free electron and is thus called a donor.
- The doped semiconductor becomes *n* type.



P-type Semiconductor

- A silicon crystal doped with a trivalent impurity. (aluminum, boron)
- Each dopant atom gives rise to a hole, and called acceptor
- the semiconductor becomes *p* type.



Difference between Intrinsic and Extrinsic Semiconductor

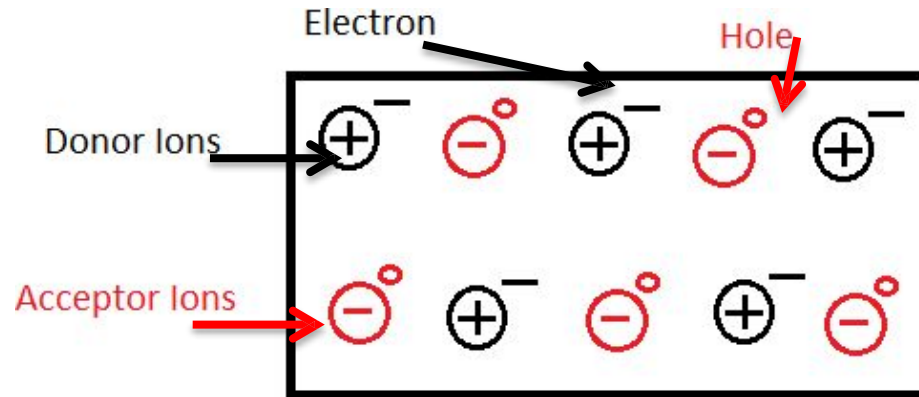
Intrinsic Semiconductor	Extrinsic Semiconductor
Pure semiconductor	Impure semiconductor
Density of electrons is equal to the density of holes	Density of electrons is not equal to the density of holes
Electrical conductivity is low	Electrical conductivity is high
Dependence on temperature only	Dependence on temperature as well as on the amount of impurity
No impurities	Trivalent impurity, pentavalent impurity

Mass Action Law

- Under thermal equilibrium the **product** of the **free electron concentration** and the **free hole concentration** is equal to a constant equal to the **square of intrinsic carrier concentration**.

$$np = n_i^2$$

Electrical Neutrality in Semiconductor



Positive Charge Density

p □ Hole Concentration

N_D □ Concentration of donor ions

Negative Charge Density

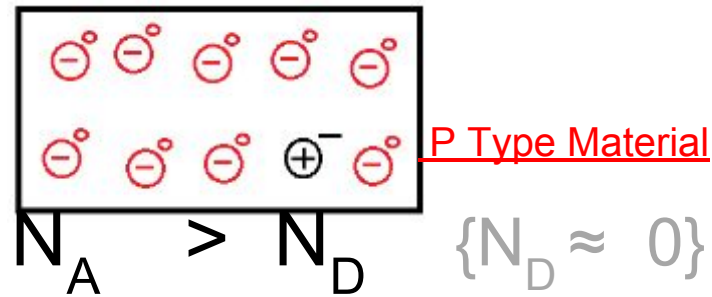
n □ Electron Concentration

N_A □ Concentration of Acceptor ions

Total +^{ve} charged density = Total – ve charged density

$$p + N_D = n + N_A$$

Charge Density in a Semiconductor



$$p_p + N_D = n_p + N_A$$

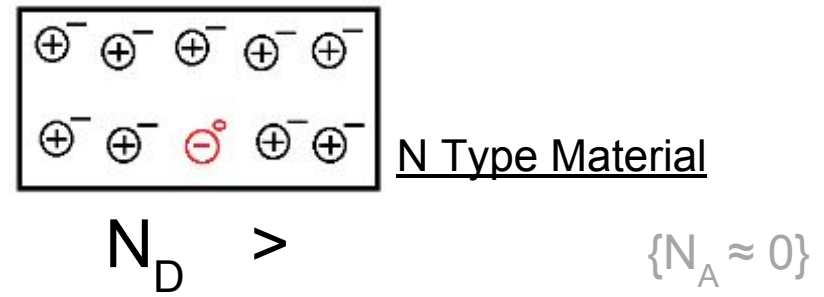
$$N_A = p_p - n_p \quad \{p_p \gg n_p\}$$

$$N_A = p_p$$

Mass action Law:

$$n_p p_p = n_i^2$$

$$n_p \approx n_i$$



$$p_n + N_D = n_n + N_A$$

$$N_D = n_n - p_n \quad \{n_n \gg p_n\}$$

$$N_D = n_n$$

$$n_n p_n = n_i^2$$

Mass action Law:

$$n^2$$

$$p_n \approx n_i$$

Conductivity of Semiconductor

$$J = J_p + J_n$$

$$J_p = qp\mu_p E$$

$$J_n = -qn(-\mu_n E)$$

$$J = qp\mu_p E + qn\mu_n E$$

$$J = q(p\mu_p + n\mu_n)E$$

$$J \equiv \sigma E$$

The **conductivity** of a semiconductor is

$$\sigma \equiv qp\mu_p + qn\mu_n$$

The **resistivity** of a semiconductor is

$$\rho \equiv \frac{1}{\sigma}$$

Problems

The mobility of free electrons and holes in pure germanium are 3800 and 1800 cm²/V-s respectively. The corresponding values for pure silicon are 1300 and 500 cm²/V-s, respectively. Determine the values of intrinsic conductivity for both germanium and silicon. Assume $n_i = 2.5 \times 10^{13}$ cm⁻³ for germanium and $n_i = 1.5 \times 10^{10}$ cm⁻³ for silicon at room temperature.

Solution: (i) The intrinsic conductivity for germanium,

$$\begin{aligned}\sigma_i &= qn_i(\mu_n + \mu_p) \\ &= (1.6 \times 10^{-19}) (2.5 \times 10^{13}) (3800 + 1800) \\ &= 0.0224 \text{ S/cm}\end{aligned}$$

(ii) The intrinsic conductivity for silicon,

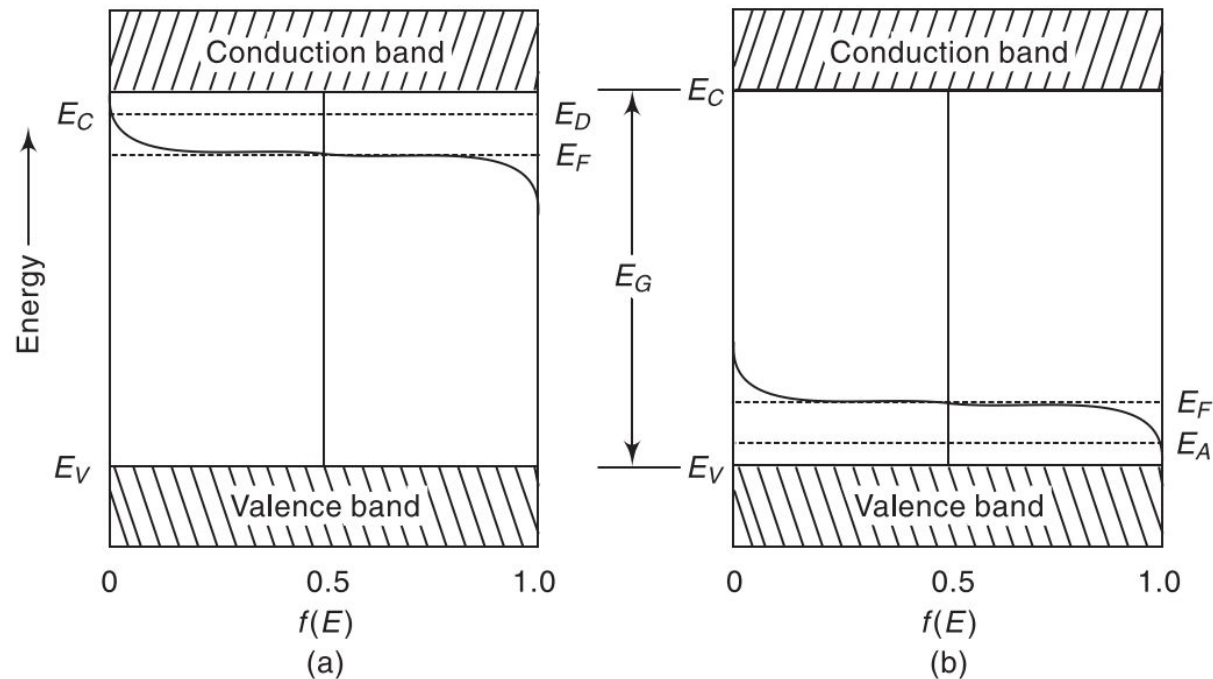
$$\begin{aligned}\sigma_i &= qn_i(\mu_n + \mu_p) \\ &= (1.6 \times 10^{-19}) (1.5 \times 10^{10}) (1300 + 500) \\ &= 4.32 \times 10^{-6} \text{ S/cm}\end{aligned}$$

CARRIER CONCENTRATION IN INTRINSIC SEMICONDUCTOR

The Fermi Dirac probability function $f(E)$ is given by

$$f(E) = \frac{1}{1 + e^{(E - E_F)/kT}}$$

where E_F is the Fermi level or characteristic energy for the crystal in eV.



Positions of Fermilevel in (a) N-type and (b) P-type semiconductors.

The concentration of electrons in the conduction band is,

$$n = N_C e^{-(E_c - E_F)/kT}$$

where $N_C = 2 \left(\frac{2\pi m_n kT}{h^2} \right)^{3/2} (1.60 \times 10^{-19})^{3/2}$, where m_n is the effective mass of an electron.

The concentration of holes in the valence band is,

$$p = N_V e^{(E_F - E_v)/kT}$$

where

$N_V = 2 \left(\frac{2\pi m_p kT}{h^2} \right)^{3/2} (1.60 \times 10^{-19})^{3/2}$, where m_p is the effective mass of a hole.

Fermi level in an Intrinsic

Fermi level in an intrinsic semiconductor In the case of intrinsic material, the crystal must be electrically neutral.

$$n_i = p_i$$

$$\text{Therefore, } N_C e^{-(E_C - E_F)/kT} = N_V e^{-(E_F - E_V)/kT}$$

Taking the logarithm on both sides,

$$\ln \frac{N_C}{N_V} = \frac{E_C + E_V - 2E_F}{kT}$$
$$E_F = \frac{E_C + E_V}{2} - \frac{kT}{2} \ln \frac{N_C}{N_V}$$

If the effective masses of a free electron and hole are the same,

$$N_C = N_V$$

$$\text{Then, } E_F = \frac{E_C + E_V}{2}$$

From the above equation, at the centre of the forbidden energy band, Fermi level is present.

Fermi level in an Extrinsic Semiconductor

Fermi level in a semiconductor having impurities The Fermi level in an N-type material is given by

$$E_F = E_C + kT \ln \frac{N_C}{N_D}$$

where $N_D = N_C e^{-(E_C - E_F)/kT}$, the concentration of donor atoms.

The Fermi level in a P-type material is given by

$$E_F = E_V + kT \ln \frac{N_V}{N_A}$$

where $N_A = N_V e^{-(E_F - E_V)/kT}$, the concentration of acceptor atoms.

Problems

In an N-type semiconductor, the Fermi level is 0.3 eV below the conduction level at a room temperature of 300 K. If the temperature is increased to 360 °K, determine the new position of the Fermi level.

Solution: The Fermi level in an N-type material is given by

$$E_F = E_C - kT \ln \frac{N_C}{N_D}$$

Therefore, $(E_C - E_F) = kT \ln \frac{N_C}{N_D}$

At $T = 300$ K, $0.3 = 300 \text{ °K} \ln \frac{N_C}{N_D}$ (1)

Similarly, $E_C - E_{F1} = 360 \text{ K} \ln \frac{N_C}{N_D}$ (2)

Eqn. (2) divided by Eqn. (1) gives

$$\frac{E_C - E_{F1}}{0.3} = \frac{360}{300}$$

Therefore, $E_C - E_{F1} = \frac{360}{300} \times 0.3 = 0.36 \text{ eV}$

Hence, the new position of the Fermi level lies 0.36 eV below the conduction level.

Find the conductivity of silicon (a) in intrinsic condition at a room temperature of 300 °K, (b) with donor impurity of 1 in 10^8 , (c) with acceptor impurity of 1 in 5×10^7 and (d) with both the above impurities present simultaneously. Given that n_i for silicon at 300 °K is $1.5 \times 10^{10} \text{ cm}^{-3}$, $\mu_n = 1300 \text{ cm}^2/\text{V-s}$, $\mu_p = 500 \text{ cm}^2/\text{V-s}$, number of Si atoms per $\text{cm}^3 = 5 \times 10^{22}$.

(a) In intrinsic condition, $n = p = n_i$

$$\begin{aligned}\text{Hence, } \sigma_i &= qn_i (\mu_n + \mu_p) \\ &= (1.6 \times 10^{-19}) (1.5 \times 10^{10}) (1300 + 500) \\ &= 4.32 \times 10^{-6} \text{ S/cm}\end{aligned}$$

(b) Number of silicon atoms/ $\text{cm}^3 = 5 \times 10^{22}$

$$\text{Hence, } N_D = \frac{5 \times 10^{22}}{10^8} = 5 \times 10^{14} \text{ cm}^{-3}$$

Further, $n \approx N_D$

$$\begin{aligned}\text{Therefore, } p &= \frac{n_i^2}{n} \approx \frac{n_i^2}{N_D} \\ &= \frac{(1.5 \times 10^{10})^2}{5 \times 10^{14}} = 0.46 \times 10^6 \text{ cm}^{-3}\end{aligned}$$

Thus $p \ll n$. Hence p may be neglected while calculating the conductivity.

$$\begin{aligned}\text{Hence, } \sigma &= nq\mu_n = N_D q \mu_n \\ &= (5 \times 10^{14}) (1.6 \times 10^{-19}) (1300) \\ &= 0.104 \text{ S/cm.}\end{aligned}$$

$$(c) N_A = \frac{5 \times 10^{22}}{5 \times 10^7} = 10^{15} \text{ cm}^{-3}$$

Further, $p \approx N_A$

Hence,

$$n = \frac{n_i^2}{p} \approx \frac{n_i^2}{N_A}$$

$$= \frac{(1.5 \times 10^{10})^2}{10^{15}} = 2.25 \times 10^5 \text{ cm}^{-3}$$

Thus, $p \gg n$. Hence n may be neglected while calculating the conductivity.

Hence,

$$\begin{aligned} \sigma &= pq\mu_p = N_A q \mu_p \\ &= (10^{15} \times 1.6 \times 10^{-19} \times 500) \\ &= 0.08 \text{ S/cm.} \end{aligned}$$

(d) With both types of impurities present simultaneously, the net acceptor impurity density is,

$$N_A' = N_A - N_D = 10^{15} - 5 \times 10^{14} = 5 \times 10^{14} \text{ cm}^{-3}$$

Hence,

$$\begin{aligned} \sigma &= N_A' q \mu_p \\ &= (5 \times 10^{14}) (1.6 \times 10^{-19}) (500) \\ &= 0.04 \text{ S/cm.} \end{aligned}$$

Current Flow in Semiconductors

There are **two mechanisms by which holes and free electrons move through a silicon crystal.**

- **Drift**

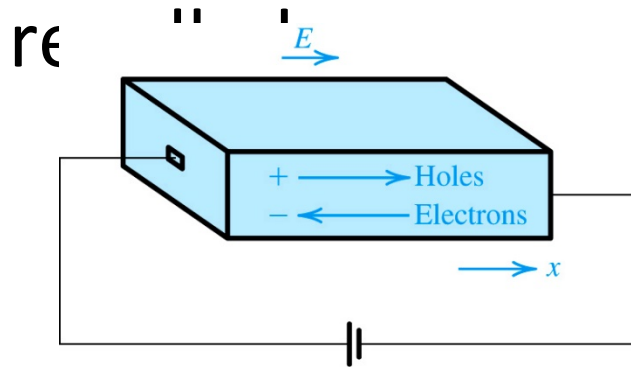
- The carrier motion is generated by the electrical field across a piece of silicon. This motion will produce drift current.

- **Diffusion**

- The carrier motion is generated by the different concentration of carrier in a piece of silicon. The diffused motion, usually carriers diffuse from high concentration to low concentration, will give rise to diffusion current.

Drift Current (I_s)

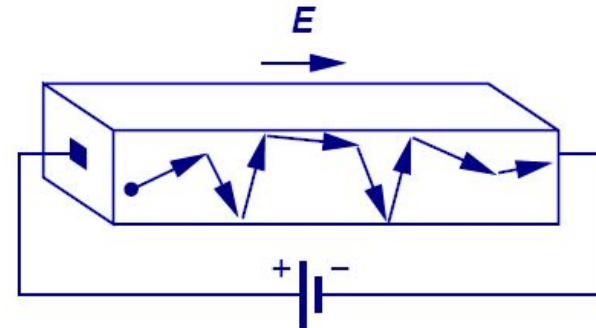
- When an electrical field (E) is applied to a semiconductor crystal holes are accelerated in the direction of E , free electrons are



μ_p = hole mobility

E = electric field

$$v_{p-drift} = \mu_p E$$



μ_n = electron mobility

E = electric field

$$v_{n-drift} = -\mu_n E$$

The **flow of electric current** due to the motion of the charge carriers under the influence of an **external electric field** is called Drift Current

$$J_{Drift} = J_{p\ Drift} + J_{n\ Drift}$$

$$J_{p\ Drift} = \quad \text{A/cm}^2$$

$$qp\mu_p E \quad J_{n\ Drift} \quad \text{A/cm}^2$$

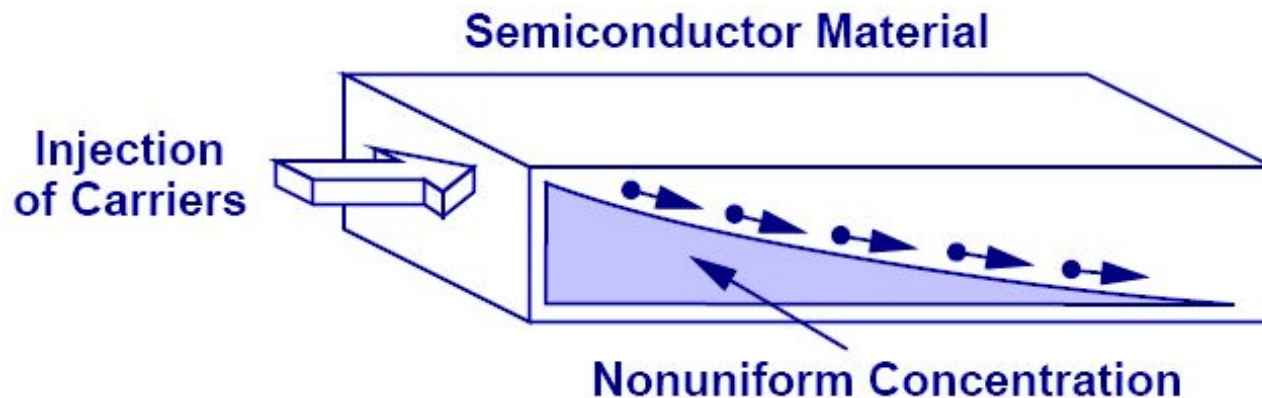
$$J_{Drift} = qp\mu_p E + qn\mu_n E$$

$$J_{Drift} = q(p\mu_p + n\mu_n)E$$

$$J_{Drift} \equiv \sigma .E$$

Diffusion Current (I_D)

- **Carrier diffusion** – is the flow of charge carriers from area of **high concentration to low concentration**.
 - It requires **non-uniform distribution** of carriers.
- **Diffusion current** – is the **current flow** that results from diffusion.
- Current flow due to mobile charge diffusion is proportional to the carrier concentration gradient.
- The proportionality constant is the diffusion constant.



J_p = current flow density attributed to holes

q = magnitude of the electron charge

D_p = diffusion constant of holes (12cm²/s for silicon)

$p(x)$ = hole concentration at point x

dp/dx = gradient of hole concentration

hole diffusion current density: $J_p = -qD_p \frac{dp(x)}{dx}$

electron diffusion current density: $J_n = -qD_n \frac{dn(x)}{dx}$

J_n = current flow density attributed to free electrons

D_n = diffusion constant of electrons (35cm²/s for silicon)

$n(x)$ = free electron concentration at point x

dn/dx = gradient of free electron concentration

▪ **Diffusion Current** $I_p = J_p \cdot A; I_n = J_n \cdot A$

$$I_D = I_p + I_n$$

- Drift current $I_S = J_{drift} A$; Due to electric field
- Diffusion current $I_D = J_{diff} A$; Due to concentration gradient

A = cross-sectional area of silicon, q = magnitude of the electron charge,

p = concentration of holes, n = concentration of free electrons,

μ_p = hole mobility, μ_n = electron mobility, E = electric field

drift current density : $J_{drift} = J_{p-drift} + J_{n-drift} = q(p\mu_p + n\mu_n)E$

diffusion current density : $J_{diff} = J_{p-diff} + J_{n-diff} = -qD_p \frac{dp(x)}{dx} - qD_n \frac{dn(x)}{dx}$

D_p = diffusion constant of holes (12cm²/s for silicon), D_n = diffusion constant of electrons (35cm²/s for silicon),

$p(x)$ = hole concentration at point x , $n(x)$ = free electron concentration at point x ,

dp/dx = gradient of hole concentration, dn/dx = gradient of free electron concentration

Total Current

Total Current in P type semiconductor

$$J_p = J_{p \text{ Drift}} + J_{p \text{ Diffusion}}$$

$$J_p = q p \mu_p E - q D_p \frac{dp}{dx}$$

Total Current in N type semiconductor

$$J_n = J_{n \text{ Drift}} + J_{n \text{ Diffusion}}$$

$$J_n = q n \mu_n E + q D_n \frac{dn}{dx}$$