18ECC203J – Module 3

8086 Interfacing with Memory and Programmable Devices

S – 6, 7, 8

S – 6

Stepper Motor interfacing

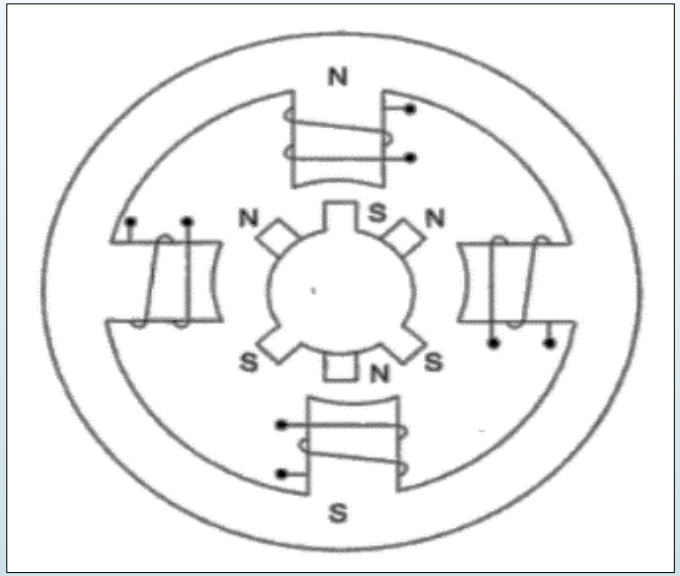
Stepper Motor Interfacing

- A stepper motor is a device to obtain an accurate position control of rotating shaft. Rotation of shaft takes place in terms of steps unlike AC or DC motors.
- To rotate the shaft, sequences of pulses are applied to the windings of the stepper motor, in a sequence.
- No of pulses required for one complete rotation of the shaft of the stepper motor is equivalent to number of teeth on its rotor.
- When the rotor teeth and stator teeth lock with each other to fix a shaft in a position
- When a pulse applied to the winding, the rotor rotates by one tooth or an angle x.

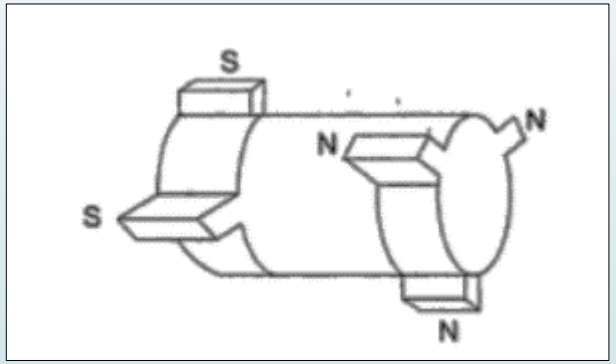
$$x = \frac{360^{\circ}}{no.\,of\ rotor\ teeth} \quad \text{.... (1)}$$

Stepper Motor Interfacing (2)

- After rotation of the shaft through angle x, the rotor locks itself with the next tooth in the sequence on the internal surface of stator.



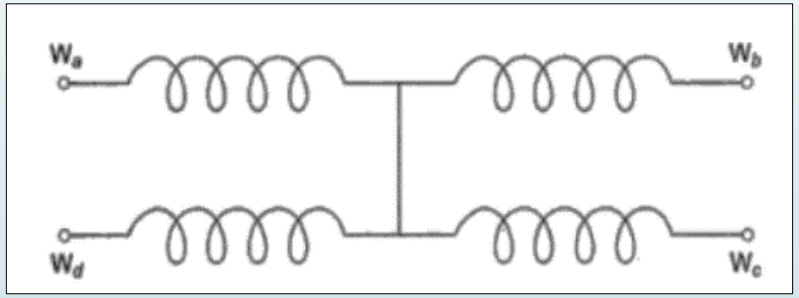
Internal Schematic of a four winding Stepper motor



Schematic of a stepper motor rotor with six teeth on its surface

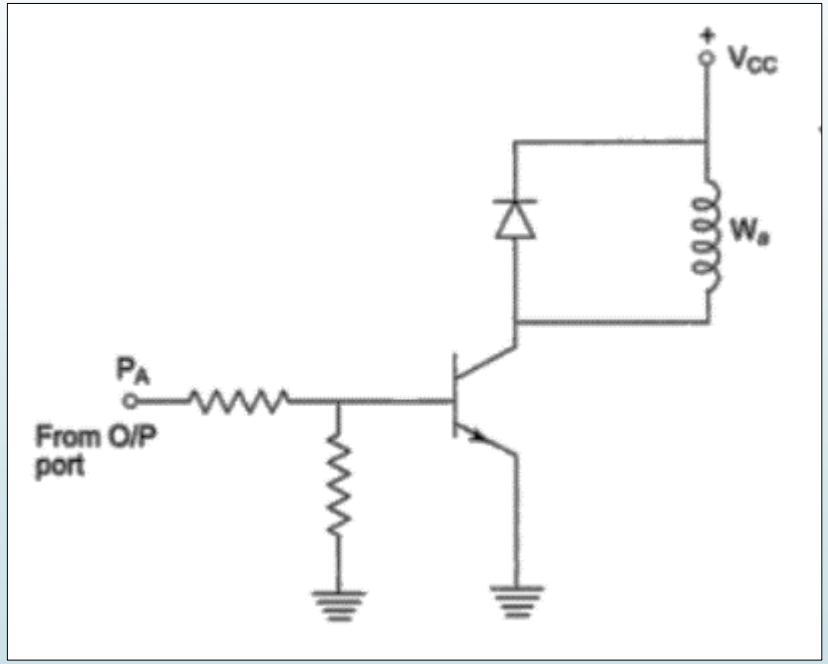
Winding Information

Stepper motors are designed to work with digital circuits. Binary level pulses (0-5 V) are applied to energize the windings.



Winding arrangement of stepper motor

Image Courtesy: Adv. µP by A.K. Ray



Interfacing Stepper Motor Winding W_a

Image Courtesy: Adv. µP by A.K. Ray

Types of Schemes

- Pulse sequence is decided by the required motion of the shaft.
- Types of schemes
  - Wave Scheme
  - Full Step Scheme
  - Half Step Scheme
- **Wave Scheme**
  - A simple scheme to rotate the shaft of stepper motor.
  - Here W_a, W_b, W_c, and W_d are applied with the required voltage pulses, in cyclic fashion. To change the rotation in opposite direction give pulse sequence in reverse direction.
- **Full Step Scheme**
  - Here consecutive two windings are excited at a time. These are shifted only one position at a time.
- **Half Step Scheme**
  - Combination of Wave and Full Step scheme. Used for step angle reduction.

Table 1: Wave Winding

Motion	Step	A	B	C	D
Clockwise	1	1	0	0	0
	2	0	1	0	0
	3	0	0	1	0
	4	0	0	0	1
	5	1	0	0	0
Anticlockwise	1	1	0	0	0
	2	0	0	0	1
	3	0	0	1	0
	4	0	1	0	0
	5	1	0	0	0

Table 2: Full Step Winding

Motion	Step	A	B	C	D
Clockwise	1	0	0	1	1
	2	0	1	1	0
	3	1	1	0	0
	4	1	0	0	1
	5	0	0	1	1
Anticlockwise	1	0	0	1	1
	2	1	0	0	1
	3	1	1	0	0
	4	0	1	1	0
	5	0	0	1	1

Operation of Stepper Motor

Stepper motor contains Permanent Magnet (rotor) and electromagnet Stator, with one-phase-on configuration.

In the top left figure, North pole of rotor is attracted by South pole of A+ electromagnet. South pole of rotor is attracted by North pole of A+ electromagnet.

A and B are stator poles.

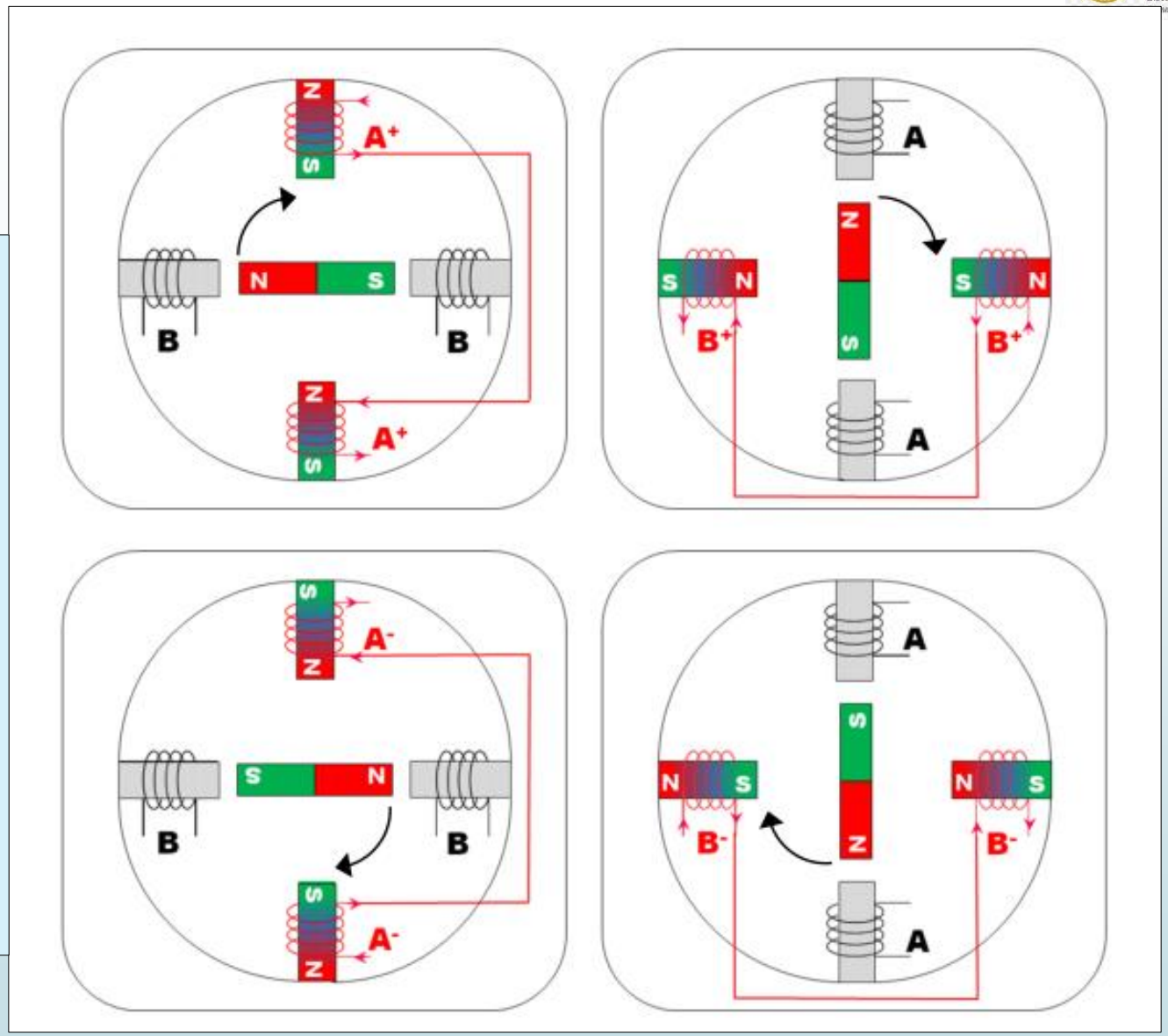


Image Courtesy: Faulhaber Brochure [1]

Typical Stepper Motor

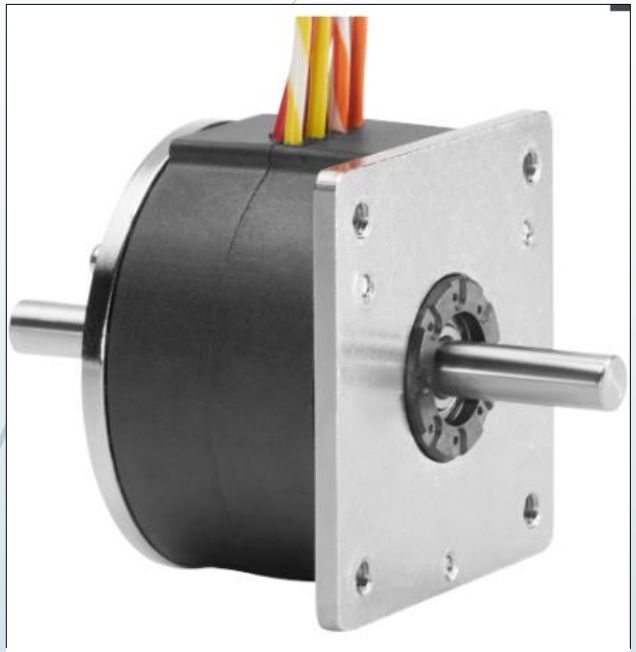


Image Courtesy: Faulhaber

A typical stepper motor may have parameters like torque 3 kg-cm, operating voltage 12 V, current rating 0.2 V and a step angle 1.8°.

The number of rotor teeth is equal to the count for one rotation, i.e. 360°. For any specified angle θ° the count (C) is calculated as:

$$C = \frac{\textbf{Number of rotor teeth}}{360^{\circ}} \times \theta^{\circ}$$

Reference

[1]_https://www.faulhaber.com/fileadmin/user_upload_global/support/MC_Support/Motors/AppNotes/Faulhaber_AN001_EN.pdf ~ Interesting and well written article

From Other Source (1/5)

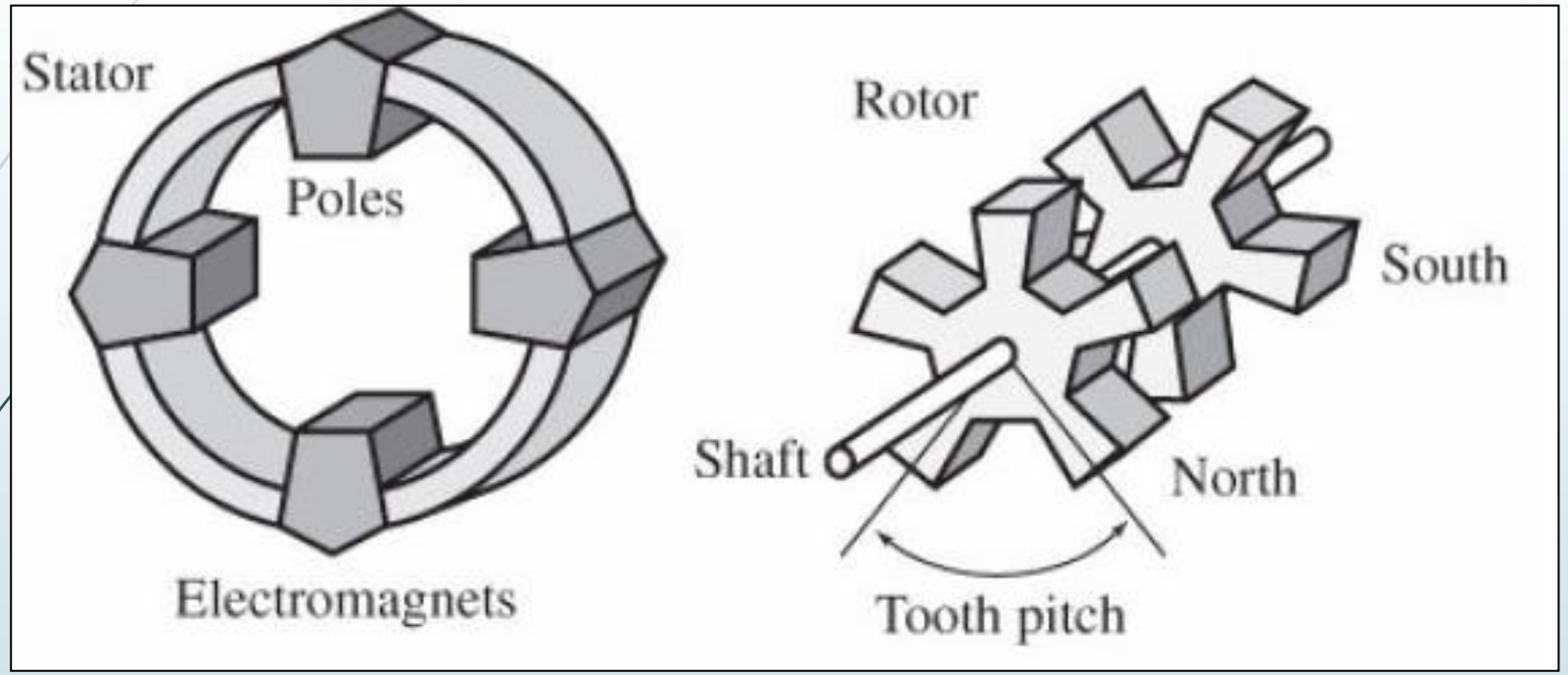


Image Courtesy: Mrs. Suganthi Brindha G., In turn Google

Rotors invariably made up of permanent magnet

From Other Source (2/5)

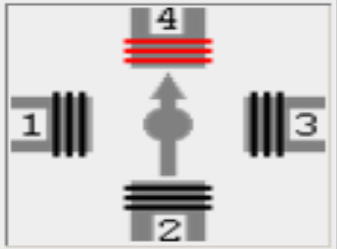
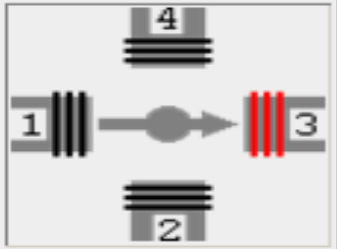
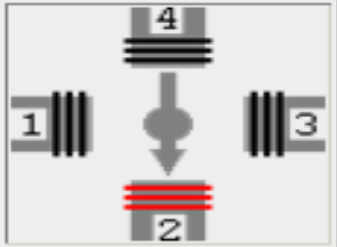
Step	Coil 4	Coil 3	Coil 2	Coil 1	
a.1	on	off	off	off	
a.2	off	on	off	off	
a.3	off	off	on	off	

Image Courtesy: Mrs. Suganthi Brindha G., In turn Google

Single Coil Excitation.

Excited coil is shown in red colour

From Other Source (3/5)

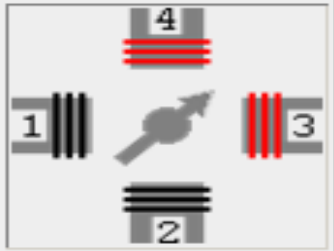
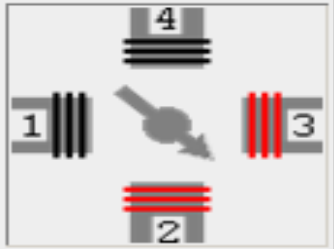
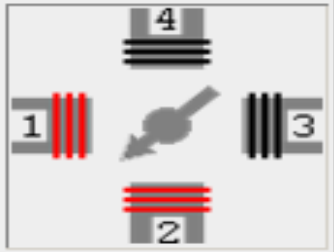
Step	Coil 4	Coil 3	Coil 2	Coil 1	
b.1	on	on	off	off	
b.2	off	on	on	off	
b.3	off	off	on	on	

Image Courtesy: Mrs. Suganthi Brindha G., In turn Google

TWO Coil Excitation.

Each successive pair of adjacent coils is energized in turn.

From Other Source (4/5)

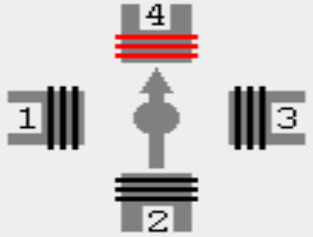
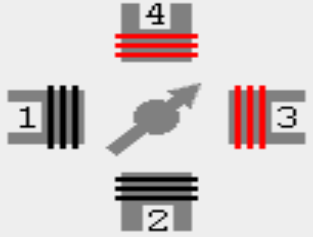
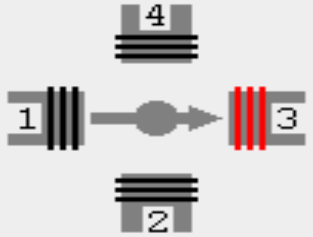
Step	Coil 4	Coil 3	Coil 2	Coil 1	
a.1	on	off	off	off	
b.1	on	on	off	off	
a.2	off	on	off	off	

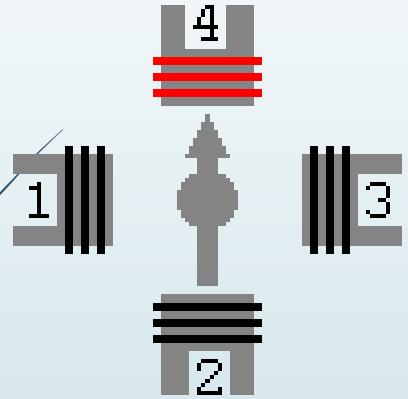
Image Courtesy: Mrs. Suganthi Brindha G., In turn Google

HALF Step Sequence.

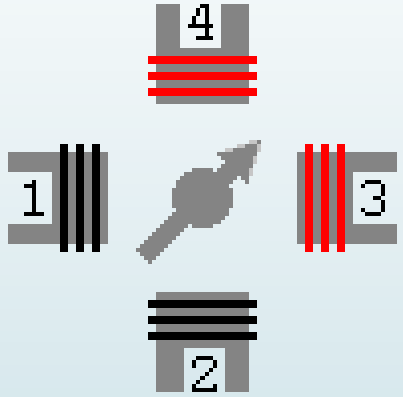
2 sequences interleaved.

normal (4 step) + wave drive (4 step) Total 8 steps.

From Other Source (5/5)

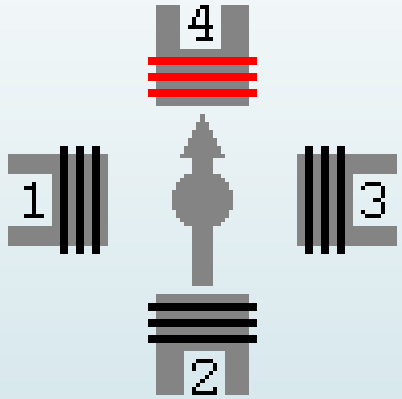


Single-Coil Excitation



Two-Coil Excitation

Interleaved Single- and Two-Coil Excitation



Half-Stepping

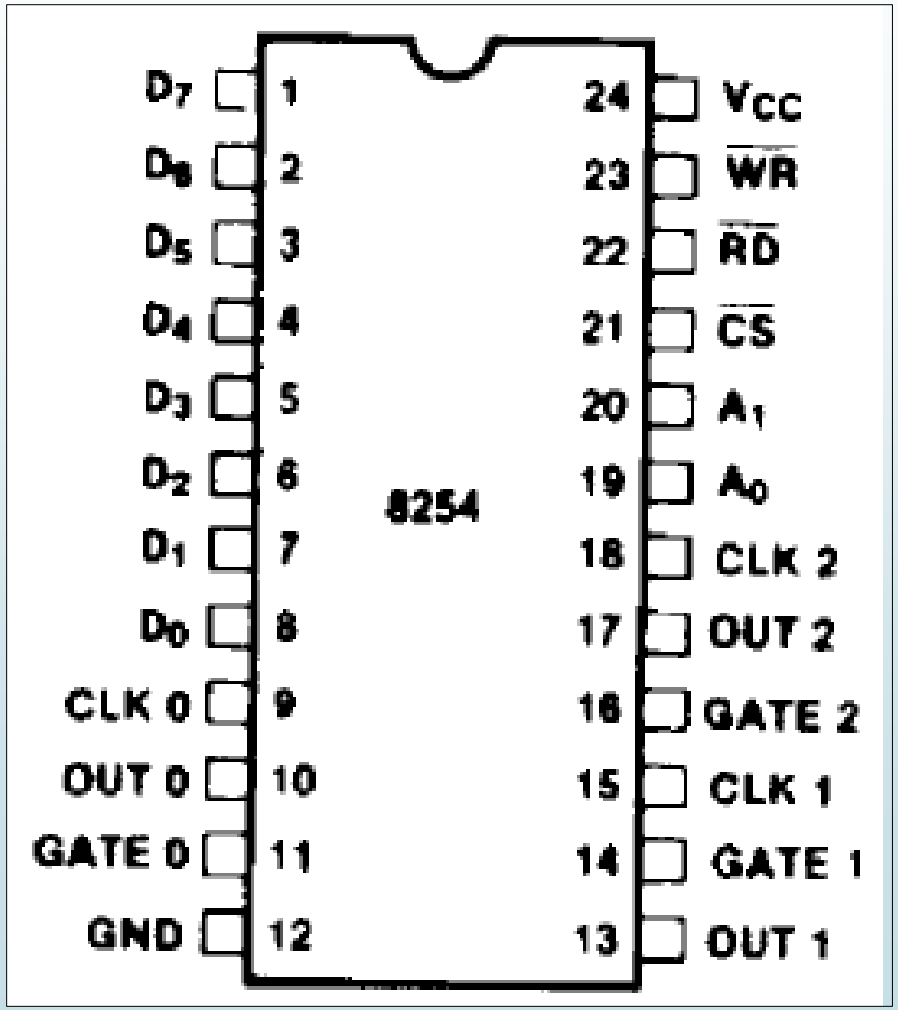
S – 7

Programmable Interval Timer 8254 & Interfacing 8254 with 8086 and programming

Features of 8254

- Three Independent 16-Bit Counters,
- Clock input up to 10 MHz,
- Status Read-Back Command,
- Six Programmable Counter Modes,
- Binary or BCD Counting,
- Single +5V Supply,
- Superset of PIT-8253.

Pin Diagram


8254
D7 1
D6 2
D5 3
D4 4
D3 5
D2 6
D1 7
D0 8
CLK 0 9
OUT 0 10
GATE 0 11
GND 12
24 VCC
23 WR
22 RD
21 CS
20 A1
19 A0
18 CLK 2
17 OUT 2
16 GATE 2
15 CLK 1
14 GATE 1
13 OUT 1

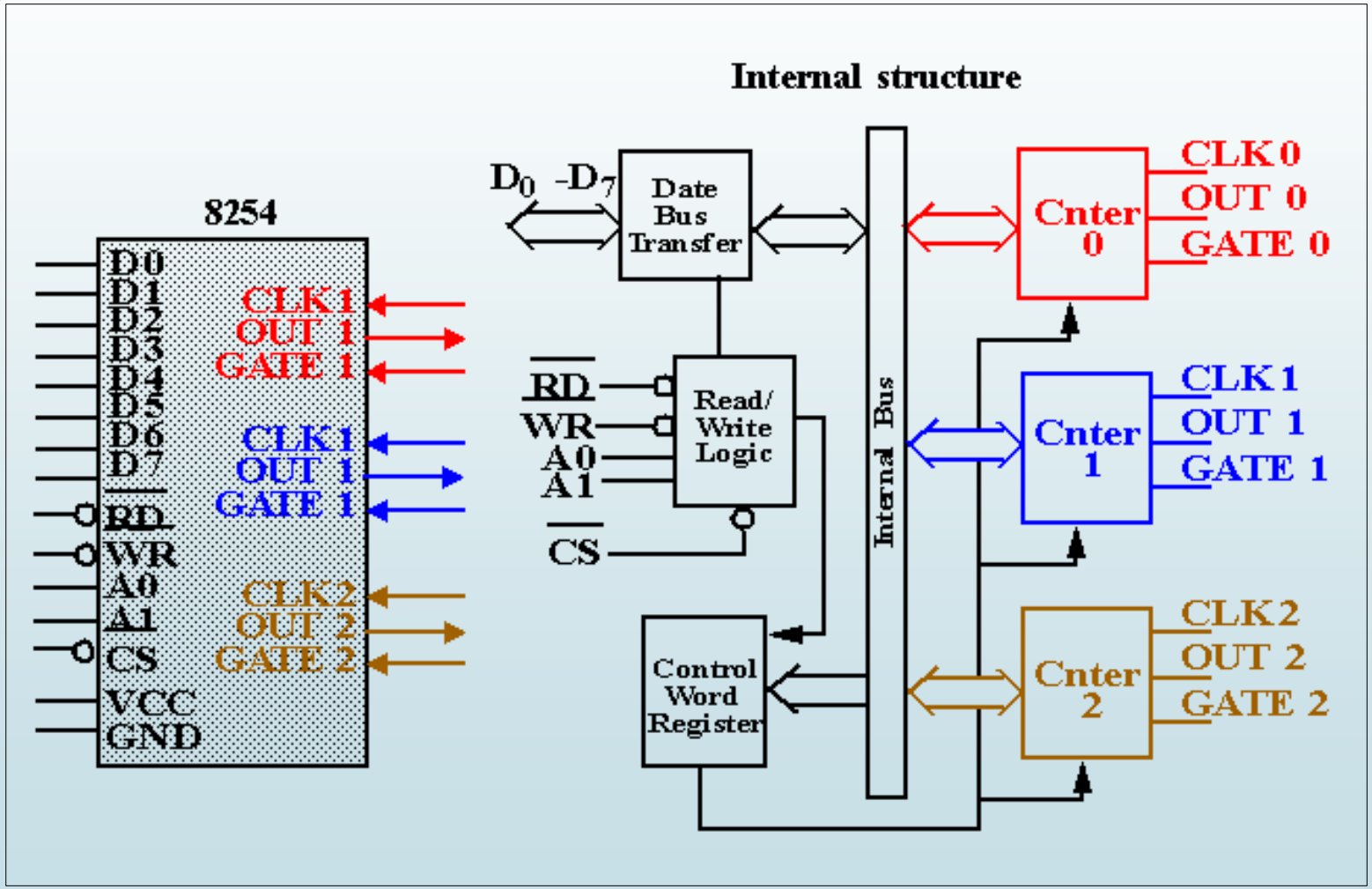
Pin Description

Symbol	Pin No.	Type	Name and Function
D_7–D_0	1–8	I/O	**DATA:** Bi-directional three state data bus lines, connected to system data bus.
CLK 0	9	I	**CLOCK 0:** Clock input of Counter 0.
OUT 0	10	O	**OUTPUT 0:** Output of Counter 0.
GATE 0	11	I	**GATE 0:** Gate input of Counter 0.
GND	12		**GROUND:** Power supply connection.
V_{CC}	24		**POWER:** +5V power supply connection.
$\overline{WR}$	23	I	**WRITE CONTROL:** This input is low during CPU write operations.
$\overline{RD}$	22	I	**READ CONTROL:** This input is low during CPU read operations.
$\overline{CS}$	21	I	**CHIP SELECT:** A low on this input enables the 8254 to respond to $\overline{RD}$ and $\overline{WR}$ signals. $\overline{RD}$ and $\overline{WR}$ are ignored otherwise.
A_1, A_0	20–19	I	**ADDRESS:** Used to select one of the three Counters or the Control Word Register for read or write operations. Normally connected to the system address bus.

A_1	A_0	Selects
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Word Register

CLK 2	18	I	**CLOCK 2:** Clock input of Counter 2.
OUT 2	17	O	**OUT 2:** Output of Counter 2.
GATE 2	16	I	**GATE 2:** Gate input of Counter 2.
CLK 1	15	I	**CLOCK 1:** Clock input of Counter 1.
GATE 1	14	I	**GATE 1:** Gate input of Counter 1.
OUT 1	13	O	**OUT 1:** Output of Counter 1.

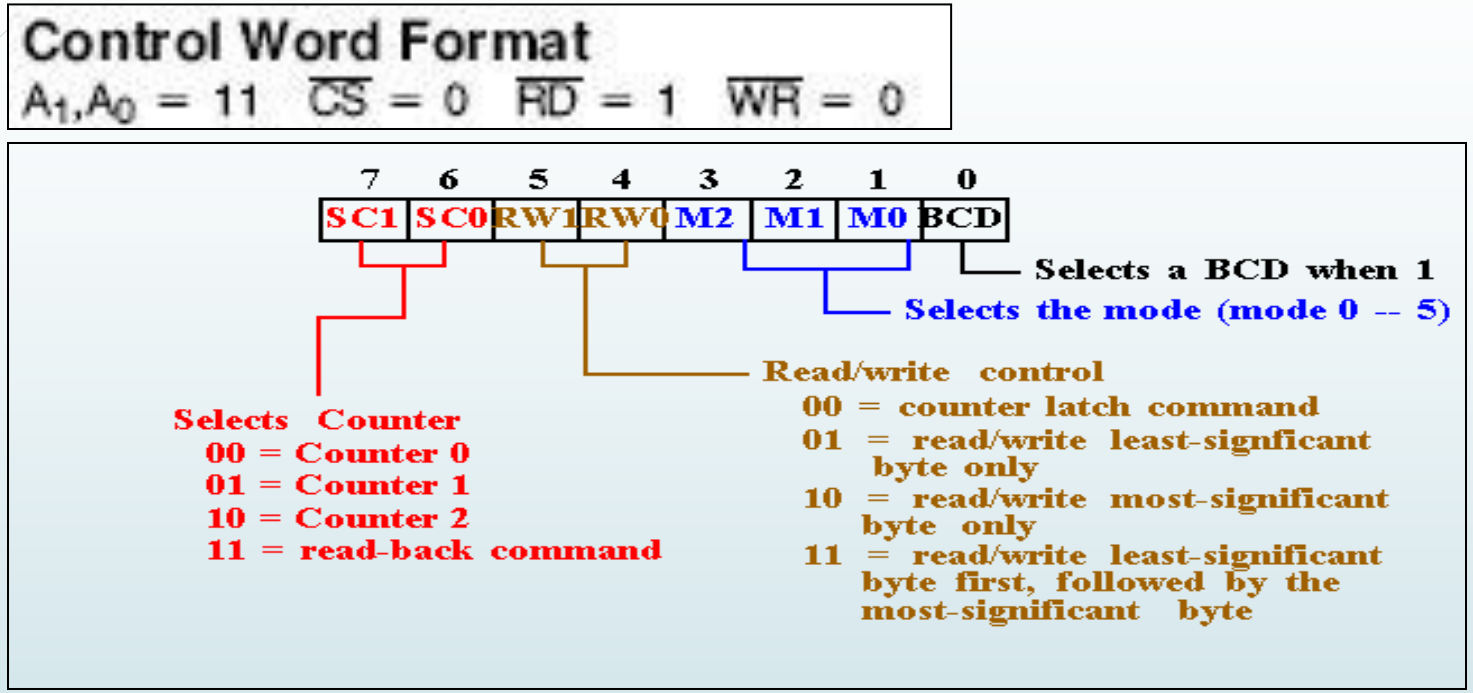
Block Diagram of 8254



Internal Blocks of Counter

- Count Register (CR) to store count (CRL & CRM),
- Counting elements (CE) are used for counting,
- Output Latch (OLL & OLM) to latch the count in CE,
- The Control Word Register is not part of the Counter itself, but its contents determine how the Counter operates.
- The status register, when latched, contains the current contents of the Control Word Register and status of the output and null count flag.

Control Word format



8254 Programming

- Each counter is individually programmed by writing a control word, followed by the initial count.
- The control word allows the programmer to select the counter, mode of operation, binary or BCD count and type of operation (read/write).

Interleaved Read and Write Operations

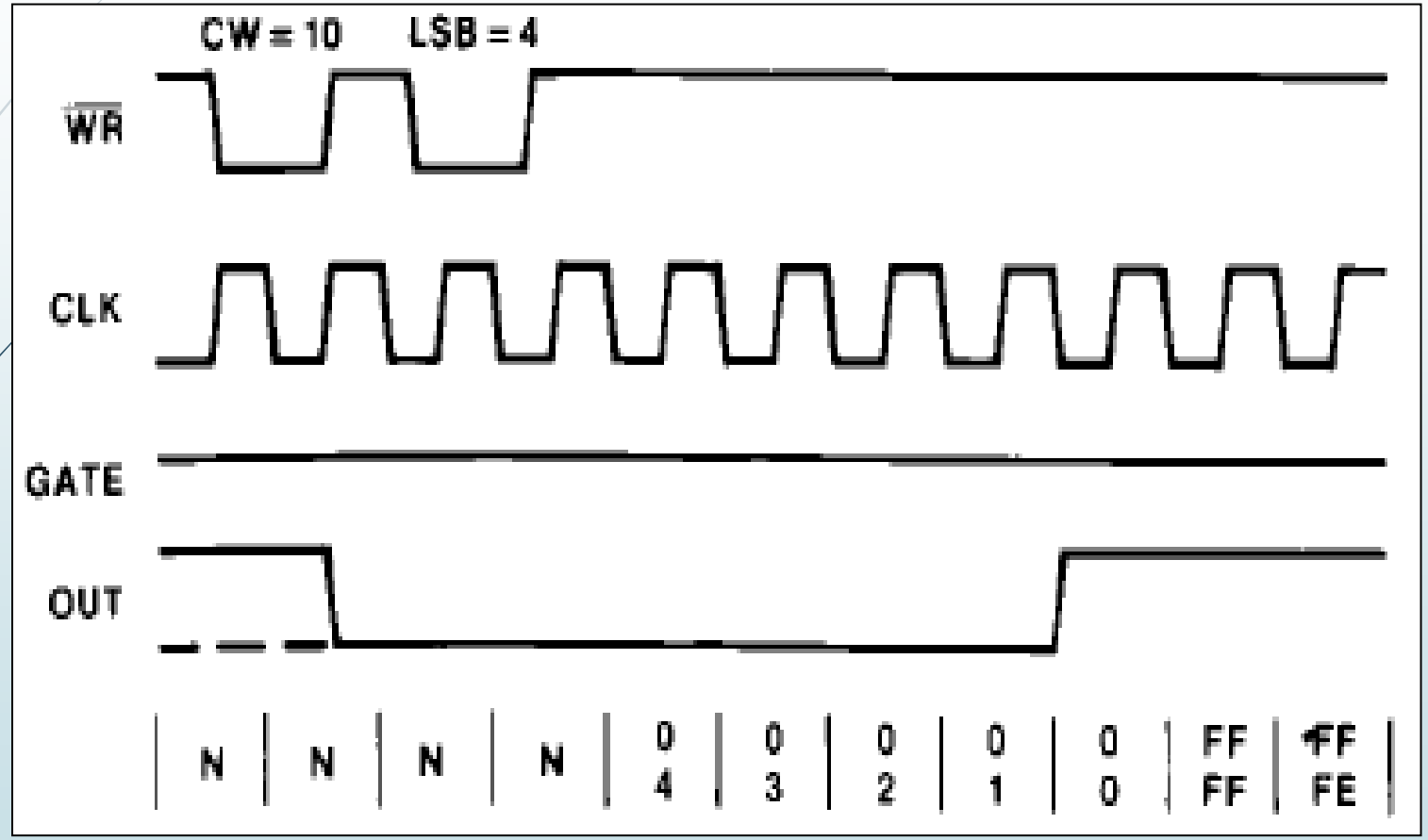
Valid sequence for read and write of the same counter set for two byte count:

1. Read least significant byte,
2. Write new least significant byte,
3. Read most significant byte,
4. Write new most significant byte.

6 Modes of 8254

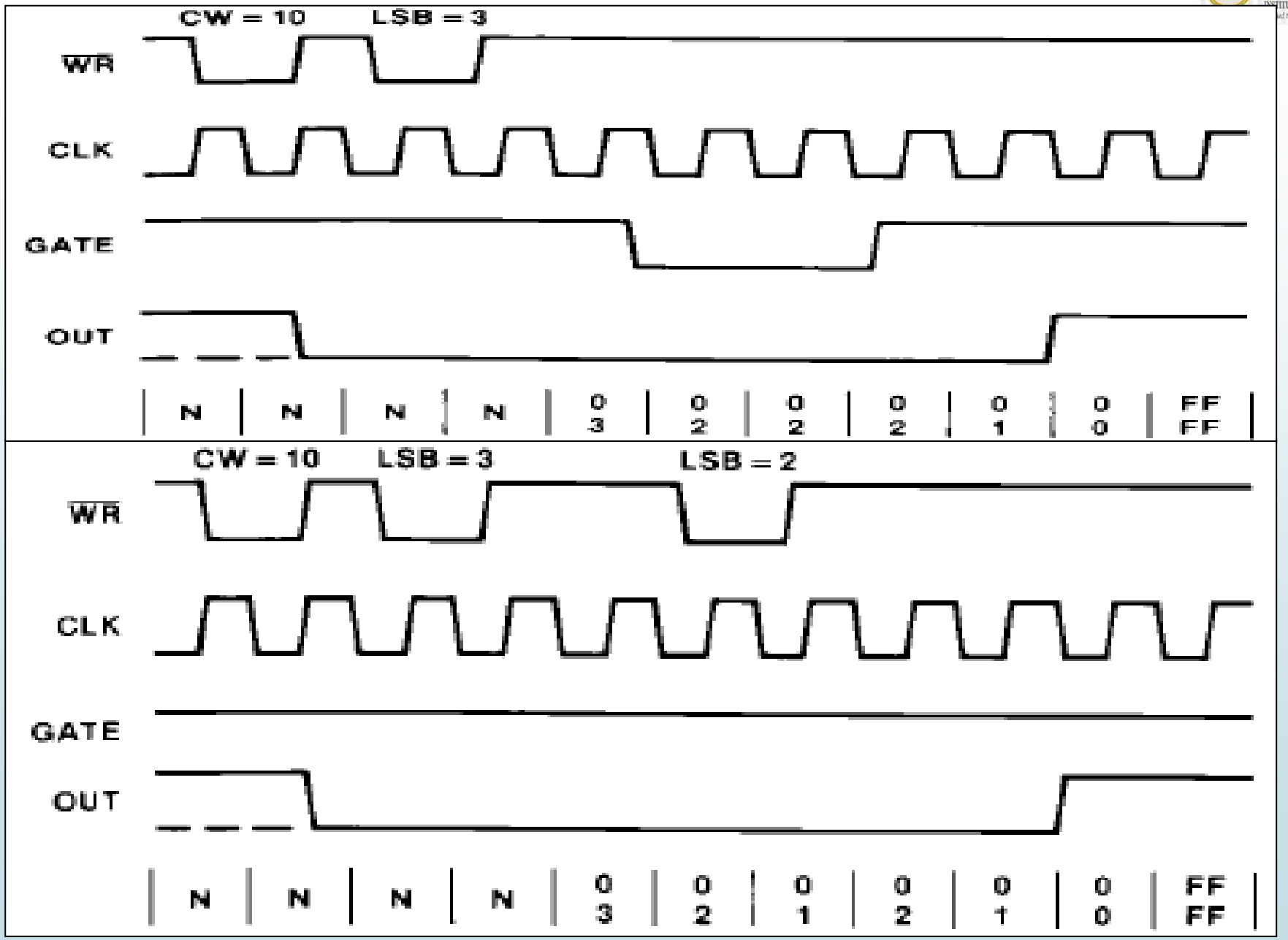
- Mode 0: Interrupt On Terminal Count
- Mode 1: Hardware Retriggerable One-shot
- Mode 2: Rate Generator
- Mode 3: Square Wave Mode
- Mode 4: Software Triggered Strobe
- Mode 5: Hardware Triggered Strobe (Retriggerable)

MODE 0 – Interrupt on Terminal Count

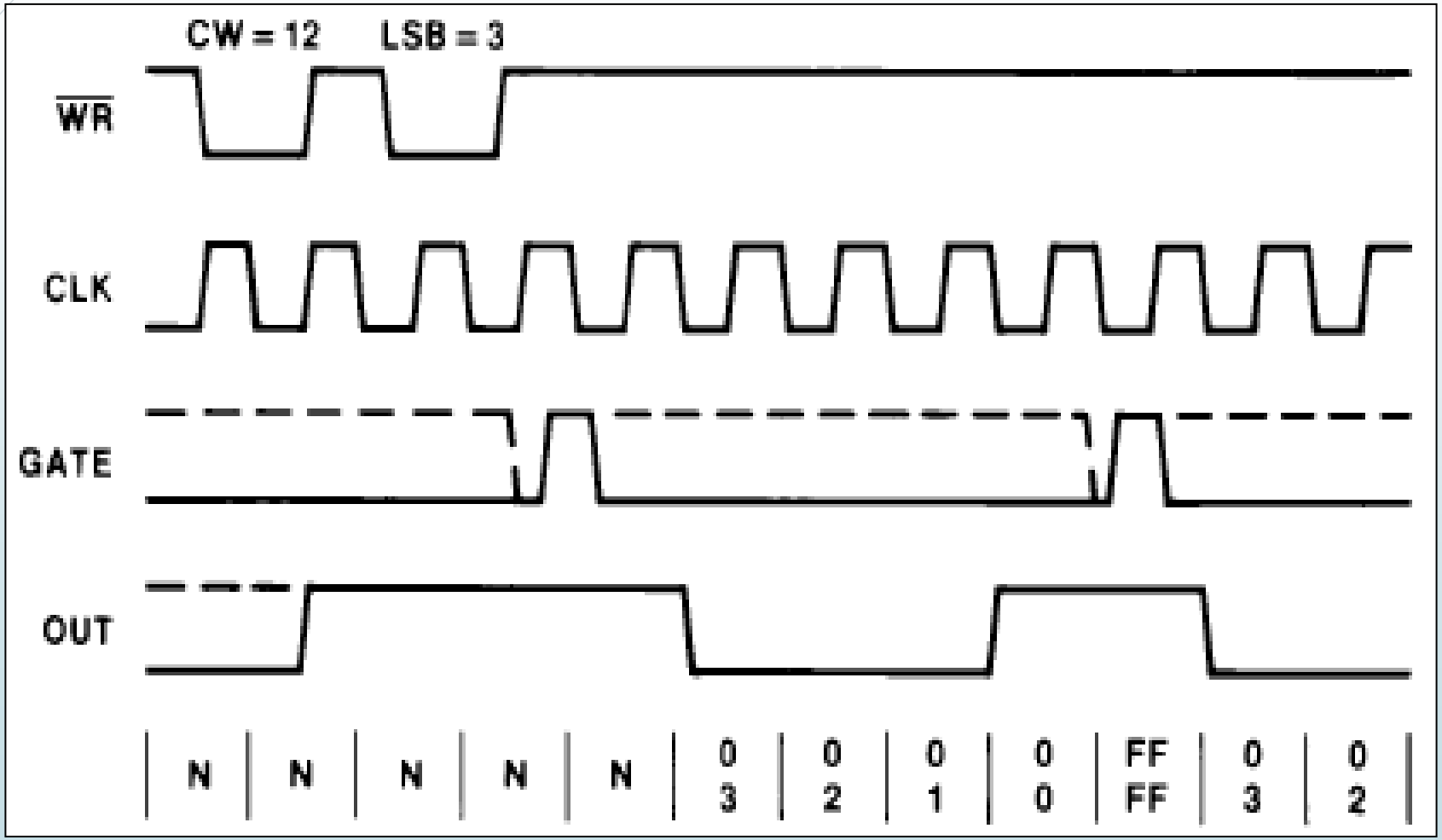


N : Undefined Count

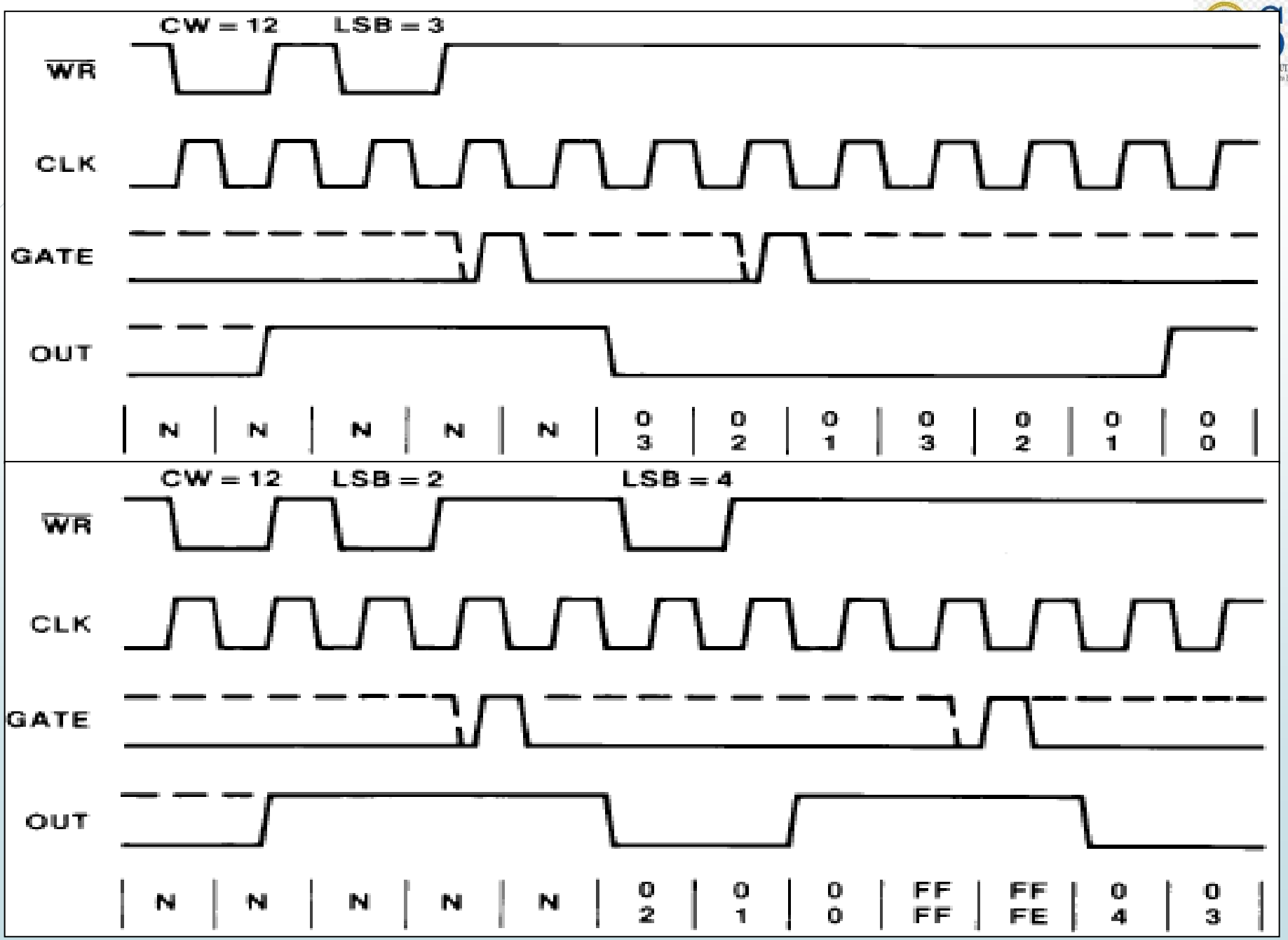
MODE 0
contd...


CW = 10
LSB = 3
WR
CLK
GATE
OUT
N N N N 03 02 02 02 01 00 FF FF
CW = 10
LSB = 3
LSB = 2
WR
CLK
GATE
OUT
N N N N 03 02 01 02 01 00 FF FF

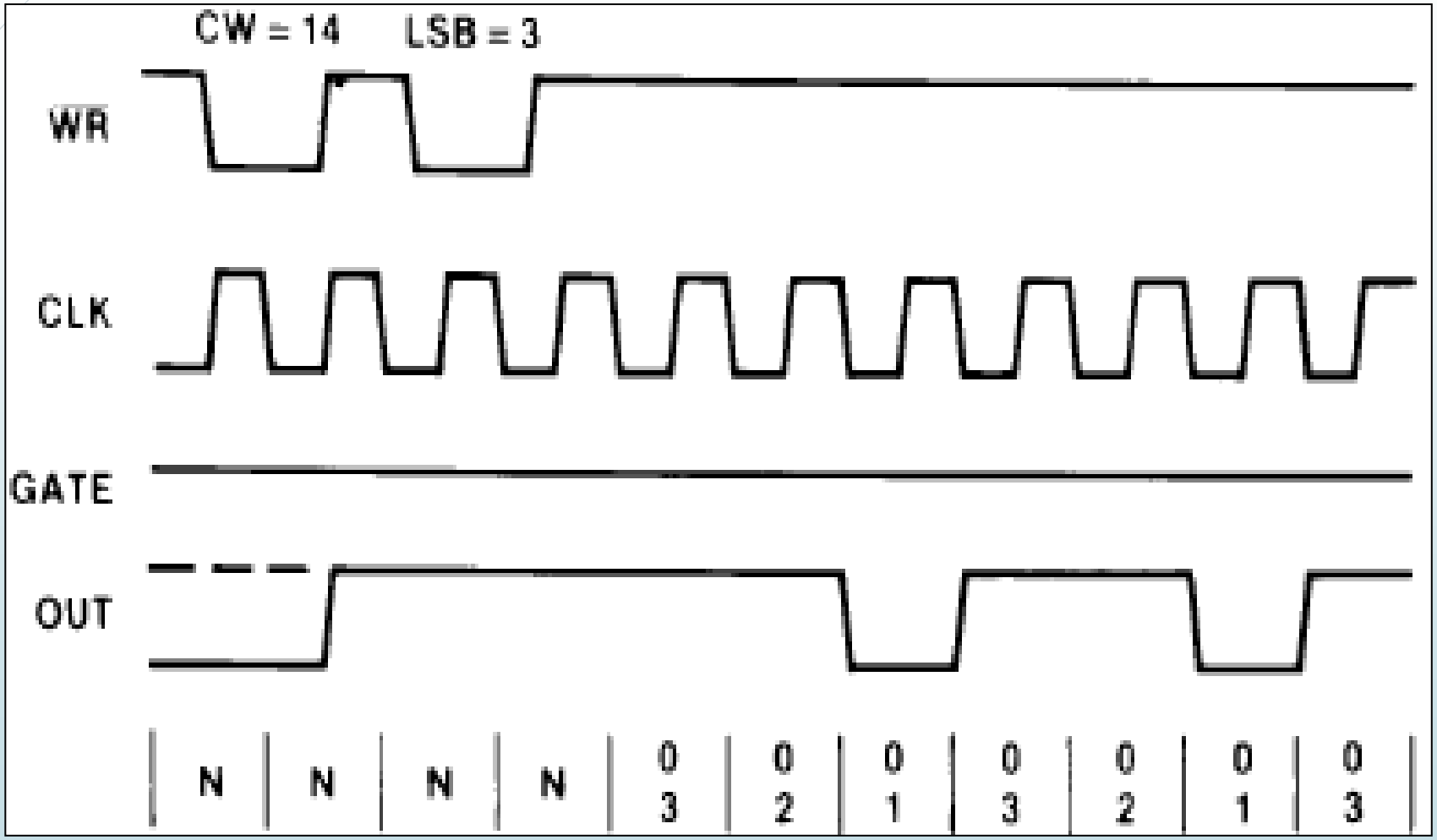
MODE 1: Hardware Retriggerable One Shot.



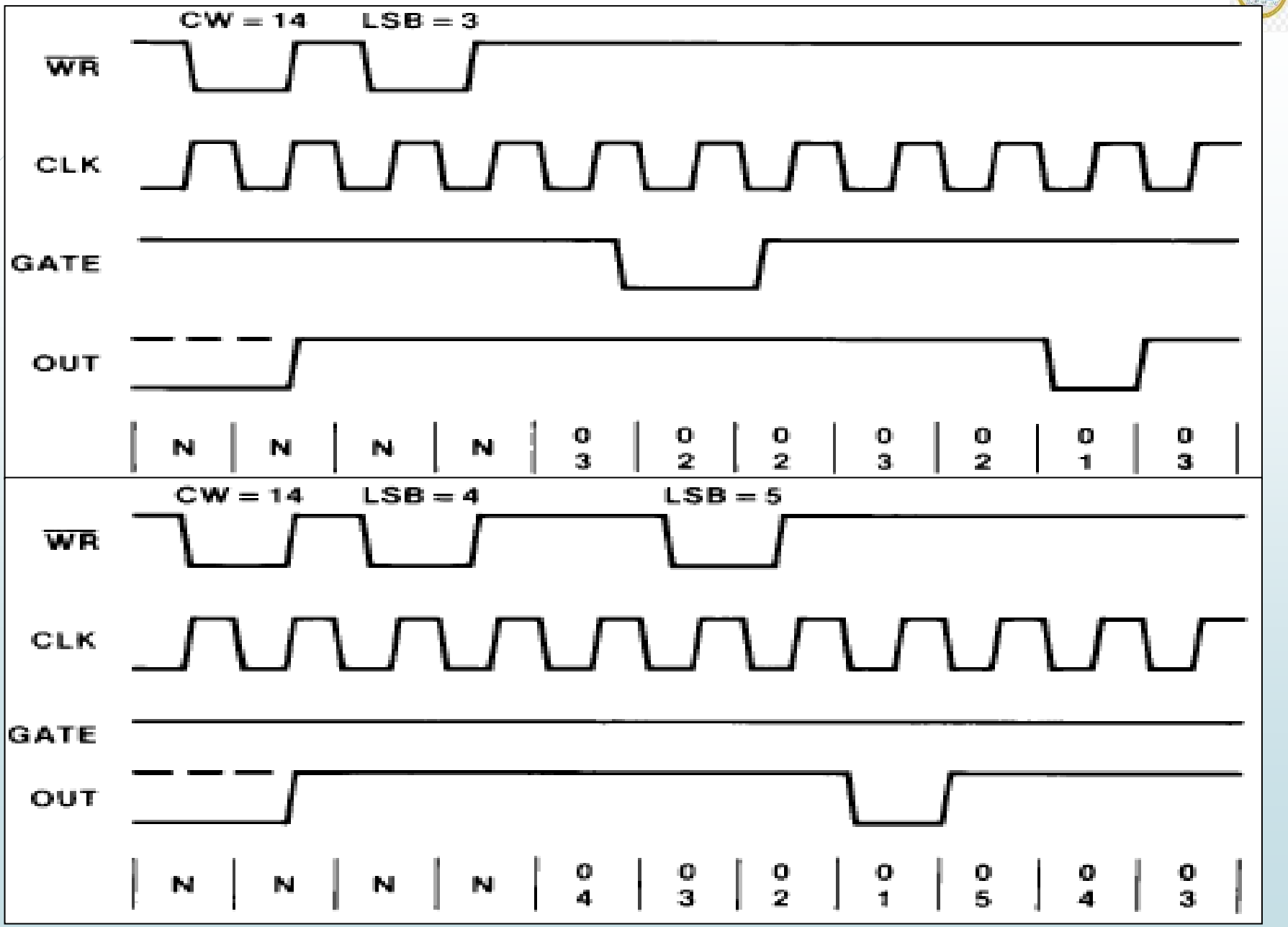
MODE 1
contd...


CW = 12
LSB = 3
WR
CLK
GATE
OUT
N N N N N 03 02 01 03 02 01 00
CW = 12
LSB = 2
LSB = 4
WR
CLK
GATE
OUT
N N N N N 02 01 00 FF FF FE 04 03

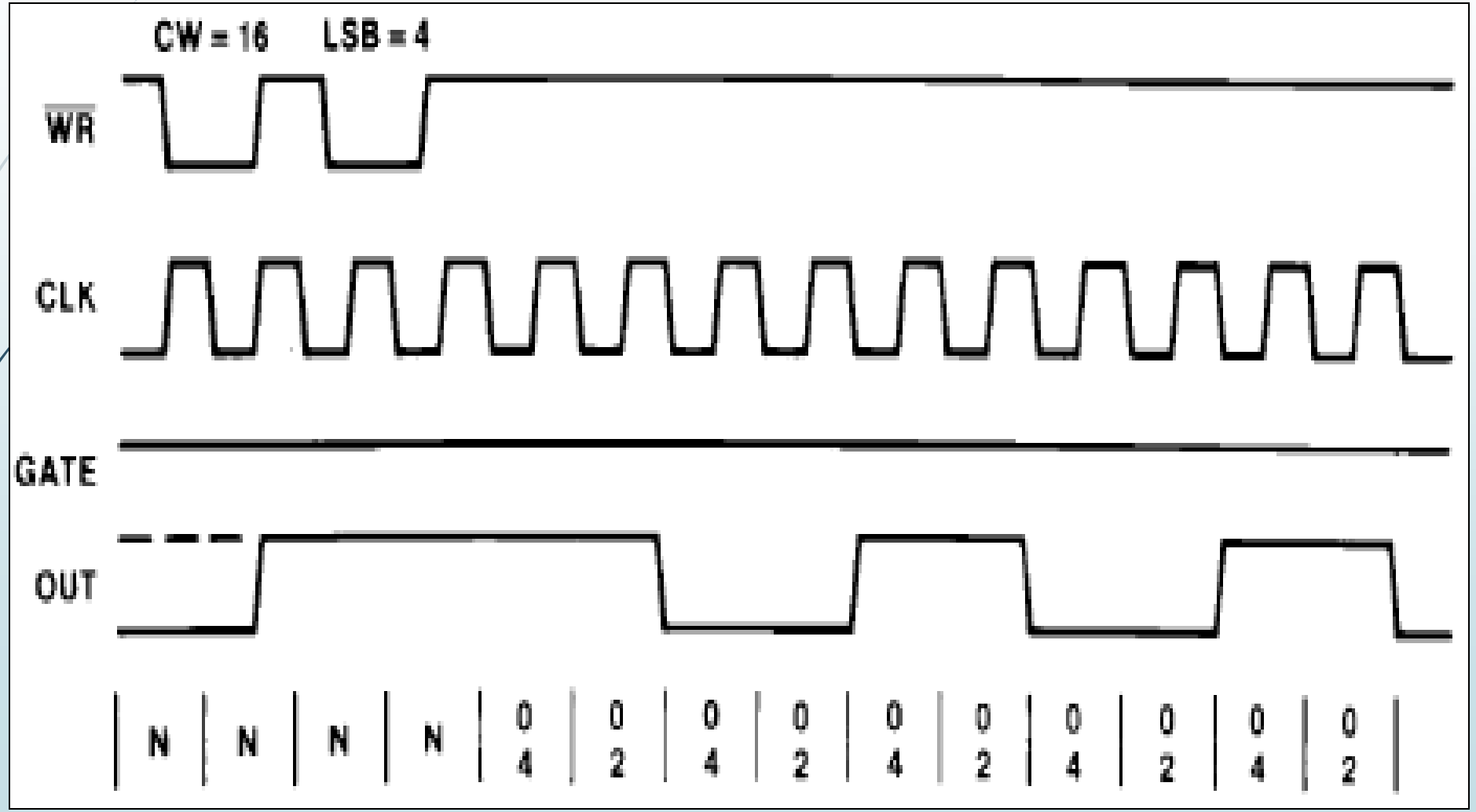
MODE 2: Rate Generator



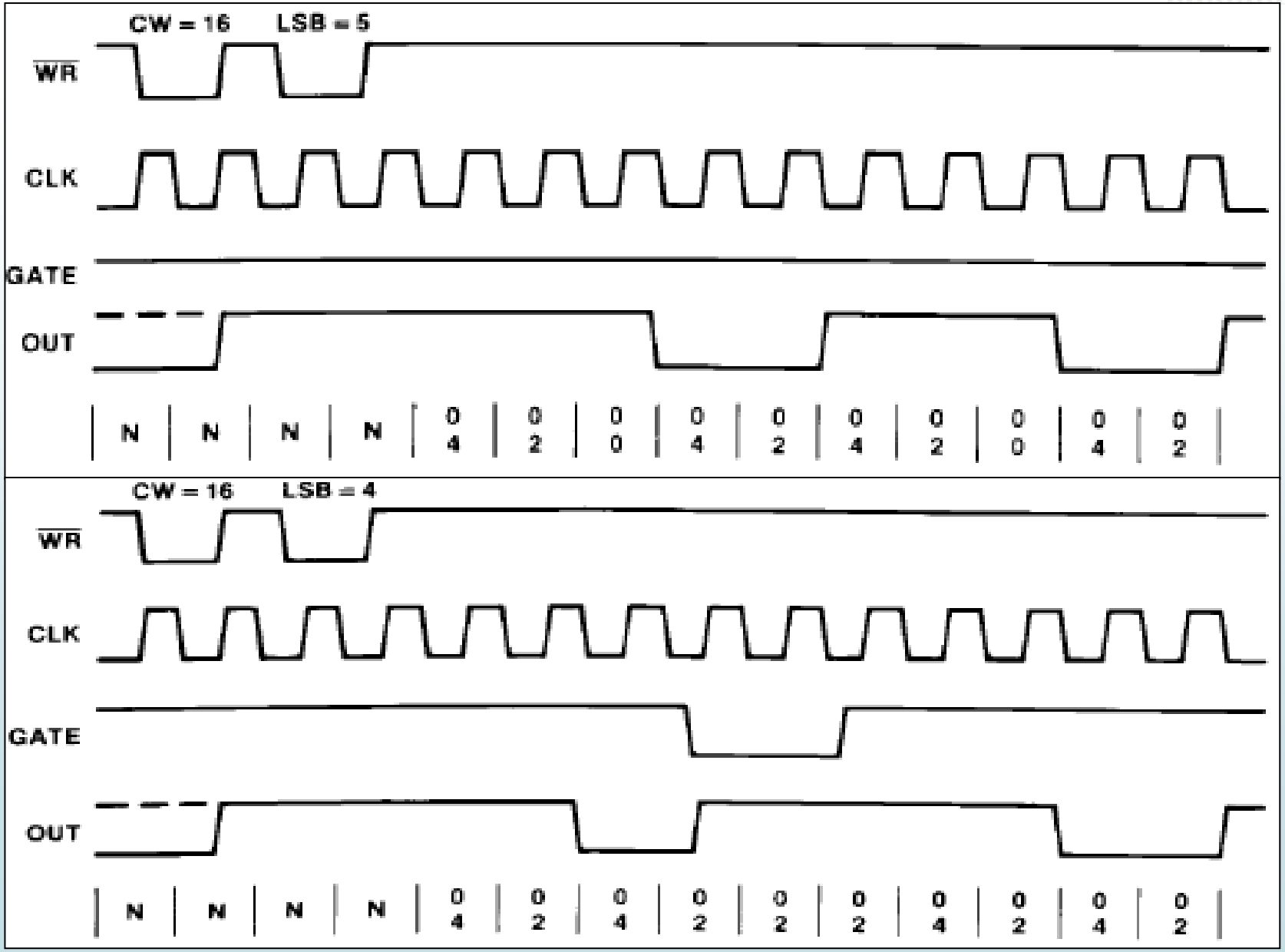
MODE 2
contd...


CW = 14
LSB = 3
WR
CLK
GATE
OUT
N N N N 03 02 02 03 02 01 03
CW = 14
LSB = 4
LSB = 5
WR
CLK
GATE
OUT
N N N N 04 03 02 01 05 04 03

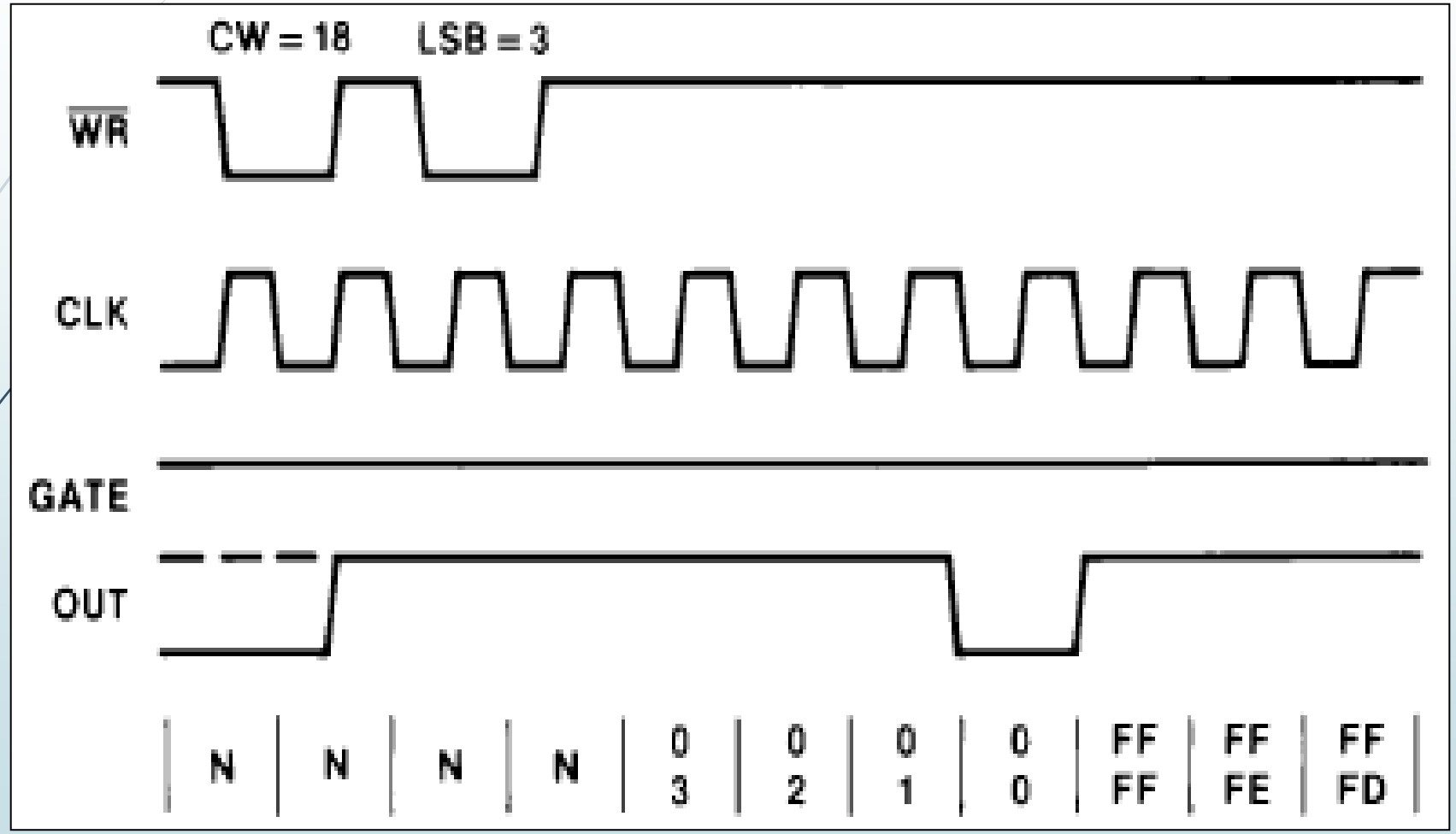
MODE 3: Square Wave Mode



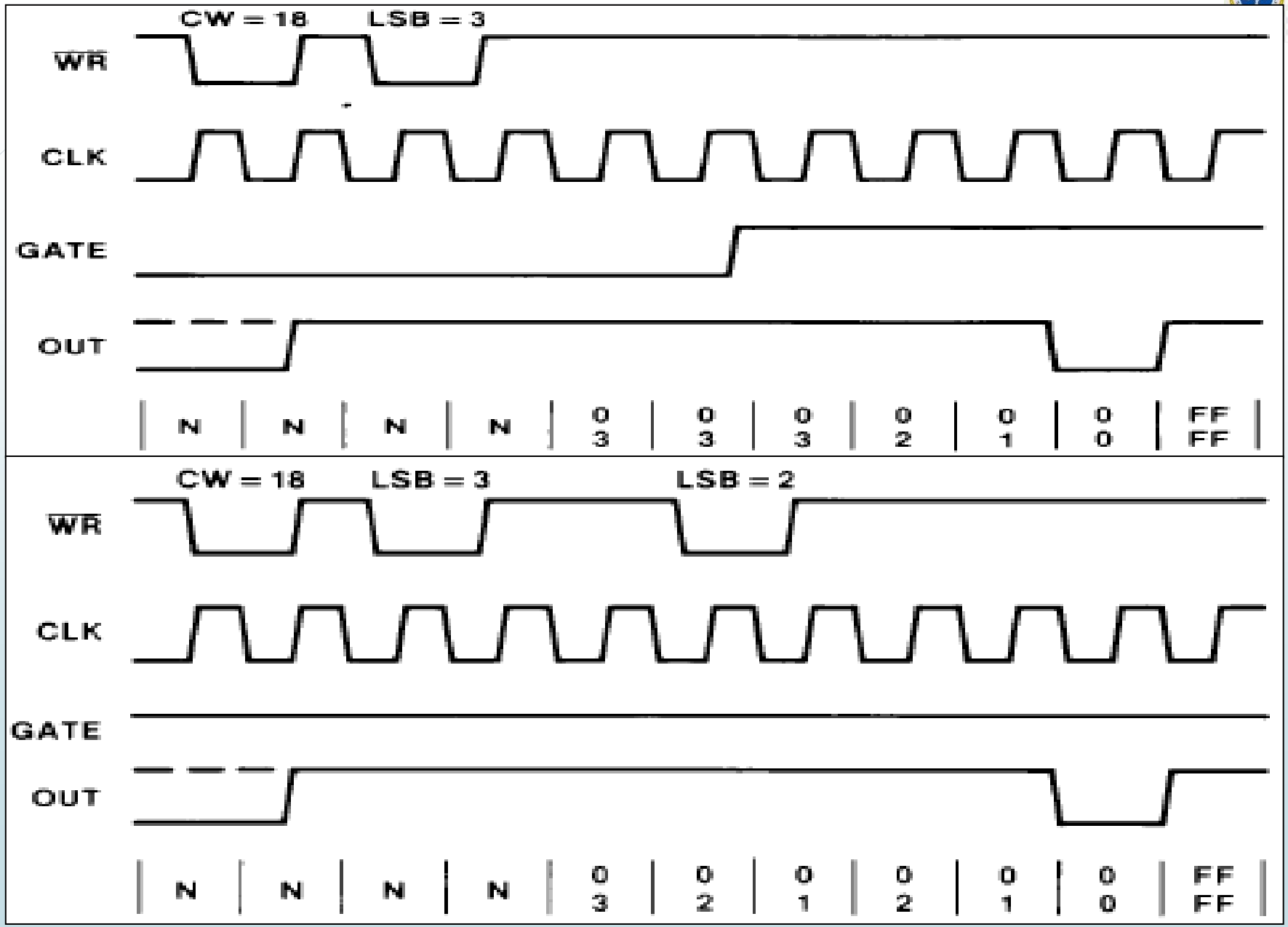
MODE 3
contd...


CW = 16
LSB = 5
WR
CLK
GATE
OUT
N N N N 04 02 00 04 02 04 02 00 04 02
CW = 16
LSB = 4
WR
CLK
GATE
OUT
N N N N 04 02 04 02 02 02 04 02 04 02

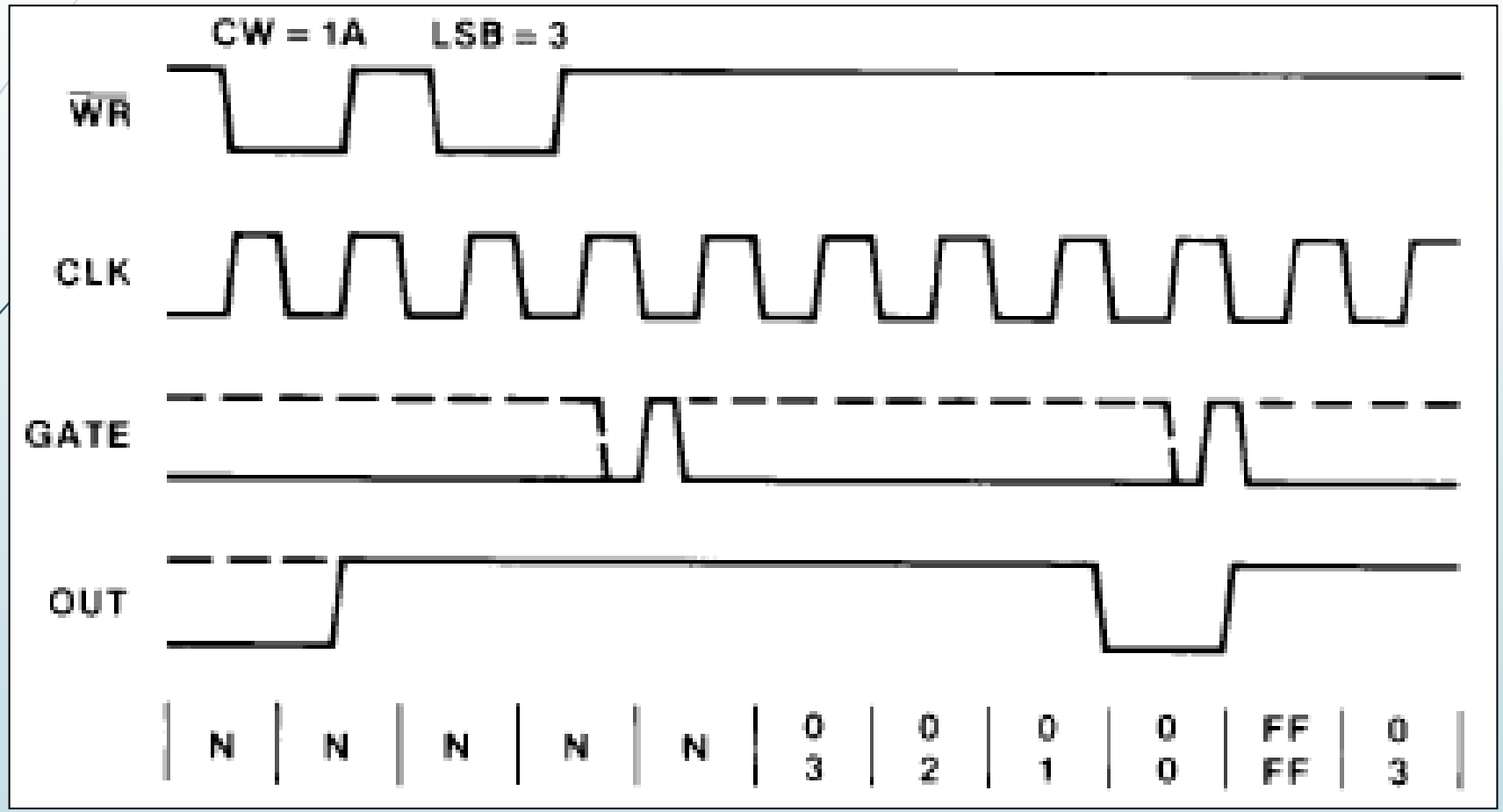
MODE 4: Software Triggered Strobe



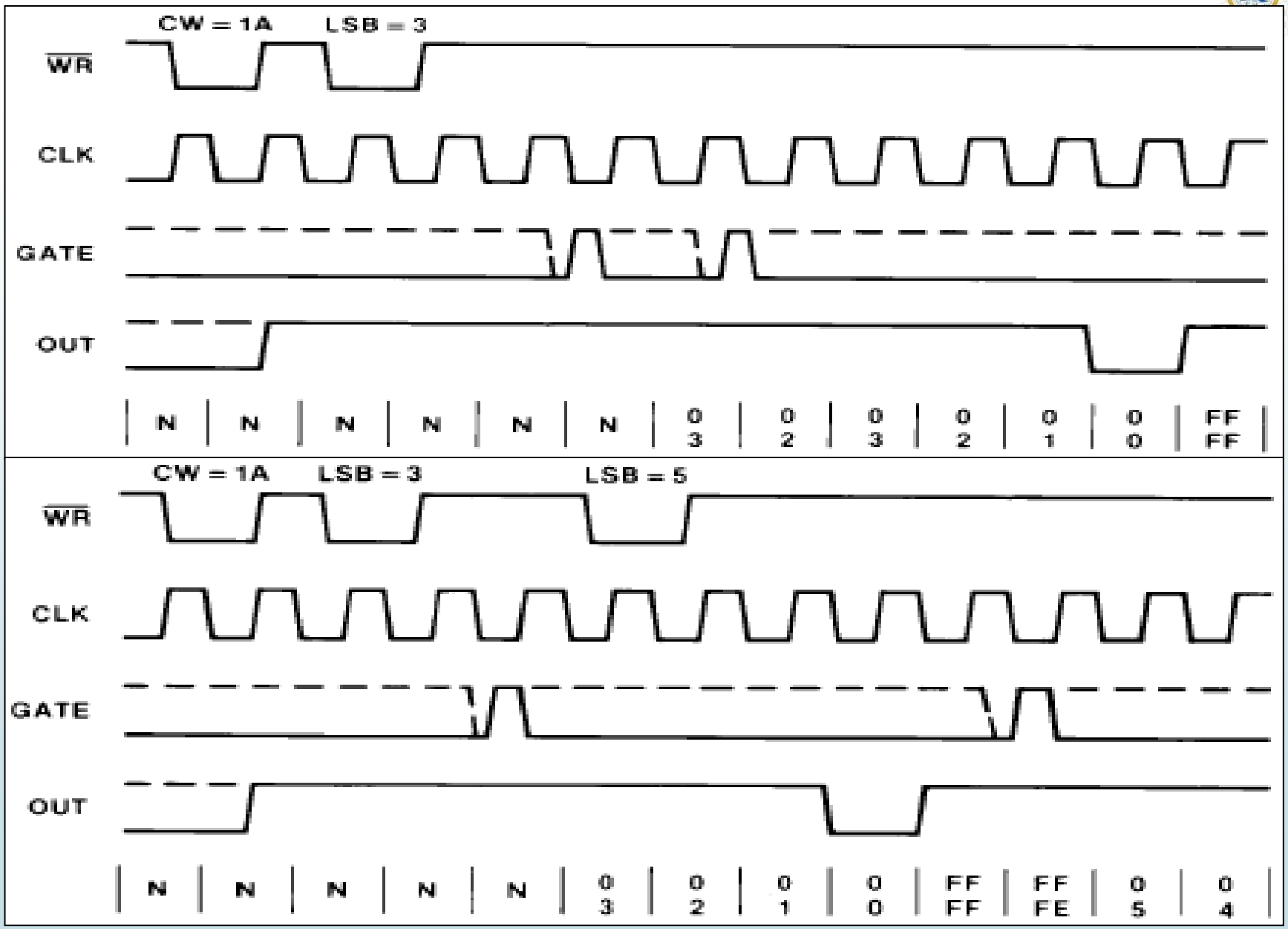
MODE 4
contd...


CW = 18
LSB = 3
WR
CLK
GATE
OUT
N N N N 03 03 03 02 01 00 FF FF
CW = 18
LSB = 3
LSB = 2
WR
CLK
GATE
OUT
N N N N 03 02 01 02 01 00 FF FF

MODE 5 : Hardware Triggered Strobe



MODE 5
contd...


CW = 1A
LSB = 3
WR
CLK
GATE
OUT
N N N N N N 03 02 03 02 01 00 FF FF
CW = 1A
LSB = 3
LSB = 5
WR
CLK
GATE
OUT
N N N N N 03 02 01 00 FF FF FF FE 05 04

8254
contd...

Signal Status Modes	Low Or Going Low	Rising	High
0	Disables Counting	— —	Enables Counting
1	— —	1) Initiates Counting 2) Resets Output after Next Clock	— —
2	1) Disables Counting 2) Sets Output Immediately High	Initiates Counting	Enables Counting
3	1) Disables Counting 2) Sets Output Immediately High	Initiates Counting	Enables Counting
4	Disables Counting	— —	Enables Counting
5	— —	Initiates Counting	— —

Figure 21. Gate Pin Operations Summary

8254
contd...

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	
0	1	0	0	0	Write into Counter 0
0	1	0	0	1	Write into Counter 1
0	1	0	1	0	Write into Counter 2
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read from Counter 0
0	0	1	0	1	Read from Counter 1
0	0	1	1	0	Read from Counter 2
0	0	1	1	1	No-Operation (3-State)
1	X	X	X	X	No-Operation (3-State)
0	1	1	X	X	No-Operation (3-State)

Figure 14. Read/Write Operations Summary

Minimum & Maximum Initial Count

Mode	Min Count	Max Count
0	1	0
1	1	0
2	2	0
3	2	0
4	1	0
5	1	0

NOTE:
0 is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

Gate Pin Operations Summary

Signal Status Modes	Low Or Going Low	Rising	High
0	Disables Counting	— —	Enables Counting
1	— —	1) Initiates Counting 2) Resets Output after Next Clock	— —
2	1) Disables Counting 2) Sets Output Immediately High	Initiates Counting	Enables Counting
3	1) Disables Counting 2) Sets Output Immediately High	Initiates Counting	Enables Counting
4	Disables Counting	— —	Enables Counting
5	— —	Initiates Counting	— —

Applications of 8254

- Real time clock
- Event-counter
- Digital one-shot
- Programmable rate generator
- Square wave generator
- Binary rate multiplier
- Complex waveform generator
- Complex motor controller

S – 8

Programmable Interrupt Controller 8259 & Interfacing 8259 with 8086 and programming

Programmable Interrupt Controller 8259

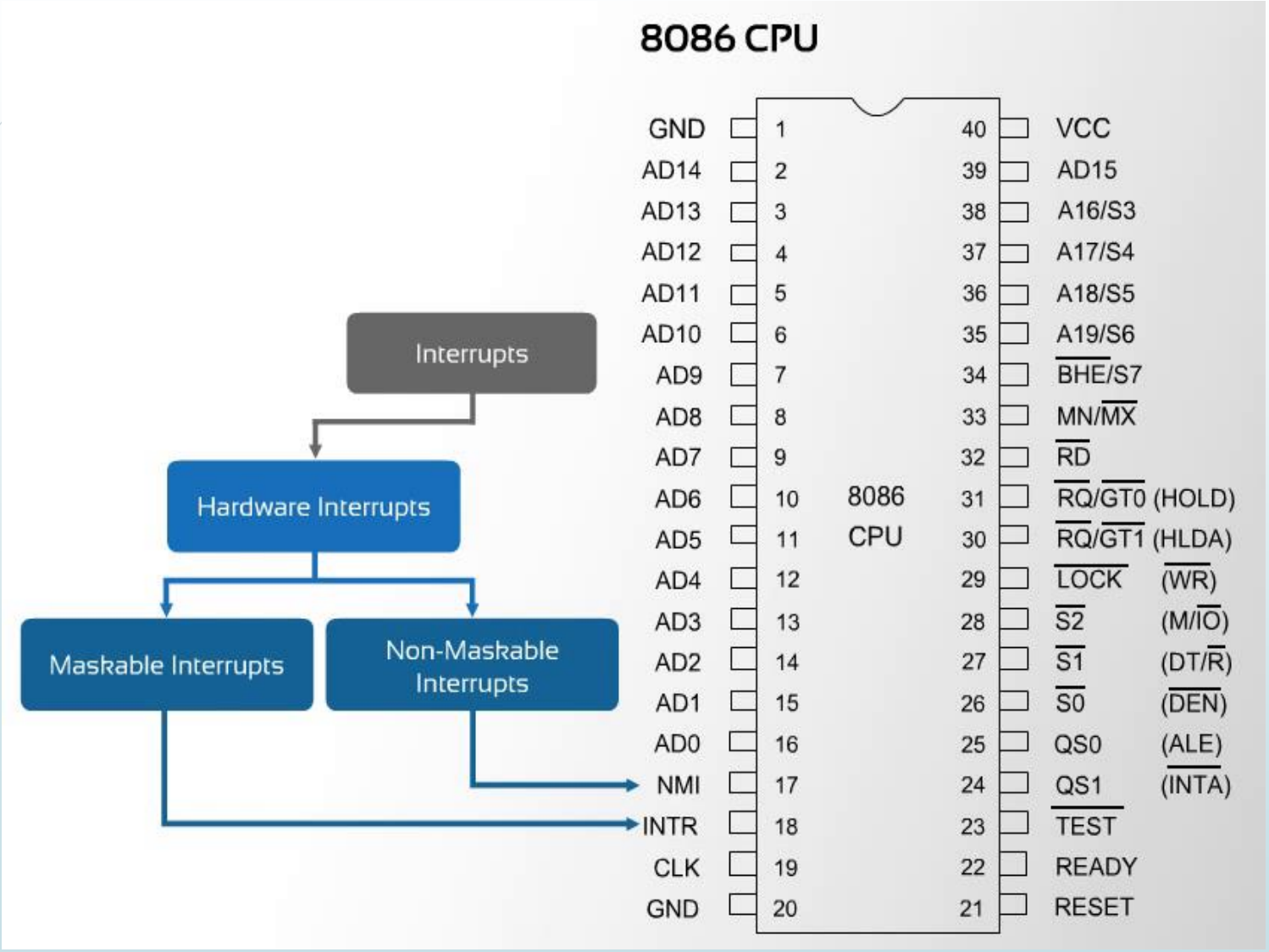


Image Courtesy: Google

8259 Programmable Interrupt Controller (PIC)

1. This IC is designed to simplify the implementation of the interrupt interface in the 8088 and 8086 based microcomputer systems.
2. This device is known as a 'Programmable Interrupt Controller' or PIC.
3. It is manufactured using the NMOS technology and It is available in 28-pin DIP.
4. The operation of the PIC is programmable under software control (Programmable)and it can be configured for a wide variety of applications.
5. 8259A is treated as peripheral in a microcomputer system.
6. 8259A PIC adds eight vectored priority encoded interrupts to the microprocessor.

8259 Programmable Interrupt Controller (PIC) (2)

7. This controller can be expanded without additional hardware to accept up to 64 interrupt request inputs. This expansion required a master 8259A and eight 8259A slaves.
8. Some of its programmable features are:
   - The ability to accept level-triggered or edge-triggered inputs.
   - The ability to be easily cascaded to expand from 8 to 64 interrupt-inputs.
   - Its ability to be configured to implement a wide variety of priority schemes.

Assignment of Signals for 8259

1. **$D_7 - D_0$** – Connected to microprocessor data bus ($AD_7 - AD_0$).
2. **$IR_7 - IR_0$** – Interrupt Request inputs are used to request an interrupt and to connect to a slave in a system with multiple 8259As.
3. **$\overline{WR}$** - the write input connects to write strobe signal of microprocessor.
4. **$\overline{RD}$** - the read input connects to the IORC signal.
5. **INT** - the interrupt output connects to the INTR pin on the microprocessor from the master, and is connected to a master IR pin on a slave.
6. **$\overline{INTA}$** - the interrupt acknowledge is an input that connects to the INTA signal on the system. In a system with a master and slaves, only the master INTA signal is connected.

Assignment of Signals for 8259 (2)

1. **A_0 -** this address input selects different command words within the 8259A.

2. **$\overline{CS}$** - chip select enables the 8259A for programming and control.

3. **$\overline{PS}$ / $\overline{EN}$ -** Slave Program/Enable Buffer is a dual-function pin.
   - ❖ When the 8259A is in buffered mode, this pin is an output that controls the data bus transceivers in a large microprocessor-based system.
   - ❖ When the 8259A is not in buffered mode, this pin programs the device as a master (1) or a slave (0).

4. **CAS_2 – CAS_0** , the cascade lines are used as outputs from the master to the slaves for cascading multiple 8259As in a system.

8259A PIC- Block Diagram

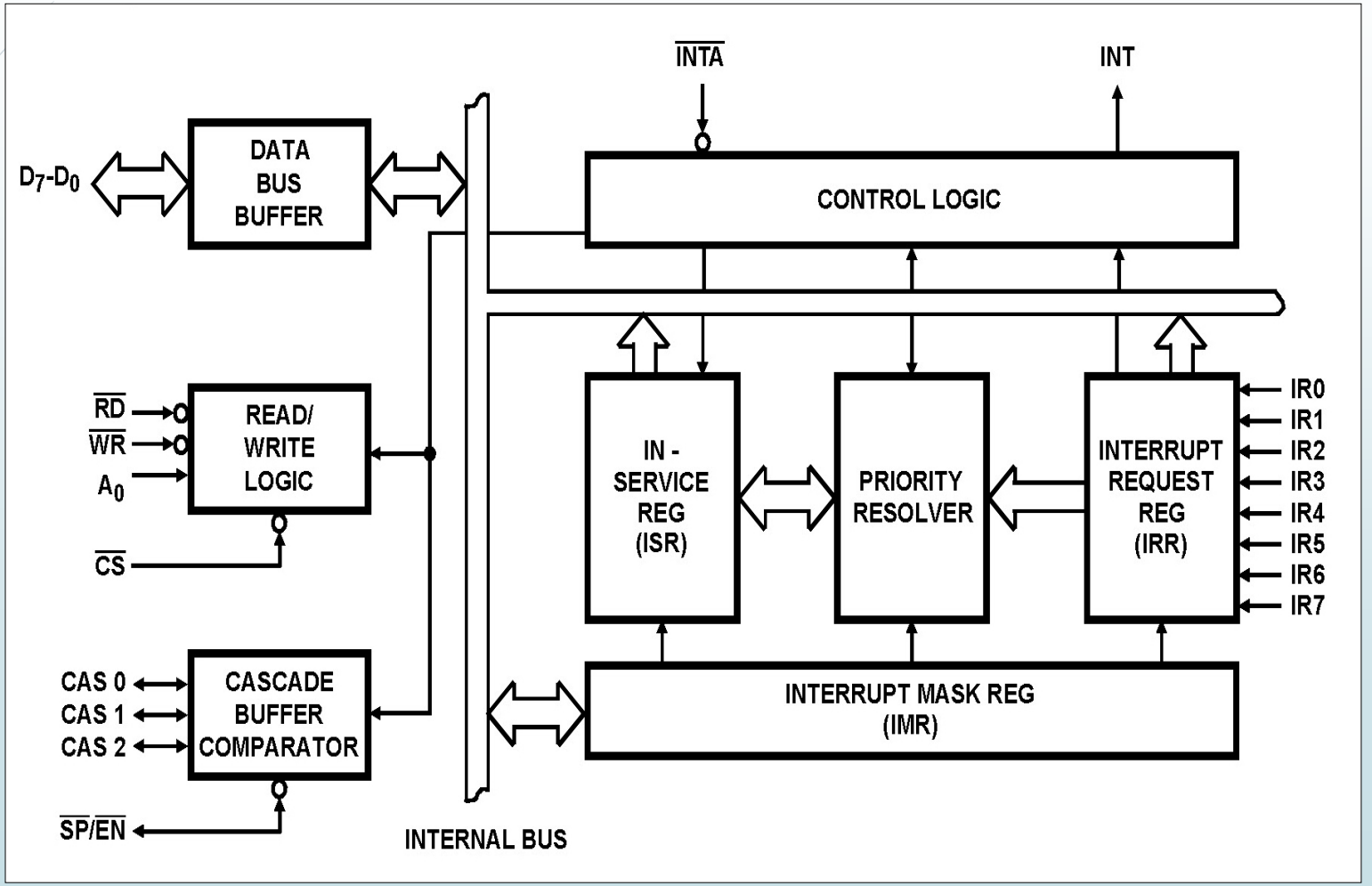


Image Courtesy: Google

8259A - Internals (1/4)

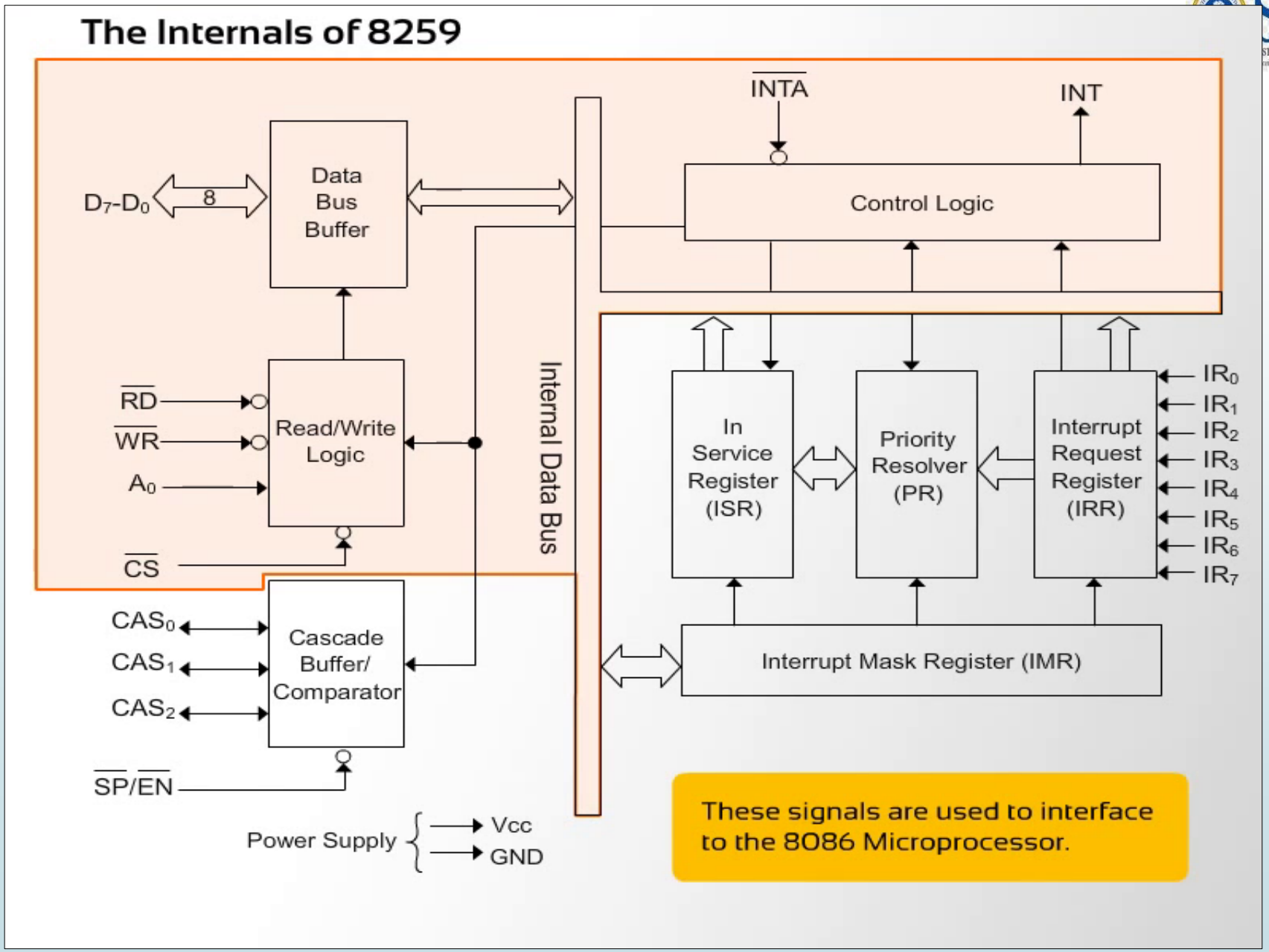


Image Courtesy: Google

8259A - Internals (2/4)

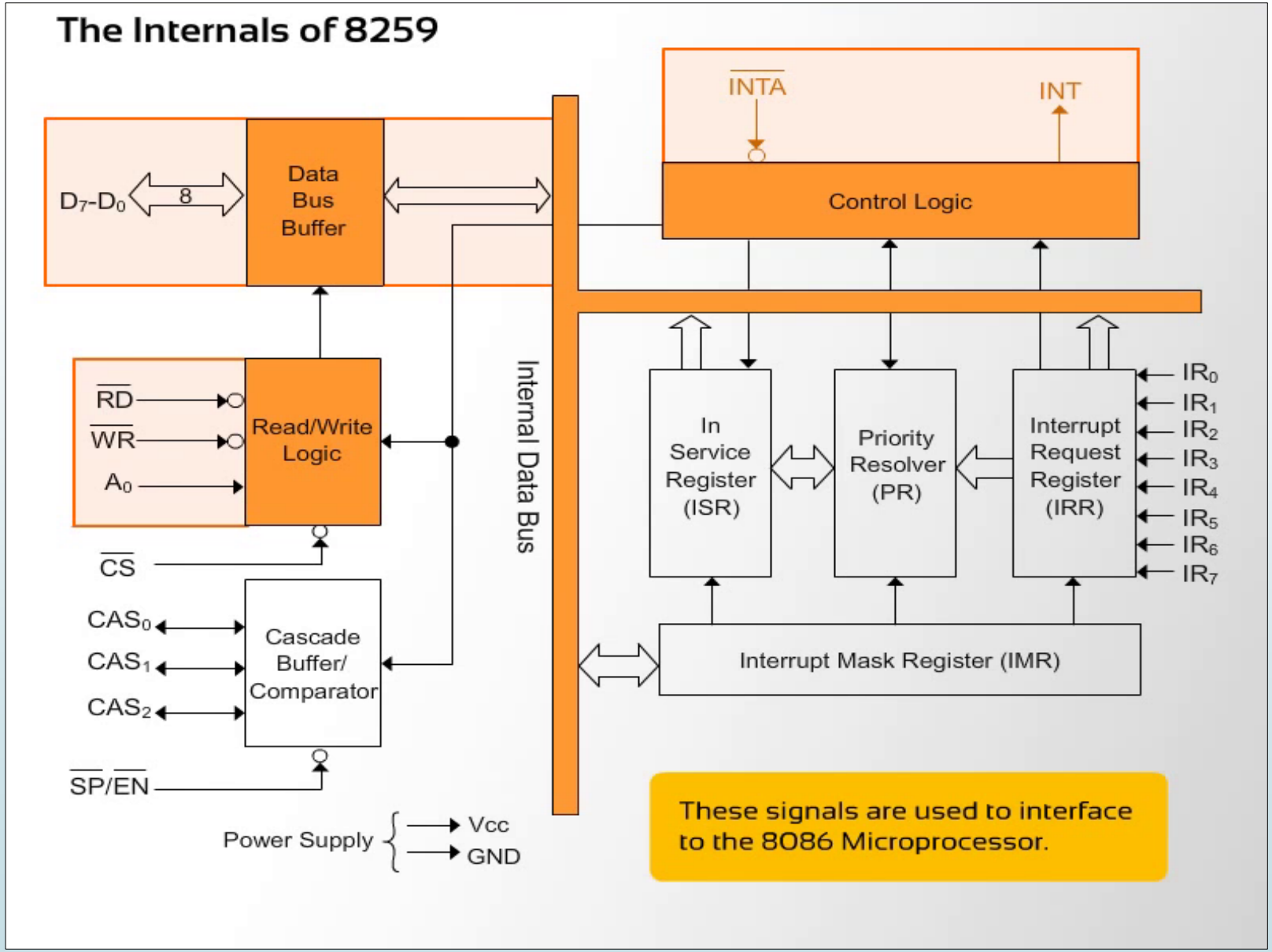


Image Courtesy: Google

8259A - Internals (3/4)

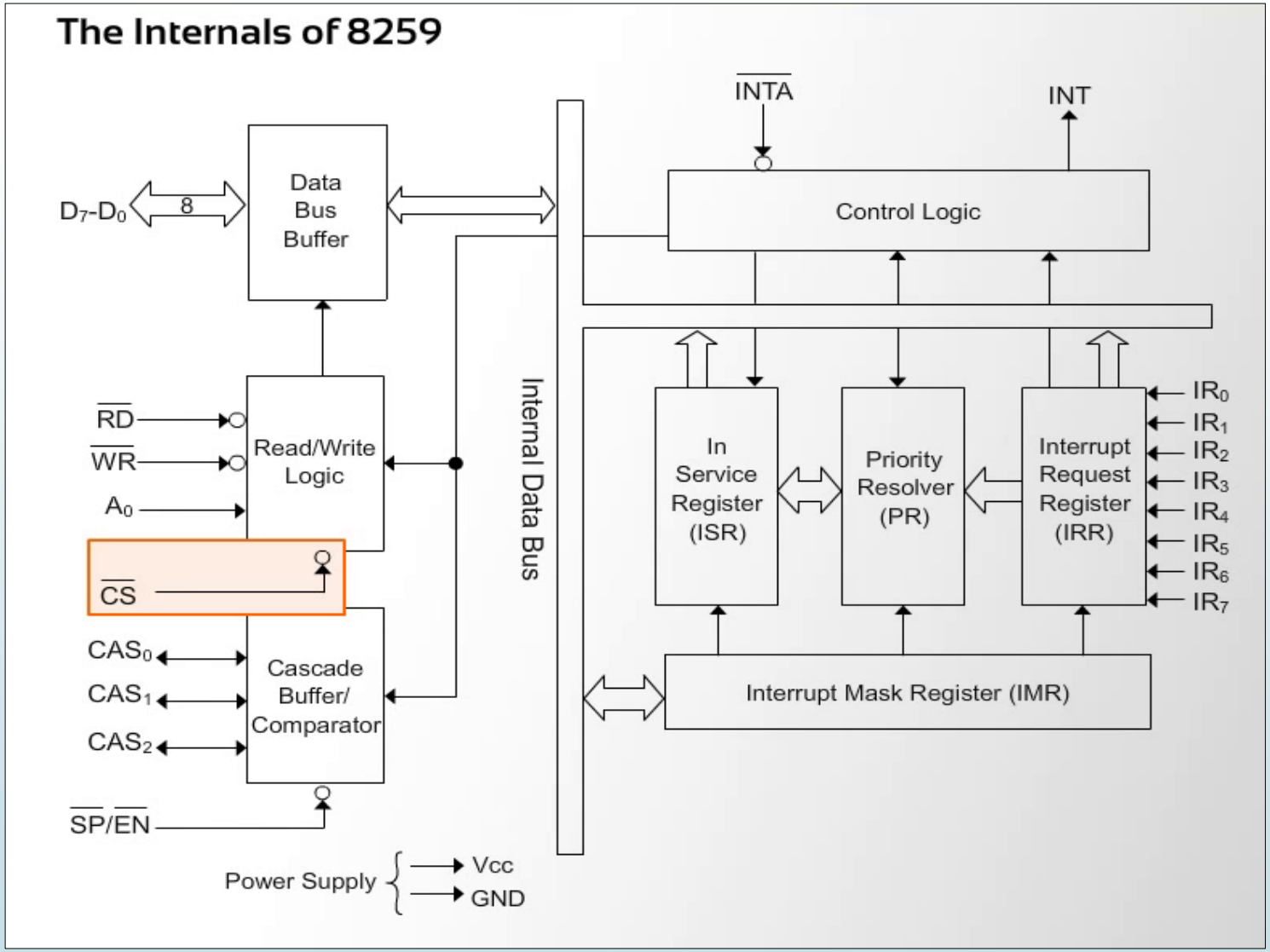


Image Courtesy: Google

8259A - Internals (4/4)

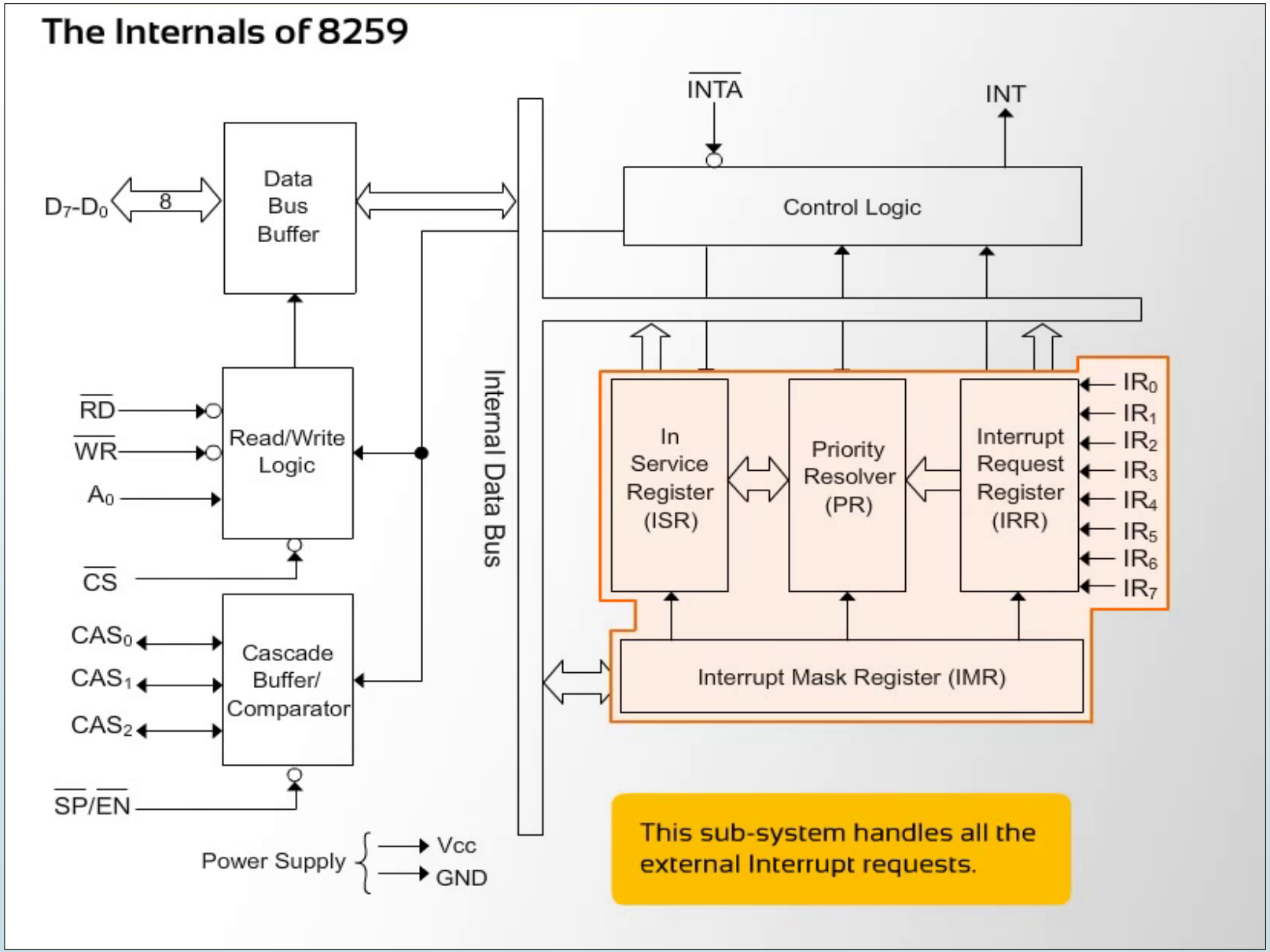


Image Courtesy: Google

8259A - Internals (IPR)

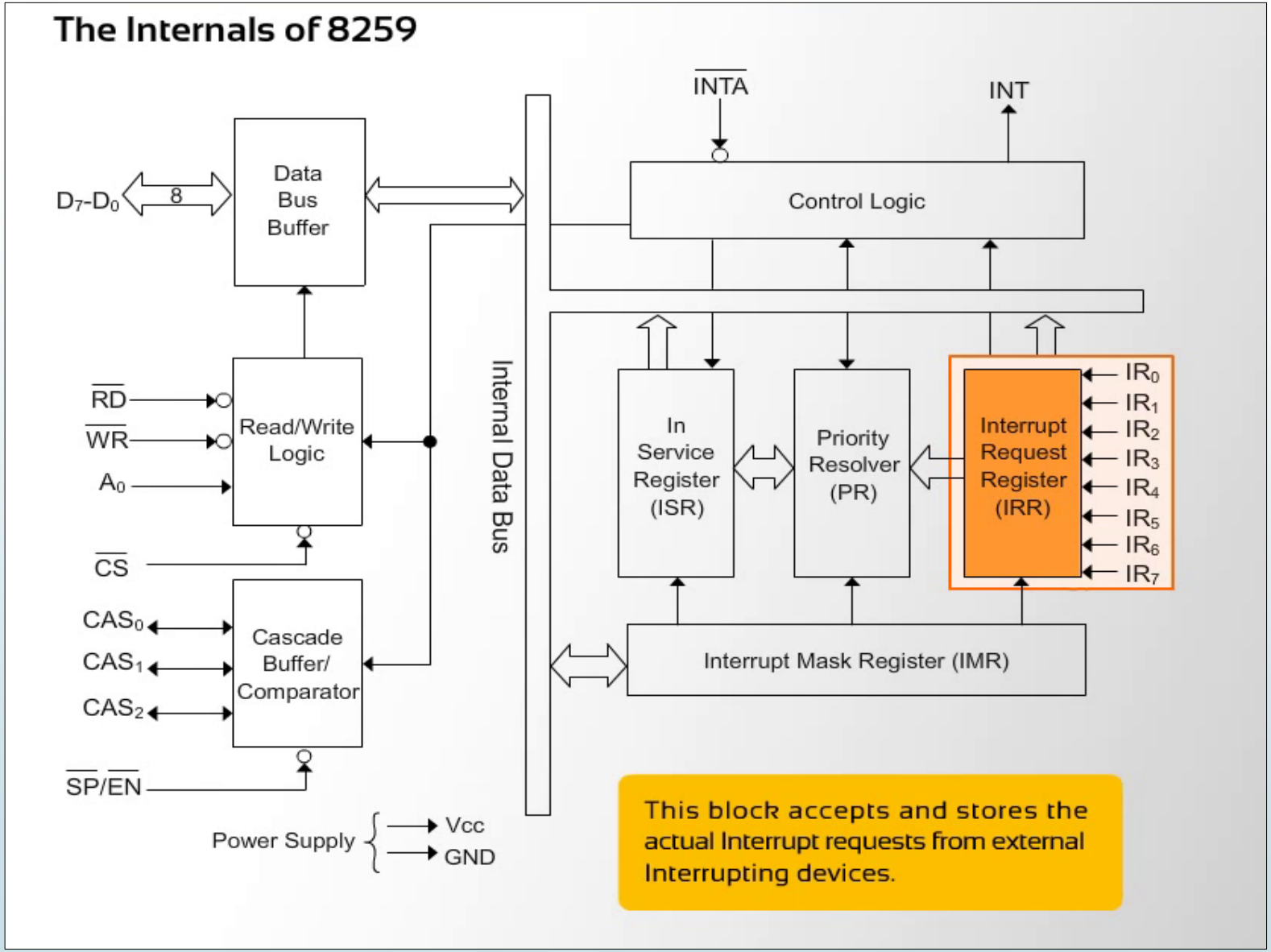


Image Courtesy: Google

8259A - Internals (ISR)

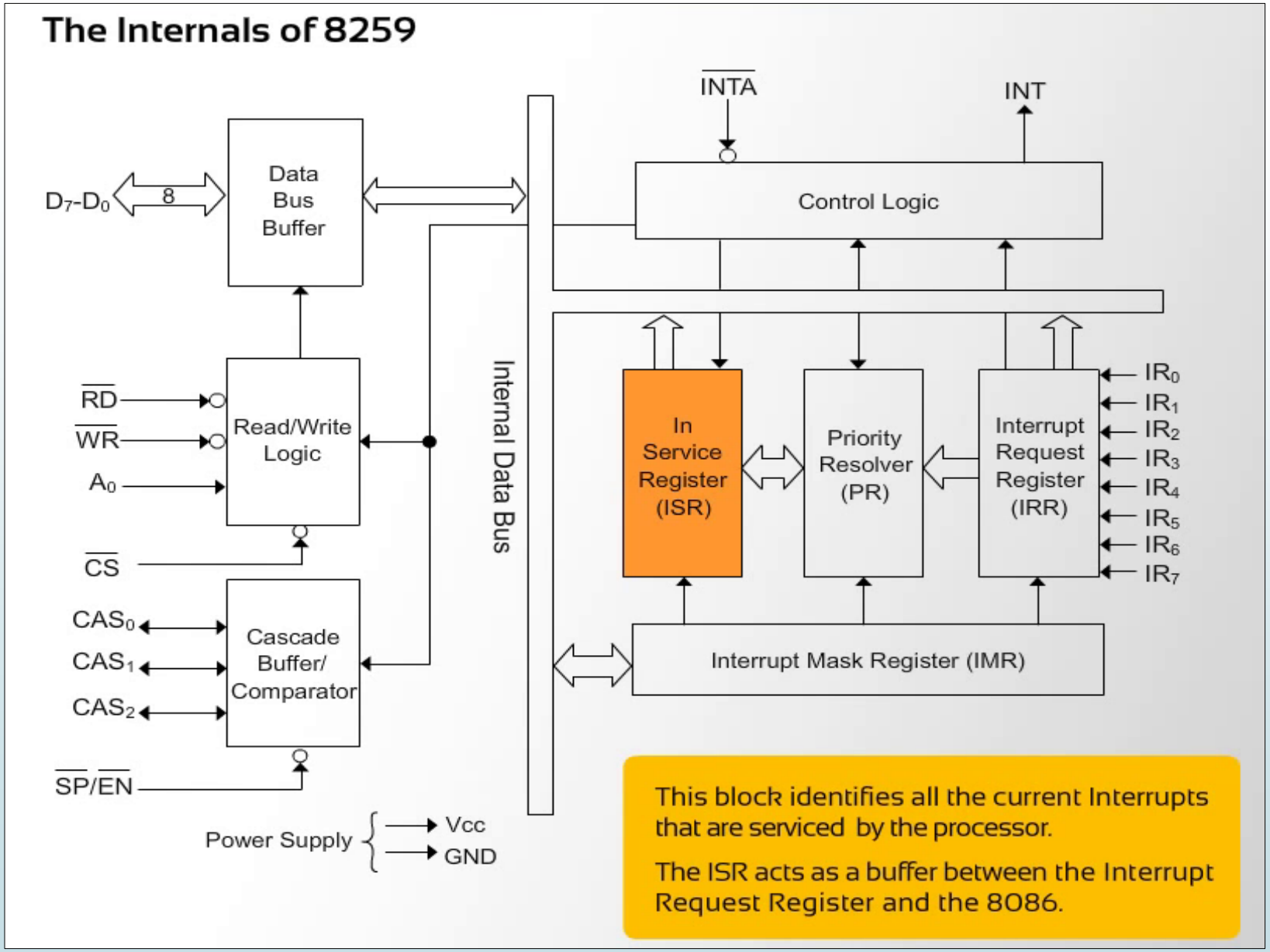


Image Courtesy: Google

8259A - Internals (PR)

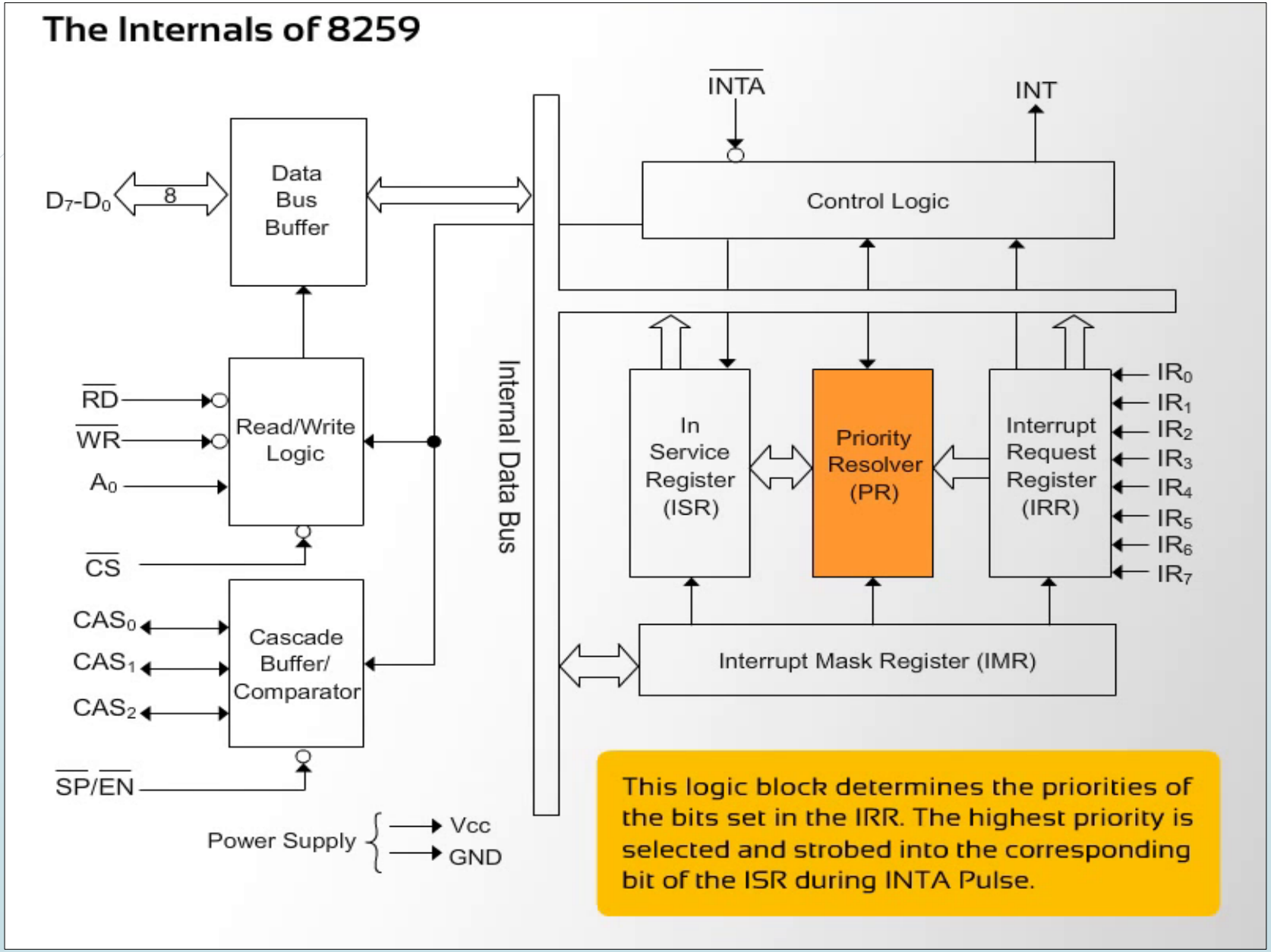


Image Courtesy: Google

8259A - Internals (IMR)

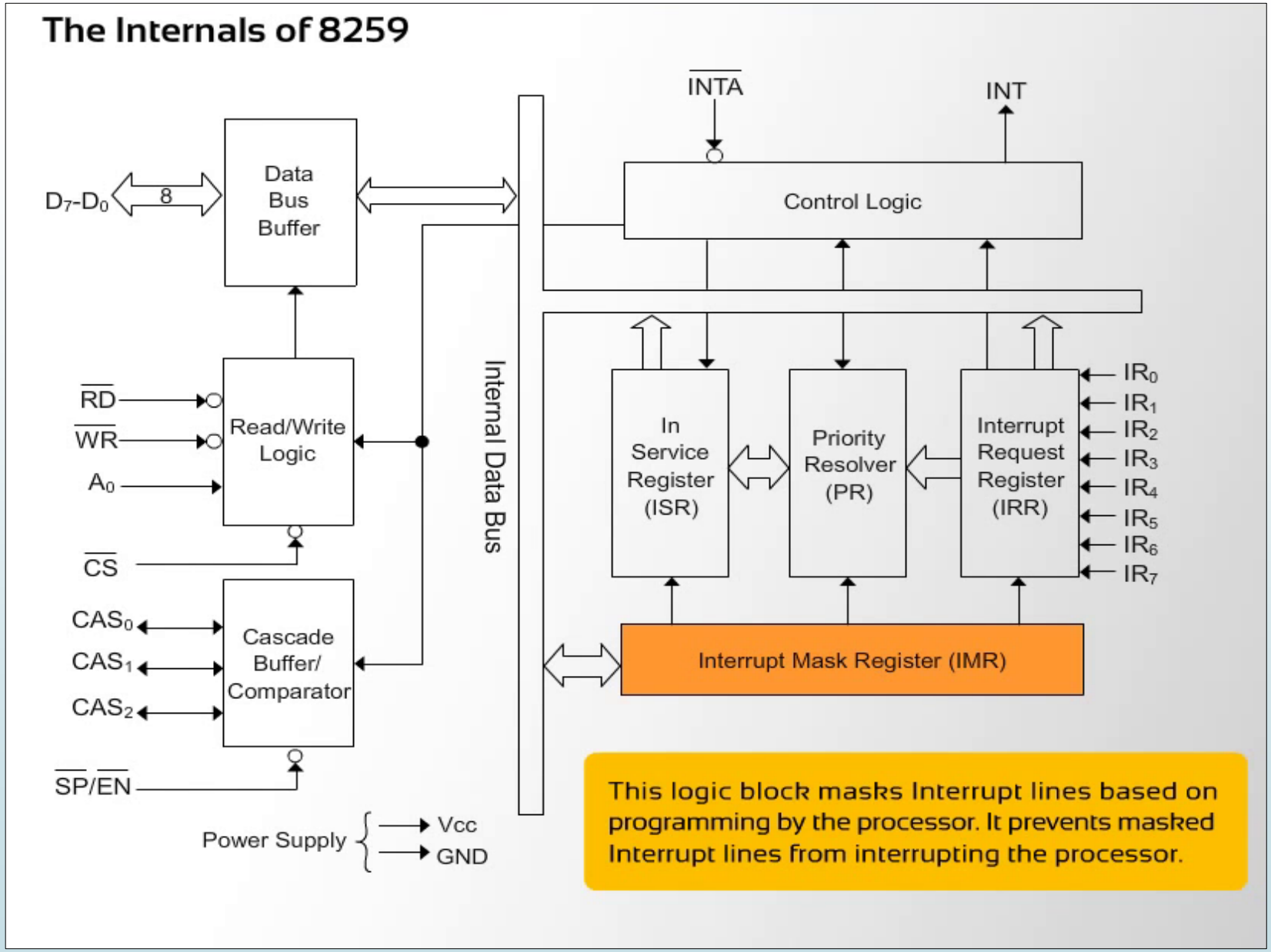


Image Courtesy: Google

8259A - Internals (CAS)

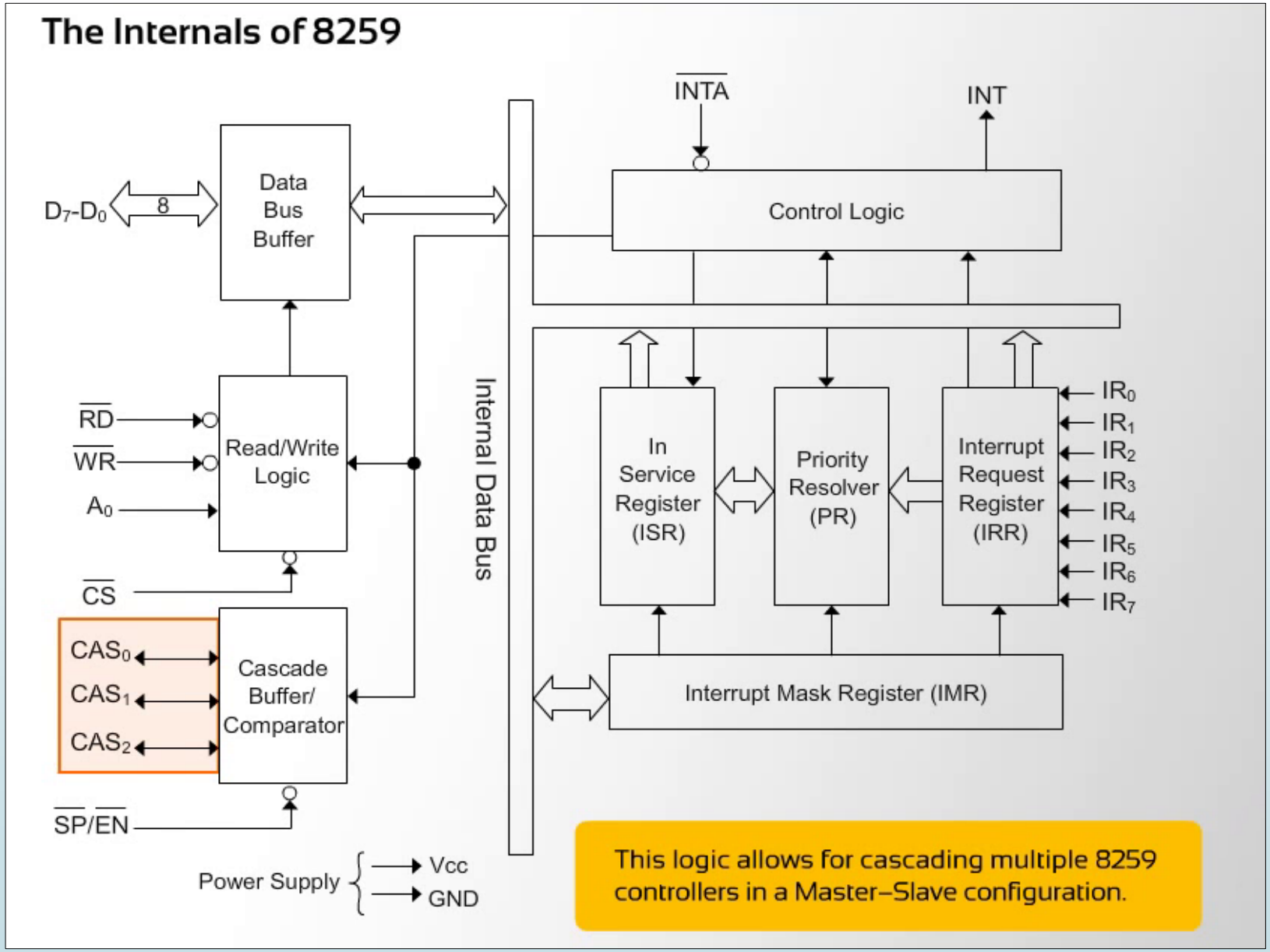
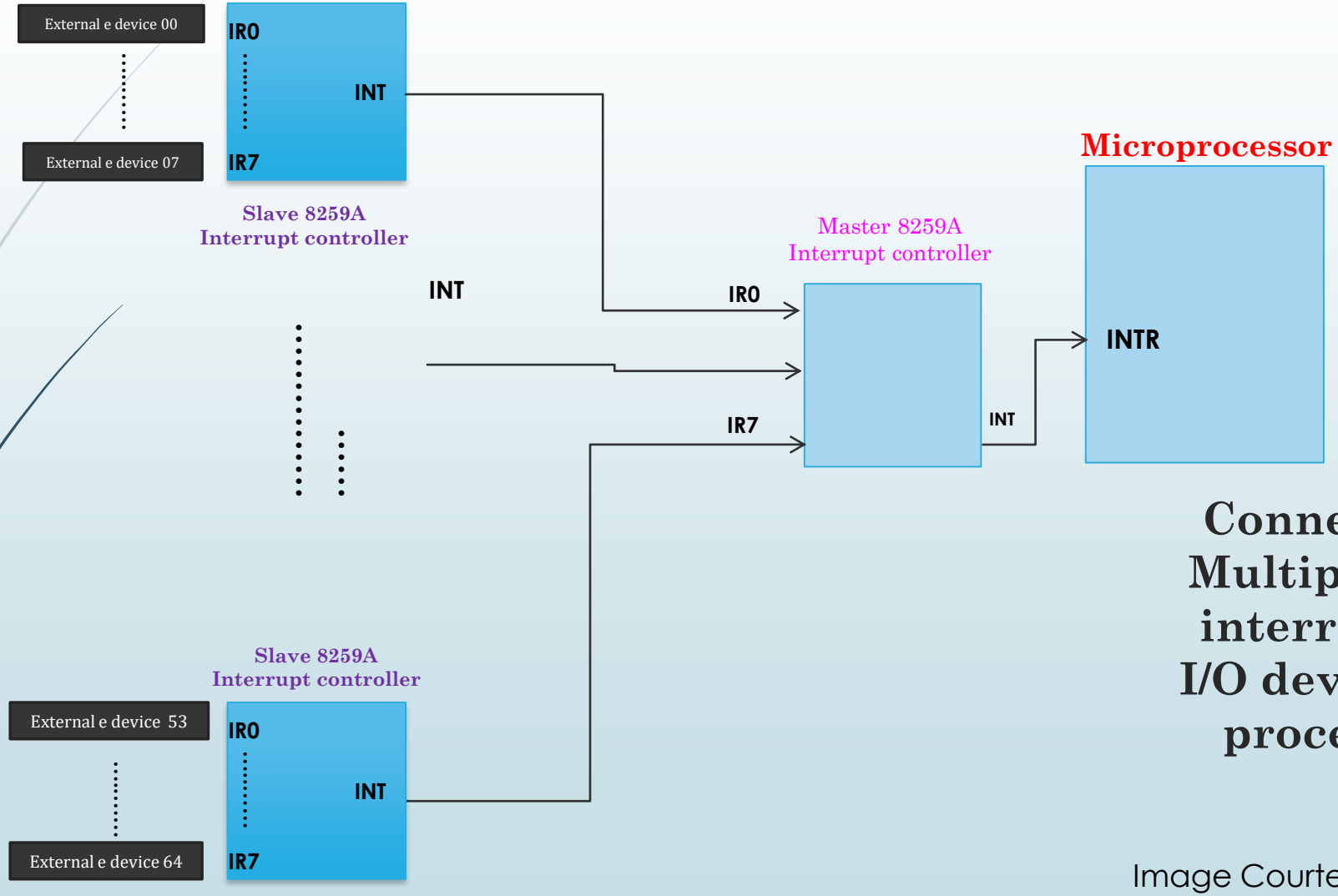


Image Courtesy: Google

Cascading multiple 8259



Connecting Multiple (64) interrupted I/O devices to processor

Image Courtesy: Google

Learning Resource

[1] K. M. Bhurchandi and A. K. Ray, "Advanced Microprocessors and Peripherals – with ARM and an Introduction to Microcontrollers and Interfacing", Tata McGraw Hill, 3rd ed., 2015.

Note: Almost all figures and text content taken from the above stated book.

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Thank You