SRM Institute of Science and Technology
College of Engineering and Technology
DEPARTMENT OF ECE
SRM Nagar, Kattankulathur – 603203, Chengalpattu District, Tamil Nadu
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18ECC103 J –Digital Electronic Principles

Question bank

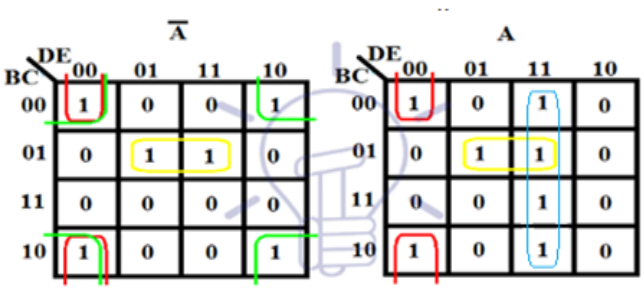
Unit 1

Binary Codes, Digital Arithmetic and Simplification of Boolean Functions

CO -1: Simplify Boolean expressions; carry out arithmetic operations with binary numbers; apply parity method for error detection and correction.

Part- A
Multiple Choice Questions

1. Obtain the minimal Boolean function from the given 5-variable K-map.



a) A'C'E'+C'D'E'+B'CE+ABDE
b) A'C'E'+C'D'E'+B'CE+ADE
c) A'C'E'+C'D'E'+B'C'E'+ADE
d) ACE+C'D'E'+B'C'E'+ADE

2. A student doing a lab experiment wants to design an EX-NOR gate. The list of ICs available in lab is IC 7404 and IC 7400. How many ICs are required if the student is using (i) only NAND gate ICs, and (ii) using both ICs?

a. 2 nos. of 7400, (ii) 1 no. of 7400 and 1 no. of 7404
b. 2 nos. of 7400, (ii) 2 nos. of 7400 and 1 no. of 7404
c. 1 no. of 7400, (ii) 1 no. of 7400 and 2 nos. of 7404
d. 1 no. of 7400, (ii) 2 nos. of 7400 and 1 no. of 7404

3. The output of a logic gate is 1 when the inputs are different Logic level. The gate is either

a) XNOR or OR or XOR
b) OR or NOR or AND

c) XOR or NAND or OR
d) AND or XNOR or NOR

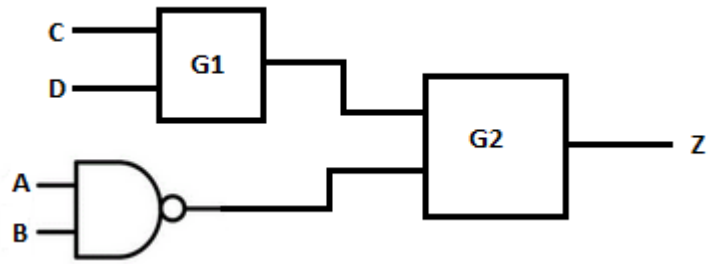
4. Find the POS expression for the function F(A,B,C) = ΠM(0,3,6,7)

a) (A'+B'+C)(B'+C')(A+B+C)
b) (B'+C)(B'+C')(A+B+C)
c) (A'+B'+C)(B'+C')(A+B)
d) (A'+B'+C)(B+C)(A+B+C)

5. Reduce the following 2-variable function and suggest which gate to buy. (AND) XOR (NOR)

a) XOR
b) XNOR
c) AND
d) NOR

6. In the given figure, what gate will be present in the place of G1, G2. If the output Z is required to be (i) Z = ABCD and (ii) Z= AB + CD.



a) (i)AND,OR (ii) NAND,NAND
b) (i) NAND,NOR (ii) NAND,NAND
c) (i) NAND,NAND (ii) NOR,AND
d) (i) NAND,NOR (ii) OR,NAND

7. Encode the binary word 1011 and 0011 into seven bit even parity hamming code respectively.
a) 1010111,1010111
b) 1010101,0011110
c) 1010101,0001110
d) 1010101,0011001

8. Convert the following
1. 32.25 Octal to hexadecimal
2. 1ABCDEF Hexadecimal to Octal

1) 1A.54 , 2) 152746757
1) 1A.54 , 2) 152756757
1) 1C.74 , 2) 152756750
1) 1B.A4 , 2) 142756757

9. Find the correct answer.

$$f = (A \oplus B) + (\overline{A \oplus B})$$
$$= \bar{A}B + \bar{B}A + \overline{AB} + AB$$
$$= \bar{A}B + \overline{AB} + AB + A\bar{B}$$
$$= \bar{A}(B + \bar{B}) + A(B + \bar{B})$$
$$= \bar{A}.(1) + A(1)$$
$$= \bar{A} + A$$
$$= 1$$

$$f = (A \oplus B) + (\overline{A \oplus B})$$
$$= \bar{A}B + \bar{B}A + \bar{A}\bar{B} + AB$$
$$= \bar{A}B + \bar{A}\bar{B} + AB + A\bar{B}$$
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$$= \bar{A} + A$$
$$= 1$$

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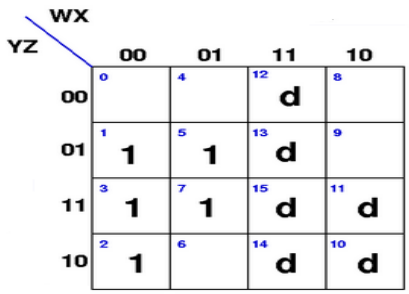
$$= \bar{A}B + \bar{B}A + \bar{A}\bar{B} + AB$$
$$= \bar{A}B + \bar{A}\bar{B} + AB + A\bar{B}$$
$$= \bar{A}(B + \bar{B}) + A(B + \bar{B})$$
$$= \bar{A}.(0) + A(0)$$
$$= \bar{A} + A$$
$$= 1$$

$$f = (A \oplus B) + (\overline{A \oplus B})$$
$$= \bar{A}B + \bar{B}A + \bar{A}\bar{B} + AB$$
$$= \bar{A}B + \bar{A}\bar{B} + AB + A\bar{B}$$
$$= \bar{B}(A + \bar{A}) + A(B + \bar{B})$$
$$= \bar{B}.(1) + A(1)$$
$$= \bar{B} + B$$
$$= 1$$

Second picture is Correct

10. Find the minimal SOP from the given K-MAP.



a) F(W,X,Y,Z) = W'Z + X'Y
b) F(W,X,Y,Z) = WZ + X'Y
c) F(W,X,Y,Z) = W'Z + XY
d) F(W,X,Y,Z) = W'Z + X'YZ'

11. Steps to be followed for 2's Complement Subtraction of a larger number from a smaller number.

(i) Determine the 2's complement of the larger number.
(ii) Add this to the smaller number.
(iii) The difference is the 2's complement of the result from step (ii) with a negative sign appended.

(i) Determine the 1's complement of the larger number.
(ii) Add this to the smaller number.
(iii) The difference is the 1's complement of the result from step (ii) with a negative sign appended.

(i) Determine the 2's complement of the smaller number.
(ii) Add this to the larger number.
(iii) The difference is the 2's complement of the result from step (ii) with a negative sign appended.

(i) Determine the 1's complement of the smaller number.
(ii) Add this to the larger number.
(iii) The difference is the 1's complement of the result from step (ii) with a negative sign appended.

12.Find the answer for the following.

1) $CFBE_{16} - AFFF_{16}$
2) $4567_8 - 3456_8$
3) $1110001101_2 - 1100001110_2$

1) $CFBE_{16} - AFFF_{16}$
2) $4567_8 - 3456_8$
3) $1110001101_2 - 1100001110_2$

1) 1FBF
2) 1111
3) 1111111

1) 1FCF
2) 1127
3) 1110011

1) 1ABF
2) 1112
3) 1011111

1) 1FBC
2) 2211
3) 1001111

13. The binary number 110110011 is equivalent octal number_____

a. 664
b. 662

c. 663
d. 665

14. In Boolean algebra, the bar sign (-) indicates_____
    a. AND gates
    b. OR gates
    c. NOT gates
    d. NAND gates

15. Minimization of Boolean Expression of A' B C' D + A' B C D + A B D
    a. BC
    b. BD
    c. A' B
    d. A' D

16. Simplifying the three variable expression using Boolean algebra of Y (A, B, C) =
    a) 1
    b) ABC
    c) C
    d) A

17. NAND .gates are preferred over others because these
    a) Have lower fabrication area
    b) Can be used to make any gate
    c) Consume least electronic power
    d) Provide maximum density in a chip

18. Which is the correct order of sequence for representing the input values in K-map?

    a) (00, 01, 10, 11)
    b) (00, 10, 01, 11)
    c) (00, 10, 11, 01)
    d) (00, 01, 11, 10)

19. The binary code of $(21.125)_{10}$ is
    a) 10101.001
    b) 10100.001
    c) 10101.010
    d) 10100.111

20. On subtracting $(1011)_2$ from $(1111)_2$ using 1's complement, we get_____
    a. 10011
    b. 0100
    c. 1010
    d. 0110

21. There are _____Minterms for 5 variables (A, B, C, D, E)

a) 31
b) 16
c) 32
d) 64

22. Add the two BCD numbers: 1000 + 0110 =?
    a) 00010100
    b) 01010000
    c) 10101111
    d) 00100100

23. Add $3F8_{16}$ and $5B3_{16}$
    a) $9AC_{16}$
    b) $9BA_{16}$
    c) $9AB_{16}$
    d) $9CA_{16}$

24. On subtracting $(1110)_2$ from $(1010)_2$ using 2's complement, we get_____
    a) -1100
    b) -0100
    c) 0100
    d) 1100

25, Product- of –Sums Expression can be implemented using

a)2-level NOR logic circuits
b)2 level NAND logic circuits
c)3 level NAND logic circuits
d) 3level NOR logic circuits

Part-B

26. Convert the following hexadecimal numbers to decimal equivalent
    (i) FFF (ii) 1622
27. Convert the Octal numbers to hexadecimal (i) 673 (ii) 3643
28. Encode data bits 0101 into a 7 bit even parity Hamming code.
29. A 7-bit Hamming code is received as 0101101.What is its correct code?
30. Simplify the expression
31. Realize NOT, OR, AND using NAND gates.
32. Realize NOT, OR, AND using NOR gates.
33. Realize the logic expression + using basic gates.
34. Realize using NAND gates .
35. Realize) using NOR gates.

36. What is a Prime Implicant? Define Essential Prime implicants.

Part C

37. Simplify using K- Map: (i) F=xy+x'y'z'+x'yz' (ii) F =A'B+BC'+B'C'
38. Simplify using K-Map. (i)F (x, y, z) =∑(1,2,3,6,7)
    (ii) F(a,b,c) = ∑(0,2,3,4,6)
39. Simplify using K-Map and implement using NAND gates.
    i. F = Σ (0,1,2,8,10,11,14,15)
    ii. F= Σ (0,2,4,5,6,7,8,10,13,15)
40. Simplify the Boolean function in SOP and POS and give the NAND and NOR implementation. F(A,B,C,D) = Σ (0,1,2,5,8,9,10)
41 .Simplify using K-MAP. F(A,B,C,D,E) = Σ(0,2,4,6,9,13,21,23,25,29,31)
42. Find the minimal sum of products for the Boolean expression
    F(A,B,C,D)= Σ(1,2,3,7,8,9,10,11,14,15) using the Quine- Mc Cluskey method.
43. Find the minimal sum of products for the Boolean expression
    F(w,x,y,z)= Σ(1,3,4,5,9,10,11)+ Σd(6,8) using the Quine- Mc Cluskey method.
44. Obtain (a) minimal sum of product and (b) minimal product of sum expressions for the given function F(A,B,C,D) = Σ m (0,2,3,6,7) + Σ d 8,10,11,15).

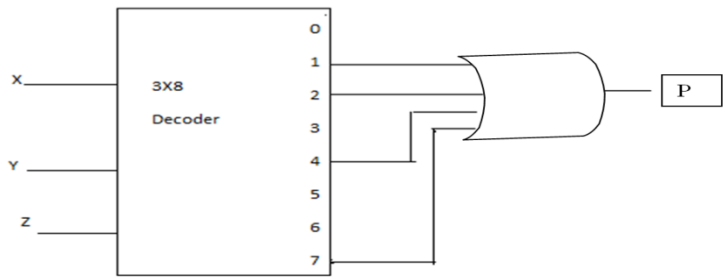
Unit 3

Combinational Systems

CO 3 : Identify eight basic types of fixed-function combinational logic functions and demonstrate how the devices / circuits can be used in building complete digital systems such as computers.

Part-A (MCQ)

Q1	What is the other name of a Multiplexer?
A	Data setter
B	Data distributor
C	Data selector
D	Both data selector and distributor
Q2	How many NOT gates are required to design a 8X1 MUX?
A	1
B	2
C	3
D	4
Q3	A decoder with enable input can function as a
A	Multiplexer
B	Demultiplexer
C	Code converter
D	Magnitude comparator
Q4	The name decoder is also used in conjunction with other code converter, such as a----------decoder
A	Binary to gray
B	Gray to binary
C	BCD to seven segments
D	Binary to BCD
Q5	Digital multiplexer is basically a combinational logic circuit to perform the operation
A	AND-AND
B	OR-OR
C	AND-OR
D	OR-AND
Q6	How many 4:1 Multiplexers are required to construct a16:1 Multiplexer?
A	4
B	2
C	5
D	16

Q7	IC decoders are made with
A	AND gate
B	OR gate
C	NAND gate
D	XOR gate
Q8	The logic circuit which performs the arithmetic sum of two bits is called as
A	Multiplexers
B	De-multiplexers
C	Half-subtractor
D	Half-adder
Q9	The circuit shown below is 
A	3 input EX-OR gate
B	3 input AND gate
C	3 input EX-NOR gate
D	3 input NAND gate
Q10	In _____ adders, the sum, and carry outputs of each stage cannot be produced until the input carry occurs.
A	Full – adder
B	Parallel adder
C	Serial adder
D	Half-adder
Q11	Convert the BCD code "1001" into gray code
A	1101
B	1100
C	1110
D	1010
Q12	What is the number of select lines required for a 1 to 16 demultiplexer?
A	16
B	1
C	8
D	4
Q13	To implement the AND function, the inputs of a 2 :1 MUX should be

A	0, A’
B	1, A
C	0.A
D	1,A’
Q14	Which gate is mostly used in Parity Checker circuit?
A	Ex or
B	Nand
C	And
D	Or
Q15	The number of EXNOR logic gate in a 2-bit magnitude comparator is
A	3
B	5
C	2
D	4
Q 16	Comparators are used in
A	Memory
B	**CPU**
C	Motherboard
D	Hard drive
Q 17	The IC number for a 4-bit magnitude comparator is
A	74LS108
B	74LS85
C	74LS09
D	74LS101
Q 18	The Multiplexer required to implement a four variable Boolean function is
A	4 to 1
B	8 to 1
C	16 to 1
D	2 to 1
Q 19	How many selections required to implement to design 32x1Multiplexer
A	4
B	3
C	2
D	5
Q 20	Convert the binary code "1111" into gray code
A	1011

B	1010	
C	1000	
D	1101	

Part-B:

1. Explain the steps for designing combinational logic circuit.
2. Draw the logic diagram for FA using two half adders with truth table and expression.
3. Draw the logic diagram for FS using two half subtractor with truth table and expression.
4. Design of full-subtractor using basic gates.
5. Design of full-adder using basic gates.
6. Draw and explain the block diagram of n-bit parallel adder(RCA).
7. Drive the carry generation expression for 4-bit CLA circuit.
8. Draw and explain the 4-bit adder/subtractor.
9. Design a 1-bit magnitude comparator.
10. Explain the working of multiplexer and demultiplexer with function table.
11. Draw the logic diagram 4-16 decoder using 3-8 decoder.
12. Draw the block diagram of 8x1Mux using 4x1 Mux and 2x1 Mux.
13. Draw the logic diagram for 16x1 Mux using 4x1 Mux.
14. Design 3-8 decoder using basic gates.
15. Implement the full adder with a decoder circuit.
16. Implement the full subtractor with a decoder circuit.
17. Implement the following using decoder
    (i) $\sum (1,4,6)$
    (ii) $\prod (2,4,6,7)$
18. Design octal to binary encoder.
19. Design a 1-bit priority encoder.
20. Design of 3-bit even and odd parity generator circuit.

Part-C

1. Design a 2-bit magnitude comparator.
2. Design 2-bit priority encoder.
3. Design the following code converters
    (i) Binary to BCD
    (ii) BCD to Excess-3
    (iii) Excess-3 to BCD
    (iv) Binary to gray
    (v) Gray to binary
4. Implement the following SOP and POS using suitable Multiplexer.
    (i) $F(A,B,C,D)= \sum(1,3,4,11,12,13,14,15)$
    (ii) $F(A,B,C,D)=\sum(0,2,6,10,11,12,13) + d(3,8,14)$
    (iii) $F(A,B,C,D)=\prod M(0,3,5,6,8,9,10,12,14)$

5. Implement full-subtractor using demultiplexer.
6. Design a carry look-ahead adder.

Unit – 4
Sequential Systems

CO4: Analyze and design Mealy and Moore models of sequential circuits using several types of flip-flops

PART A (MCQ)

1. The size of sequential circuits designed using Moore state machine is----than mealy state machine.
a) Larger (b) Smaller (c) Equal in size (d) No comparison

2. The output depends on present state of the FF & its input in
a) Mealy b) Moore c) sequential d) synchronous

3. Which flip-flop plays a vital role by functioning as the basic building block of a ripple counter?
a) S-R flip-flop b) J-K flip-flop c)D flip-flop d) T flip-flop

4. Which mechanism allocates the binary value to the states in order to reduce the cost of the combinational circuits?
a) State Reduction b) State Minimization
c) State Assignment d) State Evaluation

5. Two states are said to be equal if they have exactly same
a) Inputs b) next state c) output d) both c and b

6. The asynchronous input can be used to set the flip-flop to the
a) 1 state
b) 0 state
c) either 1 or 0 state
d) None of the Mentioned

7. In JK flip flop same input, i.e. at a particular time or during a clock pulse, the output will oscillate back and forth between 0 and 1. At the end of the clock pulse the value of output Q is uncertain. The situation is referred to as?
a) Conversion condition
b) Race around condition
c) Lock out state
d) None of the Mentioned

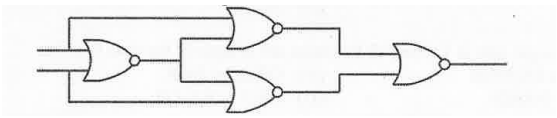
8. If one wants to design a binary counter, preferred type of flip-flop is
a) D type
b) S-R type
c) Latch
d) J-K type

9. How many types of triggering takes place in a flip flops?
a) 2
b) 3
c) 4

d) 5

10. When both inputs of SR latches are low, the latch
a) Q output goes high
b) Q' output goes high
c) It remains in its previously set or reset state
d) it goes to its next set or reset state

11. Identify the logic function performed by the given circuit



a) XOR
b) OR
c) NOR
d) EXNOR

12. How many flip flop are required to build a binary counter circuit to count from o to 1023?
a) 1
b) 6
c) 24
d) 10

13. Which of the following is true for an asynchronous sequential circuit?
a) The speed of the circuit depends on the delay of the flip-flops
b) The speed of the circuit depends on the gate delays
c) The number of flip-flops required is same as that for a synchronous sequential circuit
d) The speed of the circuit depends on outputs

Part B:

1. Derive the characteristic equation, characteristic table, excitation table of a JK flip flop

2. Compare Sequential and combinational logic circuit

3. What is race around condition? How it can be resolved?

4. Explain Master JK flip flop operation with diagram

5. Design D flip flop using T flip flop

6. Write down the general procedure to convert one type of flip flop to other type.

7. List the difference between Moore and Mealy Machine

8. Explain the operation of PISO shift register with diagram

9. Derive the Excitation table, characteristic table and characteristic equation for SR flip flop

10. Explain about 4*2 Priority encoder, how it is different from normal decoder

11. Define the following: 1) clock ii) Edge triggered

12. Compare synchronous Sequential and asynchronous Sequential logic circuit

13. Construct a simple SR latch using NAND gate, draw the truth table

14. Construct a simple SR latch using NOR gate, draw the truth table

15. Explain the operation of PIPO shift register with diagram

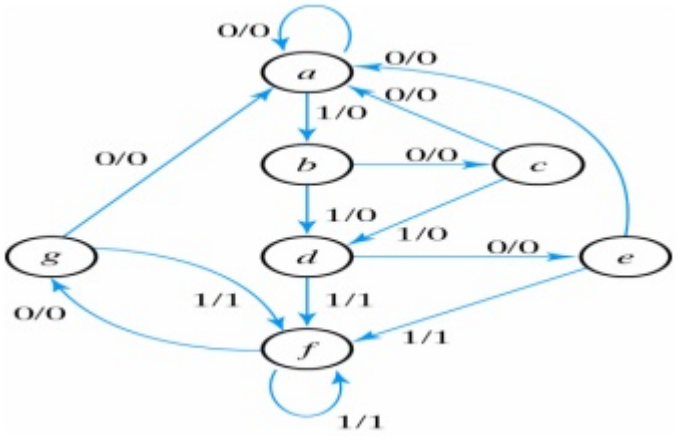
16. Draw the state diagram of JK and D flip flop

17. Design MOD-7 Asynchronous counter and draw its timing diagram.

18. Convert D Flip-flop into SR Flip Flop.

Part C:

1. Reduce the given state diagram using state reduction method



2. Design four bit synchronous up counter using JK flip flop

3. Design Three bit asynchronous up counter using T flip flop

4. Explain a 4-bit Ring counter and draw its timing diagram.

5. Design a decade synchronous down counter using T Flip Flop

6. List the types of shift registers and explain the operation of PISO shift register with diagram

7. Design a counter to count the following sequence 0-3-5-7-9-0 using T flip flop

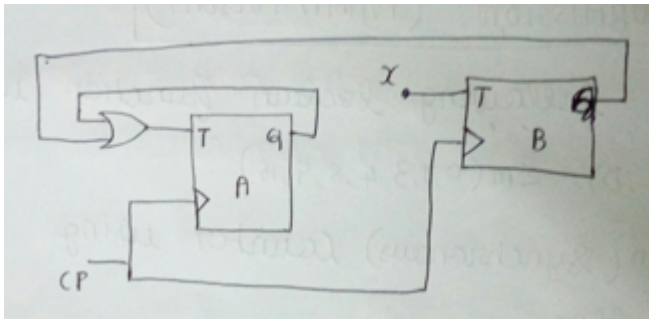
8. Draw the four bit universal shift register diagram and explain its function

9. Design a sequence detector for given sequence =”101” using Moore FSM

10. Explain a 4-bit Johnson Counter and draw its timing diagram.

11. Design the 3- bit sequential circuits that count the sequence of 0,1,2,4,5,6,0… for the applied clock pulse using D- Flip Flops.

12. Analyze the following circuit



Unit -5
Memory and Programmable Logic

CO5: Implement multiple output combinational logic circuits using PLDs; Explain the operation of a CPLD and FPGA

Part-A (MCQ)

1. The inputs in the PLD is given through _____
   a) NAND gates
   b) OR gates
   c) NOR gates
   d) AND gates
2. PAL refers to _____
   a) Programmable Array Loaded
   b) Programmable Logic Array
   c) Programmable Array Logic
   d) Programmable AND Logic
3. Outputs of the AND gate in PLD is known as _____
   a) Input lines
   b) Output lines
   c) Strobe lines
   d) Control lines
4. PLA contains _____
   a) AND and OR arrays
   b) NAND and OR arrays
   c) NOT and AND arrays
   d) NOR and OR arrays
5. PLA is used to implement _____
   a) A complex sequential circuit
   b) A simple sequential circuit
   c) A complex combinational circuit
   d) A simple combinational circuit
6. A PLA is similar to a ROM in concept except that _____
   a) It hasn't capability to read only
   b) It hasn't capability to read or write operation
   c) It doesn't provide full decoding to the variables
   d) It hasn't capability to write only
7. For programmable logic functions, which type of PLD should be used?
   a) PLA
   b) PAL
   c) CPLD
   d) SLD
8. The difference between a PAL & a PLA is _____
   a) PALs and PLAs are the same thing

b) The PLA has a programmable OR plane and a programmable AND plane, while the PAL only has a programmable AND plane

c) The PAL has a programmable OR plane and a programmable AND plane, while the PLA only has a programmable AND plane

d) The PAL has more possible product terms than the PLA

9. The FPGA refers to _____
   a) First programmable Gate Array
   b) Field Programmable Gate Array
   c) First Program Gate Array
   d) Field Program Gate Array
10. In FPGA, vertical and horizontal directions are separated by _____
    a) A line
    b) A channel
    c) A strobe
    d) A flip-flop
11. What is memory decoding?
    a) The process of Memory IC used in a digital system is overloaded with data
    b) The process of Memory IC used in a digital system is selected for the range of address assigned
    c) The process of Memory IC used in a digital system is selected for the range of data assigned
    d) The process of Memory IC used in a digital system is overloaded with data allocated in memory cell

12. How many 1024 * 1 RAM chips are required to construct a 1024 * 8 memory system?
    a) 4
    b) 6
    c) 8
    d) 12
13. How many 16k*4 RAM are required to achieve a memory with a capacity of 64K*8 RAMS?
    Ans-8
14. How many 16k*4 RAM are required to achieve a memory with a capacity of 32K*8 RAMS?
    Ans-4
15. How many 8k*2 RAM are required to achieve a memory with a capacity of 16K*8 RAMS?
    Ans-8

16. How many address line are needed to select all memory location in 32k*8 RAM?
    Ans – 15
17. How many address line are needed to select all memory location in 8k*1 RAM?
    Ans – 13

18. A 64kb memory array is designed as square with an aspect ratio of one (number of rows is equal to number of columns). The minimum number of address line required for the row decoder is
    Ans -8

19. A 16kb memory array is designed as square with an aspect ratio of one (number of rows is equal to number of columns). The minimum number of address line required for the row decoder is
    Ans -7

20. An 8085 microprocessor based system uses a 4k*8 RAM whose starting address is AA00H. The address of the last byte in this RAM is
    Ans- BA00

21. An 8085 microprocessor based system uses a 8k*8 RAM whose starting address is AA00H. The address of the last byte in this RAM is
    Ans- CA00

22. An 8085 microprocessor based system uses a 2k*8 RAM. What is the range of address it consumes?
    Ans - B200 - EEEE

Part- B

1. A 16K * 4 memory uses coincident decoding by splitting the internal decoder into *X* selection and *Y* selection.
   (a) What is the size of each decoder, and how many AND gates are required for decoding the address?
   (b) Determine the *X* and *Y* selection lines that are enabled when the input address is the binary equivalent of 6,000.
2. Derive the PLA programming table for the combinational circuit that squares a three bit number. Minimize the number of product terms.
3. Derive the ROM programming table for the combinational circuit that squares a 4 bit number. Minimize the number of product terms.
4. List the PLA programming table for the BCD to excess 3 code converter whose Boolean functions are simplified
5. Derive the PAL programming table for the combinational circuit that squares a three bit number. Minimize the number of product terms.
6. Derive the PLA programming table for the combinational circuit that squares a 4 bit number. Minimize the number of product terms.
7. List the ROM programming table for the BCD to excess 3 code converter whose Boolean functions are simplified
8. Derive the ROM programming table for the combinational circuit that squares a three bit number. Minimize the number of product terms.

9. List the main difference between PLA and PAL
10. List the main difference between PROM and PLA.
11. List the main difference between ROM and RAM.
12. What is Read and Write operation?
13. How many words can a12x8 memory can store?
14. Define ROM and RAM.
15. Define PLA.
16. What is PLD?
17. Summarize about Sequential Programmable Logic Device.
18. Summarize about FPGA.

Part-C

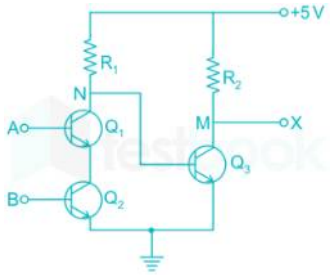
1. Implement the Boolean function with PLA
    a. $A(x,y,z) = \sum m(1,2,5,6)$
    b. $B(x,y,z) = \sum m(1,2,3,7)$
2. $C(x,y,z) = \sum m(2,5,6,7)$
3. Implement the Boolean function with ROM
4. $A(x,y,z) = \sum m(1,2,5,6)$
5. $B(x,y,z) = \sum m(1,2,3,7)$
6. $C(x,y,z) = \sum m(2,5,6,7)$
7. Implement the given function in PLA. Use only the True logic. Find the number of product term required. $A(x,y,z)=\sum m(1,2,4,6)$; $B(x,y,z)=\sum m(0,1,6,7)$; $C(x,y,z)=\sum m(2,4,5,6,7)$; $D(x,y,z)=\sum m(1,2,3,5,7)$
8. Implement the given function in PLA. Use both the True logic and the complement logic. Find the minimum number of product term required. $A(x,y,z)=\sum m(1,2,4,6)$ $B(x,y,z)=\sum m(0,1,6,7)$ $C(x,y,z)=\sum m(2,4,5,6,7)$ $D(x,y,z)=\sum m(1,2,3,5,7)$
9. Implement the Boolean function with PAL
   $A(x,y,z) = \sum m(1,2,5,6)$
   $B(x,y,z) = \sum m(1,2,3,7)$
   $C(x,y,z) = \sum m(2,5,6,7)$
10.
11. Draw the internal diagram of 1-bit SRAM.
12. Design the 2x2 memory array with suitable decoder.
13. Write short notes on different types of ROM.
14. Explain in detail about memory decoding.
15. Explain in detail about coincident memory decoding.
16. Design the 2-bit up-counter and implement in suitable SPAL structure.

Unit -2
Logic Families

CO2: Explain the operational characteristics / properties of digital ICs; implement gates as well as other types of IC devices using two major IC technologies, TTL and CMOS.

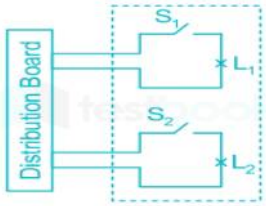
PART –'A' MCQ

1. Which of the following IC logic family has the highest fan-out?
   a. TTL b. CMOS c. ECL d. Schottky TTL
2. If A and B are the logical input to the following circuit, determine the logical relation between the input and the output X.



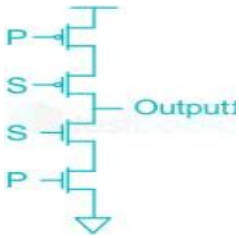
   a. X= A.B b. X= (A.B)' c. X= (A=B)' d. X= (A+B
3. A particular logic family has V = 5 V, V = 1 V, V = 3.5 V and V = 2 V. The noise margin values NM and NM will be
   a. 1.5 V, 1 V b. 5 V, 1 V c. 1 V, 1.5 V d. 4.1 V, 5 V
4. Which of the following statement is incorrect?
   a. TTL devices have logic levels of about 3.4 V and 0.2 V
   b. TTL logic normally operates from a single 5 V supply
   c. Standard TTL devices have a propagation delay that is dominated by the storage time of the bipolar transistors used
   d. TTL logic has very low power consumption and is therefore widely used in highly integrated components
5. Two voltage given as -2 V and -1 V in positive logic convention represent:
   a. -2 V is logic 1 and -1 V is logic 0
   b. -5 V is logic 0 in some circuit and 1 in the other
   c. -2 V is logic 0 and -1 V is logic 1
   d. -5 V is logic 1 in some circuits and 0 in the other
6. The figure of merit of a logic family is given by the product of:
   a. Gain and Bandwidth
   b. Propagation delay time and power dissipation
   c. Fan-out and propagation delay time
   d. Noise margin and power dissipation
7. Which among the following is the fastest switching logic family?
   a. CMOS
   b. ECL
   c. TTL
   d. DTL

8. Identify the given wiring diagram of _____.



a. Two lamps controlled by two switches, all connected in series
b. Two lamps in series, each having a switch in parallel
c. Two lamps each controlled by a separate switch
d. Two lamps in joint box system

9. Output of the circuit shown below when S = 1 and S = 0 will be_____.



a. P and High Impedance state respectively
b. High Impedance state and P' respectively
c. 0 and 1 respectively
d. X and P respectively

10. As compared to TTL, CMOS logic has

a. high speed of operation
b. higher power dissipation
c. smaller physical size
d. none of the above

11. For a typical CMOS process, the minimum feature size is set to be 25 µm. The minimum line width at the process is set to be _____

a. 100 µm
b. 12.5 µm
c. 50 µm
d. 25 µm

12. An acceptable voltage range of a logic 0 for TTL

a. 0 to 0.8 V
b. 0 to 1.5 V
c. 2 to 5
d. 3.5 to 5 V

13. Calculate the fan out of a TTL circuit with the following specifications: I (max) = 32 mA, I (max) = 1.6 mA, I (max) = 400 uA, I (max) = 10 uA

a. 10
b. 20

c. 40
d. 60

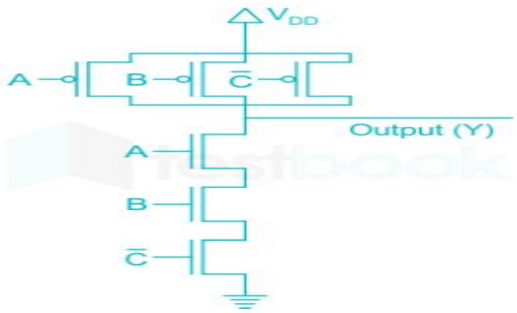
14. Which of the following logic gates can be used to implement the functionality of any logic gate?

a. XOR
b. XNOR
c. NAND
d. AND

15. Which one of the the following logic family has least propagation delay ?

a. BiCMOS
b. ECL
c. TTL
d. DTL

16. The output (Y) of the circuit shown in the figure is

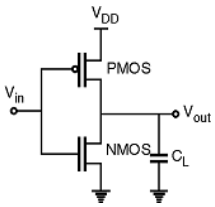


a. A'+B'+C
b. A+B'Ç'+AC'
c. A'+B+C'
d. A.B.C'

17. Which among the following logic family has least propagation delay?

A. ECL
B. TTL
C. I2L
D. DTL

18. The Circuits will act as:



a. Buffer Logic
b. AND Logic
c. OR Logic

d. Inverter Logic

PART – 'B' (4 Marks)

19. Implement a four input AND logic in TTL Logic.
20. Compare TTL and CMOS logic.
21. Give the advantages of ECL Logic
22. Write a note on Schottky diode and its application in logic design.
23. List the merits of the CMOS logic Design.
24. Compare RTL and DTL Logic Styles.
25. Why TTL Logic gives less propagation delay? Give an example.
26. Define noise margin measures with respect to TTL and CMSO Logic styles

PART- C (10 Marks)

27. Implement the logic function F= (AB+CD+E)' in CMOS logic and explain it working principle.
28. Implement a two input AND logic in ECL and its working operation in details.
29. Explain the merits and demerits of TTL logic Design with an example.
30. Write a note on (i) Noise margin (ii) Propagation Delay (iii) fan-out
31. Write a note on (i) Schottky TTL logic (ii) RTL Logic

*** THE END***