31. a. Describe the working of voltage controlled oscillator with neat sketch and list out its applications.

(OR)

b. Explain the 555 timer operation in monostable mode with relevant diagram.

32. a. With necessary diagram explain the working of PLL and describe how PLL is used in FSK demodulation.

(OR)

b. Explain Gilbert cell multiplier circuit and derive the expression for output voltage.

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Reg. No.

B.Tech. DEGREE EXAMINATION, NOVEMBER 2018
Fourth Semester

MH1012 – LINEAR INTEGRATED CIRCUITS
(For the candidates admitted during the academic year 2013 – 2014 and 2014 – 2015)

Note:
(i) **Part - A** should be answered in OMR sheet within first 45 minutes and OMR sheet should be handed over to hall invigilator at the end of 45th minute.
(ii) **Part - B** and **Part - C** should be answered in answer booklet.

Time: Three Hours   Max. Marks: 100

PART – A (20 × 1 = 20 Marks)
Answer **ALL** Questions

1. Another name for a unity gain amplifier is
   (A) Difference amplifier   (B) Comparator
   (C) Single ended   (D) Voltage follower

2. For ideal operational amplifier, the CMRR value is _____.
   (A) 0   (B) 1
   (C) ∞   (D) −1

3. The gain of an integrator circuit for a DC input is _____.
   (A) Infinity   (B) Zero
   (C) 6 dB   (D) 3 dB

4. The output of a particular op-amp increases 8V in 12 µs. The slew rate is
   (A) 90 V/µs   (B) 0.67 V/µs
   (C) 1.5 V/µs   (D) 3 V/µs

5. Precision rectifier rectifies the voltages _____.
   (A) Below 0.7 V   (B) Above 90 µV
   (C) Below 60 µV   (D) Above 0.7 V

6. An op-amp clamper is also referred as
   (A) DC cutter   (B) DC inserter
   (C) Rectifier   (D) Regulator

7. Which of the following is used as an active element in the active filter circuits?
   (A) Inductor   (B) Capacitor
   (C) Resistor   (D) Op-amp

8. In Schmitt trigger circuit, hysteresis voltage is _____.
   (A) $\dfrac{V_{UT} + V_{LT}}{2}$ (B) $V_{UT} + V_{LT}$

   (C) $V_{UT} - V_{LT}$ (D) $\dfrac{V_{UT} - V_{LT}}{2}$

9. Which of the following is used in between the sensor module and the processing unit?
   (A) Flash type ADC
   (B) Weighted resistor type DAC
   (C) R-2R ladder type DAC
   (D) Inverted R-2R DAC

10. The flash type A/D converters are also called as
   (A) Parallel non-inverting A/D converter
   (B) Parallel counter A/D converter
   (C) Parallel inverting A/D converter
   (D) Parallel comparator A/D converter

11. In 4-bit successive approximation A/D, the starting bit sequence is _____.
   (A) 0000
   (B) 1000
   (C) 1100
   (D) 1111

12. The basic step of a 9-bit DAC is 10.3 mV. If 000000000 represents 0V, what output is produced if the input is 101101111?
   (A) 5 V
   (B) 1.5 V
   (C) 2 V
   (D) 3.78 V

13. In an astable multivibrator circuit using 555 IC frequency of oscillation in the output is given as
   (A) $F = (2R_A + R_B)C \ Hz$
   (B) $F = \dfrac{1}{(R_A + R_B)C} \ Hz$
   (C) $F = \dfrac{1.45}{(R_A + 2R_B)C} \ Hz$
   (D) $F = \dfrac{R_B C}{0.69 R_A} \ Hz$

14. Which characteristics of PLL is defined as the range of frequencies over which PLL can acquire lock with input signal?
   (A) Free running state
   (B) Pull in time
   (C) Lock in range
   (D) Capture range

15. How many comparators are available in 555 timer?
   (A) 3
   (B) 2
   (C) 1
   (D) 0

16. In a typical IC monostable multivibrator circuit, at the falling edge of the trigger input, the output switches high for a period of time determined by the _____.
   (A) Value of the RC timing components
   (B) Amplitude of the input trigger
   (C) Frequency of the input trigger
   (D) Magnitude of the DC supply voltage

17. Switching regulator operates power transistor as
   (A) Low frequency on/off switch
   (B) High frequency on/off switch
   (C) Low frequency on switch
   (D) High frequency on switch

18. In which of the following oscillator, the frequency deviation is directly proportional to the DC control voltage?
   (A) RC phase shift oscillator
   (B) Wien bridge oscillator
   (C) Colpitts oscillator
   (D) Voltage controlled oscillator

19. _____ multiplier will function property if one input is held positive and the other can be changed positive or negative.
   (A) One quadrant
   (B) Two quadrant
   (C) Three quadrant
   (D) Four quadrant

20. When PLL is locked to an input frequency the error is proportional to
   (A) $f_s - f_o$
   (B) $f_c - f_o$
   (C) $f_o - f_s$
   (D) $f_o - f_c$

PART – B (5 × 4 = 20 Marks)
Answer ANY FIVE Questions

21. Design an inverting summer amplifier to get the output expression as $V_0 = -(2.5V_1 + 0.8V_2 + 4V_3)$; take $R = 2k\Omega$.

22. Write a short note on ideal characteristics of op-amp.

23. With relevant diagrams explain the clamping operation using op-amp.

24. Discuss the working principle of sample and hold circuit.

25. Explain the terms resolution and accuracy of ADC.

26. Define the following
   (i) Lock-in range
   (ii) Capture range
   (iii) Pull in time

27. Give the features of 555 timer.

PART – C (5 × 12 = 60 Marks)
Answer ALL Questions

28. a. Explain the non-ideal DC characteristics of op-amp with relevant diagrams.

   (OR)

   b.i. For V to I grounded load converter, V_{in} = 5 V, R = 10 kΩ, non-inverting voltage V_1 = 1V. Find load current and output voltage V_0.

   ii. Design an adder-subtractor circuit for $V_0 = 2V_1 + 5V_2 - 10V_3$ with value R_f = 10 kΩ.

29. a. Draw and explain the commonly used three op-amp instrumentation amplifier circuit. Derive the expression for its gain.

   (OR)

   b. Describe the working of astable multivibrator using op-amp and derive the expression for time period.

30. a. Explain in detail about successive approximation type ADC.

   (OR)

   b. With a neat diagram, explain the working principle of
   (i) R-2R ladder type DAC
   (ii) Weighted resistor DAC