Laboratory Report Cover Sheet

SRM Institute of Science and Technology
College of Engineering and Technology
Department of Electronics and Communication Engineering

18ECC103J- Digital Electronic Principles

Third Semester, 2021-22 (odd semester)

Name :

Register No. :

Day / Session :

Venue :

Title of Experiment : **Design and implement of Adders and Subtractors using logic gates**

Date of Conduction :

Date of Submission :

Particulars	Max. Marks	Marks Obtained
Pre-lab questions	10	
In-lab experiment	20	
Post-lab questions	10	
Total	40	

REPORT VERIFICATION

Date :

Staff Name :

Signature :

Lab 2: Design and implement Adder and Subtractor using logic gates

2.1 Aim

To design and verify the truth table for adders & Subtractors..

2.2 Software and Hardware Requirement

Software	:	Logisim-win-2.7.1.exe (Optional- Tinkercad / LTspice)
Discrete Components:		74LS08 Quad 2 input AND gate 74LS32 Quad 2 input OR gate 74LS86 Quad 2 input XOR gate 74LS04 Hex 1-Input NOT gate
Equipment	:	Digital IC Trainer Kit

2.3 Theory

(i) Half Adder

A Binary adder is a circuit which is able to add together two binary numbers. The half adder adds two binary digits an addend and an augend to produce a sum and carry. The sum can be implemented by using an Exclusive OR gate and an AND gate can be used for carry generation.

The Boolean expression for the sum and carry are

Sum $S = A \oplus B$

Carry $C = A.B$

(ii) Full Adder

The full adder adds an addend, an augend and carry input generated by the previous stage addition. It has two outputs, sum and carry. Full adder circuit can be implemented using AND,OR and EX-OR gates. Full adder circuit can also be implemented with the help of two half adder circuits. The first half adder is used to add two inputs and generate sum and carry output. Then second half adder combines the sum and carry input and generate final sum and carry out.

The sum and carry can be expressed as

Sum $S = A \oplus B \oplus C_{in}$

Carry $C = (A \oplus B)C_{in} + AB = AB + BC_{in} + AC_{in}$

(iii) Half Subtractors

A half subtractor is a multiple output combinational logic network that does the subtraction of two bits of binary data. It has input variables and two output variables. Two inputs are corresponding to two

input bits and two output variables corresponds to the difference bit and borrow bit. The binary subtraction is also performed by the Ex-OR gate with additional circuitry to perform the borrow operation. Thus, a half subtractor is designed by an Ex-OR gate including AND gate with A input complemented before fed to the gate.

The Boolean expression for the Difference and Barrow is

Difference D = $A \oplus B$

Barrow $B_o = \overline{\overline{A}A}. B$

(iv) Full Subtractor

A combinational logic circuit performs a subtraction between the two binary bits by considering borrow of the lower significant stage is called as the full subtractor. It has three input terminals in which two terminals corresponds to the two bits to be subtracted (minuend A and subtrahend B), and a borrow bit Bi corresponds to the borrow operation. There are two outputs, one corresponds to the difference D output and other borrow output Bo as shown in figure along with truth table.

The Boolean expression for the Difference and Barrow are

Difference D = $A \oplus B \oplus B_{in}$

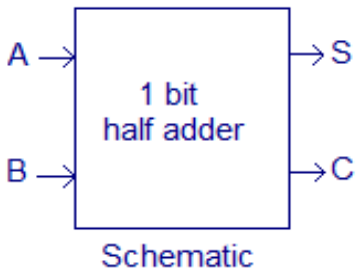
Barrow $B_o = \overline{A}B + \overline{\overline{A}A}B + \overline{A}B_{in} + B_{in}B$

2.4 Circuit Schematic and Truth Table

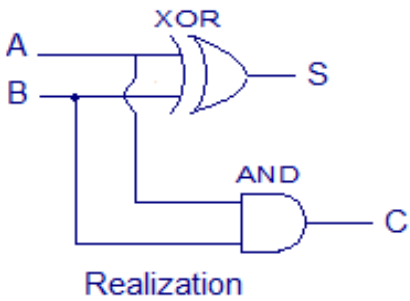
(i) **HALF ADDER**

Inputs		Outputs	
A	B	S	C
0	0	0	0
1	0	1	0
0	1	1	0
1	1	0	1

Truth table



Schematic

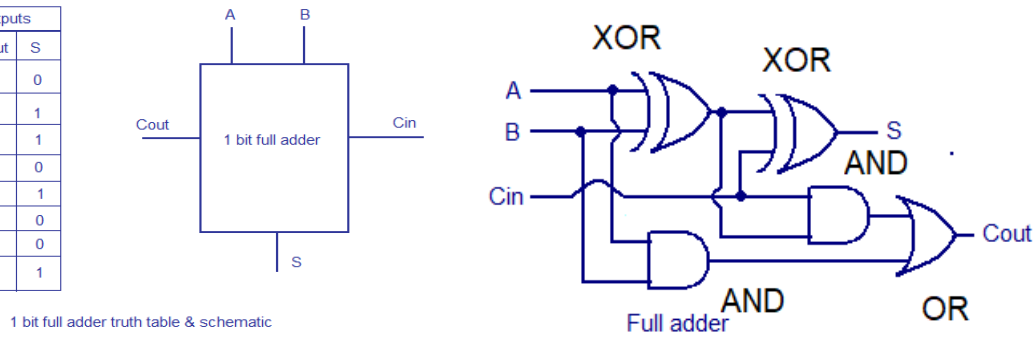


Realization

Figure 2.1: Half-Adder – Truth table and Schematic

(ii) **FULL ADDER**

Inputs			Outputs	
A	B	Cin	Cout	S
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1



1 bit full adder truth table & schematic

Figure 2.2: Full-Adder – Truth table and Schematic

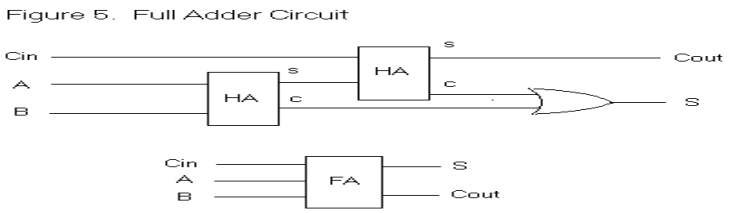
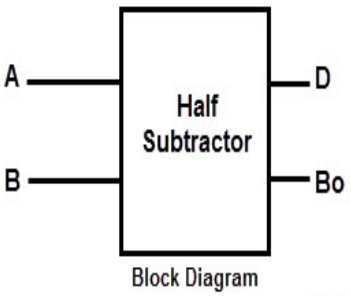


Figure 2.3: Full-Adder using two Half-Adders

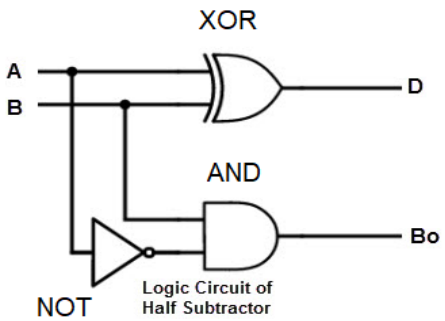
(iii) HALF SUBTRACTOR

A	B	D	B_0
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Truth Table



Block Diagram



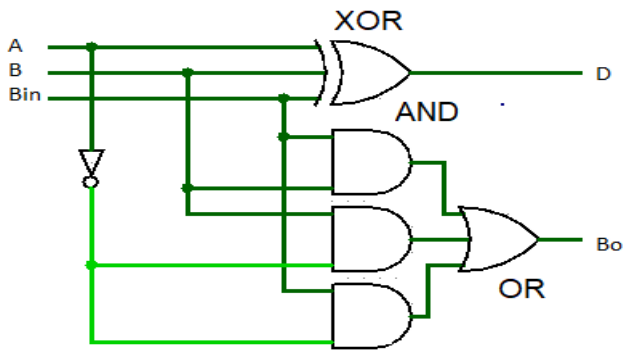
Logic Circuit of Half Subtractor

Figure 2.4: Half Subtractor Truth table and Circuit

(iv) FULL SUBTRACTOR

A	B	B_{in}	D	B_o
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Truth Table



Logic Circuit

Figure 2.5: Full Subtractor Truth table and Circuit

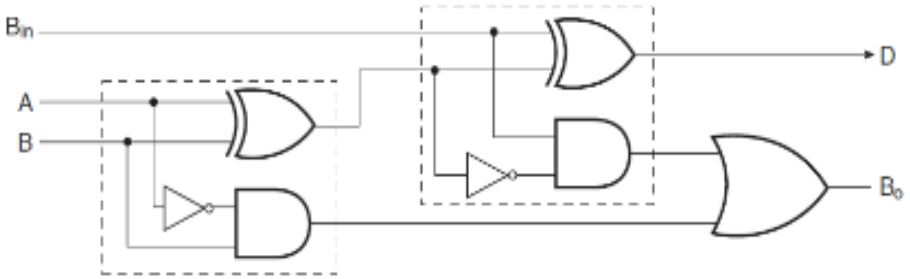


Figure2.6: Full Subtractor using Two Half- Subtractor

(v) **Lab Practice Circuits:**

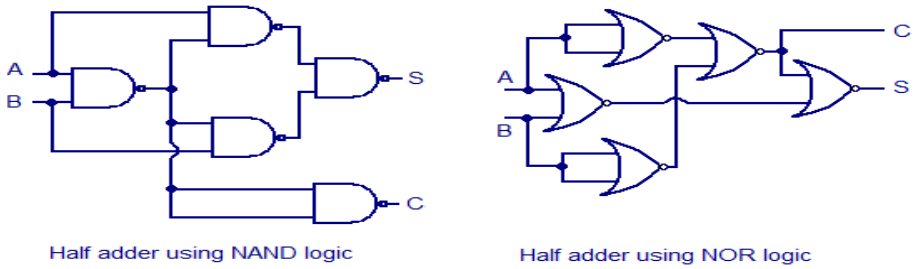


Figure 2.7: Half-Adder using NAND & NOR logic

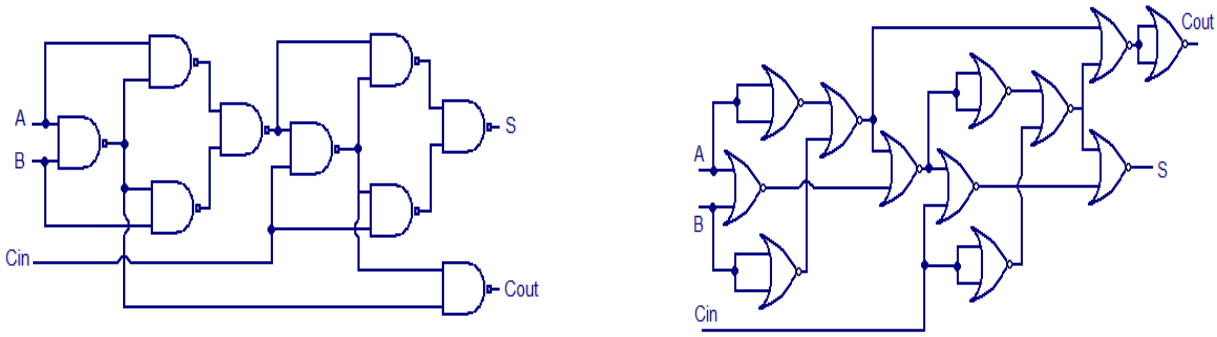


Figure 2.8: Full-Adder using NAND &NOR logic

2.5 Pre lab Questions

1. What is meant by a combinational circuit?
2. Discuss on the logic schematic and the uses of Half adder?
3. Design a circuit which can add 3 bits.
4. Realize a half adder circuit using a NAND gate.
5. Realize a Half subtractor circuit using NOR gate.
6. State the Significances and limitations of Karnaugh map.

2.6 Lab Procedure

1. Double click logisim-win-2.7.1.exe on your desktop to open Logisim.
2. Open a new project named Digital Lab.
3. In the main circuit window, select the gates as per the logic schematic and place it.
4. Change the number of inputs for each gate.
5. Select input/output devices and make connections to make circuits.
6. Save your file as Adder and Subtractor under the project from the File menu.
7. Once the circuit get done, test it by changing the input values and verify the output values as per the truth table.
8. Check the auto generated truth table from the Project menu and select Analyze Circuit and then select Table.

2.7 Post lab Questions

1. Two numbers (1101 and 1011) are applied to a 4-bit parallel adder. The input Carry is '1'. Determine the sum and output carry.
2. Obtain the output of Full adder using NAND gate using Logisim or LTSPICE.
3. Realize a Full subtractor using NOR gate using Logisim and verify its truth table.
4. Realize a 4-bit subtractor by using 4-bit adder and inverters.
5. Design a 4- bit parallel Adder/subtractor.
6. What are the advantages of complement arithmetic?

2.8 Result:

Thus, the adders and subtractors are realized using Logisim and verified its operation.