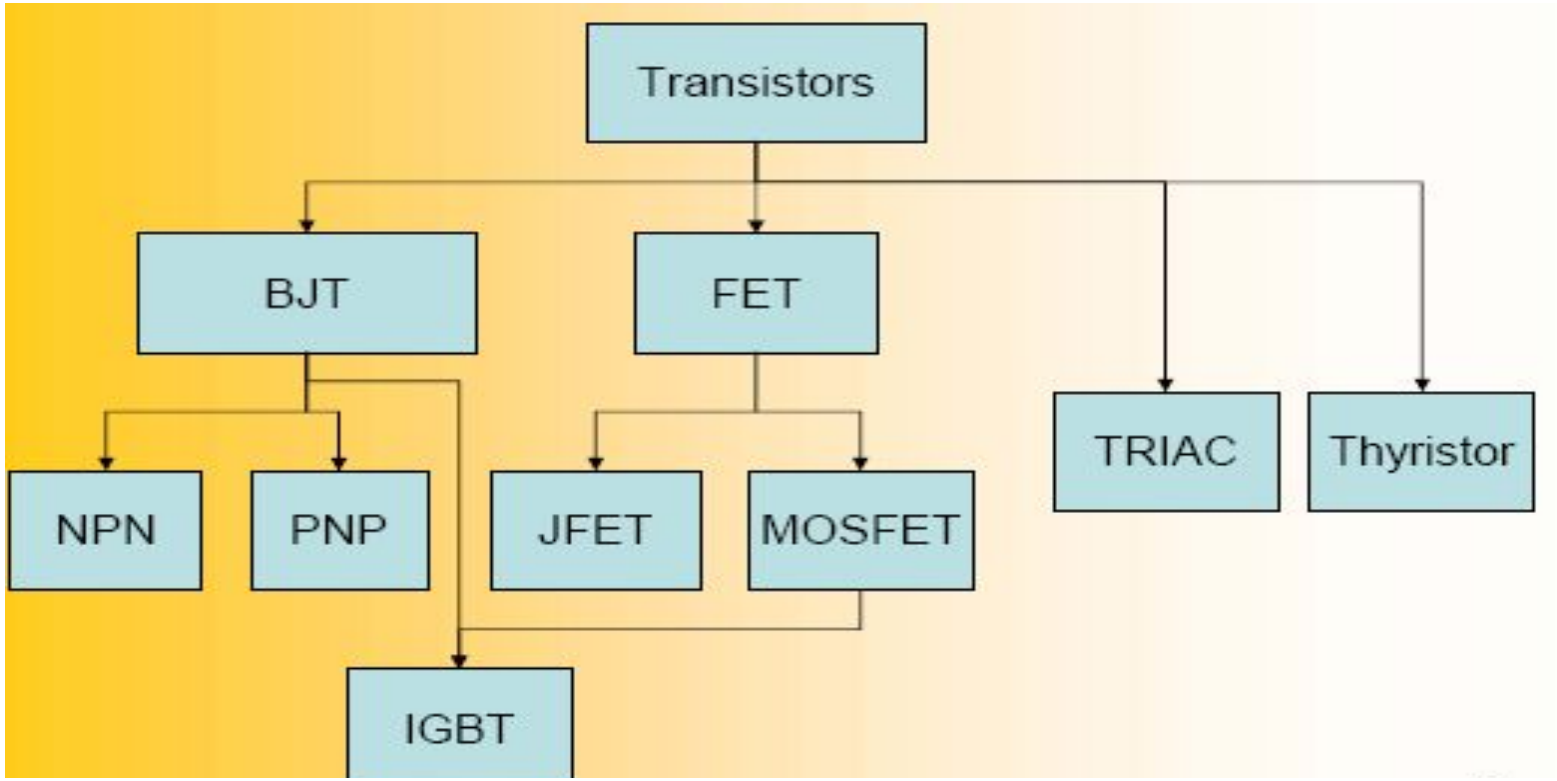
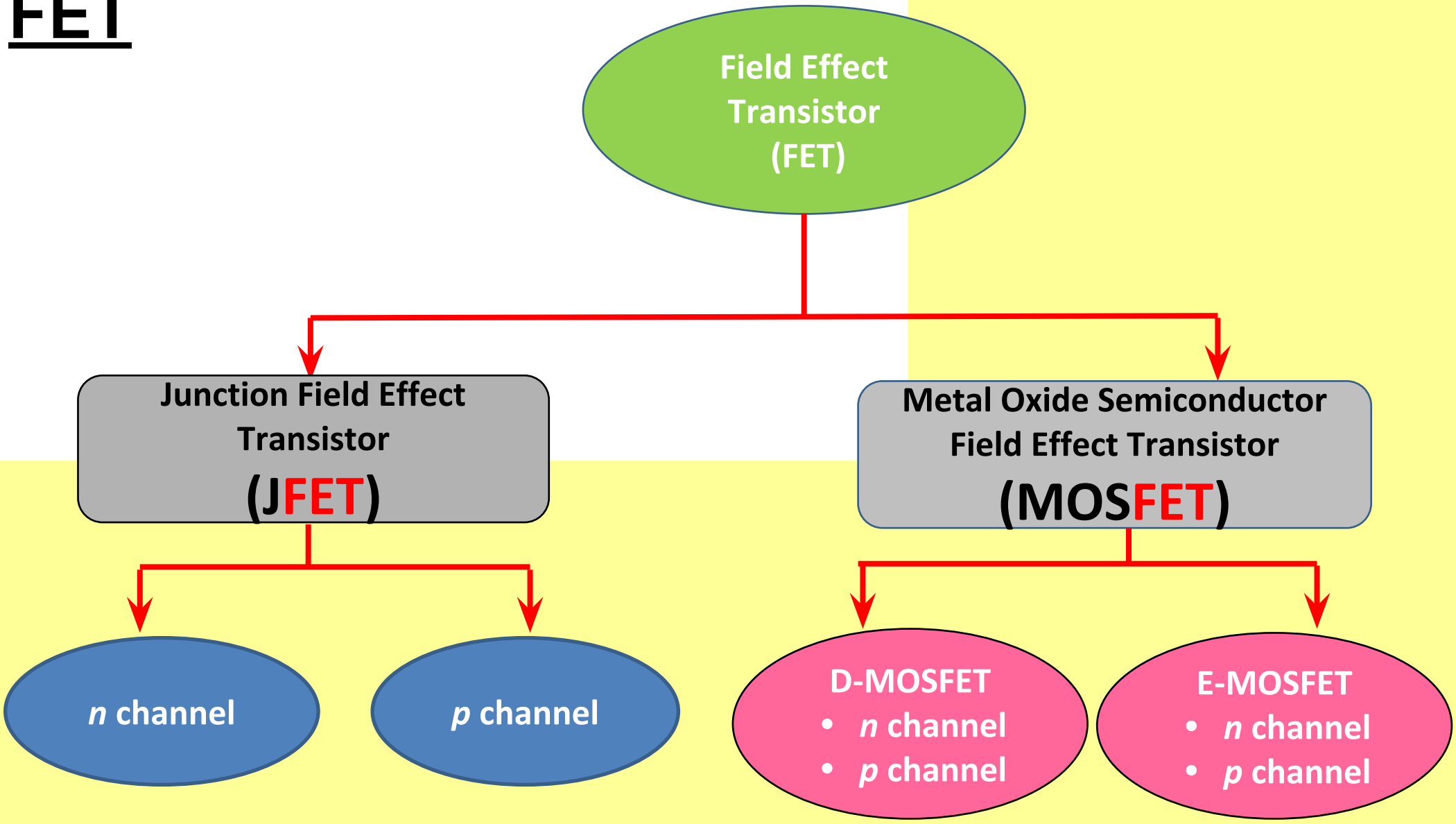
Introduction

- Field-effect transistors (FETs) are probably the simplest form of transistor
- Widely used in both analogue and digital applications
- Are characterized by a very high input resistance and small physical size, and they can be used to form circuits with a low power consumption
- Are widely used in very large-scale integration

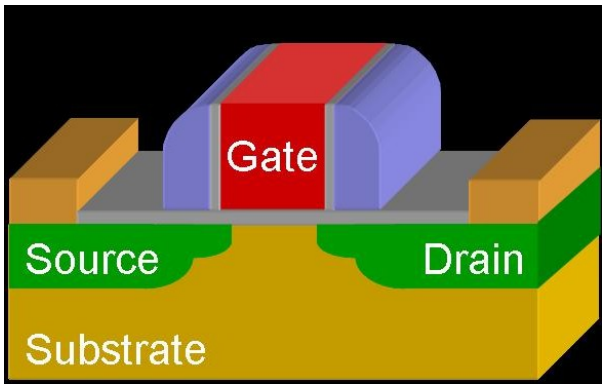


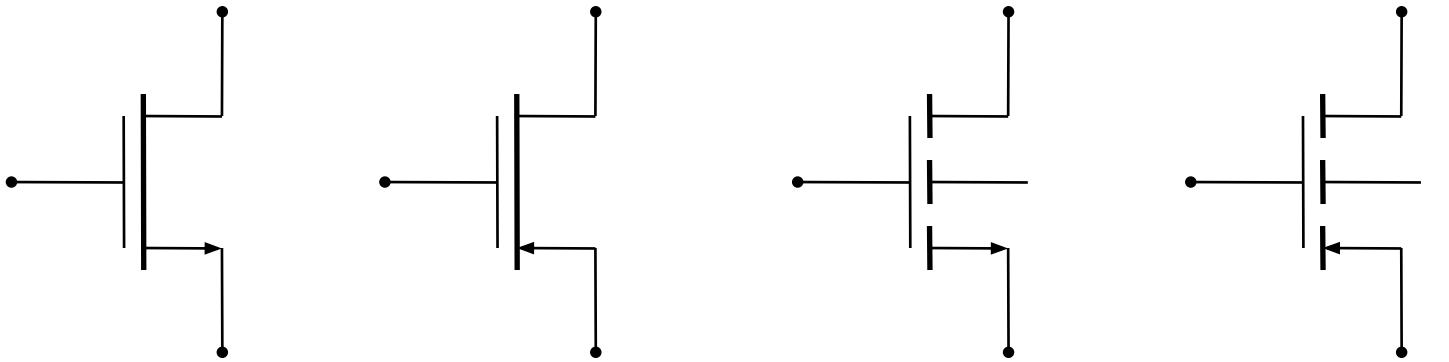
FET


Field Effect Transistor (FET)
Junction Field Effect Transistor (JFET)
Metal Oxide Semiconductor Field Effect Transistor (MOSFET)
n channel
p channel
D-MOSFET
• n channel
• p channel
E-MOSFET
• n channel
• p channel

MOSFET (Types)

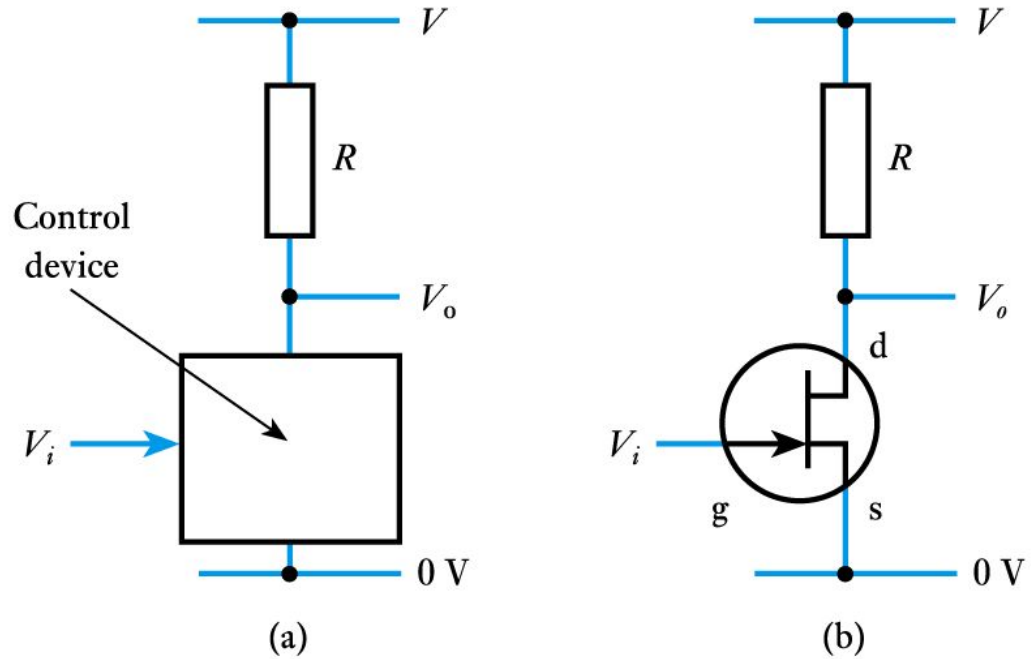
- Four types:
  - n-channel enhancement mode
    - Most common since it is cheapest to manufacture
  - p-channel enhancement mode
  - n-channel depletion mode
  - p-channel depletion mode





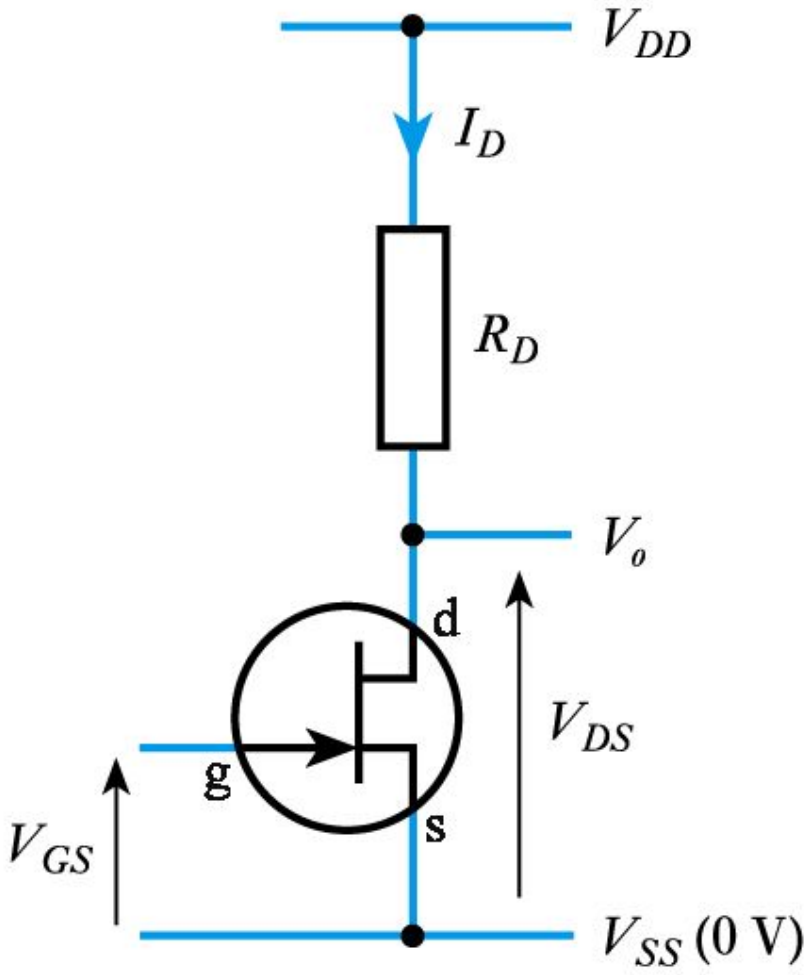
An Overview of Field-Effect Transistors

- Many forms, but basic operation is the same
- A voltage on a control input produces an electric field that affects the current between two other terminals
- when considering amplifiers we looked at a circuit using a ‘control device’
- FET is a suitable control device



Notation

- FETs are 3 terminal devices
- drain (d)
- source (s)
- gate(g)
- the gate is the control input

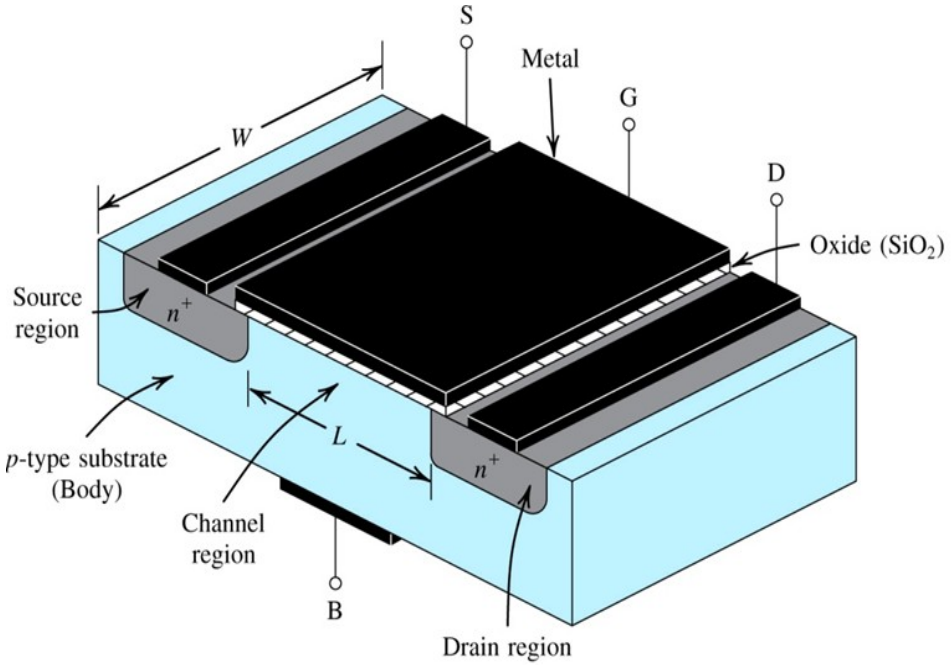


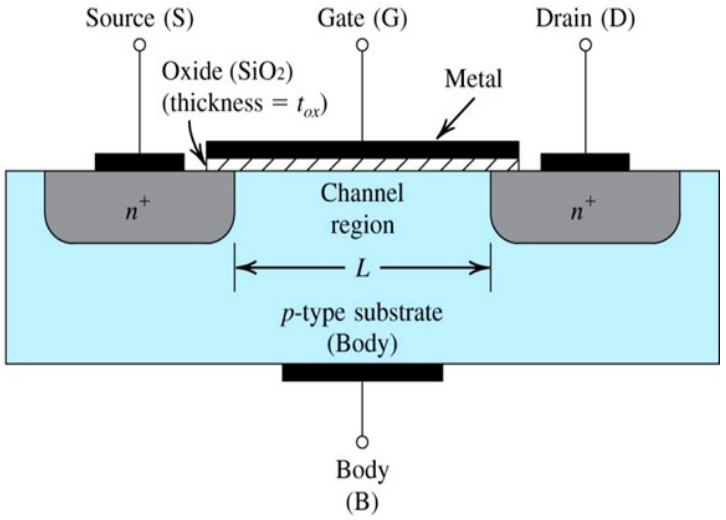
Insulated-Gate Field-Effect Transistors

- Such devices are sometimes called IGFETs (insulated-gate field-effect transistors) or sometimes MOSFETs (metal oxide semiconductor field-effect transistors)
- Digital circuits constructed using these devices are usually described as using MOS technology
- Here we will describe them as MOSFETs

Device Structure and Physical Operation

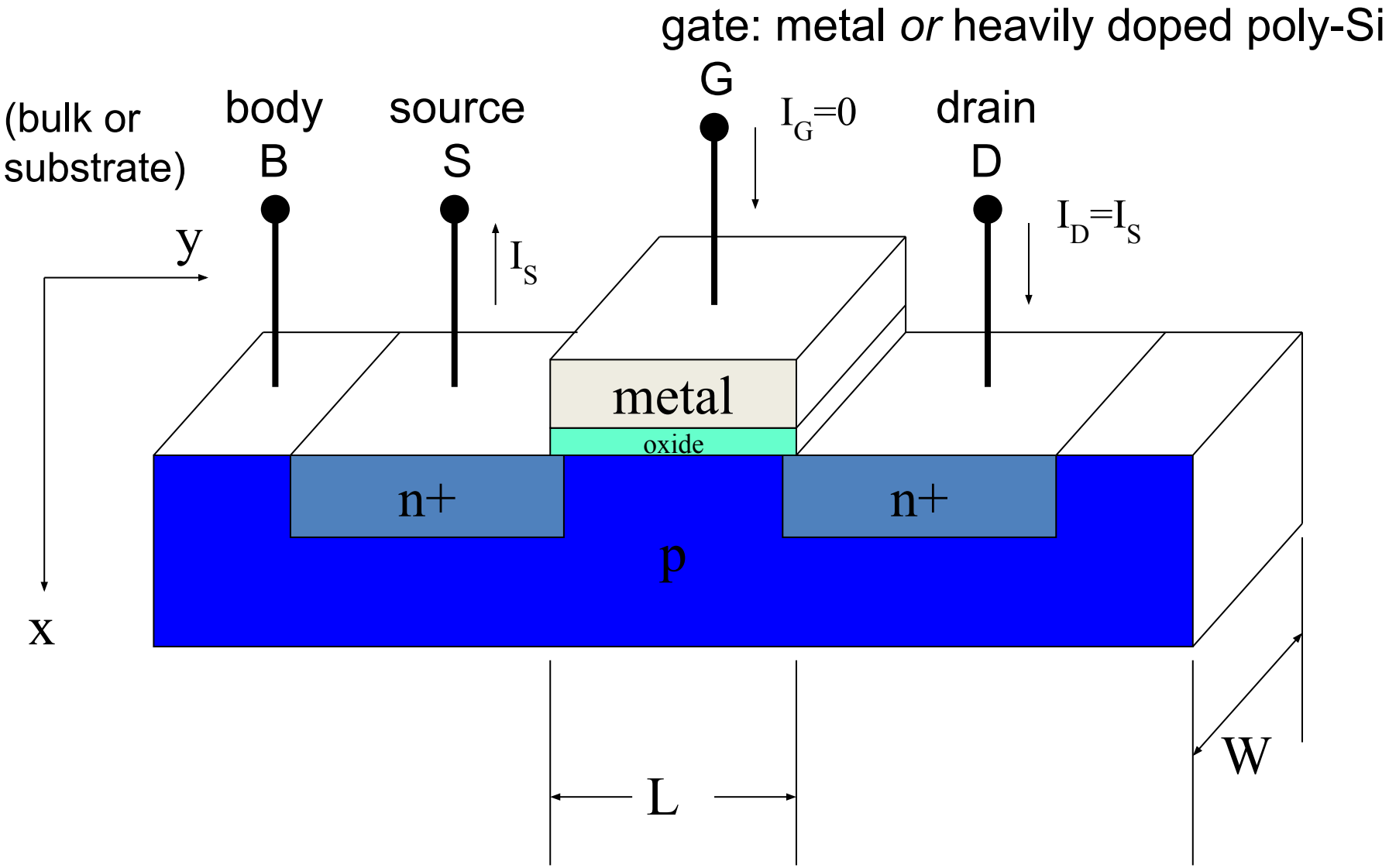
Device structure of MOSFET





- "MOS" ≡ metal-oxide-semiconductor structure
- MOSFET is a four-terminal device: gate (G), source (S), drain (D) and body (B)
- The device size (channel region) is specified by channel width (W) and channel length (L)
- Two kinds of MOSFETs: n-channel (NMOS) and p-channel (PMOS) devices
- The device structure is basically symmetric in terms of drain and source
- Source and drain terminals are specified by the operation voltage

Structure: *n-channel* MOSFET (NMOS)

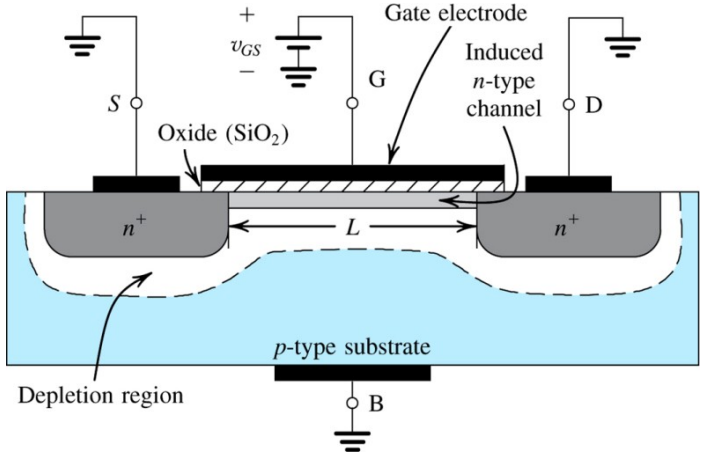


Operation with zero gate voltage

- The MOS structure form a parallel-plate plate capacitor with gate oxide layer in the middle
- Two *pn* junctions (S-B and D-B) are connected as back to back diodes
- The source and drain terminals are isolated by two depletion regions without conducting current
- The operating principles will be introduced by using the *n*-channel MOSFET as an example

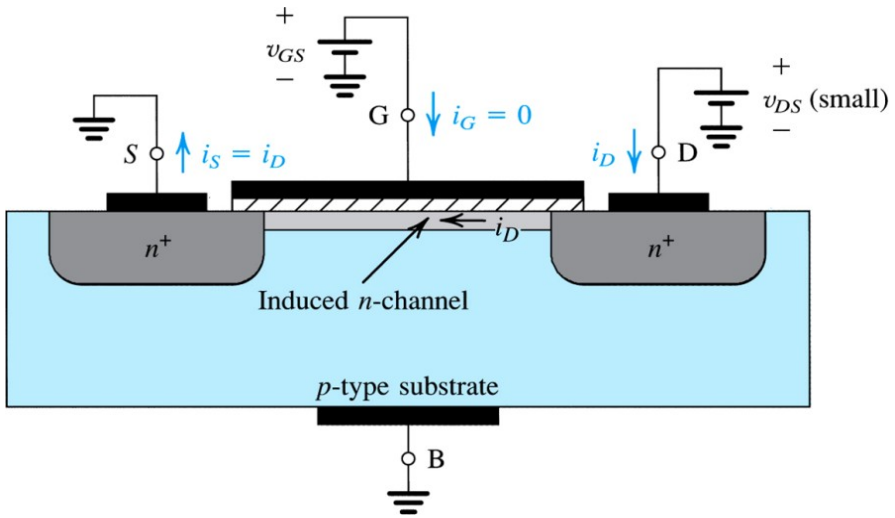
Creating a channel for current flow

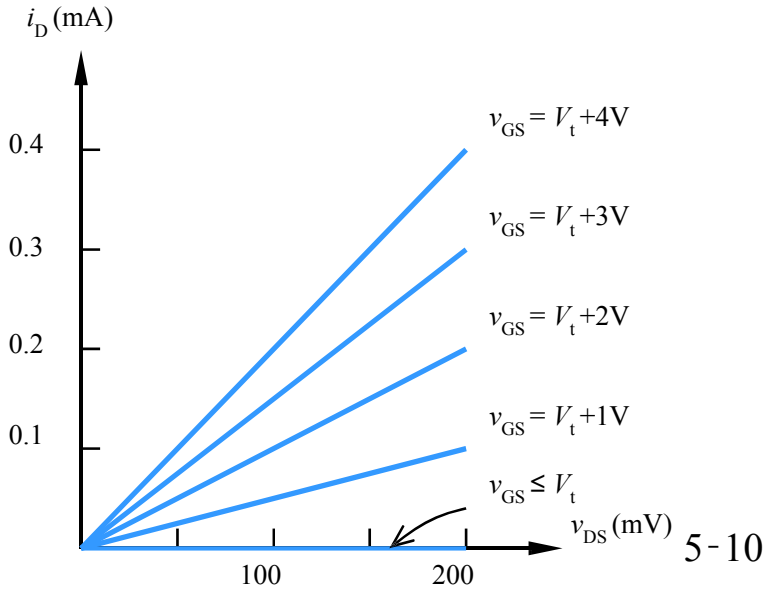
- Positive charges accumulate in gate as a positive voltage applies to gate electrode
- Electric field forms a depletion region by pushing holes in *p*-type substrate away from the surface
- Electrons accumulate on the substrate surface as gate voltage exceeds a **threshold voltage** V_t
- The induced *n* region thus forms a **channel** for current flow from drain to source
- The channel is created by inverting the substrate surface from *p*-type to *n*-type → **inversion layer**
- The field controls the amount of charge in the channel and determines the channel conductivity



Applying a small drain voltage

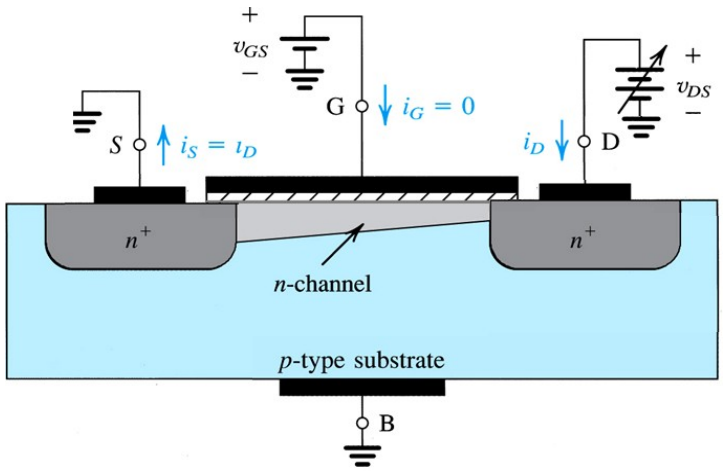
- A positive $v_{GS} > V_t$ is used to induce the channel → n-channel **enhancement-type** MOSFET
- Free electrons travel from source to drain through the induced n-channel due to a small v_{DS}
- The current i_D flows from drain to source (opposite to the direction of the flow of negative charge)
- The current is proportional to the number of carriers in the induced channel
- The channel is controlled by the **effective voltage** or **overdrive voltage**: $v_{OV} \equiv v_{GS} - V_t$
- The electron charge in the channel due to the overdrive voltage: $|Q| = C_{ox} W L v_{OV}$
- **Gate oxide capacitance** C_{ox} is defined as capacitance per unit area
- MOSFET can be approximated as a linear resistor in this region with a resistance value inversely proportional to the excess gate voltage

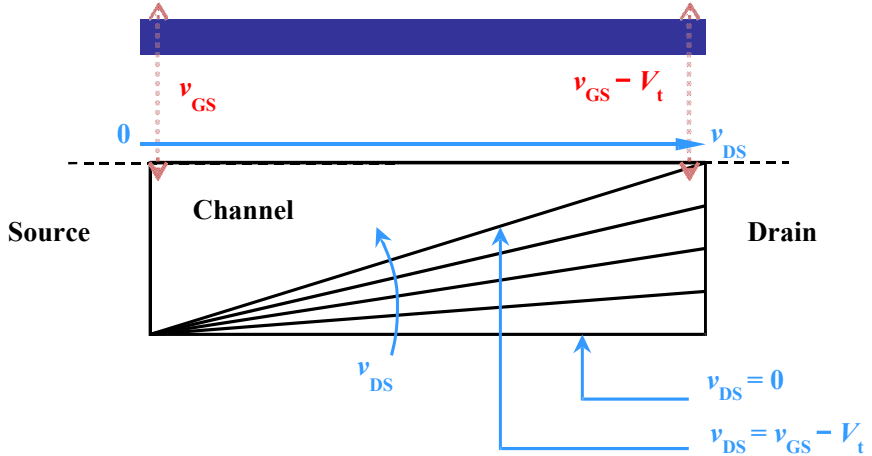




Operation as increasing drain voltage

- As v_{DS} increases, the voltage along the channel increases from 0 to v_{DS}
- The voltage between the gate and the points along the channel decreases from v_{GS} at the source end to $(v_{GS}-v_{DS})$ at the drain end
- Since the inversion layer depends on the voltage difference across the MOS structure, increasing v_{DS} will result in a tapered channel
- The resistance increases due to tapered channel and the i_D-v_{DS} curve is no longer a straight line
- At the point $v_{DSsat} = v_{GS} - V_t$, the channel is **pinched off** at the drain side
- Increasing v_{DS} beyond this value has little effect on the channel shape and i_D saturates at this value
- **Triode region**: $v_{DS} < v_{DSsat}$
- **Saturation region**: $v_{DS} \geq v_{DSsat}$





❑ Induced charge in the channel due to MOS capacitor:

$$Q_I(x) = -C_{ox}[v_{GS} - V_t - v(x)]$$

❑ Equivalent resistance dR along the channel:

$$dR = \frac{dx}{qn(x)\mu_n h(x)W} = \frac{dx}{\mu_n W Q_I(x)}$$

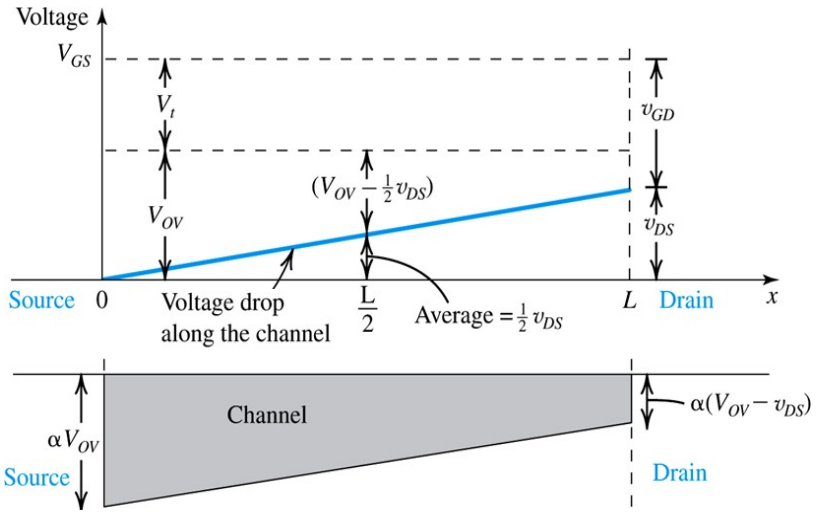
❑ I-V derivations: (more detail in next slide)

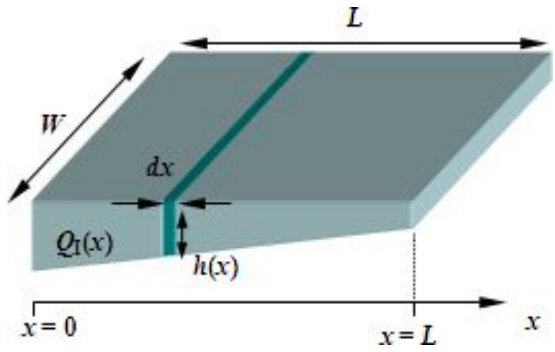
$$dv = i_D dR = \frac{i_D dx}{\mu_n W Q_I(x)} = \frac{i_D dx}{\mu_n C_{ox} W[v_{GS} - V_t - v(x)]}$$

$$\int_0^{v_{DS}} \mu_n C_{ox} W[v_{GS} - V_t - v(x)]dv = \int_0^L i_D dx$$

$$i_D = \mu_n C_{ox} \frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

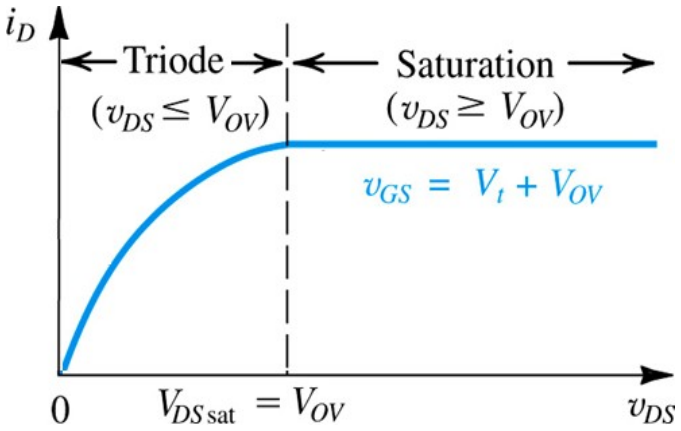
- Process transconductance parameter
- Aspect ratio: W/L
- Transconductance parameter ($\mu A/V^2$): $k_n = \mu_n C_{ox}(W/L)$





❑ Drain current of MOSFETs:

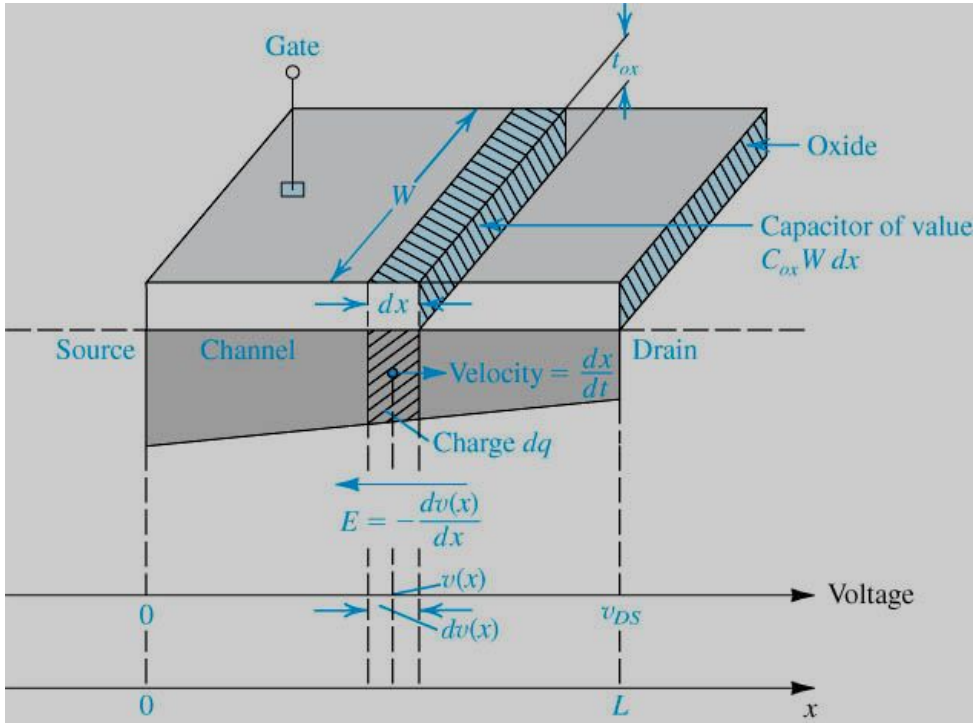
- Triode region:
- Saturation region



❑ On-resistance (channel resistance for small v_{DS}):

$$r_{DS} = 1/k_n(v_{GS} - V_t)$$

Derivation of the i_D-v_{DS} Relationship



$$i = \frac{dq}{dt} = \frac{dq}{dx}\frac{dx}{dt}$$

$$Q = CV \qquad C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \quad (4.2)$$

$$\varepsilon_{ox} = 3.9\varepsilon_0 = 3.9\times 8.854\times 10^{-12} = 3.45\times 10^{-11}\ \text{F/m}$$

$$dq = -C_{ox}(Wdx)\left[\upsilon_{GS} - \upsilon(x) - \mathrm{V}_t\right] \quad (4.3)$$

$$E(x) = -\frac{d\upsilon(x)}{dx} \quad (\because\ E = -\nabla V)$$

$$\frac{dx}{dt} = -\mu_n E(x) = \mu_n \frac{d\upsilon(x)}{dx} \quad (4.4)$$

$$i = -\mu_n C_{ox} W\left[\upsilon_{GS} - \upsilon(x) - \mathrm{V}_t\right]\frac{d\upsilon(x)}{dx}$$

$$i_D = -i = \mu_n C_{ox} W\left[\upsilon_{GS} - \upsilon(x) - \mathrm{V}_t\right]\frac{d\upsilon(x)}{dx}$$

$$i_D dx = \mu_n C_{ox} W\left[\upsilon_{GS} - \mathrm{V}_t - \upsilon(x)\right]d\upsilon(x)$$

$$\int_0^L i_D dx = \int_0^{\upsilon_{DS}} \mu_n C_{ox} W\left[\upsilon_{GS} - \mathrm{V}_t - \upsilon(x)\right]d\upsilon(x)$$

$$i_D = (\mu_n C_{ox})\left(\frac{W}{L}\right)\left[(\upsilon_{GS} - \mathrm{V}_t)\upsilon_{DS} - \frac{1}{2}\upsilon_{DS}^2\right] \quad (4.5)$$

At the beginning of saturation region, $\upsilon_{DS} = \upsilon_{GS} - V_t$

$$i_D = \frac{1}{2}(\mu_n C_{ox})\left(\frac{W}{L}\right)(\upsilon_{GS} - \mathrm{V}_t)^2 \quad (4.6)$$

$$k_n' = \mu_n C_{ox} \quad (4.7) \qquad C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \quad (4.2)$$

$$i_D = k_n'\left(\frac{W}{L}\right)\left[(\upsilon_{GS} - \mathrm{V}_t)\upsilon_{DS} - \frac{1}{2}\upsilon_{DS}^2\right] \quad \textbf{(Triode region)} \quad (4.5a)$$

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(\upsilon_{GS} - \mathrm{V}_t)^2 \quad \textbf{(saturation region)} \quad (4.6a)$$

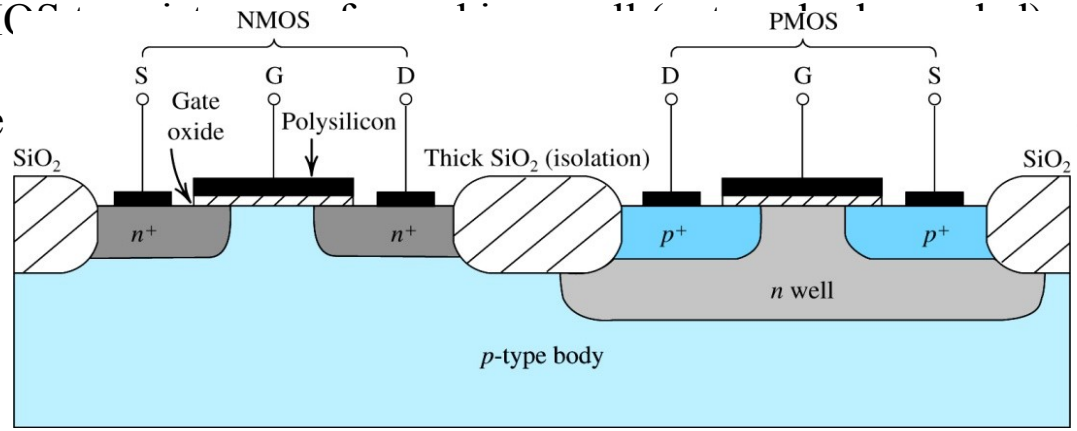
$\left(\frac{W}{L}\right)$: **Aspect ratio of the MOSFET**

The *p*-channel enhancement-type MOSFET

- *p*-channel enhanced-type MOSFETs are fabricated on *n*-type substrate with p^+ source and p^+ drain
- Normally, source is connected to high voltage and drain is connected to low voltage
- As a negative voltage applies to the gate, the resulting field pushes electrons in *n*-type substrate away from the surface, leaving behind a carrier-depletion region
- As gate voltage exceeds a negative **threshold voltage** V_t, holes accumulate on the substrate surface
- A *p*-type channel (**inversion layer**) is induced for current flow from source to drain
- Negative gate voltage is required to induce the channel → **enhancement-type** MOSFET

Complementary MOS (CMOS)

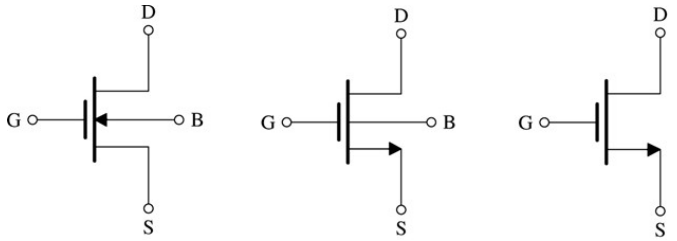
- CMOS technology employs both PMOS and NMOS devices
- If substrate is *p*-type, PMOS transistors are formed in *n* well (*n*-type body needed)
- If substrate is *n*-type, NMOS transistors are formed in *p* well (*p*-type body needed)
- The substrate and well are used for device isolation



Current-Voltage Characteristics

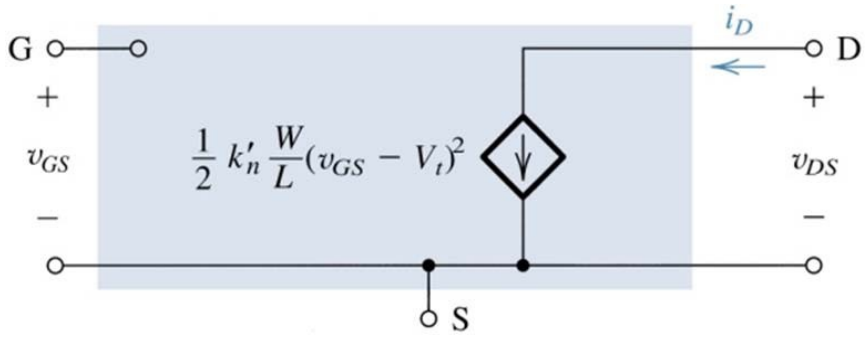
Circuit symbol

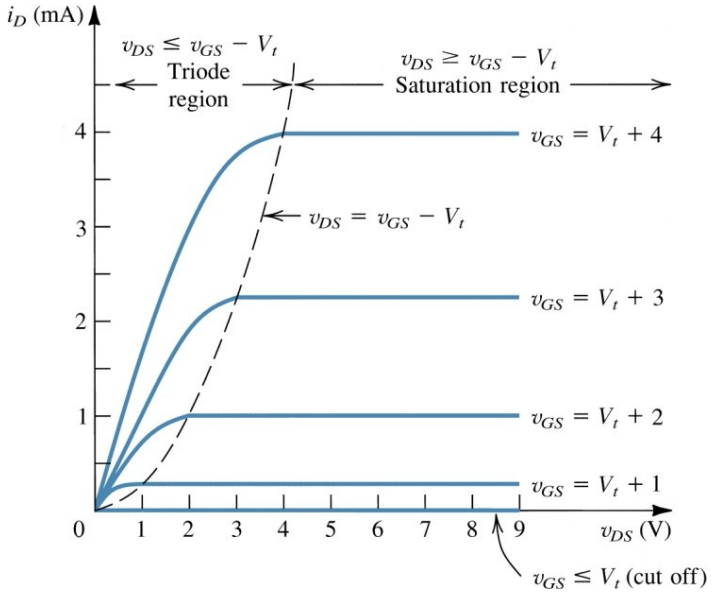
- n-channel enhancement-mode MOSFET

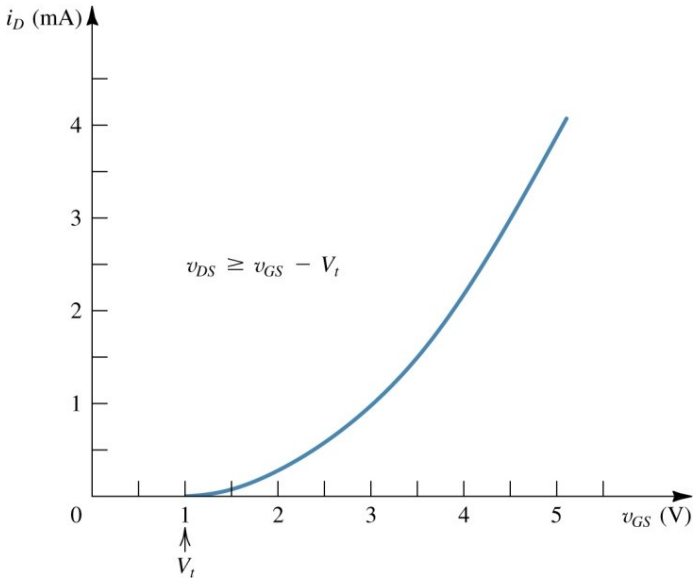


The current-voltage characteristics

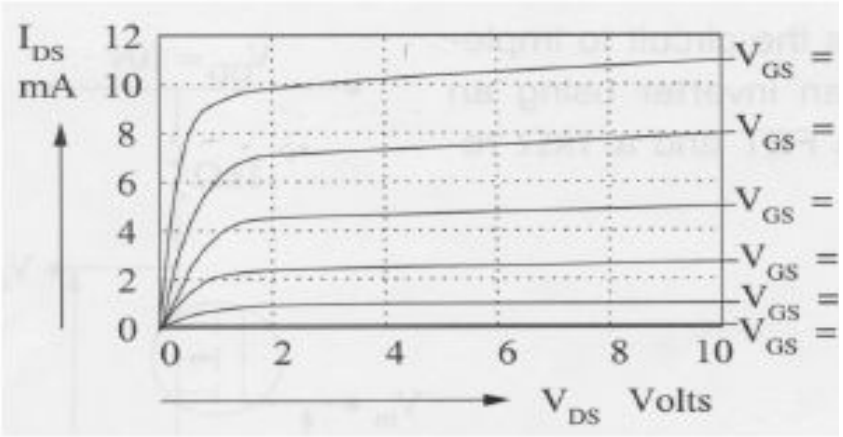
- Cut-off region: ($v_{GS} \le V_t$)
  - $i_D = 0$
- Triode region: ($v_{GS} > V_t$ and $v_{DS} < v_{GS} - V_t$)
- Saturation: ($v_{GS} > V_t$ and $v_{DS} \ge v_{GS} - V_t$)
- large-signal model (saturation)



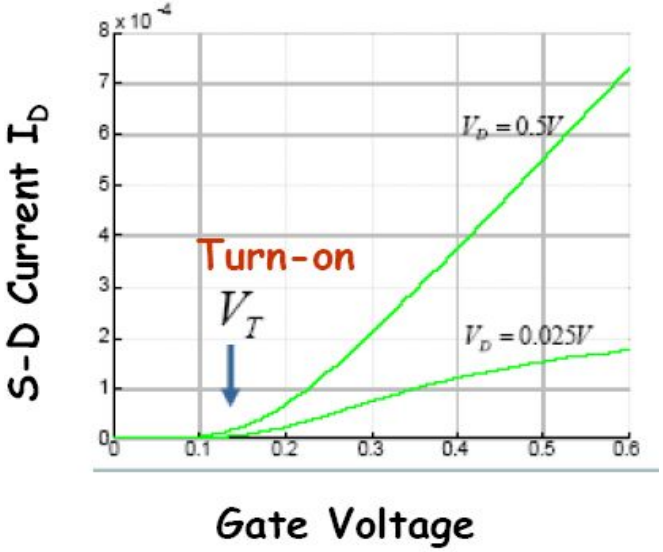


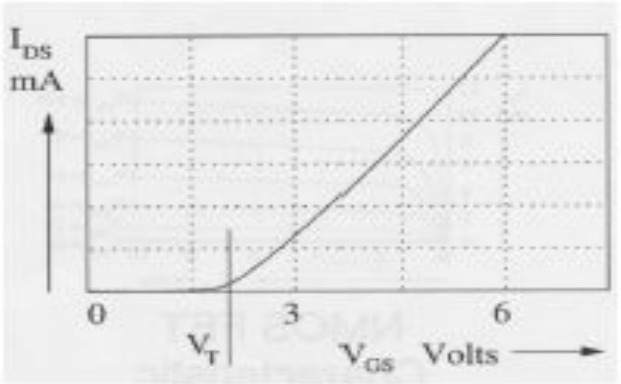


n-MOSFET Characteristics

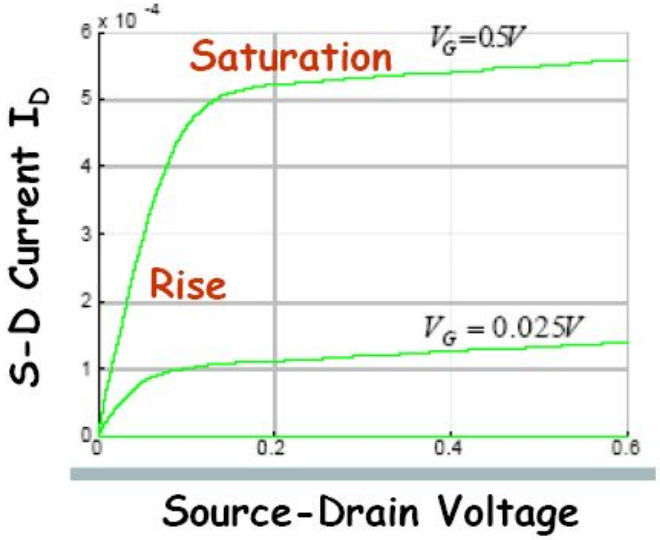


Plots V-I characteristics of the device for various Gate voltages (VGS)





At a constant value of VDS , we can also see that IDS is a function of the Gate voltage, VGS
The transistor begins to conduct when the Gate voltage, VGS , reaches the Threshold voltage: VT



Current-Voltage Characteristics

Cut-off: $V_{GS} < V_T$

$$I_D = I_S = 0$$

Triode: $V_{GS} > V_T$ and $V_{DS} < V_{GS} - V_T$

$$I_D = k_n'(W/L)[(V_{GS}-V_T)V_{DS} - {}^1/_2 V_{DS}^2]$$

Saturation: $V_{GS} > V_T$ and $V_{DS} > V_{GS} - V_T$

$$I_D = {}^1/_2 k_n'(W/L)(V_{GS}-V_T)^2$$

where k_n' = (electron mobility)x(gate capacitance)

$= \mu_n(\varepsilon_{ox}/t_{ox})$ …*electron velocity* $= \mu_n \boldsymbol{E}$

and V_T depends on the doping concentration and gate material used

(…more details later)

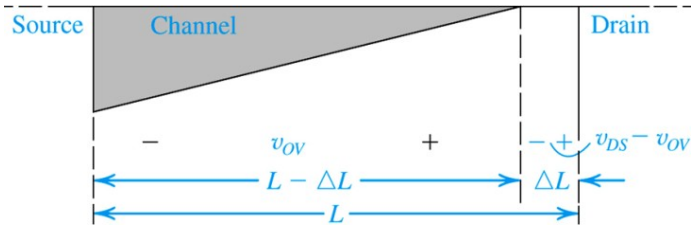
Channel length modulation

- The channel pinch-off point moves slightly away from drain as $v_{DS} > v_{DSsat}$
- The effective channel length (L_{eff}) reduces with v_{DS}
- Electrons travel to pinch-off point will be swept to drain by electric field
- The length accounted for conductance in the channel is replaced by L_{eff}:

$$\int_0^{L_{eff}} k_n' W[v_{GS} - V_t - v(x)]dv = \int_0^{v_{DS}} i\,dx$$

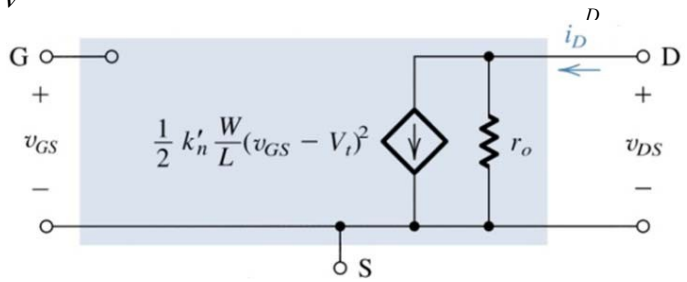
$$i_D = \frac{1}{2}k_n'\frac{W}{L_{eff}}(v_{GS} - V_t)^2 \approx \frac{1}{2}k_n'\frac{W}{L - \Delta L}(v_{GS} - V_t)^2 \approx \frac{1}{2}k_n'\frac{W}{L}(v_{GS} - V_t)^2\left(1 + \frac{\Delta L}{L}\right)$$

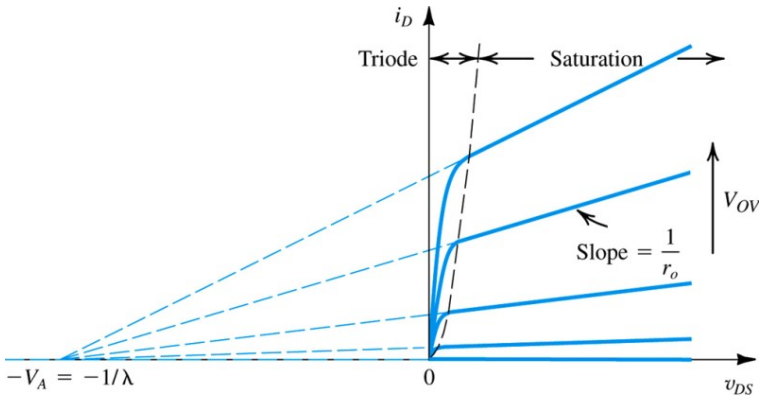
assuming that $\frac{\Delta L}{L} \propto v_{DS} \rightarrow i_D = \frac{1}{2}k_n'\frac{W}{L}(v_{GS} - V_t)^2(1 + \lambda v_{DS})$



Finite output resistance

$$r_o \equiv \left[\frac{\partial i_D}{\partial v_{DS}}\right]^{-1}_{v_{GS}=constant} = \left[\lambda\frac{k_n'}{2}\frac{W}{L}(v_{GS} - V_t)^2\right]^{-1} \approx \frac{1}{\lambda I_D} = \frac{V_A}{I_D}$$

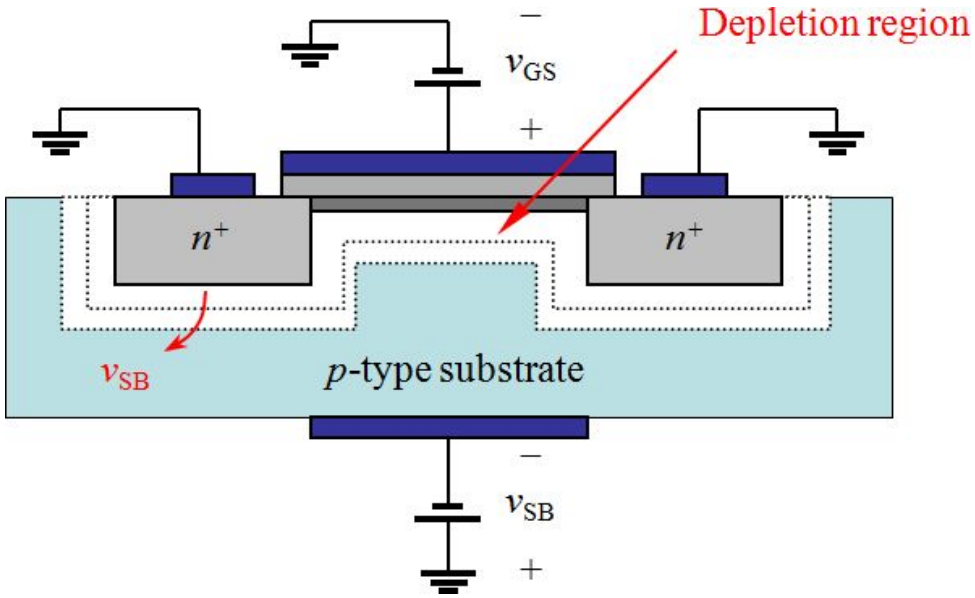




- V_A (**Early voltage**) = $1/\lambda$ is proportional to channel length: $V_A = V'_A L$
- V'_A is process-technology dependent with a typical value from 5 ~ 50 V/μm
- Due to the dependence of i_D on v_{DS}, MOSFET shows **finite output resistance** in saturation region

The body effect

- The BS and BD junction should be reverse biased for the device to function properly
- Normally, the body of a n-channel MOSFET is connected to the most negative voltage
- The depletion region widens in BS and BD junctions and under the channel as V_{SB} increases
- **Body effect**: V_t increases due to the excess charge in the depletion region under the channel
- The body effect can cause considerable degradation in circuit performance



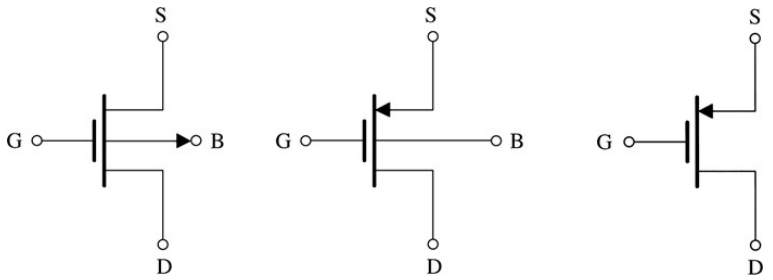
Temperature effect

- V_t decreases by ~2mV for every 1°C rise → i_D increases with temperature
- k'_n decreases with temperature → i_D decreases with increasing temperature
- For a given bias voltage, the overall observed effect of a temperature increase is a decrease in i_D

Breakdown and input protection

- Weak avalanche
  - *pn* junction between the drain and substrate suffers avalanche breakdown as V_{DS} increases
  - Large drain current is observed
  - Typical breakdown voltage 20 ~ 150 V
- Punch-through
  - Occurs at lower voltage (~20 V) for short channel devices
  - Drain current increases rapidly as the drain depletion region extends through the channel
  - Does not result in permanent damage to the device
- Gate-oxide breakdown
  - Gate-oxide breakdown occurs when gate-to-source voltage exceeds 30 V
  - Permanent damage to the device
- Input Protection
  - Protection circuit is needed for the input terminals of MOS integrated circuits
  - Using clamping diode for the input protection

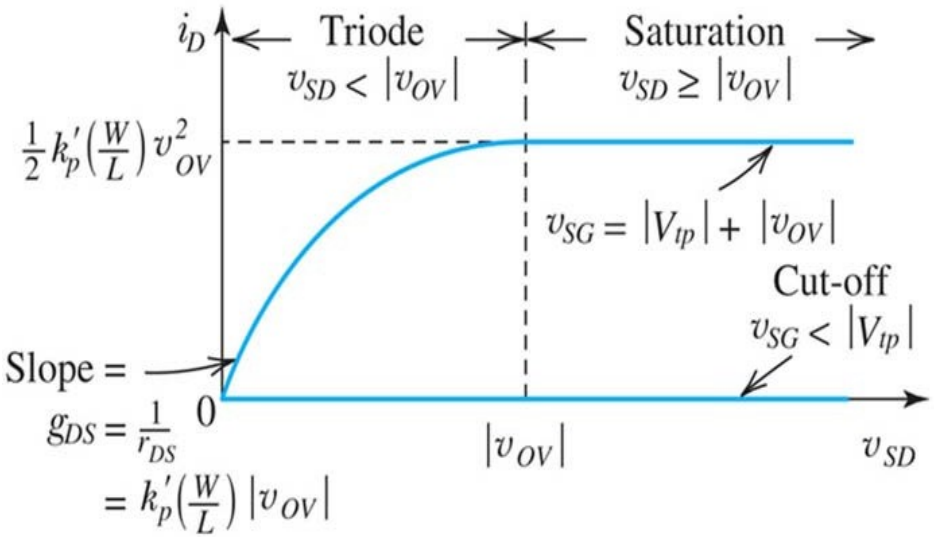
The p-channel enhancement-type MOSFET



- For a PMOS, the source is connected to high voltage and the drain is connected to low voltage
- To induce the p-channel for the MOSFET, a negative v_{GS} is required → V_t (threshold voltage) < 0V
- The body is normally connected to the most positive voltage

The current-voltage characteristics

- Cut-off region: ($v_{GS} \geq V_{tp}$)
  - $i_D = 0$
- Triode region: ($v_{GS} < V_{tp}$ and $v_{DS} > v_{GS} - V_{tp}$)
- Saturation: ($v_{GS} < V_{tp}$ and $v_{DS} \leq v_{GS} - V_{tp}$)



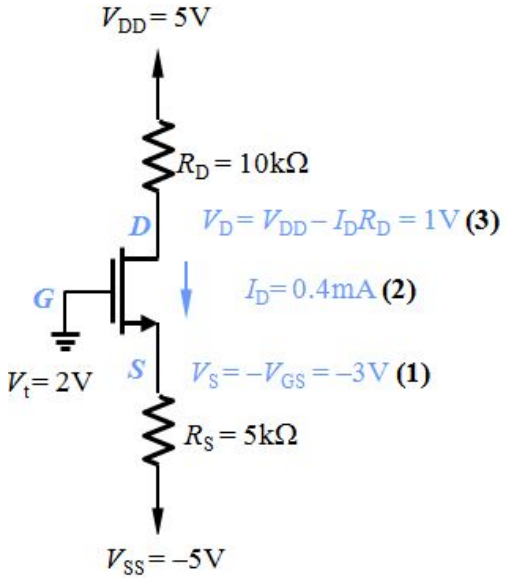
- Transconductance parameter $k'_p = \mu_p C_{ox} \approx 0.4\, k'_n$
- The values of v_{GS}, v_{DS}, V_t and λ for p-channel MOSFET operation are all negative
- Drain current i_D is still defined as a positive current

MOSFET Circuits at DC

DC analysis for MOSFET circuits

- ❑ Assume the operation mode and solve the dc bias utilizing the corresponding current equation
- ❑ Verify the assumption with terminal voltages (cutoff, triode and saturation)
- ❑ If the solution is invalid, change the assumption of operation mode and analyze again

DC analysis example

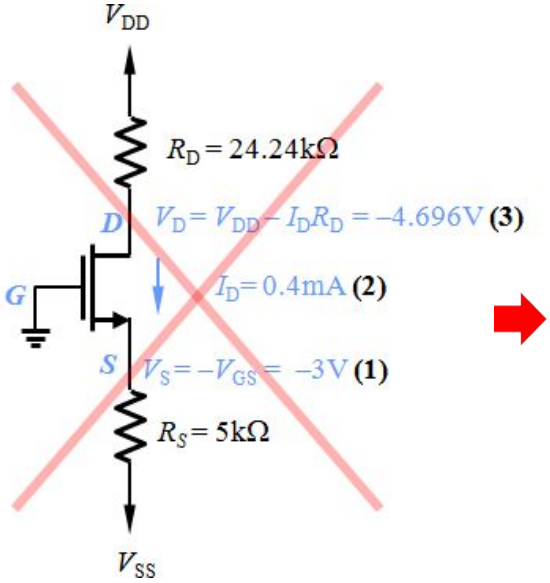


Assuming MOSFET in saturation

$-V_{SS} = V_{GS} + I_D R_S = V_{GS} + \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2 R_S$

$\rightarrow V_{GS} = 3V$ or $1V$ (not a valid solution)

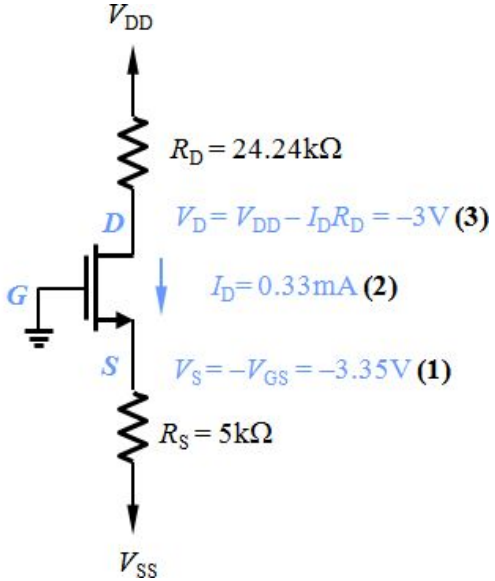
$(V_{DS} = 4V) \geq (V_{GS} - V_t = 1V) \rightarrow$ saturation



Assuming MOSFET in saturation

$\rightarrow V_{GS} = 3V$ and $V_{DS} = -1.696V$

$V_{DS} < V_{GS} - V_t \rightarrow$ not in saturation!



Assuming MOSFET in triode

$I_D = k_n' \frac{W}{L} [(V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2]$

$V_{GS} + I_D R_S = -V_{SS}$

$V_{DS} + I_D (R_D + R_S) = V_{DD} - V_{SS}$

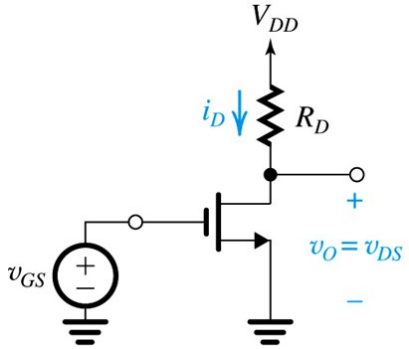
$\rightarrow V_{GS} = 3.35V$, $V_{DS} = 0.35V$ and $I_D = 0.33mA$

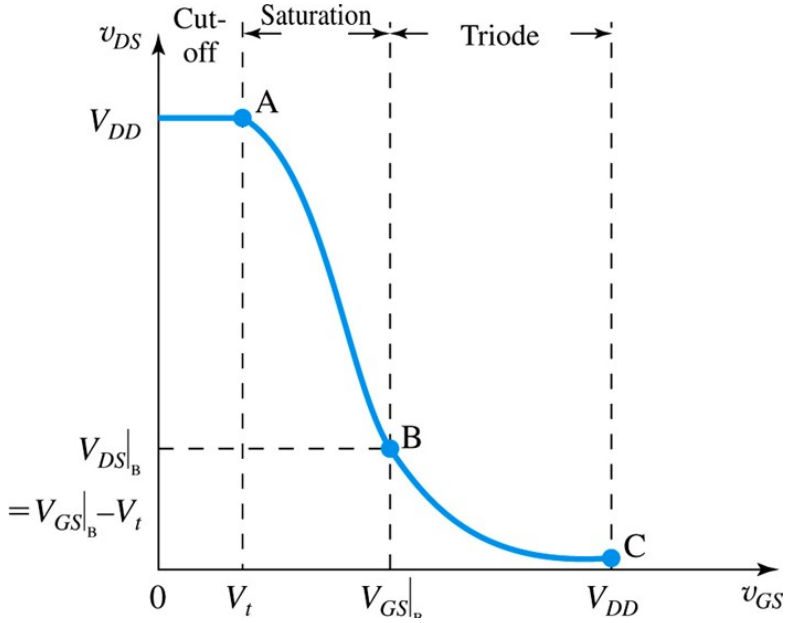
$V_{DS} < V_{GS} - V_t \rightarrow$ in triode

Applying the MOSFET in Amplifier Design

MOSFET voltage amplifier

- MOSFET with a resistive load R_D can be used as a voltage amplifier
- The voltage transfer characteristic (VTC)
  - The plot of v_I (v_{GS}) versus v_O (v_{DS})
  - DC analysis as v_{GS} increases from 0 to V_{DD}
  - Cutoff mode: (0 V ≤ $v_{GS} < V_t$)
    - $i_D = 0$
    - $v_O = v_{DS} = V_{DD}$
  - Saturation mode: ($v_{GS} > V_t$)
    - $i_D = \frac{1}{2} k_n (v_{GS} - V_t)^2$
    - $v_O = v_{DS} = V_{DD} - \frac{1}{2} k_n (v_{GS} - V_t)^2 R_D$
  - Triode mode: (v_{GS} further increases)
    - $i_D = k_n [(v_{GS} - V_t) v_{DS} - \frac{1}{2} v_{DS}^2]$
    - $v_O = v_{DS} = V_{DD} - k_n [(v_{GS} - V_t) v_{DS} - \frac{1}{2} v_{DS}^2] R_D$





Biasing the MOSFET to obtain linear amplification

- The slope in the VTC indicates voltage gain
- MOSFET in saturation can be used as voltage amplification
- Point Q is known as **bias point** or **dc operating point**

$$V_{DS} = V_{DD} - \frac{1}{2}k_n(V_{GS} - V_t)^2 R_D$$

- The signal to be amplified is superimposed on V_{GS}
  - $v_{GS}(t) = V_{GS} + v_{gs}(t)$
- The time-varying part in $v_{GS}(t)$ is the amplified signal
- The circuit can be used as a linear amplifier if:
  - A proper bias point is chosen for gain
  - The input signal is small in amplitude

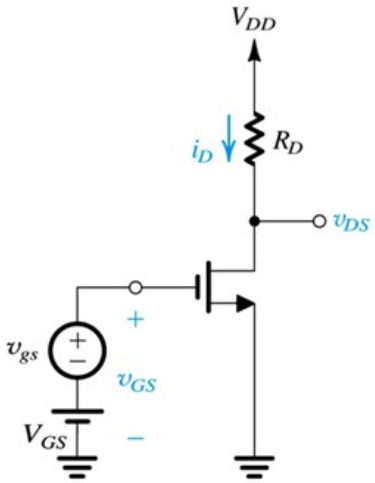
The small-signal voltage gain

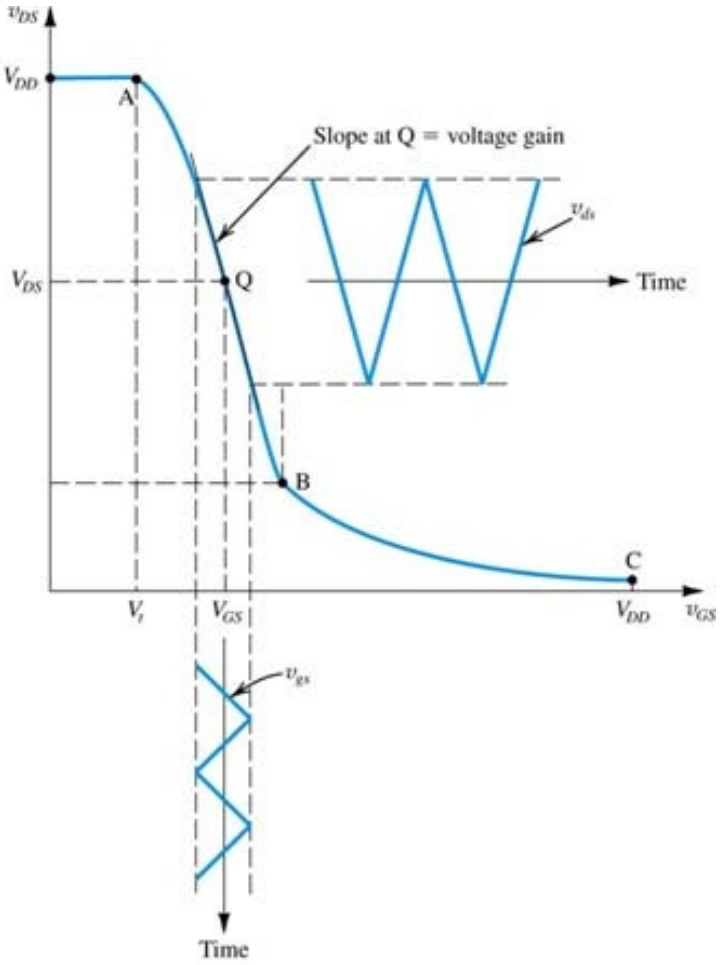
- The amplifier gain is the slope at Q:

$$A_v \equiv \left.\frac{dv_{DS}}{dv_{GS}}\right|_{v_{GS}=V_{GS}} = -k_n(V_{GS} - V_t)R_D = -k_n V_{OV} R_D$$

- Maximum voltage gain of the amplifier

$$|A_v| = \left|-\frac{I_D R_D}{V_{OV}}\right| \le \left|\frac{V_{DD}}{V_{OV}/2}\right| = |A_{v\max}|$$



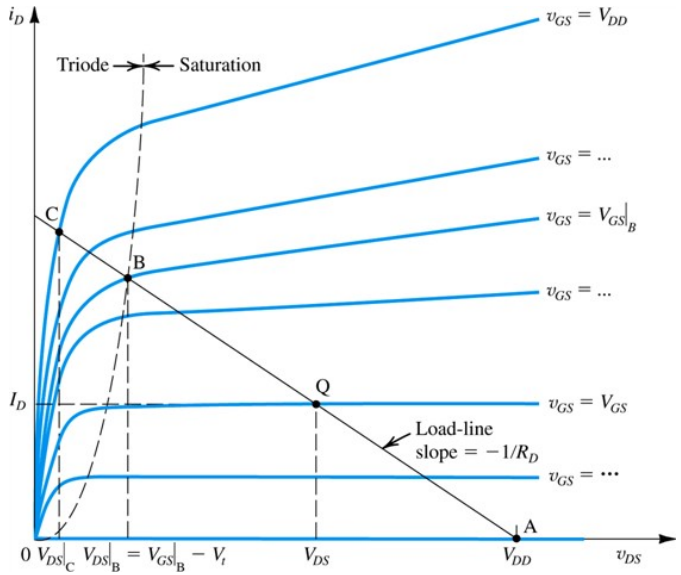


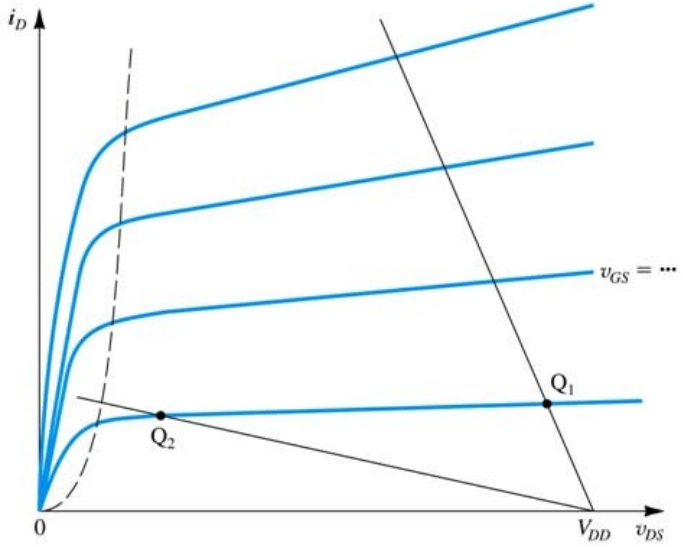
Determining the VTC by graphical analysis

- Provides more insight into the circuit operation
- **Load line**: the straight line represents in effect the load
  - $i_D = (V_{DD} - v_{DS})/R_D$
- The operating point is the intersection point

Locating the bias point *Q*

- The bias point (intersection) is determined by properly choosing the load line
- The output voltage is bounded by V_{DD} (upper bound) and V_{OV} (lower bound)
- The load line determines the voltage gain
- The bias point determines the maximum upper/lower voltage swing of the amplifier





The MOSFET as an Amplifier and as Switch

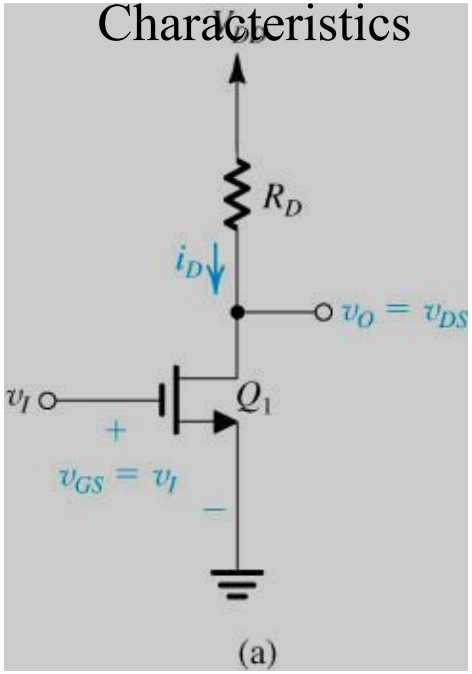
The MOSFET acts as a Voltage-Controlled Current Source ! ⇒ *Transconductance Amplifier !*

v_{GS} → i_D ⇒ **Saturation Region** !!!

$$i_D = \frac{1}{2} k_n' \frac{W}{L} (v_{GS} - V_t)^2 \quad \textbf{(4.20) Saturation current}$$ ⇒ Nonlinear !

For linear amplification, we need dc-bias voltage V_{GS} and require small input signal v_{gs}.

4.4.1 Large-Signal Operation-The Transfer Characteristics



Basic structure of the Common-Source (CS) (ground-source) amplifier.

$$v_O = v_{DS} = V_{DD} - R_D i_D \qquad \textbf{(4.35)}$$

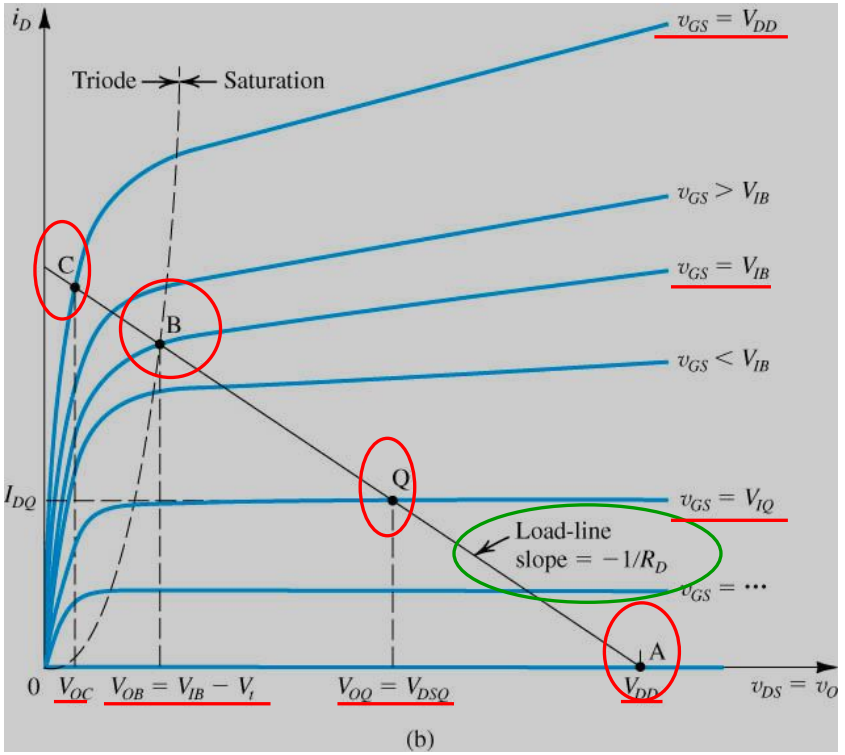
4.4.2 Graphical Derivation of The Transfer Characteristics

$$v_{DS} = V_{DD} - R_D i_D \quad \textbf{(4.36)}$$

$$i_D = \frac{V_{DD}}{R_D} - \frac{1}{R_D} v_{DS} \quad \textbf{(4.37)}$$

Load-line equation

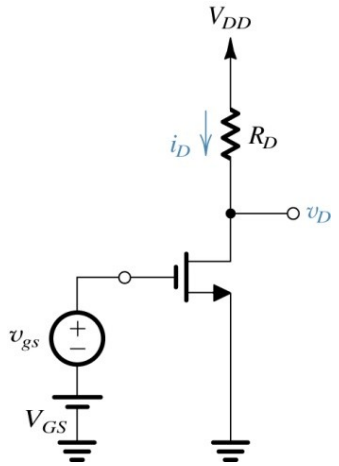
For a given input $v_I(v_{GS})$, We can find output v_O (v_{DS}).



Small-Signal Operation and Models

The DC bias point

- MOSFET in saturation
  - Drain current: $I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2 = \frac{1}{2} k_n (V_{GS} - V_t)^2 = \frac{1}{2} k_n V_{OV}^2$
  - Drain voltage: $V_{DS} = V_{DD} - I_D R_D > V_{OV}$
- The small-signal circuit parameters are determined by the bias point



The small-signal operation

- The small-signal drain current:

$$v_{GS} = V_{GS} + v_{gs}$$

$$i_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} + v_{gs} - V_t)^2 = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2 + k_n' \frac{W}{L} (V_{GS} - V_t) v_{gs} + \frac{1}{2} k_n' \frac{W}{L} v_{gs}^2$$

$$\approx \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2 + k_n' \frac{W}{L} (V_{GS} - V_t) v_{gs} = I_D + i_d$$

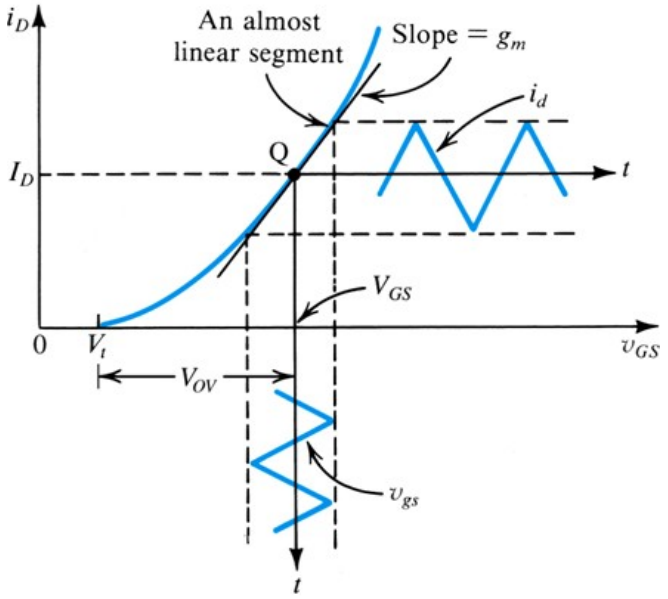
$$\rightarrow i_d = k_n' \frac{W}{L} (V_{GS} - V_t) v_{gs}$$

- The small-signal voltage gain:

$$v_D = V_{DD} - i_D R_D = V_{DD} - (I_D + i_d) R_D = V_D - i_d R_d = V_D + v_d$$

$$\rightarrow v_d = -i_d R_D = -k_n' \frac{W}{L} V_{OV} R_D v_{gs}$$

$$\rightarrow A_v \equiv \frac{v_d}{v_{gs}} = -k_n' \frac{W}{L} V_{OV} R_D$$



The small-signal parameters

- Transconductance (g_m): describes how i_d change with v_{gs}

$$g_m \equiv \frac{i_d}{v_{gs}} = \frac{\partial i_D}{\partial v_{GS}}\Big|_{v_{GS}=V_{GS}} = k_n' \frac{W}{L}(V_{GS} - V_t) = \sqrt{2k_n' \frac{W}{L} I_D}$$

- Output resistance (r_o): describes how i_d change with v_{ds}

$$r_o \equiv \left[\frac{\partial i_D}{\partial v_{DS}}\right]^{-1}_{v_{GS}=constant} \approx \frac{1}{\lambda I_D} = \frac{V_A}{I_D}$$

  - Drain current varies with v_{DS} due to channel length modulation
  - Finite r_o to model the linear dependence of i_D on v_{DS}
  - The effect can be neglected if r_o is sufficiently large

- Body transconductance (g_{mb}): describes how i_d changes with v_{bs}

$$i_D = \frac{1}{2} k_n' \frac{W}{L}(v_{GS} - V_t)^2$$

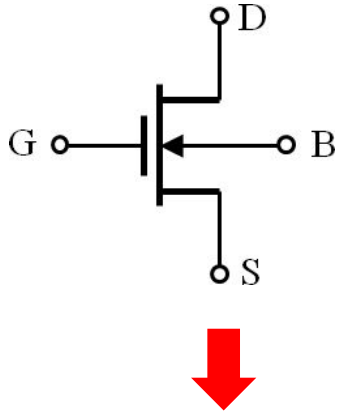
$$\rightarrow g_{mb} \equiv \frac{\partial i_D}{\partial v_{BS}}\Big|_{\substack{v_{GS}=constant \\ v_{DS}=constant}} = \frac{\partial i_D}{\partial V_t}\frac{\partial V_t}{\partial v_{BS}} = -k_n' \frac{W}{L}(v_{GS} - V_t)\frac{\partial V_t}{\partial v_{BS}} = g_m \frac{\partial V_t}{\partial v_{SB}}$$

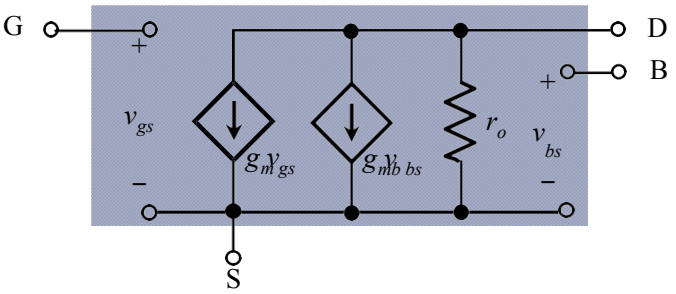
$$V_t = V_{t0} + \gamma\left[\sqrt{2\varphi_F + v_{SB}} - \sqrt{2\varphi_F}\right] \text{ where } \gamma = \sqrt{2qN_A\varepsilon_{Si}} / C_{ox}$$

$$\rightarrow \frac{\partial V_t}{\partial v_{SB}} \equiv \chi = \frac{\gamma}{2\sqrt{2\varphi_F + V_{SB}}}$$

$$g_{mb} = g_m \chi$$

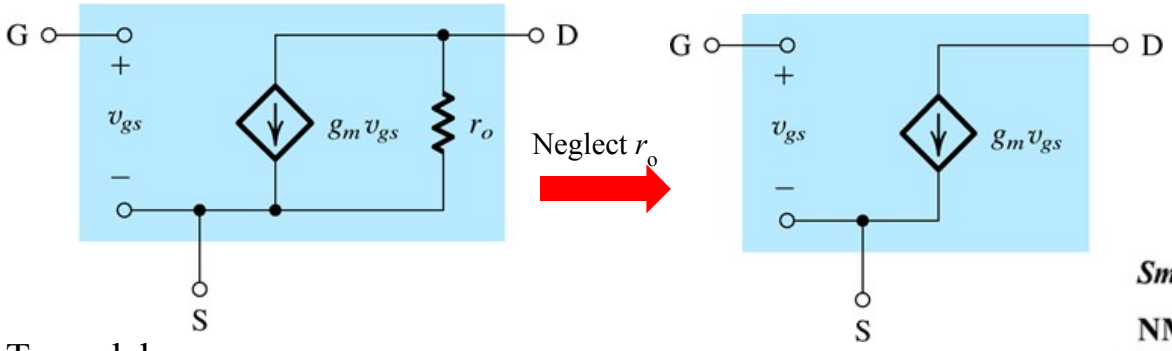
  - The body effect of the MOSFET is modeled by g_{mb}
  - Can be neglected if body and source are connected together



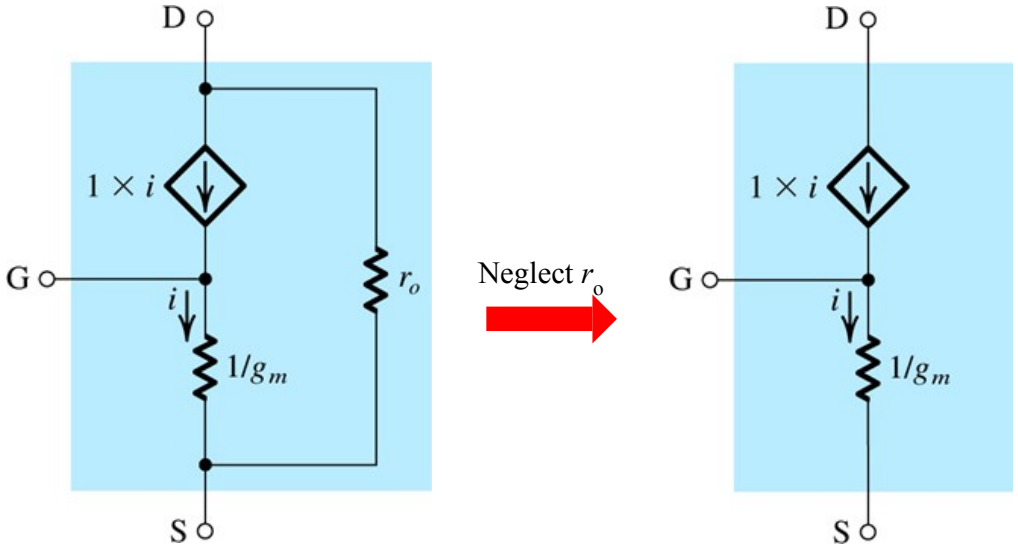


The small-signal equivalent circuit models

- Hybrid-π model



- T-model



Small-Signal Parameters

NMOS transistors

- Transconductance:

$$g_m = \mu_n C_{ox} \frac{W}{L} V_{OV} = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = \frac{2I_D}{V_{OV}}$$

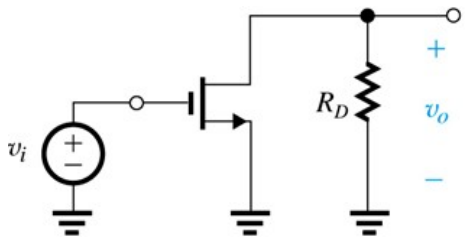
- Output resistance:

$$r_o = V_A / I_D = 1/\lambda I_D$$

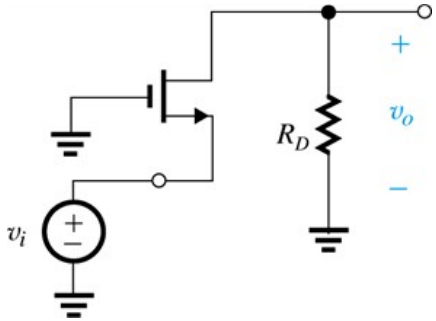
Basic MOSFET Amplifier Configuration

Three basic configurations

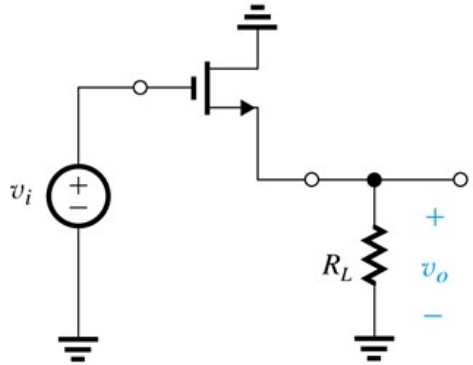
Common-Source (CS)



Common-Gete (CG)

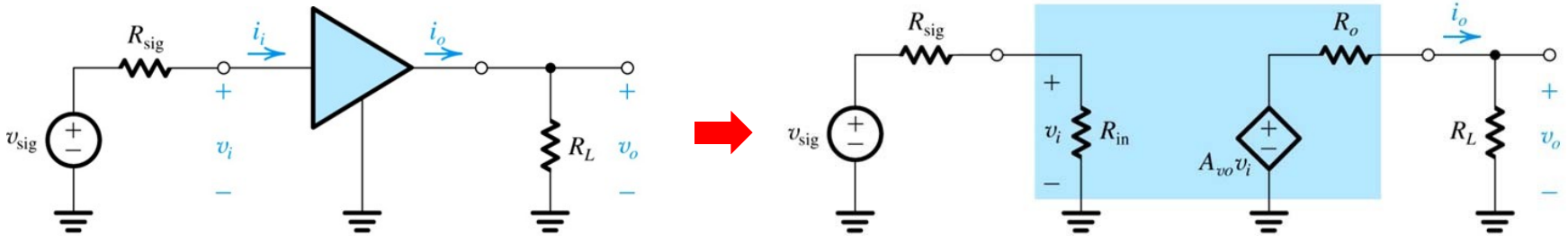


Common-Drain (CD)



Characterizing amplifiers

- The MOSFET circuits can be characterized by a voltage amplifier model (unilateral model)
- The electrical properties of the amplifier is represented by R_{in}, R_o and A_{vo}
- The analysis is based on the small-signal or linear equivalent circuit (dc components not included)
- Voltage gain: $A_v \equiv \frac{v_o}{v_i} = \frac{R_L}{R_L + R_o} A_{vo}$
- Overall voltage gain: $G_v \equiv \frac{v_o}{v_{sig}} = \frac{R_{in}}{R_{in} + R_{sig}} A_v = \frac{R_{in}}{R_{in} + R_{so}} \frac{R_L}{R_L + R_o} A_{vo}$



Biasing in MOS Amplifier Circuits

DC bias for MOSFET amplifier

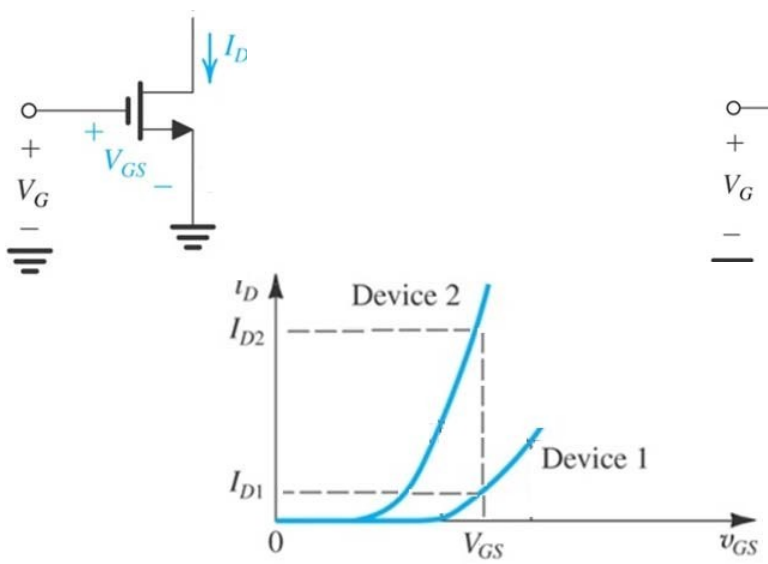
- The amplifiers are operating at a proper dc bias point
- Linear signal amplification is provided based on small-signal circuit operation
- The DC bias circuit is to ensure the MOSFET in **saturation** with a proper collector current I_D

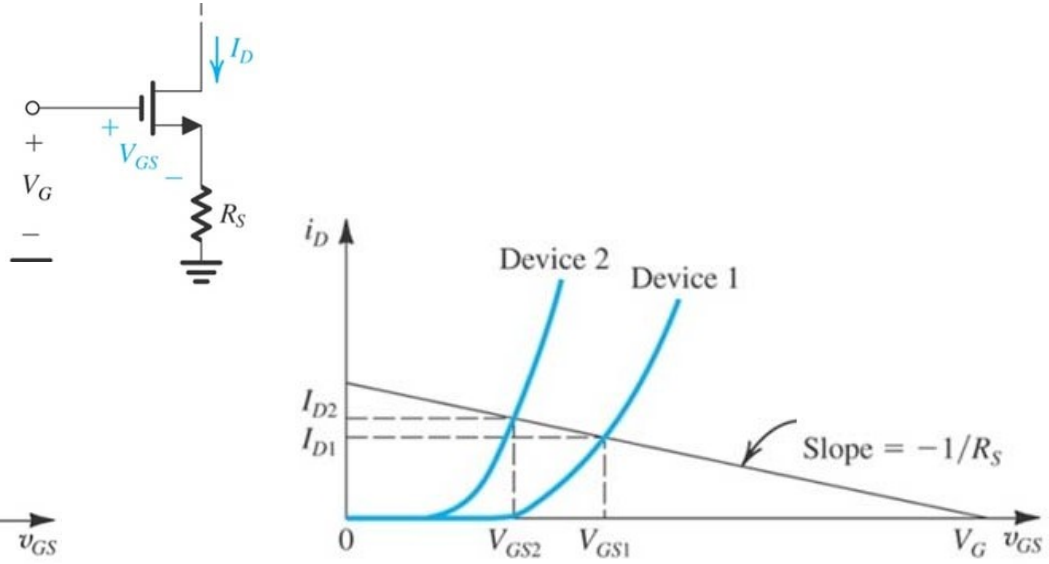
Biasing by fixing gate-to-source voltage

- Fix the dc voltage V_{GS} to specify the saturation current of the MOSFET: $I_D = \frac{1}{2}k_n(V_{GS}-V_t)^2 \equiv \frac{1}{2}k_n(V_{OV})^2$
- Bias current deviates from the desirable value due to variations in the device parameters V_t and μ_n

Biasing by fixing gate voltage and connecting a source resistance

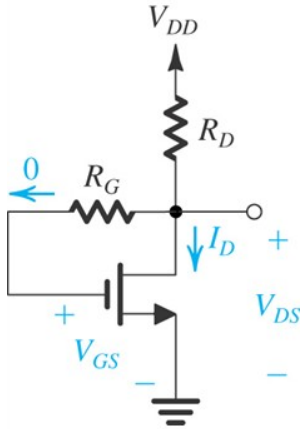
- The bias condition is specified by: $V_{GS} = V_G - I_D R_S$ and $I_D = \frac{1}{2}k_n(V_{GS}-V_t)^2$
- Drain current has better tolerance to variations in the device parameters





Biasing using a drain-to-gate feedback resistor

- A single power supply is needed
- R_G ensures the MOSFET in saturation ($V_{GS} = V_{DS}$)
- MOSFET operating point: $\frac{V_{DD} - V}{1 \; R_D} = - \; _n k (V \; _{GS} - V \; _t)^2$
- The value of the feedback resistor R_G affects the small-signal gain



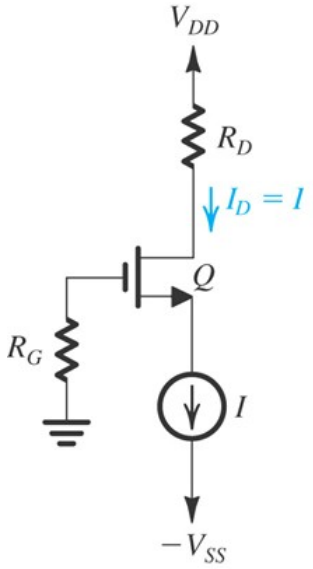
Biasing using a constant-current source

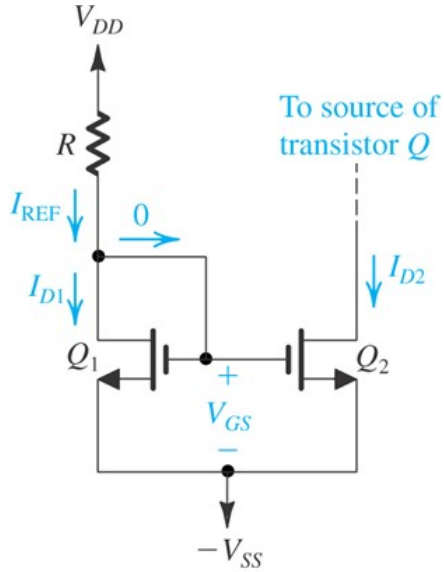
- The MOSFET can be biased with a constant current source I
- The resistor R_D is chosen to operate the MOSFET in active mode
- The current source is typically a current mirror
- Current mirror circuit:
  - MOSFETs Q_1 and Q_2 are in saturation
  - The reference current $I_{REF} = I = I_D$

$$\frac{V_{DD} - V}{1 \; R} = - \; _n k (V \; _{GS} - V \; _t)^2$$

$$I^{REF} = \frac{1}{2} k (V^{GS} - V)^2$$

  - When applying to the amplifier circuit, the voltage V_{D2} has to be high enough to ensure Q_2 in saturation





NEW

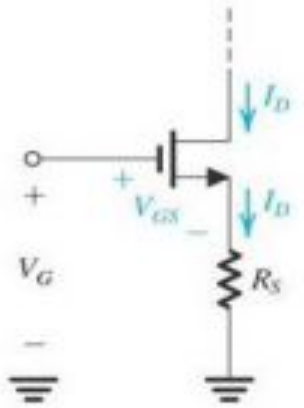
BJT vs MOSFET

- RTL logic vs CMOS logic
- DC Input impedance of MOSFET (at gate end) is infinite
  Thus, current output can drive many inputs **FANOUT**
- CMOS **static dissipation is low!!** ~ $I_{OFF}V_{DD}$
- Normally BJTs have higher transconductance/current (faster!)

$I_C = (qn_i^2D_n/W_BN_D)\exp(qV_{BE}/kT)$	$I_D = \mu C_{ox}W(V_G-V_T)^2/L$
$g_m = \partial I_C/\partial V_{BE} = I_C/(kT/q)$	$g_m = \partial I_D/\partial V_G = I_D/[(V_G-V_T)/2]$

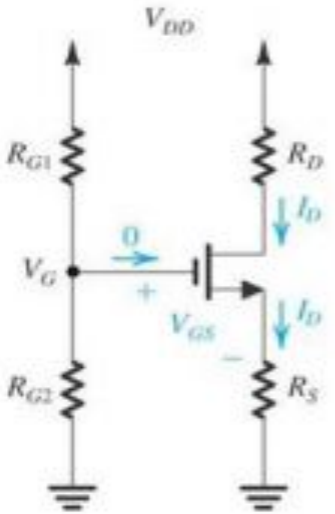
- Today's MOSFET I_D >> I_C due to near ballistic operation

MOSFET Biasing



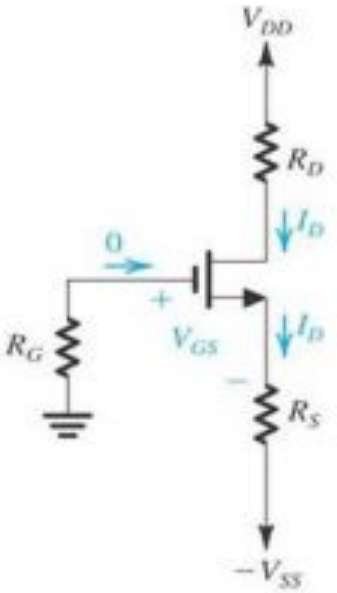
Basic Arrangement

$$V_{GS} = V_G - R_S I_D$$



Bias with <u>one</u> power supply

$$V_{GS} = V_G - R_S I_D$$



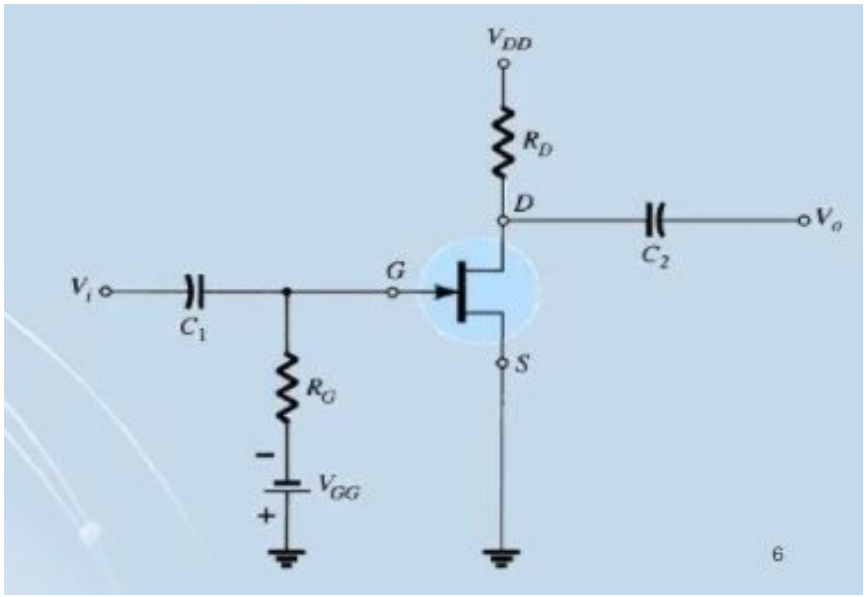
Bias with <u>two</u> power supplies

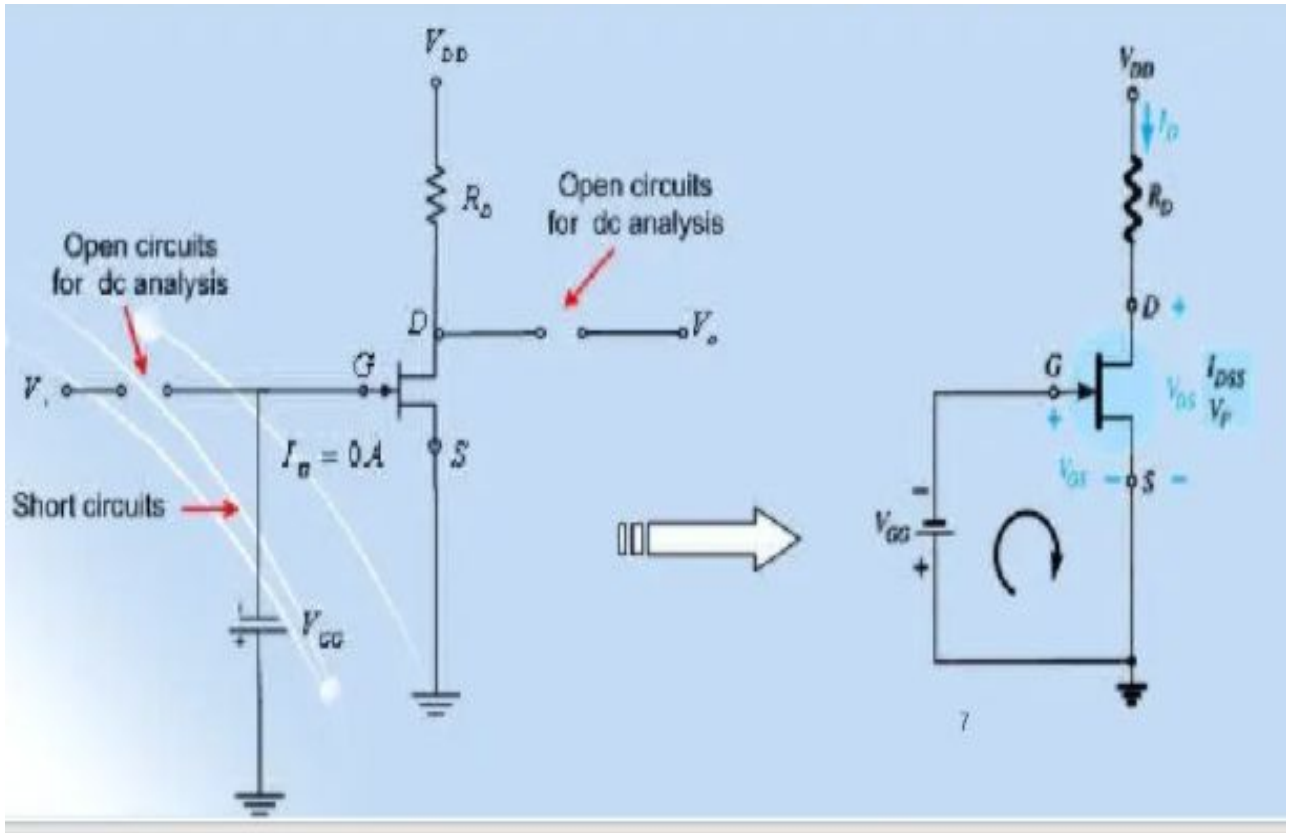
$$V_{SS} = V_{GS} - R_S I_D$$

(KVL: $0 + V_{GS} + R_S I_D - V_{SS} = 0$)

- Resistor Rs provides negative feedback

Fixed Bias


V_{DD}
R_D
D
V_o
C_2
V_i
G
C_1
R_G
S
V_{GG}
6


V_{DD}
R_D
Open circuits for dc analysis
Open circuits for dc analysis
D
V_o
V_i
G
$I_G = 0A$
S
Short circuits
V_{GG}
V_{DD}
I_D
R_D
D
G
I_{DSS}
V_P
V_{GS}
S
V_{GG}
7

Investigating the input loop

- I_G=0A, therefore

  $V_{RG}=I_G R_G=0V$

- Applying KVL for the input loop,

  $-V_{GG}-V_{GS}=0$

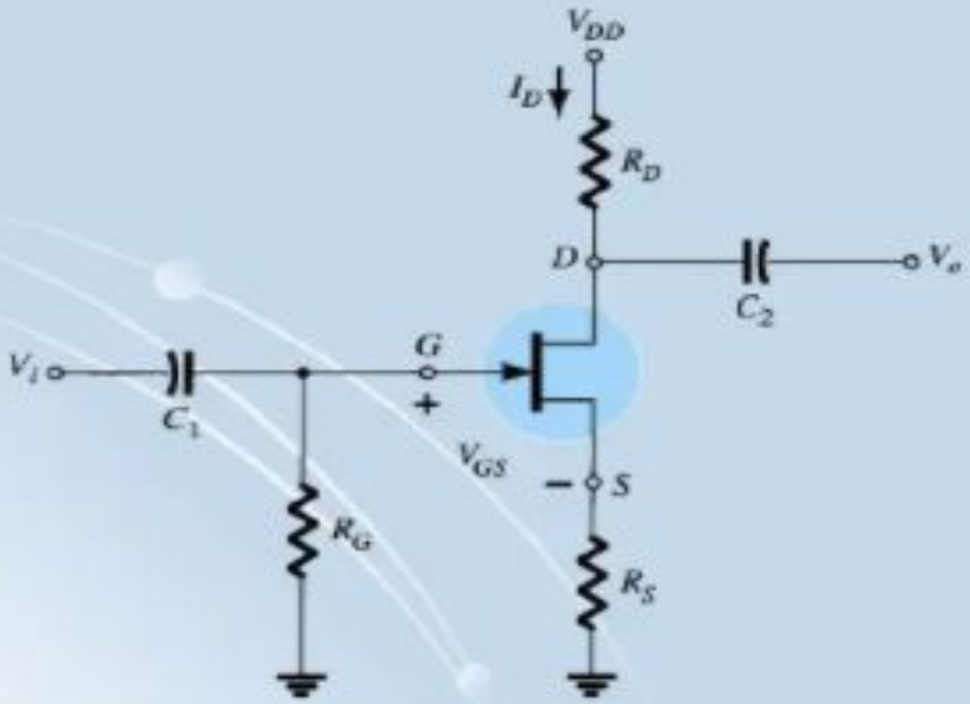
  $V_{GG}= -V_{GS}$

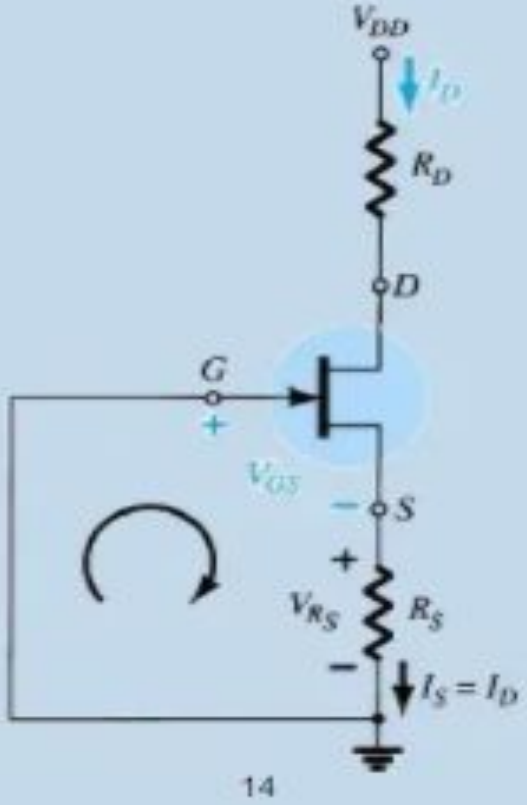
- It is called *fixed-bias configuration* due to V_{GG} is a fixed power supply so V_{GS} is fixed

- The resulting current, $I_D = I_{DSS}(1-\frac{V_{GS}}{V_P})^2$

Self Bias

- The self-bias configuration eliminates the need for two dc supplies.
- The controlling V_{GS} is now determined by the voltage across the resistor R_S





- For the indicated input loop:

$$V_{GS} = -I_D R_S$$

- Mathematical approach:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = I_{DSS}\left(1 - \frac{I_D R_S}{V_P}\right)^2$$

  - rearrange and solve.

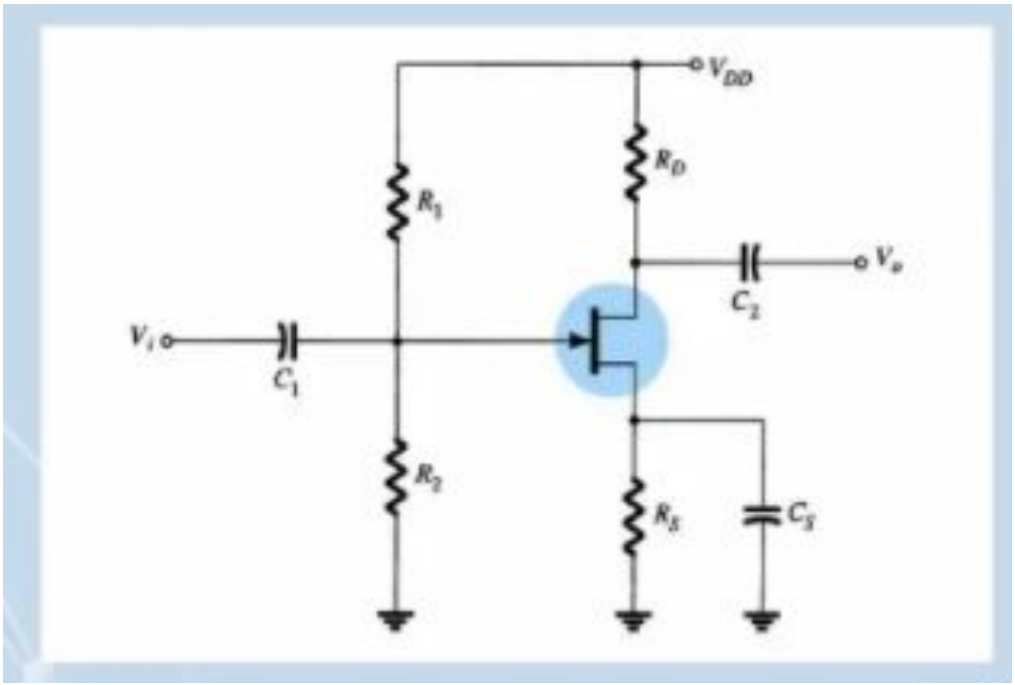
- For output loop
  - Apply KVL of output loop
  - Use $I_D = I_S$

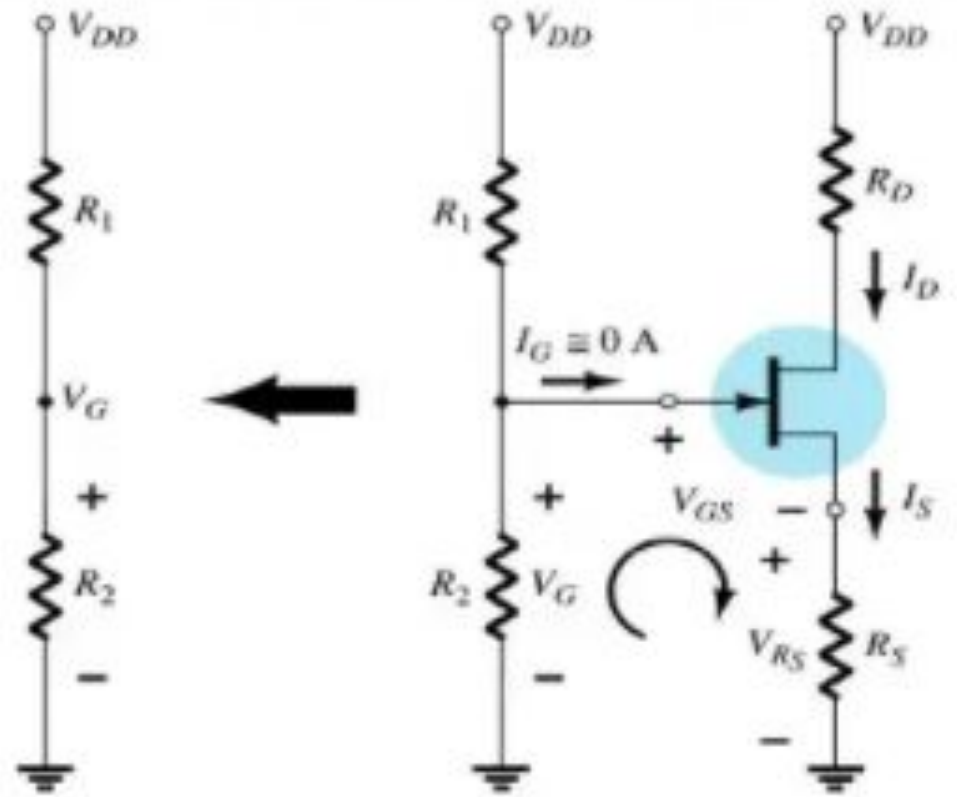
$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$

$$V_S = I_D R_S$$

$$V_D = V_{DS} + V_S = V_{DD} - V_{RD}$$

Voltage Divider Bias





- V_G can be found using the voltage divider rule

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

- Using Kirchoff's Law on the input loop:

- Rearranging and using ID =IS:

$$V_G - V_{GS} - V_{RS} = 0$$

$$V_{GS} = V_G - I_D R_S$$

- Once the quiescent values of I_{DQ} and V_{GSQ} are determined, the remaining network analysis can be found.

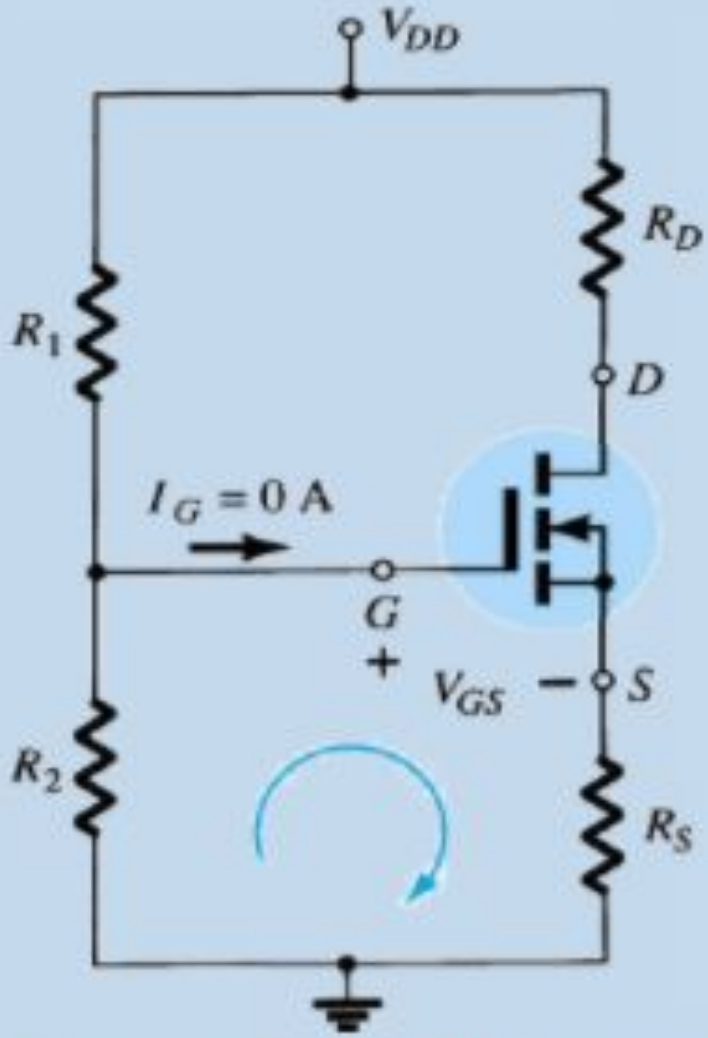
$$I_{R1} = I_{R2} = \frac{V_{DD}}{R_1 + R_2}$$

- Output loop:

$$V_{DS} = V_{DD} - I_D(R_D + I_D R_S)$$

$$V_D = V_{DD} - I_D R_D$$

$$V_S = I_D R_S$$



Again plot the line and the transfer curve to find the Q-point.
Using the following equations:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

Input loop : $V_{GS} = V_G - I_D R_S$

Output loop: $V_{DS} = V_{DD} - I_D (R_S + R_D)$