MCQ Questions PART-A

1. The inputs in the PLD is given through

   a) NAND gates b) OR gates c) NOR gates d) AND gates

2. PAL refers to

   a) Programmable Array Loaded b) Programmable Logic Array

   c) Programmable Array Logic d) None of the Mentioned

3. Outputs of the AND gate in PLD is known as

   a) Input lines b) Output lines c) Strobe lines d) None of the Mentioned

4. PLA contains

   a) AND and OR arrays b) NAND and OR arrays c) NOT and AND arrays

   d) NOR and OR arrays

5. PLA is used to implement

   a) A complex sequential circuit b) A simple sequential circuit

   c) A complex combinational circuit d) A simple combinational circuit

6. A PLA is similar to a ROM in concept except that

   a) It hasn't capability to read only b) It hasn't capability to read or write operation

   c) It doesn't provide full decoding to the variables d) It hasn't capability to write only

7. For programmable logic functions, which type of PLD should be used?

   a) PLA b) CPLD c) PAL d) SLD

8. The complex programmable logic device contains several PLD blocks and _____

   a) A language compiler b) AND/OR arrays c) Global interconnection matrix

   d) Field-programmable switches

9. Which type of device FPGA are?

   a) SLD b) SROM c) EPROM d) PLD

10. The difference between a PAL & a PLA is

    a) PALs and PLAs are the same thing

    b) The PAL has a programmable OR plane and a programmable AND plane, while the PLA only has a programmable AND plane

    c) The PLA has a programmable OR plane and a programmable AND plane, while the PAL only has a programmable AND plane

    d) The PAL has more possible product terms than the PLA

11. If a PAL has been programmed once

a) Its logic capacity is lost b) Its outputs are only active HIGH

c) Its outputs are only active LOW d) It cannot be reprogrammed

12. The FPGA refers to

a) First programmable Gate Array b) Field Programmable Gate Array

c) First Program Gate Array d) Field Program Gate Array

13. In FPGA, vertical and horizontal directions are separated by

a) A line b) A channel c) A strobe d) A flip-flop

14. Logic circuits can also be designed using

a) RAM b) ROM c) PLD d) PLA

15. In PLD, there are provisions to perform interconnections of the gates internally, because of

a) High reliability b) High conductivity c) The desired logic implementation d) The desired output

16. Why antifuses are implemented in a PLD?

a) To protect from high voltage b) To increase the memory

c) To implement the programmes d) As a switching devices

17. _____ is the fundamental architecture block or element of a target PLD.

a. System Partitioning b. Pre-layout Simulation

c. Logic cell d. Post-layout Simulation

18. Moore Machine is an application of

a. Finite automata without input b. Finite automata with output

c. Non Finite automata with output

19. In Moore machine, output is produced over the change of:

a) transitions b) states c) Both d) None of the mentioned

20. For a give Moore Machine, Given Input='101010', thus the output would be of length:

a) |Input|+1 b) |Input| c) |Input-1| d) Cannot be predicted

21) PLA is used to implement

a) A complex sequential circuit b) A simple sequential circuit

c) A complex combinational circuit d) A simple combinational circuit

22) For programmable logic functions, which type of PLD should be used?

a) PLA b) CPLD c) PAL d) SLD

23) Which type of device FPGA are?

a) SLD b) SROM c) EPROM d) PLD

24) If a PAL has been programmed once

a) Its logic capacity is lost b) Its outputs are only active HIGH

c) Its outputs are only active LOW d) It cannot be reprogrammed

25) Applications of PLAs are

a) Registered PALs b) Configurable PALs

c) PAL programming d) All of the Mentioned

26) Which of the following best describes the fusible-link PROM?

a) Manufacturer-programmable, reprogrammable

b) Manufacturer-programmable, one-time programmable

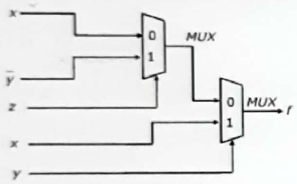
c) User-programmable, reprogrammable

d) User-programmable, one-time programmable

27) In finite state machine the data in and data out are

a) In same ports b) different ports c) same register d) different register

28)



Consider the circuit above.which is represent f(x,y,z)?

a)$x\bar{z} + xy + z\bar{y}$ b) $x\bar{z} + xy + \overline{zy}$ c) zx+$xy + \overline{yz}$ c) zx+$x\,\bar{y} + z\,\bar{y}$

29) Convert gray code into binary code: 110111

a) 101101 b)001110 c)111001 d)100101

30) How many flip flops are necessary to design a state machine with 25 states?

a) 2 b) 5 c) 25 d) 2^{25}

31)A finite state machine has an output determined only by the present state of the system is ____.

a) Moore machine b) Mealy machine c) Max machine d) Min machine

32) How many gates would be required to implement the following Boolean expression after the simplification? XY + X(X + Z) + Y(X + Z)

a) 1 b)2 c)4 d)5

33) Two states are said to be equal if they have exactly same

a) Inputs b) next state c) output d) both a and b

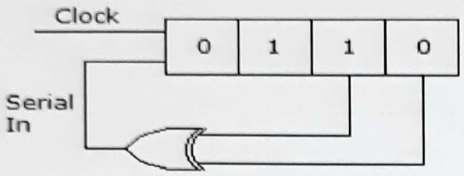
34) Which mechanism allocates the binary value to the states in order to reduce the cost of the combinational circuits?

a) State Reduction b) State Minimization c) State Assignment d) State Evaluation

35)The number of address lines in EPROM 4096 x 8 is

a) 2 b) 4 c) 8 d)12

36) In the given figure shows a 4 bit serial in parallel out right shift register. The initial contents as shown are 0110. After 3 clock pulses the contents will be



a) 17) b)0101 c)1010 d)1111

37) State table can be represented in a

a) state diagram b) map c) truth table d) graph

38) Which is the major functioning responsibility of the multiplexing combinational circuit?

a) Decoding the binary information

b) Generation of all min-terms in an output function with OR-gate

c) Generation of selected path between multiple sources and a single destination

d) All of the Mentioned

39) What is the function of an enable input on a multiplexer chip?

a) To apply VCC b) To connect ground c) To active the entire chip d) To active one half of the chip

40) One multiplexer can take the place of

a) Several SSI logic gates b) Combinational logic circuits

c) Several Ex-NOR gates d) Several SSI logic gates or combinational logic circuits

41. A PLA is similar to a ROM in concept except that

a) It hasn't capability to read only

b) It hasn't capability to read or write operation

c) It doesn't provide full decoding to the variables

d) It hasn't capability to write only

42. The complex programmable logic device contains several PLD blocks and _____

a) A language compiler b) AND/OR arrays

c) Global interconnection matrix d) Field-programmable switches

43.What is a fusing process?

a) It is a process by which data is passed to the memory

b) It is a process by which data is read through the memory

c) It is a process by which programs are burnout to the diode/transistors

d) None of the Mentioned

44.The number of address lines in EPROM 1024 x 16 is

a) 10 b) 12 c)16 d) 8

45.Applying DeMorgan's theorem to the expression $\overline{\overline{\overline{(X+Y)}+\overline{Z}}}$, we get _____

a)(X+Y)z b)$(\overline{y}+\overline{x})Z$ c)$(X+Y)\overline{z}$ d))$(\overline{y}+\overline{x})\overline{z}$

46. State table can be represented in

a)state diagram b)map c)truth table d)graph

47. Which mechanism allocates the binary value to the states in order to reduce the cost of the Combinational circuits?

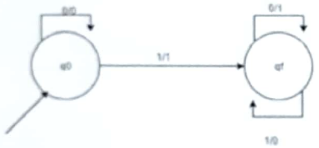
a) State Reduction b) State Minimization

c) State Assignment d) State Evaluation

48) MOD-9 counter has

a)5 states b)10 states c)9 states d)20 states

49)The following mealy machine outputs which of the following?



a)9's Complement b) 2's Complement

c) 1's Complement d) 10's Complement

50). What is the function of an enable input on a multiplexer chip?

a) To apply Vcc b) To connect ground c) To active the entire chip d) To active one half of the chip

51.Reduction of flip-flops in a sequential circuits are referred as

a)reduction b) state reduction c)next state d)both a and b

52. Memory elements in clocked sequential circuits are called

a)latches b)flip-flop c)signals d)gates

53.In Moore models, output are function of only

a)present state b)input state c)next state d)both a and b

54. Unused states are treated as Don't cares conditions during

a)Execution b)Pulse trigger c) Design of a circuit d)None

55) Table that lists inputs for required change of states is called

a)truth table b)excitation table c)state table d)clock table

56) In last step of design procedure we

a)draw map b)draw circuit c)draw table d)draw a logic diagram

57) ROM is a device that includes both decoder and?

a)encoder b)Multiplexer c)OR Gates d)None

58) Reed–Muller expansion produces expression in the form of

a) SOP b) POS c) ESOP d) NSOP

59).Which of the following expression remove hazard from : xy + zx ' ?

a) $z\bar{x} + xy$ b) xy+wyz+ $z\bar{x}$ c) xy+yz+ $z\bar{x}$ d) xy+wz+ $z\bar{x}$

60) Two states are said to be equal if they have exactly same

a) Inputs b) output c) next state d)both a and c

61) Out of multiplexer and demultiplexer, which can be used as a logic function generator?

- A.Multiplexer only B.Demultiplexer only C.Both D.None

62) _____ is the fundamental architecture block or element of a target PLD.

a.System Partitioning b. Pre-layout Simulation c. Logic cell d. Post-layout Simulation

63) An Antifuse programming technology is predominantly associated with _____.

a. SPLDs b. FPGAs c. CPLDs d. All of the above

64) Which one is not the type of hazard

a. Static- 0 hazard Static -1 hazard Dynamic hazard None

65) In a logic circuit delay is an hazard is independent form

a. Delay excisting b. Clock pulse c. Latches d. Feedback

66) Which statement is suitable to explain glitch

a. A glitch is produce in a logic circuit when a circuit output may produce a short pulse

b. A glitch is produce in a logic circuit when a circuit output never produce a short pulse

c. A glitch is produce in a logic circuit when a circuit output may produce a high pulse

d. A glitch is produce in a logic circuit when a circuit output never produce a high pulse

67) Any condition that a processor can stay is called as

a) Page fault b) Hazard c) System error d) None

68) When steady-state analysis predicts that the output should not change the short pulse generated by a circuit is called

a) Behavior pulse Output pulse c. Dlitch d) Glitch

69) An hazard is excist in a circuit

a) When a circuit has the possibility of producing a glitch

b) When a circuit has the possible tolerance to filter a glitch

c) When a circuit has maximum probability to stop unwanted glitch

d) When a circuit is on its minimum limit to remove glitch

70) The dynamic hazard problem occurs in

a) Combinational circuit alone b) Sequential circuit only c) Both a and b d) None

71) Which one is suitable to detecting the hazard in circuit

a) Karnaugh map b) Boolean expression c) Logic gates d) None

72) Data hazard occur when

a) Greater performance loss

b) Pipeline changes the order of read/ write access to operands

c) Some functional unit is fully pipelined

d) Machine size is limited

73) Which circuit hazards must be eliminated

a) Combination circuit b) Sequential circuit c) Multiprocessor d) Decoder

74) Which of the following are problems that can arise pipelining

a) Data hazards b) Water hazards c) Dukes hazards d)None

75) Static hazards can be detected by using k-map in

a. Two level sum of product b. Two level of product of sum c.Both 1 & 2 d.Neither 1 nor 2

76) What happens when variables and it compliment were connected to the same And gate in two level of SOP

a. Static -0 hazards occur only b. Static -1 hazards occur only c. Dynamic hazards

d. must exists but (b) not compulsory

77) The term consensus also referred as

a. Resolvent b. Reproduction c. Reconstruction d.Revolution

78) What happens when variables and it compliment were connected to the same OR gate in two level of product of Sum

a. Static -0 hazards occur only b. static -1 hazards occur only c. Dynamic hazards d.Dynamic-0

79) In dynamic hazards multiple output transition can occur if

a. Circuit have single path with different delay b. Circuit have multiple path with different delay

c. Circuit have single path with single delay d. Circuit have multiple path with single delay

80) Hazard analysis and elimination are typically needed in

a. Combinational circuit b. Synchronous Sequential circuit c. Asynchronous sequential circuit

81) Which hazard is overcome by properly designed two level AND –OR or OR-AND circuit

a. Dynamic hazard b. Static-0 hazard c. Static-1 hazard d. None

82) To eliminate the hazards from the logic circuits, which is used from the following

a. Adding Consensus b. Removing consensus c. Adding momentary values d. Adding glitch

83) This set of Automata Theory Multiple Choice Questions & Answers (MCQs) focuses on "Moore Machine".

1. Moore Machine is an application of:

a) Finite automata without input b) Finite automata with output

c) Non- Finite automata with output d) None of the mentioned

84) In Moore machine, output is produced over the change of:

a) transitions b) states c) Both d) None of the mentioned

85) For a give Moore Machine, Given Input='101010', thus the output would be of length:

a) |Input|+1 b) |Input| c) |Input-1| d) Cannot be predicted

86) The total number of states and transitions required to form a moore machine that will produce residue mod 3.

a) 3 and 6 b) 3 and 5 c) 2 and 4 d) 2 and 5

87) In mealy machine, the O/P depends upon?

a) State b) Previous State c) State and Input d) Only Input

88) The ratio of number of input to the number of output in a mealy machine can be given as:

a) 1 b) n: n+1 c) n+1: n d) None of the mentioned

89) Mealy and Moore machine can be categorized as:

a) Inducers b) Transducers c) Turing Machines d) Linearly Bounder Automata

90) The major difference between Mealy and Moore machine is about:

a) Output Variations b) Input Variations c) Both d) None of the mentioned

91) In mealy machine, the O/P depends upon?

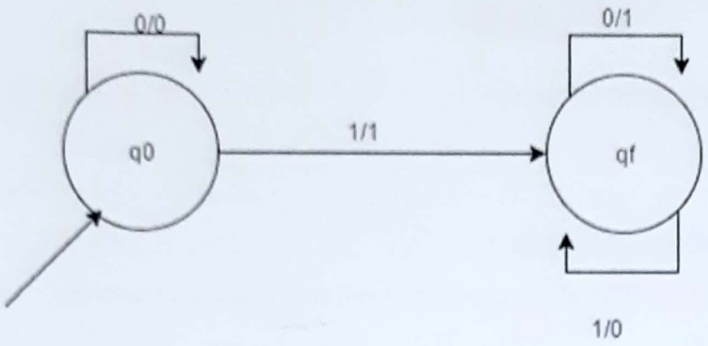
a) State b) Previous State c) State and Input d) Only Input

92) Which of the given are correct?

a) Moore machine has 6-tuples b) Mealy machine has 6-tuples

c) Both Mealy and Moore has 6-tuples d) None of the mentioned

93) The following mealy machine outputs which of the following?



a) 9's Complement b) 2's Complement c) 1's Complement d) 10's Complement

94) The O/P of Mealy machine can be represented in the following format:

a) Op(t)= δ(Op(t)) b) Op(t)= δ(Op(t)i(t)) c) Op(t): ∑ d) None of the mentioned

95) The ratio of number of input to the number of output in a mealy machine can be given as:

a) 1 b) n: n+1 c) n+1: n d) None of the mentioned

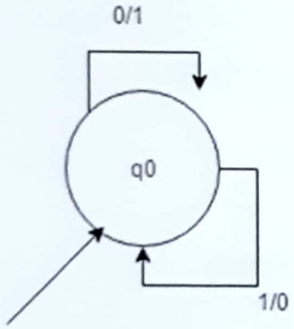
96) Mealy and Moore machine can be categorized as:

a) Inducers b) Transducers c) Turing Machines d) Linearly Bounder Automata

97) The major difference between Mealy and Moore machine is about:

a) Output Variations b) Input Variations c) Both d) None of the mentioned

98) Which of the following does the given Mealy machine represents?



a) 9's Complement b) 2's Complement c) 1's Complement d) 10's Complement

99) Which one among the following is true?

A mealy machine

a) produces a language b) produces a grammar c) can be converted to NFA

d) has less circuit delays

100) Moore Machine is an application of:

a) Finite automata without input b) Finite automata with output c) Non- Finite automata with output

PART-B

1. Find minimal SOP expressions for the following:
   a. Z=AD+BCD+A†C
   b. Z=AB(A†CD+AE+EG)
   c. Z=ABC+AB†CE+ACDE+A†B†D+B†CDE
2. With the state diagram as example, list the difference between Mealy and Moore circuit.
3. i. Write a short notes on PROM.
   ii. Implement the Boolean function using PAL F = ∑(2,12,13).
4. List the types of operator available in VHDL and explain any two.
5. Explain the package in VHDL.
6. Write a VHDL code for D-flip flop.
7. Design a single bit comparator and write the VHDL code for the same.
8. Implement Full Adder only using 2:1 MUX in Shannon's expansion.
9. Explain Static-1 hazard using an example.
10. Write the differences between Moore and Mealy Machine.
11. Implement F (A, B, C) = ∑ (1, 3, 4, 7) using ROM.
12. Compare PAL, PLA and ROM.
13. Prove A'B'C'D'+A'BC'D'+A'BD+A'BC'D+ABCD+ACD'+B'CD'= A'C'D'+A'BD+B'CD'+ABC using Consensus Theorem
14. Implement 2 input NAND Gate using 2:1 and 4:1 MUX.
15. What is the difference between Signal and Variable? Give an example.
16. Explain the various wait statements in VHDL.
17. What is the use of Procedure? How it will be called in the main program?
18. Write a VHDL code for Half Subtractor using dataflow model.
19. Using behavioral model, write a VHDL program for D flip-flop.
20. What is the use of Concurrent Select statement? Explain with an example.
21. How Generate statement is used? Give example.
22. With an example, Explain the Enumerated data type.
23. Write a program for 1X4 De-multiplexer using structural model.
24. Implement 4:2 Encoder using behavioral model.

PART-C

1. a) i) Implement F(A,B,C,D) = $\sum$ (5, 7, 10, 15) using Reed-Muller Expansion. (6)

   ii) Find the hazard free circuit for the function F (A, B, C) = $\sum$ (1, 3, 6, 7). (6)

   b) Design mod-5 Synchronous Counter using JK Flip-Flops. (12)

2. a) Draw a Logic Diagram, State Table and State Diagram using Moore Model for the sequential circuit which consists of two JK Flip-Flops, an input x and an output y. The input to the flip-flops and output are as

   J_A=B, J_B=x', K_A=Bx', K_B=A $\oplus$ x and output y=AB (12)

   b) With neat diagram elaborate the details of Xilinx XC-4000 CLB. (12)

3. a) Draw a state diagram to detect the sequence "1101" without overlapping using Mealy Model and also design it using D Flip-Flops. (12)

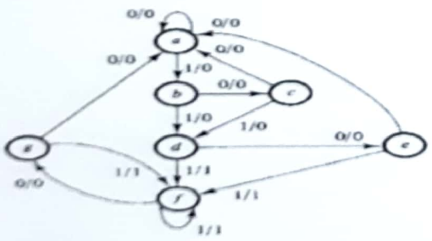
   b) Implement the following functions using PLA (12)

   F_1(A,B,C) = $\sum$ (3,5,6,7) F_2(A,B,C) = $\sum$ (0,2,4,7)

4. a) Realize the following using PAL (12)

   1. W(A,B,C,D) = $\sum$ (2,12,13)
   2. X(A,B,C,D) = $\sum$ (7,8,9,10,11,12,13,14,15)
   3. Y(A,B,C,D) = $\sum$ (0,2,3,4,5,6,7,8,10,11,15)
   4. Z(A,B,C,D) = $\sum$ (1,2,8,12,13)

5 b) (12)



Draw the reduced State Diagram using State Reduction Technique.

6. a) i) Implement the expression F=(A·B) + (B'·C) + D using Shannon's Expansion Theorem.

   ii) Draw the state diagram for Moore Machine to detect the sequence "11011" with overlapping.

7 b) Reduce the number of Gates required for the circuit which has the following Multiple Output functions F1(w,x,y,z)= $\sum$(3,6,7,11,12,13,14,15)

$F2(w,x,y,z)= \sum(4,6,7,12,14,15)$ $F3(w,x,y,z)= \sum(3,4,11,12,13)$

8. Explain Reed Muller expansion theorem with an example.

9. By applying the Shannon's expansion theorem implement the following function using one 2xl multiplexer and logic gates. F – X'Y'Z'+ X'Y'Z'+ X'YZ + XY'Z'+ XY'z

10. Simplify the following Boolean equation and eliminate the consensus terms.

F_1= A'C'+ ABD + BC'D + AB'D'+ ABCD'

F_2=A'B+ABD+AB'CD'+BC

11. a With the design example, explain how multiplexer is working as logic function generator.

b. A sequential circuit has one input (X) and one output (Z). The circuit produces an output Z=1 ior the input sequence 101. Find the Mealy state graph and design the circuit using D flip flop. X = 001 101 1001010100; Z =00AA010000010100

12. Design a synchronous 3-bit gray code up-counter using JK flip flops.

13. With a neat sketch explain the Xilinx 4000 architecture.

14 . i. What is an entity in VHDL?

ii. What is the significance of architecture declaration in VHDL?

iii. Define process statement and list its types and explain any two.

15 b. i. Explain the different types of data objects present in VHDL.

ii. Distinguish between concurrent and sequential signal assignment with e6ample.

16. a. Develop a VHDL program for BCD adder using full adders and logic gates as a component.

17 b .i. Write a VHDL program for 3x8 decoder with enable input in dataflow modeling.

ii. Write a VHDL program for 4-bit up/down counter in behavioral modeling.

18. Write a program to design 1X16 De-multiplexer using 1X4 De-multiplexer.

19. Implement 4-bit Up counter using behavioral model.

20. What are the different Data Types in VHDL? Explain with examples.

21. What are the different types of Data Objects in VHDL? Explain with examples.

22. Design and implement 8X1 Multiplexer using 4X1 and 2X1 Multiplexer.

23. i) Using case statement, write a program for JK Flipflop.

ii) How Function is declared in package and how it is called in main program?

24. Convert 4-bit i) Binary to Gray code ii) Gray to Binary code.