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	Objective &:- Using a single THOO IC, connect a circuit produces:	16/10/23	1-6	B 186
<b>3</b> d	LAB-II: Objective 1:- Construct a circuit using hasic sates: F = AB + AB C	06/11/23	7-13	O the
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## **DIGITAL LOGIC DESIGN LAB (EET1211)**

#### LAB I: Examine the Operation of Logic Gates

#### Siksha 'O' Anusandhan Deemed to be University, Bhubaneswar

Branch:	Section:	Sub Group Number:	
Name	Registration No.	Signature	
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Marks: \_\_\_\_\_/10

Remarks:

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Teacher's Signature

II. PRE-LAB

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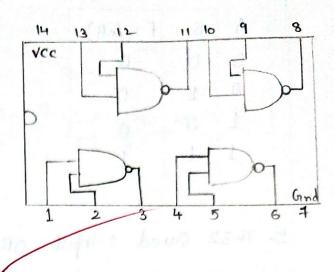
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1.7400 Quad 2-input NAND gate:

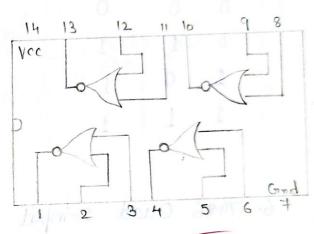
A	B	F=(A.B)'
0	0	1
0	1	1
1	0	1
1	1	0



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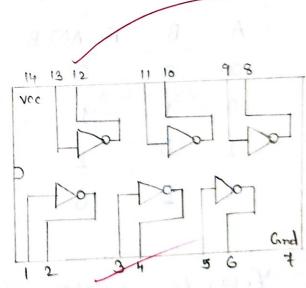
2. 7402 Quad 2-input NOR gates:

Α	В	F = (A+B)'
0	0	1
0	1	0
1	0	0
1	1	0



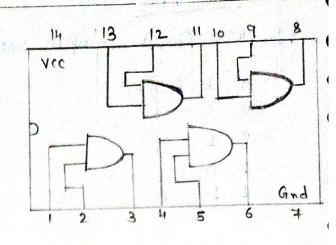
3. 7404 hex inverter:

Α	F= A'
0	1
1	0



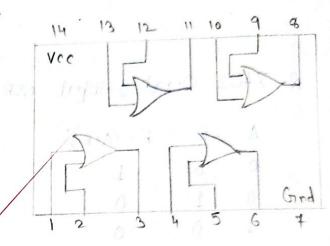
4. 7408 Quad 2-input AND gates:

A	В	F = (A.B)
0	0	0
0	1	0
1	0	0
1	1	1



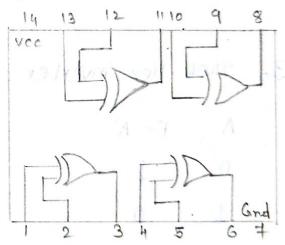
5. 7432 Quad 2-input OR gates:

Α	В	F = A+B
0	0	0
0	1	1
1	0	1
1	1	1



6. 7486 Quad 2-input XÓR gates:

Α	В	F= A T B
0	0	0
0	1	1
1	0	1
1	1	0

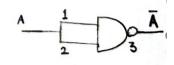


4. (a) An inverter:

A	A
0	1
1	0

NOT:





(b)	A	2-input	AND	:
		2		

JA	В	A·B	
0	0	0	permit (All Shrift has suffi
0	7,	0	
1	0	0	
1	7	1	

#### AND:

$$\begin{array}{c|c}
A & 1 \\
B & 2
\end{array}$$

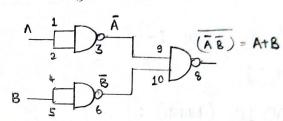
$$\begin{array}{c|c}
\overline{AB} & 5 \\
\hline
6
\end{array}$$

$$\begin{array}{c|c}
\overline{(AB)} = AB$$

### (C) A 2-input OR:

Andrew Constitution of the Parket	A	В	A+B
-	0	0	0
-	0	1	1
-	1	0	1
	1	1	1

$$\frac{\Lambda}{B}$$
  $\frac{\Lambda + B}{A}$ 

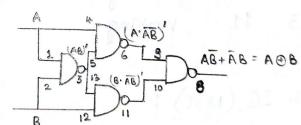


## (d) A 2-input XOR:

	A	В	AOB
7	D	0	0
7	0	10	1
4	1	0	1
	1	1	0

XOR:





#### III: LAB:

### Components Required:

#### Objective à

SI. No.	Components Name (Description)	Quantity
1	7400 IC (NAND)	1
a	Wires	As required

Objective 1

51. No.	Components (Description)	Quantity
	Wires	As required
l d	7400 IC (NAND)	1
3	7432 IC (OR)	1 1
4	7486 IC (XOR)	1 Halana A
5	7408 IC (AND)	1
6	7404 IC (NOW)	14
7	7402 IC (NOR)	1000

### Observation Table:-

### Objective 1

(a) 7400 IC (NAND):

-		
I/P	0/P	Status
1,2	3	Working
4,5	6	Working
9,10	8	Working
12,13	11	Working

# (b) 7402 IC (NOR):

Ī		0.10	61.1
N. Park	I/P	0/P	status
	2,3	1 3	Working-
	5,6	4	Working
	8,9	10	Working
	11,12	13	Working

(c) 7404 IC (NOT):

1	)				
1	I/P	O/P	status		
-	1	2	norking		
-	3	4	working		
	5	6	Working		
	9	8	Working		
	11	10	Working		
	1.13	12	Working		
		The state of the s	11		

# (d) 74808 IC (AND):

7\P	O/P	Status
2,1	3	Working
5,84	<b>4</b> 6	working
10,9	8	Working
136, 12	11	Working

# (e) 7432 IC (OR):

1		-	
1	I/P	0/P	Status
	1,2	3	Working
	4,5	6	Working
	9,10	8	Working
	12,13	11	Working
-			0

### (F) 7486 IC (XOR):

+	I/P	O/P	Status
100	1,2	3 /	Working
	415	6	Working
	9,10	8	Working
	12, 13	11	Working

# Objective 2

### (a) An inverter (NOT):

A	Y	Status
0	1 1	Working
1	0	Norking

### (b) A 2-input AND:

A	B	У	Status
0	0	0	Working
0	1	0	Working
1	0	0	Working
1	1	1	Working

# (C) A 2-input OR:

Α	В	Y	Status
0	0	O	Norking
0	1	1	Working
1	0	1	Working
1	1	1	Working

# (d) A 2-input XOR:

A	В	У	Status
0	0	0	Working
0	1	1	Working
§ 7	0	1	Working
1	1	0	Working

# Conclusion :-

# Objective 1

we have concluded that all pins of given ICs are working perfectly.

#### Objective 2

We have concluded that NAND is a universal gate because we are able to produce an inverter, AND, OR and an XOR gate using one 7400 IC.

# IV: POST LAB:

1. What is the voltage range for operation of digital circuits?

The voltage range for operation of digital circuits

- 2. What is the significance of ground and V<sub>cc</sub> connection?

  → V<sub>cc</sub> is the power input for a device, it provides

  the voltage to the circuit generally higher than the
- 3. Which gates are known as the universal gates 8 why!
- We can construct any gates using this.
- 4. What is the min" no. of NAND gates used to realize,
- > 4 NAND gates are required to realize an XDR

Well W