DIGITAL LOGIC DESIGN LAB (EET1211)

LAB II: Examine and analyze the gate level minimization for Boolean function

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Branch:	**Section:**	**Subgroup No.:**
Name	**Registration No.**	**Signature**

Marks: _____/10

Remarks:

Teacher's Signature

I. Objective:

1. Construct a circuit for the Boolean function given below using basic gates and verify the truth table.

   a) $F(A,B,C) = AB + AB'C$
   b) $F(X,Y,Z) = XY + X'Z + Y'Z$

2. Simplify the following Boolean functions to minimum number of literals and design the circuit using minimum number of basic gates.

   a) $F(X,Y,Z) = X'Y'Z' + X'YZ' + XY'Z' + XYZ'$
   b) $F(X,Y,Z) = XYZ' + X'Y + X'Z + YZ$

II. Pre-lab:

For each objective in prelab describe the following points:

a) Draw the circuit diagram.
b) Obtain the truth table.

III. LAB:

Components Required:

Sl. No.	Name of the Components	Specification	Quantity

Observation:

IV. Conclusion:

V. POST LAB:

1. Prove the following equation using truth table:
   $$(x + y)(x' + z) = xz + x'y$$
2. Draw a circuit that uses only one AND gate and one OR gate to realize the Boolean function
   $$F = WXYZ + VXYZ + UXYZ$$