DIGITAL LOGIC DESIGN LAB (EET1211)

LAB III: Design, Construct & examine the Combinational Circuit to Solve a Given Problem

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Branch:	**Section:**	**Subgroup No.:**
Name	**Registration No.**	**Signature**

Marks: _____/10

Remarks:

Teacher's Signature

I. Objective:

1. Design a combinational circuit with four inputs, A, B, C and D, and one output F. The output F value is 1 when A=0 or (B=1 and C=1) or (B=1 and C=1 and D=1)

2. Design a combinational circuit with three inputs, x, y, and z, and three outputs, A, B, and C. When the binary input is 0, 1, 2, or 3, the binary output is two greater than the input. When the binary input is 4, 5, 6, and 7, the binary output is two less than the input.

3. Design, construct, and test a circuit that generates an even parity bit from three message bits.

4. Minimize the Boolean function Implement the Boolean function $F(A, B, C, D) = \prod M(2,3,4,5,6,7,10,11)$ using K-map and implement the function two-level NOR-gate circuit.

II. Pre-lab:

Obj. 1:

a) Obtain the truth table.
b) Derive the Boolean expression that only use the NAND gate to realize.
c) Draw the circuit using NAND-gate only.

Obj. 2:

a) Obtain the truth table.
b) Derive the Boolean expression using any minimization technique.
c) Draw the circuit using minimum number of basic gates.

Obj. 3:

a) Obtain the truth table.
b) Derive the Boolean expression using any minimization technique.
c) Draw the circuit using minimum number of gates.

Obj. 4:

a) Solve the Boolean expression using K-map.
b) Obtain the truth table.
c) Derive the Boolean expression that only use the NOR gate to realize.
d) Draw the circuit using NOR-gate only.

III. LAB:

Components Required:

Sl. No.	Name of the Components	Specification	Quantity

Observation:

IV. Conclusion:

V. POST LAB:

1. Design a combinational circuit with three inputs (x, y, and z) and two output (F_1 and F_2). The output F_1 is 1 when the binary value of the inputs is an even number. The output F_2 is 1 when the binary value of the inputs is an odd number.
2. Design a 2-bit comparator circuits with two inputs (A and B) and three outputs ($(A < B)$,$(A = B)$, and $(A > B)$).