

MCIMX6UL-BB

Schematics DevBoard

Table of Content

Page 1	Cover
Page 2	Block Diagram
Page 3	PWR TREE
Page 4	LCD
Page 5	HDMI
Page 6	USB
Page 7	CAN
Page 8	Sensor
Page 9	Codec
Page 10	Ethernet x1
Page 11	Ethernet x2
Page 12	SD/BT
Page 13	Camera
Page 14	DBG/JTAG
Page 15	SYS PWR
Page 16	SODIMM BB
Page 17	NOTE
Page 18	IOMUX
Page 19	
Page 20	
Page 21	
Page 22	
Page 23	
Page 24	
Page 25	
Page 26	
Page 27	
Page 28	

1. Unless Otherwise Specified:

All resistors are in ohms, 10%, 1/8 Watt, 0603

All capacitors are in uF, 20%, 50V, 0603

All voltages are DC

All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

Revision History

Rev. Code	Date	By	Description
A	2015-02-28	Javen	1 Revision A released
B	2015-07-07	Javen	1 DNP R1023 DNP R1436, R1404, Add R1436 DNP R1517, Install R1520 Change Camera J1801 connector Change JTAG J1902 footprint Change SODIMM J2101 footprint Change R2101 from PU to PD Change J1901 PIN sequence
C	2015-07-14	Javen	1 Add R919-R946, L903-L905 DNP R1436, Install R1404, R1435 Change HP_MIC1IN to LINPUT1 Add BT_DISABLE, ECSP14_SS0, ECSP14_MOSI, ECSP14_SCLK for BT Add R2107-R2116 to reduce the VSNVS power consumption due to the TAMPER reason Add L903-L930 as FCC/CE backup Change Camera J1801 connector direction on layout Add C905 Change J1701 from TOP contact to BOT contact for BT
C1	2016-05-05	Javen	1 DNP J1801, J1001 due to cost reason
C2	18-Oct-2016	Marek B.	Updated to be NCL compliance. - parts: J901, J1701, J1802, J2101 - Title blocks
C3	17-May-2018	Marek B.	U1302 set to DNP (Obsolete) U1201 & U1202 changed to TJA1044GT/3
D	14-Sept-2022	Ananya Gupta	1. U1401 is updated to WM8962BEC5N/R 2. D1903 is updated to APB83025ESGC-F01 3. J1001 is updated to HD119F-3A04205 4. U1301 is updated to FLS8974CFR3 5. U2106 (UM1750S-00) is added for generating DVDD_1V8
E	17-April-2023	Bhaskar Reddy N	1. R1807, R1808, R1810, R1811 value updated to 1.2K 2. R1407, R1431, R1432, R1433, R1434 value updated to 51 Ohms 3. Updated the block diagram & Power tree 4. Added I2C redriver U2107(TCA9416DDFR) for I2C2 port near Audio Codec 5. Added R2141, R2142, R2143, R2144, R2145, R2146, R2147, C2161 6. Made DNP - R2141, R2142, R2143, R2144, R2146, R2147 7. Added R2148

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:

_B Denotes - Active-Low Signal
<> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

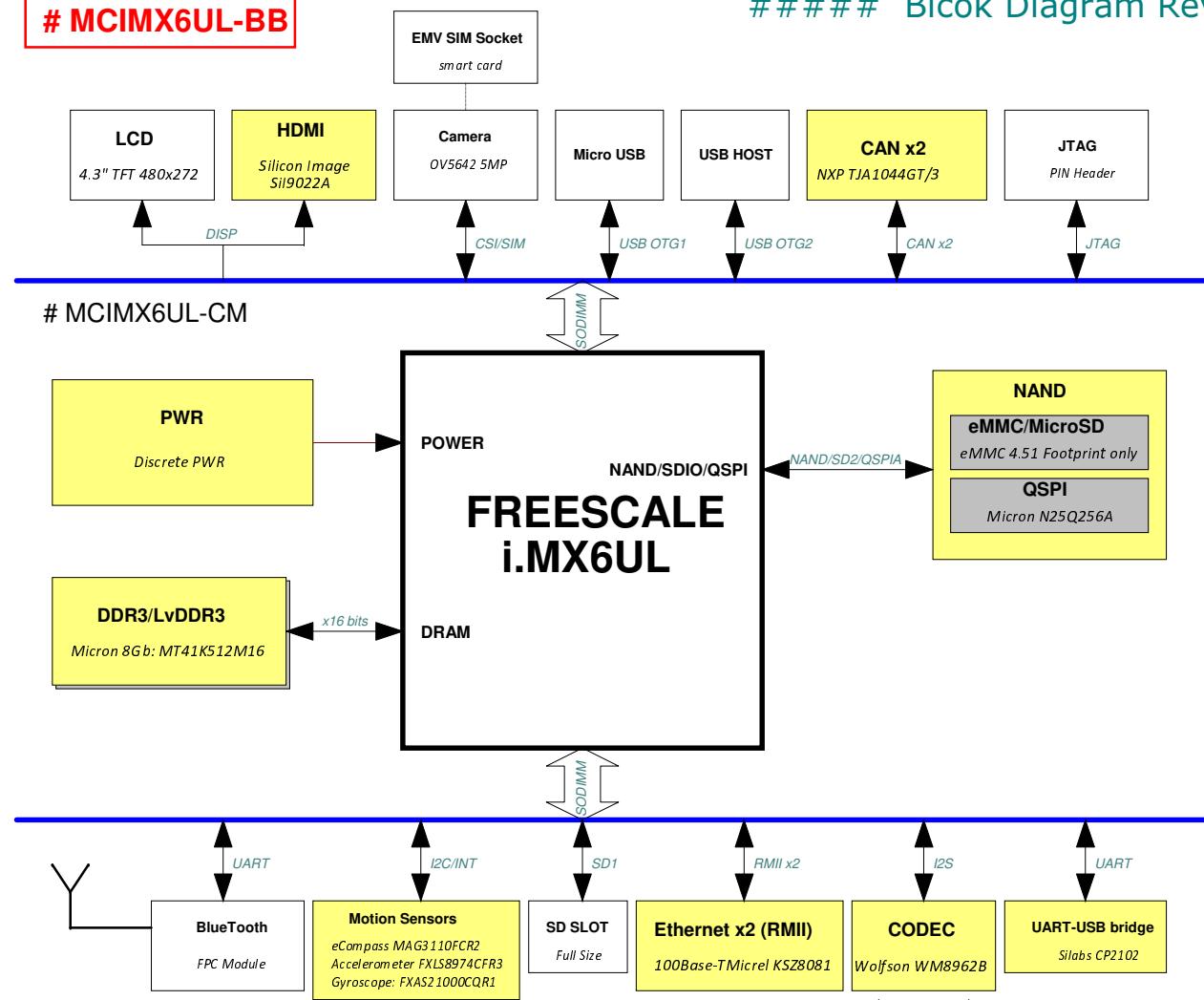
 Microcontroller Solutions Group 6501 William Cannon Drive West Austin, TX 78735-8588	
<small>This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.</small>	
<small>(C) NXP SEMICONDUCTORS Classification: X -PUB-</small>	
<small>Designer: _____ Drawing Title: _____</small>	
<small>Drawn by: _____ Page Title: _____</small>	
<small>Approved: _____ Title and Rev History</small>	
<small>Size: C Document Number: SCH-28616 PDF: SPF-28616 Rev: E</small>	
<small>Date: Thursday, April 20, 2023 Sheet: 1 of 18</small>	

i.MX6UL EVK Block Diagram

MCIMX6UL-BB

Blcok Diagram Rev 1.0

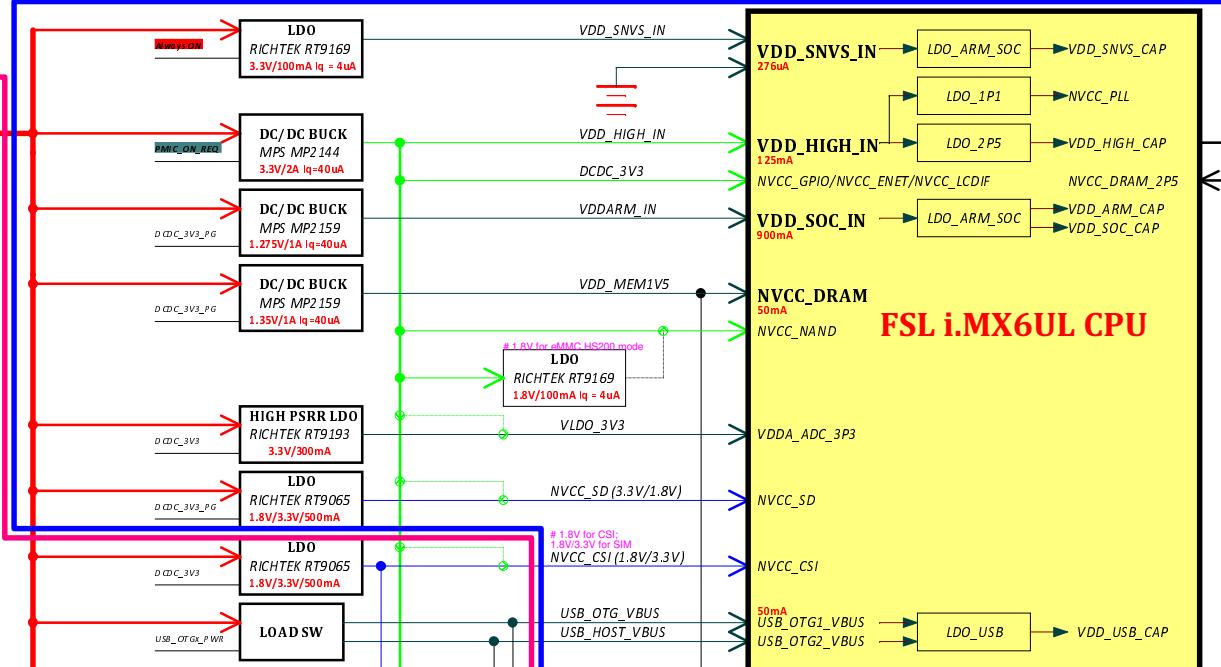
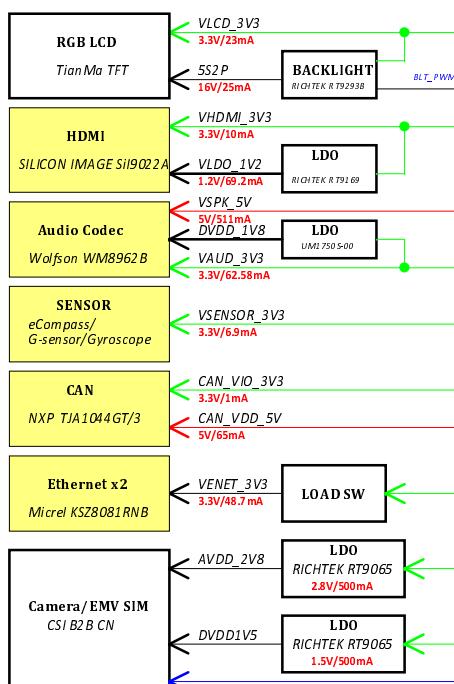
MPN: MCIMX6UL-BB
MPN: MCIMX6UL-CM
Agile No: 28616
Agile No: 28617



ICAP Classification:	CP:	ILO:	X	PUB:
Drawing Title: MCIMX6UL-BB				
Page Title: Block Diagram				
Size C Document Number SCH-28616 PDF: SPF-28616 Rev E				
Date: Thursday, April 20, 2023	Sheet 2	of	18	

i.MX6UL EVK PWR TREE

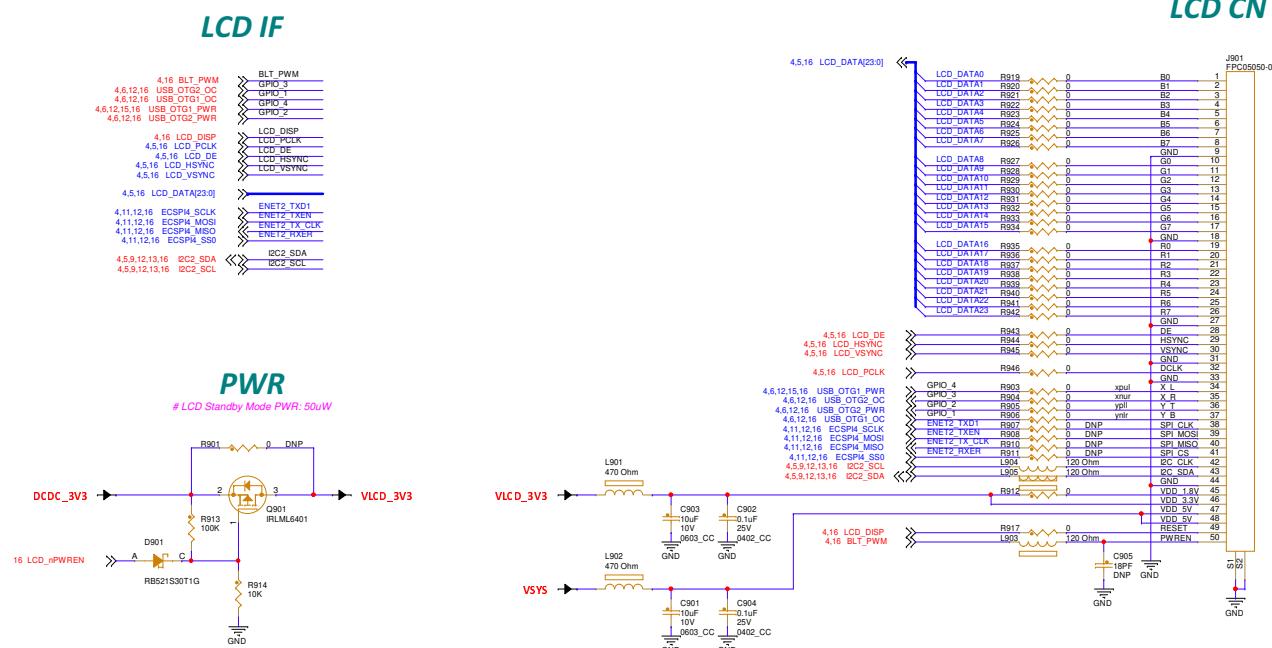
WALL Adapter: 5V/3A
MCIMX6UL-BB



MCIMX6UL-CM



ICAP Classification:	CP:	ILO:	X	PUB:	
Drawing Title: MCIMX6UL-BB					
Page Title: PWR TREE					
Size C Document Number SCH-28616 PDF: SPF-28616 Rev E					
Date: Thursday, April 20, 2023		Sheet 3	of	18	



ICAP Classification: CP: _____ IUO: X

Drawing Title:

MCIMX6UL-BB

Page Title: LCD

Size Document Number
C SCH-28616 RDE: SPE-286

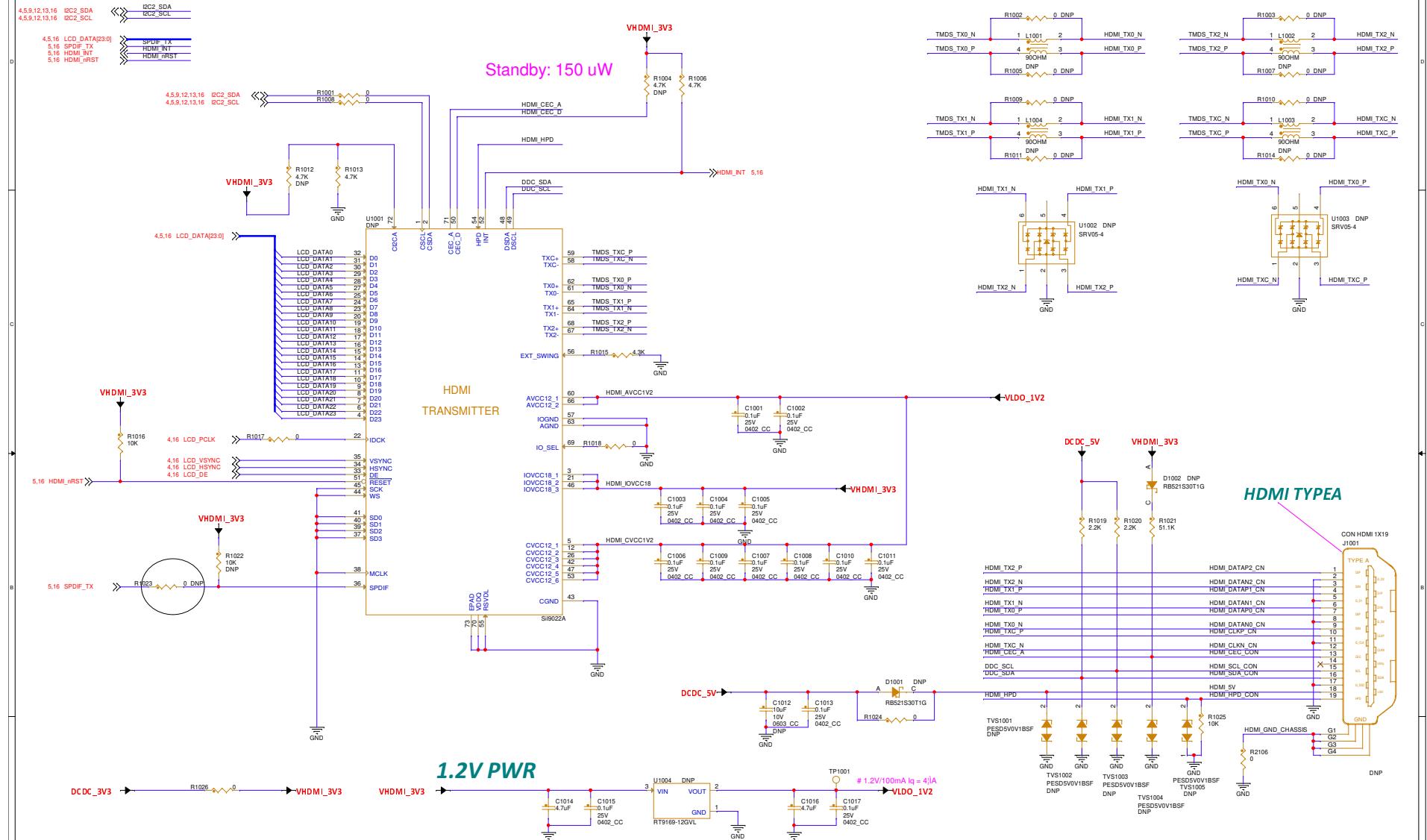
SCH-28616 PDF: SPF-286

Date: Thursday, April 20, 2023 Street
1

HDMI Transmitter

EMI/ESD

#Res Overlap with EMI Choke



NXP

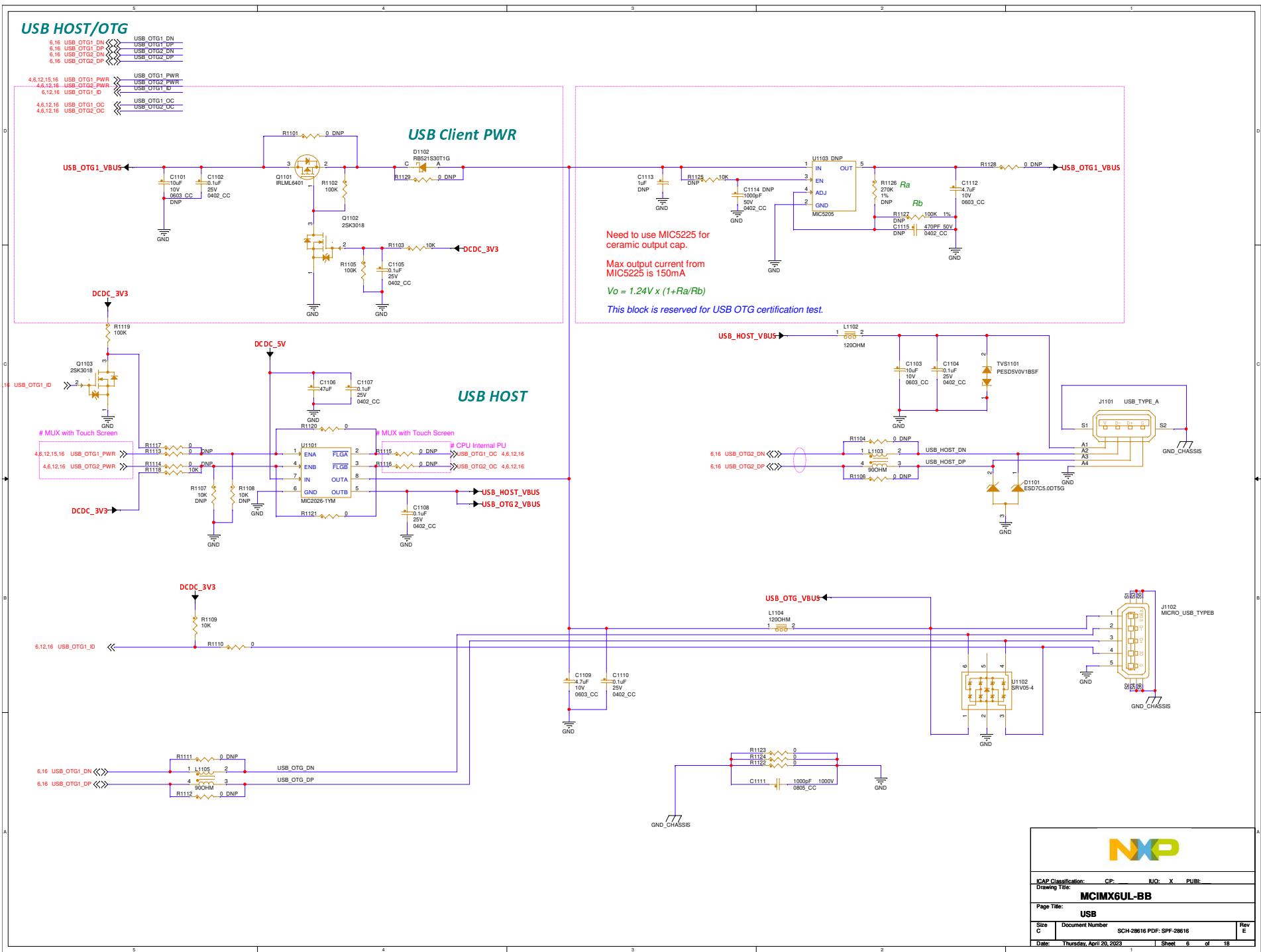
ICAP Classification: CP: X PUB:

Drawing Title: MCIMX6UL-BB

Page Title: HDMI

Size C Document Number SCH-28616 PDF: SPF-28616 Rev E

Date: Thursday, April 20, 2023 Sheet 5 of 18

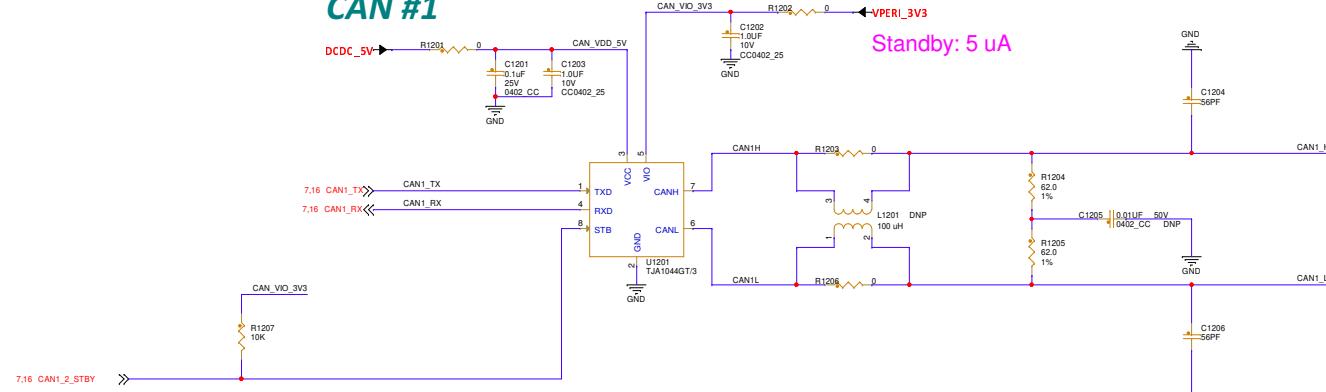


High Speed CAN Transceiver

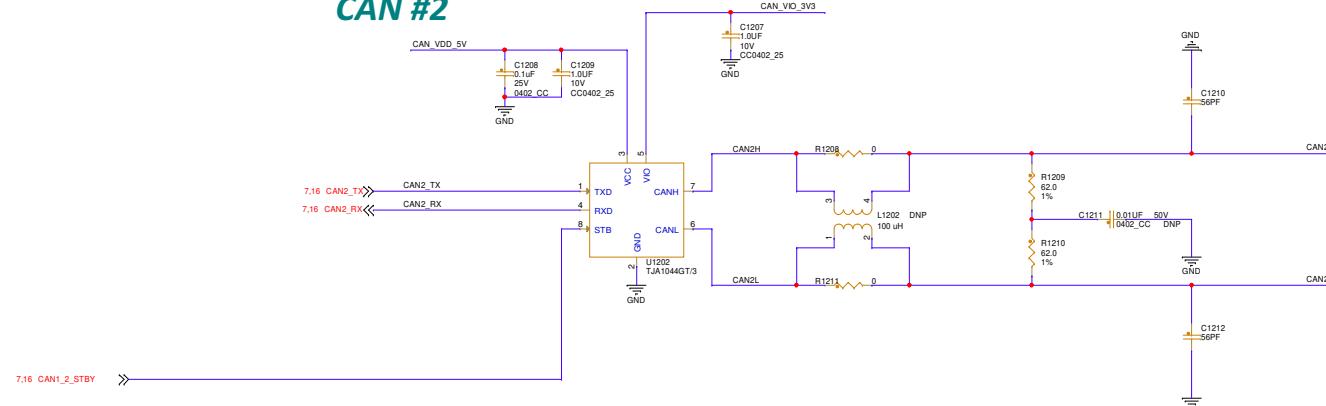
FSL High Speed CAN Transceiver



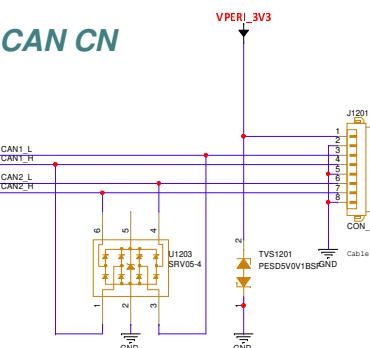
CAN #1



CAN #2



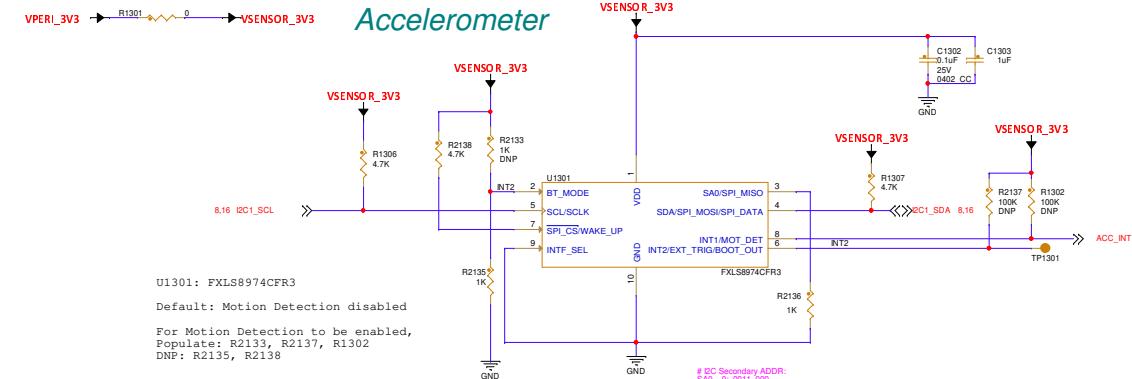
CAN CN



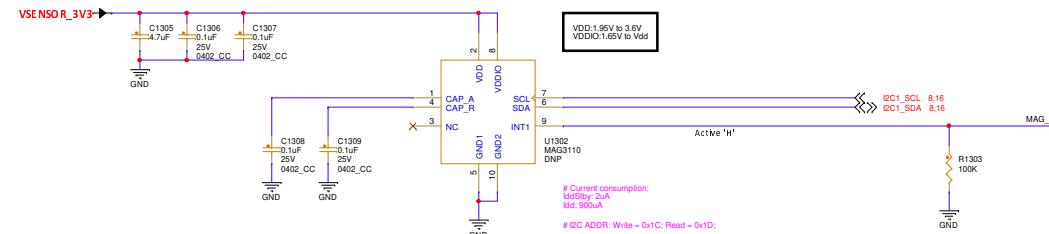
NXP

ICAP Classification:	CP:	I/O:	X	PUB:
Drawing Title: MCIMX6UL-BB				
Page Title: CAN				
Size C Document Number SCH-28616 PDF: SPF-28616 Rev E				
Date: Thursday, April 20, 2023	Sheet 7	of	18	

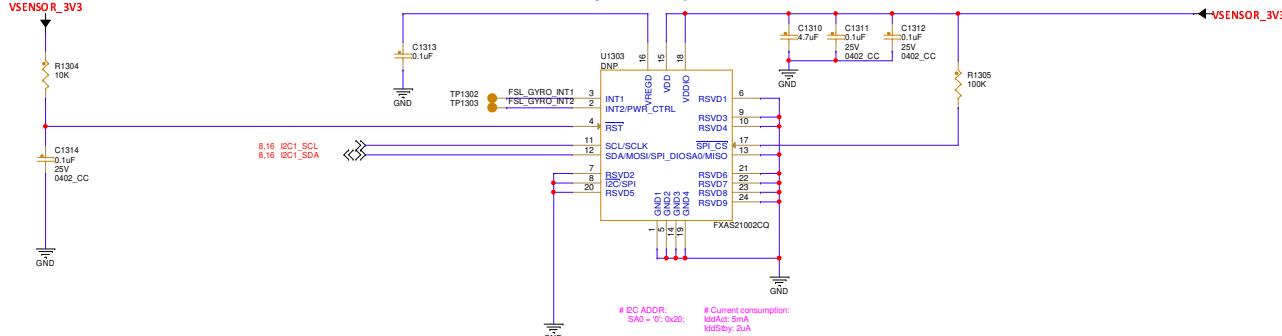
Motion Sensor 9-axis



e-Compass

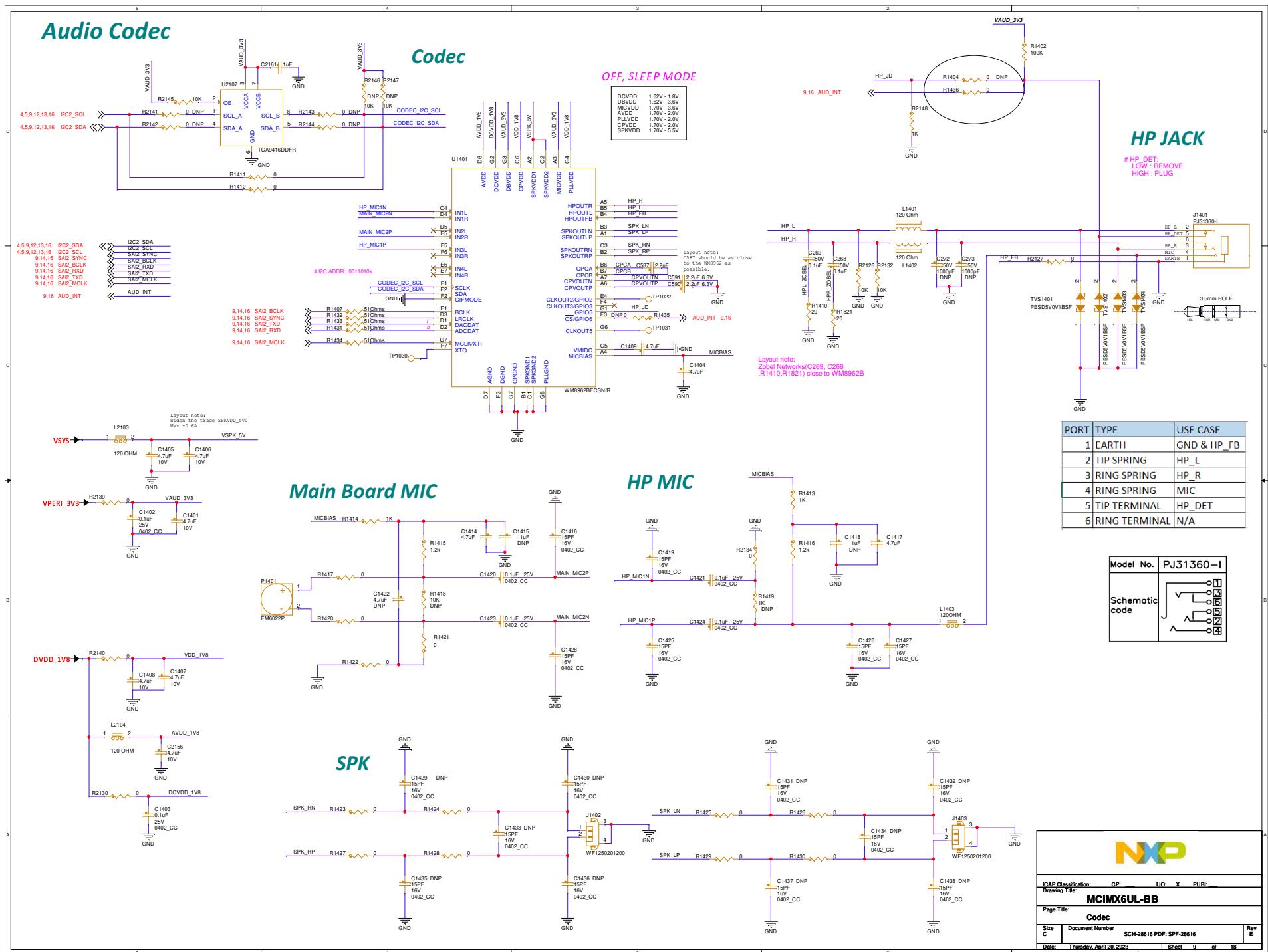


Gyroscope



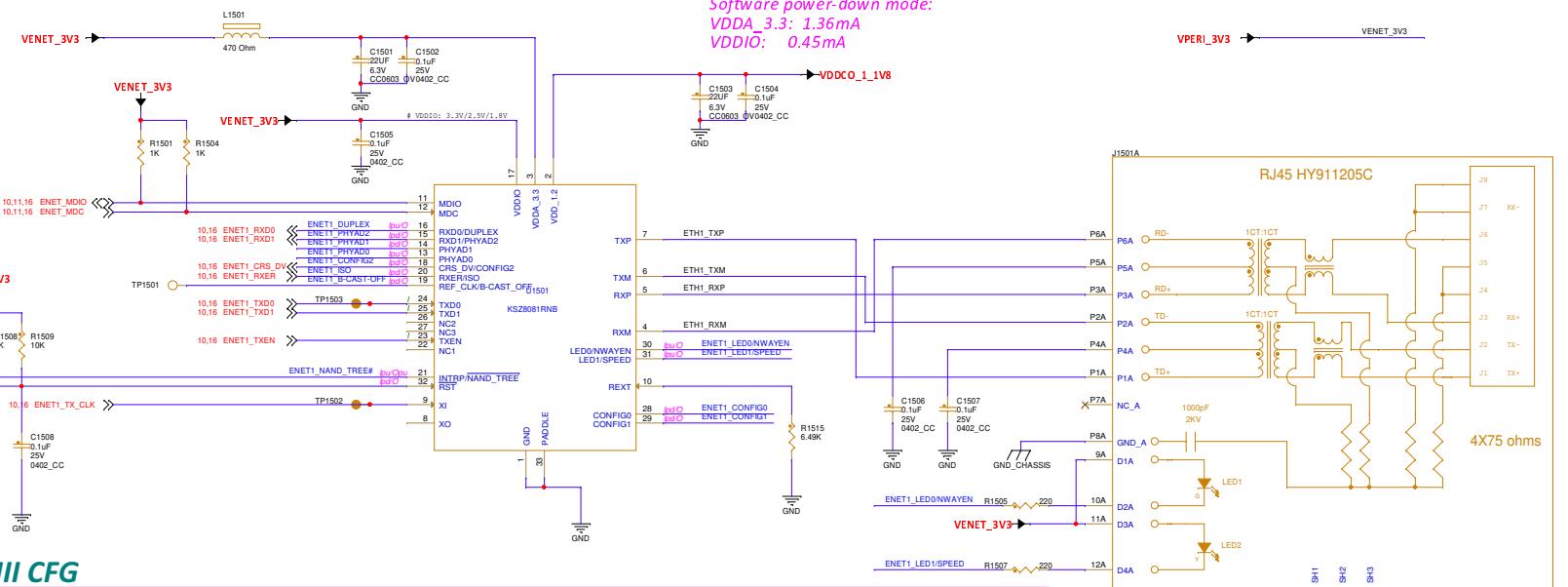
NXP

ICAP Classification:	CP: X	ILO: X	PUB: E
Drawing Title: MCIMX6UL-BB			
Page Title: Sensor			
Size C	Document Number	SCH-28616 PDF: SPF-28616	Rev E
Date: Thursday, April 20, 2023	Sheet 8	of 18	

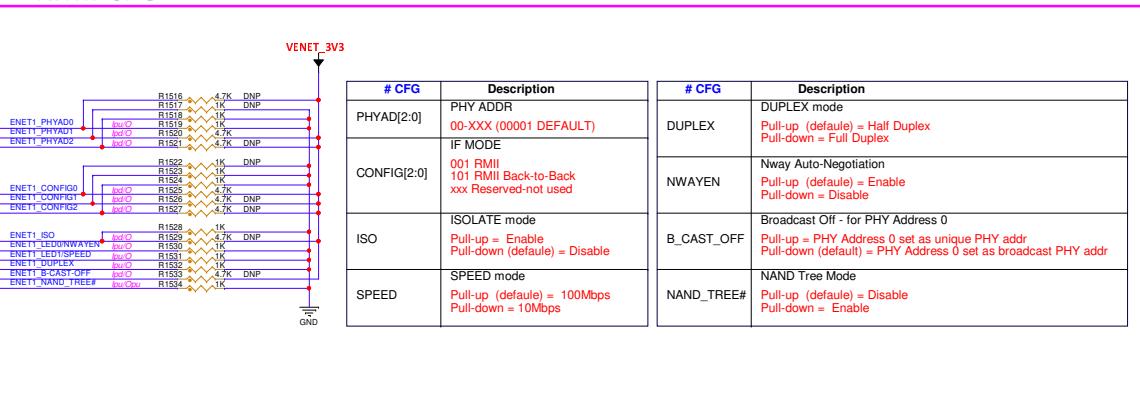


100M ETHERNET RMII PHY x1

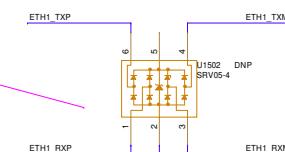
10,11,16 ENET_MDO
10,11,16 ENET_MDC
10,11,16 ENET1_RXD0
10,16 ENET1_RXD1
10,16 ENET1_RXD2
10,16 ENET1_TX_Clk
10,16 ENET1_RXD0
10,16 ENET1_RXD1
10,16 ENET1_RXD2
10,16 ENET1_RXR
10,16 ENET1_CRS_DV
10,16 ENET1_nINT
11,16 ENET1_RST



RMII CFG

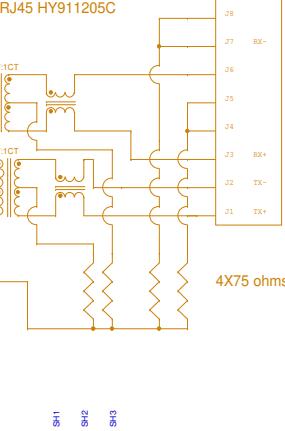


2rd LEVEL ESD



PHY PWR

VPERI_3V3 → VENET_3V3

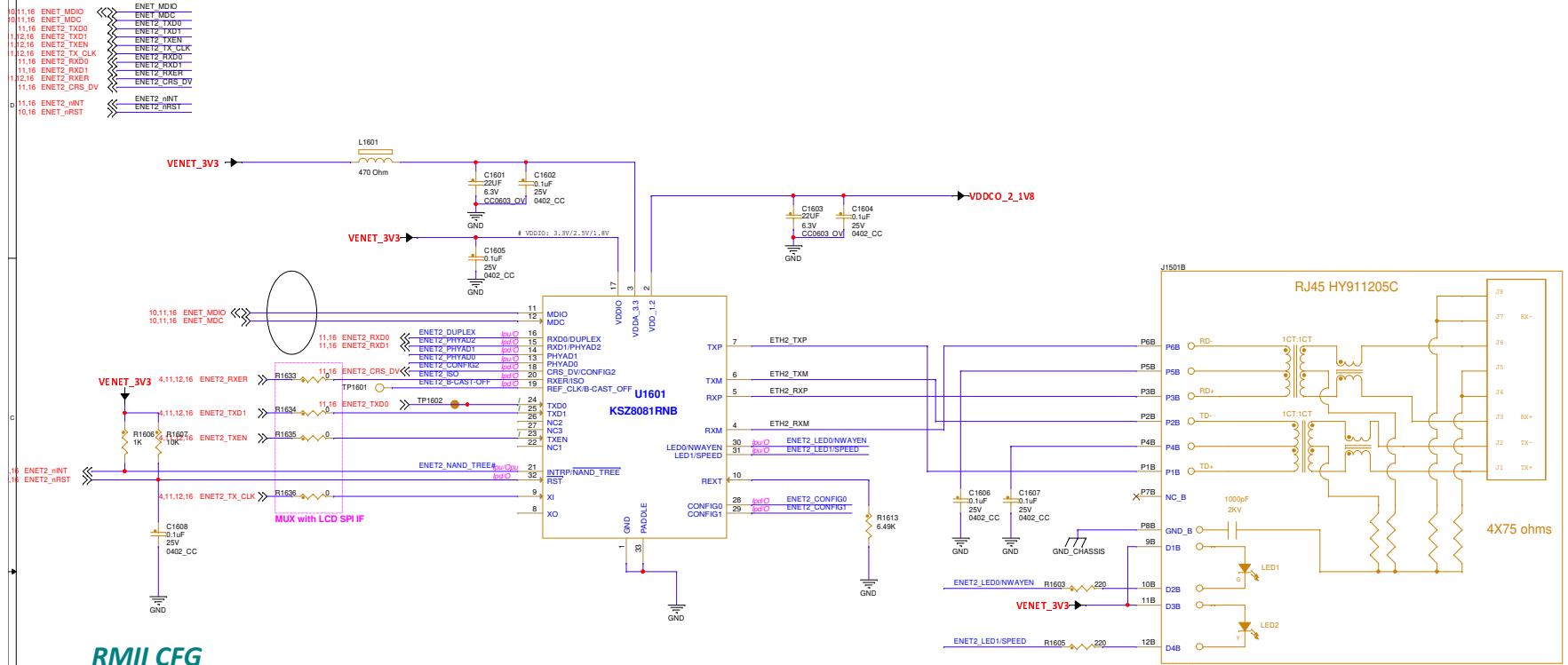


ESD PROTECTION

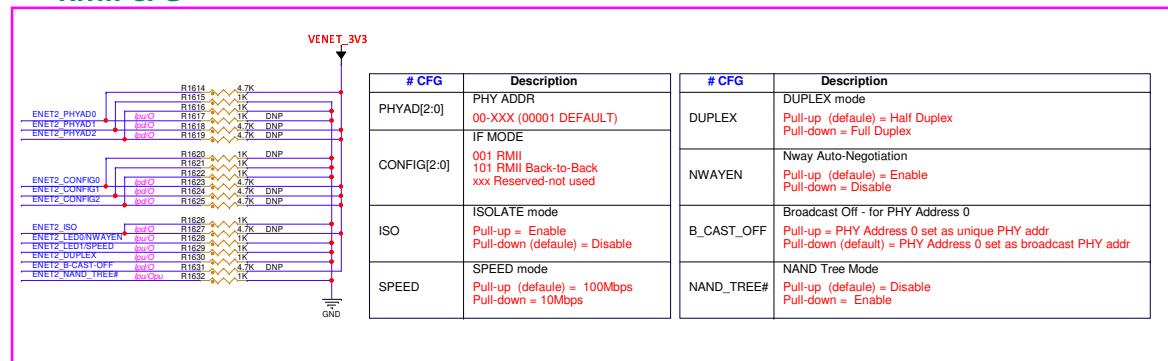
NXP

ICAP Classification: CP: I/O: X PUBL:
Drawing Title: MCIMX6UL-BB
Page Title:
ENET x1
Size C Document Number SCH-28616 PDF: SPF-28616 Rev E
Date: Thursday, April 20, 2023 Sheet 10 of 18

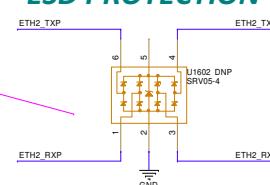
100M ETHERNET RMII PHY x2



RMII CFG



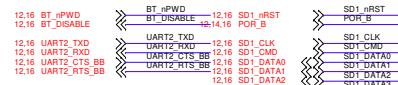
2rd LEVEL ESD



NXP

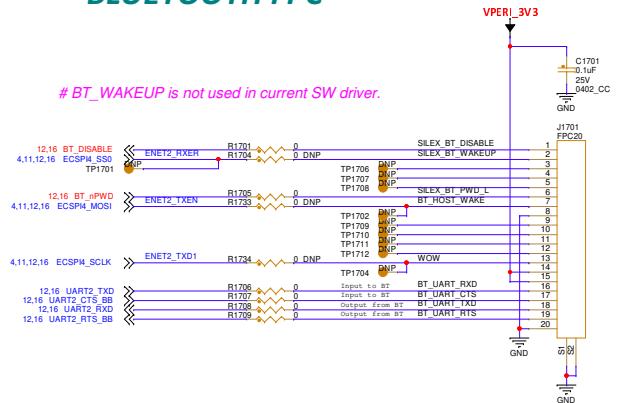
ICAP Classification:	CP:	ILO:	X	PUB:
Drawing Title:	MCIMX6UL-BB			
Page Title:	ENET x2			
Size	Document Number	SCH-28616 PDF: SPF-28616		Rev E
C				
Date:	Thursday, April 20, 2023		Sheet 11 of 18	

BLUETOOTH / SD FULL SOCKET

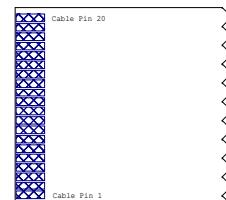


NOTE:
The AUX SDIO CARD SOCKET and the BLUETOOTH CABLE CONNECTOR have been designed and tested specifically for use with the WiFi/BT combo card SX-SDCAN-2830BT Developed and sold by Silex Technology. The developer may need to consult the datasheet of other WiFi solutions for compatibility with this card socket.

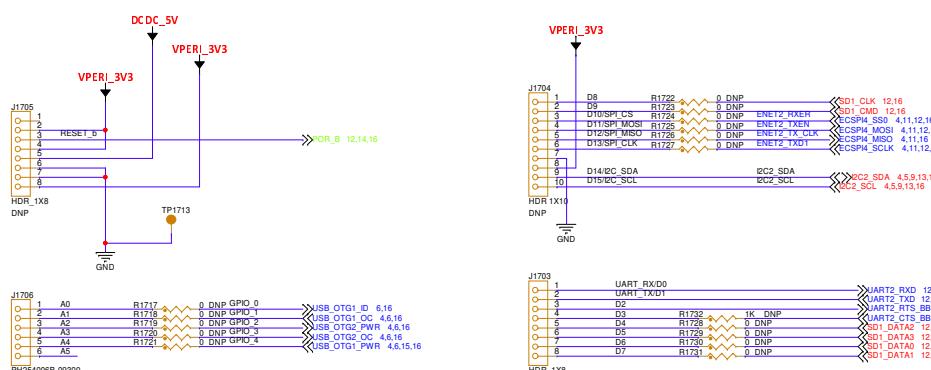
BLUETOOTH FPC



NOTE:
Pin 1 of the cable connector on the Smart Device board is opposite Pin 20 of the WiFi/BT module. For the FFC to lie flat, the pin order number needs to be reversed on the schematics.

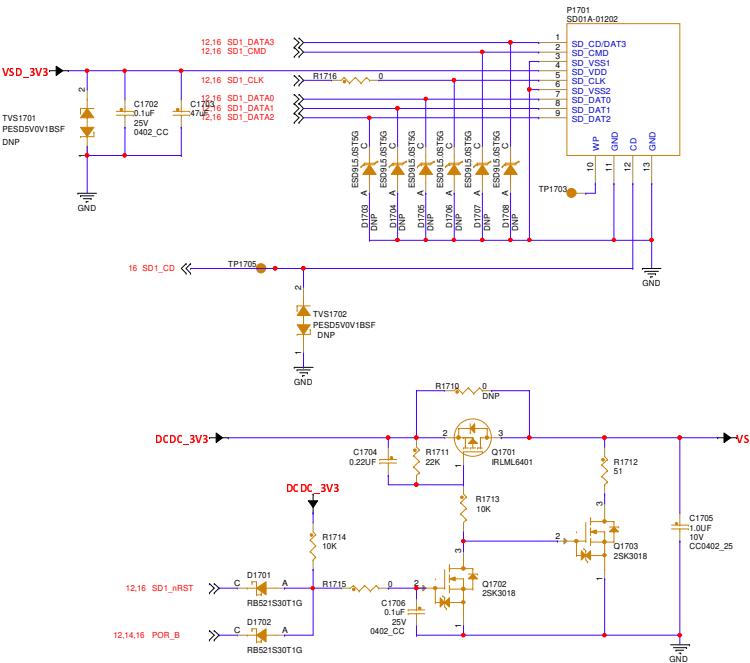


ARDUINO_HEADERS



SD SLOT

for WiFi and SD Accessories



NXP

ICAP Classification: CP: ILO: X PUB:

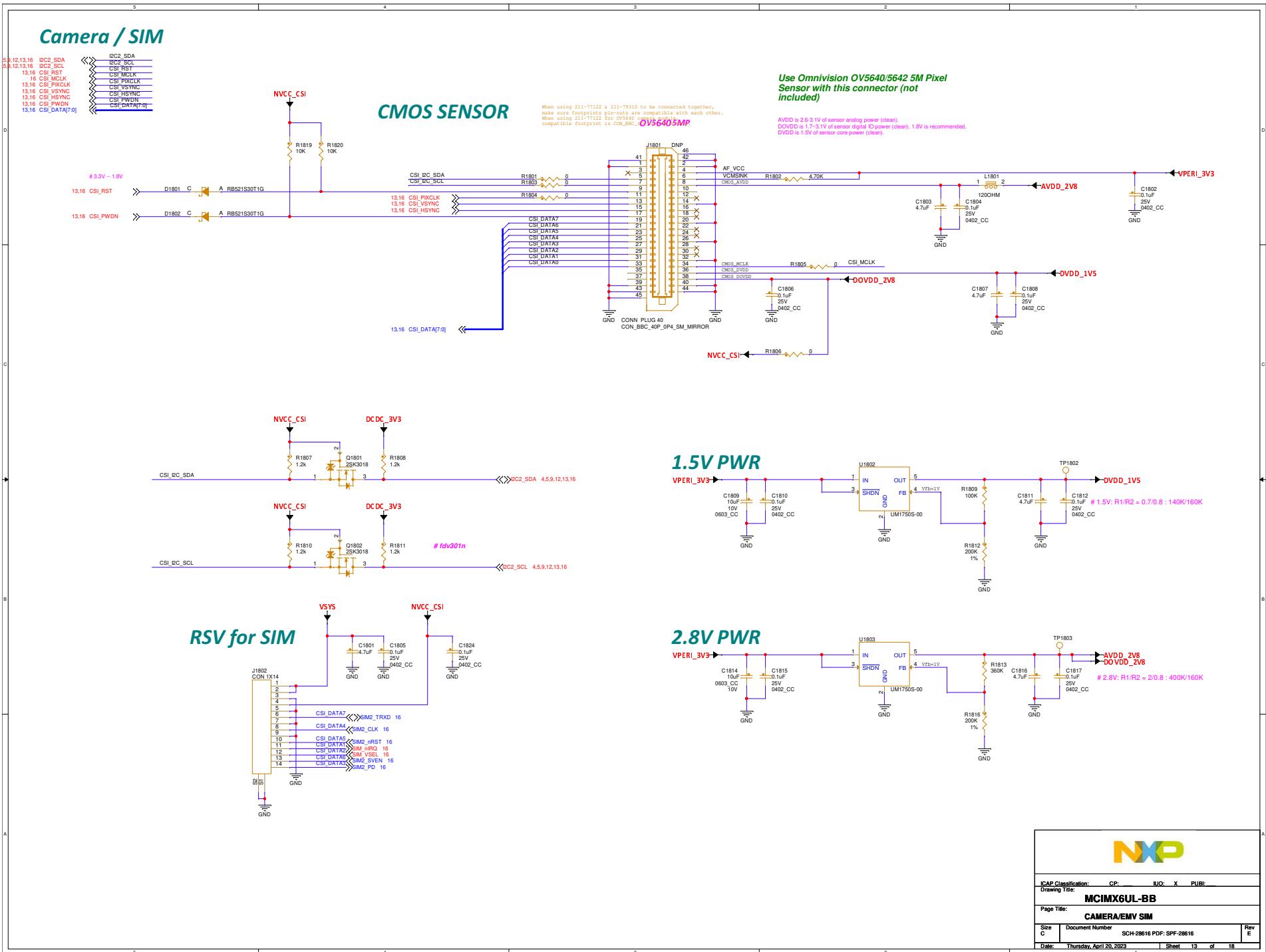
Drawing Title: MCIMX6UL-BB

Page Title:

BT/SD

Size C Document Number SCH-28616 PDF: SPF-28616 Rev E

Date: Thursday, April 20, 2023 Sheet 12 of 18

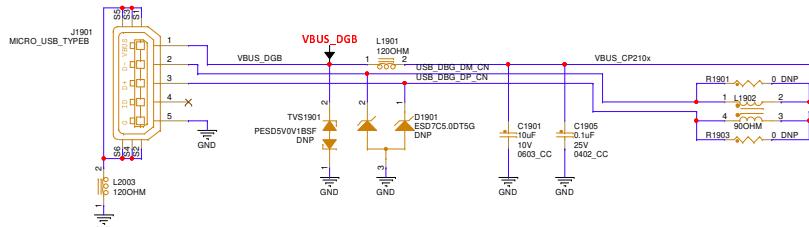


UART-USB DBG / JTAG

9,14,16 JTAG_nTRST
9,14,16 JTAG_TDI
9,14,16 JTAG_TDO
9,14,16 JTAG_TMS
9,14,16 JTAG_TCK
12,14,16 POR_B

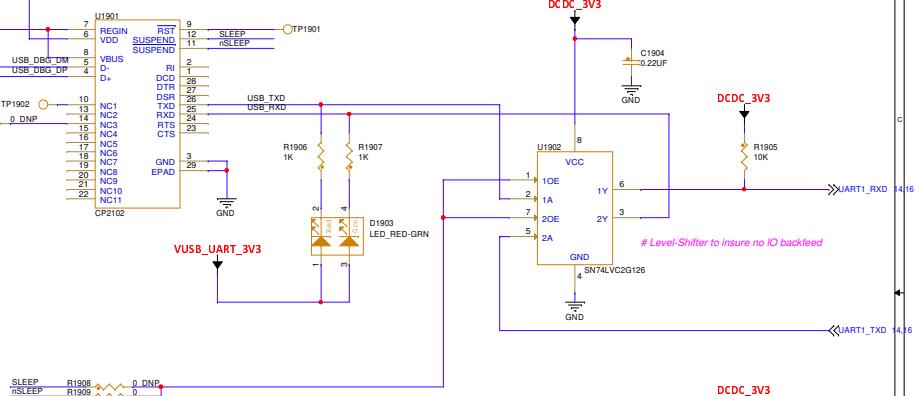
14,16 UART1_RXD
14,16 UART1_TXD

UART1_RXD
UART1_TXD



VUSB_UART_3V3

USB-UART Bridge



VUSB_UART_3V3

SLEEP

nSLEEP

R1908

R1909

R1910

R1911

R1912

R1913

R1914

R1915

R1916

R1917

R1918

R1919

R1920

R1921

R1922

R1923

R1924

R1925

R1926

R1927

R1928

R1929

R1930

R1931

R1932

R1933

R1934

R1935

R1936

R1937

R1938

R1939

R1940

R1941

R1942

R1943

R1944

R1945

R1946

R1947

R1948

R1949

R1950

R1951

R1952

R1953

R1954

R1955

R1956

R1957

R1958

R1959

R1960

R1961

R1962

R1963

R1964

R1965

R1966

R1967

R1968

R1969

R1970

R1971

R1972

R1973

R1974

R1975

R1976

R1977

R1978

R1979

R1980

R1981

R1982

R1983

R1984

R1985

R1986

R1987

R1988

R1989

R1990

R1991

R1992

R1993

R1994

R1995

R1996

R1997

R1998

R1999

R2000

R2001

R2002

R2003

R2004

R2005

R2006

R2007

R2008

R2009

R2010

R2011

R2012

R2013

R2014

R2015

R2016

R2017

R2018

R2019

R2020

R2021

R2022

R2023

R2024

R2025

R2026

R2027

R2028

R2029

R2030

R2031

R2032

R2033

R2034

R2035

R2036

R2037

R2038

R2039

R2040

R2041

R2042

R2043

R2044

R2045

R2046

R2047

R2048

R2049

R2050

R2051

R2052

R2053

R2054

R2055

R2056

R2057

R2058

R2059

R2060

R2061

R2062

R2063

R2064

R2065

R2066

R2067

R2068

R2069

R2070

R2071

R2072

R2073

R2074

R2075

R2076

R2077

R2078

R2079

R2080

R2081

R2082

R2083

R2084

R2085

R2086

R2087

R2088

R2089

R2090

R2091

R2092

R2093

R2094

R2095

R2096

R2097

R2098

R2099

R2100

R2101

R2102

R2103

R2104

R2105

R2106

R2107

R2108

R2109

R2110

R2111

R2112

R2113

R2114

R2115

R2116

R2117

R2118

R2119

R2120

R2121

R2122

R2123

R2124

R2125

R2126

R2127

R2128

R2129

R2130

R2131

R2132

R2133

R2134

R2135

R2136

R2137

R2138

R2139

R2140

R2141

R2142

R2143

R2144

R2145

R2146

R2147

R2148

R2149

R2150

R2151

R2152

R2153

R2154

R2155

R2156

R2157

R2158

R2159

R2160

R2161

R2162

R2163

R2164

R2165

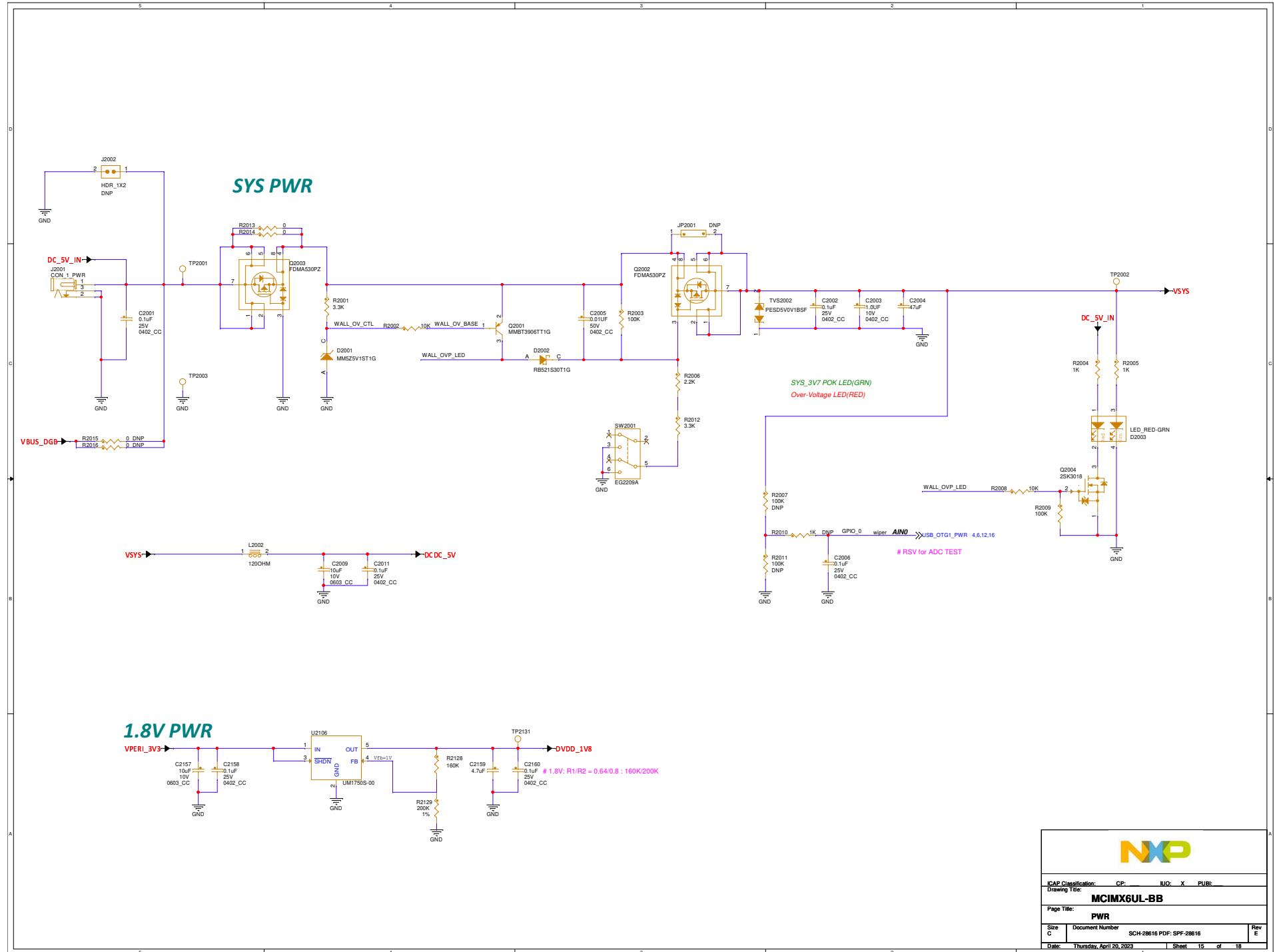
R2166

R2167

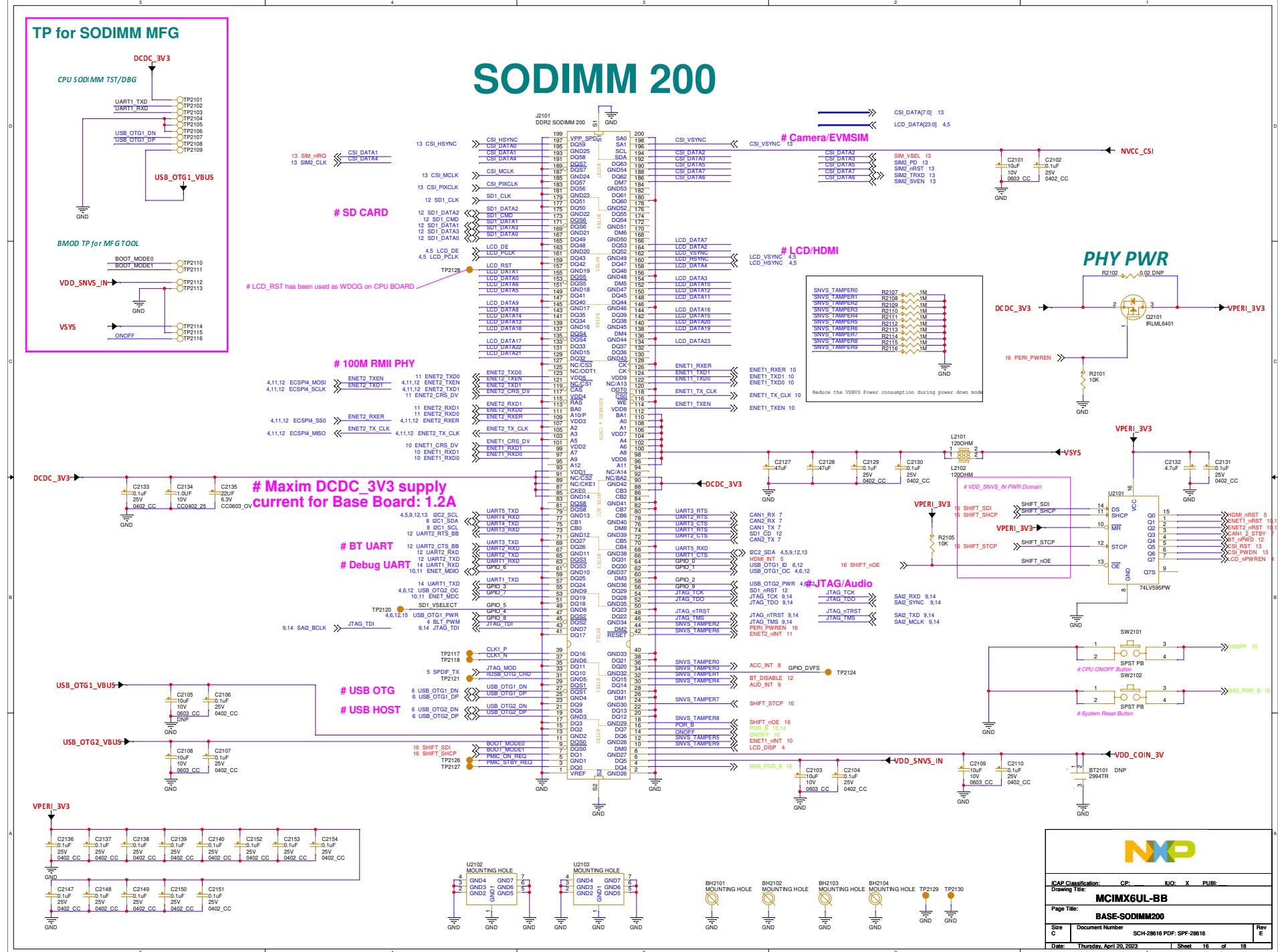
R2168

R2169

R2170



SODIMM 200



NOTE: EMV SIM will be placed on the daughter board

All pins using ~reset as harden :

PAD	Default State	Simulation Value
UART3_TX_DATA	Output Buffer(LOW) during reset --> Output keeper + Input enable after reset done	0 in real silicon
LCD_DATA00~LCD_DATA23	100K pull down + input enable during reset --> Output keeper + Input enable after reset done (this is boot option, we don't need change)	0 in real silicon

PAD	Default State	Signal Path	PAD Simulation Value
UART3_TX_DATA	Output Buffer(LOW) during reset --> Output keeper + Input enable after reset done	sjc.ipt_jta_active --> PAD	0 in real silicon
		(note : sjc.ipt_jta_active also connected to snvs_hp.sec_vio_in_1. This is security related, we don't plan to change it.)	ALT7

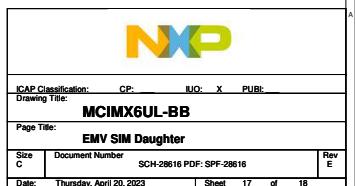
All pins using ~src.en_system_clk as harden :

PAD	Default State	Simulation Value
GPIO1_IO03	100K pull down + input enable during reset --> Output keeper + Input enable after reset done	0 in real silicon

PAD	Default State	Signal Path	PAD Simulation Value
GPIO1_IO03	100K pull down + input enable during reset --> Output keeper + Input enable after reset done	PAD --> ccmsrcmix. src_tester_ack	0 in real silicon
		This is the requirement of TE test	ALT7

All pins using snvs_hp.snvs_sec_vio_in_5_en as harden :

PAD	Default State	Simulation Value
CSI_PIXCLK	Output keeper + Input enable (snvs_sec_vio_in_5_en is 1 b0 in normal state, so harden is not triggered in normal state). snvs_sec_vio_in_5_en is controlled by SNVS register. It can be disable or enable.	X (0 or 1 in real silicon)



	5	4	3	2	1
D	i.MX6UL IOMUX				
	NAME	Default	ALTo	ALT1	ALT2
	TEST_MODE	Icu.TEST_MODE	Icu.TEST_MODE		
	ICU_PWDN	SIG_PWDN_B	SIG_PWDN_B		
	SNVS_PMC_O_N_REQ	snvs.DL_Wrapper,SNVS_WAKEUP_ALARM	snvs.DL_Wrapper,SNVS_WAKEUP_ALARM		
	CSU_BOOT_BT1_REQ	snvs.DL_Wrapper,SNVS_BT1	snvs.DL_Wrapper,SNVS_BT1		
	BOOT_MODE1	snic.BOOT_MODE[0]	snic.BOOT_MODE[0]		
	BOOT_MODE2	snic.BOOT_MODE[1]	snic.BOOT_MODE[1]		
	SWI_BT1	snvs.DL_Wrapper,SNVS_BT1	snvs.DL_Wrapper,SNVS_BT1		
	SHVS_TAMPER1	snvs.DL_Wrapper,TAMPER1	snvs.DL_Wrapper,TAMPER1		
	SHVS_TAMPER2	snvs.DL_Wrapper,TAMPER2	snvs.DL_Wrapper,TAMPER2		
	SHVS_TAMPER3	snvs.DL_Wrapper,TAMPER3	snvs.DL_Wrapper,TAMPER3		
	SHVS_TAMPER4	snvs.DL_Wrapper,TAMPER4	snvs.DL_Wrapper,TAMPER4		
	SHVS_TAMPER5	snvs.DL_Wrapper,TAMPER5	snvs.DL_Wrapper,TAMPER5		
	SHVS_TAMPER6	snvs.DL_Wrapper,TAMPER6	snvs.DL_Wrapper,TAMPER6		
	SHVS_TAMPER7	snvs.DL_Wrapper,TAMPER7	snvs.DL_Wrapper,TAMPER7		
	SHVS_TAMPER8	snvs.DL_Wrapper,TAMPER8	snvs.DL_Wrapper,TAMPER8		
	SHVS_TAMPER9	snvs.DL_Wrapper,TAMPER9	snvs.DL_Wrapper,TAMPER9		
	ITAG_IOD	sig.IOD[0]	sig.IOD[0]		
	JTAG_TMS	sig.JTMS	sig.JTMS		
	JTAG_TDI	sig.JTDI	sig.JTDI		
	JTAG_TDO	sig.JTDO	sig.JTDO		
	JTAG_TSTB	sig.JTSTB	sig.JTSTB		
	G_P0_1_0_0	gpb0_1_0_0	gpb0_1_0_0		
	G_P0_1_0_1	gpb0_1_0_1	gpb0_1_0_1		
	G_P0_1_0_2	gpb0_1_0_2	gpb0_1_0_2		
	G_P0_1_0_3	gpb0_1_0_3	gpb0_1_0_3		
	G_P0_1_0_4	gpb0_1_0_4	anatop.ENET_REF_Clk1		
	G_P0_1_0_5	gpb0_1_0_5	anatop.ENET_REF_Clk2		
	G_P0_1_0_6	gpb0_1_0_6	anatop.ENET_REF_Clk3		
	G_P0_1_0_7	gpb0_1_0_7	anatop.ENET_REF_Clk4		
	G_P0_1_0_8	gpb0_1_0_8	anatop.ENET_REF_Clk5		
	G_P0_1_0_9	gpb0_1_0_9	anatop.ENET_REF_Clk6		
	G_P0_1_0_10	gpb0_1_0_10	anatop.ENET_REF_Clk7		
	G_P0_1_0_11	gpb0_1_0_11	anatop.ENET_REF_Clk8		
	G_P0_1_0_12	gpb0_1_0_12	anatop.ENET_REF_Clk9		
	G_P0_1_0_13	gpb0_1_0_13	anatop.ENET_REF_Clk10		
	G_P0_1_0_14	gpb0_1_0_14	anatop.ENET_REF_Clk11		
	G_P0_1_0_15	gpb0_1_0_15	anatop.ENET_REF_Clk12		
	G_P0_1_0_16	gpb0_1_0_16	anatop.ENET_REF_Clk13		
	G_P0_1_0_17	gpb0_1_0_17	anatop.ENET_REF_Clk14		
	G_P0_1_0_18	gpb0_1_0_18	anatop.ENET_REF_Clk15		
	G_P0_1_0_19	gpb0_1_0_19	anatop.ENET_REF_Clk16		
	G_P0_1_0_20	gpb0_1_0_20	anatop.ENET_REF_Clk17		
	G_P0_1_0_21	gpb0_1_0_21	anatop.ENET_REF_Clk18		
	G_P0_1_0_22	gpb0_1_0_22	anatop.ENET_REF_Clk19		
	G_P0_1_0_23	gpb0_1_0_23	anatop.ENET_REF_Clk20		
	G_P0_1_0_24	gpb0_1_0_24	anatop.ENET_REF_Clk21		
	G_P0_1_0_25	gpb0_1_0_25	anatop.ENET_REF_Clk22		
	G_P0_1_0_26	gpb0_1_0_26	anatop.ENET_REF_Clk23		
	G_P0_1_0_27	gpb0_1_0_27	anatop.ENET_REF_Clk24		
	G_P0_1_0_28	gpb0_1_0_28	anatop.ENET_REF_Clk25		
	G_P0_1_0_29	gpb0_1_0_29	anatop.ENET_REF_Clk26		
	G_P0_1_0_30	gpb0_1_0_30	anatop.ENET_REF_Clk27		
	G_P0_1_0_31	gpb0_1_0_31	anatop.ENET_REF_Clk28		
	G_P0_1_0_32	gpb0_1_0_32	anatop.ENET_REF_Clk29		
	G_P0_1_0_33	gpb0_1_0_33	anatop.ENET_REF_Clk30		
	G_P0_1_0_34	gpb0_1_0_34	anatop.ENET_REF_Clk31		
	G_P0_1_0_35	gpb0_1_0_35	anatop.ENET_REF_Clk32		
	G_P0_1_0_36	gpb0_1_0_36	anatop.ENET_REF_Clk33		
	G_P0_1_0_37	gpb0_1_0_37	anatop.ENET_REF_Clk34		
	G_P0_1_0_38	gpb0_1_0_38	anatop.ENET_REF_Clk35		
	G_P0_1_0_39	gpb0_1_0_39	anatop.ENET_REF_Clk36		
	G_P0_1_0_40	gpb0_1_0_40	anatop.ENET_REF_Clk37		
	G_P0_1_0_41	gpb0_1_0_41	anatop.ENET_REF_Clk38		
	G_P0_1_0_42	gpb0_1_0_42	anatop.ENET_REF_Clk39		
	G_P0_1_0_43	gpb0_1_0_43	anatop.ENET_REF_Clk40		
	G_P0_1_0_44	gpb0_1_0_44	anatop.ENET_REF_Clk41		
	G_P0_1_0_45	gpb0_1_0_45	anatop.ENET_REF_Clk42		
	G_P0_1_0_46	gpb0_1_0_46	anatop.ENET_REF_Clk43		
	G_P0_1_0_47	gpb0_1_0_47	anatop.ENET_REF_Clk44		
	G_P0_1_0_48	gpb0_1_0_48	anatop.ENET_REF_Clk45		
	G_P0_1_0_49	gpb0_1_0_49	anatop.ENET_REF_Clk46		
	G_P0_1_0_50	gpb0_1_0_50	anatop.ENET_REF_Clk47		
	G_P0_1_0_51	gpb0_1_0_51	anatop.ENET_REF_Clk48		
	G_P0_1_0_52	gpb0_1_0_52	anatop.ENET_REF_Clk49		
	G_P0_1_0_53	gpb0_1_0_53	anatop.ENET_REF_Clk50		
	G_P0_1_0_54	gpb0_1_0_54	anatop.ENET_REF_Clk51		
	G_P0_1_0_55	gpb0_1_0_55	anatop.ENET_REF_Clk52		
	G_P0_1_0_56	gpb0_1_0_56	anatop.ENET_REF_Clk53		
	G_P0_1_0_57	gpb0_1_0_57	anatop.ENET_REF_Clk54		
	G_P0_1_0_58	gpb0_1_0_58	anatop.ENET_REF_Clk55		
	G_P0_1_0_59	gpb0_1_0_59	anatop.ENET_REF_Clk56		
	G_P0_1_0_60	gpb0_1_0_60	anatop.ENET_REF_Clk57		
	G_P0_1_0_61	gpb0_1_0_61	anatop.ENET_REF_Clk58		
	G_P0_1_0_62	gpb0_1_0_62	anatop.ENET_REF_Clk59		
	G_P0_1_0_63	gpb0_1_0_63	anatop.ENET_REF_Clk60		
	G_P0_1_0_64	gpb0_1_0_64	anatop.ENET_REF_Clk61		
	G_P0_1_0_65	gpb0_1_0_65	anatop.ENET_REF_Clk62		
	G_P0_1_0_66	gpb0_1_0_66	anatop.ENET_REF_Clk63		
	G_P0_1_0_67	gpb0_1_0_67	anatop.ENET_REF_Clk64		
	G_P0_1_0_68	gpb0_1_0_68	anatop.ENET_REF_Clk65		
	G_P0_1_0_69	gpb0_1_0_69	anatop.ENET_REF_Clk66		
	G_P0_1_0_70	gpb0_1_0_70	anatop.ENET_REF_Clk67		
	G_P0_1_0_71	gpb0_1_0_71	anatop.ENET_REF_Clk68		
	G_P0_1_0_72	gpb0_1_0_72	anatop.ENET_REF_Clk69		
	G_P0_1_0_73	gpb0_1_0_73	anatop.ENET_REF_Clk70		
	G_P0_1_0_74	gpb0_1_0_74	anatop.ENET_REF_Clk71		
	G_P0_1_0_75	gpb0_1_0_75	anatop.ENET_REF_Clk72		
	G_P0_1_0_76	gpb0_1_0_76	anatop.ENET_REF_Clk73		
	G_P0_1_0_77	gpb0_1_0_77	anatop.ENET_REF_Clk74		
	G_P0_1_0_78	gpb0_1_0_78	anatop.ENET_REF_Clk75		
	G_P0_1_0_79	gpb0_1_0_79	anatop.ENET_REF_Clk76		
	G_P0_1_0_80	gpb0_1_0_80	anatop.ENET_REF_Clk77		
	G_P0_1_0_81	gpb0_1_0_81	anatop.ENET_REF_Clk78		
	G_P0_1_0_82	gpb0_1_0_82	anatop.ENET_REF_Clk79		
	G_P0_1_0_83	gpb0_1_0_83	anatop.ENET_REF_Clk80		
	G_P0_1_0_84	gpb0_1_0_84	anatop.ENET_REF_Clk81		
	G_P0_1_0_85	gpb0_1_0_85	anatop.ENET_REF_Clk82		
	G_P0_1_0_86	gpb0_1_0_86	anatop.ENET_REF_Clk83		
	G_P0_1_0_87	gpb0_1_0_87	anatop.ENET_REF_Clk84		
	G_P0_1_0_88	gpb0_1_0_88	anatop.ENET_REF_Clk85		
	G_P0_1_0_89	gpb0_1_0_89	anatop.ENET_REF_Clk86		
	G_P0_1_0_90	gpb0_1_0_90	anatop.ENET_REF_Clk87		
	G_P0_1_0_91	gpb0_1_0_91	anatop.ENET_REF_Clk88		
	G_P0_1_0_92	gpb0_1_0_92	anatop.ENET_REF_Clk89		
	G_P0_1_0_93	gpb0_1_0_93	anatop.ENET_REF_Clk90		
	G_P0_1_0_94	gpb0_1_0_94	anatop.ENET_REF_Clk91		
	G_P0_1_0_95	gpb0_1_0_95	anatop.ENET_REF_Clk92		
	G_P0_1_0_96	gpb0_1_0_96	anatop.ENET_REF_Clk93		
	G_P0_1_0_97	gpb0_1_0_97	anatop.ENET_REF_Clk94		
	G_P0_1_0_98	gpb0_1_0_98	anatop.ENET_REF_Clk95		
	G_P0_1_0_99	gpb0_1_0_99	anatop.ENET_REF_Clk96		
	G_P0_1_0_100	gpb0_1_0_100	anatop.ENET_REF_Clk97		
	G_P0_1_0_101	gpb0_1_0_101	anatop.ENET_REF_Clk98		
	G_P0_1_0_102	gpb0_1_0_102	anatop.ENET_REF_Clk99		
	G_P0_1_0_103	gpb0_1_0_103	anatop.ENET_REF_Clk100		
	G_P0_1_0_104	gpb0_1_0_104	anatop.ENET_REF_Clk101		
	G_P0_1_0_105	gpb0_1_0_105	anatop.ENET_REF_Clk102		
	G_P0_1_0_106	gpb0_1_0_106	anatop.ENET_REF_Clk103		
	G_P0_1_0_107	gpb0_1_0_107	anatop.ENET_REF_Clk104		
	G_P0_1_0_108	gpb0_1_0_108	anatop.ENET_REF_Clk105		
	G_P0_1_0_109	gpb0_1_0_109	anatop.ENET_REF_Clk106		
	G_P0_1_0_110	gpb0_1_0_110	anatop.ENET_REF_Clk107		
	G_P0_1_0_111	gpb0_1_0_111	anatop.ENET_REF_Clk108		
	G_P0_1_0_112	gpb0_1_0_112	anatop.ENET_REF_Clk109		
	G_P0_1_0_113	gpb0_1_0_113	anatop.ENET_REF_Clk110		
	G_P0_1_0_114	gpb0_1_0_114	anatop.ENET_REF_Clk111		
	G_P0_1_0_115	gpb0_1_0_115	anatop.ENET_REF_Clk112		
	G_P0_1_0_116	gpb0_1_0_116	anatop.ENET_REF_Clk113		
	G_P0_1_0_117	gpb0_1_0_117	anatop.ENET_REF_Clk114		
	G_P0_1_0_118	gpb0_1_0_118	anatop.ENET_REF_Clk115		
	G_P0_1_0_119	gpb0_1_0_119	anatop.ENET_REF_Clk116		
	G_P0_1_0_120	gpb0_1_0_120	anatop.ENET_REF_Clk117		
	G_P0_1_0_121	gpb0_1_0_121	anatop.ENET_REF_Clk118		
	G_P0_1_0_122	gpb0_1_0_122	anatop.ENET_REF_Clk119		
	G_P0_1_0_123	gpb0_1_0_123	anatop.ENET_REF_Clk120		
	G_P0_1_0_124	gpb0_1_0_124	anatop.ENET_REF_Clk121		
	G_P0_1_0_125	gpb0_1_0_125	anatop.ENET_REF_Clk122		
	G_P0_1_0_126	gpb0_1_0_126	anatop.ENET_REF_Clk123		
	G_P0_1_0_127	gpb0_1_0_127	anatop.ENET_REF_Clk124		
	G_P0_1_0_128	gpb0_1_0_128	anatop.ENET_REF_Clk125		
	G_P0_1_0_129	gpb0_1_0_129	anatop.ENET_REF_Clk126		
	G_P0_1_0_130	gpb0_1_0_130	anatop.ENET_REF_Clk127		
	G_P0_1_0_131	gpb0_1_0_131	anatop.ENET_REF_Clk128		
	G_P0_1_0_132	gpb0_1_0_132	anatop.ENET_REF_Clk129		
	G_P0_1_0_133	gpb0_1_0_133	anatop.ENET_REF_Clk130		
	G_P0_1_0_134	gpb0_1_0_134	anatop.ENET_REF_Clk131		
	G_P0_1_0_135	gpb0_1_0_135	anatop.ENET_REF_Clk132		
	G_P0_1_0_136	gpb0_1_0_136	anatop.ENET_REF_Clk133		
	G_P0_1_0_137	gpb0_1_0_137	anatop.ENET_REF_Clk134		
	G_P0_1_0_138	gpb0_1_0_138	anatop.ENET_REF_Clk135		
	G_P0_1_0_139	gpb0_1_0_139	anatop.ENET_REF_Clk136		
	G_P0_1_0_140	gpb0_1_0_140	anatop.ENET_REF_Clk137		
	G_P0_1_0_141	gpb0_1_0_141	anatop.ENET_REF_Clk138		
	G_P0_1_0_142	gpb0_1_0_142	anatop.ENET_REF_Clk139		
	G_P0_1_0_143	gpb0_1_0_143	anatop.ENET_REF_Clk140		
	G_P0_1_0_144	gpb0_1_0_144	anatop.ENET_REF_Clk141		
	G_P0_1_0_145	gpb0_1_0_145	anatop.ENET_REF_Clk142		
	G_P0_1_0_146	gpb0_1_0_146	anatop.ENET_REF_Clk143		
	G_P0_1_0_147	gpb0_1_0_147	anatop.ENET_REF_Clk144		
	G_P0_1_0_148	gpb0_1_0_148	anatop.ENET_REF_Clk145		
	G_P0_1_0_149	gpb0_1_0_149	anatop.ENET_REF_Clk146		
	G_P0_1_0_150	gpb0_1_0_150	anatop.ENET_REF_Clk147		
	G_P0_1_0_151	gpb0_1_0_151	anatop.ENET_REF_Clk148		
	G_P0_1_0_152	gpb0_1_0_152	anatop.ENET_REF_Clk149		
	G_P0_1_0_153	gpb0_1_0_153	anatop.ENET_REF_Clk150		
	G_P0_1_0_154	gpb0_1_0_154	anatop.ENET_REF_Clk151		
	G_P0_1_0_155	gpb0_1_0_155	anatop.ENET_REF_Clk152		
	G_P0_1_0_156	gpb0_1_0_156	anatop.ENET_REF_Clk153		
	G_P0_1_0_157	gpb0_1_0_157	anatop.ENET_REF_Clk154		
	G_P0_1_0_158	gpb0_1_0_158	anatop.ENET_REF_Clk155		
	G_P0_1_0_159	gpb0_1_0_159	anatop.ENET_REF_Clk156		
	G_P0_1_0_160	gpb0_1_0_160	anatop.ENET_REF_Clk157		
	G_P0_1_0_161	gpb0_1_0_161	anatop.ENET_REF_Clk158		
	G_P0_1_0_162				