(1)

ASSIGNMENT-1

VARTUL
E→316
19019201000316

(1) COA is the study of Internal working, structuring & implementation of computer system.

⇒ Computer Organization → It refers to the operational unit & their interaction that realize the architectural specification.

eg (i) Control Signal
(ii) Memory technology used.

⇒ Computer Architecture → It refers to those attribute of a system that have a direct impact on the logical execution of Program

eg (i) The Instruction set
(ii) No. of bits used to represent various data.

(2) $A^* B + A^* (B^* D + C^* E)$

$= A^* B + A^* (BD^* + CE^*)$

$= A^* B + A^* (BD^* CE^* +)$

$= AB^* + ABD^* CE^* + ^*$

$= AB^* ABD^* CE^* + ^* +$

(3) The arbitration is a mechanism which decides the selection of current master to access the bus.

Among several units that are connected to ~~same bus~~ a shared bus, it may happen that more than 1 unit may request to access the bus a same time. In such situation access to the bus is given to the master having highest priority. The 3 given mechanism commonly used for this are:-

(i) Daisy Chaining (ii) Parallel Arbitration

(iii) Independent priority

(4) (i) In this organization, the registers communicate with each other not only for direct data transfer, but also while performing various micro-operations.

(ii) Seven registers are used for general purpose, the O/P of each register is connected to two multiplexer (MUXs) I/P

(iii) Three select lines are used to select any of the seven registers & the contents of selected registers are supplied to the I/P's of ALU

(iv) The busses A & B are used to form the I/P to the common ALU

(v) The operation to be performed is selected in the ALU & is determined by the arithmetic or logical micro-operation by using function select lines

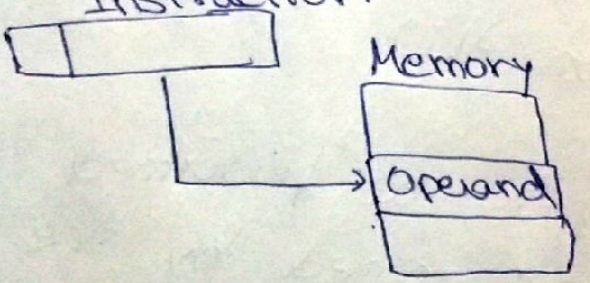
(vi) The result of the micro-operation is available as O/P data and also goes into the I/P of all the registers.

(vii) Any one of the destination registers receives the info. from O/P bus which is selected by decoder.

(6) (i) Direct => A very simple form of addressing is direct addressing, in which the addressing field contains the effective address of operand: EA = A where,

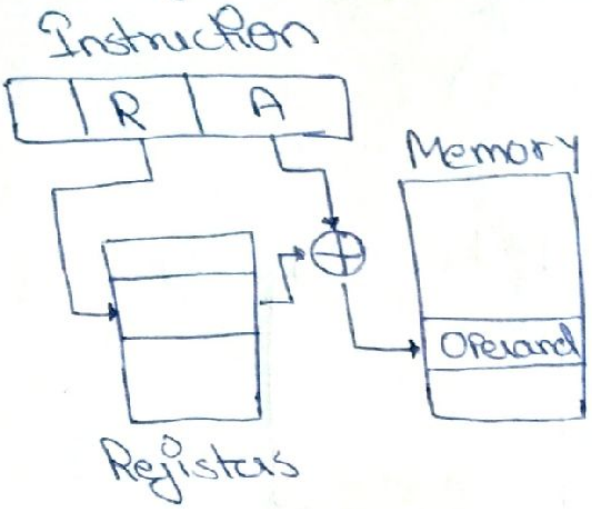
EA = Actual address of the location containing the referenced operand

A = Contents of the address field in the instruction



(ii) Displacement Addressing => A very powerful mode of addressing combines the capability of direct addressing & register indirect addressing. It is known by a variety of names depending upon the contents of its use but the basic mechanism is the same. Displacement addressing requires that

the Instruction have two address fields, atleast one of which is explicit.



(iii) Relative Addressing:- It means that the next instruction to be carried out is an offset number of locations away, relative to the address of the current instruction.

Consider this bit of pseudo code.

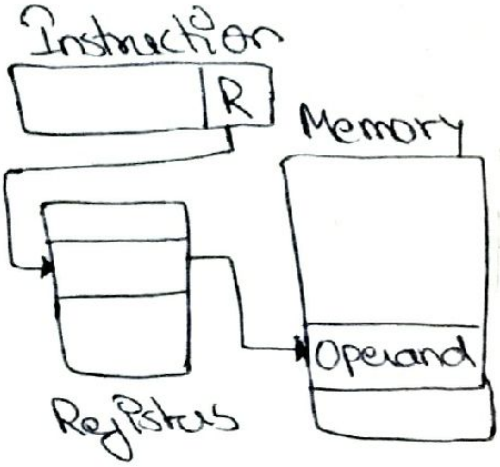
→ Jump + 3 if accumulator == 2
→ Code executed if accumulator is NOT = 2
→ Jump +5
→ acc:

In the code, the 1st line of code is checking to see if the accumulator has the value of 2 then the next Instruction is 3 line away

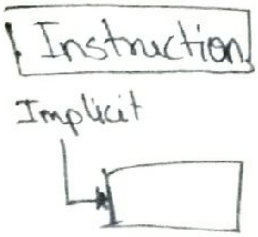
(iv) Register indirect mode :- Register indirect mode is similar to the indirect addressing. The

only diff. is whether the address field refers to a memory location or a register. Thus for register indirect address,

$$EA = (R)$$



(v) Implied mode :- In this mode, the operands are specified implicitly in the definition of the instruction. All register reference instructions that use an accumulator are implied mode instruction. Zero address instruction in a stack-organized computer are implied mode instruction since the operands are implied to be on top of the stack.



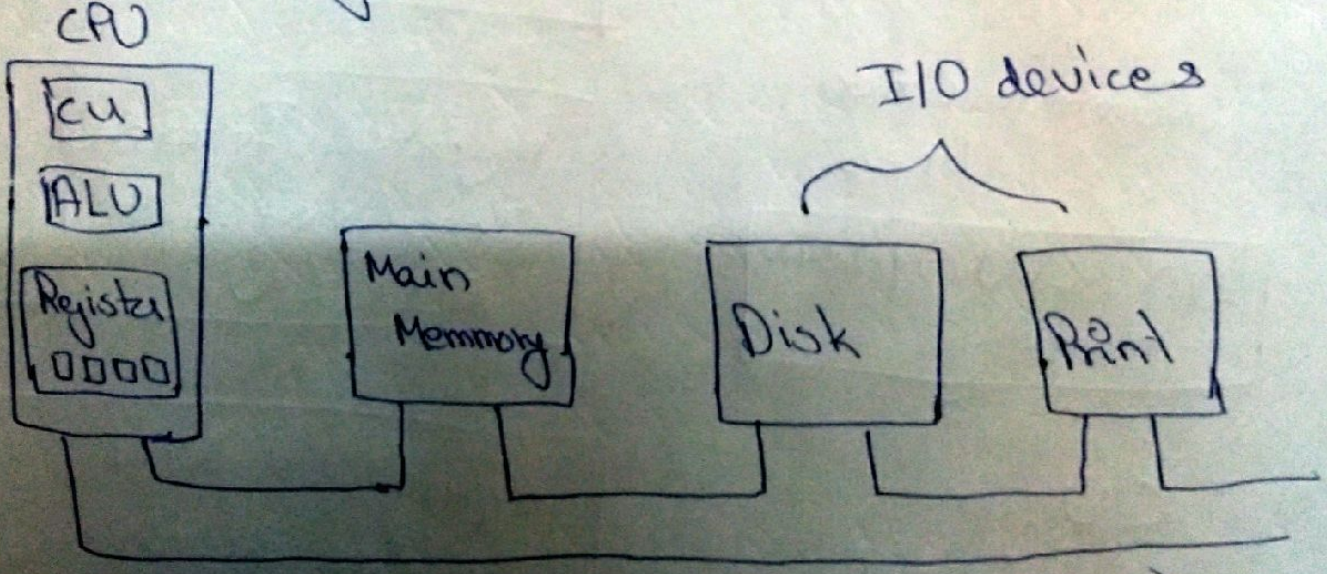
(vi) Immediate mode :- In this mode, the operand is specified in the instruction itself. The

operand field contains the actual operand to be used in conjunction with the operation specified in the instruction

Instruction

| Operand |

(5) A process must have three functional unit to be what we call a computer. A unit that perform all operation on data. A unit that which remains the data. A unit ~~where~~ which sequence the operation by ALU. "Process organization" is a term describing how these three elements are implemented & how they interconnect to accomplish 3 tasks.



(Processor Organization)

The major structural component of CPU

(i) Control Unit → Control the operation of CPU & hence the comp.

(ii) ALU → Perform computer data processing function.

(iii) Register → Provide storage Internal to the CPU

(iv) CPU → Interconnection, communication among the control unit, ALU & registers.

Peripheral
↓
Computer
↓
Communication lines

CPU, MM, System Interconnection, I/O

I/O, CPU, system memory

Register, Internal CPU Interconnection, ALU, CU

CU Structure

Sequential logic, Register decoder of CU, &