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IInd Year
CS

# ASSIGNMENT-1

## COMPUTER ARCHITECTURE & ORGANISATION

**Qus-1** What is computer Organisation & ~~Management~~ Architecture?

Computer Organization and architecture is the study of internal working, structuring and implementation of computer system

Computer Organisation refers to the operational unit and their interconnection that realize the architectural specification

Eg
- → control signal
- → memory technology used.

Computer Architecture refers those attributes of a system that have a direct impact on the logical execution of Program.

Eg
- → the instruction set
- → no of bit used to represent various data

**Qus-2** Discuss bus ~~abberation~~ Arbitration in detail?

The distributed arbitration process service all Processor request on the basic priority and hardware bus priority resolve the technique which can establish by requesting control signal

Bus arbitration is process for acknowledgement of priority to system bus and processor or Peripheral devices.

There are two type of Bus.

(a) Centralised or Serial Arbitration.

(b) Distributed or Parallel Arbitration

CENTRALISED ARBITRATION:

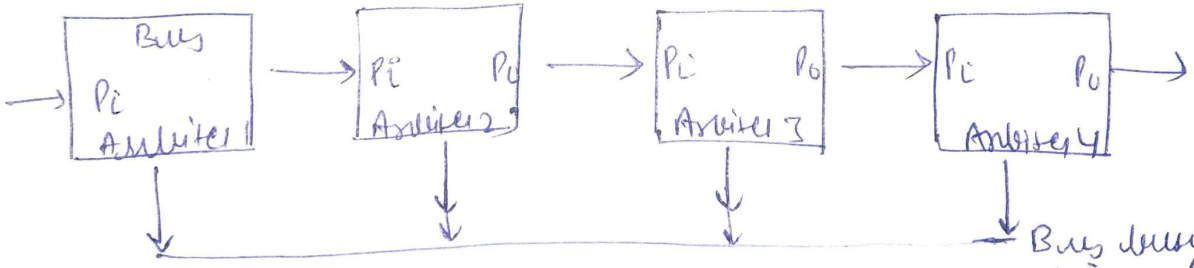
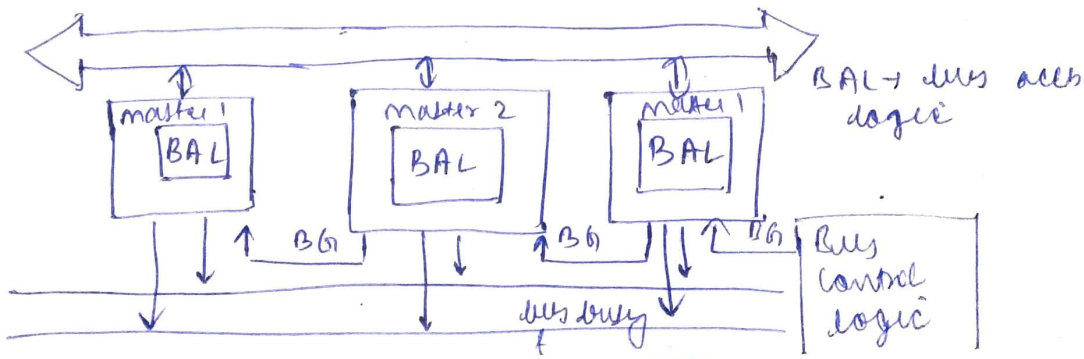



Fig - Serial Arbitration  Pi → Priority input
Po → Priority output

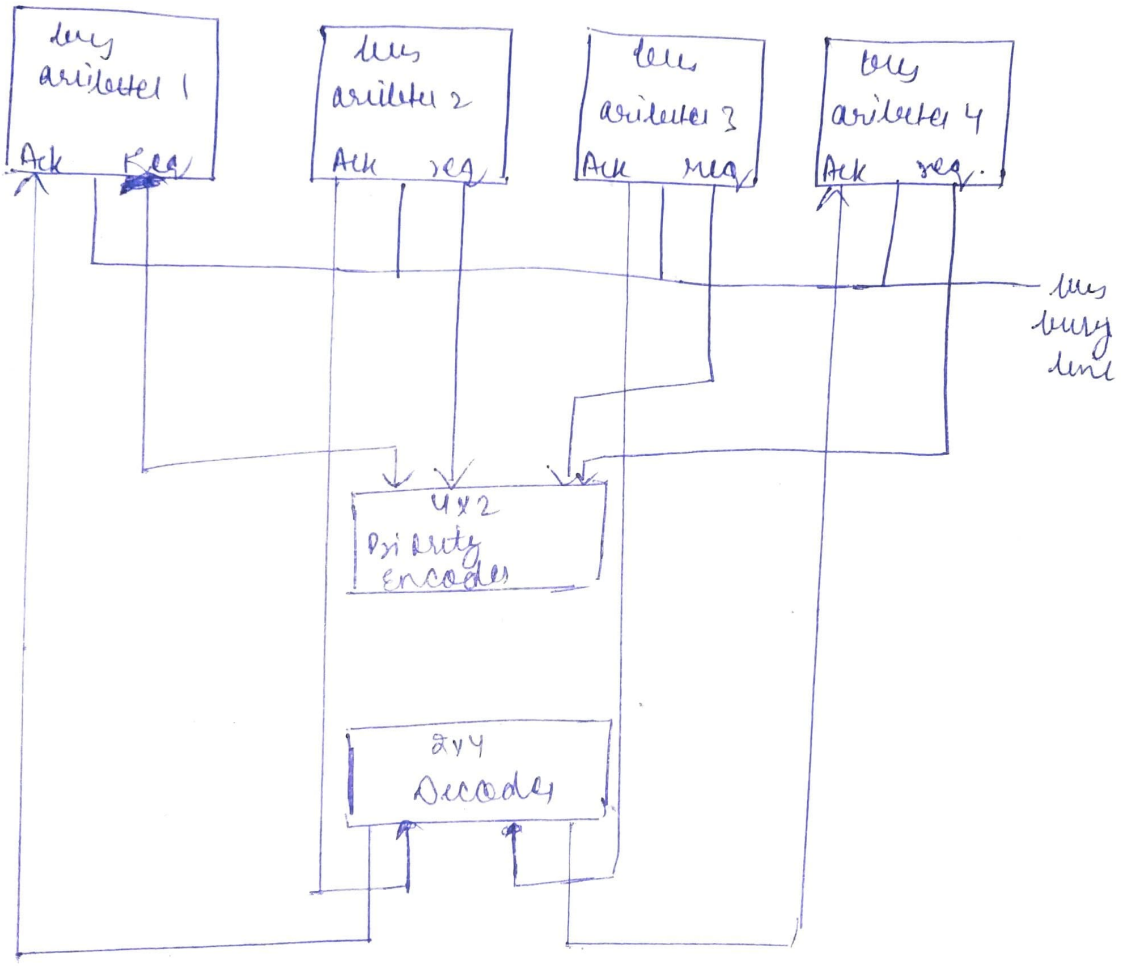


The Processor Organization is a term describing how these elements are interconnected and how they interconnect to the above dia, show the serial arbitration. also called daisy chain method. In the diagram, there are four Processors $P_1$, $P_2$, $P_3$ & $P_4$ in series. which are also connected to system bus the Priority is fixed for every Processor. In this diagram, $P_1$ has highest Priority and $P_4$ has lowest Priority. there are 2 types of signals put on every Processor.

Pi and Po, Pi ~~for~~ is connected to logical and Po for each Processes is connected to the Pi for further Processor.

PARALLEL ARIBATION: In parallel bus arbitration technique use an external method encode and decoder (Priority decoder) each bus arbiter in the Parallel scheme has a bus request output line and bus acknowledge input line.

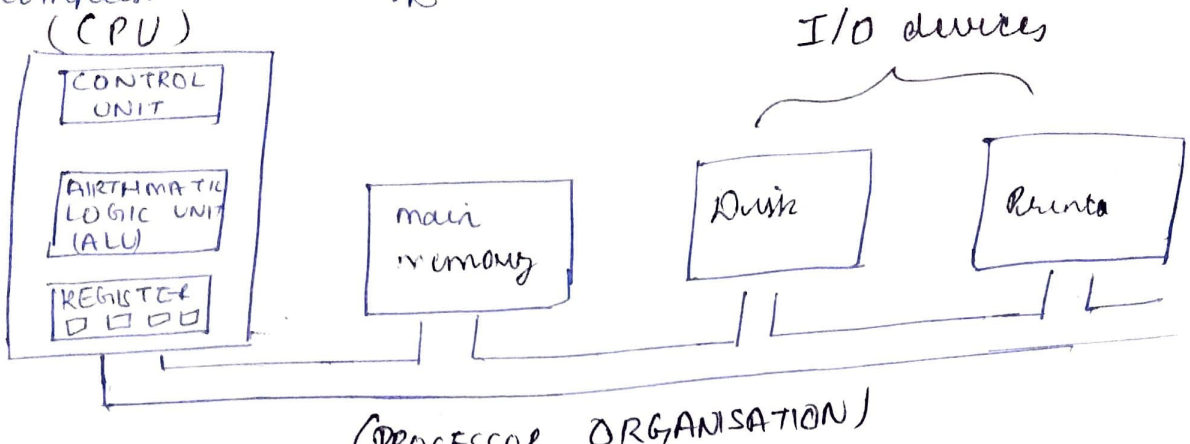
Each arbiter enable the request line when its Processor is requesting access to the system bus. The Processor take control of the bus if its acknowledge input line is enable




Ans:- Explain Processor Organization.

A Processor must have three functional unit to be what we call a computer. A unit that perform ALU Operation on data. A unit that which remembers the data. (memory). A unit which sequence the Operation by ALU (control unit)

(5) "Processor Organization" is a term describing how those three elements are implemented and how they interconnect to accomplish these task




(PROCESSOR ORGANISATION)

The major structural component of CPU.

(1) Control unit: control the operation of CPU & hence the comp.
(2) ALU: Perfes computer data Processing Function
(3) Register ... Provide storage Internal to the CPU.
(4) CPU interconnection communication among the control unit, ALU, & Register

Peripheral

↓

computer

↓

communication lines

I/O, CPU, system, memory

CPU, mm, system interconnection, I/O

Register, Internal CPU interconnection, ALU, Control unit

sequential logic, Register decoder of CU, control memory

CONTROL UNIT STRUCTURE

Que-4 What is stack & how registers are organized using stack?

A stack is a storage structure that store the info in such a way that the last info stored retrive first (LIFO)

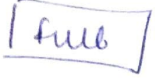
→ It is useful feature included in CPU

→ Item stored first is the last to be retrieve

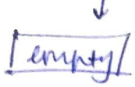
→ two operation push (insert to stack) and pop (delete from stack)

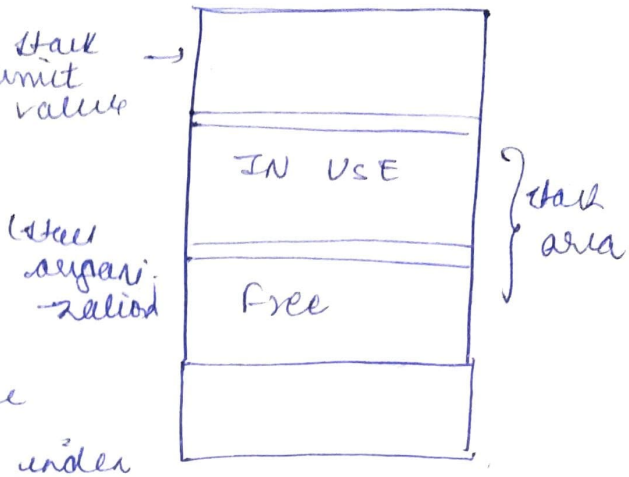
→ Register that hold the adress of the stack called stack Pointer (SP)

Full = 1 when stack is full

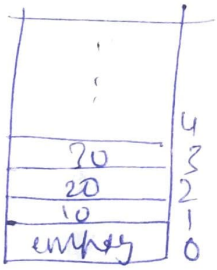



Empty = 1 when stack is empty




In register stack we insert the digit 10, 20, 30 and the initial index of stack is empty. In register stack it store the register except initial box of stack is always empty

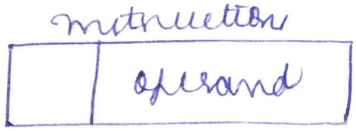



Que-5 What is addressing mode? Explain different type with diagram.

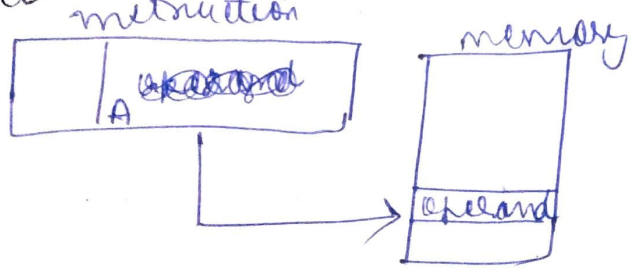
The different kind of ways the Programmer can refer to data stored in memory is known as addressing mode.

most common addressing modes are :-

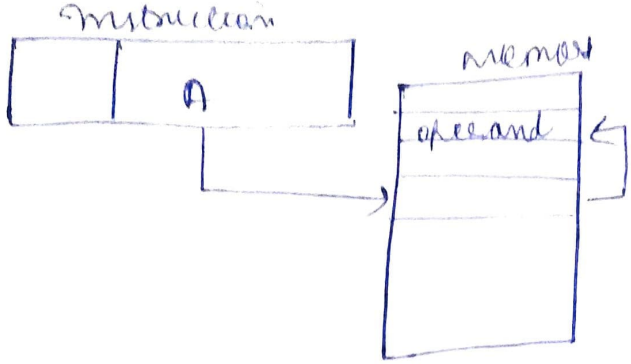
1) Immediate



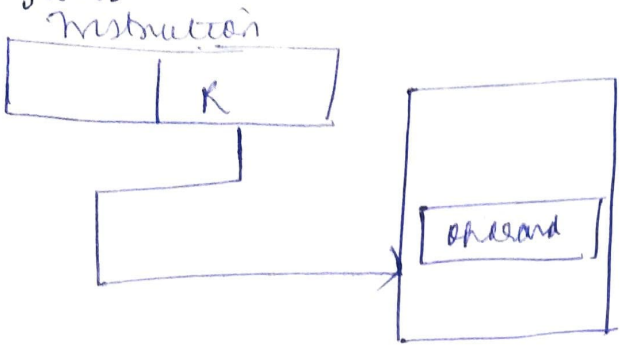

2) Direct



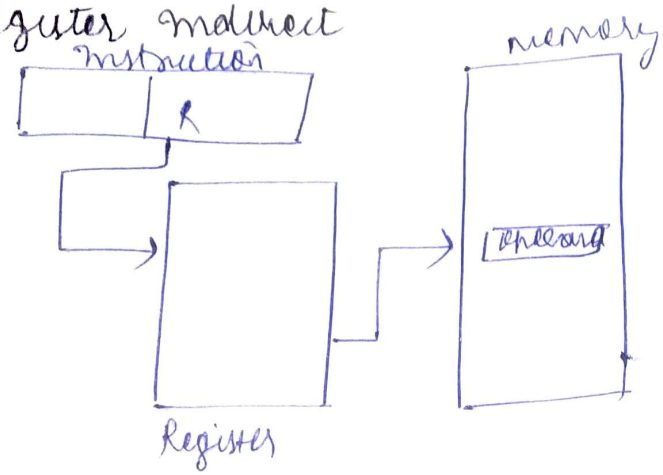
④ Indirect



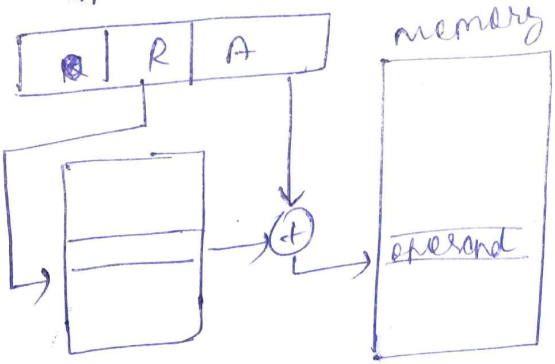

⑨ Register




⑤ Register indirect



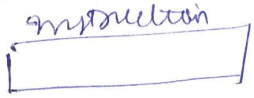

⑥ Displacement




A → content of an address field in the instruction.

R → content of an address field in the instruction that refers to a register.

⑦ ~~Reference~~ Stack




implicit

Top of stack Register.

Ques 6 Solve this expression using zero adress instruction f

(156 * 25) + [30 * (35 + 20)]

| | |
|---|---|
| Push 156 | TOS ← 156 |
| Push 25 | TOS ← 25 |
| MUL | TOS ← 156 x 25 = 3900 |
| PUSH 30 | TOS ← 30 |
| PUSH 35 | TOS ← 35 |
| Push 20 | TOS ← 25 |
| Add | TOS ← 55 |
| Mul | TOS ← 55 x 30 = 1650 |
| Add | TOS ← 1650 + 3900 |

Ans = 5550