

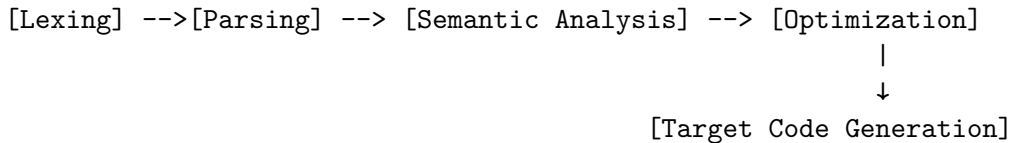
50.054 Code Generation (Stack Machine)

ISTD, SUTD

Learning Outcomes

1. Name the difference among the target code platforms
2. Implement the target code generation to JVM bytecode given a Pseudo Assembly Program

Recap Compiler Pipeline



- ▶ Target Code Generation
 - ▶ Input: some IR as input
 - ▶ Output: the target code (executable)

Instruction Selection

- ▶ 3-address instruction
 - ▶ RISC (Reduced Instruction Set Computer) architecture. E.g. Apple PowerPC, ARM, Pseudo Assembly
- ▶ 2-address instruction
 - ▶ CISC (Complex Instruction Set Computer) architecture. E.g. Intel x86
- ▶ 1-address instruction
 - ▶ Stack machine. E.g. JVM

Assembly code vs Machine code

- ▶ The actual target codes are in binary (Machine code).
- ▶ The assembly codes in human readable representation of the Machine code.

Assembly Language

Machine Language

```
mov ecx, ebx  
mov esp, edx  
mov edx, r9d  
mov rax, rdx
```

Assembler + Linker

```
100101011001  
010011111011  
111010101101  
01010101010
```

Programmer

Processor

3-address instruction

- ▶ `dst <- src1 op src2`
- ▶ Simple instruction set
- ▶ More registers (and temp variables)

```
x <- 1  
y <- 2  
r <- x + y
```

or

```
load x 1  
load y 2  
add r x y
```

2-address instruction

- ▶ op dst src
- ▶ More complex instruction set
- ▶ Fewer registers

load x 1

load y 2

add x y

- ▶ r is the same as x

1-address instruction

- ▶ AKA P-code, stack machine code
- ▶ More complex instruction set with stack for computation (not to confuse with stack for function call)
- ▶ Minimum registers, e.g. JVM has only 3 registers.

```
push 1  
push 2  
add  
store r
```


JVM bytecode (reduced set)

(JVM Instructions) $jis ::= [] \mid ji \ jis$
(JVM Instruction) $ji ::= ilabel \ l \mid iload \ n \mid istore \ n \mid iadd \mid isub \mid imul$
 $\mid if_icmpge \ l \mid if_icmpne \ l \mid igoto \ l \mid sipush \ c \mid ireturn$
(JVM local vars) $n ::= 1 \mid 2 \mid \dots$
(constant) $c ::= -32768 \mid \dots \mid 0 \mid \dots \mid 32767$

1. a register for the first operand and result
2. a register for the second operand
3. a register for controlling the state of the stack operation (we can't use it.)

An Example

// PA1

1: x <- input

2: s <- 0

3: c <- 0

4: b <- c < x

5: ifn b goto 9

6: s <- c + s

7: c <- c + 1

8: goto 4

9: _ret_r <- s

10: ret

► PA variables to JVM variables

► input to 1,

► x to 2,

► s to 3,

► c to 4

► and b to 5

► PA labels to JVM labels

► 4 to l1

► 9 to l2

iload 1 *// push the content of input to r0*

istore 2 *// pop r0's content to x,*

sipush 0 *// push the value 0 to r0*

istore 3 *// pop r0 to s*

sipush 0 *// push the value 0 to r0*

istore 4 *// pop r0 to c*

ilabel l1 *// mark label l1*

iload 4 *// push the content of c to r0*

iload 2 *// push the content of x to r1*

if_icmpge l2 *// if r0 >= r1 jump,*

// pop both r0 r1

iload 4 *// push the content of c to r0*

iload 3 *// push the content of s to r1*

iadd *// sum up r0 and r1 and result in r0*

istore 3 *// pop r0 to s*

iload 4 *// push the content of c to r0*

sipush 1 *// push a constant 1 to r1*

iadd

istore 4 *// pop r0 to c*

igoto l1

ilabel l2

iload 3 *// push the content of s to r0*

ireturn

Operational Semantics of JVM

$$\begin{array}{lll} \text{(JVM Program)} & J & \subseteq \textit{jis} \\ \text{(JVM Environment)} & \Delta & \subseteq n \times c \\ \text{(JVM Stack)} & S & = _, _ \mid c, _ \mid c, c \end{array}$$

Small step operational semantics

$$J \vdash (\Delta, S, \textit{jis}) \longrightarrow (\Delta', S', \textit{jis}')$$

Operational Semantics of JVM

$$(sjLoad1) \quad J \vdash (\Delta, _, _, \text{iload } n; jis) \longrightarrow (\Delta, \Delta(n), _, jis)$$

$$(sjLoad2) \quad J \vdash (\Delta, c, _, \text{iload } n; jis) \longrightarrow (\Delta, c, \Delta(n), jis)$$

$$(sjPush1) \quad J \vdash (\Delta, _, _, \text{sipush } c; jis) \longrightarrow (\Delta, c, _, jis)$$

$$(sjPush2) \quad J \vdash (\Delta, c_0, _, \text{sipush } c_1; jis) \longrightarrow (\Delta, c_0, c_1, jis)$$

$$(sjLabel) \quad J \vdash (\Delta, r_0, r_1, \text{ilabel } l; jis) \longrightarrow (\Delta, r_0, r_1, jis)$$

$$(sjStore) \quad J \vdash (\Delta, c, _, \text{istore } n; jis) \longrightarrow (\Delta \oplus (n, c), _, _, jis)$$

$$(sjAdd) \quad J \vdash (\Delta, c_0, c_1, \text{iadd}; jis) \longrightarrow (\Delta, c_0 + c_1, _, jis)$$

$$(sjGoto) \quad J \vdash (\Delta, r_0, r_1, \text{igoto } l'; jis) \longrightarrow (\Delta, r_0, r_1, \text{codeAfterLabel}(J, l'))$$

$$(sjCmpNE1) \quad \frac{c_0 \neq c_1 \quad jis' = \text{codeAfterLabel}(J, l')}{J \vdash (\Delta, c_0, c_1, \text{if_icmpne } l'; jis) \longrightarrow (\Delta, _, _, jis')}$$

$$(sjCmpNE2) \quad \frac{c_0 = c_1}{J \vdash (\Delta, c_0, c_1, \text{if_icmpne } l'; jis) \longrightarrow (\Delta, _, _, jis')}$$

Operational Semantics of JVM

$$\begin{aligned} \text{codeAfterLabel}(\text{ireturn}, l) &= \text{error} \\ \text{codeAfterLabel}(\text{ilabel } l; jis, l') &= \begin{cases} jis & l == l' \\ \text{codeAfterLabel}(jis, l') & \text{otherwise} \end{cases} \\ \text{codeAfterLabel}(ji; jis, l) &= \text{codeAfterLabel}(jis, l) \end{aligned}$$

From PA to JVM

- ▶ M - a mapping from PA temporary variables to JVM local variables.
- ▶ L - a mapping from PA labels (which are used as the targets in some jump instructions) to JVM labels.
- ▶ We have three types of rules.
 - ▶ $M, L \vdash lis \Rightarrow jis$
 - ▶ $M \vdash s \Rightarrow jis$
 - ▶ $L \vdash l \Rightarrow jis$

From PA to JVM

Converting PA operands

$$(jConst) \quad M \vdash c \Rightarrow [sipush \ c]$$

$$(jVar) \quad M \vdash t \Rightarrow [iload \ M(t)]$$

Converting PA Labels

$$(jLabel1) \quad \frac{I \notin L}{L \vdash I \Rightarrow []}$$

$$(jLabel2) \quad \frac{I \in L}{L \vdash I \Rightarrow [ilabel \ I]}$$

From PA to JVM

$$(\text{jMove}) \quad \frac{L \vdash l \Rightarrow jis_0 \quad M \vdash s \Rightarrow jis_1 \quad M, L \vdash lis \Rightarrow jis_2}{M, L \vdash l : t \leftarrow s; lis \Rightarrow jis_0 + jis_1 + [\text{istore } M(t)] + jis_2}$$

// PA1

1: x <- input

2: s <- 0

3: c <- 0

...

▶ $M = \{(input, 1), (x, 2), (s, 3), (c, 4), (b, 5)\}$

▶ $L = \{(4, l1), (9, l2)\}$

iload 1 // push the content of input to r0

istore 2 // pop r0's content to x,

sipush 0 // push the value 0 to r0

istore 3 // pop r0 to s

sipush 0 // push the value 0 to r0

istore 4 // pop r0 to c

...

From PA to JVM

$$(jEq) \frac{L \vdash l_1 \Rightarrow jis_0 \quad M \vdash s_1 \Rightarrow jis_1 \quad M \vdash s_2 \Rightarrow jis_2 \quad M, L \vdash lis \Rightarrow jis_3}{M, L \vdash l_1 : t \leftarrow s_1 == s_2; l_2 : \text{ifn } t \text{ goto } l_3; lis \Rightarrow jis_0 + jis_1 + jis_2 + [\text{if_icmpne } L(l_3)] + jis_3}$$

$$(jLThan) \frac{L \vdash l_1 \Rightarrow jis_0 \quad M \vdash s_1 \Rightarrow jis_1 \quad M \vdash s_2 \Rightarrow jis_2 \quad M, L \vdash lis \Rightarrow jis_3}{M, L \vdash l_1 : t \leftarrow s_1 < s_2; l_2 : \text{ifn } t \text{ goto } l_3; lis \Rightarrow jis_0 + jis_1 + jis_2 + [\text{if_icmpge } L(l_3)] + jis_3}$$

// PA1

...

4: b <- c < x

5: ifn b goto 9

...

► $M = \{(input, 1), (x, 2), (s, 3), (c, 4), (b, 5)\}$

► $L = \{(4, l1), (9, l2)\}$

...

ilabel l1 // mark label l1

iload 4 // push the content of c to r0

iload 2 // push the content of x to r1

if_icmpge l2 // if r0 >= r1 jump,
// pop both r0 r1

...

From PA to JVM

$$\begin{array}{l} \text{(jAdd)} \quad \frac{L \vdash I \Rightarrow jis_0 \quad M \vdash s_1 \Rightarrow jis_1 \quad M \vdash s_2 \Rightarrow jis_2 \quad M, L \vdash lis \Rightarrow jis_3}{M, L \vdash I : t \leftarrow s_1 + s_2; lis \Rightarrow jis_0 + jis_1 + jis_2 + [iadd, istore M(t)] + jis_3} \\ \text{(jSub)} \quad \frac{L \vdash I \Rightarrow jis_0 \quad M \vdash s_1 \Rightarrow jis_1 \quad M \vdash s_2 \Rightarrow jis_2 \quad M, L \vdash lis \Rightarrow jis_3}{M, L \vdash I : t \leftarrow s_1 - s_2; lis \Rightarrow jis_0 + jis_1 + jis_2 + [isub, istore M(t)] + jis_3} \\ \text{(jMul)} \quad \frac{L \vdash I \Rightarrow jis_0 \quad M \vdash s_1 \Rightarrow jis_1 \quad M \vdash s_2 \Rightarrow jis_2 \quad M, L \vdash lis \Rightarrow jis_3}{M, L \vdash I : t \leftarrow s_1 * s_2; lis \Rightarrow jis_0 + jis_1 + jis_2 + [imul, istore M(t)] + jis_3} \end{array}$$

// PA1

...

6: s <- c + s

7: c <- c + 1

...

► $M = \{(input, 1), (x, 2), (s, 3), (c, 4), (b, 5)\}$

► $L = \{(4, l1), (9, l2)\}$

...

iload 4 // push the content of c to r0

iload 3 // push the content of s to r1

iadd // sum up r0 and r1 and result in r0

istore 3 // pop r0 to s

iload 4 // push the content of c to r0

sipush 1 // push a constant 1 to r1

iadd

istore 4 // pop r0 to c

...

From PA to JVM

$$\begin{array}{l} \text{(jGoto)} \quad \frac{L \vdash l_1 \Rightarrow jis_0 \quad M, L \vdash lis \Rightarrow jis_1}{M, L \vdash l_1 : goto\ l_2; lis \Rightarrow jis_0 + [igoto\ l_2] + jis_1} \\ \text{(jReturn)} \quad \frac{L \vdash l_1 \Rightarrow jis_0 \quad M \vdash s \Rightarrow jis_1}{M, L \vdash l_1 : rret \leftarrow s; l_2 : ret \Rightarrow jis_0 + jis_1 + [ireturn]} \end{array}$$

// PA1

...

8: goto 4

9: _ret_r <- s

10: ret

► $M = \{(input, 1), (x, 2), (s, 3), (c, 4), (b, 5)\}$

► $L = \{(4, l1), (9, l2)\}$

...

igoto l1

ilabel l2

iload 3 // push the content of s to r0

ireturn

Bytecode Optimization

SIMP

$r = (1 + 2) * 3$

PA

1: $t \leftarrow 1 + 2$

2: $r \leftarrow t * 3$

sipush 1

sipush 2

iadd

istore 2 *// 2 is t*

iload 2

sipush 3

imul

istore 3 *// 3 is r*

Bytecode Optimization

SIMP

$r = (1 + 2) * 3$

PA

1: $t \leftarrow 1 + 2$

2: $r \leftarrow t * 3$

We could apply

1. Liveness analysis on PA level or
2. Generate JVM byte code directly from SIMP.
 - This requires the expression of SIMP assignment to be left nested.

sipush 1

sipush 2

iadd

sipush 3

imul

istore 3 *// 3 is r*