

Please check that this question paper contains 9 questions and 2 printed pages within first ten

[Total No. of Questions: 09]

Uni. Roll No. ....

[Total No. of Pages: ..2....]

Program: .....B.Tech.....

Semester:.....3.....

Name of Subject: Digital Circuits and Logic Design

Subject Code: ...ESIT-101.....

Paper ID: ...16042...

**Time Allowed: 02 Hours**

**Max. Marks: 60**

**NOTE:**

- 1) Each question is of 10 marks.
- 2) Attempt any six questions out of nine
- 3) Any missing data may be assumed appropriately

07-01-2022(M)

- 1) Simplify following expressions using Boolean algebra

a)  $F(P,Q,R)=P'Q+QR'+QR+PQ'R'$

b)  $F(X,Y,Z)=X'Y'Z'+X'YZ'+X'YZ+XYZ'$

- 2) Design 1 bit full adder using Multiplexer.

- 3) Provide minimized SOP expression for the following K-Map

|   |   |   |   |
|---|---|---|---|
| 1 | 0 | 0 | 1 |
| 0 | d | 0 | 0 |
| 0 | 0 | d | 1 |
| 1 | 0 | 0 | 1 |

- 4) Convert following:

a)  $(331)_8 = ( )_{16} = ( )_{10}$

b)  $(11001010)_2 = ( )_{\text{Gray code}}$

c)  $(111)_2 = ( )_{\text{BCD}}$

d)  $(1101)_2 + (1110)_2 = ( )_8$

**5) Design 3 bit Synchronous Down Counter.**

**6) Simplify K-Map**

|    |    | ab | 00 | 01 | 11           | 10 |
|----|----|----|----|----|--------------|----|
|    |    | cd | 00 | 01 | 11           | 10 |
| 00 | 01 | 00 | 1  | X  | X            | 1  |
|    |    | 01 | X  |    |              | 1  |
| 11 |    | 11 |    |    |              |    |
| 10 |    | 10 | 1  |    | ExamSide.Com | X  |

**7) What are various techniques to convert Analog to Digital signals? Explain any one in detail.**

**8) Prove the following using Boolean algebra:**

a)  $PQ + P'R + QR = PQ + P'R$

b)  $XY + X'Z = (X+Z)(X'+Y)$

**9) a) Explain working of Even parity generator with circuit diagram.**

**b) Why gray codes are used in K-Maps. Explain in detail.**

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Uni. Roll No. ....

04 DEC 2019

EVENING

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Program/ Course: B.Tech. (Sem. 3<sup>rd</sup>)  
Name of Subject: Digital Circuits and Logic Design  
Subject Code: ESIT-101  
Paper ID: 1133

Time Allowed: 3 Hours

Max. Marks: 60

NOTE:

- 1) **Parts A and B are Compulsory**
- 2) **Part C has Two Questions Q8 and Q9. Both are compulsory, but with internal choice.**
- 3) Any missing data may be assumed appropriately.

**Part - A**

[Marks: 02 each]

**Q1.**

- a) Convert  $(11101)_2$  into decimal and  $(25)_8$  into binary.
- b) List the pros and cons of BCD code.
- c) Differentiate between Latch and Flip-flop?
- d) What Is Race-around problem? How can it be rectified?
- e) Why collector resistor is a significant component in RTL?
- f) A 6 bit R-2R ladder D/A converter has reference voltage of 6.5V. Find i) Resolution  
ii) Full Scale Voltage.

**Part - B**

[Marks: 04 each]

- Q2.** Explain the basic types of Logic Gates along with their block diagrams and truth tables.
- Q3.** Design a full adder with logical expression for sum and carry.
- Q4.** How does SR Flip Flop works?
- Q5.** Minimize the following function using K map.  $f(A,B,C,D) = \Sigma m(3,4,5,7,9,13,14,15)$
- Q6.** Distinguish between DMUX and MUX. Design a 4:1 Multiplexer.
- Q7.** Write a program in VHDL to design an AND gate.

Q8. Distinguish between a) Level and Edge Triggering b) Combinational and sequential circuits. c ) Mealy and Moore Machine d) Decoder and Demultiplexer.

OR

Simplify the following function  $f(A,B,C,D) = \sum m(2,6,8,9,10,11,14,15)$  using Quine-McCluskey (QM) tabular method.

Q9. Distinguish between synchronous and asynchronous counter. Design a MOD 6 asynchronous counter.

OR

Explain with the help of block diagram working of Successive Approximation A/D Converter. You have to provide some analog voltage and derive the equivalent digital form for it. Also list the various applications of A/D and D/A Converters.

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Uni. Roll No. ....

Program: B.Tech. (Batch 2018 onward)

MORNING

Semester: 3<sup>rd</sup>

27 DEC 2022

Name of Subject: Digital Circuits and Logic Design

Subject Code: ESIT-101

Paper ID: 16042

**Time Allowed: 03 Hours**

**Max. Marks: 60**

**NOTE:**

- 1) Parts A and B are compulsory
- 2) Part-C has Two Questions Q8 and Q9. Both are compulsory, but with internal choice
- 3) Any missing data may be assumed appropriately

**Part – A**

**[Marks: 02 each]**

**Q1.**

- a) Define 1's complement and 2's complement.
- b) What are the various uses of VHDL?
- c) Illustrate the advantages of Ring Counter.
- d) Write a short note on SOP and POS.
- e) Convert  $(10101)_2$  to decimal.
- f) Compare encoder and decoder.

**Part – B**

**[Marks: 04 each]**

**Q2.** State and prove De-Morgan's Theorem.

**Q3.** What are universal gates? Realize the following gates using universal gates:

- a. AND
- b. EX-NOR

**Q4.** Illustrate the working of Master Slave J-K flip flop.

**Q5.** Reduce the following Boolean expression:  $x'y'z + y'z + xz$ .

**Q6.** What is full subtractor? Draw a full subtractor circuit.

**Q7.** Explain the working of Gray code. Write its importance and its uses.

**Part – C**

**[Marks: 12 each]**

**Q8.** Write short note on following:

- a. RTL logic family **(6 marks)**
- b. R-2R Ladder **(6 marks)**

**OR**

Design an  $8 \times 1$  multiplexer using  $4 \times 1$  and  $2 \times 1$  multiplexer.

**Q9.** Design 2-bit Synchronous Up counter using JK flip flop.

**OR**

Minimize the following Boolean function-

$$F(A, B, C, D) = \Sigma m(1, 3, 4, 6, 8, 9, 11, 13, 15) + \Sigma d(0, 2, 14)$$

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Uni. Roll No. ....

Program: B.Tech. (Batch 2018 onward)

Semester: 3

Name of Subject: Digital Circuits and Logic Design

Subject Code: ESIT-101

Paper ID: 16042

Time Allowed: 03 Hours

Max. Marks: 60

**NOTE:**

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**Part – A**

[Marks: 02 each]

**Q1.**

- a) What is De-Morgan's Theorem? (LOTS)
- b) What is decoder? Compare decoder and demultiplexer with suitable block diagram. (LOTS)
- c) Explain the term resolution and accuracy of A/D convertors. (LOTS)
- d) What is the difference between a latch and a flip flop. (LOTS)
- e) Perform Subtraction using 2's Complement:  $(101001)_2 - (001100)_2$  (HOTS)
- f) Add the following decimal numbers using BCD Addition and verify your result: 599 and 984 (HOTS)

**Part – B**

[Marks: 04 each]

**Q2.** Minimize the following expressions using Boolean algebra: (LOTS)

- 1)  $A'B'C + A'B'C' + ABC + ABC'$
- 2)  $(ABC)'(A + C)(A + C')$

**Q3.** Implement full adder using two half adders and one OR gate. (LOTS)

**Q4.** What is Race around condition? How it can be avoided? Also discuss the working of Master Slave J-K Flip Flop. (LOTS)

**Q5.** Explain the working of 3-bit shift register. (HOTS)

**Q6.** Design 4-to-16 decoder with 2-to-4 decoder. (HOTS)

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Q7. Draw the circuit of BCD adder and explain it. (HOTS)

**Part – C**

[Marks: 12 each]

Q8. Simplify the minterm expression for  $F : F(P,Q,R,S) = \sum (0,2,5,7,8,10,13,15)$  using K-Map. The minterms 2, 7, 8 and 13 are 'do not care' terms. (LOTS)

OR

What are universal gates and why they are called so? Implement AND, OR, NOT and XOR gates using NAND gates. (LOTS)

Q9. Design a combinational circuit to implement a 4-bit Binary to Gray code convertor. (HOTS)

OR

Differentiate between synchronous and asynchronous counters. Design 3-bit synchronous up counter using T flip flops. (HOTS)

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Uni. Roll No. ....

Program: B.Tech. (Batch 2018 onward)

MORNING

Semester: 3<sup>rd</sup>

27 DEC 2022

Name of Subject: Digital Circuits and Logic Design

Subject Code: ESIT-101

Paper ID: 16042

**Time Allowed: 03 Hours**

**Max. Marks: 60**

**NOTE:**

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**Part – A**

**[Marks: 02 each]**

**Q1.**

- a) Define 1's complement and 2's complement.
- b) What are the various uses of VHDL?
- c) Illustrate the advantages of Ring Counter.
- d) Write a short note on SOP and POS.
- e) Convert  $(10101)_2$  to decimal.
- f) Compare encoder and decoder.

**Part – B**

**[Marks: 04 each]**

**Q2.** State and prove De-Morgan's Theorem.

**Q3.** What are universal gates? Realize the following gates using universal gates:

- a. AND
- b. EX-NOR

**Q4.** Illustrate the working of Master Slave J-K flip flop.

**Q5.** Reduce the following Boolean expression:  $x'y'z + y'z + xz$ .

**Q6.** What is full subtractor? Draw a full subtractor circuit.

**Q7.** Explain the working of Gray code. Write its importance and its uses.

**Part – C**

**[Marks: 12 each]**

**Q8.** Write short note on following:

- a. RTL logic family **(6 marks)**
- b. R-2R Ladder **(6 marks)**

**OR**

Design an  $8 \times 1$  multiplexer using  $4 \times 1$  and  $2 \times 1$  multiplexer.

**Q9.** Design 2-bit Synchronous Up counter using JK flip flop.

**OR**

Minimize the following Boolean function-

$$F(A, B, C, D) = \Sigma m(1, 3, 4, 6, 8, 9, 11, 13, 15) + \Sigma d(0, 2, 14)$$

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Uni. Roll No. ....

Program: B.Tech. (Batch 2018 onward)

Semester: 3rd

Name of Subject: Digital Circuits and Logic Design

Subject Code: ESIT-101

Paper ID: 16042

Scientific calculator is Allowed

**Time Allowed: 03 Hours**

**Max. Marks: 60**

**NOTE:**

- 1) Parts A and B are compulsory
- 2) Part-C has Two Questions Q8 and Q9. Both are compulsory, but with internal choice
- 3) Any missing data may be assumed appropriately

**Part – A**

**[Marks: 02 each]**

**Q1.**

- Q1. a) What are ASCII codes.  
b) What is 2's complement of  $(111011)_2$ .  
c) Differentiate between Flip flop and Register.  
d) What is the need for VHDL.  
e) State and prove De Morgan's theorem.  
f) Give the use of half adder.

**Part – B**

**[Marks: 04 each]**

Q2) K-Map follows Gray coding scheme. Explain why?

Q3) Convert the following:

- a)  $(331)_8 = ( )_{16} = ( )_{10}$
- b)  $(11001010)_2 = ( )_{\text{Gray code}}$
- c)  $(111)_2 = ( )_{\text{BCD}}$
- d)  $(1101)_2 + (1110)_2 = ( )_8$

Q4) Simplify following expressions using Boolean algebra

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a)  $F(P,Q,R)=P'Q+QR'+QR+PQ'R'$

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b)  $F(X,Y,Z)=X'Y'Z'+X'YZ'+X'YZ+XYZ'$

Q5) What are Sum of Products and Product of Sum terms in digital circuits? Explain in detail.

Q6) Using Universal gates, create following gates

- a) XOR      b) AND

Q7) Design 4:2 Encoder circuit with truth table and circuit diagram.

**Part - C**

[Marks: 12 each]

Q8) Design 3 bit Synchronous Up Counter.

OR

Simplify the given K-Map

|  |    | ab | 00 | 01 | 11 | 10 |
|--|----|----|----|----|----|----|
|  |    | cd | 00 | 01 | 11 | 10 |
|  | 00 |    | 1  | X  | X  | 1  |
|  | 01 |    | X  |    |    | 1  |
|  | 11 |    |    |    |    |    |
|  | 10 |    | 1  |    |    | X  |

Q9) Explain Successive approximation Analog to Digital convertor in detail.

OR

Demonstrate the working of Master Slave flip-flop in detail.

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