Code Conversion

BCD to Excess-3

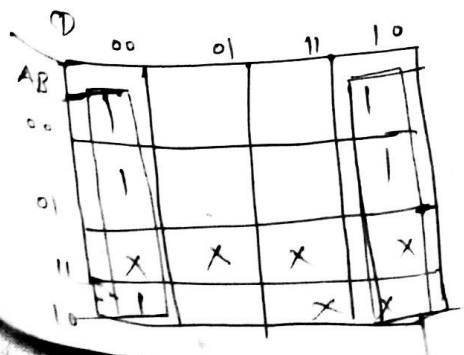
Input BCD

A	B	C	D
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	0	1

Output Excess-3

w	x	y	z
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0

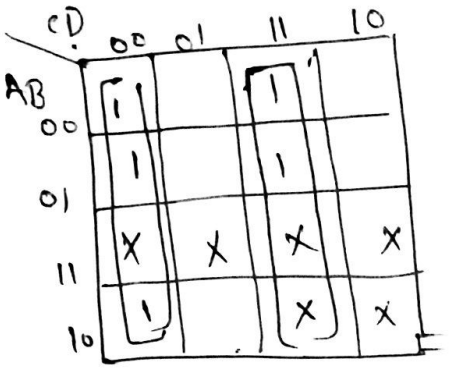
Minimised expression for z.



[1010, 1011, 1100, 1101, 1110, 1111]

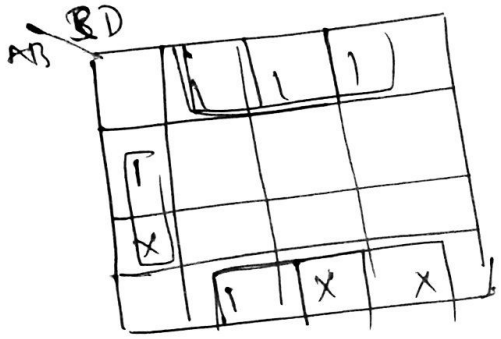
$z = D'$

for y



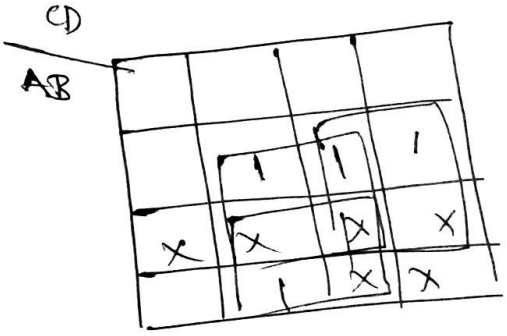
$C'D' + CD$

for x



$x = B'C + B'D + BC'D'$

for w

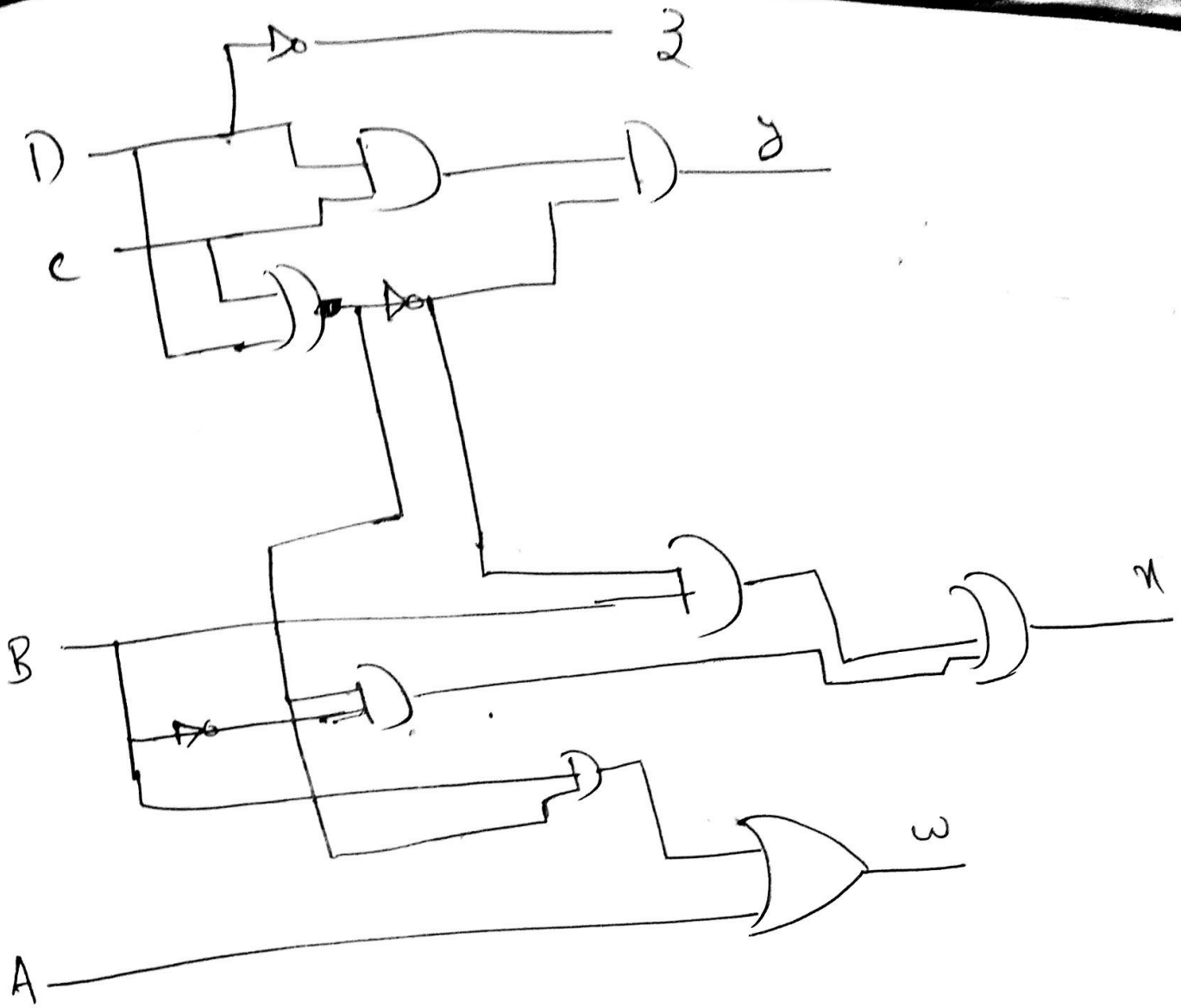


$BD + BC + A$

$z = D'$, $y = CD + (C+D)'$

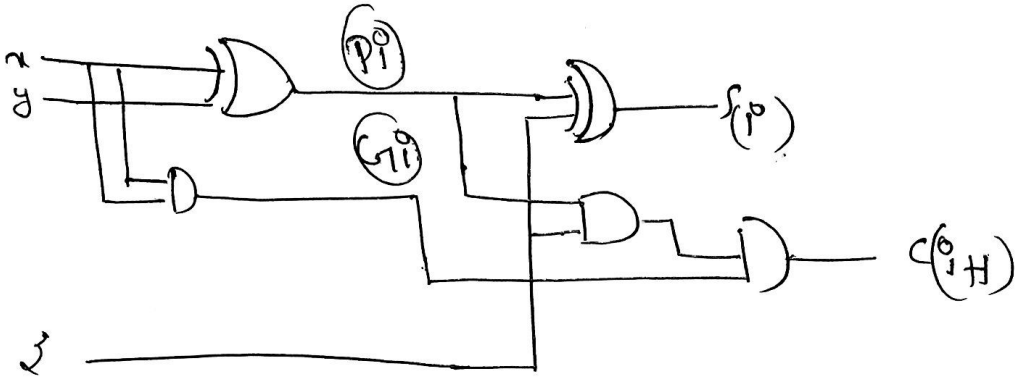
$x = B'(C+D) + B(C+D)'$

$w = A + BC + BD = A + B(C+D)$


3
D
y
C
x
B
w
A

Implementation of Full adder with two half adder and & Or gate

$S = xy'z' + x'y'z + xyz + x'yz'$ $\quad C = xz + xy + yz$



$$S = z \oplus (x \oplus y)$$

$$= z'(xy' + x'y) + z(xy' + x'y)'$$

$$= xy'z' + x'yz' + xyz + x'y'z$$

$$C = z(xy' + x'y) + xy = xy + yz + xz$$

Binary Parallel adder

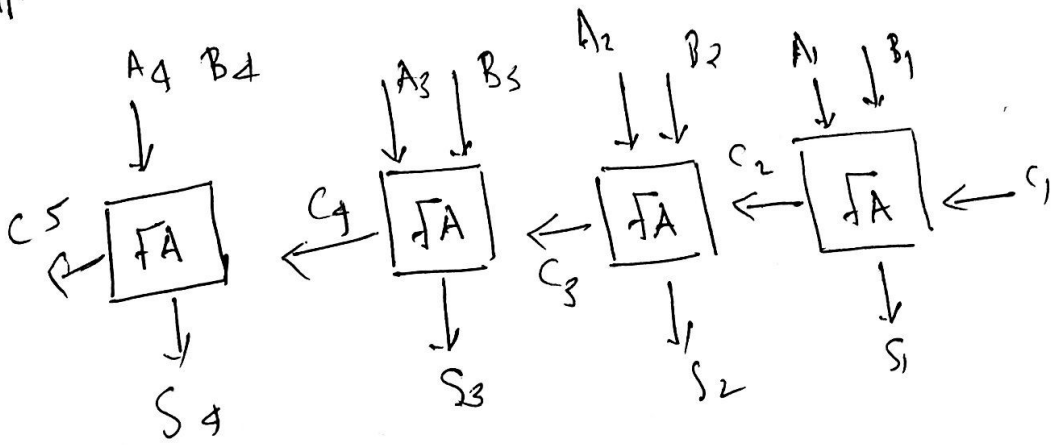
Full adders in chain carry of each input is connected to the next stage

Eg:→

Subscript (i)	4	3	2	1	
input carry	0	1	1		
augend	1	0	1	1	A_i
Addend					B_i

Sum output: 1 1 1 0 8°

0 0 1 1



(4 Bit Parallel Adder)

Delay → Carry of the current stage is required for next stages and this causes a chained delay and to overcome this we have to use the look ahead carry generator.

From the implementation of full adder from half adder & Or gate.

$$P_i^\circ = A_i^\circ \oplus B_i^\circ$$

$$G_i^\circ = A_i^\circ B_i^\circ$$

and from these

$$S_i^\circ = P_i^\circ \oplus C_i^\circ$$

$$C_{i+1} = G_i^\circ + P_i^\circ C_i^\circ$$

$G_i \rightarrow$ Carry generate, P_i = Propagate $(c_i - c_{i+1})$

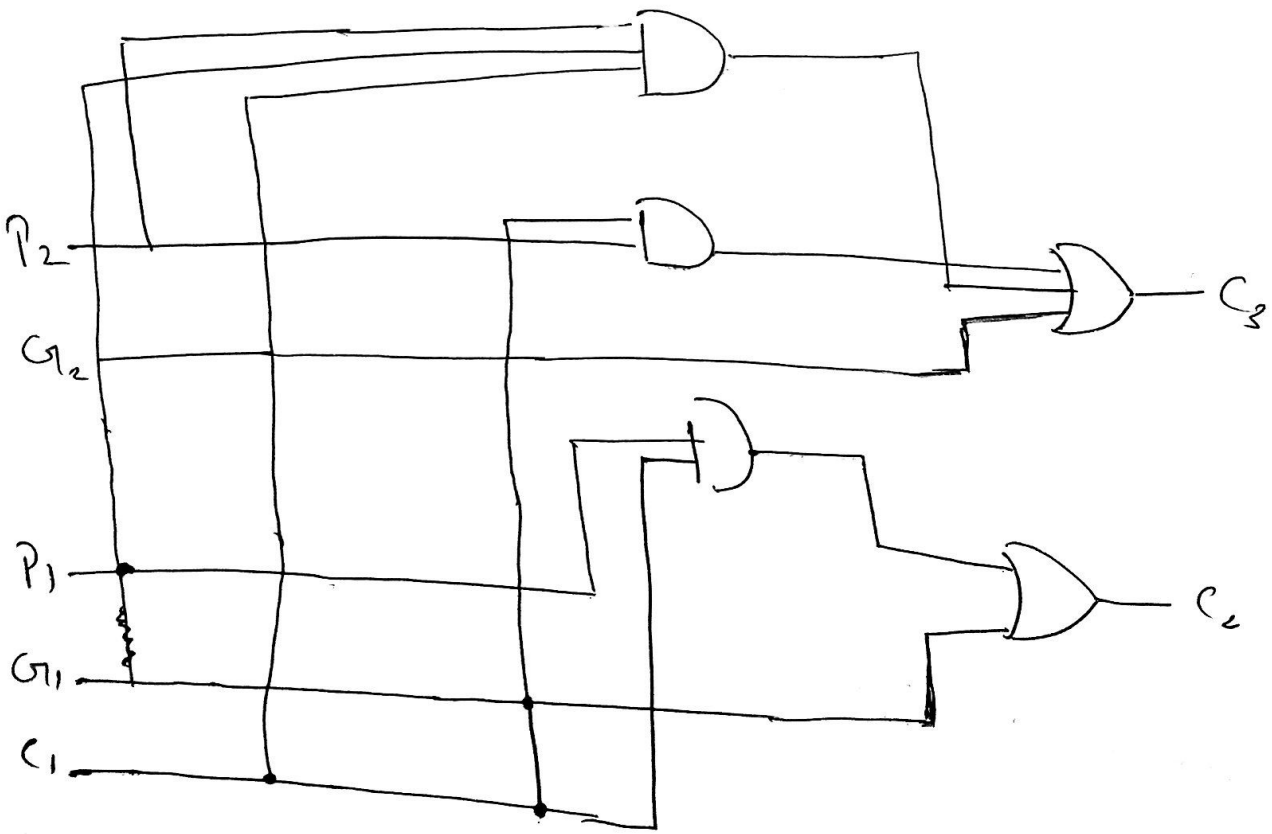
$$C_2 = G_1 + P_1 C_1$$

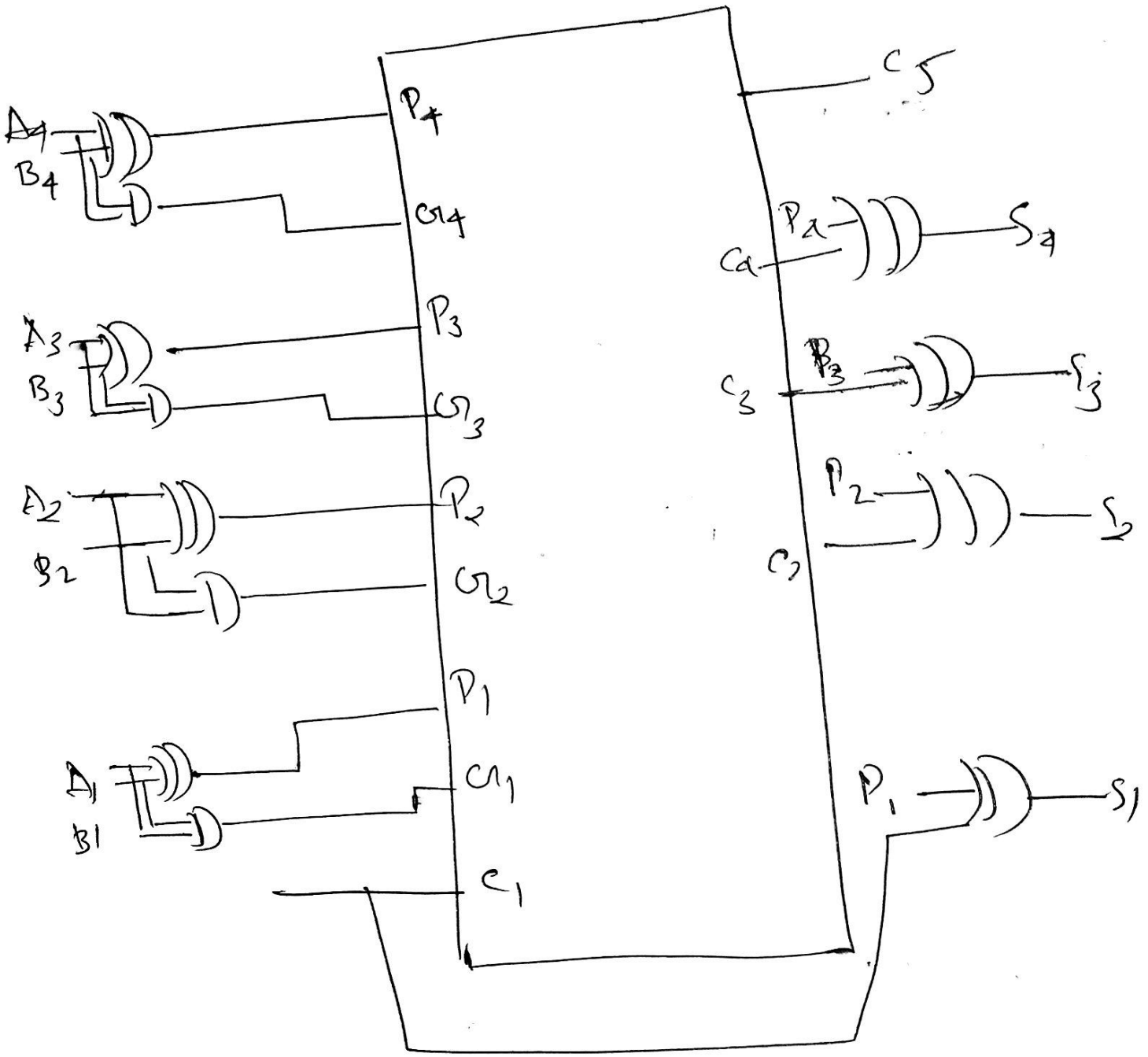
$$C_3 = C_2 + P_2 C_2 = G_2 + P_2 (G_1 + P_1 C_1)$$

$$C_4 = C_3 P_3 + G_3 = G_3 + P_3 G_2 + P_3 G_2 G_1 + P_3 P_2 P_1 G$$

(Depend only on two first Carry so Delay is minimised)

Circuit diagram




A4
B4
P4
G4
C5
P4
S4
C4
A3
B3
P3
G3
B3
S3
C3
A2
B2
P2
G2
P2
S2
C2
P1
A1
B1
G1
P1
S1
C1