SRAM is much costlier than DRAM.

Synchronous DRAM:

Exchanges data with the **processor synchronized to an external clock** signal and running at the full speed of the **processor/memory bus without imposing wait states.**

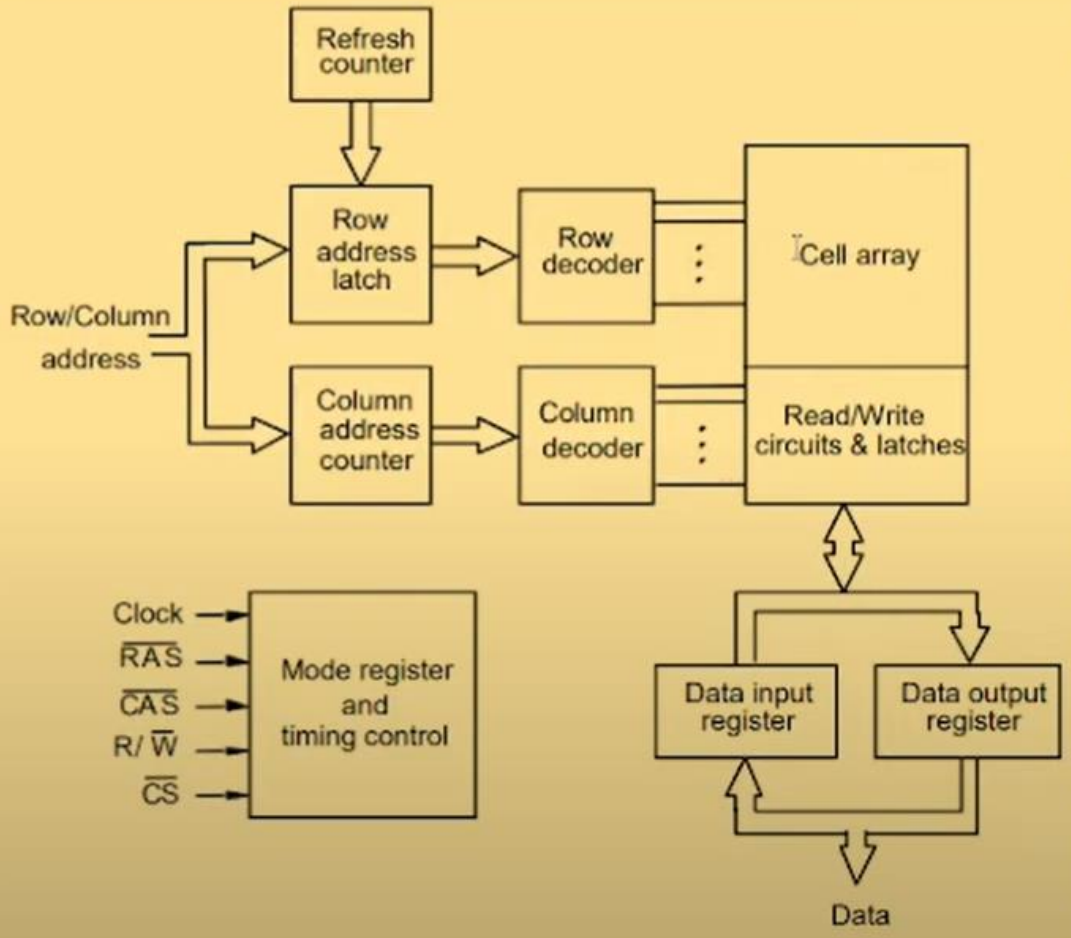
In a typical DRAM, the **processor presents addresses and control levels to the memory**, indicating that a set of **data at a particular location in memory should be either read from or written into the DRAM.**

After a delay, the access time, the **DRAM either writes or reads the data.** During the access-time delay, the **DRAM performs various internal functions**, such as activating the high capacitance of the row and column lines, sensing the data, and routing the data out through the output buffers. **The processor must simply wait through this delay, slowing system performance.**

With synchronous access, the DRAM moves data in and out under control of the system clock. **The processor or other master** issues the instruction and address information, which is latched by the DRAM. The **DRAM then responds after a set number of clock cycles.** Meanwhile, the **master can safely do other tasks while the SDRAM is processing the request.**

Following diagram shows typical SDRAM.

Synchronous DRAMs



- *Operation is directly synchronized with processor clock signal.*
- *The outputs of the sense circuits are connected to a latch.*
- *During a Read operation, the contents of the cells in a row are loaded onto the latches.*
- *During a refresh operation, the contents of the cells are refreshed without changing the contents of the latches.*
- *Data held in the latches correspond to the selected columns are transferred to the output.*
- *For a burst mode of operation, successive columns are selected using column address counter and clock. CAS signal need not be generated externally. A new data is placed during raising edge of the clock*

Table 6.3 SDRAM Pin Assignments

A0 to A13	Address inputs
BA0, BA1	Bank address lines
CLK	Clock input
CKE	Clock enable
$\overline{CS}$	Chip select
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQ0 to DQ7	Data input/output
DQM	Data mask