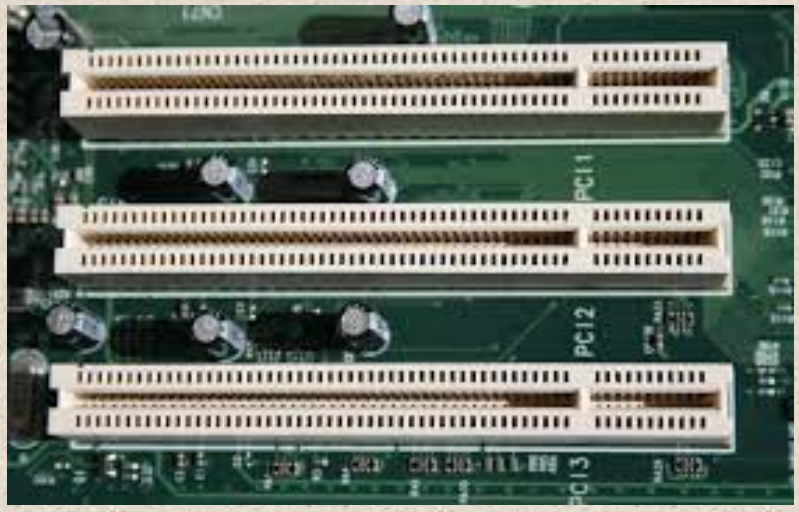
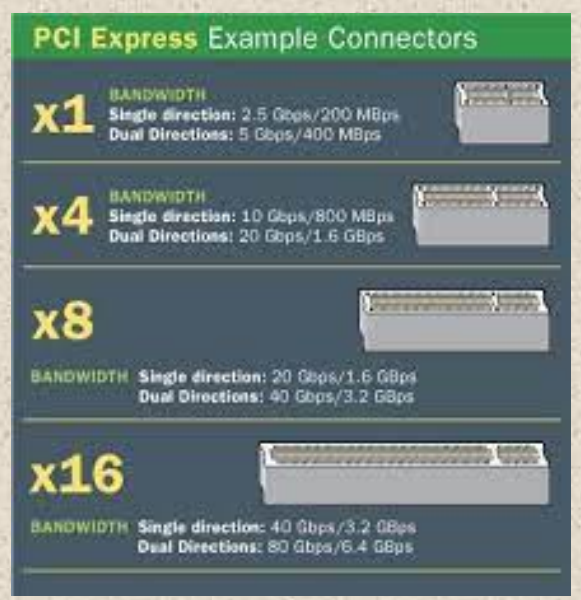
Peripheral Component Interconnect (PCI)





- A popular **high bandwidth, processor independent** bus that can function as a mezzanine or **peripheral bus**
- Delivers **better system performance** for high speed I/O subsystems
  - Graphics Display adapters
  - Network interface card
  - Sound card
  - Ehternet card
  - Video capture card
  - TV card tuner
- PCI Special Interest Group (SIG)
  - Industry Association (developed PCIe)
  - Created to develop further and maintain the compatibility of the PCI specifications
- PCI is used in Personal computer , Workstation , Server systems

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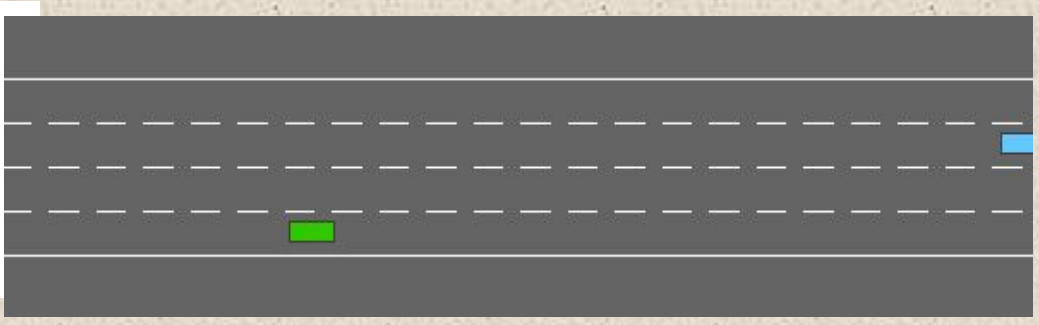
- The **PCI (Peripheral Component Interface) standard is designed for high-speed, efficient data movement.**
- Since its introduction in the early 1990s, the PCI architecture has seen a number of improvements allowing faster data transfers. *(PCI replaces Accelerated Graphics Port).*
- PCI bus performance is dependent on **two factors:**
- **Clock speed and bus width**
  - **Clock Speed** – refers to the number of clock cycles a certain component generates per second. This is typically described in Megahertz (MHz). PCI architectures run as slow as 8 MHz and as fast as 133 MHz. Most commonly, it runs at 33 or 66 MHz.
  - **Bus width** refers to the number of bits transferred per second
- Using a **highway as an analogy**, consider **clock speed as the speed limit**, while **bus width is the number of lanes**
- A PCI bus acts in a similar manner. **Increasing clock speed or bus width allows you to move more data per second**

Clock Speed	Bus Width	Overall Data Throughput
33 MHz	32-bit	132 MB/sec.
66 MHz	32-bit	264 MB/sec.
33 MHz	64-bit	264 MB/sec.
66 MHz	64-bit	528 MB/sec.



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PCI-X

- It is the latest implementation of PCI bus technology, uses the same **64-bit** architecture as the current standard
- PCI-X has doubled the clock speed to **133 MHz**, allowing transfer speeds up to **1 GB/sec**.
- **PCI Express (PCIe)**
  - Point-to-point interconnect scheme intended to replace bus-based schemes such as PCIx or PCI
- **Key requirements of PCIe**
  - high capacity to support the needs of higher data rate I/O devices, such as Gigabit Ethernet
  - need to support time dependent data streams

S.NO	PCI	PCI-X
1.	PCI is a computer bus that connects hardware devices.	PCI-X is a computer bus that connects hardware devices and has an expansion card.
2.	It was introduced in the year 1992 by Intel.	It was introduced in the year 1998 by IBM, HP and Compaq.
3.	Conventional PCI is another name for PCI.	Peripheral Component Interconnect eXtended is the abbreviated form of PCI-X.
4.	Hot swapping feature is optional.	Hot swapping feature was made mandatory.
6.	PCI provides a slower data rate	PCI-X provides faster data rate.
7.	PCI was replaced by PCI-X.	PCI-X was replaced by PCI-E.
8.	The speed of a PCI slot is upto 133MB/s.	The speed of a PCI-X slot is upto 1064MB/s.
9.	It has less features.	It has more features.
10.	The width of PCI is about 32 or 64 bits.	The width of PCI-X is 64 bits

The Relationship Between PCI vs PCI-X vs PCI-E

- The main difference between the previous PCI card and PCI-X card and the successor PCIe card is "**parallel vs serial" data transmission.**
- PCI and PCI-X network cards follow the original PCI standard, classic shared bus architecture with all connected peripherals using **the same bus in parallel**
  - **The overall performance will go down as the increase of added devices.**
- PCI-E card,, **adopts dedicated point-to-point serial technology,** resembling an on-board network, therefore each individual device has its own bus, which creates a more efficient bus system

NOTE:

- ***one serial connection*** *with a* ***higher clock*** *can match the* ***speed*** *of multiple* ***parallel lines*** *moving on the* ***same load****.*

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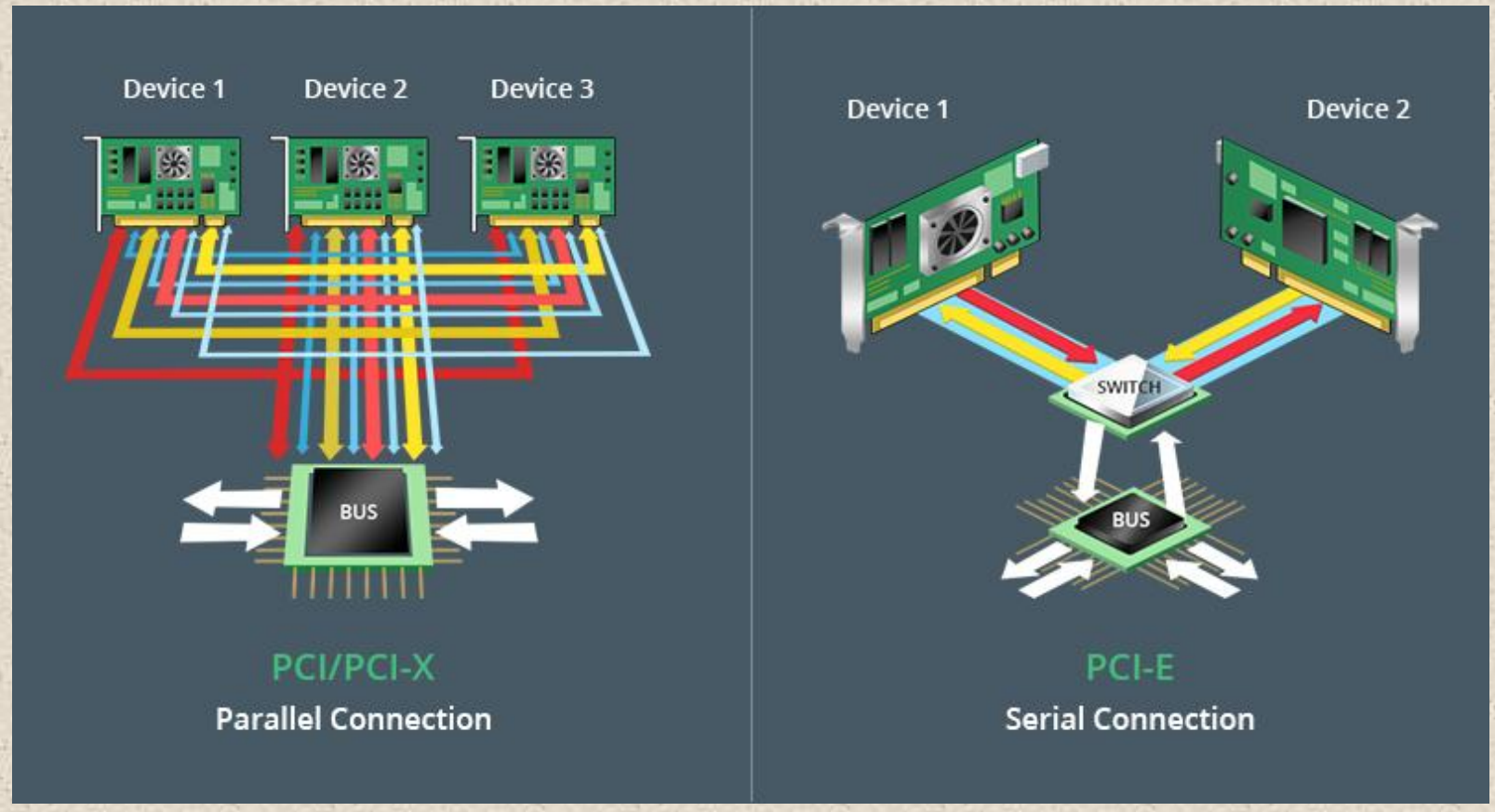

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Type	Working Topology	Bus Type	Clock Speed	Transmission Speed
PCI	Parallel transmission	32-bit 64-bit	33MHz 66MHz	32-bit: 133MB/s, 266MB/s 64-bit: 266MB/s, 533MB/s
PCI-X	Parallel transmission	64-bit	66MHz 100MHz 133MHz (Up to 533MHz)	533MB/s; 800MB/s; 1066MB/s
PCI-E (PCIe 1.0 8x version)	Serial transmission	8-bit	2.5GHz	4GB/s

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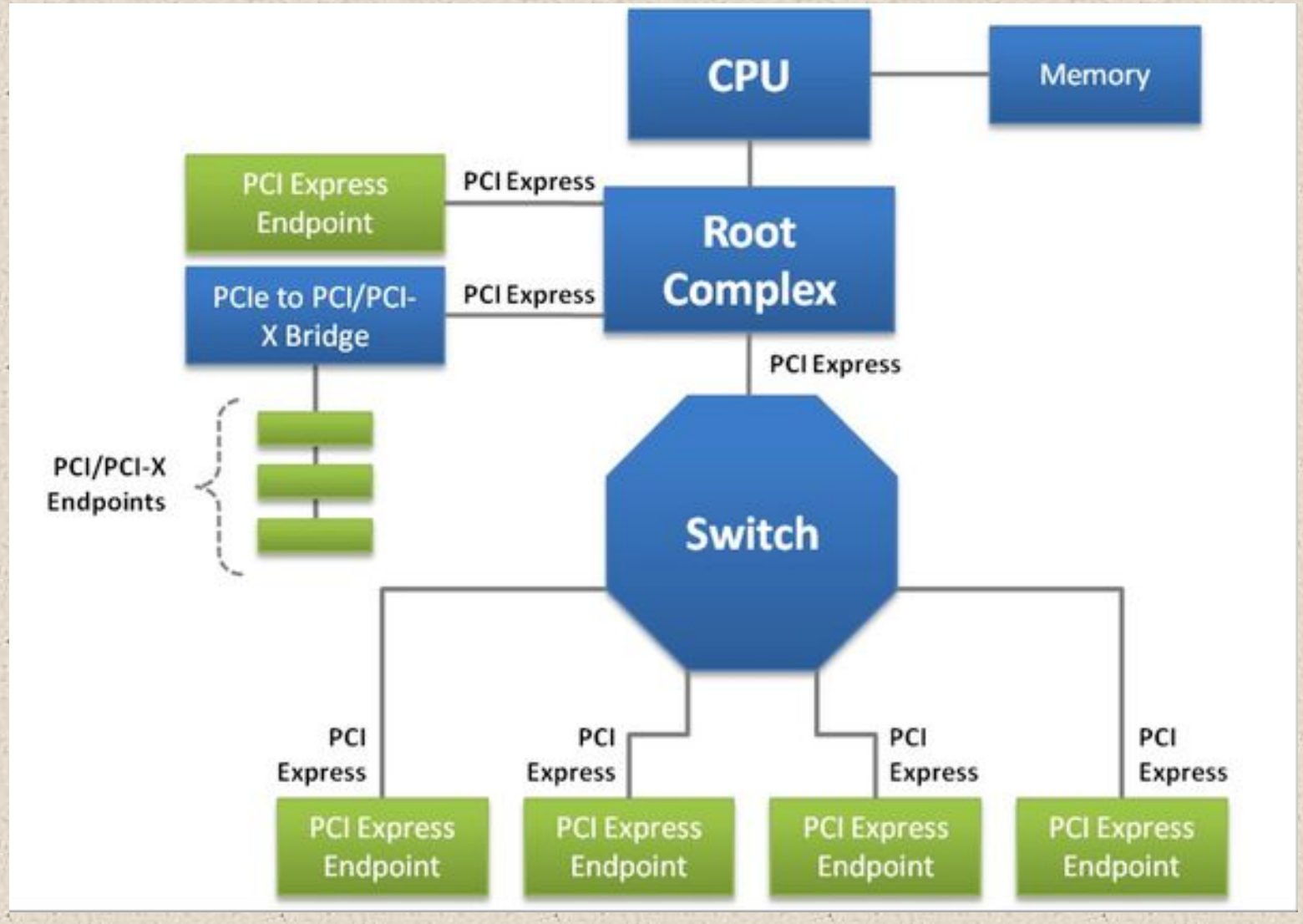
Configuration Using PCIe



Configuration Using PCIe (contd…)

- . A **root complex** device, also referred to as a *chipset* or a *host bridge,* connects the processor and memory subsystem to the PCI Express switch fabric comprising one or more PCIe and PCIe switch devices.

- The root complex (Chipset)
  - acts as a buffering device and deals with difference in data rates between I/O controllers and memory and processor components
  - translates between PCIe transaction formats and the processor and memory signal and control requirements
  - will support multiple PCIe ports, some of which attach directly to a PCIe device and some of which attach to a switch that manages multiple PCIe streams.

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Configuration Using PCIe (contd…)

- PCIe links from the chipset may attach to the following devices that implement PCIe
  - **Switch -** manages multiple PCIe streams
  - **End Points –** IO device or controller – implements PCLe like Gigabit ethernet switch, a graphics, disk interface etc.,
  - **Legacy endpoint –** IO transaction and may support locked transaction
  - **PCIe / PCI bridge –** allows older PCI devices to be connected to PCIe based system
- Endpoints initiate transactions as a requester or respond to transactions as a completer
  - Two Types of End-Points exists as
    - PCIe endpoint
    - Legacy endpoint

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Configuration Using PCIe (contd…)

- **PCIe endpoint:**
  - An I/O device or controller that implements PCIe such as
    - a Gigabit Ethernet switch
    - a graphics or video controller
    - disk interface
    - a communications controller.
- **Legacy endpoint**
  - support IO transactions and support locked transaction semantics as a completer but not as a requester
- **PCIe/PCI bridge**
  - Allows older PCI devices to be connected to PCIe-based systems.

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- **PCIe is a point-to-point architecture**
  - Each PCIe port consists of number of bidirectional lanes . A PCI port can provide 1, 4, 6, 16, or 32 lanes.
- **PCIe uses a multilane distribution technique**
  - Data are distributed to the four lanes -1 byte at a time using a simple round-robin scheme. At each physical lane, data are buffered and processed 16 bytes (128 bits) at a time. Each block of 128 bits is encoded into a unique 130-bit codeword
- **PCIe relies on the receiver synchronizing**
  - PCIe does not use its clock line to synchronize. It is necessary for the receiver to be synchronized with the transmitter, so that the receiver knows when each bit begins and ends.
  - If there is any drift between the clocks used for bit transmission and reception of the transmitter and receiver, errors may occur
  - Synchronization can be achieved by the receiver looking for transitions in the data and synchronizing its clock to the transition

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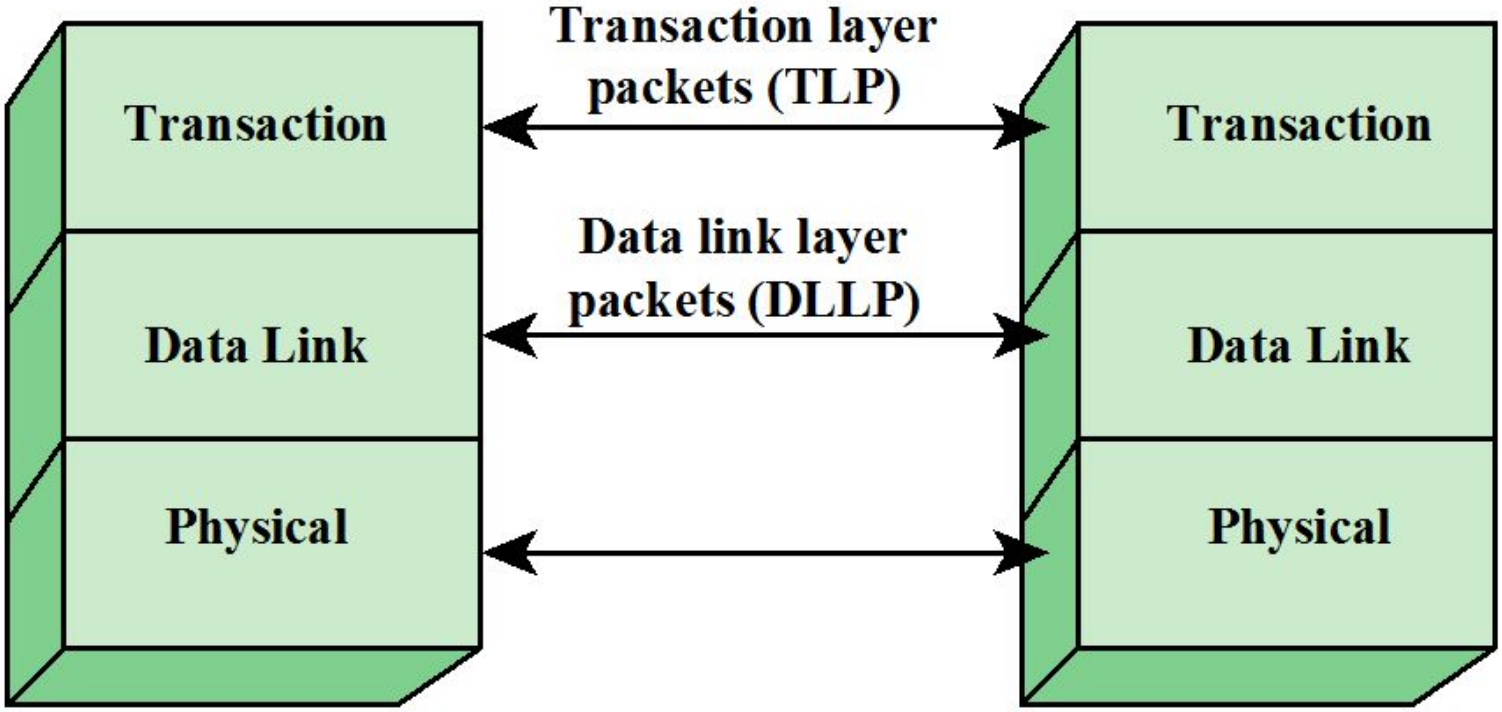
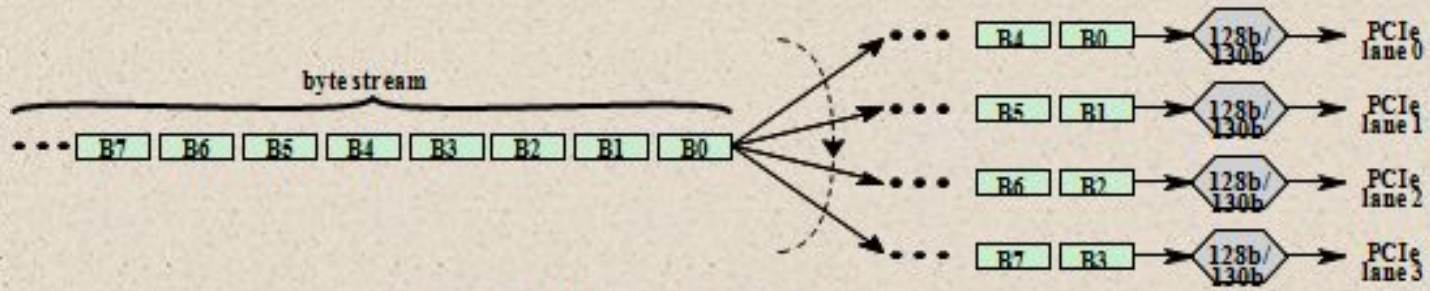
PCIe Protocol Layers



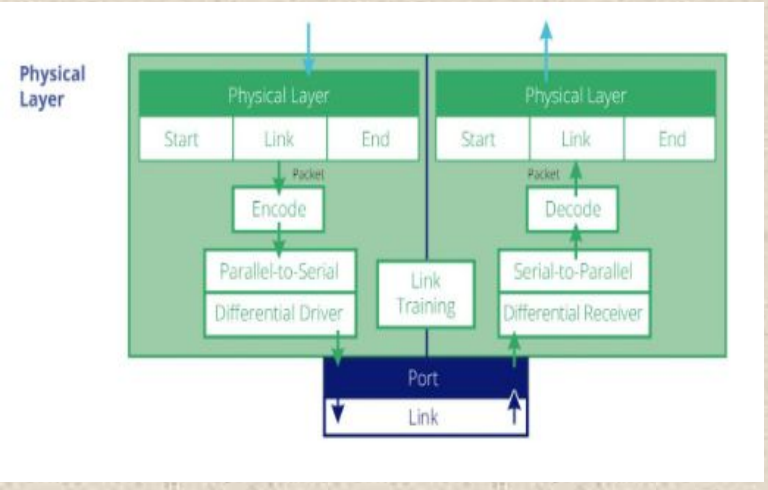
PCIe Protocol Layers (contd...)

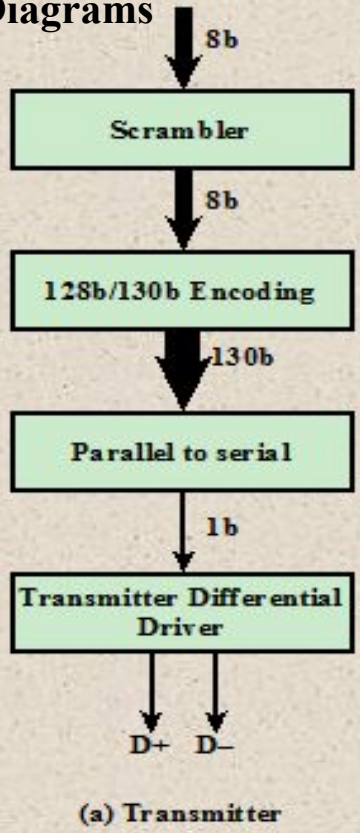
- **Physical**
  - Consists of the actual wires carrying the signals, as well as circuitry and logic to support ancillary features required in the transmission and receipt of the 1s and 0s
- **Data link**
  - Responsible for reliable transmission and flow control.
  - Data packets generated and consumed by the DLL are called Data Link Layer Packets (DLLPs)
- **Transaction**
  - Generates and consumes data packets used to implement load/store data transfer mechanisms and also manages the flow control of those packets between the two components on a link. Data packets generated and consumed by the TL are called Transaction Layer Packets (TLPs).
- **Software Layers**
  - Above the TL are software layers that generate read and write requests that are transported by the transaction layer to the I/O devices using a packet-based transaction protocol.

PCIe Physical Layer (contd...)

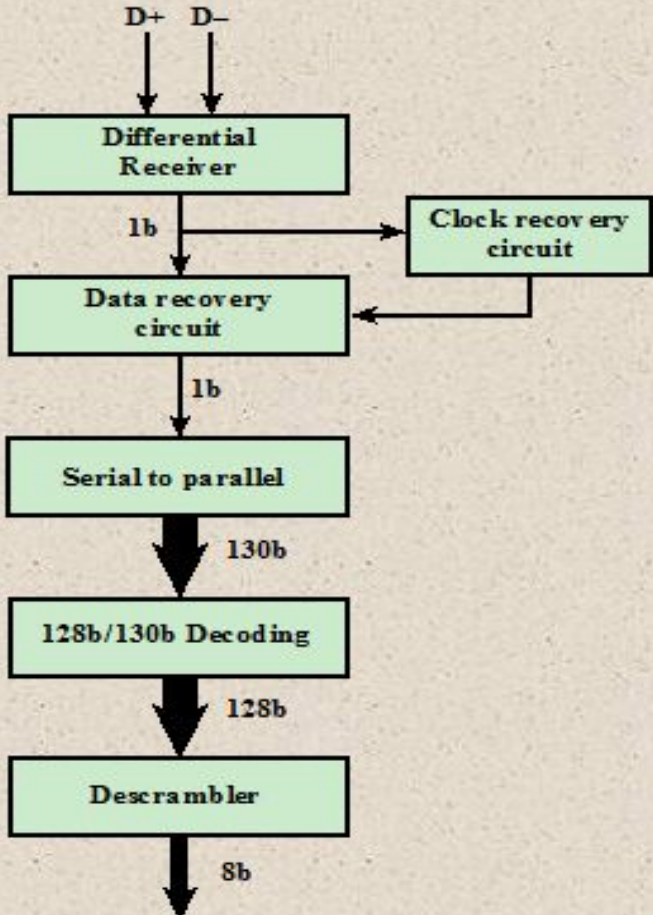


PCIe Transmit and Receive Block Diagrams





(a) Transmitter



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PCIe Physical Layer (contd...)

- Overcoming the problem of a long string of bits
  - **Scrambling**
    - does not increase the number of bits to be transmitted
    - is a mapping technique that tends to make the data appear more random
    - At the receiving end, a **descrambling** algorithm recovers the original data sequence.
  - **Encoding**
    - additional bits are inserted into the bit stream to force transitions
    - Each group of 128 bits of input is mapped into a 130-bit block by adding a 2-bit block sync header. The value of the header is 10 for a data block and 01 for lled an *ordered set block, which refers to a link-level information block*

PCIe Physical Layer (contd...)

- Encoding
  - **Transmitter Side**
    - Data to be transmitted are fed into a scrambler. The scrambled output is then fed into a 128b/130b encoder, which buffers 128 bits and then maps the 128-bit block into a 130-bit block. This block then passes through a parallel-to-serial converter and is transmitted one bit at a time using differential signalling
  - **Receiver Side**
    - a clock is synchronized to the incoming data to recover the bit stream. This then passes through a serial-to-parallel converter to produce a stream of 130-bit blocks. Each block is passed through a 128b/130b decoder to recover the original scrambled bit pattern, which is then descrambled to produce the original bit stream.

PCIe

Transaction Layer (TL)

- Receives read and write requests from the software above the TL and creates request packets for transmission to a destination via the link layer
- Most transactions use a *split transaction* technique
  - A request packet is sent out by a source PCIe device which then waits for a response called a *completion* packet
  - The completion following a request is initiated by the completer only when it has the data and/or status ready for delivery
  - Each packet has a unique identifier that enables completion packets to be directed to the correct originator.

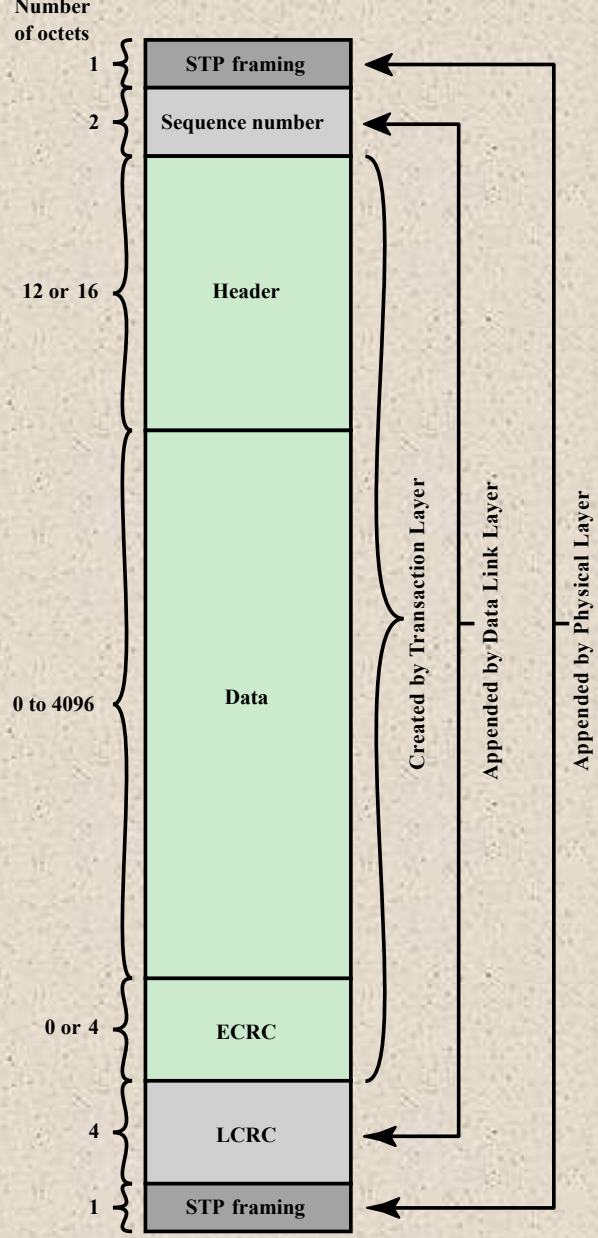
PCIe

Transaction Layer (TL)

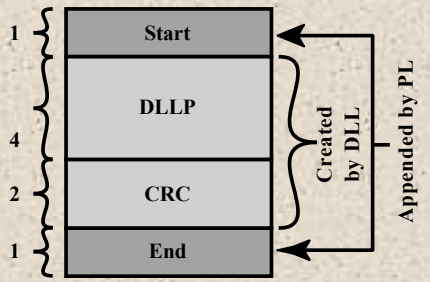
- TL messages and some write transactions are **posted transactions** (meaning that no response is expected)
- TL packet format supports 32-bit memory addressing and extended 64-bit memory addressing

TLP PACKET ASSEMBLY

- PCIe transactions are conveyed using transaction layer packets
- A TLP originates in the transaction layer of the sending device and terminates at the transaction layer of the receiving device
- Upper layer software sends the following information needed to create the core of the TLP
  - **Header**
    - The header describes the type of packet and includes information needed by the receiver to process the packet, including any needed routing information
  - **Data**
    - A data field of up to 4096 bytes may be included in the TLP. Some TLPs do not contain a data field
  - **ECRC (Endpoint)**
    - An optional end-to-end CRC field enables the destination TL layer to check for errors in the header and data portions of the TLP



(a) Transaction Layer Packet



(b) Data Link Layer Packet

PCIe Protocol Data Unit Format

PCIe

Data Link Layer (DLL)

- Data link layer is to ensure reliable delivery of packets across the PCIe link
  - creates TLPs
  - transmits DLLPs
- *DATA LINK LAYER PACKETS*
  - Data link layer packets originate at the data link layer of a transmitting device and terminate at the DLL of the receiving device
  - **3** important groups of DLLPs used in managing a link
    - flow control packets
      - regulate the rate at which TLPs and DLLPs can be transmitted across a link
    - power management packets
      - used in managing power platform budgeting
    - TLP ACK and NAK packets
      - used in TLP processing

TRANSACTION LAYER PACKET PROCESSING

- The DLL adds two fields to the core of the TLP created by the TL
  - a 16-bit sequence
  - number and a 32-bit link-layer CRC (LCRC)

- When a TLP arrives at a device, the DLL strips off the sequence number and LCRC fields and checks the LCRC. There are two possibilities
  - If no errors are detected, the core portion of the TLP is handed up to the local transaction layer.
    - If this receiving device is the intended destination, then the TL processes the TLP
    - Otherwise, the TL determines a route for the TLP and passes it back down to the DLL for transmission over the next link on the way to the destination.
  - If an error is detected, the DLL schedules an NAK DLL packet to return back to the remote transmitter. The TLP is eliminated

- When the DLL transmits a TLP, it retains a copy of the TLP. If it receives a NAK for the TLP with this sequence number, it retransmits the TLP. When it receives an ACK, it discards the buffered TLP.

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