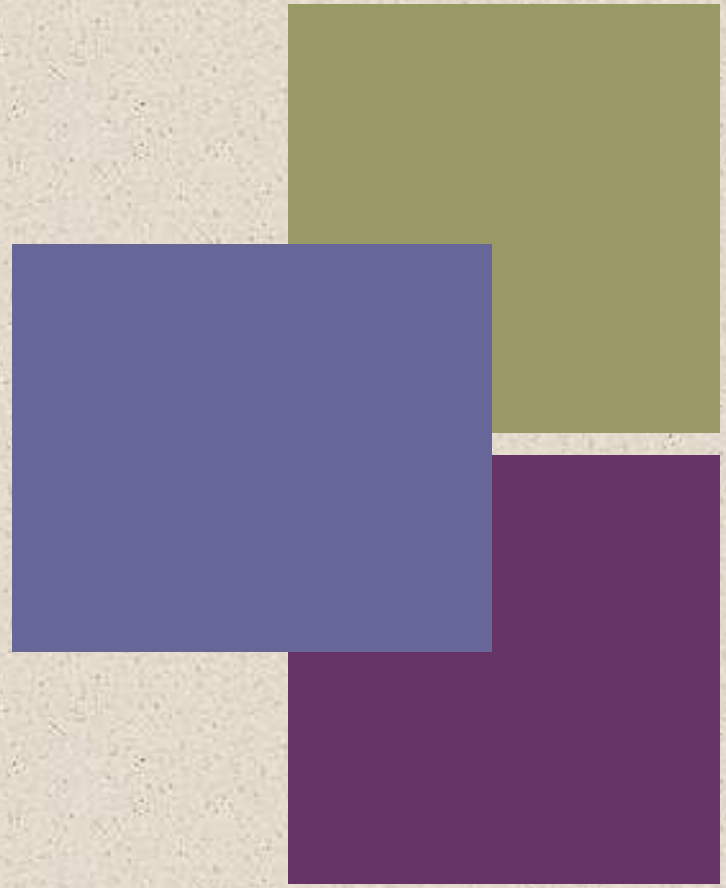


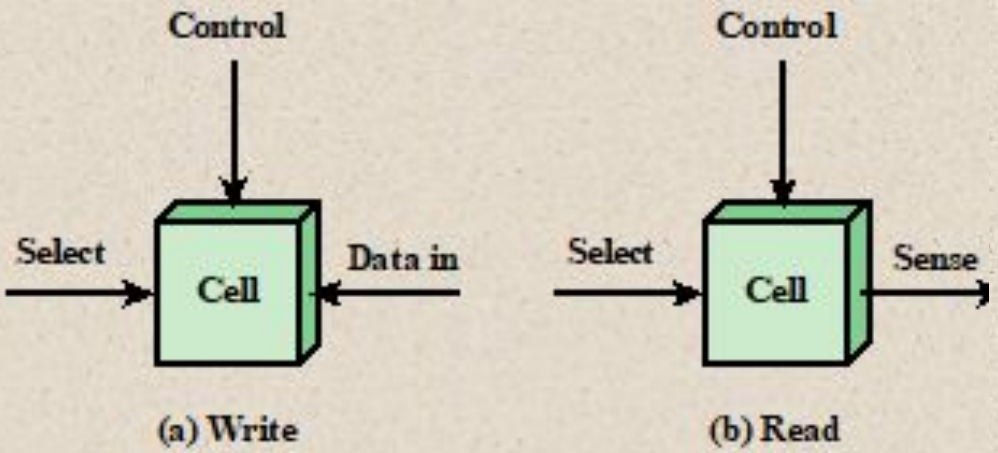
Internal Memory, Semiconductor memory

The basic element of a **semiconductor memory** is the **memory cell**.

All semiconductor memory cells **share certain properties**

- They exhibit two stable (or semi-stable) states, which can be used to represent binary 1 and 0.
- They are capable of being written into (at least once), to set the state.
- They are capable of being read to sense the state.

- Most commonly, the cell has **three functional terminals** capable of carrying an electrical signal.
- The **select terminal**, as the name suggests, selects a memory cell for a read or write operation. The control terminal indicates read or write.
- The memory cell **will store** the **bit that is on its input** lead **when the WRITE control signal is ON** and **will place the bit** that is in the cell **on its output lead when the READ control signal is ON**



Memory Type	Category	Erasure	Write Mechanism	Volatility
Random-access memory (RAM)	Read-write memory	Electrically, byte-level	Electrically	Volatile
Read-only memory (ROM)	Read-only memory	Not possible	Masks	Nonvolatile
Programmable ROM (PROM)				
Erasable PROM (EPROM)	Read-mostly memory	UV light, chip-level	Electrically	
Electrically Erasable PROM (EEPROM)		Electrically, byte-level		
Flash memory		Electrically, block-level		

Table 5.1
Semiconductor Memory Types

Dynamic RAM (DRAM)

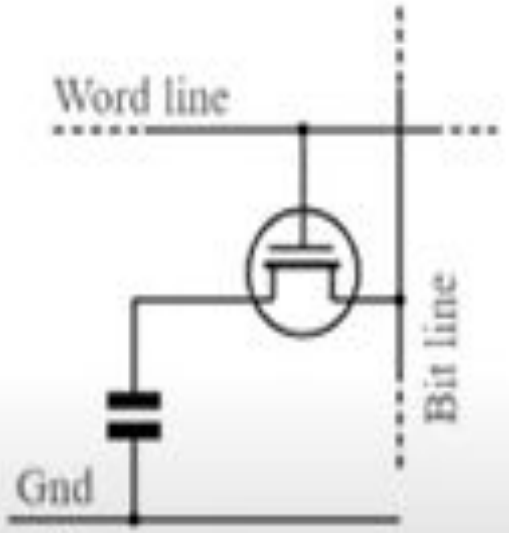
- RAM technology is divided into two technologies:
  - Dynamic RAM (DRAM)
  - Static RAM (SRAM)
- DRAM
  - Made with cells that store data as charge on capacitors
  - Presence or absence of charge in a capacitor is interpreted as a binary 1 or 0
  - Requires periodic charge refreshing to maintain data storage
  - The term *dynamic* refers to tendency of the stored charge to leak away, even with power continuously applied

Dynamic RAM (DRAM)

Working of DRAM

- Basics

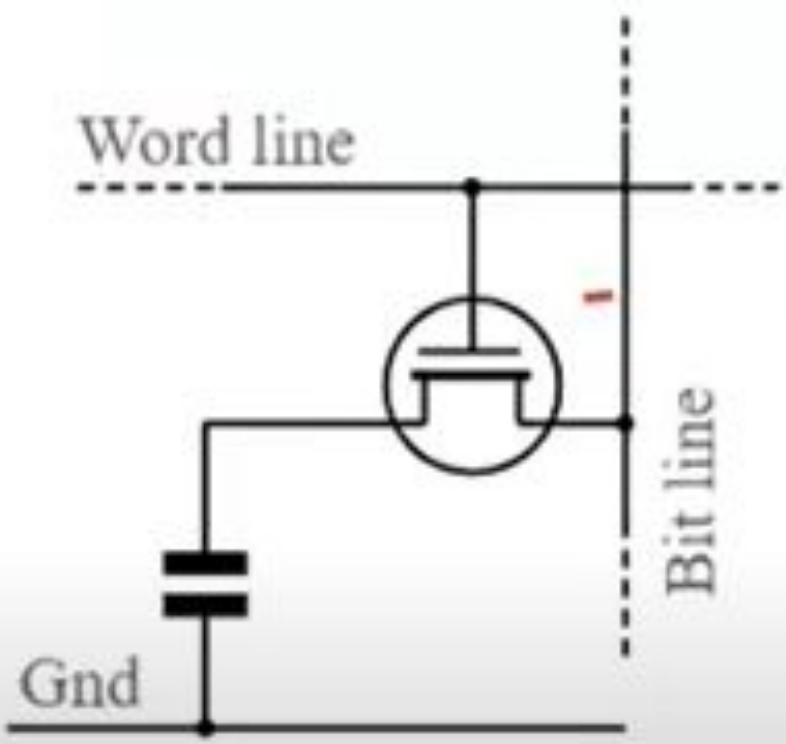
- Data is held by the storage capacitor.
- Dynamic: Needs periodic refreshing.
- Volatile: loses data when powered OFF
- Single transistor. Therefore smaller, high density and cheaper.
- Charge storage, Q = CVdd



Dynamic RAM (DRAM)

- Write Operation

1. WL = 1
2. Access transistors turned ON.
3. Apply voltage (Logic 1 = Vdd and Logic 0 =GND) to Bit Line.
4. Accordingly, capacitor will be charged to Vdd or discharged to GND.



Dynamic RAM (DRAM)

- Hold Operation

1. WL = 0
2. Access transistors turned OFF.
3. Charge is held on a capacitor.

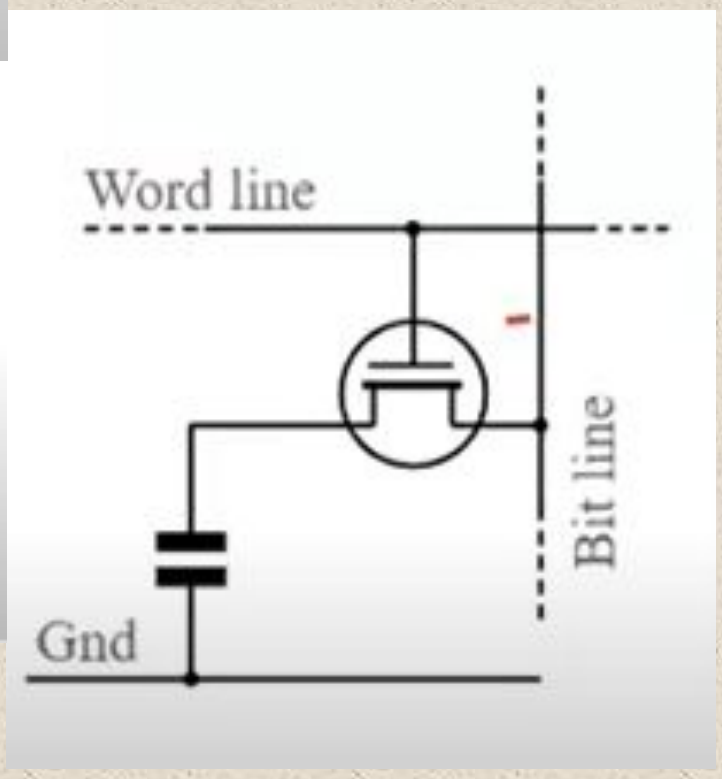
4. Leakage currents due to discharging of a capacitor.

I = Q/T = CV/T

5. Determine T to find out the hold time: (Maximum time upto which the voltage of the capacitor remains high enough to be at logic 1)

T = CV/I

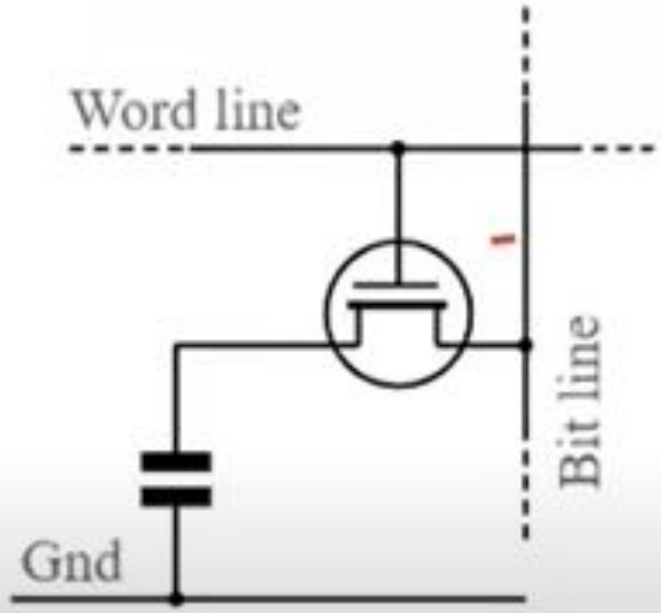
6. Accordingly, determine the refresh rate.



Dynamic RAM (DRAM)

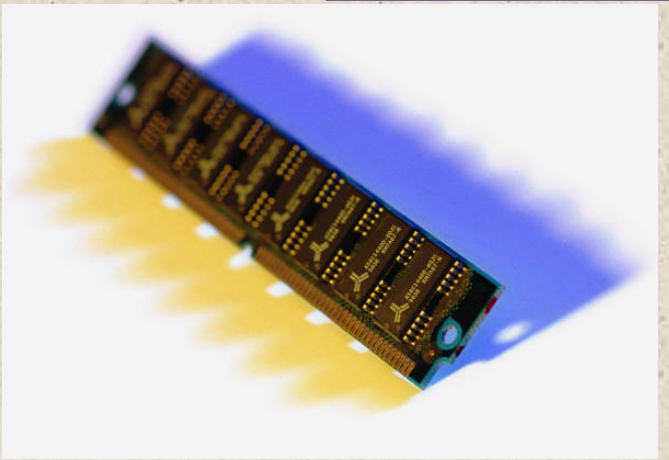
- Read Operation

1. WL = 1
2. Access transistors turned ON.
3. Charge of the capacitor would get distributed with bit line capacitance.
4. This will change the bit line voltage as 1 or 0



Static RAM (SRAM)

- Digital device that uses the same logic elements used in the processor
- Binary values are stored using traditional flip-flop logic gate configurations
- Will hold its data as long as power is supplied to it

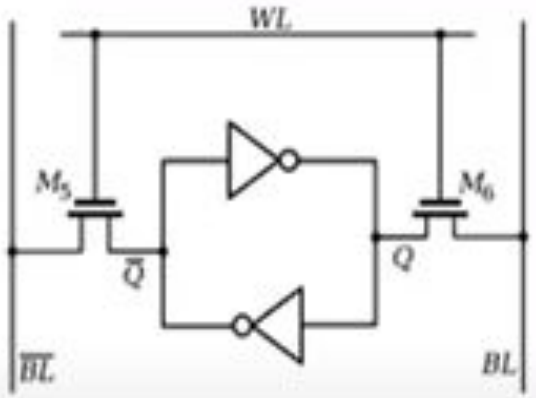


Static RAM (SRAM)

Working of SRAM

- Write

1. WL = 1
2. Access transistors are turned ON
3. Values are applied at both BL and BL_bar.
4. Data in the latch is overwritten with the new value.



- Hold

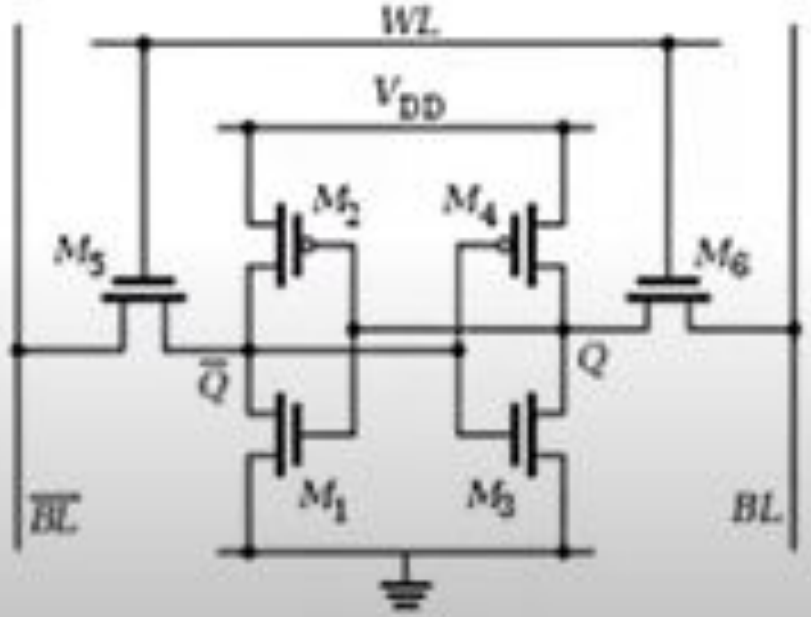
1. WL = 0
2. Data is held in the latch mode

- Read

1. WL = 1
2. Access transistors are turned ON
3. BL and BL_bar values are read by Sense Amplifier

Static RAM (SRAM)

All CMOS, lesser Power dissipation, better noise margin, larger size



SRAM versus DRAM

- Both volatile
  - Power must be continuously supplied to the memory to preserve the bit values

SRA
M

DRA
M

DYNAMIC RAM (DRAM)

- Bits stored as charge in capacitors.
- Charges leak.
- Need refreshing even when powered.
- Simpler construction.
- Smaller per bit.
- Less expensive.
- Need refresh circuits.
- Slower.
- Main memory.

STATIC RAM (SRAM)

- Bits stored as on/off switches.
- No charges to leak.
- No refreshing needed when powered.
- More complex construction.
- More expensive
- Faster
- Cache
- Digital
  - Uses flip-flops