2024 VLSI 期末考试回忆版

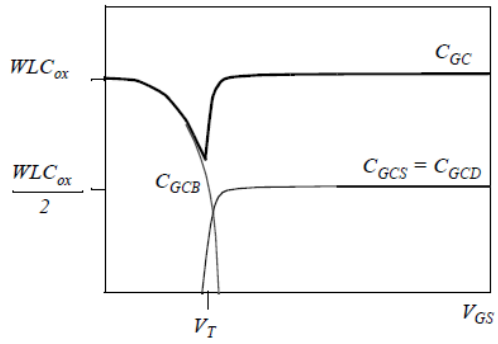
1.名词解释

(1) abstraction hierarchy	(6) charging sharing
(2) strong inversion	(7) path effort
(3) parasitic parameter	(8) domino logic
(4) physical synthesis	(9) combinational logic
(5) mobility degradation	(10) clock to pad

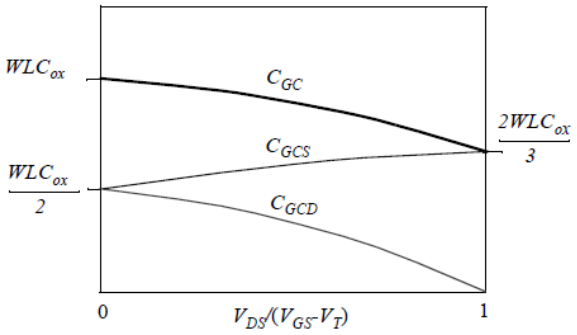
2.描述如何利用 Y-Chart 进行 IC 电路设计。

3. Compute the NMOS and PMOS saturation voltages and saturation currents per micron of width for a 130 nm technology. Assume a channel length of 100 nm, tox = 22 Å, Cox = 1.6*10^(-6)F/cm, VTn = 0.4 V, VTp = -0.4 V, VGS = 1.2 V. Use vsat = 8*10^6 cm/s.

4.描述并总结下图。

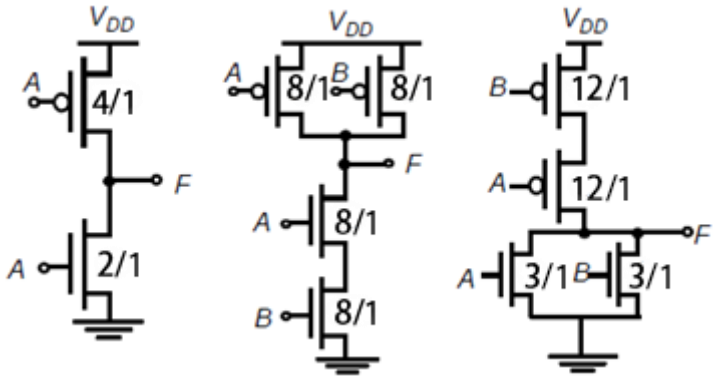


(a) C_{GC} as a function of V_{GS} (with V_{DS}=0)



(b) C_{GC} as a function of the degree of saturation

5.计算下图所示各电路 Logic effort。

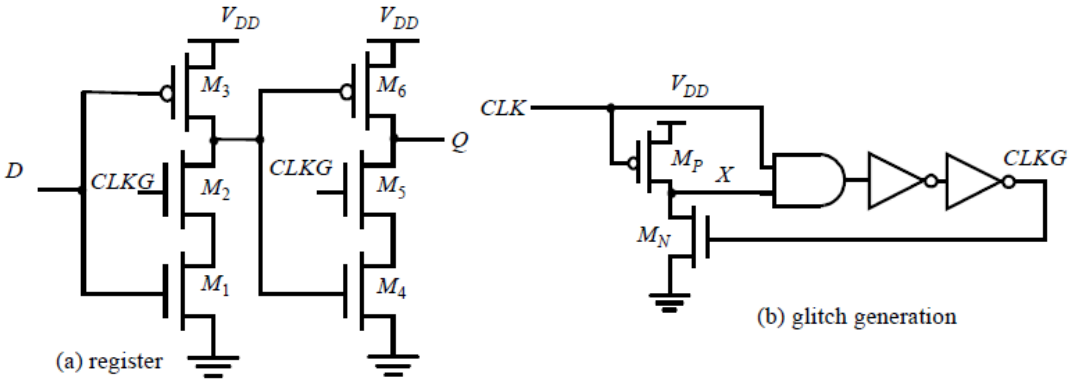


6.用 CMOS 电路实现布尔表达式 F = /(D+A·(B+C))

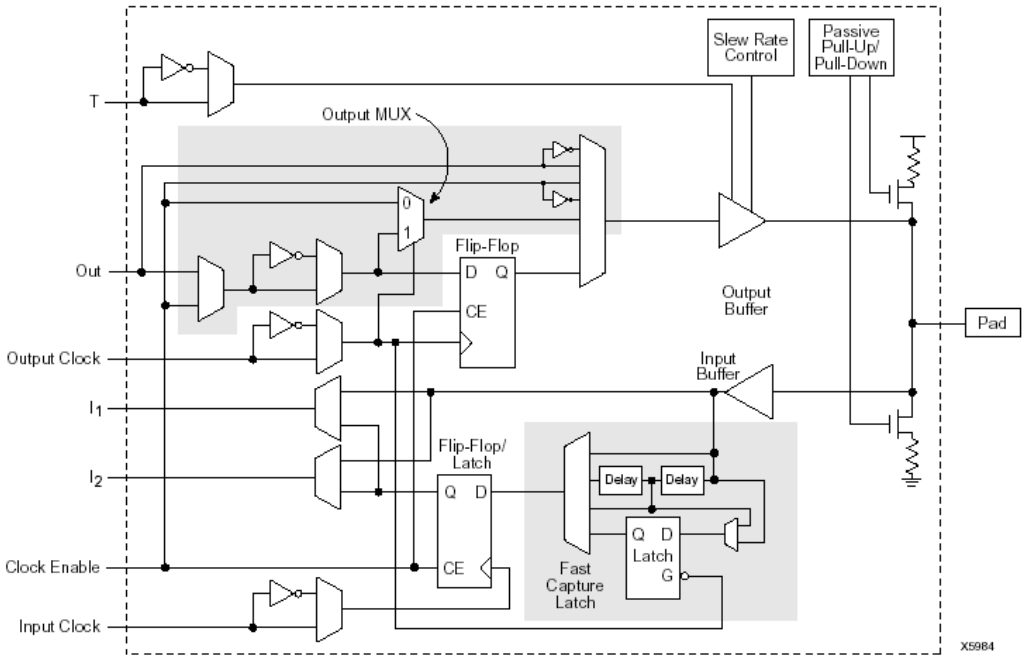
7.

（1）描述下图所示电路的工作原理

（2）计算建立时间 t_{SU}、保持时间 t_H 和传播延迟 t_{CO}，其中，钟控反相器的延迟为 t_{INV}=30ps，与门和非门的传输延迟均为 20ps。



8.描述如下图所示的电路



9.下图 FSM 的状态由 One-Hot 码编写。

（1）证明下图状态机为什么有高 placing and routing efficiency

（2）写出 state1、state2、state4 的 NS(next state)等式