ARMv8-A A64 Instruction Cheatsheet

Based on ARM Architecture Reference Manual (DDI0487)

General Notes

- Registers: `X0--X30` (64-bit), `W0--W30` (32-bit)
- `XZR/WZR`: Zero register
- `SP`: Stack Pointer
- Flags: **N** (Negative), **Z** (Zero), **C** (Carry), **V** (Overflow)
- Instructions with `S` suffix update NZCV

Arithmetic Instructions

Addition

- **ADD Rd, Rn, Rm/#imm**
  Add operands, no flags updated.
- **ADDS Rd, Rn, Rm/#imm**
  Add and update NZCV.
- **ADC Rd, Rn, Rm**
  Add with carry flag.
- **ADCS Rd, Rn, Rm**
  Add with carry, update NZCV.

Subtraction

- **SUB Rd, Rn, Rm/#imm**
  Subtract operands.
- **SUBS Rd, Rn, Rm/#imm**
  Subtract and update NZCV.
- **SBC Rd, Rn, Rm**
  Subtract with borrow.
- **SBCS Rd, Rn, Rm**
  Subtract with borrow, update NZCV.

Logical & Bitwise

- **AND Rd, Rn, Rm/#imm**
  Bitwise AND.
- **ANDS Rd, Rn, Rm**
  AND and update NZCV.
- **ORR Rd, Rn, Rm/#imm**
  Bitwise OR.
- **EOR Rd, Rn, Rm**
  Exclusive OR.
- **BIC Rd, Rn, Rm**
  Bit clear: `Rn & ~Rm`.

Shift & Bitfield

- **LSL Rd, Rn, #imm**
  Logical shift left.
- **LSR Rd, Rn, #imm**
  Logical shift right.
- **ASR Rd, Rn, #imm**
  Arithmetic shift right.
- **ROR Rd, Rn, #imm**
  Rotate right.
- **CLZ Rd, Rn**
  Count leading zeros.
- **CLS Rd, Rn**
  Count leading sign bits.
- **RBIT Rd, Rn**
  Reverse bits.
- **REV/REV16/REV32**
  Reverse byte order.

Compare & Test

- **CMP Rn, Rm/#imm**
  Compare (SUBS without result).
- **CMN Rn, Rm**
  Compare negative (ADDS).
- **TST Rn, Rm**
  Test bits (ANDS).

Branches

- **B label**
  Unconditional branch.
- **BL label**
  Branch with link (call).
- **RET**
  Return from subroutine.
- **BR Rn**
  Branch to register.
- **B.{cond} label**
  Conditional branch (EQ, NE, LT, GT, etc.).
- **CBZ/CBNZ Rt, label**
  Compare register to zero.
- **TBZ/TBNZ Rt, #bit, label**
  Test bit and branch.

Load / Store

Basic

- **LDR Rt, [Rn, #imm]**
  Load 32/64-bit.
- **STR Rt, [Rn, #imm]**
  Store 32/64-bit.
- **LDRB/LDRH**
  Load byte / halfword.
- **LDRSB/LDRSH**
  Load signed byte / halfword.

Advanced

- **LDP/STP Rt1, Rt2, [Rn]**
  Load/store pair.
- **LDUR/STUR**
  Unscaled offset.
- **LDXR/STXR**
  Exclusive (atomic).
- **PRFM**
  Prefetch memory.

Floating Point

- **FADD/FMSUB/FMUL/FDIV**
  Floating-point arithmetic.
- **FNEG/FABS**
  Negate / absolute value.
- **FCMP/FCMPE**
  Compare floating-point, update NZCV.
- **FCVT**
  Convert FP $\leftrightarrow$ integer.
- **FCVTZS/FCVTZU**
  FP to int (round to zero).

SIMD / NEON

- **VADD, VSUB, VMUL**
  Vector arithmetic.
- **VLD1, VST1**
  Vector load/store.
- **VCNT**
  Count bits per element.

System Instructions

- **MRS Xt, sysreg**
  Read system register.
- **MSR sysreg, Xt**
  Write system register.
- **SVC #imm**
  Supervisor call.
- **HLT #imm**
  Halt (debug).
- **NOP**
  No operation.
- **WFI / WFE**
  Wait for interrupt / event.
- **SEV / SEVL**
  Send event.
- **DMB / DSB / ISB**
  Memory and instruction barriers.