19/7/18

UNIT-I Basic structures of computers

Functional unit, Basic operational concepts, Bus structures, system software, performance, History of computer development.

computer types

— Digital computer

a. Input as Digital Information
b. processor - Instruction
c. Result as output
d. fast

1. size
2. cost
3. performance
4. Requirement

1. Desktop computer (or) personal computer.
2. Notebook computers
3. Work stations (or) services
4. Enterprise system
5. super computer.

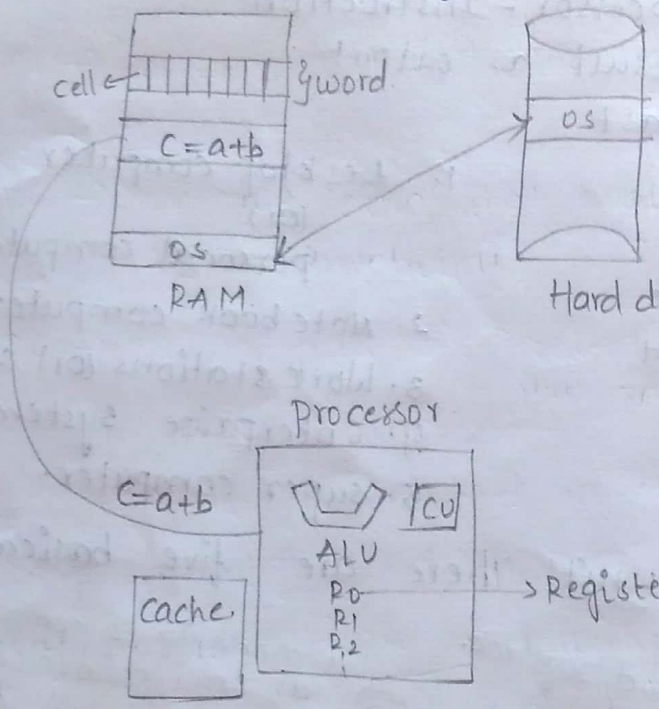
22/7/18 Functional unit:- There are five basical function -al units

(i) Input → keyboard, joystick.
(ii) output
(iii) memory → Primary → RAM (is made up of components called as semi-conductor cells.), cache, Registers (these are fast compared to secondary)
Secondary → HD, magnetic tapes, CD's, DVD's, flappy disks
(iv) processor
(v) control unit.

→ The cells, count are called as word.
→ the word has word length -16 to 64 cells
→ each cell can store 0's, 1's information.
→ In olden days, in RAM 10's of thousands of millions of words, Now a days in RAM 100's of thousands of millions of words
→ Every word is having unique address/location.
→ The important communication happens between memory and processor.

→ Any time the processor can acess reading any adress location for reading (or) writing data so main memory is called as RAM (Random access memory)

→ The time required to read (or) write data from memory is called memory access time. That will be generally nano seconds



→ The need of registers is when we store values in register ~~we~~ when wee need value we donot need to go to memory they can be available in register it self.

→ Register's are limited, we cannot have more than 16, Registers and the cost is high.

→ when Register's are filled the ~~registers~~ processor call's those ~~are~~ value from cache memory.

→ cache memory always maintain's a duplicate of registers

→ registers are present in processor & cache memory is close to processor.

→ These are not fast but helps to get faster.

→ control unit acts like co-ordinator. It co-ordinates all our hardware components

→ control unit is responsible at what clk signal component works

→ control unit is wired timing signal to all it's hardware components

→ In a single unit of clk cycle the printer can print 10,000 lines of code.

→ But processor is faster than printer.

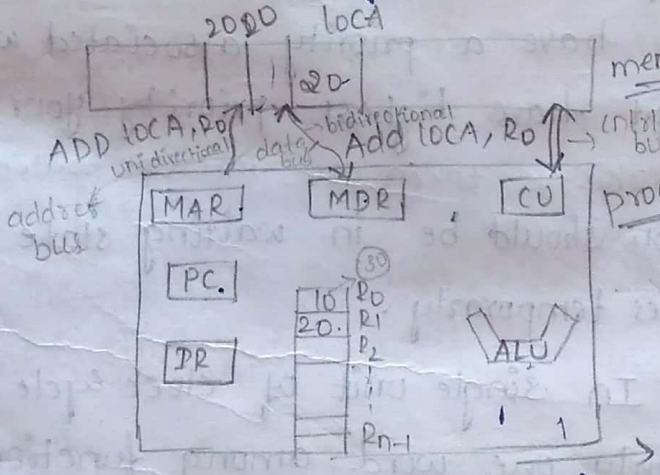
(Registers → cache memory → memory) this is speed hierarchy (or) memory hierarchy

23/11/18 **Basic operational concept:-**

↳ memory location.

Eg: ADD LOCA, R0

→ Add the components in the location A and store it register R0.



→ The components in memory location does not change but the components in registers are overwritten

→ load LOCA, R1
Add R1, R2

→ C.U acts like timing signal.

1) MAR - Memory address register.
2) MDR - Memory data register.
3) PC - Program counter.
4) IR - Instruction Register.
5) 'n' general purpose registers.
6) control unit.

R0, R1, ... Rn-1 are called as n-general purpose registers

→ cu knows the next instruction.

→ control unit places the address of next instruction into program counter

→ From processor MAR is only directly connected to memory.
It is only having pointer to MAR-memory

→ Here in ADD LOCA, R0 we donot know LOCA to find that MAR is connected to memory LOCA is at 2000 addrees then 20 is moved to MDR then it is stored at regisiter R0

→ MAR → contains next instruction address it is unidirectional

MDR → contains data that may be value/Instruction
It is bidirectional.

IR → It contains the present instruction. in that particular unit of clock cycle.

→ CU is also bidirectional.

→ Add LOCA, R0 is decoded in MDR which cannot be done in single unit of clock cycle.

→ Every interupt have a priority associated with it

→ If the interupt have highest priority your next is interupt ↓ This is taken care interupt routine.

→ present instruction should be in waiting state that stores all it values temporarly.

24/4/18 Bus structures:- In single unit of clock cycle we can transfer only one word among functional units. [Word = 16 bits]

→ All the 16-bit information should transfer parllely. means 16-wires transfer parllely.

→ Then we call that collection of wires as Data bus.

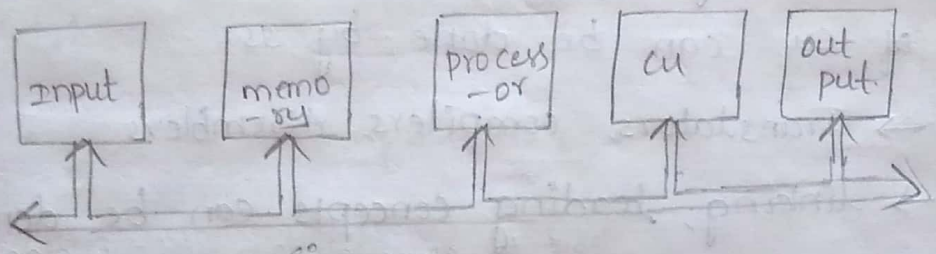
→ we can transfer multiple words in single unit clock cycle if we have multiple data buses

but the disadvantage is the cost is high.

→ If we transfer multiple words (i.e; multiple programs) in single unit of clock cycle then it is called concurrency

→ It always better to have single data base so that cost is low.

Single bus architecture:-



→ Single bus is combination of data bus, control bus and address bus.

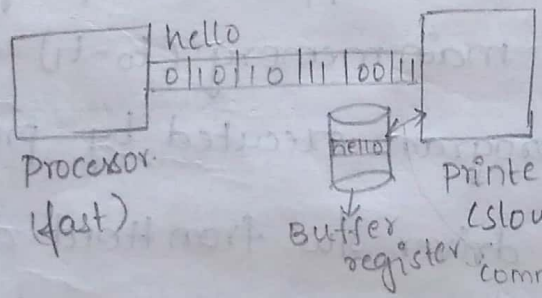
eg:- processor giving sequence of characters to printer

→ processor is fast printer is slow.

→ Speed match between processor & printer

→ Effective utilisation of processor fails (∵ since processor has to wait until printer prints) result is

The solution for this is provided by Buffer register which is capable of storing one word.



System software:- Better example for system software is OS (operating system)

→ The role of OS is Booting

→ It is also responsible for controlling control unit

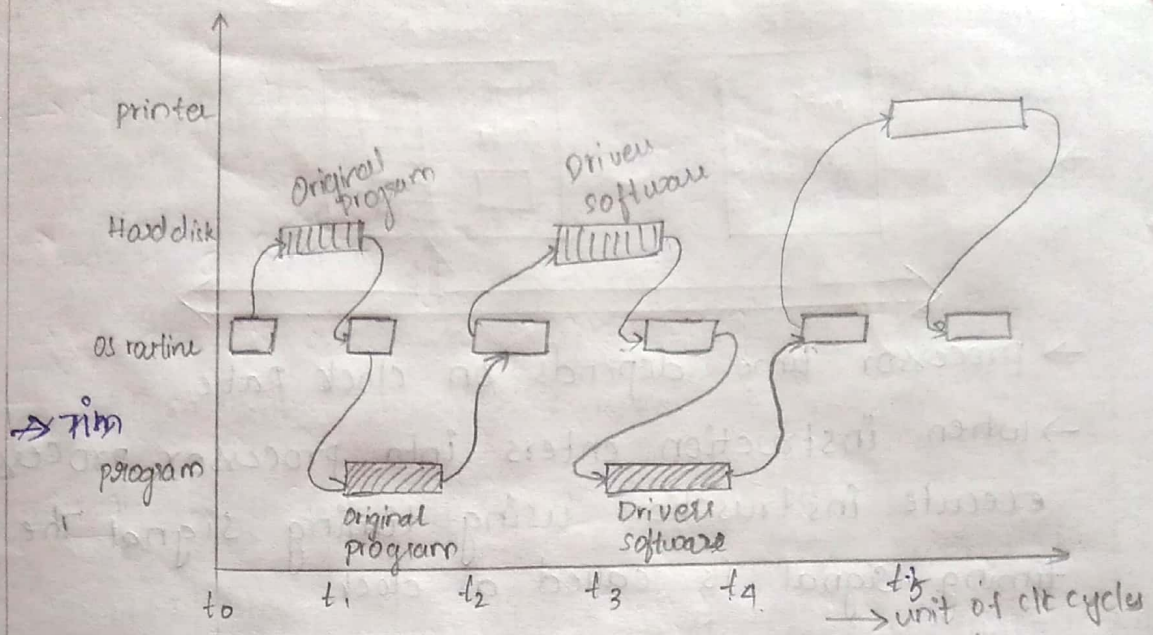
26/4/18 → commands execution is possible (eg:- edit ...)
→ Data can be moved from Hard disk to main memory using s.s
→ Main memory to Hard disk data movement is possible.
→ It gives support to excel, word processor ....
→ Working of control unit i.e., Intialising duties of cu can be done by ss.
→ Translators, compilers, Assemblers.
→ linking, loading concepts can be done by s.s
→ Text editor (able to store alpha numeric characters in harddisk) is also a ss [note pad]
→ File is also a ss.

Advantages:- [os]

Eg:- Program has to print by printer.

Requirements:- program
os routine
Hard disk
Printer

① Os Routine takes Application program from Hard disk to main memory (t_0-t_1)
② Application program executed by processor (t_1-t_2)
③ store printer driver s/w from Hard disk to main memory (t_2-t_3)
④ processor has to execute the instruction of driver s/w. (t_3-t_4).
⑤ printer starts printing (t_4-t_5)



time required to complete the task is $t_5 - t_0$. This is called elapsed time.

→ Time required $= t_5 - t_0$

This is called elapsed time.

→ In the period of $(t_4 - t_5)$, the processor, memory, IDLE we can use these to execute other tasks.

→ In $t_0 - t_1$ time we can use processor for other task. this is called multi-tasking (or) Multi-programing.

Skills

performance:-

It depends on.

- Quick
- compiler.
- Machine Instructions
- Hardware components
- co-ordination is good.
- Elapsed time.

→ Elapsed time depends on processor time.

→ cache memory ↓ processor time ↓

1. **processor time:-**

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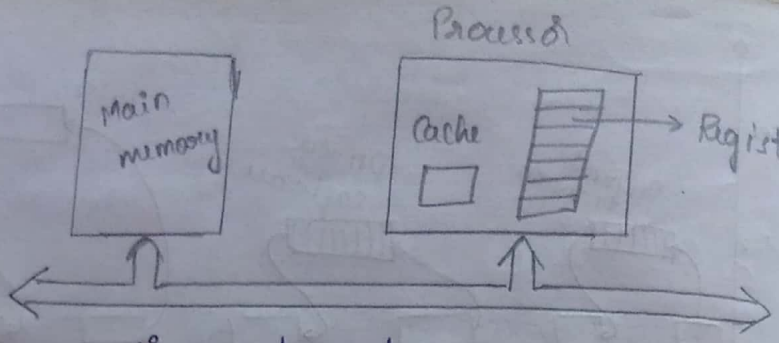

→ processor time depends on clock Rate.

→ when instruction enters into processor, processor execute instruction using timing signal. The timing signal is called as clock.

→ If P is (or) No. of length of instruction, R is clock Rate

$$R \propto \frac{1}{P}$$

If $P \uparrow \Rightarrow R \downarrow \Rightarrow$ processor slow

If $P \downarrow \Rightarrow R \uparrow \Rightarrow$ processor fast

1 Million = 1M
1 Billion = 1G

$$500\ MHz = \frac{1}{500MHz\ (length)} = 2ns\ (R)$$

$$1250\ MHz\ (1.25\ GHz) = \frac{1}{1250\ MHz} = 0.8ns$$

2) Basic performance equation

$$T \propto \frac{1}{R}$$

$$T = \frac{N \times S}{R}$$

T - processor time ↓
R - clock Rate ↑
N - No. of instructions ↓
S - Avg time required to execute instruction
Avg no. of basic steps ↓
Step - unit of clock cycle.

MM - processor

Processer time depends on S

3. Pipe lining & Super scalar operation:-

Assume S = 1

⇒ executing more than one instruction in a single

unit of clock cycle depends on hardware components are called pipe lining or super scalar operation.

→ when processor is busy with executing instruction

Add R_1, R_2, R_3 # $R_1 + R_2 \rightarrow R_3$

→ At this time memory, system unit are in IDLE state.

→ At this time if next instruction is moved from MM to cache memory (or) processor using bus then this is called executing several instructions in a single unit of clock cycle (or) pipe lining (or) super scalar operation (or) multitasking.

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4. Clock Rate:-

To increase the clock Rate perform the below

⇒ Change the integrated circuit technology i.e; we need to use the advanced IC technology in processor.

→ Reducing the length of the instruction (or) have simple instructions

$P \downarrow \rightarrow R \uparrow \rightarrow T \downarrow \quad [\because R = \frac{1}{P}]$

5. Instruction set:-

To write a program we have complex instruction set & simple instruction set.

For example,

factorial

complex (Recursion)
N ↓ - S ↑

Simple (Non-Recursion)
N ↑ - S ↓

N - High level language instructs
S - tracing
Ng.
↳ factorial using loop.
No. steps less
small no. basic steps
so steps more.

RISC - Reduced Instruction set - simple

CISC - Complex Instruction set

$N \alpha \frac{1}{S}$

6 compiler:-

→ It is always better to have N ↓ & S ↓ to ↑ ↓ but it is not possible.

⇒ It is possible if you have proper compiler.

⇒ If compiler is more efficient then the system will work faster.

⇒ Machine level languages are o/p of the compiler in the memory

⇒ compiler converts high-level language instructions into Machine-level language instructions according to memory grammer

⇒ It is always better to have less no of instructions & very simple instructions i.e., N↓ & S ↓

⇒ N belongs to memory & S belongs to processor.

7. performance measurement:-

$$\text{Spec Rating} = \frac{\text{Running time required for Reference computer.}}{\text{Running time required for Testing computer.}}$$

⇒ we can't measure processor time exactly because all the caluclations we do are estimations

⇒ For these reasons, the computer community adopted the idea of measuring performances using bench-mark programs (standardized programs)

⇒ All these standardized programs are kept in one reference system.

⇒ System performance -ed on this whic performance of the

⇒ Spec 95 worked -n w/40.

Spec 2000 worke

It spec Rating = times faster for n program

Spec Ratin

solution includes all compiler, user de

Multi processors

Multi processor

The execution using multiproc

In a single -truction is multiprocessor

Multicomputer A

suppose, execute.

Step 1:- Divide

Step 2:- Assign another

These com architecture

⇒ System performance Evaluation concept (spec) perform -ed on this which is used to measure the performance of the system.

⇒ spec 95 worked on the system SUN SPARC statio -n w/40.

Spec 2000 worked on the system ultrasparc 10

It spec Rating = 50 it means test computer is 50 times faster than reference computer.

for n programs,

$$\text{Spec Rating} = \left(\prod_{i=1}^{n} \text{spec}_i\right)^{1/n}.$$

solution includes all computer programs like as program, compiler, user defined programs.

Multi processors and Multi computers:-

Multi process or Architecture:-

The execution time for one or more instructions using multiprocessor is very less.

In a single unit of clockcycle more than one ins -truction is fetched from memory to the multiprocessor so that speed is high.

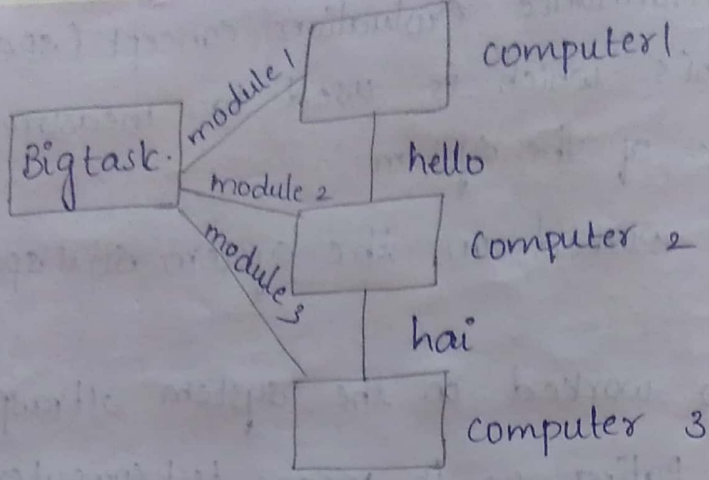
Multicomputer Architecture

Suppose, I have complex (or) big program to execute.

Step 1:- Divide big program into modules

Step 2:- Assign some set of modules to computer 1 & another set of modules to computer 2.

These computers can exchange messages this architecture is called Multi computer Architecture.



History & development of computers:-

⇒ Before 300 years, mechanical components are used to caluclate addition, subtraction, multiplication & division, logorthemic & trignometric functions

Eg:- gear wheels, lever, pulleys.

Results here punched on cards

⇒ After that electro-mechanical components are used

Eg:- Telephone mechanism systems.

⇒ electronic computers were designed & built at university of pennysl vania based on vaccume tube technology used in radios, military radar equipments

⇒ Based on development technologies used in Fabrication of memory, processor, i/o devices. computers are developed into 4 generations

1) 1st generation 1945-1955

2) 2nd generation 1955-1965

3) 3rd generation 1965-1975

4) 4th generation 1975-present.

1st generation :- (1935-1945)

⇒ To write programs Assembly language is used.

⇒ Arithmetic operations are performed in milli seconds using vaccum tube technology.
⇒ This based on electronic technology.
⇒ I/o are used as type writers
⇒ memory is developed by mercury delay line.
⇒ storing data in memory is introduced by John van Neumon.

2nd generation:-

⇒ Transistors were introduced at AT&T Bells labs.
⇒ This is replacement for vaccum tubes.
⇒ Magnetic drums are used as secondary store devices
⇒ to write code high level language is used
Eg:- FORTRAN
⇒ compilers were introduced
⇒ IBM is the source for 2nd generation of computers.

3rd generation:-

⇒ Integrated circuits was introduced
⇒ Many Transistors on a single silicon chip is called Integrated circuit
⇒ This technology is used to develop memory & processor.
⇒ os has been developed.
⇒ cache & virtual memory are introduced
⇒ IBM system 360 comes under this generation.
⇒ DEC-PDP mini computer is developed in this generation

5/12/18 4th generation:-

⇒ very large scale Integrated circuit Technology.
⇒ Eg:- Desktop computers, laptops, workstations
⇒ Application of 4th generation is Internet, LAN, WAN.
⇒ If more than one computer connected together to exchange data (or) information is called LAN

⇒ communication blw one or more computers using Internet - VAN.

⇒ cloud computing, high performance, distributed comp. pipe lining was used in this ~~effi~~ generation.

⇒ Artifical Intelligence & II computers are used in this generation.

1. Mechanical components → Electro mechanical components.
   Electronic components (vaccum tubes - transistors.
   integrated circuits - VLSI)

→ seconds - milliseconds - nano seconds - Electronic speed