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VERSION	A. 0
DATE	2014. 04. 05
DESIGNER	

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SH01 - COVER SHEET

SH02 - OPTIONS

SH03 - FPGA_BANK0

SH04 - FPGA BANK1

SH05 - FPGA BANK2

SH06 - FPGA BANK3-DDR3

SH07 - FPGA_CONFIG

SH08 - FPGA_POWER

SH09 - DVI1

SH10 - DVI2

SH11 - VGA

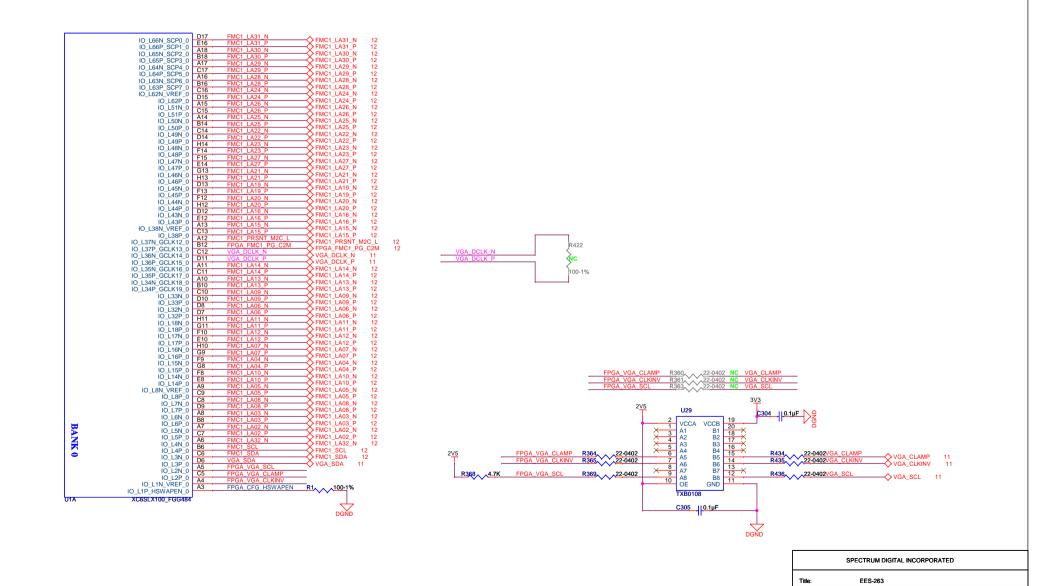
SH12 - FMC LPC1

SH13 - FMC_LPC2

SH14 - GPIO

SH15 - POWER IN

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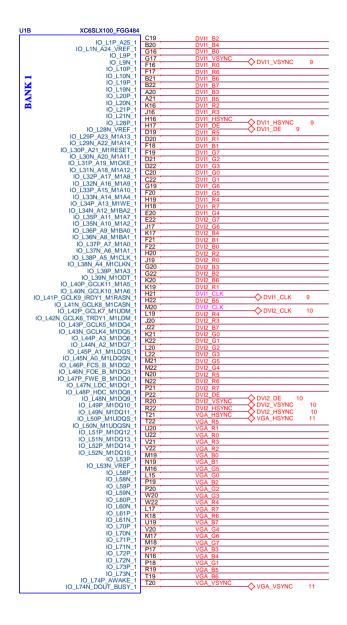
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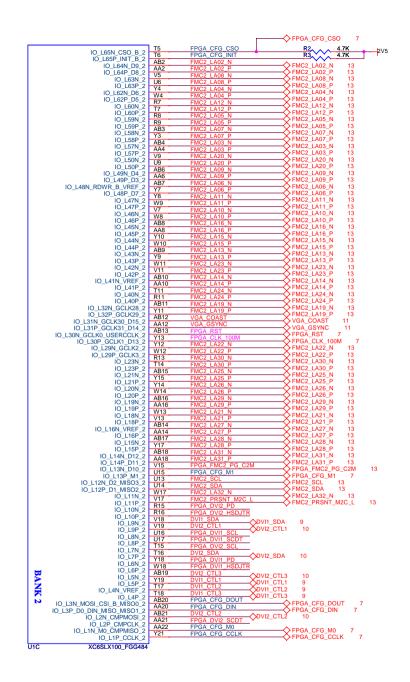
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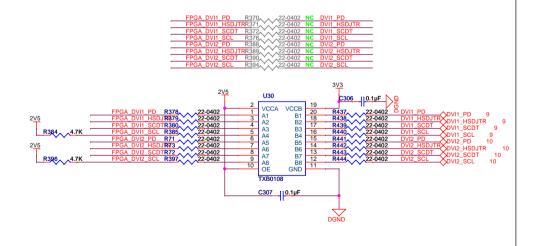


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DVI2_B[07] DVI2_G[07] DVI2_R[07]	DVI2_B[07] DVI2_G[07] DVI2_R[07]	10 10 10
VGA_R[07] VGA_G[07] VGA_B[07]	VGA_R[07] VGA_G[07] VGA_B[07]	11 11 11

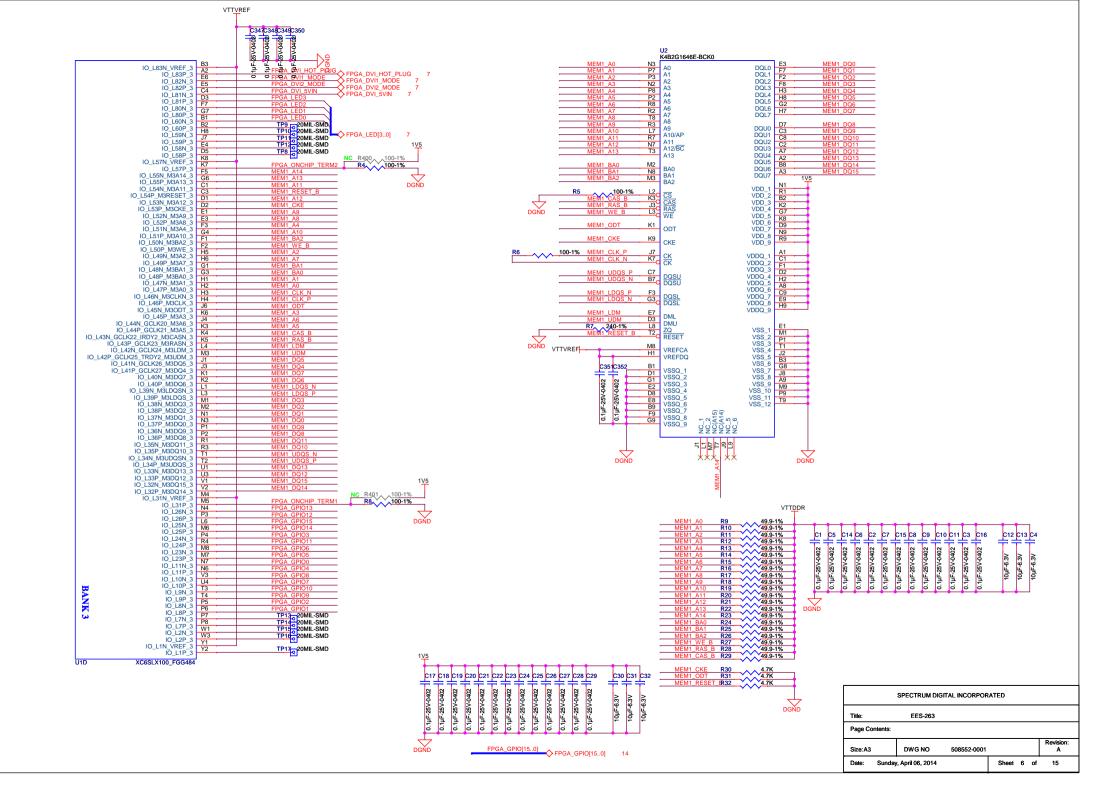
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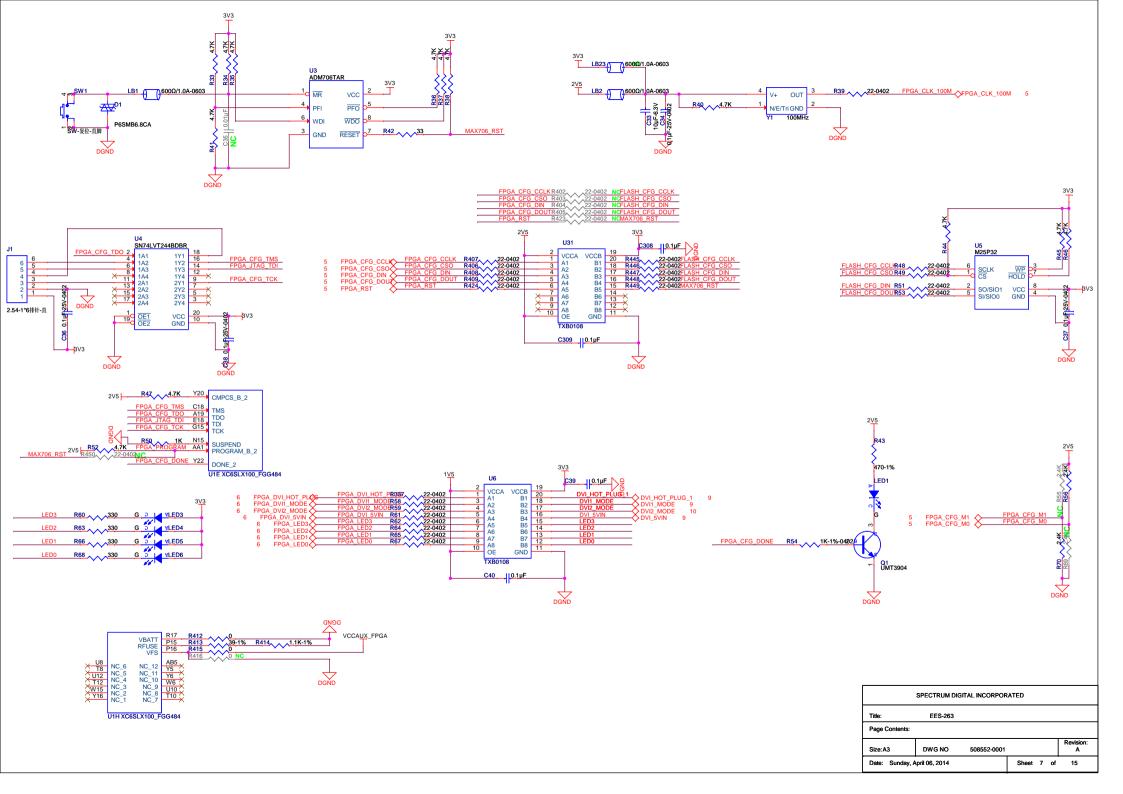
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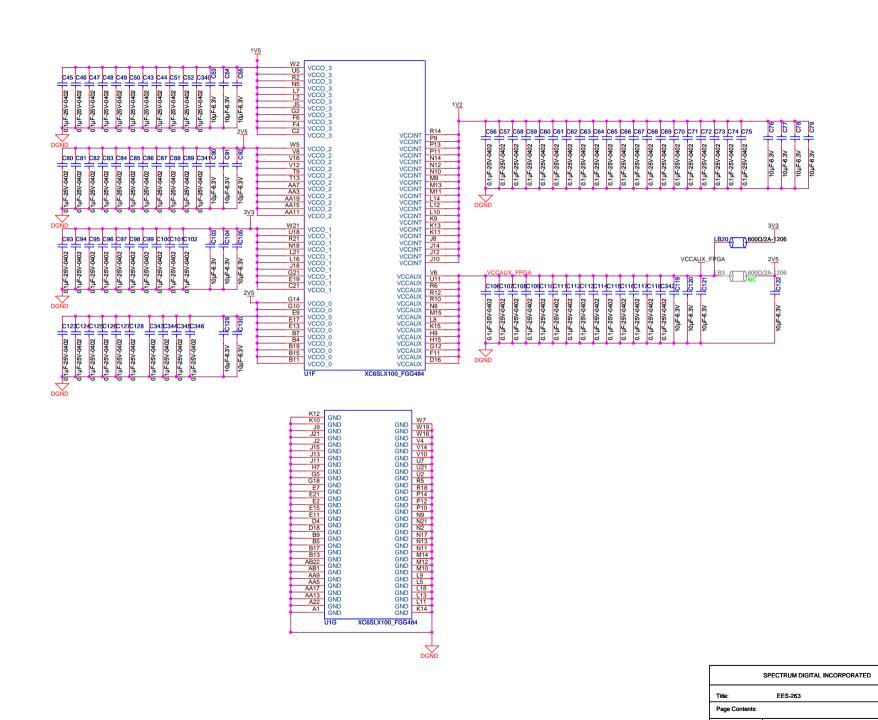




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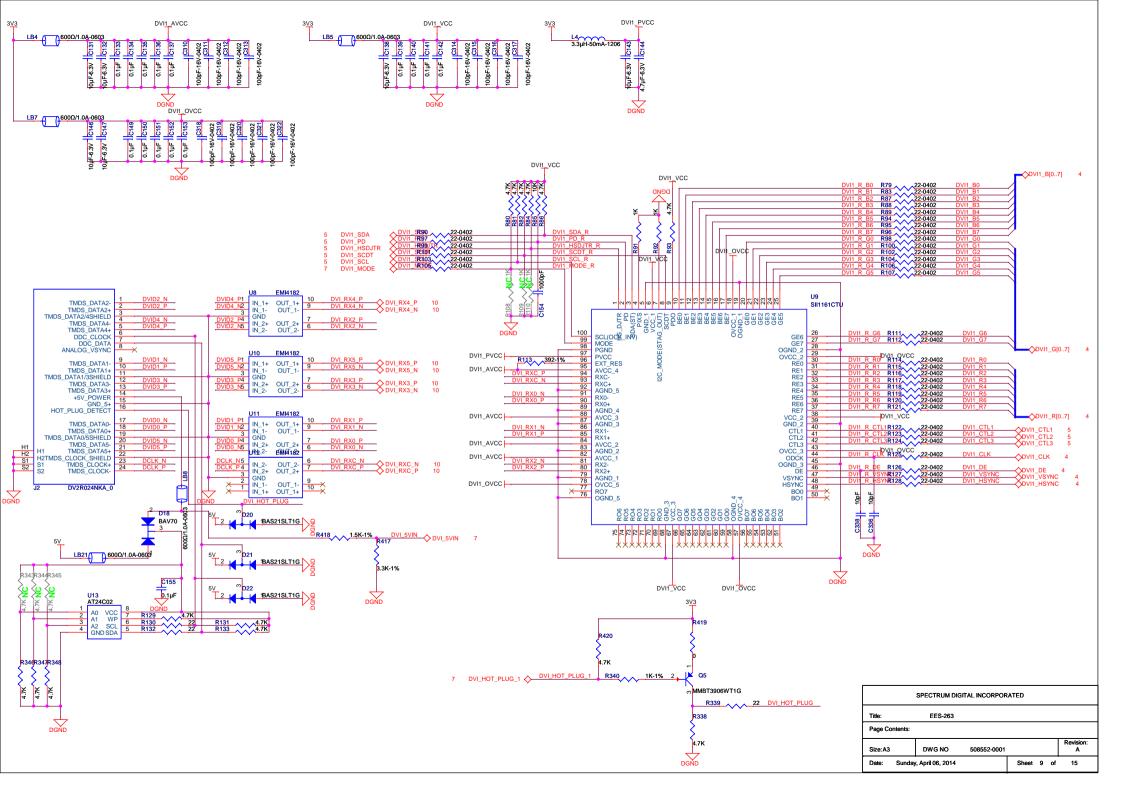
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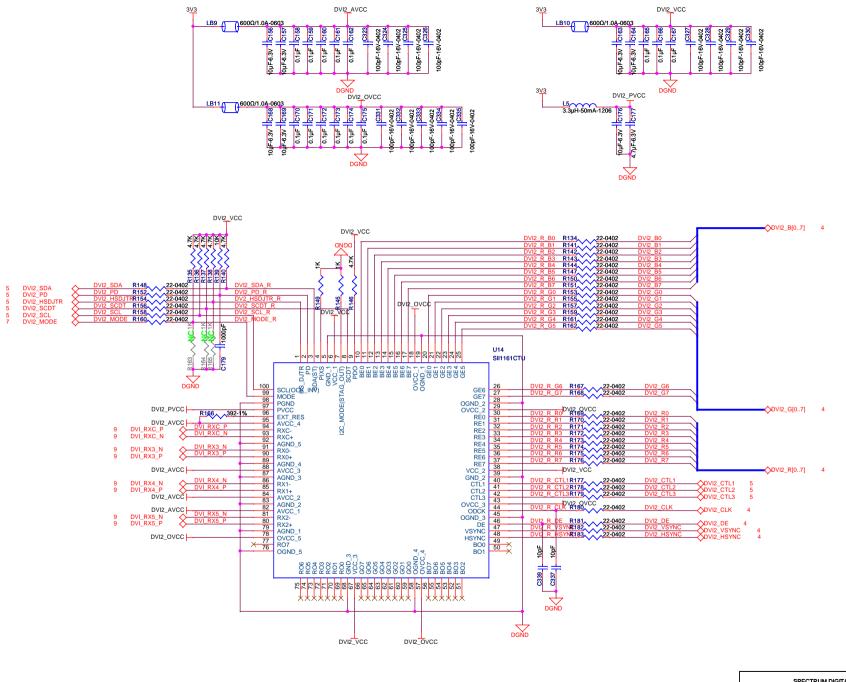
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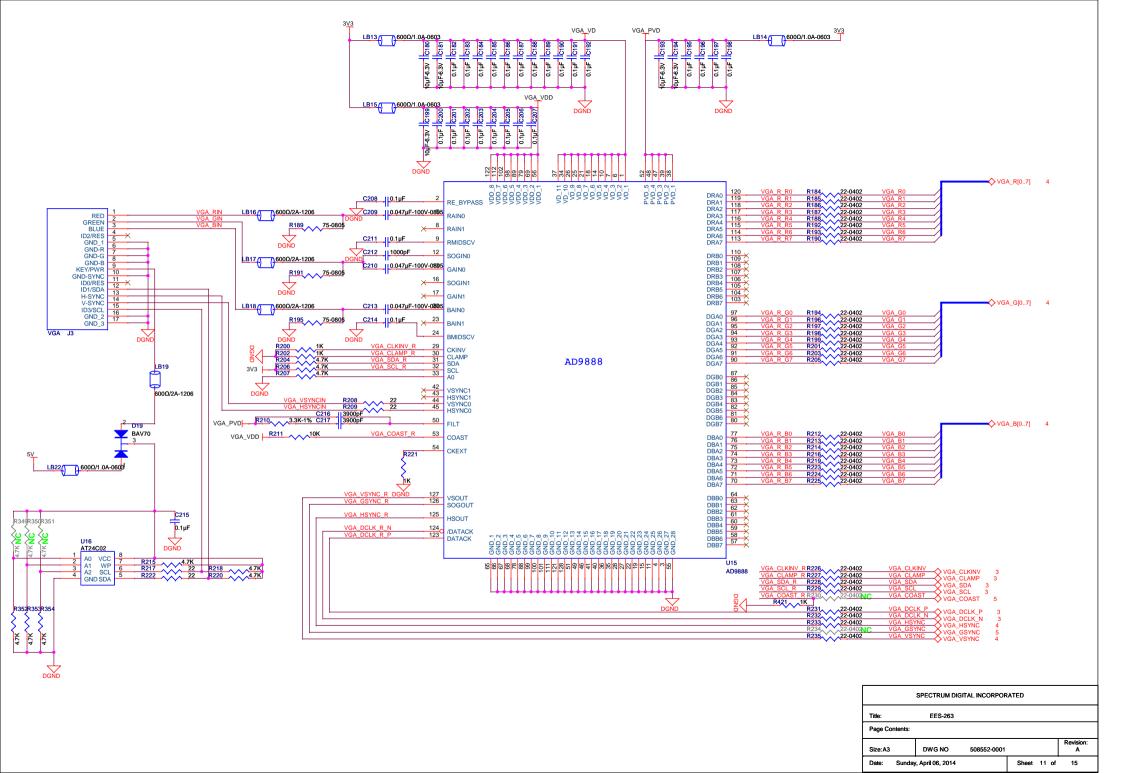
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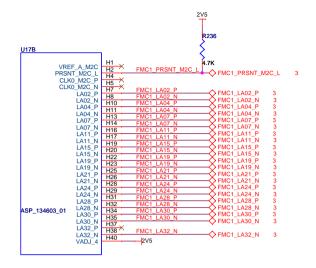
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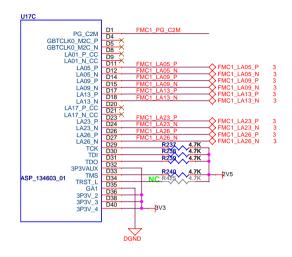


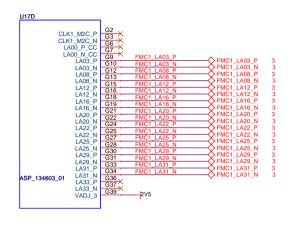


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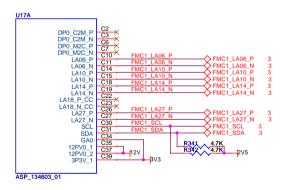
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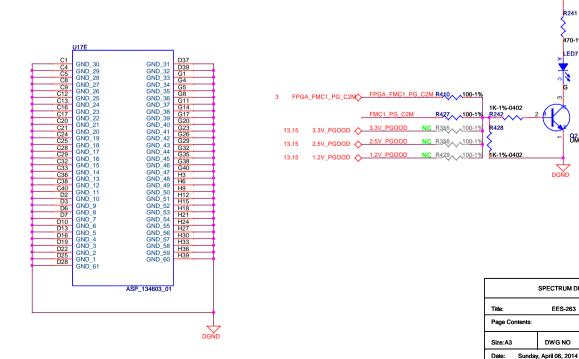
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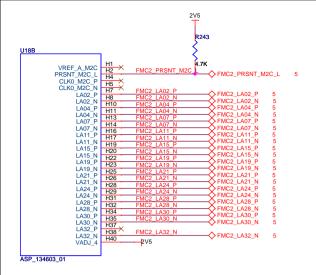
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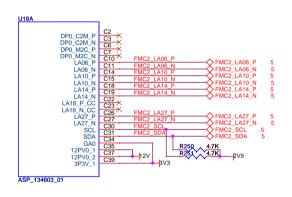
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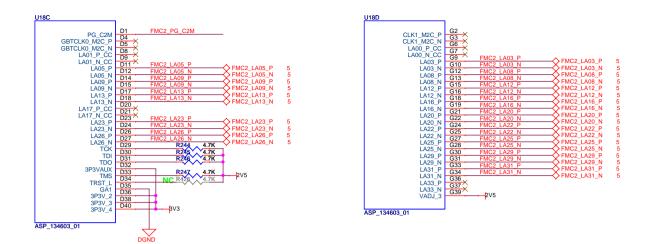
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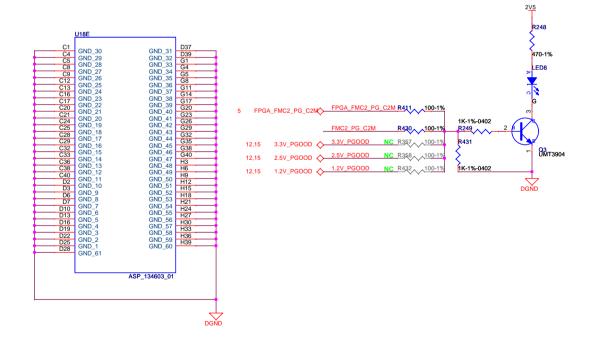




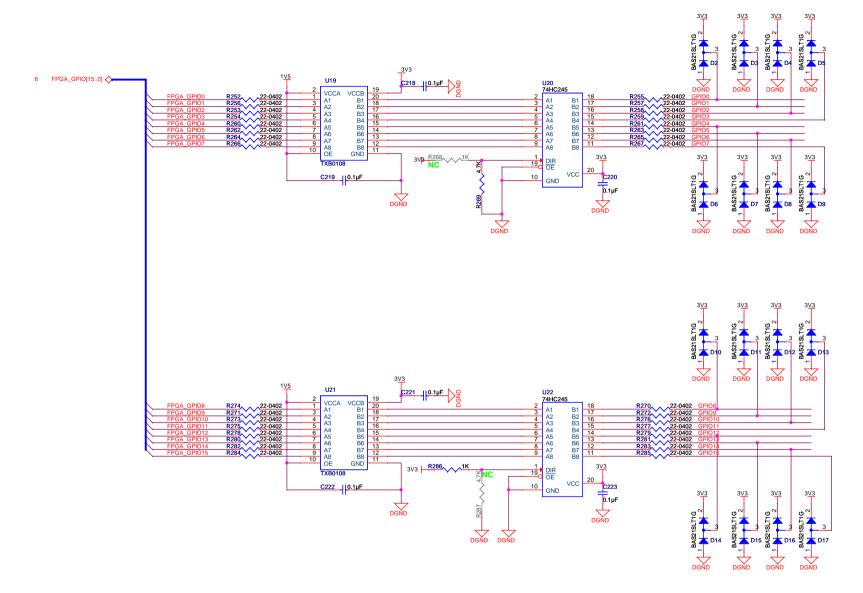


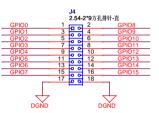






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