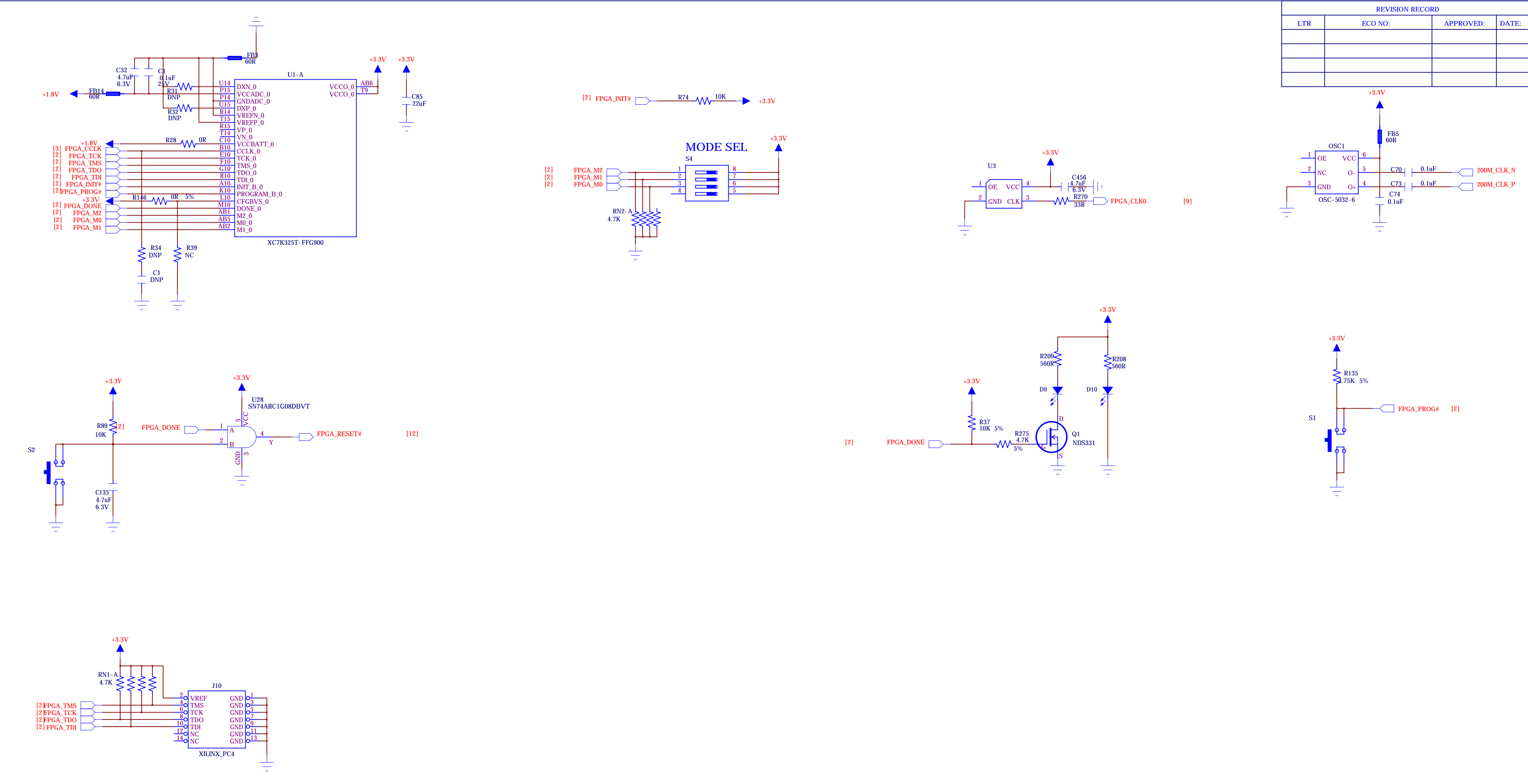


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12	BANK18_DVI				
13	FPGA_POWER				
14	POWER_SUPPLY1				
15	POWER_SUPPLY2				

	TITLE:			
DRAWN:	DRAWING NO:			
CHECKED:				
QUALITY CONTROL:				
STANDARDIZED:	VERSION:	SIZE:	SCALE:	SHEET: OF
RELEASED:	E-Elements technology Co., Ltd.			

Table 2-1: 7 Series FPGA Configuration Modes

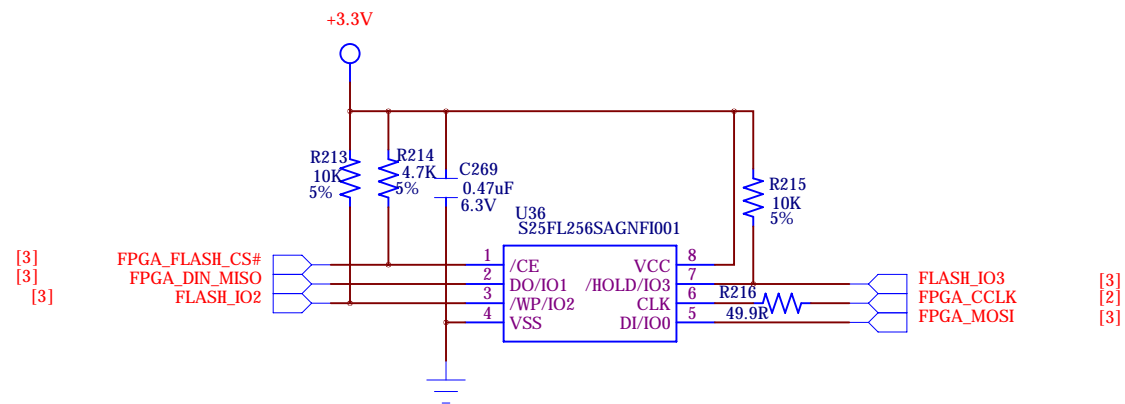
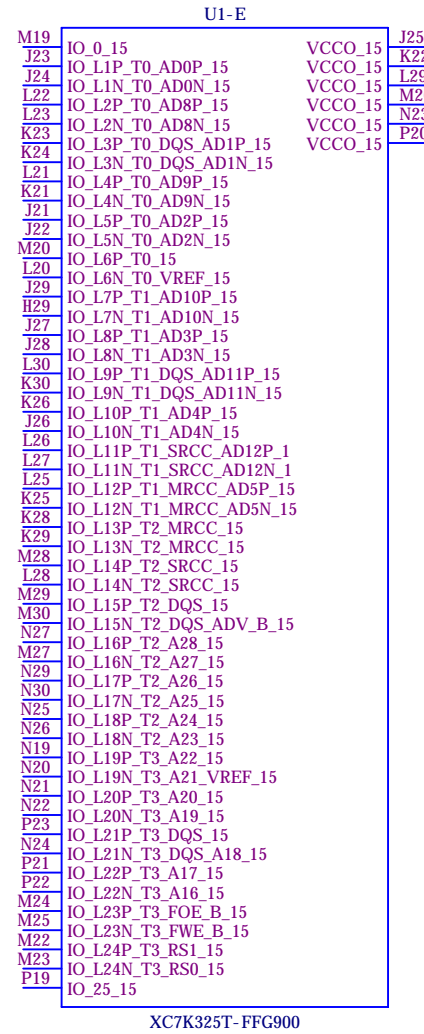
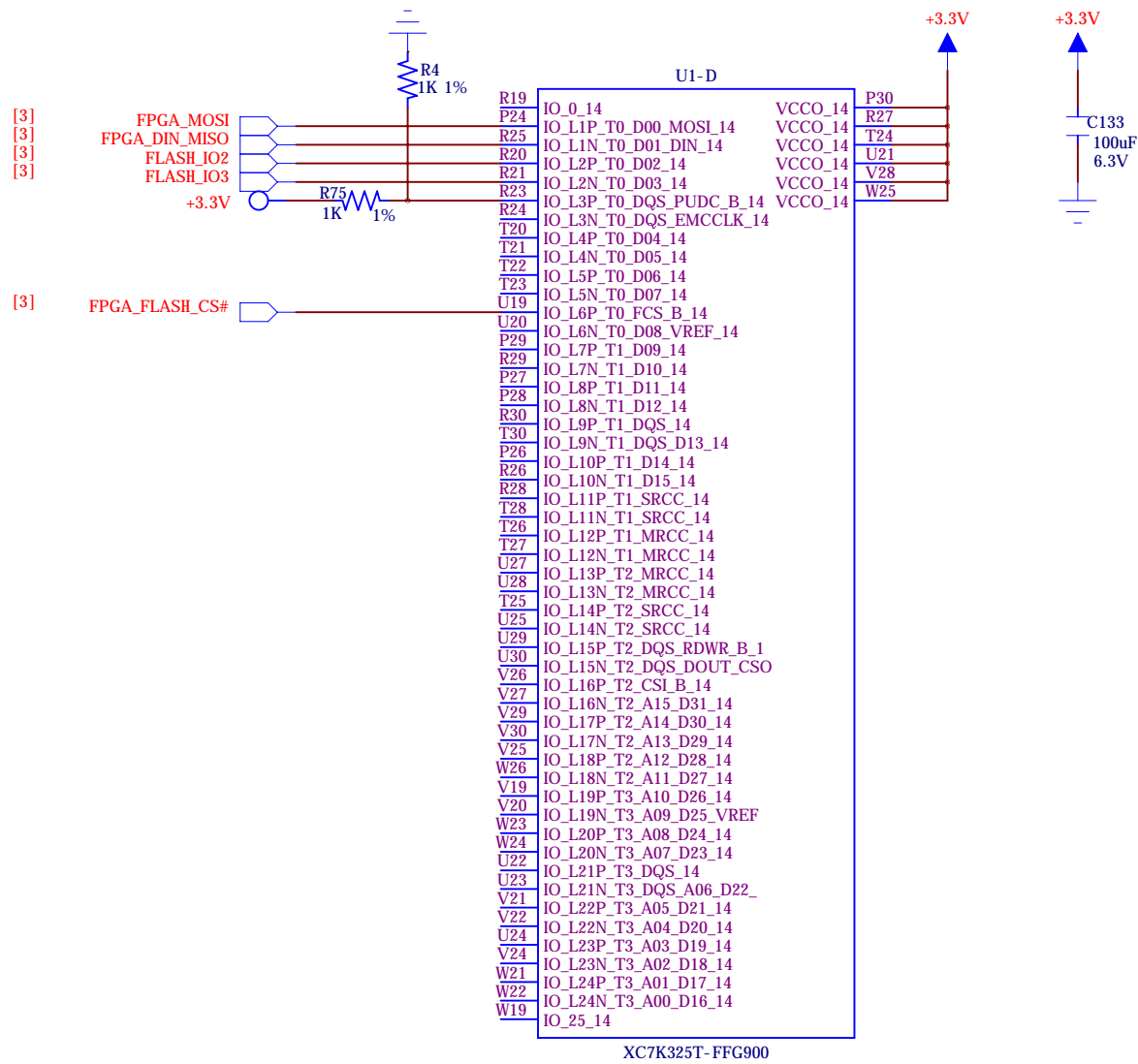
Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	x1	Output
Master SPI	001	x1, x2, x4	Output
Master BPI	010	x8, x16	Output
Master SelectMAP	100	x8, x16	Output
JTAG	101	x1	Not Applicable
Slave SelectMAP	110	x8, x16, x32 ⁽¹⁾	Input
Slave Serial ⁽²⁾	111	x1	Input



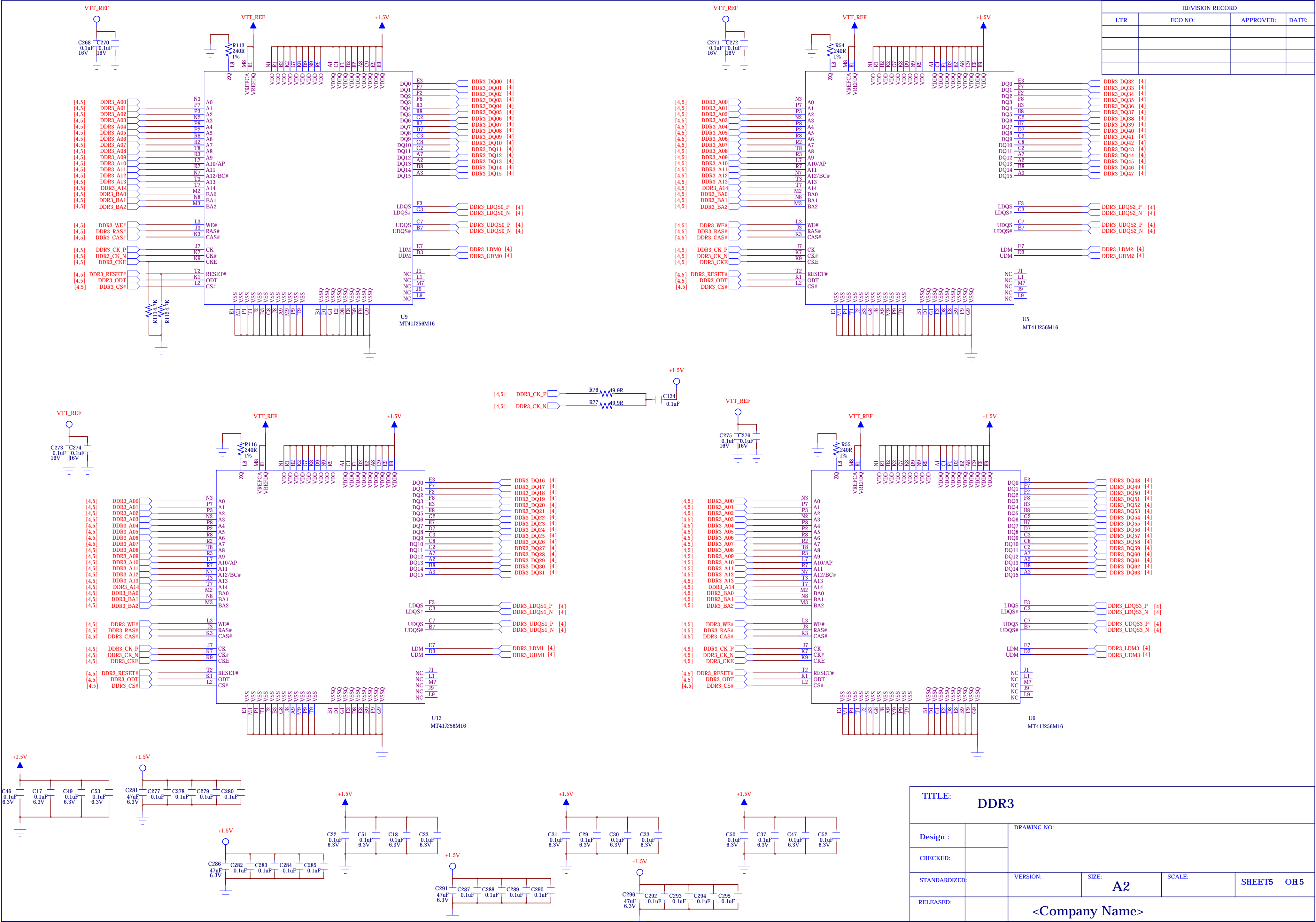
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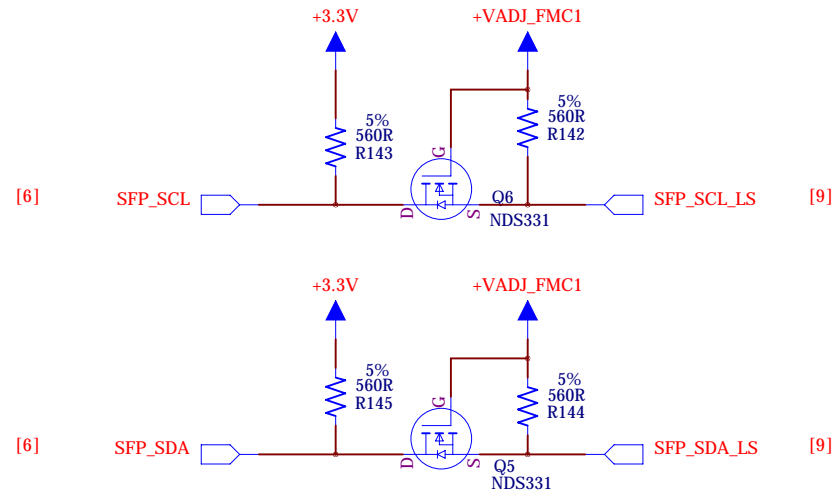
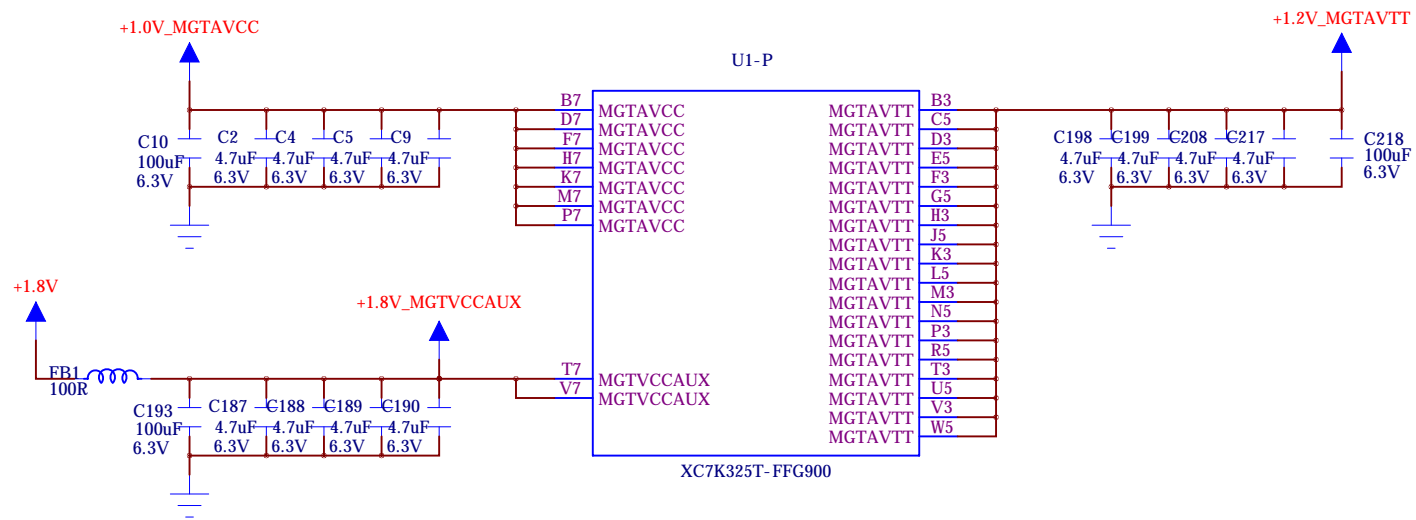
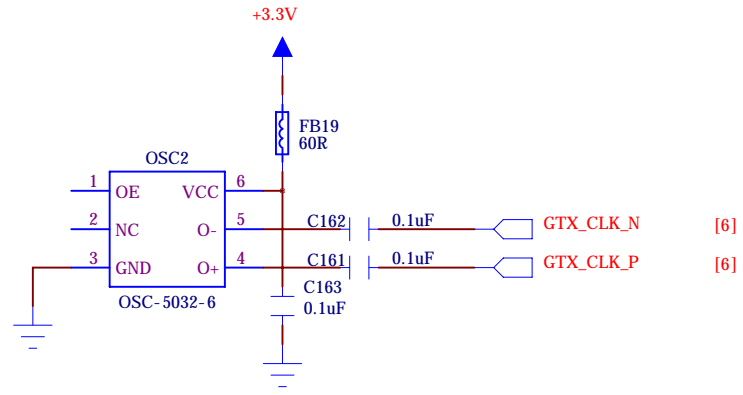
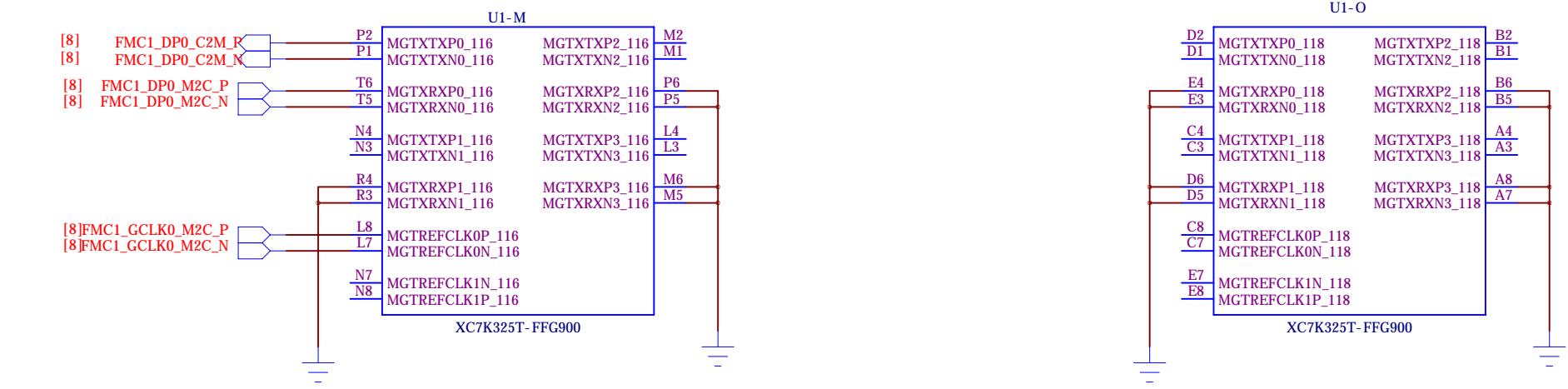
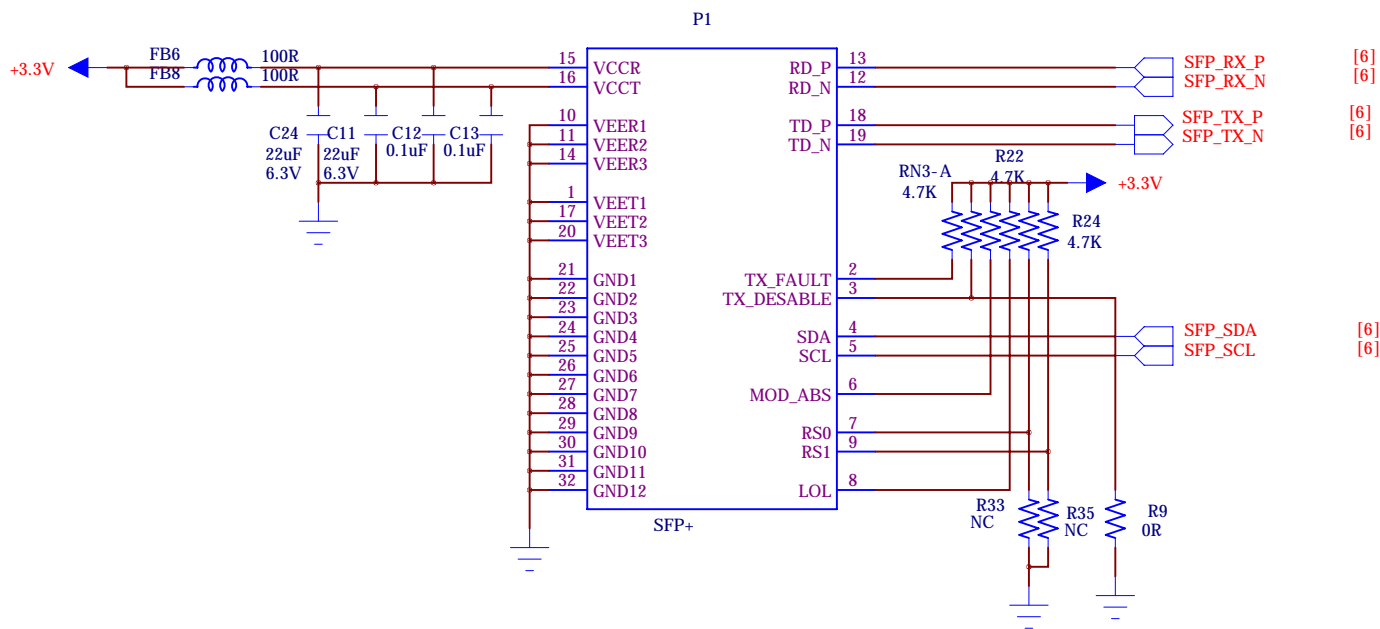
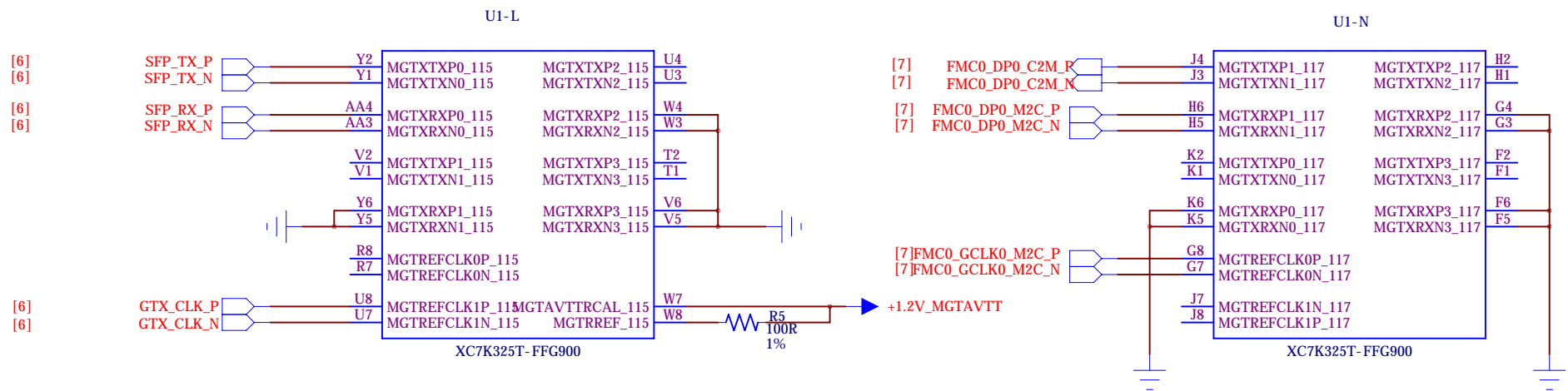
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CHECKED:					
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RELEASED:		<Company Name>			



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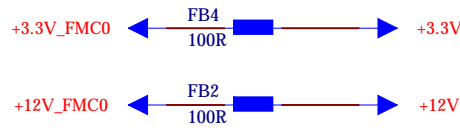
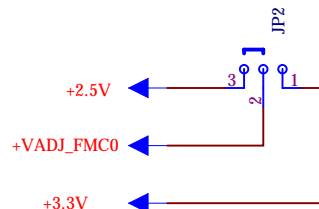
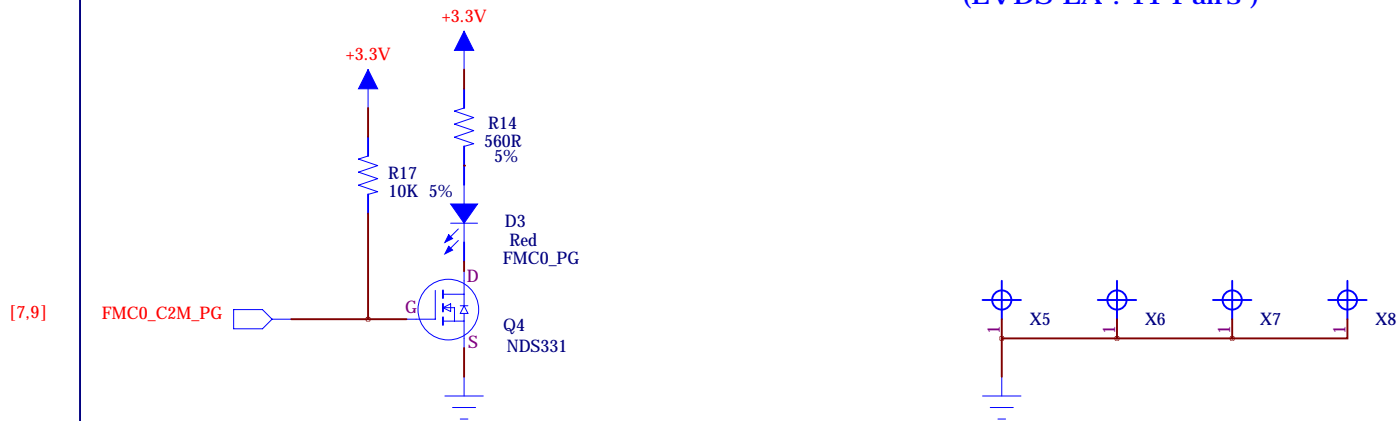
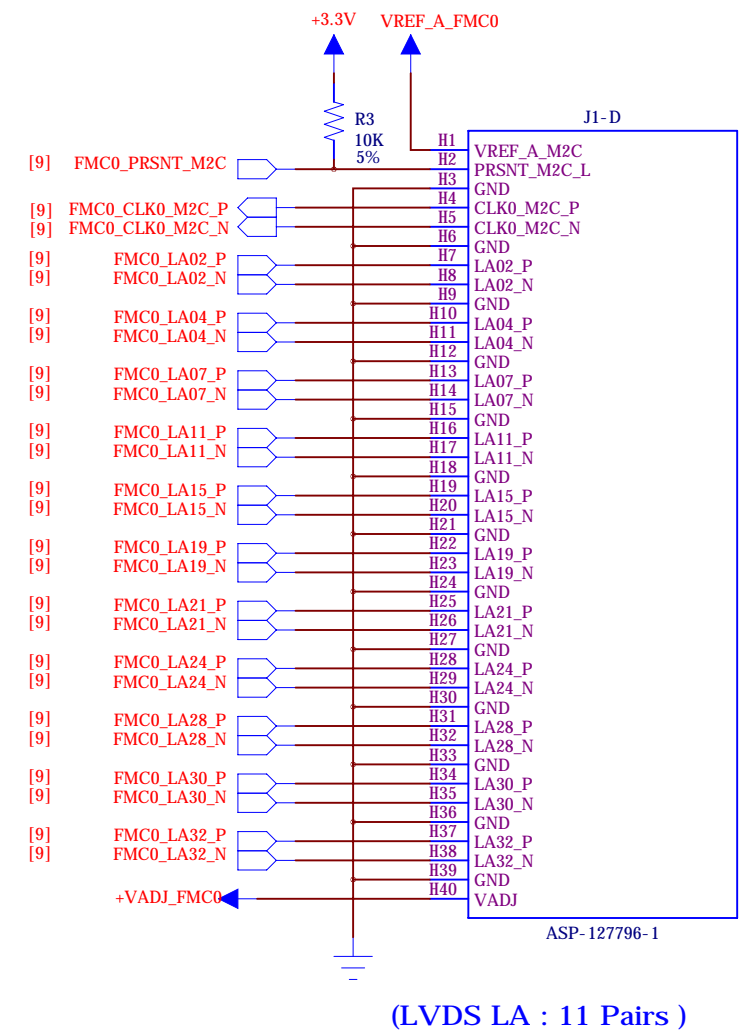
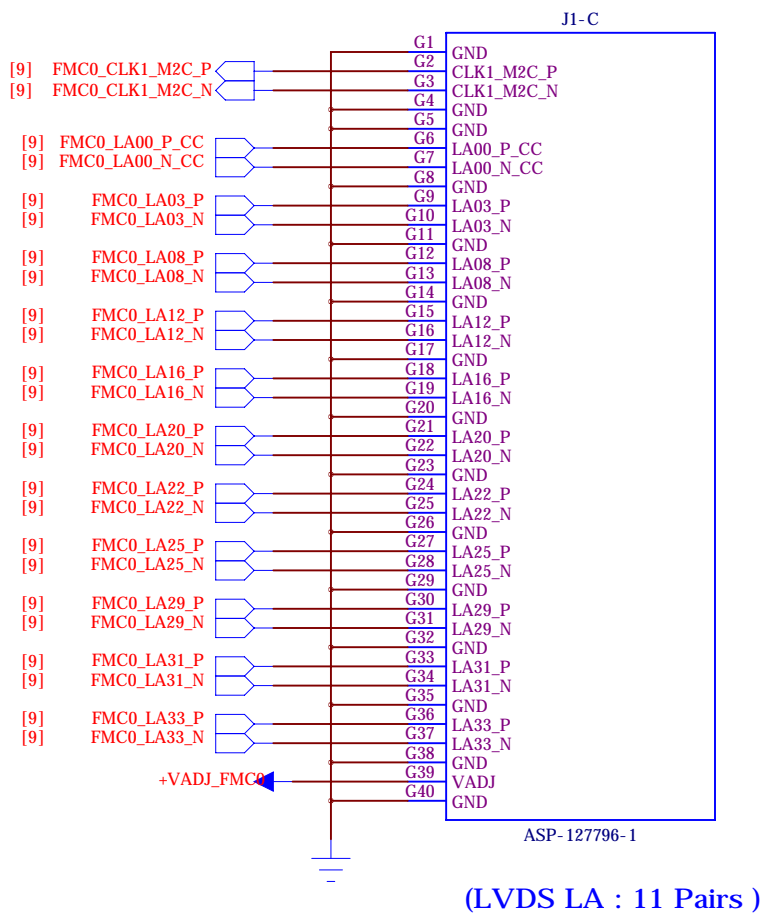
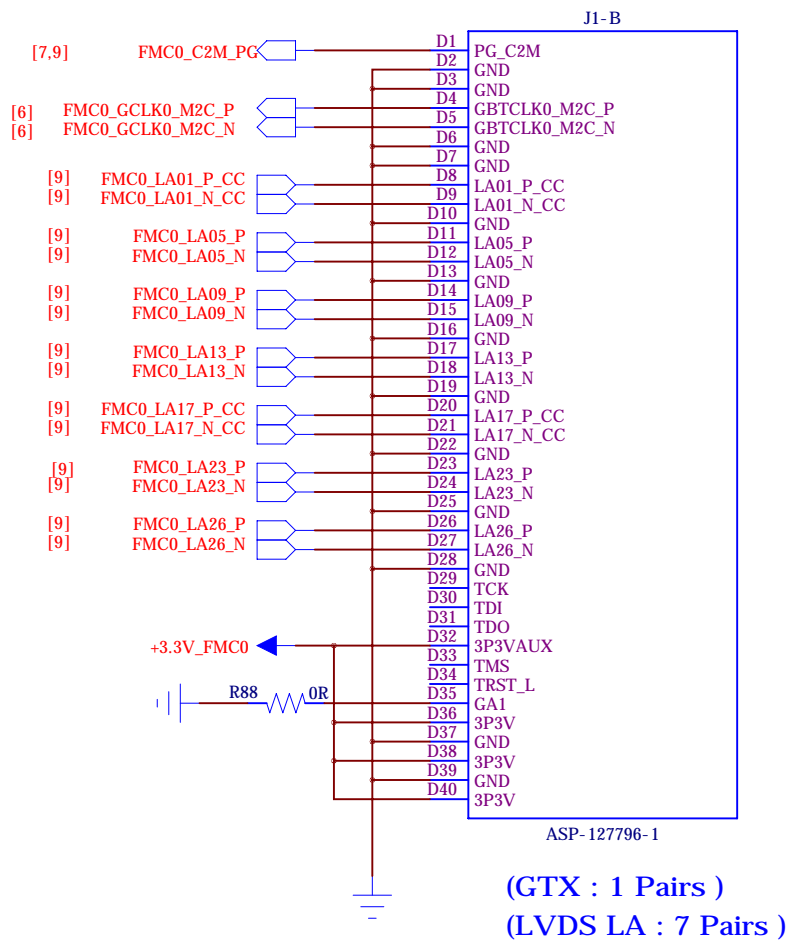
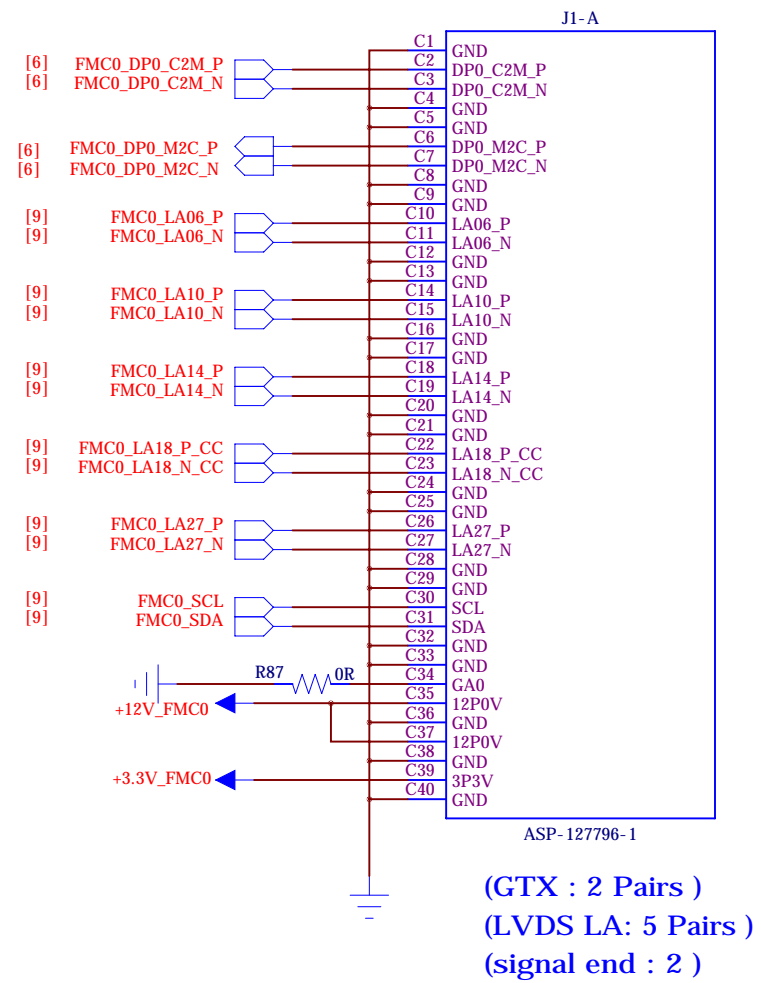
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LTR	ECO NO:	APPROVED:	DATE:



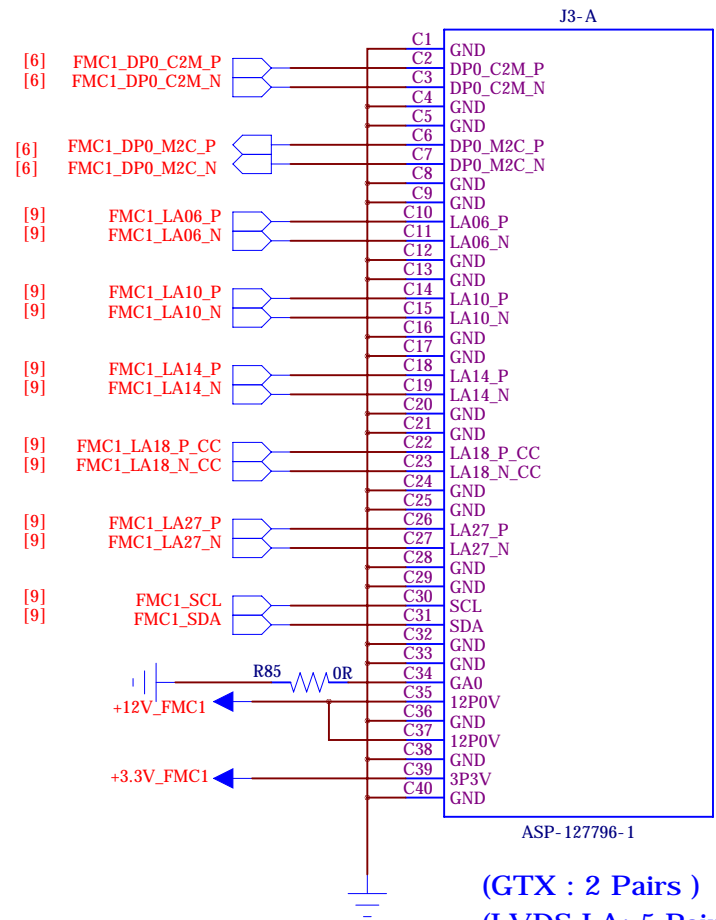
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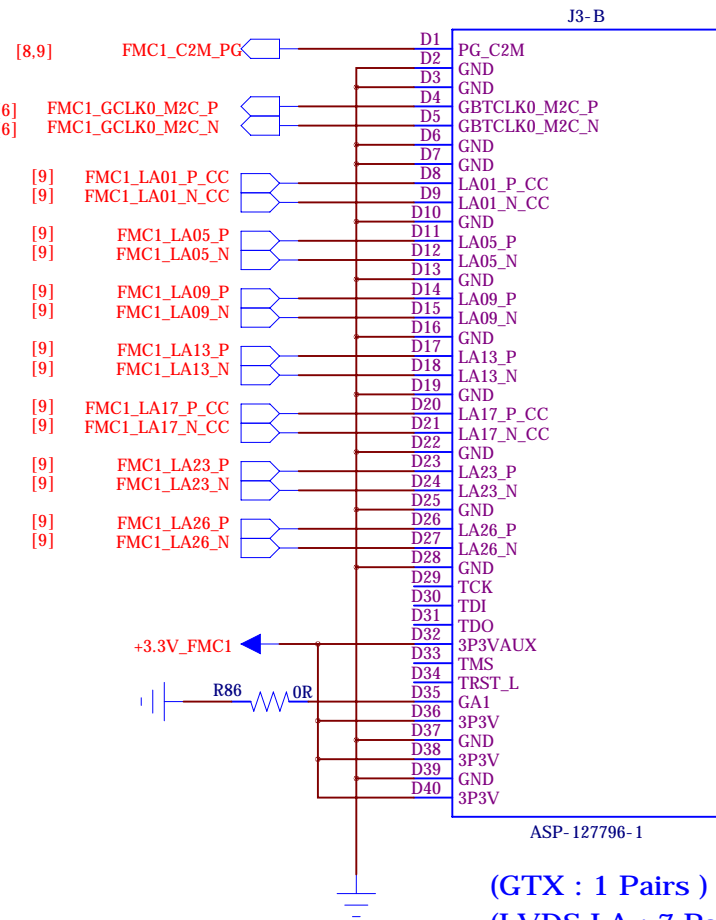


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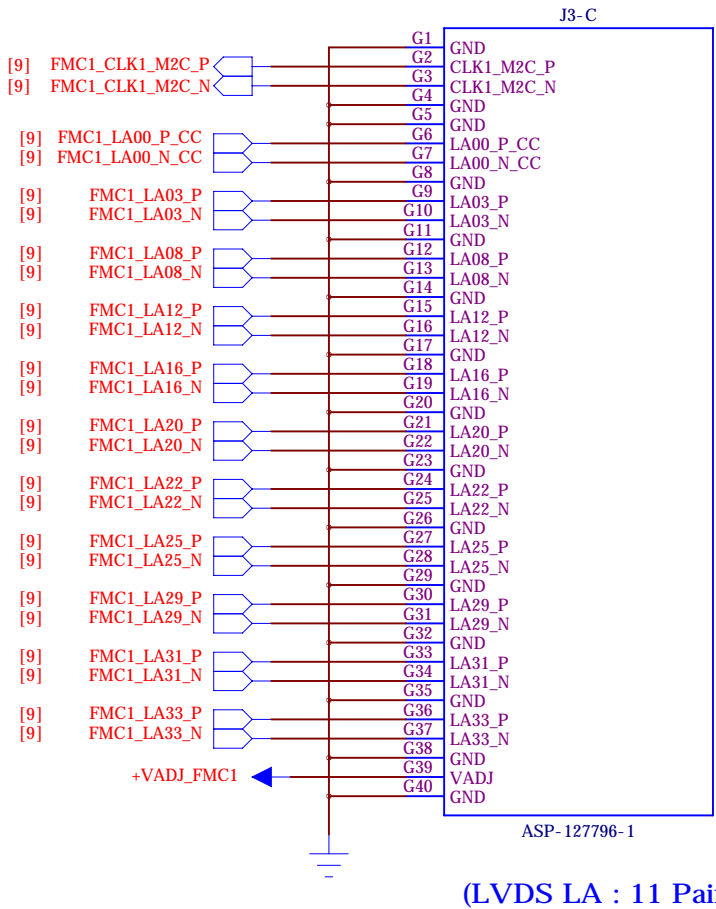
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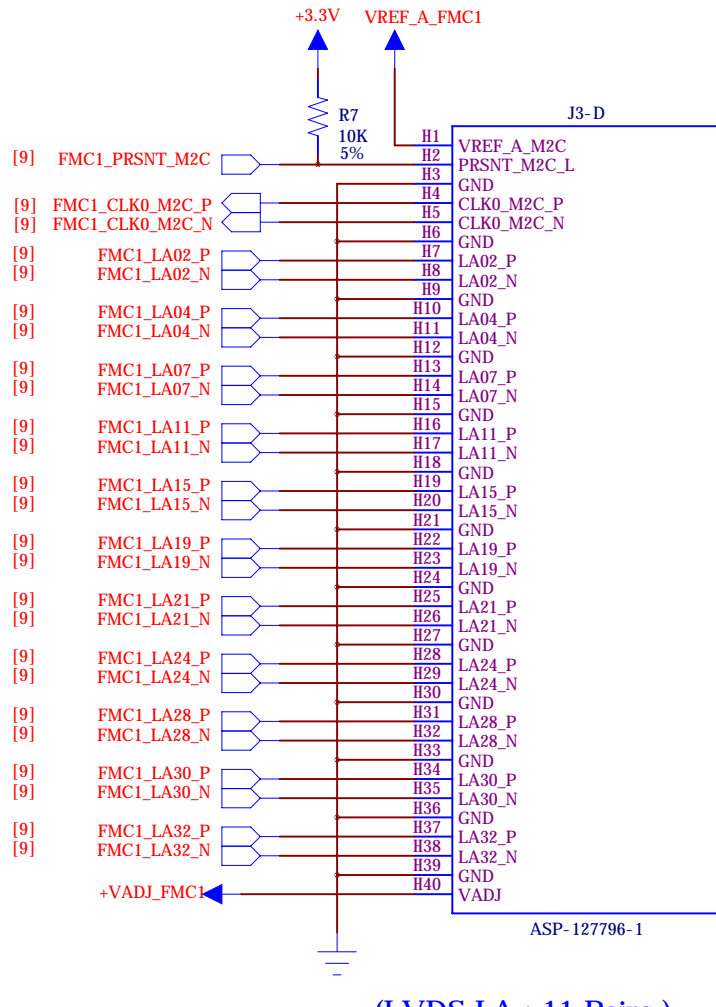
(GTX : 2 Pairs)
(LVDS LA: 5 Pairs)
(signal end : 2)



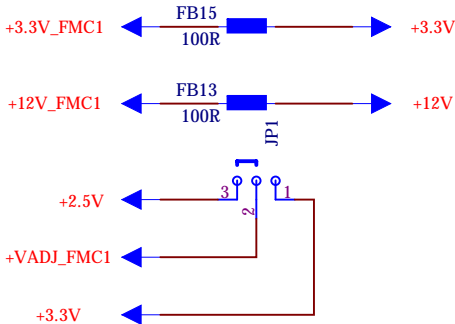
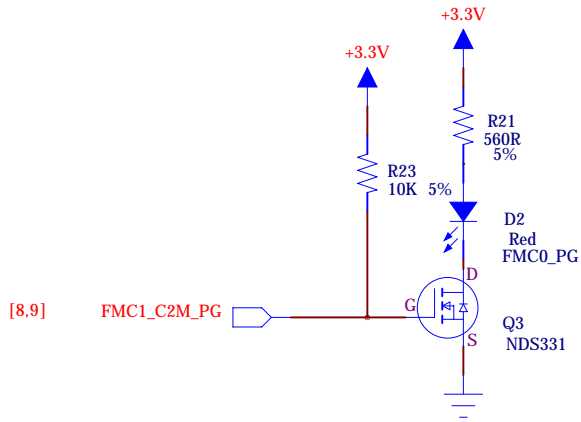
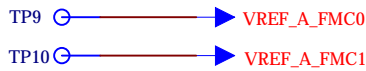
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(LVDS LA : 7 Pairs)



(LVDS LA : 11 Pairs)

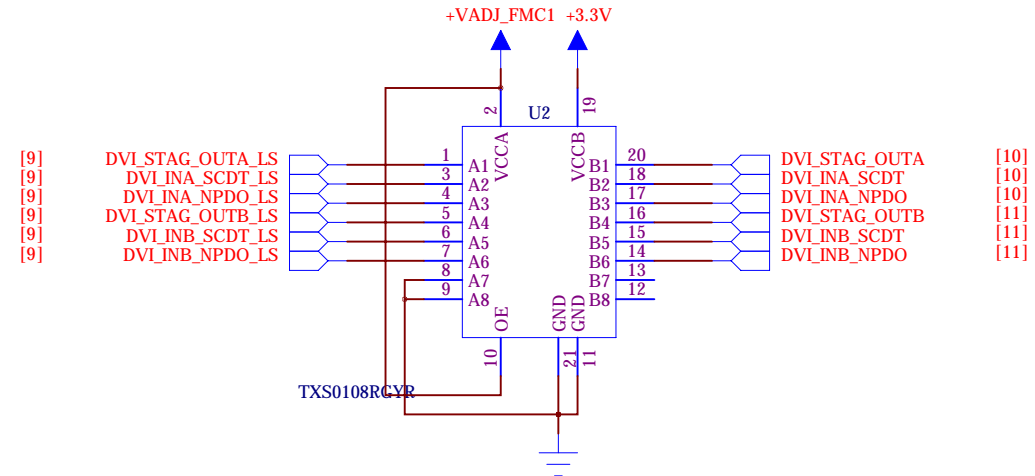
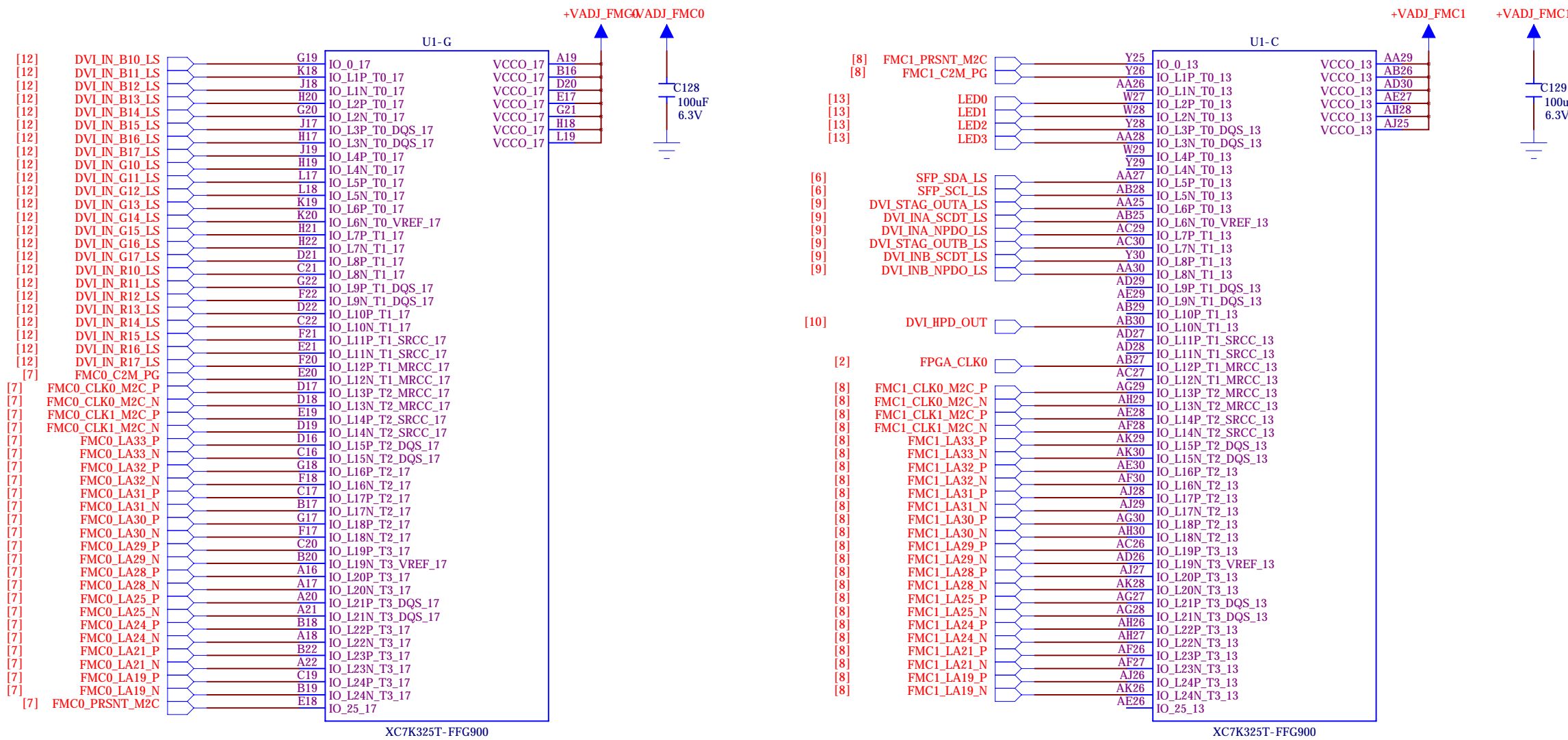
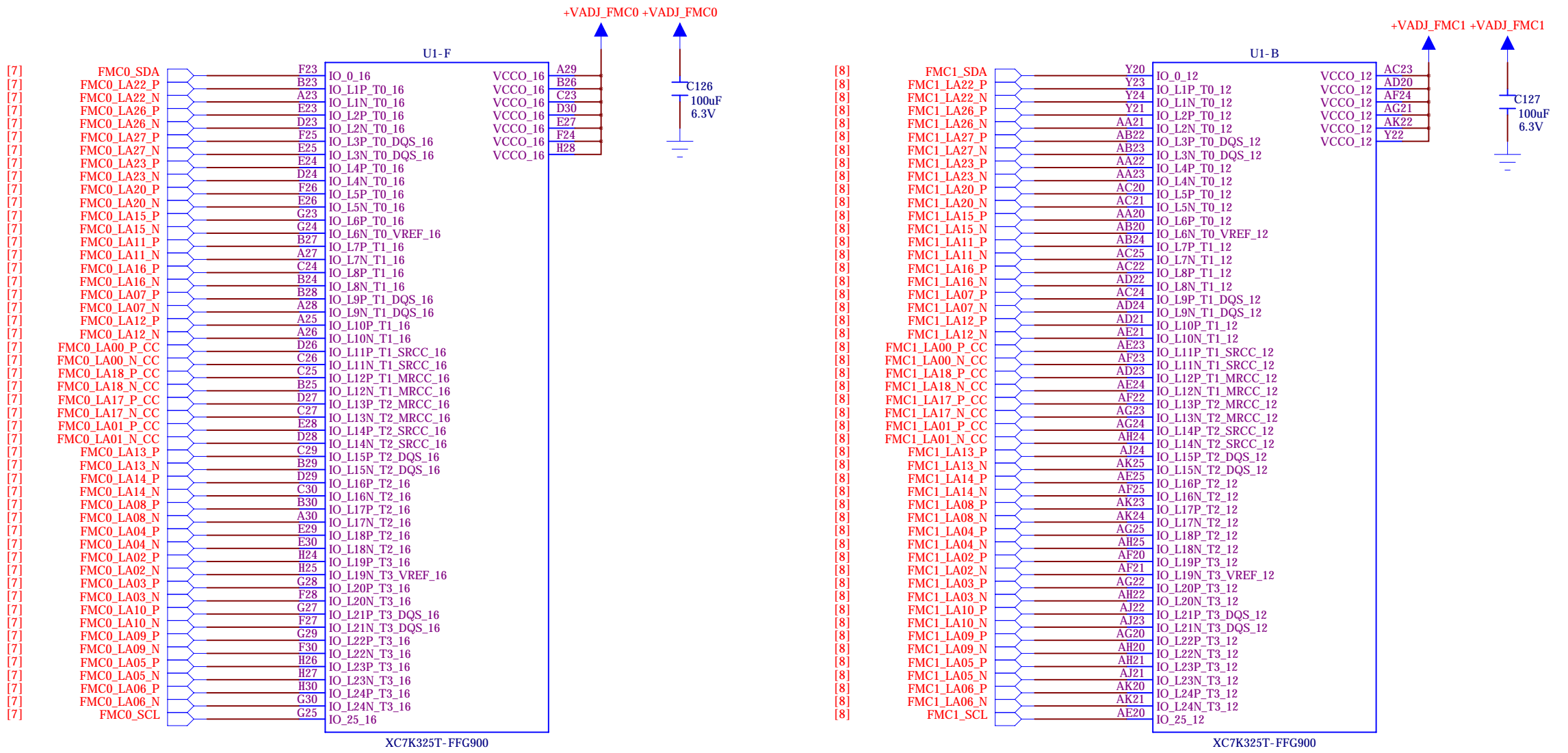


(LVDS LA : 11 Pairs)



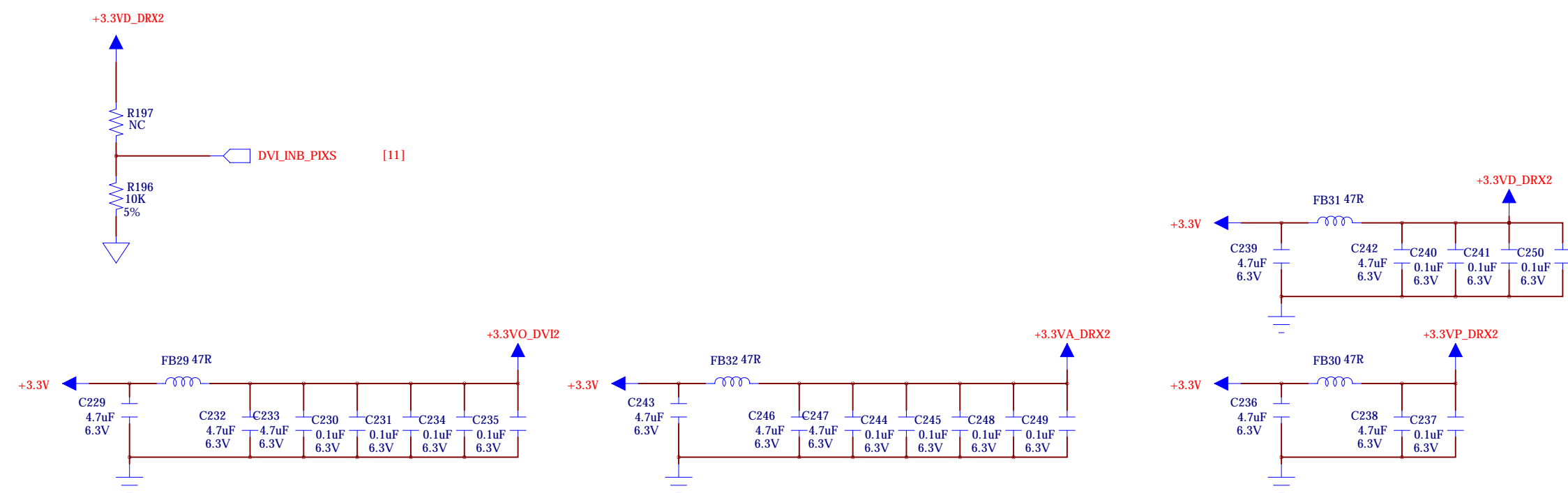
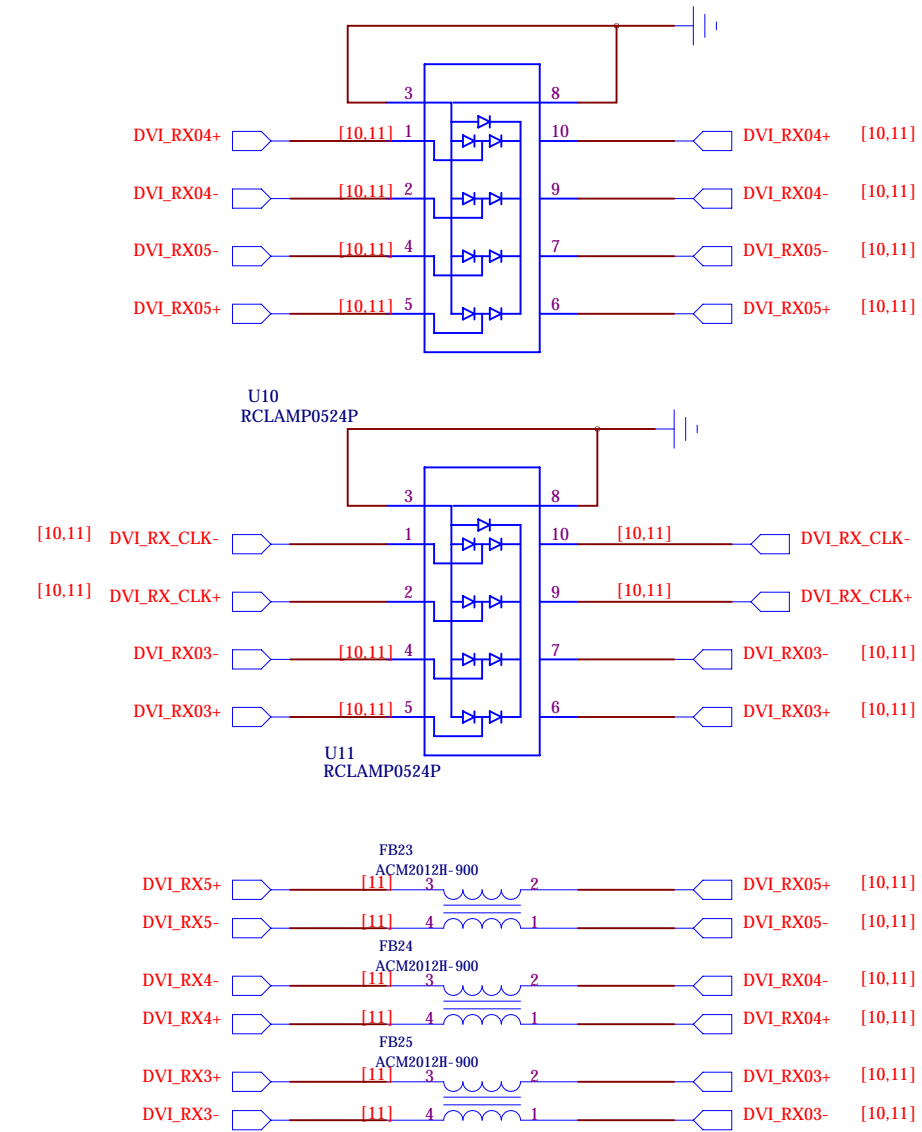
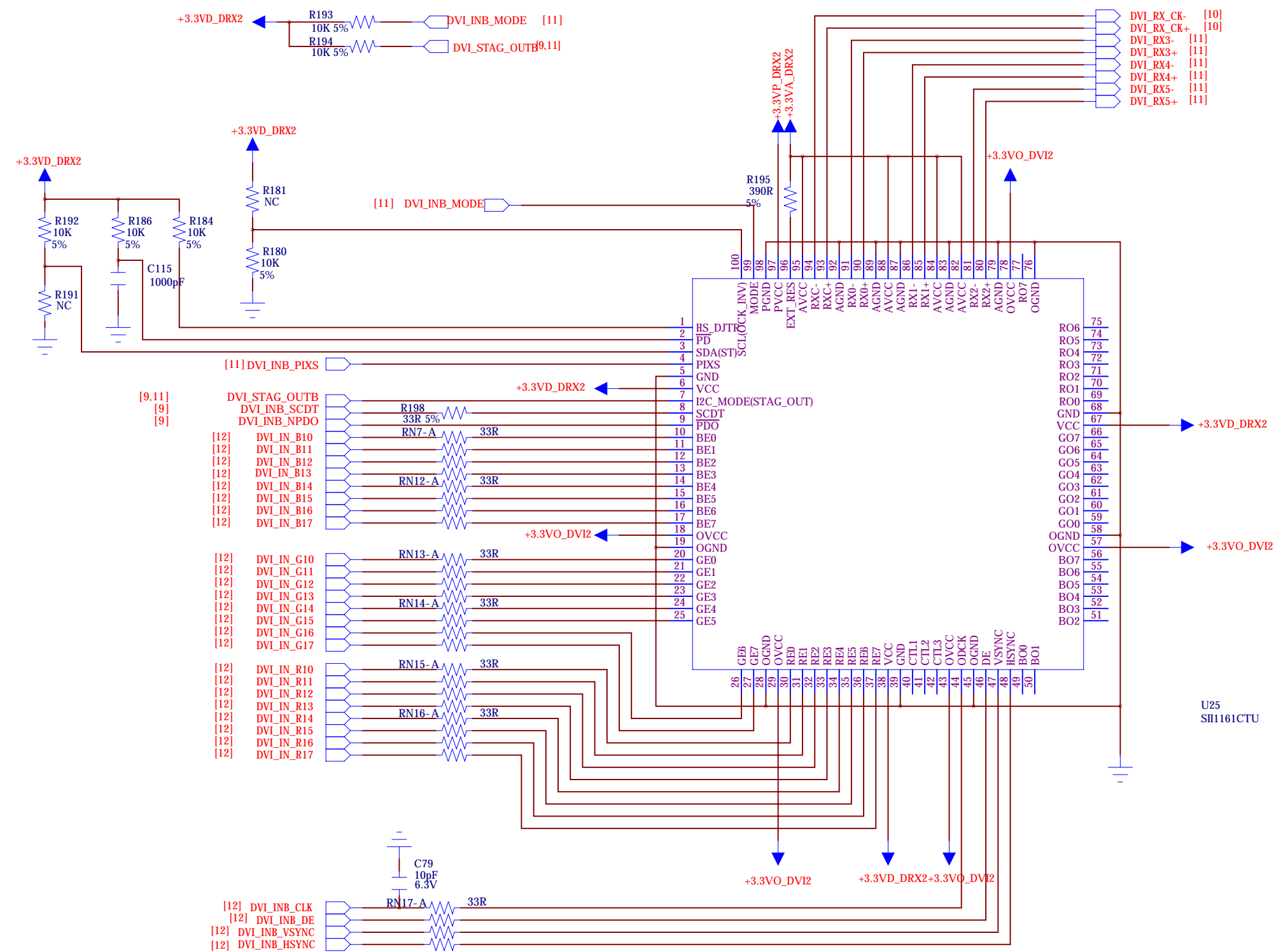
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STANDARDIZED:		VERSION:	SIZE: A2	SCALE:	SHEET8 OH 5
RELEASED:		<Company Name>			

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



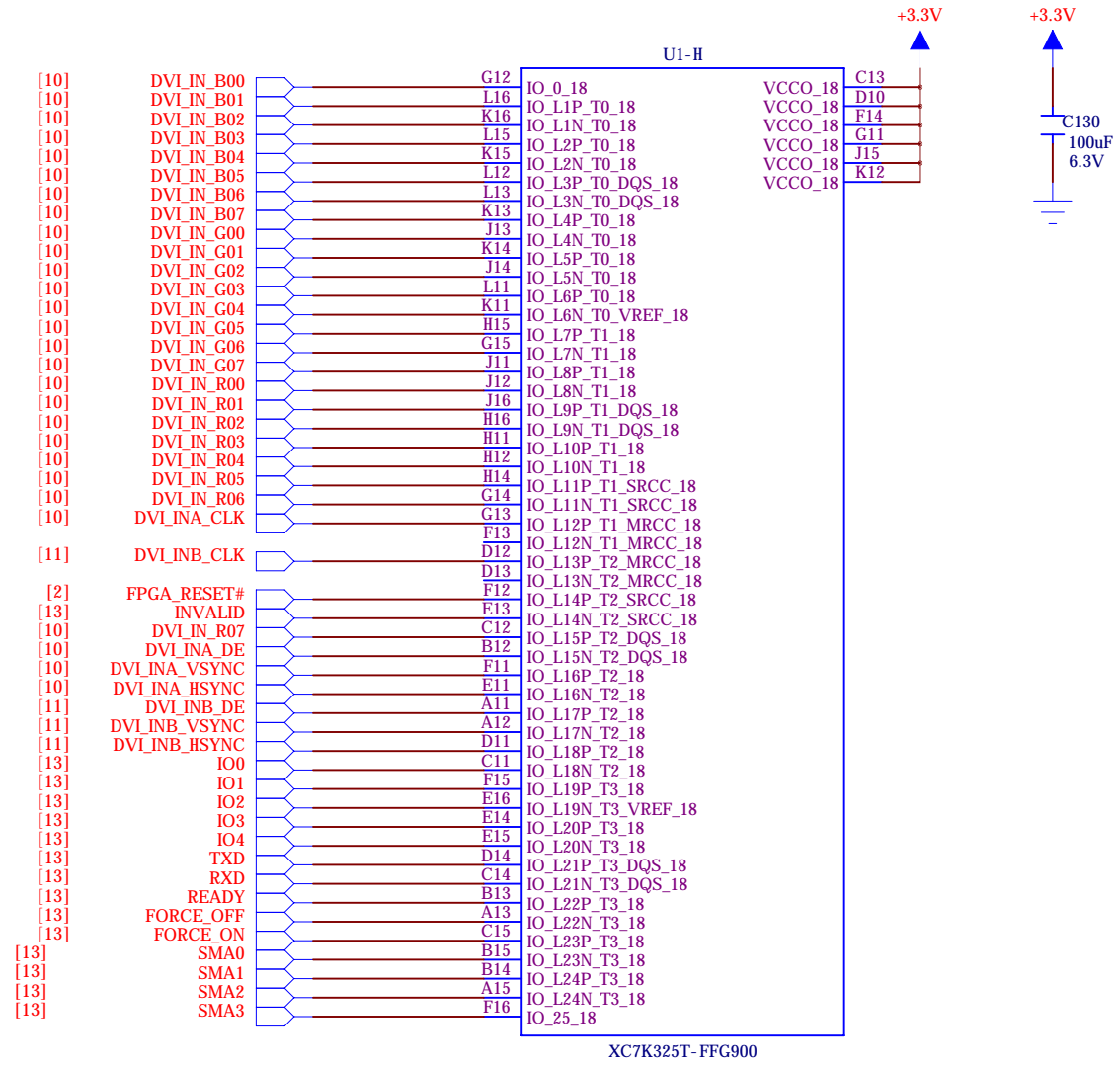
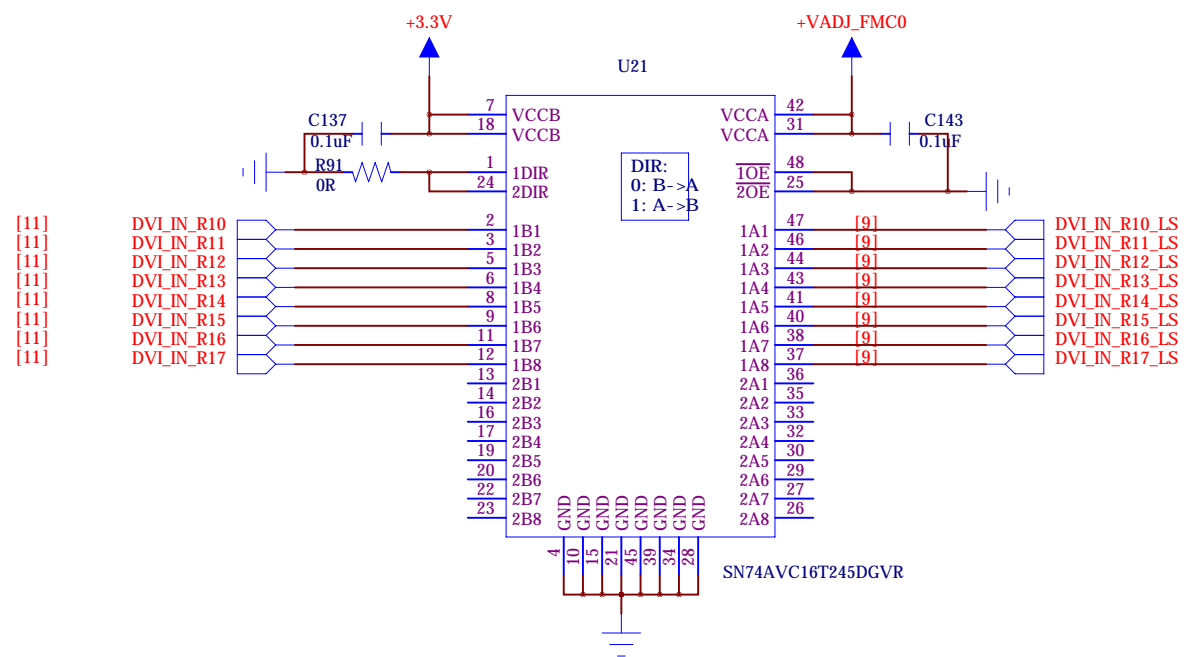
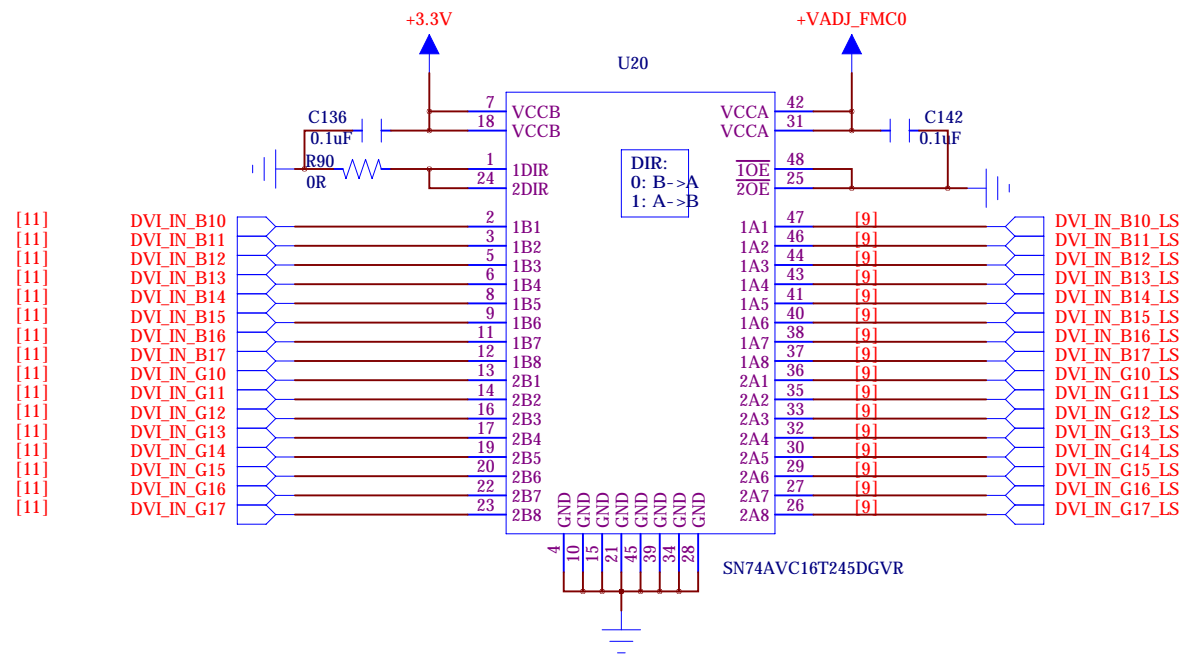
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RELEASED:		<Company Name>			

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LTR	ECO NO:	APPROVED:	DATE:



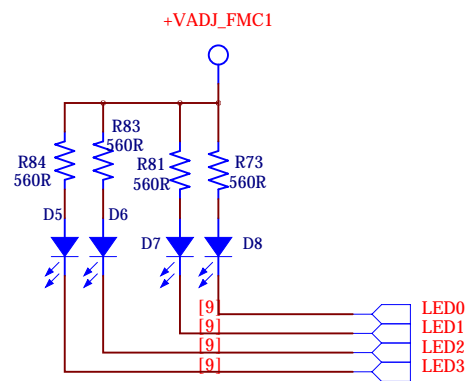
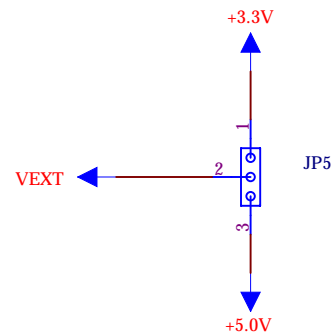
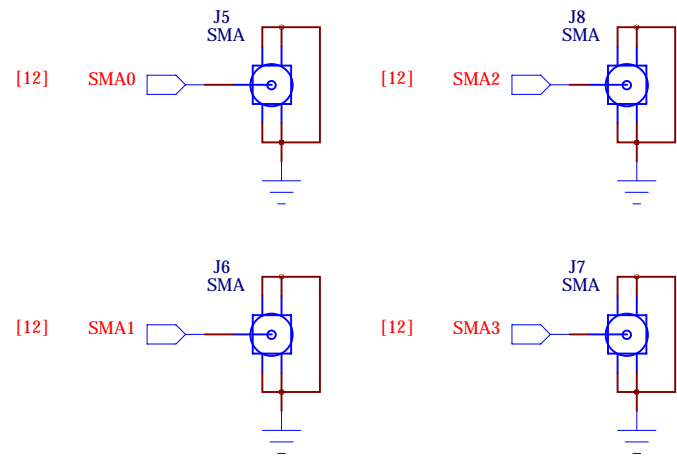
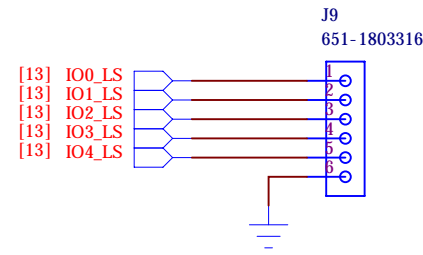
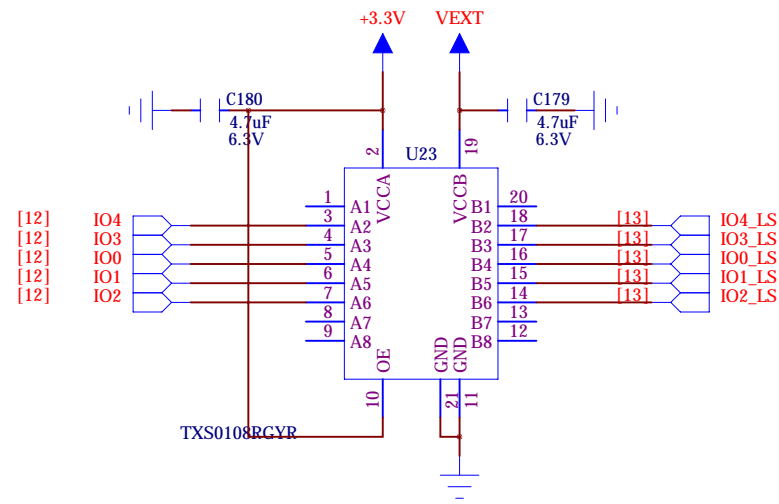
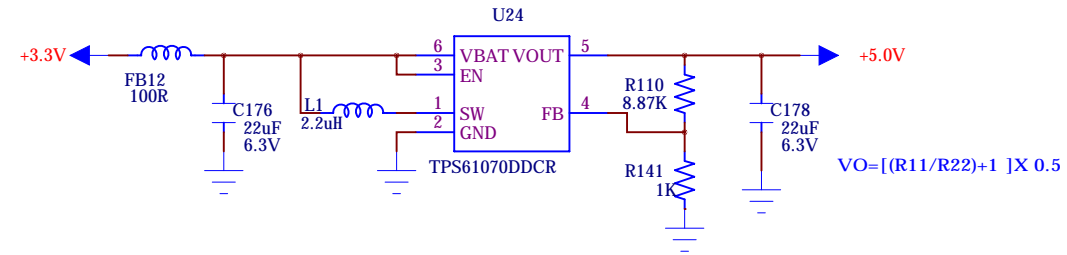
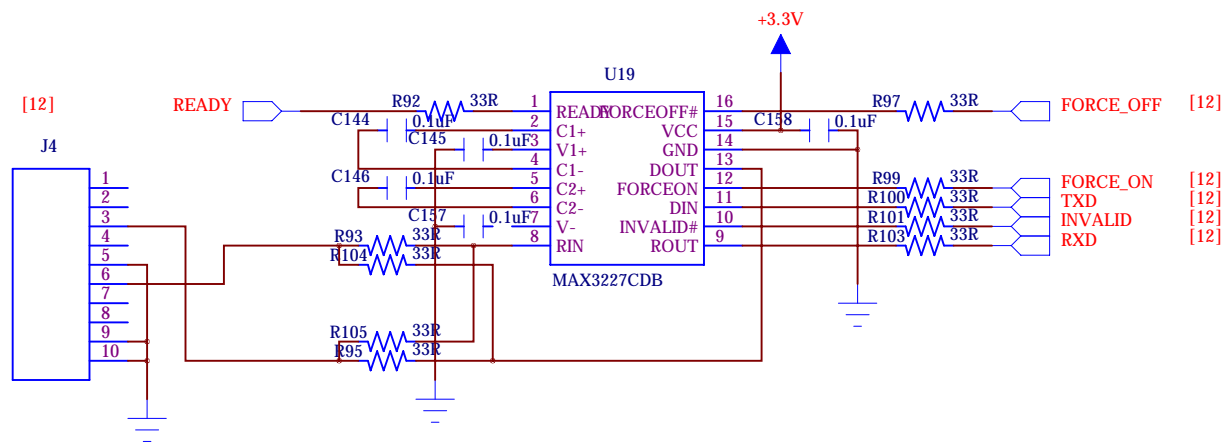
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CHECKED:					
STANDARDIZED:		VERSION:	SIZE: A2	SCALE:	SHEET11 OH 5
RELEASED:		<Company Name>			

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LTR	ECO NO:	APPROVED:	DATE:



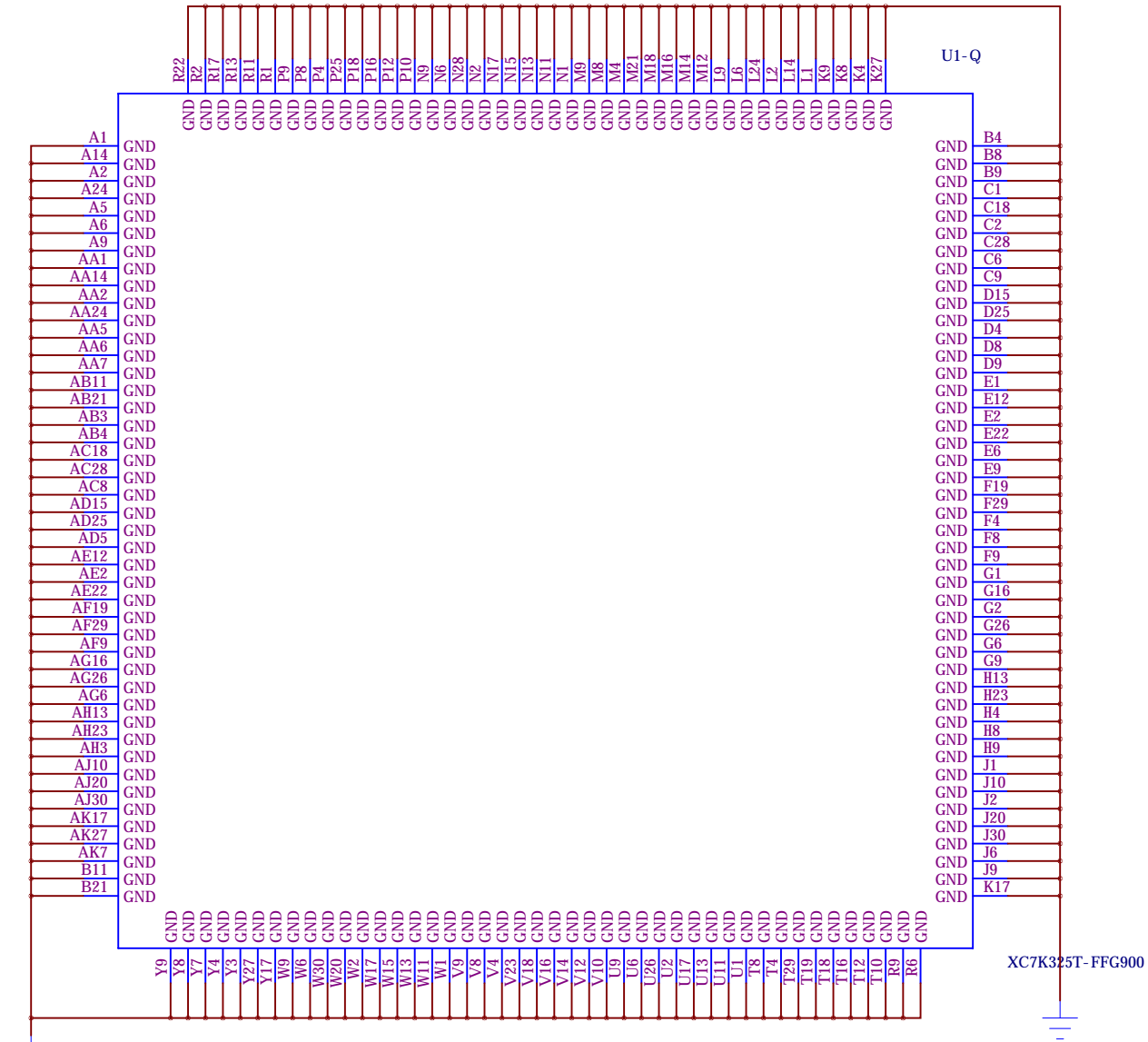
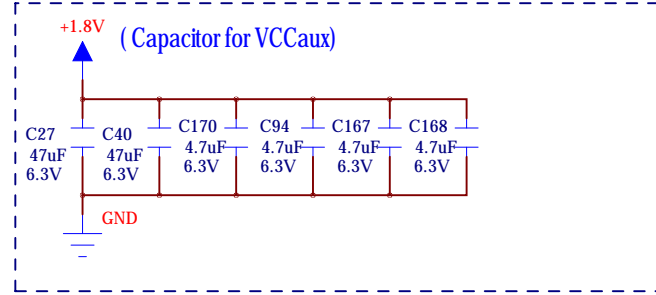
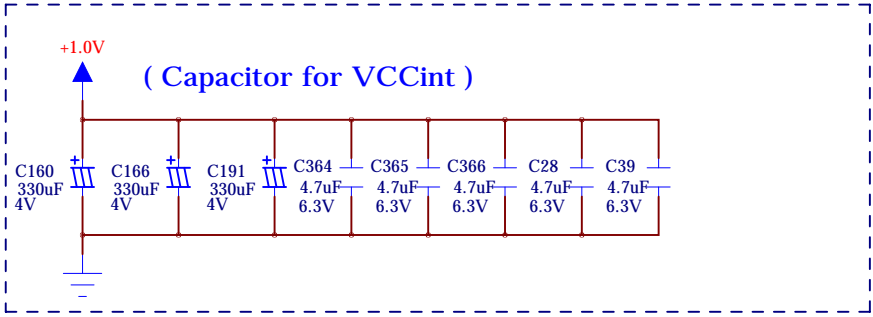
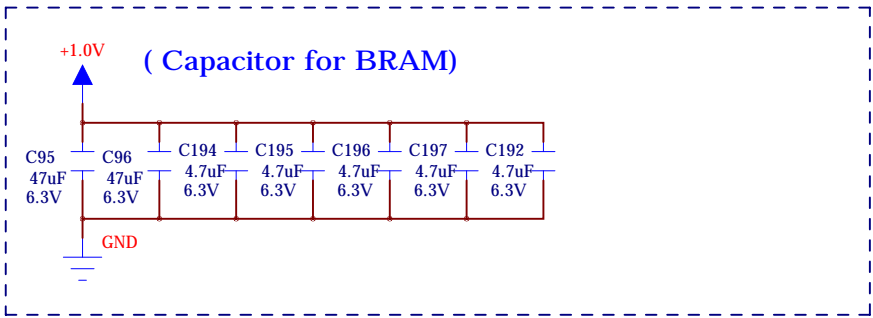
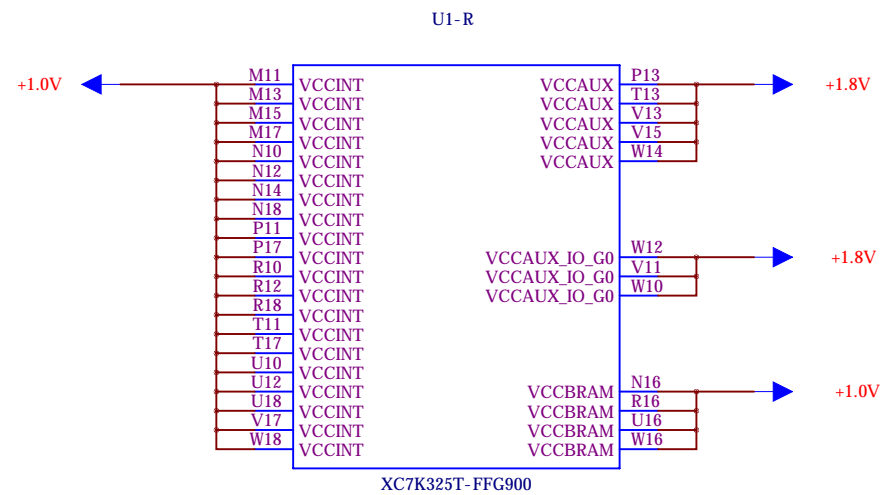
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TITLE: USER_IO					
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LTR	ECO NO:	APPROVED:	DATE:



TITLE: FPGA_POWER					
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STANDARDIZED:		VERSION:	SIZE: A2	SCALE:	SHEET14 OH5
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