# MICHAEL LANDER

37 Kingsville Lane, Richmond Hill • 647-571-0124 • michael.lander@mail.utoronto.ca linkedin.com/in/michaellander1 • https://github.com/Codinghero279

## **EDUCATION**

## **Bachelor of Applied Science in Computer Engineering**

Sep 2023 - Apr 2027

University of Toronto

- Edward S Rogers Sr. Admission Scholarship
- Faculty Of Applied Science And Engineering Admission Scholarship
- Courses: Data Structures and Algorithms, Software Design, Computer Networks, Signals and Systems

### **EXPERIENCE**

#### **Firmware Team Member**

May 2025 - Present

U of T Aerospace Team, Space Systems

- Develop and Test Firmware Using C in Zephyr RTOS for our FINCH mission Cube Satellite
- Use **Zephyr Drivers** for our Heater and Real-Time Clock Systems
- Tested CAN bus Driver on the Oscilloscope for Communication Between our Two On-Board PCBs

#### Al Trainer

Mar 2025 - Sep 2025

Outlier Al

- Reviewed and Provided Quality Feedback on Machine-Generated Responses, Helping Raise model Precision/Recall Scores with 90% accuracy Through Consistent Application of Evaluation Guidelines.
- Generated and Curated High-Quality Training Prompts Across Diverse Domains, Contributing to a 20% Increase in Model Response Relevance During A/B Testing

#### **Creative Director**

Jan 2024 - Apr 2024

U of T Engineering Team

- Developed a Functional, Non-Intrusive Medical Device Prototype, Resulting in 98% Data Tracking Accuracy, Ensuring Better Diagnoses of Sleep Disorders
- Led Creative Decisions of The Team Regarding Many Elements of the Project
- The Prototype Budget was Kept Under \$100

#### **PROJECTS**

# Responsive Web Application | HTML, CSS, Javascript

- Built a Travel Tracking Website with Interactive Leaflet.js Mapping and Published it on GitHub Pages
- Implemented Local Storage for User Data Persistence and 95% Accurate Vector Layer Interactions

## FPGA Memory Game | C, RISC V Assembly

- An Interactive Memory-Based Game Developed On An FPGA Board Running A NIOS V Processor
- User-Triggered Clock Randomizes Every Path; Has Full VGA and Audio Output

# Mapping Software | C++

- Developed Customizable, Interactive Mapping Software with a Team
- Uses OSM Data; Algorithms Like Dijkstra's Employed for Efficient Pathway Calculations
- Optimized Memory Usage And Processing Speeds; Multithreaded for up to 4x Performance

## FPGA Brick Breaker | Verilog, C

- An Interactive Brick Breaker Game Developed on a De1-SoC FPGA Board Using Verilog and C
- De1-SoC Push Buttons Used for Movement; Has Full VGA and Audio Output

## **TECHNICAL SKILLS**

Languages: C/C++, Python, HTML, CSS, JavaScript, Verilog HDL, RISC-V Assembly, MATLAB

Tools: Git, GitHub, Linux, VS Code, PyCharm, Zephyr, LTspice