Homework 2

Due on September 16 (Thursday), 2021

Problem 1.

For a 32-bit MIPS architecture, a “bridge” called memory-bus of 16-bit wide, transfers data bytes between DRAM memory and CPU. The bus has its own clock of 8-MHz, which is a different and slower clock from the CPU clock due to the big speed gap between CPU execution and data movement. The **bus clock** represents the speed of the bus. The **bus cycle** is a timeslot that refers to how much data can move across the bus simultaneously by the bus-width, such as 16-bit in the cycle. **One bus cycle** is equivalent to **four bus clock cycles** in this architecture.

Question 1

What is the data transfer rate across the bus in bytes/second?

Question 2

To improve the data transfer performance, which choice is better: (1) to widen the data bus from 16-bit to 32-bit; or (2) to double the external clock frequency of the bus clock from 8-MHz to 16-MHz?

Problem 2.

For the following code sequence and memory locations along with their contents in hexadecimal numbers.

```
add $t0, $zero, $zero
lw    $t1, 0($t0)
lb    $t2, 2($t0)
sb    $t1, 5($t0)
```

Memory

Data (hex)	Word Address (Decimal)
…	
0 0 0 0 0 0 0 0	24
0 0 0 0 0 0 0 0	20
0 0 0 0 0 0 0 0	16
1 0 0 0 0 0 1 0	12
0 1 0 0 0 4 0 2	8
1 1 1 1 1 1 1 1	4
0 0 A B C D 1 0	0

What are the updates of the memory and registers $t1 and $t2 by considering (1) “Big Endian” and (2) “Little Endian” formats?

Problem 3.

What is the single MIPS instruction or, if not possible, the shortest sequence of MIPS instruction for the following programing programming requests? Note: we use decimal numbers for MIP programming, and explain each MISP instruction you have used by programming comments.

1. Decrements register R10 by 200

2. Set register R15 with value of 200

3. y [20] = y[30] + x, where x is register R9, and y is an array of integers with memory location of 0.

Problem 4.

Implementing a data movement request that copies a block of words from one memory address to another by a set of MIPS instructions. The starting address of the source block is stored in register $t1, and the destination starting address is stored in register $t2, and the number of words to be copied is in register $t3, which is a positive integer.

Problem 5.

For the following MIPS program, determine a sequence of 32 bits for each instruction by referencing the Table (Figure 2.6) in the textbook (4^{th} edition) on pp 100, and by referencing the example of “Showing Branch Offset in Machine Language” in the textbook (4^{th} edition), pp. 131:

```
Loop: lw R6, -1(R31)
      addi R18, R3, -513
      sw   R28, -3 (R5)
      bne R7, R5, Loop
```