Homework 4

Due on September 30 (Thursday), 2021

Problem 1.

For a single-cycle design of a MIPS processor, how does instruction “lbu” work based on its data flow along with the control signals? Using the HomeWork4-slides figure (“Circuit for Instruction lbu”) to explain all the related data flow and control signals within the single cycle. Please divide you single cycle into 5 stages: (1) instruction fetching, (2) instruction decoding, (3) ALU execution, (4) memory access, and (5) register writing.

Note: lbu: load byte unsigned from memory to register.

lbu $s1, 20($s2) # $s1 = Memory ([$s2 +20])

Problem 2.

Considering the following sequence of MIPS code, your task is to use pipelining building blocks to execute this set of instructions.

```
add $R2, $R0, $R0
lw $R1, 0($R2)
addi $R3, $R1, 20
add $R1, $R2, $R0
or $R1, $R2, $R0
```

Questions 1
How many stall cycles would occur in a MIPS pipelining without Pipeline Forwarding? Using the pipelining building blocks to explain your result.

Questions 2
How many stall cycles would occur in a MIPS pipelining with Pipeline Forwarding? We assume that Pipeline Forwarding exists between DM-to-ALU, ALU-to-ALU, and DM-to-DM. Using the pipelining building blocks to explain your result.