Homework 5

Due on October 19 (Tuesday), 2021

Problem 1.

A 128KB data cache that uses a 32-bit address in three cache block sizes: 1 Byte, 4 Bytes, and 8 Bytes. One structure is a direct-mapped cache, and another one is a 2-way set associative cache. The design consists of two components:

(1) The 32-bit memory address is subdivided into several sections in bits so that each address can map to its cache location
(2) Each cache block includes the cache storage and other necessary bits (valid and tag bits).

You are asked to write two groups of results with your explanations:

Group 1: three direct-mapped caches with block sizes of 1, 4, and 8 Bytes.

Group 2: three 2-way set associative caches with block sizes of 1, 4, and 8 Bytes.

Problem 2.

For a data cache with a 92% hit rate and a 2-cycle hit latency, calculate the average memory access latency. Assume that latency to memory and the cache miss penalty together is 124 cycles. Note: The cache data can only be accessed after memory returns the data.

Problem 3.

The machine in this problem has a byte-addressable memory of 2^{16} bytes. The direct-mapped cache consists of 32 cache blocks, and the cache block size is 8 bytes.

Question 1

How is the 16-bit memory address divided into byte offset, cache index, and tag?

Question 2

What is the capacity of the cache in bytes?

Question 3

Why tag is also stored in the cache?

Question 4

For the following four memory addresses, what cache block would each be mapped to?

0001 0001 0001 1011
1100 0011 0011 0100
1101 0000 0001 1101
1010 1010 1010 1010