CSE3421
Computer Architecture

Homework 2

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Problem 1

For a 32-bit MIPS architecture, a “bridge” called memory-bus of 16-bit wide transfer data bytes between DRAM memory and CPU. A clock of 8-MHz is used for the bus, which is a different and slower clock from the CPU clock due to the speed gap between CPU execution and data communication between CPU and memory. The bus clock represents the speed of the bus and refers to how much data can move across the bus simultaneously by the bus-width, such as 16-bit in this case. This architecture has a bus cycle for 16-bit in four bus clock cycles.

Question 1

What is the data transfer rate across the bus in bytes/second?

In CPU we deal with # instructions per cycle (CPU cycle)

Data transfer between CPU/memory is determined by memory bus clock (bus cycle time)

In contrast, we only have one “clock” in our body. The heartbeat can be measured anywhere, e.g., wrist, ankle, and others.

Problem 1 (continued)

Question 2

To improve the data transfer performance, which choice is better: (1) to widen the data bus from 16-bit to 32-bit; or (2) to double the external clock frequency of the bus clock from 8-MHz to 16-MHz?

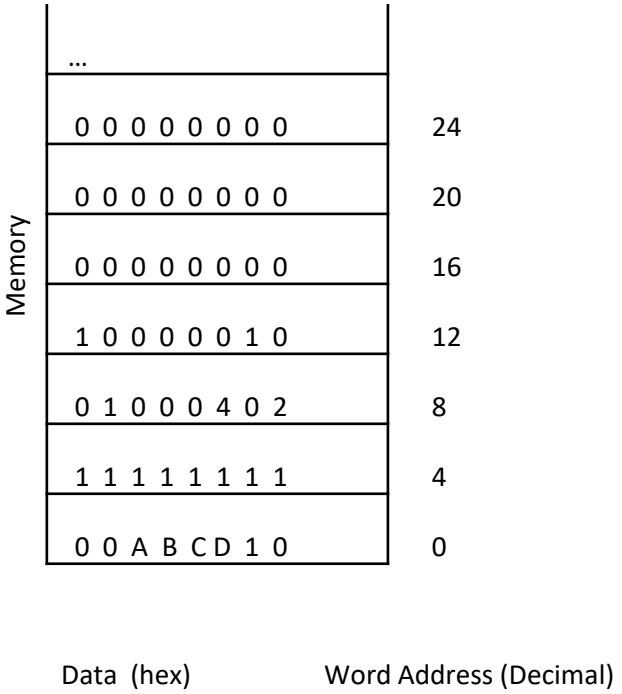
Same patten of thinking

In Highway, traffic performance is determined by Speed Limit and number of lanes

Problem 2

For the following code sequence and memory locations along with their contents in hexadecimal numbers.

```
add $t0, $zero, $zero
lw    $t1 , 0($t0)
lb    $t2 , 2($t0)
sb    $t1, 5($t0)
```



What are the updates of the memory and registers $t1 and $t2 by considering (1) “Big Endian” and (2) “Little Endian” formats.

Problem 2

```
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lw    $t1 , 0($t0)
lb    $t2 , 2($t0)
sb    $t1, 5($t0)
```

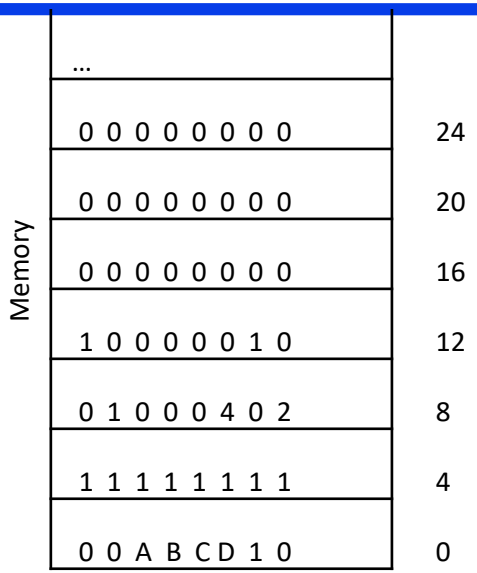

Concept reviews:

Byte-addressable memory

B-endian and L-endian are only used to count the order of bytes in memory for load and store in a byte unit.

Problem 3

What is the single MIPS instruction or, if not possible, the shortest sequence of MIPS instruction for the following programing programming requests. Note: we use decimal numbers for MIP programming and explain each MISP instruction you have used by programming comments.

1. Decrement register R10 by 200

2. Set register R15 with value of 200

Problem 3 (continued)

3. y [20] = y[30] + x, where x is register R9, and y is an array of integers with memory location of 0.

Index values of 20, and 30 map to physical memory locations.

Problem 4

Implementing a data movement request that copies a block of words from one memory address to another. The starting address of the source block is stored in register $t1, and the destination starting address is stored in register $t2, and the number of words to be copied is in register $t3, which is a positive integer.

How do you write this by a high-level language?

Using a set of instructions to follow the same logic flow.

Problem 5

For the following MIPS program, determine a sequence of 32 bits for each instruction:

```
Loop: lw R6, -1(R31)
      addi R18, R3, -513
      sw   R28, -3 (R5)
      bne  R7, R5, Loop
```

We studied in this class.