A 16-way Time-Interleaved SAR ADC Design for SerDes Links at 16 Gbps

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by

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Under the guidance of

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CERTIFICATE

This is to certify that the thesis entitled **A 16-way Time-Interleaved SAR ADC Design for SerDes Links at 16 Gbps**, submitted by **K ADITYA SAI** to Indian Institute of Technology Bhubaneswar, is a record of bonafide research work under my supervision and I consider it worthy of consideration for the Mid-semester project review of the degree of Master of Technology of the Institute.

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K ADITYA SAI

Abstract

In today's technology, high-speed links play an important role, enabling faster, cheaper, and more reliable data communication. Data converters, present in some form in almost all modern high-speed links, are a key to performing equalization - the process of compensating bandwidth limitations of the communication channel. In particular, high-speed ADCs at the receiver front ends can enable easily-scalable digital implementations of various equalization schemes, such as feed-forward equalization (FFE), decision-feedback equalization (DFE), and even maximum-likelihood sequence estimation (MLSE). However, power limitations of on-chip high-speed link receivers make front-end ADC design very challenging. Therefore, in this work we design a time-interleaved ADC which can be used in the Receiver front end of a High-speed SerDes Link. This leads us to the idea of heavily interleaving very simple and efficient ADCs to obtain high aggregate data conversion rates with low resolution ADCs working at comparatively mediocre data conversion rates. In this work specifically, a 16-way time-interleaved SAR ADC has been targeted to work with a conversion rate of 16 Gbps on SerDes links. This means that each sub-ADC's targeted conversion rate will be relaxed to only 1 Gbps. Various design elements of the SAR ADC have been designed and simulated separately. All these simulations have been done in Cadence Virtuoso tool. These circuits are implemented using the USMC 65 nm 1.2 V CMOS technology. The statistical performance of the SerDes Link with the inclusion of ADC on the receiver side is also being studied and simulated. The time-domain simulations of the SerDes Links are being done in MATLAB R2022a.

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List of Abbreviations

ADC	Analog to Digital Converters
DAC	Digital to Analog Converters
SAR	Successive Approximation Register
TI	Time-Interleaving
FFE	Feed Forward Equalization
DFE	Decision Feedback Equalization
MLSE	Maximum-Likelihood Sequence Estimation
SerDes	Serializer - Deserializer
BER	Bit Error Rate
Gbps	Giga Bits Per Second
PAM	Pulse Amplitude Modulation
PRBS	Pseudo Random Bit Sequence

Chapter 1

Introduction

Most modern digital systems consist of multiple integrated circuits (ICs), which need to communicate with each other. As the processing speed of each IC increases, it demands higher and higher input/output (I/O) bandwidth. The term high-speed link refers to both the physical channel and the I/O circuits that aim to support this ever-increasing need for bandwidth. To keep up, high-speed links are forced to both employ more parallel channels and increase the data rate in each channel.

Although communicating digital 0s and 1s, especially over wires, may seem trivial, at high frequencies, it becomes more complex. The resistive and dielectric losses in wires increase at high frequencies, resulting in distorted digital signals and presenting constant new challenges to link design as data rates increase. Significant effort goes into developing better communication channels, ranging from more advanced printed circuit boards, IC packages, and connectors to optical, capacitive, inductive, and radio-frequency (RF) interconnects. Meanwhile, most high-speed links today have to resort to multiple signal processing techniques to overcome the bandwidth limitations of existing channels.

Basic signal processing tasks, such as continuous-time equalization, finite-impulse

response filtering, and decision-feedback equalization can be efficiently performed with analog circuits. However, as the complexity of filters increases to compensate for channel losses at higher and higher frequencies, exploiting the benefits of digital scaling by moving signal processing to digital domain becomes an interesting alternative. To accomplish this in a link receiver, an analog signal from the channel needs to be digitized first, requiring a high-speed analog-to-digital converter (ADC).

1.1 Background

As the demand for high data rate continues to rise, driven by evolving applications and larger user base, it has become increasingly difficult to develop power and area efficient wireline links needed to support such an infrastructure. Both single lane data rate and density has to increase within the limited printed circuit board (PCB) real estate. Recent trends of various wireline standards show a consistent 2x increase in aggregate bandwidth requirements approximately every three to four years [1]. Current standards such as 400 Gigabit Ethernet (IEEE802.3bs [2]) and OIF Common Electrical I/O 56G (CEI-56G [3]) are pushing the limits of conventional wireline links based on mixed-signal processing with a per-lane bandwidth requirement of 56Gb/s, which motivates the need for new wireline architectures.

Any wireline link over a typical communication channel can be modelled as a system shown in Figure 1.1. The link consists of a transmitter (Tx), a channel, and a receiver (Rx). The Tx starts with a sequence of bits that need to be sent, and typically uses non-return-to-zero (NRZ) pulse amplitude modulation (PAM) schemes to transmit signals in the voltage domain. In this example, PAM2 is used with only two distinct voltage levels. The channel, which includes PCB traces and connectors, is a low-pass filter in the frequency domain, creating signal loss up to and beyond the Nyquist frequency, which is half of the link's symbol rate. Equivalently, the channel has a corresponding time-domain pulse response, which convolves with the transmitted data. The pulse response of the channel contains inter-symbol interference (ISI), which alters the signal and the receiver is now prone to errors when recovering the received data.

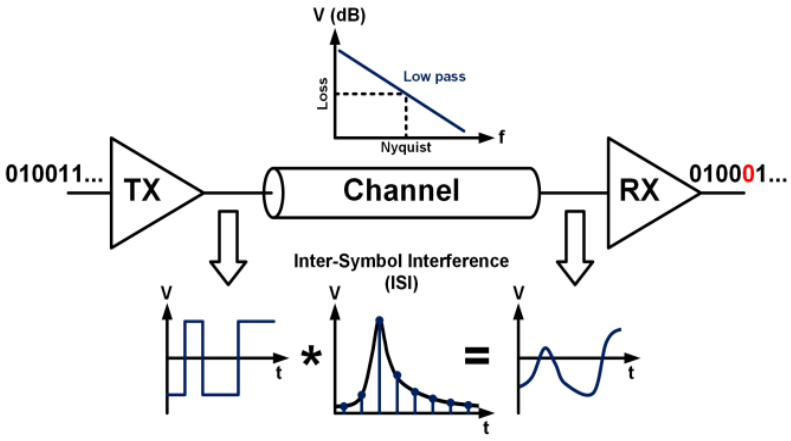

Figure 1.1: Block Diagram of a Simple Communication Channel [4]

Eye diagrams provide a pictorial way to judge whether a channel/link is healthy. Eye diagrams are generated by overlapping unit intervals (UI) of the signal of interest in the time domain. Figure 1.2 shows examples of open and closed eye diagrams. When channel ISI and noise in the link system is much smaller than the actual data signal, we obtain an open eye diagram (Figure 1.2(a)) in which the eye has a vertical opening, eye height (E.H) and a horizontal opening, eye width (E.W). The dither around the data levels are due to residual ISI and noise. Figure 1.2(b) shows an example of a closed eye diagram. In such a system, ISI and noise overwhelm the transmitted data, therefore making the high and low data levels indistinguishable. For a given PAM scheme, there will be PAM-1 eyes in the eye diagram.

Bit error rate (BER) is the metric that ultimately quantifies a link's performance. As illustrated by the PAM2 example in Figure 1.3, the TX only sends voltages representing either a "0" or "1" in the probability domain. After channel ISI and circuit/environment noise are added, the receiver sees a signal whose probability density function (PDF) is a sum of two Gaussian-like peaks. The area under the curves' crossed-over portions gives the probability of a wrong bit decision, thus BER.

In order to compensate for ISI due to channel loss and meet the required BER specifications, different equalization techniques are used in link systems. Figure 1.4

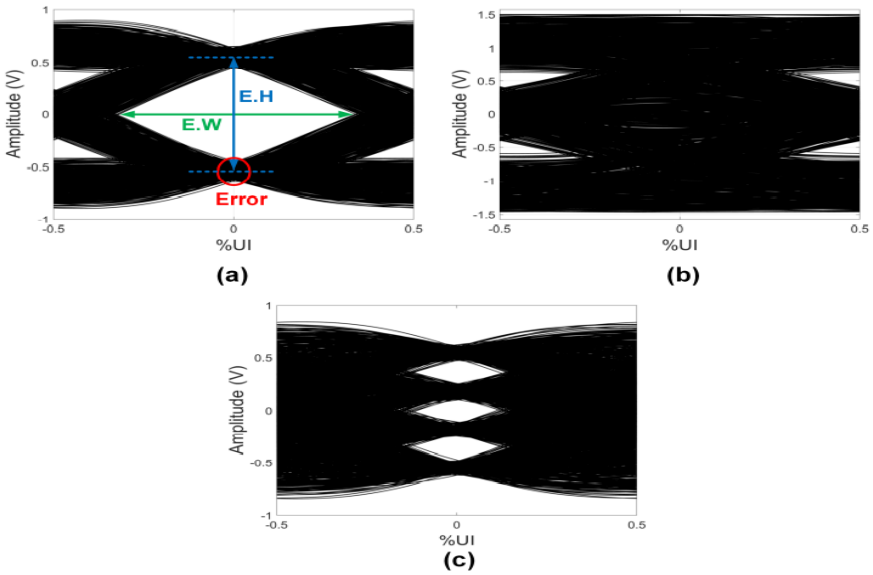

Figure 1.2: Examples of (a) an open eye diagram for PAM2, (b) a closed eye diagram for PAM2 and (c) an open eye diagram for PAM4 [4]

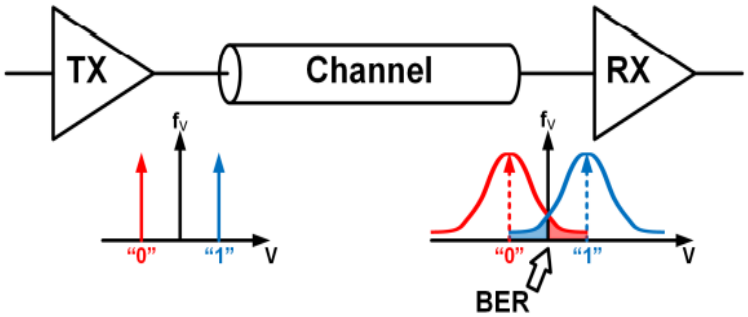

Figure 1.3: Bit error rate in wireline links [4]

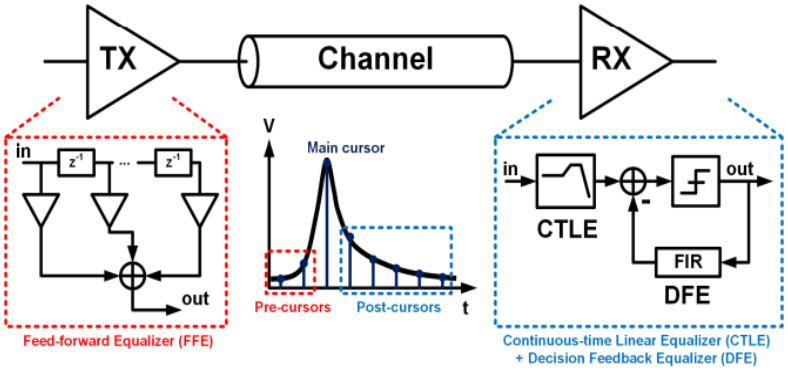

Figure 1.4: Equalization in conventional mixed-signal links [4]

shows conventional mixed-signal equalization blocks on both the TX and RX end [4]. The main cursor in a channel's pulse response is the signal of interest. Any ISI cursors before the main cursor are called pre-cursors. A feed-forward equalizer (FFE), which is typically implemented on the TX side, normally cancels pre-cursors. Any ISI cursors following the main cursor are considered post-cursors, which are often taken care of by the receiver with a continuous-time linear equalizer (CTLE) and decision feedback equalizer (DFE). The CTLE acts as high-pass filter to compensate for the channel's low-pass action. Due to the high-pass nature of CTLEs, any high frequency receiver input noise will be boosted similar to the actual signal. To avoid excessive noise amplification, DFEs pass the noise-less recovered bits through a finite impulse response (FIR) filter that matches the post-cursor portions of the channel to achieve ISI cancellation. The TX FFE can also provide some coarse equalization for post-cursors.

1.2 Organization

- To understand the application space for ADCs , we first review the basic concepts of high-speed link systems in Chapter 2.
- In Chapter 3, we look in detail, at the design of a sub-ADC including Sampling switch, StrongARM Latch, SAR Logic and the integration of these elements to form an SAR ADC.

- In Chapter 4, we take a look at the preliminary results that we have obtained in the due course of this work thus far.
- In Chapter 5, the work to be done in the future will be discussed followed by conclusions.
- In Chapter 6, various references have been cited.

Chapter 2

An Overview of High-Speed Link Systems

A typical high-speed link system consists of 3 basic components: a serializing transmitter, a communication channel, and a deserializing receiver, as shown on the block diagram in Figure 2.1.

The transmitter usually includes a multiplexer that converts parallel data into serial stream, a line driver that send data bits through the physical channel, and a clock source, usually implemented as a phase-locked loop (PLL).
The receiver decides which discrete digital value has most likely been transmitted.

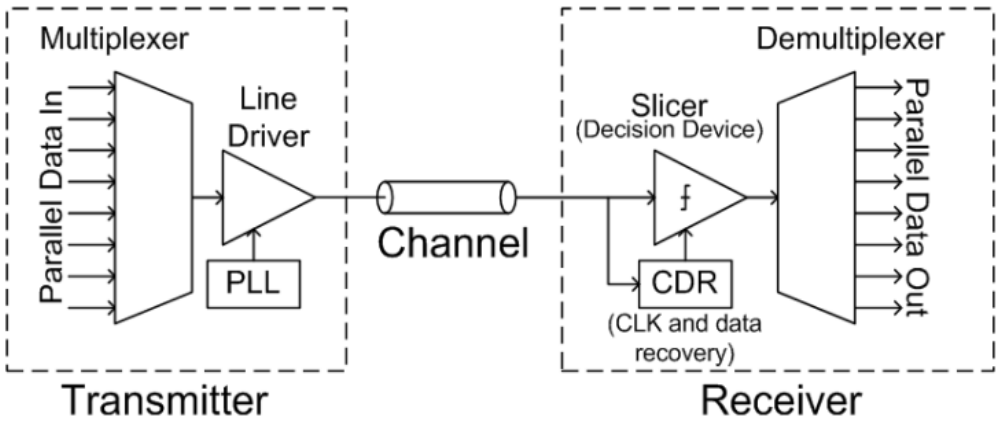

Figure 2.1: Block diagram of a high-speed link [5]

The decision device is usually referred to as slicer or comparator. Then the serial data stream is usually demultiplexed into parallel word, more naturally suited for data processing. If no explicit clock signal is sent along with the data, a clock and data recovery (CDR) block is needed to derive the timing information from data transitions.

A convenient way of describing a channel is by the pulse response of the channel. A pulse response of the channel is its output resulting from an isolated single-bit pulse (...0001000...) at its input. A general low-pass nature of most channels suggests that they cannot instantaneously respond to infinitely sharp edges of a pulse, delaying and dispersing it, as shown in Figure 2.2. When such pulse response is sampled at bit times, the largest sample is called the cursor; the samples before the cursor are called pre-cursors, and the samples after the cursors are called post-cursors. Pre-cursors interfere with previously sent bits, while post-cursors interfere with the following bits. To cancel such inter-symbol interference, most modern links use equalization. An equalizer provides an inverse channel response such that the overall frequency response is flat over the bandwidth of interest.

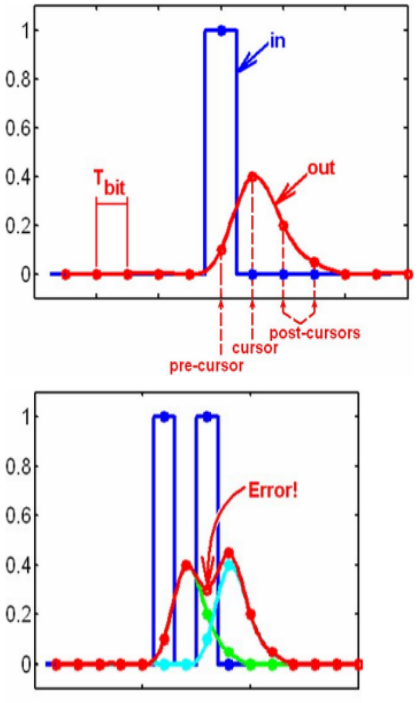

Figure 2.2: Pulse dispersion and inter-symbol interference [5]

2.1 Linear Equalization

Equalization is an important application space for digital-to-analog and analog-to-digital converters. Equalizer implementations fall into 3 general categories: analog, semi-digital, and digital. As we shall see, this classification is somewhat oversimplified, because most "analog" equalizers incorporate some digital adjustment, while all "digital" equalizers require ADCs and DACs to interface digital processors with analog channels. In fact, most equalizers operate on both analog and digital signals, so ADCs and DACs are needed to perform the conversion between the two domains. It is mainly equalizers that drive the development of data converters in high-speed links. To understand how ADCs can be optimized for this purpose, let us describe a few most common equalization techniques used in high-speed links.

2.2 Digital Feedback Equalization

All linear equalizers suffer from another problem. Ideally, an equalizer placed at the transmitter would boost a signal at high frequencies leaving low-frequency content intact. However, due to limited voltage swing of the channel driver, the filter is forced to attenuate lower frequencies rather than amplify higher frequencies, reducing the total signal energy and, thus, the signal-to-noise ratio (SNR). On the other hand, an equalizer placed at the receiver amplifies high-frequency noise along with the signal, again degrading the SNR.

To circumvent such noise amplification problem, non-linear equalizers can be used. The simplest, efficient, and thus most common non-linear equalizer used in high-speed link receivers is a decision-feedback equalizer (DFE), depicted in Figure 2.3 for a 4-tap example. Assuming that the 4 previous bits were detected correctly, DFE subtracts their influence from the currently received analog input voltage, thus cancelling their post-cursor ISI. Note that DFE cannot cancel pre-cursor ISI, because the cursor bit

has not been sliced yet.

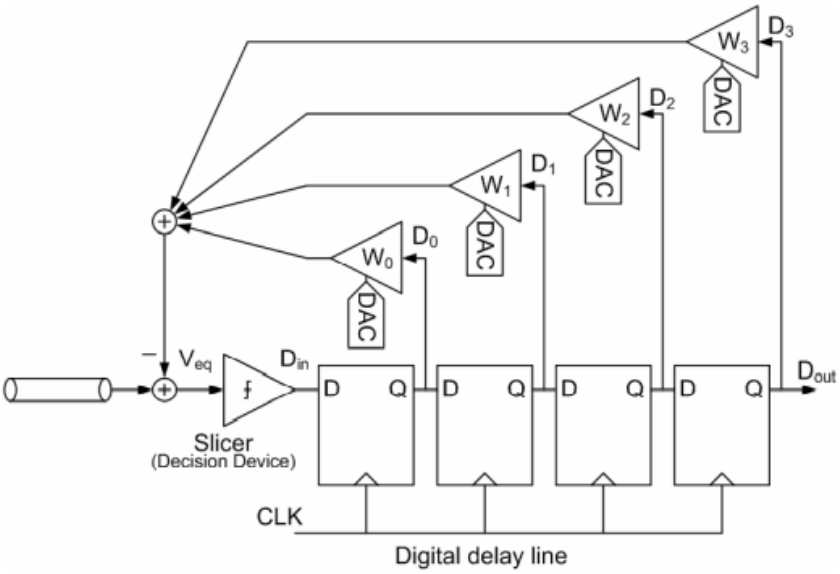

Figure 2.3: Decision-feedback equalizer on the receiver side [5]

Nevertheless, DFE is very useful, because due to its non-linear nature (it contains a comparator), it does not amplify high-frequency noise from the channel. It is susceptible to error propagation, however, meaning that if a bit has been incorrectly detected, its ISI will not be corrected properly, leading to error propagating to the current bit. While this may cause chains of errors in low-SNR channels (like wireless), such error propagation is much less probable in higher-reliability short-reach copper links.

2.3 Digital Equalizer Implementations

Implementing a filter in digital domain allows one to compute filtering results with higher resolution in digital domain and then round them off only once to the closest data converter level. This is in contrast with semi-digital implementation, where the value of each tap is rounded off, leading to accumulation of rounding errors. This problem is illustrated in Figure 2.4. Only three taps are shown for simplicity, but one can imagine the problem only getting worse for more taps. To understand this issue more fully, we can view the operation of the filter as a function of data bits as moving along a tree. The "root" of the tree is output for no filter taps. For one single tap, depending

whether the previous data bit was 0 or 1, the filter output branches to either (–W0) or W0. If the filter has two taps, depending on whether data bits were 00, 01, 10, or 11, there are four possibilities for the filter output: (-W1,-W0), (-W1,+W0), (+W1,-W0), and (+W1,+W0). For 3 taps, there are 8 possible outputs, and for N_{taps} $taps - 2^{N_{taps}}$. Figure 2.4(a) shows the tree without any quantization. Figure 2.4(b) illustrates how quantization of each individual tap weight leads to error accumulation. Finally, Figure 2.4(c) shows that computing filter output with higher precision in digital domain and then rounding solves the error accumulation problem.

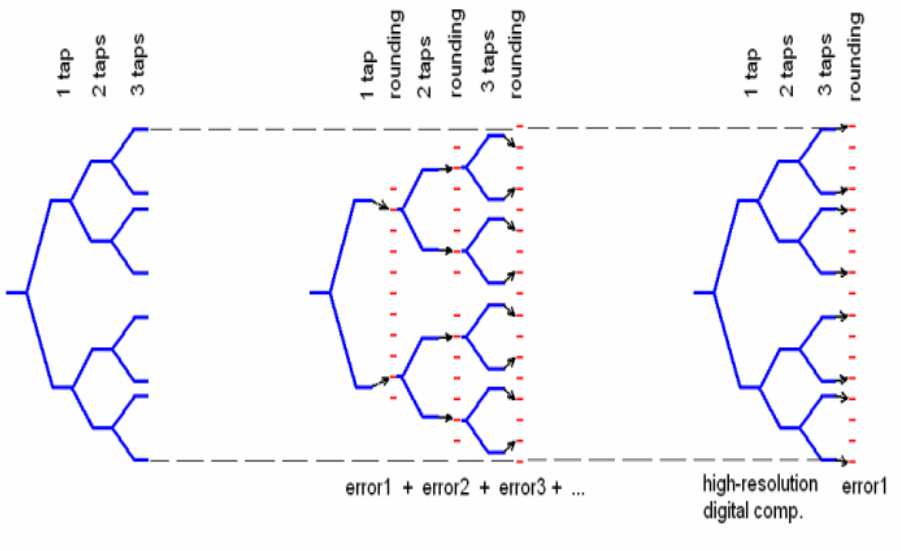

Figure 2.4: FIR filter output as a function of input bits (a) without any quantization, (b) with each tap weight Wi quantized separately, and (c) with filter output computed digitally with high resolution and then rounded off to the closest available data converter level [5]

Unfortunately, implementing a digital filter at high speed and with high resolution is also problematic. Thus, instead of performing digital computations on-the-fly, look-up tables (LUTs) can be used, as demonstrated by B. Casper, et. al. in [6] for transmit equalization.

2.4 ADC for Receiver Equalization

Apart from digital filters, the digital transmit equalizer requires a baud-rate DAC, while the digital receive equalizer requires a baud-rate ADC. As baud rates of modern links extend well into Gbps range, both DACs and ADCs operating at such rates are large research topics in themselves. In this work, we focus only on designing high-speed ADCs for the link receivers. The complexity, and even feasibility, of this task as well as the choice of the ADC topology depend on system requirements for the ADC. While the baud rate of the link determines the sampling rate of the ADC, its resolution is defined by two considerations.

First, the LSB size must be small enough so that it does not noticeably degrade the noise margin of the link, defined by half a signal swing minus all bounded error sources. Equalization normally removes the precursor and postcursor ISI, leaving only the main cursor as a signal to be detected and reducing the useful signal swing by the sum of magnitudes of all pre- and post-cursors. On top of this attenuation, the bounded error sources include unequalized ISI, reflections, and crosstalk. The ADC quantization error becomes an additional bounded error source, and thus should be kept to a small fraction α of the main cursor. The value of α should be typically less than 10-20

Second, the ADC range must cover the entire swing of the receiver input, including the worst-case effects from the pre- and post-cursor ISI (unless they have been cancelled by the transmit equalizer). The worst-case signal swing is equal to the sum of magnitudes of all taps in a pulse response (pre- and post-cursors plus the cursor itself).

Given these two considerations, the number of ADC levels (

$$N_{levels} = 2^{N_{bits}}$$

) should be approximately:

$$N_{levels} = 2^{N_{bits}} = \sum_{i=-\infty}^{\infty} |P_i|/\alpha.P_0$$

where P_i is the ith tap in a channel pulse response, with i ¡ 0 for pre-cursors, i ¿ 0 for post-cursors and i = 0 for the main-cursor. α is the fraction of equalized signal amplitude allocated to quantization error of the ADC. Taking $\alpha = 10\%$ and pulse response shown in Figure 2.2 as an example, we obtain $Nlevels = 20$ *and* $Nbits = 4.3$. As it turns out, for most typical backplane channels, Nbits of 4-5 bits is required. Thus, for this work, we will target a resolution of 6-7 bits.

Chapter 3

Sub-ADC Design

Figure 3.1 shows the common ADC topologies used in these serial links, which include flash, binary/multibit search, and successive approximation register (SAR). Flash ADCs employ comparators at each reference level, with a 6-b flash ADC requiring 63 comparators that simultaneously evaluate over a single cycle. This allows for very high-speed operation with relatively low time-interleave factors between four and eight. The main downside is the large comparator count, although rectifying architectures can reduce this. Overall, flash ADCs are a reasonable choice for PAM2, but the resolution is a bit low for PAM4.

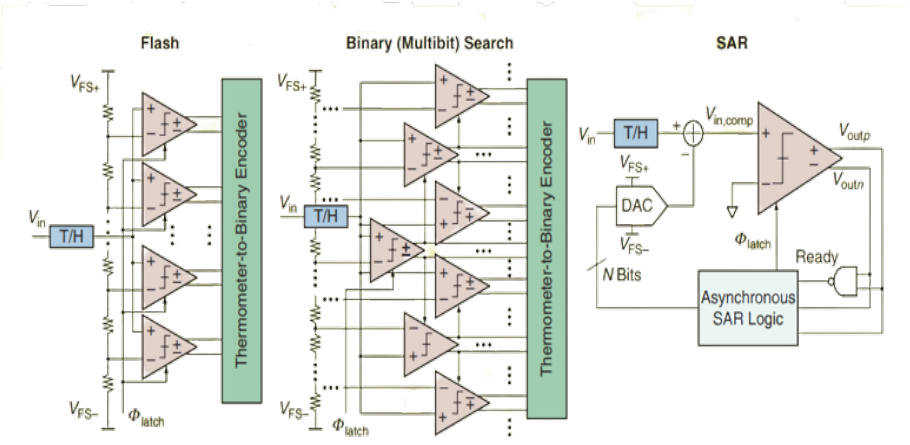

Figure 3.1: The common ADC topologies used in serial link receivers. [7]

Binary or multi-bit search ADCs combine desirable properties of flash and SAR ADCs. While conventional binary search ADCs have the same number of comparators as a flash ADC, the architecture employs a binary search algorithm with the most significant bit (MSB) comparator's output deciding which MSB-1 comparator is clocked, and so on. This results in only the necessary comparators evaluating, or six in a 6-b converter. The binary search ADC avoids the digital-to-analog converter (DAC) settling and logic delay present in SARs but is slower than a flash due to the serial comparator evaluation. Overall, this is also a good choice for PAM-2 applications, but the area is often high for PAM-4 applications.

An SAR ADC employs a binary search conversion over multiple clock cycles. The simplest implementations require only one comparator per unit ADC, whose decision adjusts a reference DAC to make the full signal quantization in a successive approximation manner, with a 6-b converter clocking the comparator six times. This results in a slower unit ADC relative to flash or binary search, with high-speed converters using higher interleave factors of 32–128. This is an excellent choice for 6–8-b resolution to support both PAM-2 and PAM-4, and it is the dominant architecture for PAM-4 ADC-based receivers. Given this, the next section provides an overview of key ADC circuits in the context of a time-interleaved SAR ADC. Note that many of the circuit concepts are also relevant to other ADC topologies.

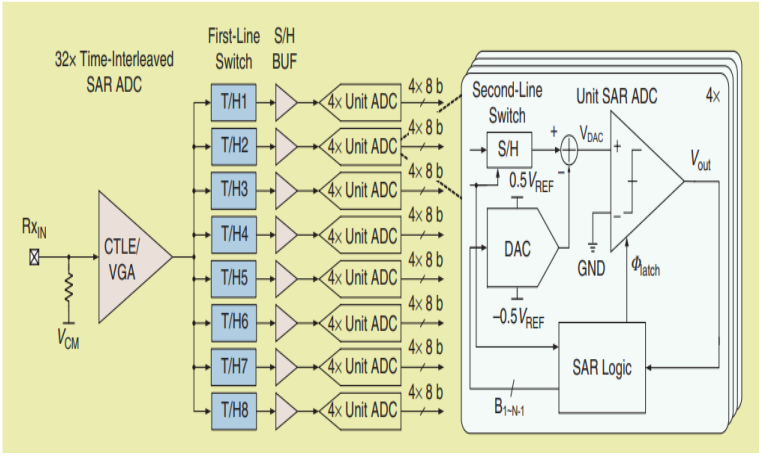

Figure 3.2: A 32-way time-interleaved SAR ADC. GND: ground; S/H BUF: sample/hold buffer. [7]

3.1 Sampling Switch

The input T/H circuit must track and sample/hold the full-bandwidth input signal for further sampling by the unit ADCs. Due to this high-bandwidth requirement, many high-speed ADCs employ a bootstrapped T/H switch [11]. The collection of transistors and the offset storage capacitor shown in Figure 5 produce a signal independent overdrive on the main sampling switch to keep the tracking bandwidth constant. When the clock is low and the switch is off, the capacitor is precharged to VDD. One terminal of the capacitor is then connected to the input when the clock goes high, forcing the other terminal to VDD above it, which should result in a signal-independent VDD overdrive on the switch when it is on. This results in an improvement in signal-to-noise-and-distortion ratio (SNDR), particularly at high frequencies.

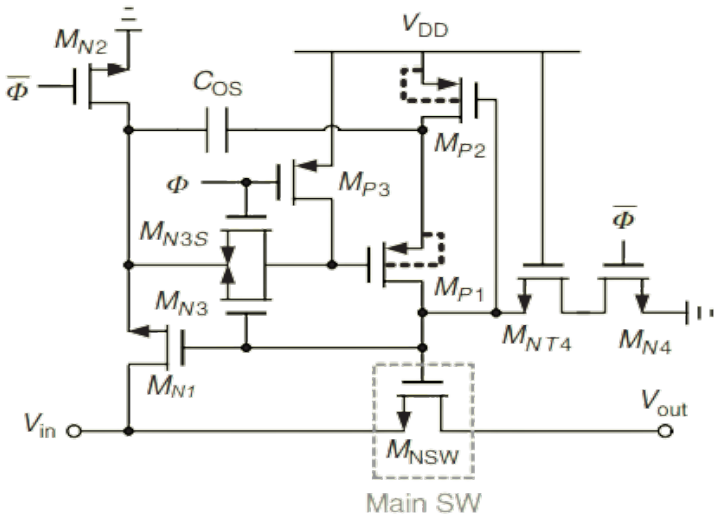

Figure 3.3: Bootstrapped T/H [7]

After the second-line switch, the unit ADC consists of the capacitive reference DAC, the comparator, and SAR logic. The DAC generates residue signals for each bit conversion by subtracting a binary weighted reference from the sampled input signal. This is done via charge sharing in a capacitive DAC, with a typical $65\,nm$ CMOS implementation.

3.2 StrongARM Latch

The comparator is a sense amplifier that is desgined by using a StrongARM Latch topology. The StrongARM latch topology finds wide usage as a sense amplifier, a comparator, or simply a robust latch with high sensitivity. The term "StrongARM" commemorates the use of this circuit in Digital Equipment Corporation's StrongARM microprocessor, but the basic structure was originally introduced by Toshiba's Kobayashi. The StrongARM latch has become popular for three reasons:

1. it consumes zero static power
2. it directly produces rail-to-rail outputs
3. its input-referred offset arises from primarily one differential pair.

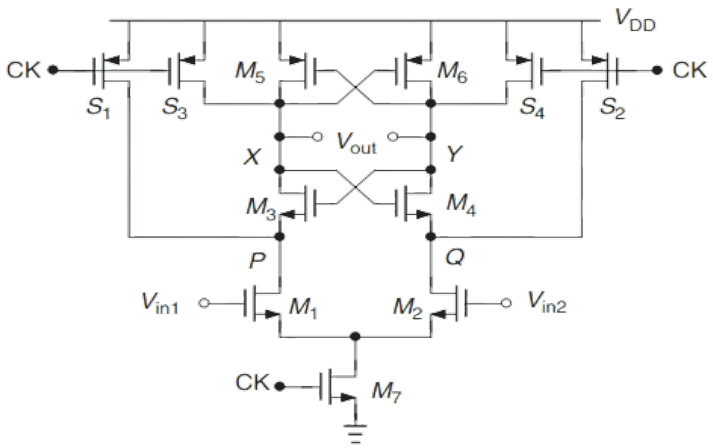

Figure 3.4: Modified StrongARM Latch [7]

The comparator makes a decision on the DAC signal to generate the output bits that serve as the binary search codes for the SAR logic that controls the DAC. Noise and offset considerations generally set the minimum comparator size. However, the brute-force design of a comparator for a given offset performance leads to excessive power and area in modern CMOS processes.

3.3 SAR Logic

Finally, the SAR logic generates both the comparator clock and the DAC control signals based on the comparator output. A conventional synchronous SAR ADC uses logic that generates an internal clock operating at N + 1 times the unit ADC sampling frequency to allow for one tracking cycle and N-bit conversion cycles. However, given metastability considerations, each cycle should be timed to satisfy the worst-case comparator input that will occur only once in the multi-bit conversion.

Chapter 4

Preliminary Results

The proposed SAR ADC architecture is being studied, researched, and simulated. So far, the bootstrapped T/H switch, and the StrongARM Latch have been simulated in Cadence Virtuoso tool. The channel has also been statistically modelled by including the effect of ADC's quantization noise in a SerDes link using MATLAB. The results are following sections.

4.1 Time Domain Analysis of SerDes Link

A RPBS sequence was generated and passed through an AWGN channel in a SerDes wireline channel. The eye diagram of the channel response was plotted as shown in Figure 4.1.

Next, quantization was added to the channel response in order to see the effect of including an ADC in the receiver. The waveforms clearly shows that an open eye can be achieved with a quantization of about 5-6 bits and nothing lower than that. The eye diagrams for quantization with 8, 5, and 3 bits have been plotted in Figure 4.2 to understand this phenomena.

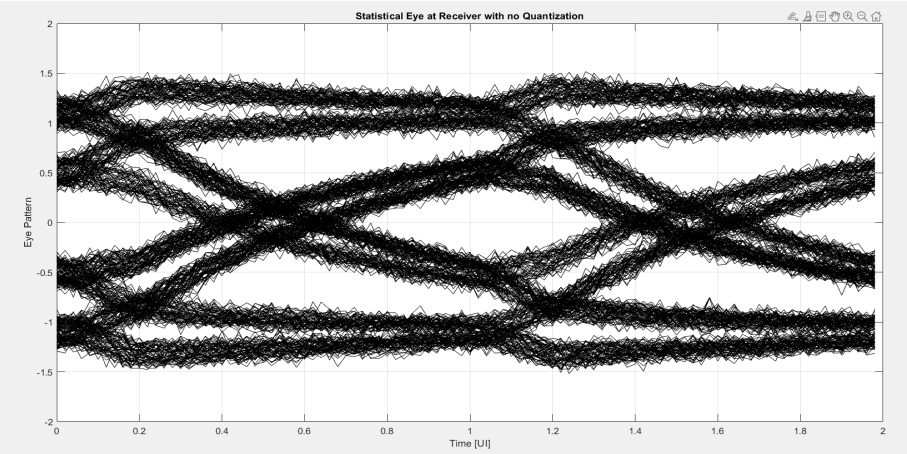

Figure 4.1: Statistical Eye with no Quantization

4.2 Design of Sub-ADC

4.2.1 Bootstrapped switch

A simple bootstrapped switch has been designed and simulated using the Cadence Virtuoso tool with $USMC$ $65\,nm$ PDK. The sampling frequency was chosen to be $1\,GHz$ and the message signal frequency was chosen to be $125\,MHz$. The resulting waveform can be seen in the Figure 4.3. Very little non-idealities and non-linearities can be observed which are negligible.

4.2.2 StrongARM Latch

A StrongARM Latch has also been simulated using Cadence Virtuoso tool in $USMC65\,nm$ PDK. The **Clock** was a pulse with a period of **1 GHz**. The input V_{in1} was **grounded**, whereas the input V_{in2} was connected to V_{DD}. The output clearly shows V_x reaches an output voltage of V_{DD}, while V_y settles to 0 voltage after a while within the clock cycle.

Another latch circuit has also been designed by clocking the differential pair through the cross-coupled NMOS pair in order to have a low kick-back current through the circuit when the circuit is in idle state. Its results can be seen in Figures 4.7-8. We

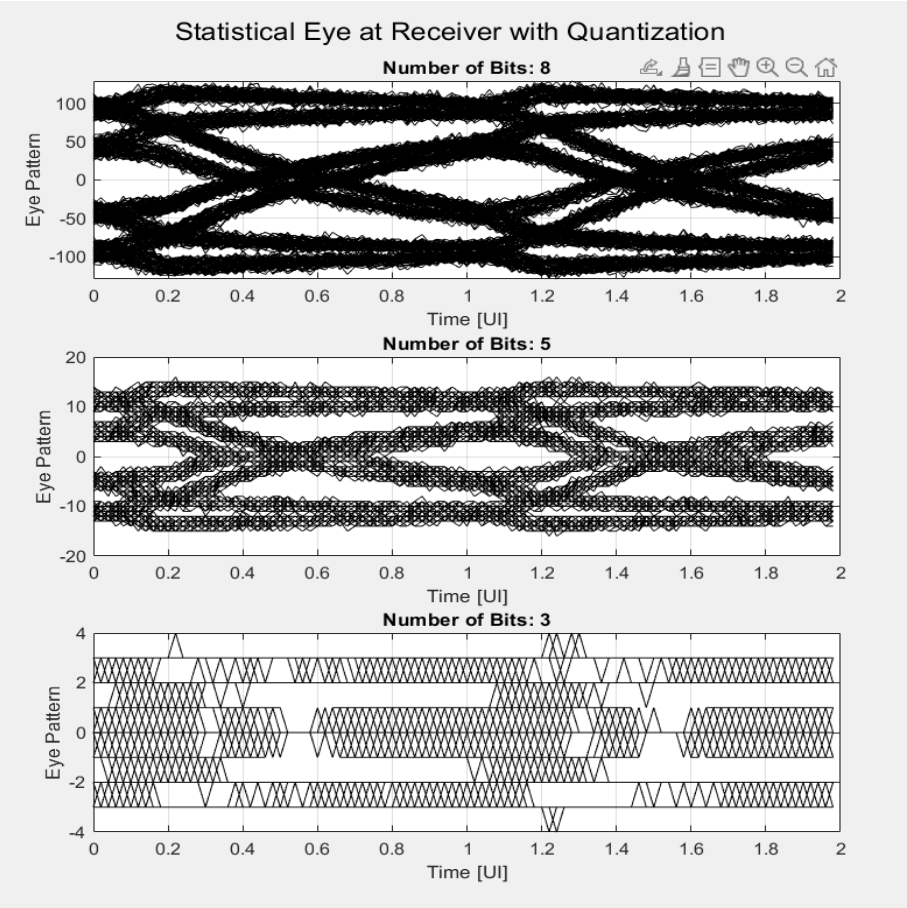

Figure 4.2: Statistical Eye with Quantization

can see that in the case of low kick-back circuit, the output voltages have more controlled peaks and peak only upto $1.3\,V$, whereas in the earlier case, the output voltages ($V_x \, and \, V_y$) peaked upto $1.4\,V$.

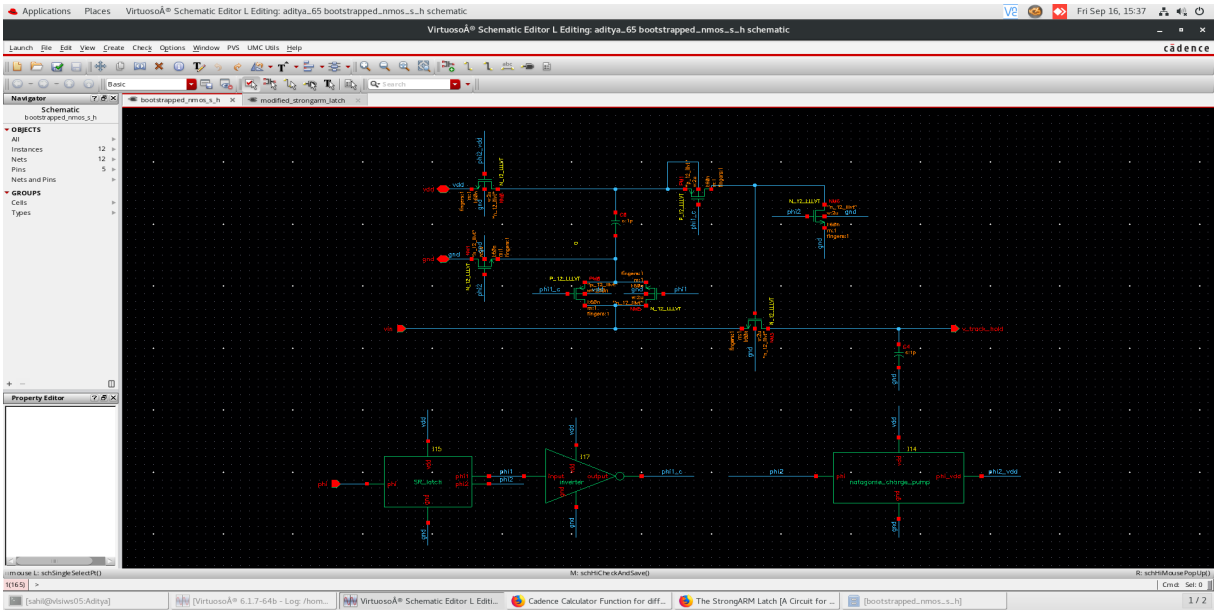

Figure 4.3: Bootstrapped Track and Hold Circuit Schematic

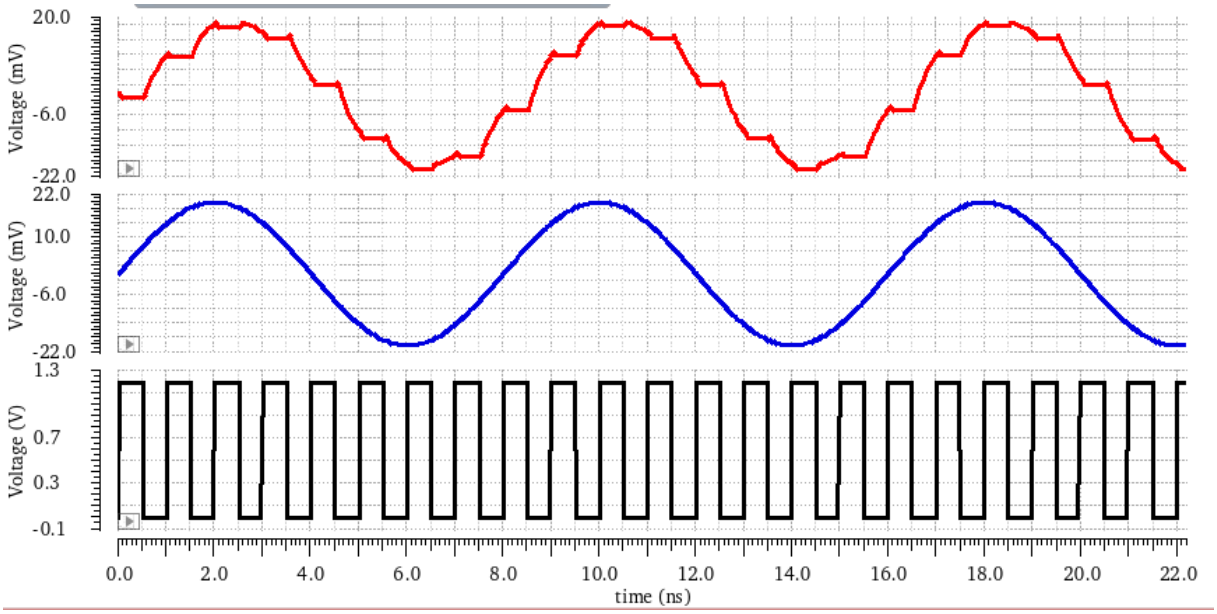

Figure 4.4: Bootstrapped Track and Hold Waveform

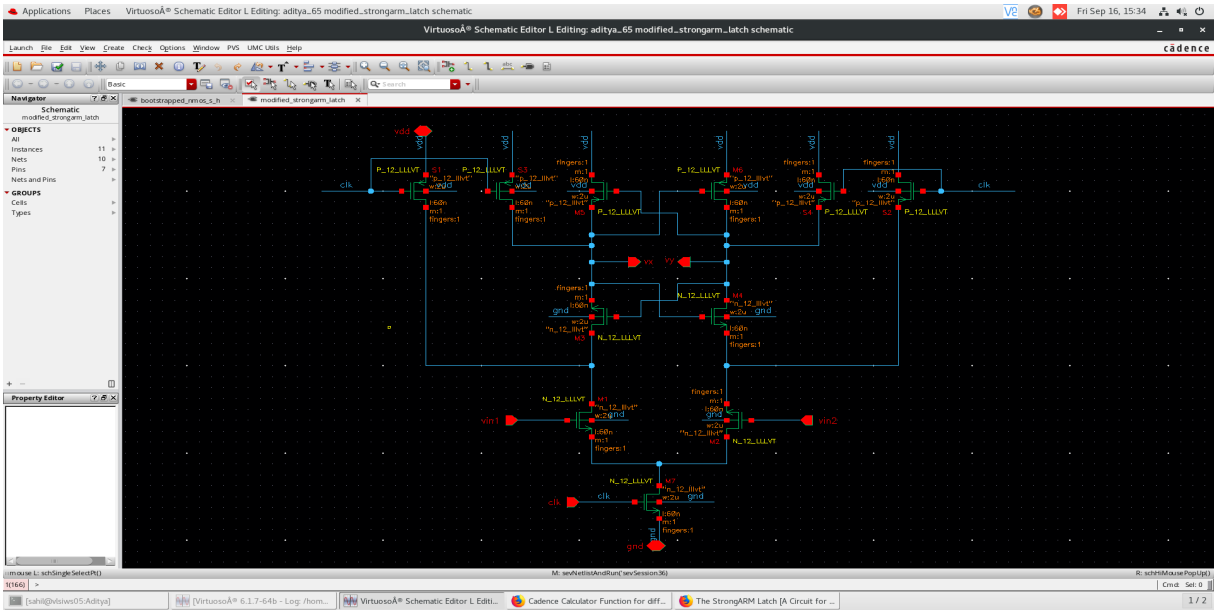

Figure 4.5: StrongARM Latch Circuit Schematic

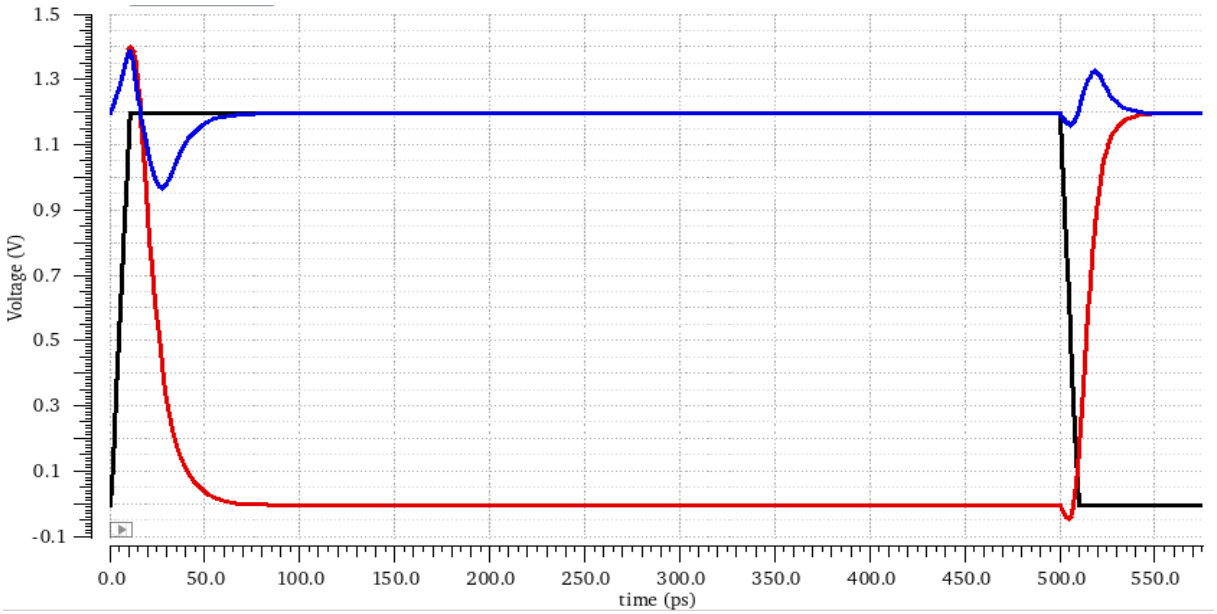

Figure 4.6: StrongARM Latch Output Waveform

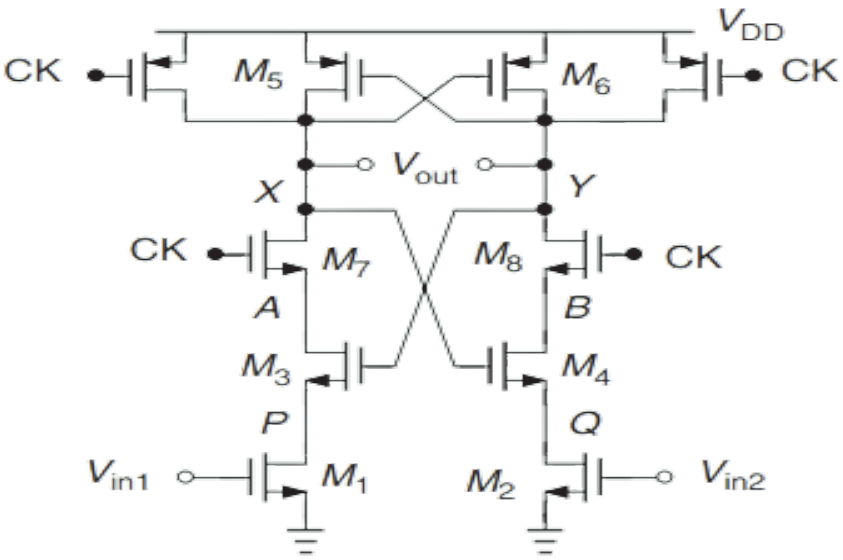

Figure 4.7: An alternative topology for lower kick-back noise [7]

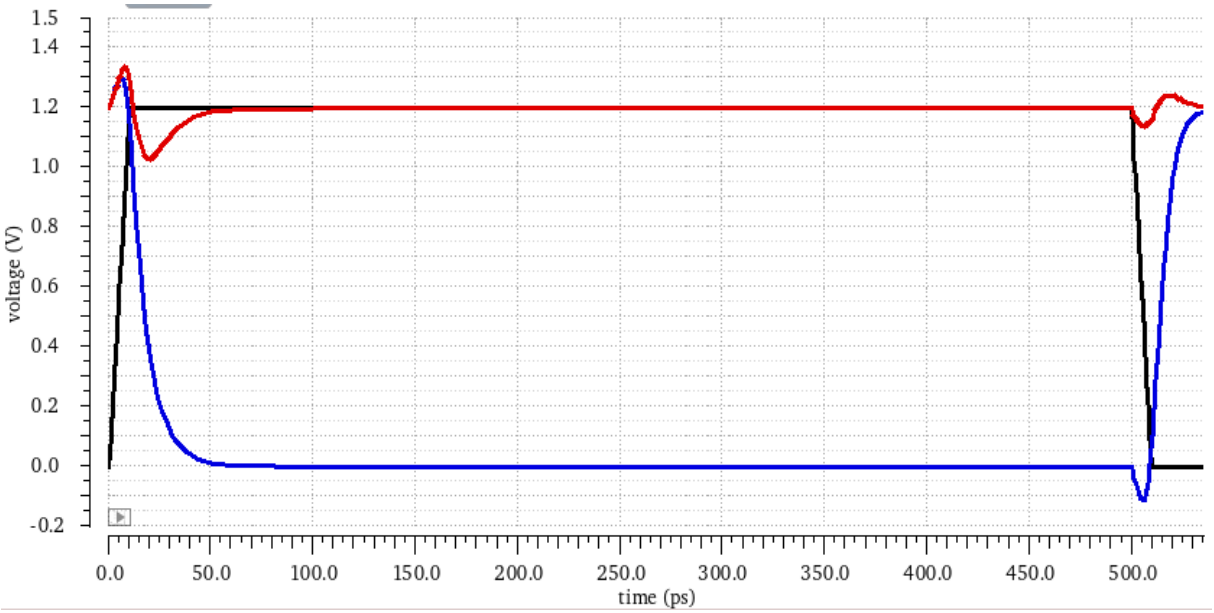

Figure 4.8: StrongARM Latch Low kick-back Output Waveform

Chapter 5

Conclusions and Future Work

5.1 Future Work to be Done

So far, the track and hold switch and slicer of the unit ADC have been designed and simulated using Cadence Virtuoso tool USMC 65 nm technology package. By the end of this semester, the complete design and simulation of the ADC is expected to be completed.

In the second part of my thesis, further enhancements will be made to the designed sub-ADC and will be made useful for integrating the ADC-based Receiver with SerDes links in real life.

5.2 Conclusions

The results thus far obtained of the circuits designed were found to be satisfactory as approved by me supervisor Dr Nijwm Wary. Few circuits in this report have been directly attached as screen shots taken from Cadence Virtuoso. I hereby, claim no responsibility of those diagrams. In future reports, I will take care that all the circuits will be drawn by me and the plots will be redrawn.

Chapter 6

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