

Diagram, schematic

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***1.Codul descrierii structurale explicite:***

module CD\_BCD7Seg\_s(D,C,B,A,ya,yb,yc,yd,ye,yf,yg);

input A,B,C,D;

output ya,yb,yc,yd,ye,yf,yg;

wire wa1,wa2; //wire pemtru output ya

wire wb1,wb2,wb3; //wire pentru output yb

wire wc1,wc2,wc3,wc4,wc5;//wire pentru output yc

wire wd1,wd2,wd3,wd4,wd5,wd6,wd7;//wire pentru output yd

wire we1,we2,we3;//wire pentru output ye

wire wf1,wf2,wf3,wf4,wf5;//wire pentru output yf

wire wg1,wg2,wg3,wg4,wg5;//wire pentru output yg

not(wa,A);// wire notA

not(wb,B);// wire notB

not(wc,C);// wire notC

not(wd,D);// wire notD

// iesirea a in ordinea ec. simplificate:

// gr.1 D`

// gr.2 B`

and(wa1,A,C);// gr.3 AC

and(wa2,wc,wa); // gr.4 C`A`

or(ya,wd,wb,wa1,wa2);//output ya

// iesirea b in ordinea ec. simplificate:

//gr.1 C

and(wb1,D,wb,wa);//gr.2 DB`A`

and(wb2,D,B,A);//gr.3 DBA

and(wb3,wd,B,wa);//gr.4 D`BA`

and(wb4,wd,wb,A);//gr.5 D`B`A

or(yb,C,wb1,wb2,wb3,wb4);//output yb

// iesirea c in ordinea ec. simplificate:

and(wc1,B,wa);//gr.1 BA`

and(wc2,C,wa);//gr.2 CA`

and(wc3,C,B);//gr.3 BC

and(wc4,D,wc);//gr.4 DC`

and(wc5,wd,wb,A);//gr.5 D`B`A

or(yc,wc1,wc2,wc3,wc4,wc5);//output yc

// iesirea d in ordinea ec. simplificate:

and(wd1,wd,C);//gr.1 D`C

and(wd2,wd,B);//gr.2 DB`

and(wd3,wd,wa);//gr.3 D`A`

and(wd4,A,C);//gr.4 AC

and(wd5,C,wb,wa);//gr.5 CB`A`

and(wd6,D,wb,A);//gr.6 DB`A

and(wd7,D,wc,B,wa);//gr.7 DCB`A`

or(yd,wd1,wd2,wd3,wd4,wd5,wd6,wd7);//output yd

// iesirea e in ordinea ec. simplificate:

and(we1,wd,wb);//gr.1 D`B`

and(we2,wb,A);//gr.2 B`A

and(we3,C,A);//gr.3 CA

or(ye,we1,we2,we3);//output ye

// iesirea f in ordinea ec. simplificate:

and(wf1,wd,wb);//gr.1 D`B`

and(wf2,wd,C);//gr.2 D`C

and(wf3,C,B,A);//gr.3 CBA

and(wf4,D,wc,B);//gr.4 DC`B

and(wf5,D,wc,A);//gr.5 DC`A

or(yf,wf1,wf2,wf3,wf4,wf5);//output yf

// iesirea g in ordinea ec. simplificate:

and(wg1,wd,B);//gr.1 D`B

and(wg2,wc,A);//gr.2 C`A

and(wg3,C,wb,wa);//gr.3 CB`A`

and(wg4,D,wb,A);//gr.4 DB`A

and(wg5,wc,B);//gr.5 C`B

or(yg,wg1,wg2,wg3,wg4,wg5);//output yg

endmodule

***2.Codul descrierii comportamentale:***

module CD\_BCD7Seg\_c(D,C,B,A,ya,yb,yc,yd,ye,yf,yg);

input D,C,B,A;

output ya,yb,yc,yd,ye,yf,yg;

reg ya,yb,yc,yd,ye,yf,yg;

always @(D or C or B or A)

case({D,C,B,A})

4'b0000:{ya,yb,yc,yd,ye,yf,yg}=7'b1001110;

4'b0001:{ya,yb,yc,yd,ye,yf,yg}=7'b1110111;

4'b0010:{ya,yb,yc,yd,ye,yf,yg}=7'b1111001;

4'b0011:{ya,yb,yc,yd,ye,yf,yg}=7'b1001001;

4'b0100:{ya,yb,yc,yd,ye,yf,yg}=7'b1111111;

4'b0101:{ya,yb,yc,yd,ye,yf,yg}=7'b1111110;

4'b0110:{ya,yb,yc,yd,ye,yf,yg}=7'b1111011;

4'b0111:{ya,yb,yc,yd,ye,yf,yg}=7'b1111111;

4'b1000:{ya,yb,yc,yd,ye,yf,yg}=7'b1110000;

4'b1001:{ya,yb,yc,yd,ye,yf,yg}=7'b1011111;

4'b1010:{ya,yb,yc,yd,ye,yf,yg}=7'b1011011;

4'b1011:{ya,yb,yc,yd,ye,yf,yg}=7'b0110011;

4'b1100:{ya,yb,yc,yd,ye,yf,yg}=7'b1111001;

4'b1101:{ya,yb,yc,yd,ye,yf,yg}=7'b1101101;

4'b1110:{ya,yb,yc,yd,ye,yf,yg}=7'b0110000;

4'b1111:{ya,yb,yc,yd,ye,yf,yg}=7'b1111110;

endcase

endmodule

***3.Codul pentru standul de test al descrierii structurale explicite:***

module CD\_BCD7Seg\_s\_tb;

reg A,B,C,D;

wire ya,yb,yc,yd,ye,yf,yg;

CD\_BCD7Seg\_s uut(D,C,B,A,ya,yb,yc,yd,ye,yf,yg);

initial begin

D=0;C=0;B=0;A=0;

#10D=0;C=0;B=0;A=1;

#10D=0;C=0;B=1;A=0;

#10D=0;C=0;B=1;A=1;

#10D=0;C=1;B=0;A=0;

#10D=0;C=1;B=0;A=1;

#10D=0;C=1;B=1;A=0;

#10D=0;C=1;B=1;A=1;

#10D=1;C=0;B=0;A=0;

#10D=1;C=0;B=0;A=1;

#10D=1;C=0;B=1;A=0;

#10D=1;C=0;B=1;A=1;

#10D=1;C=1;B=0;A=0;

#10D=1;C=1;B=0;A=1;

#10D=1;C=1;B=1;A=0;

#10D=1;C=1;B=1;A=1;

end

initial

$monitor("D=%b,C=%b,B=%b,A=%b,ya=%b,yc=%b,yc=%b,yA=%b,ye=%b,yf=%b,yg=%b",D,C,B,A,ya,yb,yc,yd,ye,yf,yg);

Endmodule

***4. Codul pentru standul de test al descrierii comportamentale:***

module CD\_BCD7Seg\_c\_tb;

reg A,B,C,D;

wire ya,yb,yc,yd,ye,yf,yg;

CD\_BCD7Seg\_c uut(D,C,B,A,ya,yb,yc,yd,ye,yf,yg);

initial begin

D=0;C=0;B=0;A=0;

#10D=0;C=0;B=0;A=1;

#10D=0;C=0;B=1;A=0;

#10D=0;C=0;B=1;A=1;

#10D=0;C=1;B=0;A=0;

#10D=0;C=1;B=0;A=1;

#10D=0;C=1;B=1;A=0;

#10D=0;C=1;B=1;A=1;

#10D=1;C=0;B=0;A=0;

#10D=1;C=0;B=0;A=1;

#10D=1;C=0;B=1;A=0;

#10D=1;C=0;B=1;A=1;

#10D=1;C=1;B=0;A=0;

#10D=1;C=1;B=0;A=1;

#10D=1;C=1;B=1;A=0;

#10D=1;C=1;B=1;A=1;

end

initial $monitor("D=%b,C=%b,B=%b,A=%b,ya=%b,yb=%b,yc=%b,yd=%b,ye=%b,yf=%b,yg=%b",D,C,B,A,ya,yb,yc,yd,ye,yf,yg);

endmodule

***5. Codul pentru standul de test pentru verificarea echivalentei:***

module CD\_BCD7Seg\_eq\_tb;

reg D,C,B,A;

wire yas,ybs,ycs,yds,yes,yfs,ygs;

wire yac,ybc,ycc,ydc,yec,yfc,ygc;

wire eq1,eq2,eq3,eq4,eq5,eq6,eq7;

CD\_BCD7Seg\_s uut1(D,C,B,A,yas,ybs,ycs,yds,yes,yfs,ygs);

CD\_BCD7Seg\_c uut2(D,C,B,A,yac,ybc,ycc,ydc,yec,yfc,ygc);

initial begin

D=0;C=0;B=0;A=0;

#10D=0;C=0;B=0;A=1;

#10D=0;C=0;B=1;A=0;

#10D=0;C=0;B=1;A=1;

#10D=0;C=1;B=0;A=0;

#10D=0;C=1;B=0;A=1;

#10D=0;C=1;B=1;A=0;

#10D=0;C=1;B=1;A=1;

#10D=1;C=0;B=0;A=0;

#10D=1;C=0;B=0;A=1;

#10D=1;C=0;B=1;A=0;

#10D=1;C=0;B=1;A=1;

#10D=1;C=1;B=0;A=0;

#10D=1;C=1;B=0;A=1;

#10D=1;C=1;B=1;A=0;

#10D=1;C=1;B=1;A=1;

end

assign eq1=(yas==yac);

assign eq2=(ybs==ybc);

assign eq3=(ycs==ycc);

assign eq4=(yds==ydc);

assign eq5=(yes==yec);

assign eq6=(yfs==yfc);

assign eq7=(ygs==ygc);

initial

$monitor("D=%b,C=%b,B=%b,A=%b,yas=%b,ybs=%b,ycs=%b,yds=%b,yes=%b,yfs=%b,ygs=%b",

"yac=%b,yab=%b,ycc=%b,ydc=%b,yec=%b,yfc=%b,ygc=%b",

"eq1=%b,eq2=%b,eq3=%b,eq4=%b,eq5=%b,eq6=%b,eq7=%b"

,D,C,B,A,yas,ybs,ycs,yds,yes,yfs,ygs,

yac,ybc,ycc,ydc,yec,yfc,ygc,

eq1,eq2,eq3,eq4,eq5,eq6,eq7);

endmodule

***6.Captura de ecran pentru forma de unda a descrierii structurale explicite:***

A screenshot of a computer

Description automatically generated with medium confidence

***7.Captura de ecran pentru forma de unda a descrierii comportamentale:***

A screenshot of a computer

Description automatically generated

***8.Captura de ecran pentru forma de unda a verificarii echivalentei:*** A screenshot of a computer

Description automatically generated with medium confidence