Attention Please: Under the technology license agreement between MStar and Dolby/SRS/BBE, MStar is obliged not to provide samples that incorporate Dolby/SRS/BBE technology to any third party who is not a qualified licensee of Dolby/SRS/BBE respectively.

FEATURES

- LCD TV controller with PIP display functions
- Input supports up to UXGA & 1080P
- Panel supports up to full HD (1920x1080)
- TV decoder with 3-D comb filter
- Multi-standard TV sound demodulator and decoder
- 10-bit triple-ADC for TV and RGB/YPbPr
- 10-bit video data processing
- Integrated DVI/HDCP/HDMI compliant receiver
- High-quality dual scaling engines & dual 3-D video de-interlacers
- 3-D video noise reduction
- MStarACE-3 picture/color processing engine
- Embedded On-Screen Display (OSD) controller engine
- Built-in MCU supports PWM & GPIO
- Built-in dual-link 8/10-bit LVDS transmitter
- 5-volt tolerant inputs
- Low EMI and power saving features
- 216-pin LQFP

■ NTSC/PAL/SECAM Video Decoder

- Supports NTSC M, NTSC-J, NTSC-4.43, PAL (B,D,G,H,M,N,I,Nc), and SECAM
- Automatic TV standard detection
- 3-D Comb filter for NTSC/PAL
- 5 configurable CVBS & Y/C S-video inputs
- Supports Closed-caption, and V-chip
- CVBS video output

■ Video IF for Multi-Standard Analog TV

- Digital low IF architecture
- Stepped-gain PGA with 26 dB tuning range and 1 dB tuning resolution
- Maximum IF analog gain of 37dB in addition to digital gain
- Programmable TOP to accommodate different tuner gain to optimize noise and linearity performance

■ Multi-Standard TV Sound Decoder

- Supports BTSC/A2/EIA-J demodulation and decoding
- FM stereo & SAP demodulation
- L/Rx2 and SIF audio inputs
- L/Rx2 loudspeaker and line outputs
- Supports sub-woofer output
- Built-in audio output DAC's
- Audio processing for loudspeaker channel, including volume, balance, mute, tone, and P/G EQ
- Support MP3 decode
- Optional advanced surround available (Dolby[1], SRS[2], BBE[3]... etc) **Note**

■ Digital Audio Interface

- S/PDIF digital audio input & output
- HDMI audio channel processing capability
- Programmable delay for audio/video synchronization

■ Analog RGB Compliant Input Ports

- Two analog ports support up to UXGA
- Supports HDTV RGB/YPbPr/YCbCr
- Supports Composite Sync and SOG (Sync-on-Green) separator
- Automatic color calibration

■ DVI/HDCP/HDMI Compliant Input Port

- Two DVI/HDMI input ports with built-in switch
- Supports TMDS clock up to 225MHz @ 1080P 60Hz with 12-bit deep-color resolution
- Single link on-chip DVI 1.0 compliant receiver
- High-bandwidth Digital Content Protection (HDCP) 1.1 compliant receiver
- High Definition Multimedia Interface (HDMI) 1.3 compliant receiver with CEC support

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[1] Trademark of Dolby Laboratories
[2] Trademark of SRS Labs, Inc.
[3] Registered trademark of BBE Sound, Inc.

- Long-cable tolerant robust receiving
- Support HDTV up to 1080P

■ Auto-Configuration/Auto-Detection
- Auto input signal format and mode detection
- Auto-tuning function including phasing, positioning, offset, gain, and jitter detection
- Sync detection for H/V Sync

■ High-Performance Scaling Engines
- Fully programmable shrink/zoom capabilities
- Nonlinear video scaling supports various modes including Panorama

■ Video Processing & Conversion
- 3-D motion adaptive video de-interlacer
- Edge-oriented adaptive algorithm for smooth low-angle edges
- Automatic 3:2 pull-down & 2:2 pull-down detection and recovery
- PIP with programmable size and location, supports multi-video applications
- MStar 3rd Generation Advanced Color Engine (MStarACE-3) automatic picture enhancement gives:
  - Brilliant and fresh color
  - Intensified contrast and details
  - Vivid skin tone
  - Sharp edge
  - Enhanced depth of field perception
  - Accurate and independent color control
- sRGB compliance allows end-user to experience the same colors as viewed on CRTs and other displays
- Programmable 12-bit RGB gamma CLUT
- 3-D video noise reduction
- Frame rate conversion

■ On-Screen OSD Controller
- 16/256 color palette
- 512 1/2/4/8-bit per pixel fonts
- Supports texture function
- Supports 4K attribute/code
- Horizontal and vertical stretch of OSD menus
- Pattern generator for production test
- Supports OSD MUX and alpha blending capability
- Supports blinking and scrolling for closed caption applications

■ LVDS Panel Interface
- Supports 8/10-bit dual link LVDS up to full HD (1920x1080)
- Supports 2 data output formats: Thine & TI data mappings
- Compatible with TIA/EIA
- Dithering with 6/8 bits options
- Reduced swing for LVDS for low EMI
- Supports flexible spread spectrum frequency with 360Hz~11.8MHz and up to 25% modulation

■ Integrated Micro Controller
- Embedded 8032 micro controller
- Configurable PWM's and GPIO's
- Low-speed ADC inputs for system control
- SPI bus for external flash
- Supports external MCU option controlled through 4-wire double-data-rate direct MCU bus or 8-bit direct MCU bus

■ External Connection/Component
- USB 2.0 port with internal switch to host controller
- 16-bit data bus for external frame buffer (DDR DRAM)
- All system clocks synthesized from a single external clock

GENERAL DESCRIPTION

The MST6M16GS is a high performance and fully integrated IC for multi-function LCD monitor/TV with resolutions up to full HD (1920x1080). It is configured with an integrated triple-ADC/PLL, an integrated DVI/HDCP/HDMI receiver, a multi-standard TV video and audio decoder, a video de-interlacer, a scaling engine, the MStarACE-3 color engine, an on-screen display controller, an 8-bit MCU and a built-in output panel interface. By use of external frame buffer, PIP/POP is provided for multimedia applications. Furthermore, 3-D video decoding and processing are fulfilled for high-quality TV applications. To further reduce system costs, the MST6M16GS also integrates intelligent power management control capability for green-mode requirements and spread-spectrum support for EMI management.

PIN DIAGRAM (MST6M16GS)
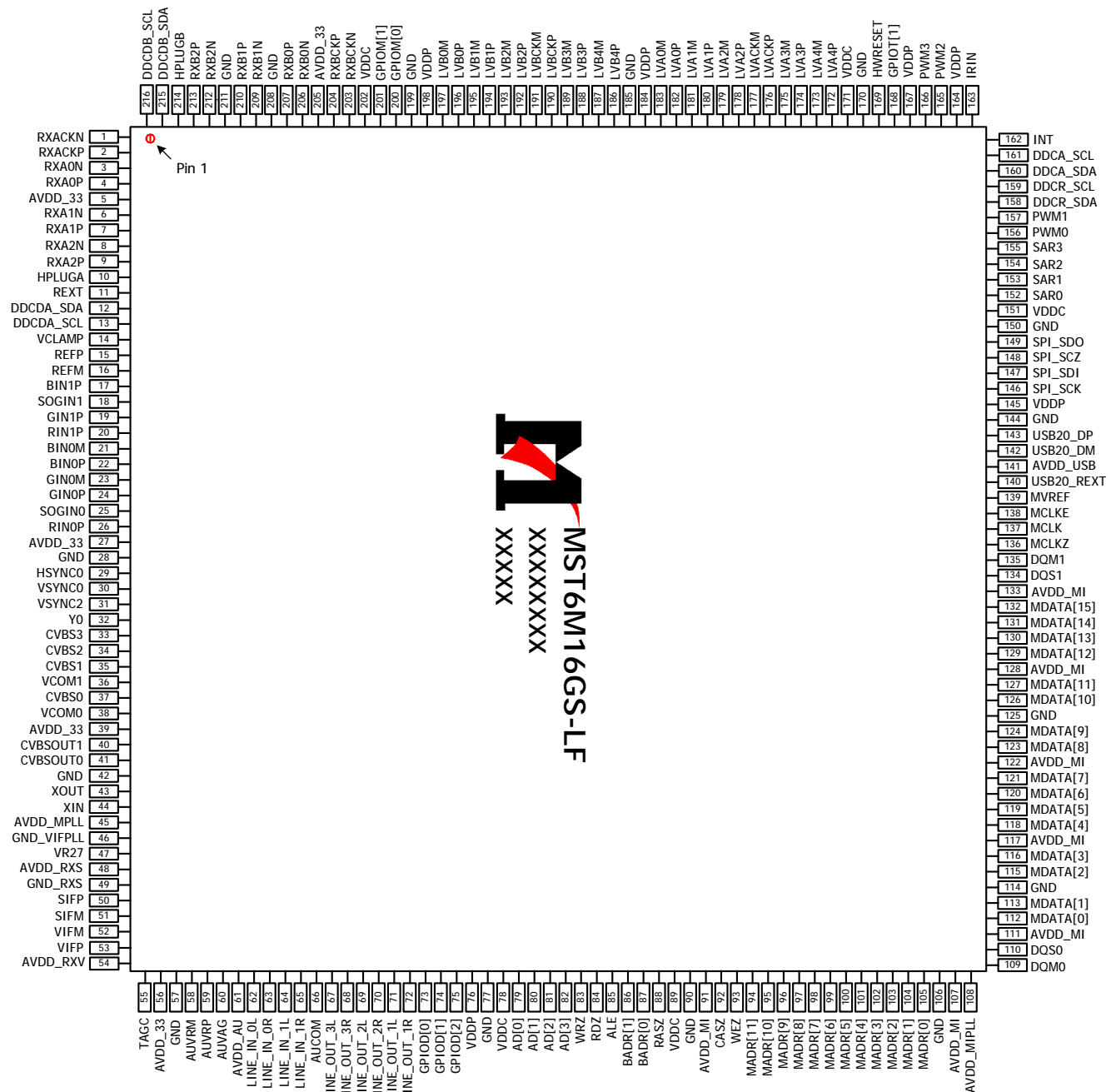
PIN DESCRIPTION

MCU Interface

Pin Name	Pin Type	Function	Pin
AD[3]	I/O w/5V-tolerant	MCU 4-bit DDR Direct Bus; 4mA driving strength	82
AD[2:0]	I/O (not 5V-tolerant)	MCU 4-bit DDR Direct Bus; 4mA driving strength	81-79
WRZ	I/O w/ 5V-tolerant	MCU Bus WDZ, active low	83
RDZ	I/O w/ 5V-tolerant	MCU Bus RDZ, active	84
ALE	I/O w/ 5V-tolerant	MCU Bus ALE, active high	85
SPI_SCK	Output (not 5V-tolerant)	SPI Flash Serial Clock	146
SPI_SDI	Output (not 5V-tolerant)	SPI Flash Serial Data Input	147
SPI_SCZ	Output (not 5V-tolerant)	SPI Flash Chip Select	148
SPI_SDO	Input w/ 5V-tolerant	SPI Flash Serial Data Output	149
INT	I/O w/ 5V-tolerant	External Interrupt Input/Output	162
HWRESET	Schmitt Trigger Input w/ 5V-tolerant	Hardware Reset; active high	169

Analog Video Interface

Pin Name	Pin Type	Function	Pin
REXT	Analog Input	External Resister 390 ohm to AVDD_33	11
VCLAMP		CVBS/YC Mode Clamp Voltage Bypass	14
REFP		Internal ADC Reference Top De-coupling Pin	15
REFM		Internal ADC Reference Bottom De-coupling Pin	16
HSYNC0	Schmitt Trigger Input w/ 5V-tolerant	Analog HSYNC Input from Channel 0	29
VSYNC0	Schmitt Trigger Input w/ 5V-tolerant	Analog VSYNC Input from Channel 0	30
VSYNC2	Schmitt Trigger Input w/ 5V-tolerant	Analog VSYNC Input from Channel 2	31
BIN0M	Analog Input	Reference Ground for Analog Blue Input from Channel 0	21
BIN0P	Analog Input	Analog Blue Input from Channel 0	22
GIN0M	Analog Input	Reference Ground for Analog Green Input from Channel 0	23
GIN0P	Analog Input	Analog Green Input from Channel 0	24
SOGIN0	Analog Input	Sync-On-Green Input from Channel 0	25
RIN0P	Analog Input	Analog Red Input from Channel 0	26
BIN1P	Analog Input	Analog Blue Input from Channel 1	17

Pin Name	Pin Type	Function	Pin
SOGIN1	Analog Input	Sync-On-Green Input from Channel 1	18
GIN1P	Analog Input	Analog Green Input from Channel 1	19
RIN1P	Analog Input	Analog Red Input from Channel 1	20
Y0	Analog Input	Luma Video Input 0 / CVBS Input Channel 4 (CVBS4)	32
CVBS3	Analog Input	Analog CVBS (Composite) / S-Video (Y/C) Input Channel 3	33
CVBS2	Analog Input	Analog CVBS (Composite) / S-Video (Y/C) Input Channel 2	34
CVBS1	Analog Input	Analog CVBS (Composite) / S-Video (Y/C) Input Channel 1	35
CVBS0	Analog Input	Analog CVBS (Composite) / S-Video (Y/C) Input Channel 0	37
VCOM1	Analog Input	Common Analog Input Reference Ground 1 (for CVBS/ADCB)	36
VCOM0	Analog Input	Common Analog Input Reference Ground 0 (for CVBS/ADCB)	38
CVBSOUT1	Analog Output	CVBS (Composite) Video Output Channel 1	40
CVBSOUT0	Analog Output	CVBS (Composite) Video Output Channel 0	41

Analog Audio Interface

Pin Name	Pin Type	Function	Pin
AUVRM	Analog Output	Negative Reference Voltage for Audio ADC	58
AUVRP	Analog Output	Positive Reference Voltage for Audio ADC	59
AUVAG	Analog Output	Reference Voltage for Audio Common Mode	60
LINE_IN_0L	Analog Input	Audio Line Input Left Channel 0	62
LINE_IN_0R	Analog Input	Audio Line Input Right Channel 0	63
LINE_IN_1L	Analog Input	Audio Line Input Left Channel 1	64
LINE_IN_1R	Analog Input	Audio Line Input Right Channel 1	65
AUCOM	Analog Input	Reference Ground for Audio Line Input	66
LINE_OUT_1L	Analog Output	Main Audio Output Left Channel 1 (DA0)	71
LINE_OUT_1R	Analog Output	Main Audio Output Right Channel 1 (DA0)	72
LINE_OUT_2L	Analog Output	Main Audio Output Left Channel 2 (AA1)	69
LINE_OUT_2R	Analog Output	Main Audio Output Right Channel 2 (AA1)	70
LINE_OUT_3L	Analog Output	Main Audio Output Left Channel 3 (AA0)	67
LINE_OUT_3R	Analog Output	Main Audio Output Right Channel 3 (AA0)	68

DVI/HDMI Interface

Pin Name	Pin Type	Function	Pin
RXACKN	DVI/HDMI Input	Negative DVI/HDMI Input for A Link Clock Channel	1
RXACKP	DVI/HDMI Input	Positive DVI/HDMI Input for A Link Clock Channel	2
RXA0N	DVI/HDMI Input	Negative DVI/HDMI Input for A Link Data Channel 0	3
RXA0P	DVI/HDMI Input	Positive DVI/HDMI Input for A Link Data Channel 0	4
RXA1N	DVI/HDMI Input	Negative DVI/HDMI Input for A Link Data Channel 1	6
RXA1P	DVI/HDMI Input	Positive DVI/HDMI Input for A Link Data Channel 1	7
RXA2N	DVI/HDMI Input	Negative DVI/HDMI Input for A Link Data Channel 2	8
RXA2P	DVI/HDMI Input	Positive DVI/HDMI Input for A Link Data Channel 2	9
RXBCKN	DVI/HDMI Input	Negative DVI/HDMI Input for B Link Clock Channel	203
RXBCKP	DVI/HDMI Input	Positive DVI/HDMI Input for B Link Clock Channel	204
RXB0N	DVI/HDMI Input	Negative DVI/HDMI Input for B Link Data Channel 0	206
RXB0P	DVI/HDMI Input	Positive DVI/HDMI Input for B Link Data Channel 0	207
RXB1N	DVI/HDMI Input	Negative DVI/HDMI Input for B Link Data Channel 1	209
RXB1P	DVI/HDMI Input	Positive DVI/HDMI Input for B Link Data Channel 1	210
RXB2N	DVI/HDMI Input	Negative DVI/HDMI Input for B Link Data Channel 2	212
RXB2P	DVI/HDMI Input	Positive DVI/HDMI Input for B Link Data Channel 2	213

LVDS Interface

Pin Name	Pin Type	Function	Pin
LVA0M	Output	LVDS A-Link Channel 0 Negative Data Output	183
LVA0P	Output	LVDS A-Link Channel 0 Positive Data Output	182
LVA1M	Output	LVDS A-Link Channel 1 Negative Data Output	181
LVA1P	Output	LVDS A-Link Channel 1 Positive Data Output	180
LVA2M	Output	LVDS A-Link Channel 2 Negative Data Output	179
LVA2P	Output	LVDS A-Link Channel 2 Positive Data Output	178
LVA3M	Output	LVDS A-Link Channel 3 Negative Data Output	175
LVA3P	Output	LVDS A-Link Channel 3 Positive Data Output	174
LVA4M	Output	LVDS A-Link Channel 4 Negative Data Output	173
LVA4P	Output	LVDS A-Link Channel 4 Positive Data Output	172
LVACKM	Output	LVDS A-Link Negative Clock Output	177
LVACKP	Output	LVDS A-Link Positive Clock Output	176
LVB0M	Output	LVDS B-Link Channel 0 Negative Data Output	197

Pin Name	Pin Type	Function	Pin
LVB0P	Output	LVDS B-Link Channel 0 Positive Data Output	196
LVB1M	Output	LVDS B-Link Channel 1 Negative Data Output	195
LVB1P	Output	LVDS B-Link Channel 1 Positive Data Output	194
LVB2M	Output	LVDS B-Link Channel 2 Negative Data Output	193
LVB2P	Output	LVDS B-Link Channel 2 Positive Data Output	192
LVB3M	Output	LVDS B-Link Channel 3 Negative Data Output	189
LVB3P	Output	LVDS B-Link Channel 3 Positive Data Output	188
LVB4M	Output	LVDS B-Link Channel 4 Negative Data Output	187
LVB4P	Output	LVDS B-Link Channel 4 Positive Data Output	186
LVBCKM	Output	LVDS B-Link Negative Clock Output	191
LVBCKP	Output	LVDS B-Link Positive Clock Output	190

GPIO Interface

Pin Name	Pin Type	Function	Pin
GPIOD[2:0]	I/O (not 5V-tolerant)	General Purpose Input/Output	75-73
GPIOT[1]	I/O w/ 5V-tolerant	General Purpose Input/Output	168
GPIOM[1:0]	I/O w/ 5V-tolerant	General Purpose Input/Output	201, 200
SAR0	I/O (not 5V-tolerant)	SAR Low Speed ADC Input 0	152
SAR1	I/O (not 5V-tolerant)	SAR Low Speed ADC Input 1	153
SAR2	I/O (not 5V-tolerant)	SAR Low Speed ADC Input 2	154
SAR3	I/O (not 5V-tolerant)	SAR Low Speed ADC Input 3	155
PWM0	I/O (not 5V-tolerant)	Pulse Width Modulation Output; 4mA driving strength / MCU Configuration Input 0 During Reset / General Purpose Input/Output	156
PWM1	I/O (not 5V-tolerant)	Pulse Width Modulation Output; 4mA driving strength / MCU Configuration Input 1 During Reset / General Purpose Input/Output	157
PWM2	I/O (not 5V-tolerant)	Pulse Width Modulation Output; 4mA driving strength / General Purpose Input/Output	165
PWM3	I/O (not 5V-tolerant)	Pulse Width Modulation Output; 4mA driving strength / General Purpose Input/Output	166
IRIN	Input w/5V-tolerant	IR Receiver Input / General Purpose Input/Output	163

DRAM Interface

Pin Name	Pin Type	Function	Pin
BADR[1:0]	Output	DRAM Memory Bank Address	86, 87
RASZ	Output	Row Address Strobe; active low	88
CASZ	Output	Column Address Strobe; active low	92
WEZ	Output	Write Enable; active low	93
MADR[11:0]	Output	DRAM Memory Address	94-105
DQM[1:0]	Output	Data Mask for Low Byte; active high	135, 109
DQS[1:0]	I/O	Data Strobe	134, 110
MDATA[15:0]	I/O	DRAM Memory Data Bus	132-129, 127, 126, 124, 123, 121-118, 116, 115, 113, 112
MCLKZ	Output	DRAM Memory Negative Differential Clock	136
MCLK	Output	DRAM Memory Positive Differential Clock	137
MCLKE	Output	DRAM Memory Clock Enable	138
MVREF	Input	Reference Voltage for DDR SDRAM Interface	139

USB Interface

Pin Name	Pin Type	Function	Pin
USB20_REXT		USB External Resistor Pin; Connected through 900 ohm (±1%) Resistor to GND	140
USB20_DM	Analog I/O	USB 2.0 Inverting Data Input/Output	142
USB20_DP	Analog I/O	USB 2.0 Non-inverting Data Input/Output	143

VIF Interface

Pin Name	Pin Type	Function	Pin
VR27		Compensation Capacitor for Regulator	47
SIFP	Analog Input	Positive Sound IF Input	50
SIFM	Analog Input	Negative Sound IF Input	51
VIFM	Analog Input	Negative Video IF Input	52
VIFP	Analog Input	Positive Video IF Input	53
TAGC	Analog Output	Tuner Automatic Gain Control Output	55

Misc Interface

Pin Name	Pin Type	Function	Pin
XOUT	Analog Output	Crystal Oscillator Output	43
XIN	Analog Input	Crystal Oscillator Input	44
DDCR_SDA	I/O w/ 5V-tolerant	DDC Data for ROM	158
DDCR_SCL	I/O w/ 5V-tolerant	DDC Clock for ROM	159
DDCA_SDA	I/O w/ 5V-tolerant	DDC Data for Analog Interface; 4mA driving strength	160
DDCA_SCL	Input w/ 5V-Tolerant	DDC Clock for Analog Interface	161
HPLUGA	I/O w/ 5V-tolerant	Hot-plug control for DVI/HDMI Port A	10
HPLUGB	I/O w/ 5V-tolerant	Hot-plug control for DVI/HDMI Port B	214
DDCDA_SDA	I/O w/ 5V-Tolerant	DDC Data and HDCP Slave Serial Bus Data I/O for DVI/HDMI Port A; 4mA driving strength	12
DDCDA_SCL	Input w/ 5V-tolerant	DDC Clock and HDCP Slave Serial Bus Clock Input for DVI/HDMI Port A	13
DDCDB_SDA	I/O w/ 5V-Tolerant	DDC Data and HDCP Slave Serial Bus Data I/O for DVI/HDMI Port B; 4mA driving strength	215
DDCDB_SCL	Input w/ 5V-tolerant	DDC Clock and HDCP Slave Serial Bus Clock Input for DVI/HDMI Port B	216

Power Pins

Pin Name	Pin Type	Function	Pin
AVDD_33	3.3V Power	Analog Power	5, 27, 39, 56, 205
AVDD_MPLL	3.3V Power	MPLL Power	45
GND_VIFPLL	Ground	VIF PLL Ground	46
AVDD_RXS	3.3V Power	Sound Path Receiver Power	48
GND_RXS	Ground	Sound Path Receiver Ground	49
AVDD_RXV	3.3V Power	Video Path Receiver Power	54
AVDD_AU	3.3V Power	Audio Power	61
AVDD_MI	2.5V Power	Memory Interface Power	91, 107, 111, 117, 122, 128, 133
AVDD_MIPLL	3.3V Power	Memory Interface PLL Power	108
AVDD_USB	3.3V Power	USB Power	141
VDDC	1.2V Power	Digital Core Power	78, 89, 151, 171, 202
VDDP	3.3V Power	Digital Input/Output Power	76, 145, 164, 167, 184, 198

Pin Name	Pin Type	Function	Pin
GND	Ground	Ground	28, 42, 57, 77, 90, 106, 114, 125, 144, 150, 170, 185, 199, 208, 211

ELECTRICAL SPECIFICATIONS

Analog Interface Characteristics

Parameter	Min	Typ	Max	Unit
VIDEO ADC Resolution		10		Bits
DC ACCURACY				
Differential Nonlinearity		TBD	TBD	LSB
Integral Nonlinearity		TBD		LSB
VIDEO ANALOG INPUT				
Input Voltage Range				
Minimum			0.5	V p-p
Maximum	1.0			V p-p
Input Bias Current			1	uA
Input Full-Scale Matching		1.5		%FS
Brightness Level Adjustment		62		%FS
SWITCHING PERFORMANCE				
Maximum Conversion Rate	165			MSPS
Minimum Conversion Rate			12	MSPS
HSYNC Input Frequency	15		200	kHz
PLL Clock Rate	12		165	MHz
PLL Jitter		500		ps p-p
Sampling Phase Tempco		15		ps/°C
DYNAMIC PERFORMANCE				
Analog Bandwidth, Full Power		250		MHz
DIGITAL INPUTS				
Input Voltage, High (V_{IH})	2.5			V
Input Voltage, Low (V_{IL})			0.8	V
Input Current, High (I_{IH})			-1.0	uA
Input Current, Low (I_{IL})			1.0	uA
Input Capacitance		5		pF
DIGITAL OUTPUTS				
Output Voltage, High (V_{OH})	VDDP-0.1			V
Output Voltage, Low (V_{OL})			0.1	V
VIDEO ANALOG OUTPUT				
CVBS Buffer Output				
Output Low		1.5		V
Output High		2.0		V

Parameter	Min	Typ	Max	Unit
AUDIO				
ADC Input		2.0		V p-p
DAC Output		2.0		V p-p
SIF Input Range				
Minimum			0.1	V p-p
Maximum	1.0			V p-p
FSSW Input [Note]	0		1.8	V
SAR ADC Input	0		3.3	V

Specifications subject to change without notice.
Note: Input full scale is typically 1.8V, but input range is 0 ~ 3.3V.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
3.3V Supply Voltages	V_{VDD_33}	-0.3		3.6	V
2.5V Supply Voltages	V_{VDD_25}	-0.3		2.75	V
1.2V Supply Voltages	V_{VDD_12}	-0.3		1.32	V
Input Voltage (5V tolerant inputs)	$V_{IN5Vtol}$	-0.3		5.0	V
Input Voltage (non 5V tolerant inputs)	V_{IN}	-0.3		V_{VDD_33}	V
Ambient Operating Temperature	T_A	0		70	°C
Storage Temperature	T_{STG}	-40		150	°C
Junction Temperature	T_J			150	°C
Thermal Resistance (Junction to Air) Natural Conversion	θ_{JA}		TBD		°C/W
Thermal Resistance (Junction to Case) Natural Conversion	θ_{JC}		TBD		°C/W

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and does not imply functional operation of the device. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
MST6M16GS	0°C to +70°C	LQFP	216
MST6M16GS-LF	0°C to +70°C	LQFP	216
MST6M16GS-S1	0°C to +70°C	LQFP	216
MST6M16GS-LF-S1	0°C to +70°C	LQFP	216
MST6M16GS-S2	0°C to +70°C	LQFP	216
MST6M16GS-LF-S2	0°C to +70°C	LQFP	216
MST6M16GS-S3	0°C to +70°C	LQFP	216
MST6M16GS-LF-S3	0°C to +70°C	LQFP	216
MST6M16GS-S4	0°C to +70°C	LQFP	216
MST6M16GS-LF-S4	0°C to +70°C	LQFP	216
MST6M16GS-S5	0°C to +70°C	LQFP	216
MST6M16GS-LF-S5	0°C to +70°C	LQFP	216

Note on product suffix:
1. "LF": Lead-free version.
2. "S1" ~ "S5": Advanced surround features.

Code	Description
S1	SRS TruSurround XT™ SRS(O) TruSurround XT
S2	Dolby® ProLogic® II + Dolby® Virtual Speaker
S3	Dolby® ProLogic® II + Virtual Dolby® Surround
S4	BBE®
S5	BBE® ViVA™

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MARKING INFORMATION

MST6M16GS

- Part Number
- Lot Number
- Operation Code A
- Operation Code B
- Date Code (YYWW)
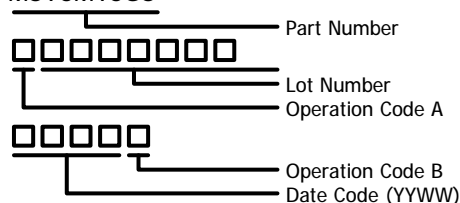
DISCLAIMER

MSTAR SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. NO RESPONSIBILITY IS ASSUMED BY MSTAR SEMICONDUCTOR ARISING OUT OF THE APPLICATION OR USER OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

Electrostatic charges accumulate on both test equipment and human body and can discharge without detection.   MST6M16GS comes with ESD protection circuitry; however, the device may be permanently damaged when subjected to high energy discharges.   The device should be handled with proper ESD precautions to prevent malfunction and performance degradation.

REVISION HISTORY

Document	Description	Date
MST6M16GS_ds_v01	• Initial release	Jun 2008
MST6M16GS_ds_v02	• Added 3-D Comb and Advanced Sound Technology related information • Updated Features / Digital Audio Interface and Analog RGB Compliant Input Ports • Updated to DDR DRAM in Features • Updated Mechanical Dimensions	Jul 2008

MECHANICAL DIMENSIONS
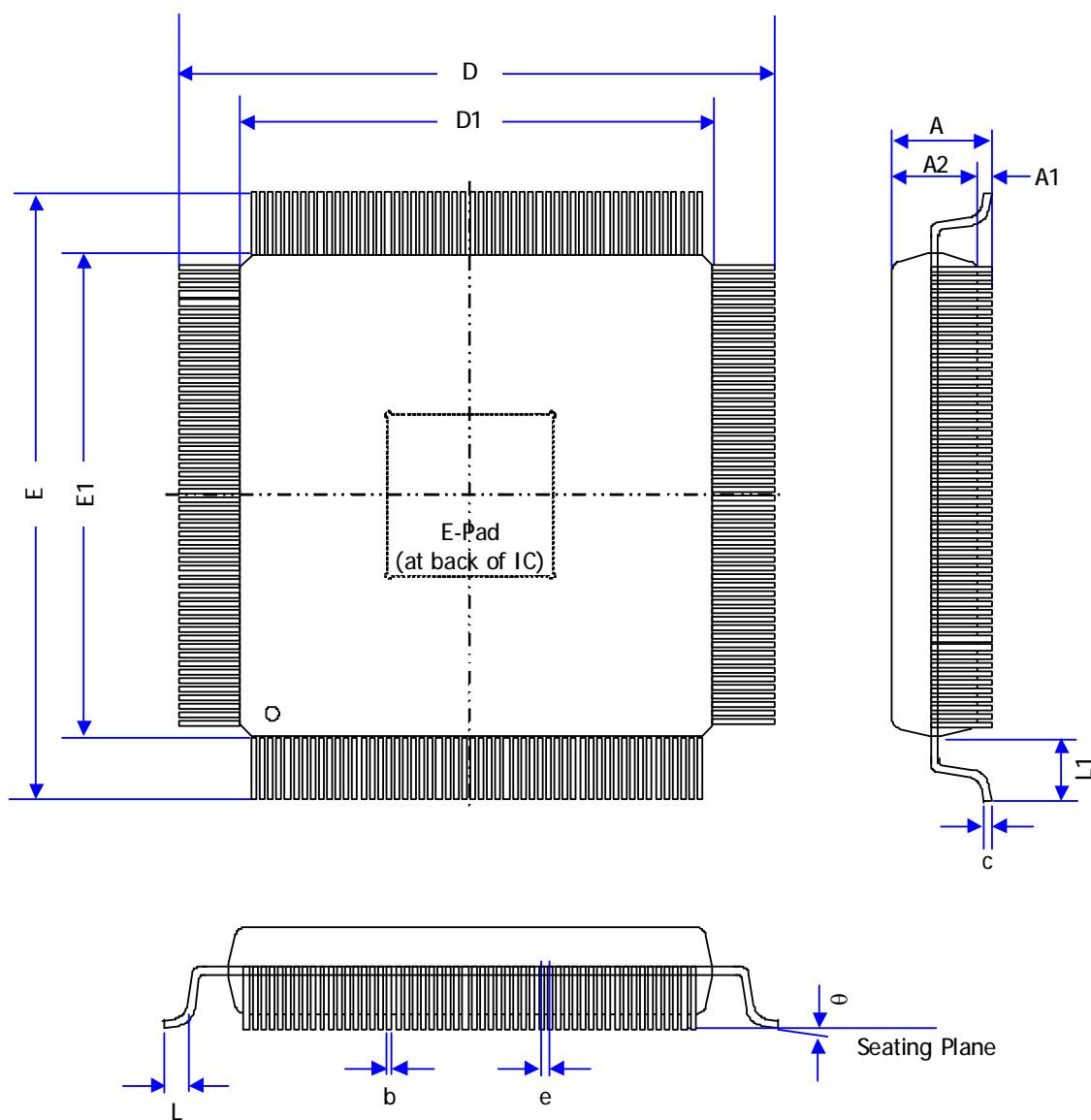
Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	1.60	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	26.00			1.024		
D1	24.00			0.945		
E	26.00			1.024		
E1	24.00			0.945		

Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
θ	0°	-	7°	0°	-	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		
b	-	0.18	-	-	0.007	-
c	-	0.14	-	-	0.006	-
e	0.40 BSC			0.016 BSC		

REGISTER DESCRIPTION

ISP Register (Bank = 08)

ISP Register (Bank = 08)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (0800h)	REG0800	7:0	Default : 0x55	Access : R/W
	ISP_PASSWORD[7:0]	7:0	ISP password 0xAAAA. If password is correct, enable ISP. If password is incorrect, disable ISP.	
00h (0801h)	REG0801	7:0	Default : 0x55	Access : R/W
	ISP_PASSWORD[15:8]	7:0	Please see description of '0800h'.	
01h (0802h)	REG0802	7:0	Default : 0x00	Access : WO
	SPI_COMMAND[7:0]	7:0	SPI command. If write data to this port, ISP will start operation.	
02h (0804h)	REG0804	7:0	Default : 0x00	Access : R/W
	ADR1[7:0]	7:0	SPI address 1, A[7:0].	
02h (0805h)	REG0805	7:0	Default : 0x00	Access : R/W
	ADR2[7:0]	7:0	SPI address 2, A[15:8].	
03h (0806h)	REG0806	7:0	Default : 0x00	Access : R/W
	ADR3[7:0]	7:0	SPI address 3, A[23:16].	
04h (0808h)	REG0808	7:0	Default : 0x00	Access : WO
	WDATA[7:0]	7:0	SPI write data register.	
05h (080Ah)	REG080A	7:0	Default : -	Access : RO
	RDATA[7:0]	7:0	SPI read data register.	
06h (080Ch)	REG080C	7:0	Default : 0x04	Access : R/W
	-	7	Reserved.	
	SPI_CLK_DIV8	6	SPI_CLOCK = MCU_CLOCK/8.	
	SPI_CLK_DIV7	5	SPI_CLOCK = MCU_CLOCK/7.	
	SPI_CLK_DIV6	4	SPI_CLOCK = MCU_CLOCK/6.	
	SPI_CLK_DIV5	3	SPI_CLOCK = MCU_CLOCK/5.	
	SPI_CLK_DIV4	2	SPI_CLOCK = MCU_CLOCK/4.	
	SPI_CLK_DIV3	1	SPI_CLOCK = MCU_CLOCK/3.	
	SPI_CLK_DIV2	0	SPI_CLOCK = MCU_CLOCK/2.	
07h (080Eh)	REG080E	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	DEVICE_SEL[2:0]	2:0	Select Device.	

ISP Register (Bank = 08)

Index (Absolute)	Mnemonic	Bit	Description	
			000: PMC. 001: Next Flash. 010: ST. 011: SST. 100: ATMEL.	
08h (0810h)	REG0810	7:0	Default : 0x00	Access : WO
	-	7:1	Reserved.	
	SPI_CE_CLR	0	Clear SPI chip select; this bit is write-then-clear register. 1: For clear. 0: For not clear.	
09h (0812h)	REG0812	7:0	Default : 0x01	Access : R/W
	TCES_TIME[7:0]	7:0	SPI chip enable setup/hold time. 0x0000: Delay 1 SPI clock. 0x0001: Delay 2 SPI clock. 0x000f: Delay 16 SPI clock. 0xffff: Delay 64k SPI clock. Default delay 2 SPI clock.	
09h (0813h)	REG0813	7:0	Default : 0x00	Access : R/W
	TCES_TIME[15:8]	7:0	Please see description of '0812h'.	
0Ah (0814h)	REG0814	7:0	Default : 0xF3	Access : R/W
	TBP_TIME[7:0]	7:0	Byte-program time for device SST. 0x0000: Delay 1 SPI clock. 0x0001: Delay 2 SPI clock. 0x000f: Delay 16 SPI clock. 0xffff: Delay 64k SPI clock. Default delaying 500 SPI clock. Assume SPI clock is 40ns; delay 500*40 = 20 us.	
0Ah (0815h)	REG0815	7:0	Default : 0x01	Access : R/W
	TBP_TIME[15:8]	7:0	Please see description of '0814h'.	
0Bh (0816h)	REG0816	7:0	Default : 0x04	Access : R/W
	TCEH_TIME[7:0]	7:0	SPI Chip enable pulse high time. 0x0000: Delay 1 SPI clock. 0x0001: Delay 2 SPI clock. 0x000f: Delay 16 SPI clock. 0xffff: Delay 64k SPI clock. Default delaying 5 SPI clock.	
0Bh	REG0817	7:0	Default : 0x00	Access : R/W

ISP Register (Bank = 08)

Index (Absolute)	Mnemonic	Bit	Description	
(0817h)	TCEH_TIME[15:8]	7:0	Please see description of '0816h'.	
0Ch (0818h)	**REG0818**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	SPI_RD_REQ	0	SPI read data request for CPU to read SPI data via RIU. If CPU reads SPI data via XIU, request not needed.	
0Dh (081Ah)	**REG081A**	**7:0**	**Default : 0x14**	**Access : R/W**
	ISP_RP_ADR1[7:0]	7:0	Programmable ISP Read port address[15:0].	
0Dh (081Bh)	**REG081B**	**7:0**	**Default : 0xC2**	**Access : R/W**
	ISP_RP_ADR1[15:8]	7:0	Please see description of '081Ah'.	
0Eh (081Ch)	**REG081C**	**7:0**	**Default : 0x81**	**Access : R/W**
	ISP_RP_ADR2[7:0]	7:0	Programmable ISP Read port address[31:0].	
0Eh (081Dh)	**REG081D**	**7:0**	**Default : 0x1F**	**Access : R/W**
	ISP_RP_ADR2[15:8]	7:0	Please see description of '081Ch'.	
0Fh (081Eh)	**REG081E**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	ENDIAN_SEL_SPI	0	0: Big endian. 1: Little endian.	
10h (0820h)	**REG0820**	**7:0**	**Default : -**	**Access : RO**
	-	7:1	Reserved.	
	ISP_ACTIVE	0	ISP active flag.	
11h (0822h)	**REG0822**	**7:0**	**Default : -**	**Access : RO**
	-	7:2	Reserved.	
	CPU_ACTIVE	1	CPU active flag.	
	-	0	Reserved.	
12h (0824h)	**REG0824**	**7:0**	**Default : -**	**Access : RO**
	-	7:3	Reserved.	
	DMA_ACTIVE	2	DMA active flag.	
	-	1:0	Reserved.	
13h (0826h)	**REG0826**	**7:0**	**Default : -**	**Access : RO**
	-	7:6	Reserved.	
	ISP_FSM[5:0]	5:0	Check ISP_FSM.	
14h (0828h)	**REG0828**	**7:0**	**Default : -**	**Access : RO**
	-	7:3	Reserved.	

ISP Register (Bank = 08)

Index (Absolute)	Mnemonic	Bit	Description	
	SPI_MASTER_FSM[2:0]	2:0	Check SPI_MASTER_FSM.	
15h (082Ah)	**REG082A**	**7:0**	**Default : -**	**Access : RO**
	-	7:1	Reserved.	
	SPI_RD_DATA_RDY	0	SPI read data ready flag. 1: Read data ready. 0: Read data not ready.	
16h (082Ch)	**REG082C**	**7:0**	**Default : -**	**Access : RO**
	-	7:1	Reserved.	
	SPI_WR_DATA_RDY	0	SPI write ready flag. 1: Write data ready. 0: Write data not ready.	
17h (082Eh)	**REG082E**	**7:0**	**Default : -**	**Access : RO**
	-	7:1	Reserved.	
	SPI_WR_CM_RDY	0	SPI write command ready flag. 1: Write command ready. 0: Write command not ready.	
18h (0830h)	**REG0830**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	CPU_RST_FM_ISP	0	ISP generate reset to CPU. When ISP programming is done, software may issue a reset to CPU.	
19h (0832h)	**REG0832**	**7:0**	**Default : -**	**Access : RO**
	-	7:1	Reserved.	
	ISP_OLD_EN	0	Read flag enable for ISP_OLD_EN.	
20h (0840h)	**REG0840**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	FORCE_ISP_IDLE	0	Force ISP to idle.	
21h (0842h)	**REG0842**	**7:0**	**Default : 0x00**	**Access : R/W**
	AAI_NUM[7:0]	7:0	For SST SPI flash use. At AAI mode, set amount of data that will be written. 0x0000: For 1 byte programming. 0x0001: For 2 byte programming. 0xFFFF: For 64k byte programming.	
21h (0843h)	**REG0843**	**7:0**	**Default : 0x00**	**Access : R/W**
	AAI_NUM[15:8]	7:0	Please see description of '0842h'.	
22h	**REG0844**	**7:0**	**Default : 0x00**	**Access : R/W**

ISP Register (Bank = 08)

Index (Absolute)	Mnemonic	Bit	Description	
(0844h)	PAGE_PRO	7	Force SPI command; force page programming.	
	FAST_READ	6	Force SPI command; force fast read.	
	READ	5	Force SPI command; force read.	
	WRCR	4	Force SPI command; force WRCR.	
	RDCR	3	Force SPI command; force RDCR.	
	WRSR	2	Force SPI command; force WRSR.	
	RDSR	1	Force SPI command; force RDSR.	
	AAI	0	Force SPI command; force AAI mode.	
22h (0845h)	**REG0845**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	MAN_ID_REG	1	Force SPI command; force read manufacturer ID.	
	B_ERASE_REG	0	Force SPI command; force black erase.	
25h (084Ah)	**REG084A**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_MD[7:0]	7:0	Test mode; user define SPI waveform. 0x7777: User defined. Others: Not user defined. Before entering TEST_MODE, please make sure ISP/DMA disable.	
25h (084Bh)	**REG084B**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_MD[15:8]	7:0	Please see description of '084Ah'.	
26h (084Ch)	**REG084C**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	TEST_SPI_CEB	0	User generate SPI chip enable waveform.	
27h (084Eh)	**REG084E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	TEST_SPI_SCK	0	User generate SPI clock waveform.	
28h (0850h)	**REG0850**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	TEST_SPI_SI	0	User generate SPI data waveform.	
29h (0852h)	**REG0852**	**7:0**	**Default : -**	**Access : RO**
	-	7:1	Reserved.	
	TEST_SPI_SO	0	SPI Data output for RIU read. Delay 1us for every setting (test mode). EX1. W(0x21,0x0) --> delay 1us --> W(0x23,0x1) -->	

ISP Register (Bank = 08)

Index (Absolute)	Mnemonic	Bit	Description	
			delay 1us --> W(0x22,0x1) --> delay 1us --> W(0x22,0x0) --> delay 1us ....--> W(ox21,0x1) EX2. W(0x21,0x0) --> delay 1us --> W(0x22,0x1) --> delay 1us --> W(0x22,0x0) --> delay 1us --> R(0x24) --> delay 1us ....> W(0x21,01).	
2Ah (0854h)	REG0854	7:0	Default : 0x00	Access : R/W
	TRIGGER_MD[7:0]	7:0	Trigger mode. 0x3333: Trigger mode. Others: Not trigger mode. Disable ISP/DMA, before entering trigger mode.	
2Ah (0855h)	REG0855	7:0	Default : 0x00	Access : R/W
	TRIGGER_MD[15:8]	7:0	Please see description of '0854h'.	

M2MCU Register (Bank = 10)

M2MCU Register (Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (1000h)	REG1000	7:0	Default : 0x00	Access : R/W
	SRAM_START_ADDR_1[7:0]	7:0	SRAM Start Address[23:16].	
00h (1001h)	REG1001	7:0	Default : 0x00	Access : R/W
	SRAM_START_ADDR_1[15:8]	7:0	Please see description of '1000h'.	
01h (1002h)	REG1002	7:0	Default : 0xFF	Access : R/W
	SRAM_END_ADDR_1[7:0]	7:0	SRAM End Address[23:16].	
01h (1003h)	REG1003	7:0	Default : 0xFF	Access : R/W
	SRAM_END_ADDR_1[15:8]	7:0	Please see description of '1002h'.	
02h (1004h)	REG1004	7:0	Default : 0x00	Access : R/W
	SRAM_START_ADDR_0[7:0]	7:0	SRAM Start Address[15:0].	
02h (1005h)	REG1005	7:0	Default : 0x00	Access : R/W
	SRAM_START_ADDR_0[15:8]	7:0	Please see description of '1004h'.	
03h (1006h)	REG1006	7:0	Default : 0xFF	Access : R/W
	SRAM_END_ADDR_0[7:0]	7:0	SRAM End Address[15:0].	
03h (1007h)	REG1007	7:0	Default : 0xFF	Access : R/W
	SRAM_END_ADDR_0[15:8]	7:0	Please see description of '1006h'.	
04h (1008h)	REG1008	7:0	Default : 0x01	Access : R/W
	DRAM_START_ADDR_1[7:0]	7:0	DRAM Start Address[23:16].	
04h (1009h)	REG1009	7:0	Default : 0x00	Access : R/W
	DRAM_START_ADDR_1[15:8]	7:0	Please see description of '1008h'.	
05h (100Ah)	REG100A	7:0	Default : 0x0F	Access : R/W
	DRAM_END_ADDR_1[7:0]	7:0	DRAM End Address[23:16].	
05h (100Bh)	REG100B	7:0	Default : 0x00	Access : R/W
	DRAM_END_ADDR_1[15:8]	7:0	Please see description of '100Ah'.	
06h (100Ch)	REG100C	7:0	Default : 0x00	Access : R/W
	DRAM_START_ADDR_0[7:0]	7:0	DRAM Start Address[15:0].	
06h (100Dh)	REG100D	7:0	Default : 0x80	Access : R/W
	DRAM_START_ADDR_0[15:8]	7:0	Please see description of '100Ch'.	
07h (100Eh)	REG100E	7:0	Default : 0xFF	Access : R/W
	DRAM_END_ADDR_0[7:0]	7:0	DRAM End Address[15:0].	
07h (100Fh)	REG100F	7:0	Default : 0xFF	Access : R/W
	DRAM_END_ADDR_0[15:8]	7:0	Please see description of '100Eh'.	

M2MCU Register (Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
08h (1010h)	REG1010	7:0	Default : 0x01	Access : R/W
	SPI_START_ADDR_1[7:0]	7:0	SPI Start Address[23:16].	
08h (1011h)	REG1011	7:0	Default : 0x00	Access : R/W
	SPI_START_ADDR_1[15:8]	7:0	Please see description of '1010h'.	
09h (1012h)	REG1012	7:0	Default : 0x0F	Access : R/W
	SPI_END_ADDR_1[7:0]	7:0	SPI End Address[23:16].	
09h (1013h)	REG1013	7:0	Default : 0x00	Access : R/W
	SPI_END_ADDR_1[15:8]	7:0	Please see description of '1012h'.	
0Ah (1014h)	REG1014	7:0	Default : 0x00	Access : R/W
	SPI_START_ADDR_0[7:0]	7:0	SPI Start Address[15:0].	
0Ah (1015h)	REG1015	7:0	Default : 0x80	Access : R/W
	SPI_START_ADDR_0[15:8]	7:0	Please see description of '1014h'.	
0Bh (1016h)	REG1016	7:0	Default : 0xFF	Access : R/W
	SPI_END_ADDR_0[7:0]	7:0	SPI End Address[15:0].	
0Bh (1017h)	REG1017	7:0	Default : 0xFF	Access : R/W
	SPI_END_ADDR_0[15:8]	7:0	Please see description of '1016h'.	
0Ch (1018h)	REG1018	7:0	Default : 0x03	Access : R/W
	MCU_BANK_USE_XFR	7	Use xfr to switch bank.	
	TEST_SEL[2:0]	6:4	Test bus selection.	
	DUMMY4	3	Reg_dummy4.	
	DUMMY3	2	Reg_dummy2.	
	DUMMY2	1	Reg_dummy2.	
	DUMMY1	0	Reg_dummy1.	
0Ch (1019h)	REG1019	7:0	Default : 0x00	Access : R/W
	MCU_BANK_XFR[7:0]	7:0	Xfr BANK(64KB).	
0Dh (101Ah)	REG101A	7:0	Default : 0x00	Access : R/W
	TWA[7:0]	7:0	Reg_twa for RIU Bridge.	
0Dh (101Bh)	REG101B	7:0	Default : 0x00	Access : R/W
	TAW[7:0]	7:0	Reg_taw for RIU Bridge.	
20h (1040h)	REG1040	7:0	Default : 0x00	Access : R/W
	P0_OV[7:0]	7:0	P0 overide by P0_REG 0: Disable. 1: Enable.	

M2MCU Register (Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
20h (1041h)	REG1041	7:0	Default : 0x00	Access : R/W
	P0_REG[7:0]	7:0	Data to overide P0.	
21h (1042h)	REG1042	7:0	Default : 0x00	Access : R/W
	P1_OV[7:0]	7:0	P1 overide by P1_REG 0: Disable. 1: Enable.	
21h (1043h)	REG1043	7:0	Default : 0x00	Access : R/W
	P1_REG[7:0]	7:0	Data to overide P1.	
22h (1044h)	REG1044	7:0	Default : 0x00	Access : R/W
	P2_OV[7:0]	7:0	P2 overide by P2_REG 0: Disable. 1: Enable.	
22h (1045h)	REG1045	7:0	Default : 0x00	Access : R/W
	P2_REG[7:0]	7:0	Data to overide P2.	
23h (1046h)	REG1046	7:0	Default : 0x00	Access : R/W
	P3_OV[7:0]	7:0	P3 overide by P3_REG 0: Disable. 1: Enable.	
23h (1047h)	REG1047	7:0	Default : 0x00	Access : R/W
	P3_REG[7:0]	7:0	Data to overide P3.	
24h (1048h)	REG1048	7:0	Default : 0x00	Access : R/W
	P0_CTRL[7:0]	7:0	MCU Port 0 output enable control.	
25h (104Ah)	REG104A	7:0	Default : 0x00	Access : R/W
	P0_OE[7:0]	7:0	MCU Port 0 output enable.	
26h (104Ch)	REG104C	7:0	Default : 0x00	Access : R/W
	P0_IN[7:0]	7:0	MCU Port 0 output enable from output data.	
27h (104Eh)	REG104E	7:0	Default : 0x00	Access : R/W
	P1_CTRL[7:0]	7:0	MCU Port 1 output enable control.	
27h (104Fh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
28h (1050h)	REG1050	7:0	Default : 0x00	Access : R/W
	P1_OE[7:0]	7:0	MCU Port 1 output enable.	
29h (1052h)	REG1052	7:0	Default : 0x00	Access : R/W
	P1_IN[7:0]	7:0	MCU Port 1 output enable from output data.	

M2MCU Register (Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
2Ah (1054h)	REG1054	7:0	Default : 0x00	Access : R/W
	P2_CTRL[7:0]	7:0	MCU Port 2 output enable control.	
2Bh (1056h)	REG1056	7:0	Default : 0x00	Access : R/W
	P2_OE[7:0]	7:0	MCU Port 2 output enable.	
2Ch (1058h)	REG1058	7:0	Default : 0x00	Access : R/W
	P2_IN[7:0]	7:0	MCU Port 2 output enable from output data.	
2Dh (105Ah)	REG105A	7:0	Default : 0x00	Access : R/W
	P3_CTRL[7:0]	7:0	MCU Port 3 output enable control.	
2Eh (105Ch)	REG105C	7:0	Default : 0x00	Access : R/W
	P3_OE[7:0]	7:0	MCU Port 3 output enable.	
2Fh (105Eh)	REG105E	7:0	Default : 0x00	Access : R/W
	P3_IN[7:0]	7:0	MCU Port 3 output enable from output data.	
40h (1080h)	REG1080	7:0	Default : 0x55	Access : R/W
	RESET_CPU0[7:0]	7:0	Reset CPU0.	
40h (1081h)	REG1081	7:0	Default : 0xAA	Access : R/W
	RESET_CPU0[15:8]	7:0	Please see description of '1080h'.	
41h (1082h)	REG1082	7:0	Default : 0x55	Access : R/W
	RESET_CPU1[7:0]	7:0	Reset CPU1.	
41h (1083h)	REG1083	7:0	Default : 0xAA	Access : R/W
	RESET_CPU1[15:8]	7:0	Please see description of '1082h'.	
42h (1084h)	REG1084	7:0	Default : 0x00	Access : R/W
	SW_RESET_CPU0[7:0]	7:0	SW reset CPU0(8051).	
42h (1085h)	REG1085	7:0	Default : 0x00	Access : R/W
	SW_RESET_CPU0[15:8]	7:0	Please see description of '1084h'.	
43h (1086h)	REG1086	7:0	Default : 0x00	Access : R/W
	SW_RESET_CPU1[7:0]	7:0	SW reset CPU1(aeon).	
43h (1087h)	REG1087	7:0	Default : 0x00	Access : R/W
	SW_RESET_CPU1[15:8]	7:0	Please see description of '1086h'.	
44h ~ 4Fh (1088h ~ 109Fh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
50h (10A0h)	REG10A0	7:0	Default : 0x00	Access : R/W
	AND[7:0]	7:0		

M2MCU Register (Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
50h (10A1h)	REG10A1	7:0	Default : 0x00	Access : R/W
	OR[7:0]	7:0		
51h (10A2h)	REG10A2	7:0	Default : 0x00	Access : R/W
	TRIG_IB_A[7:0]	7:0		
51h (10A3h)	REG10A3	7:0	Default : 0x00	Access : R/W
	TRIG_IB_A[15:8]	7:0	Please see description of '10A2h'.	
52h (10A4h)	REG10A4	7:0	Default : 0x00	Access : R/W
	TRIG_IB_A[23:16]	7:0	Please see description of '10A2h'.	
53h (10A6h)	REG10A6	7:0	Default : 0x00	Access : R/W
	TRIG_XB_A[7:0]	7:0		
53h (10A7h)	REG10A7	7:0	Default : 0x00	Access : R/W
	TRIG_XB_A[15:8]	7:0	Please see description of '10A6h'.	
54h (10A8h)	REG10A8	7:0	Default : 0x00	Access : R/W
	TRIG_XB_A[23:16]	7:0	Please see description of '10A6h'.	
55h (10AAh)	REG10AA	7:0	Default : 0x00	Access : R/W
	TRIG_XB_D[7:0]	7:0		
55h (10ABh)	REG10AB	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	EN_XB_RD	4		
	EN_XB_WR	3		
	EN_XB_D	2		
	EN_XB_A	1		
	EN_IB_A	0		
58h (10B0h)	REG10B0	7:0	Default : 0x00	Access : RO
	IB_ADDR0[7:0]	7:0		
58h (10B1h)	REG10B1	7:0	Default : 0x00	Access : RO
	IB_ADDR0[15:8]	7:0	Please see description of '10B0h'.	
59h (10B2h)	REG10B2	7:0	Default : 0x00	Access : RO
	IB_ADDR0[23:16]	7:0	Please see description of '10B0h'.	
59h (10B3h)	REG10B3	7:0	Default : 0x00	Access : RO
	IB_DATAI0[7:0]	7:0		
5Ah (10B4h)	REG10B4	7:0	Default : 0x00	Access : RO
	IB_ADDR1[7:0]	7:0		

M2MCU Register (Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
5Ah (10B5h)	REG10B5	7:0	Default : 0x00	Access : RO
	IB_ADDR1[15:8]	7:0	Please see description of '10B4h'.	
5Bh (10B6h)	REG10B6	7:0	Default : 0x00	Access : RO
	IB_ADDR1[23:16]	7:0	Please see description of '10B4h'.	
5Bh (10B7h)	REG10B7	7:0	Default : 0x00	Access : RO
	IB_DATAI1[7:0]	7:0		
5Ch (10B8h)	REG10B8	7:0	Default : 0x00	Access : RO
	IB_ADDR2[7:0]	7:0		
5Ch (10B9h)	REG10B9	7:0	Default : 0x00	Access : RO
	IB_ADDR2[15:8]	7:0	Please see description of '10B8h'.	
5Dh (10BAh)	REG10BA	7:0	Default : 0x00	Access : RO
	IB_ADDR2[23:16]	7:0	Please see description of '10B8h'.	
5Dh (10BBh)	REG10BB	7:0	Default : 0x00	Access : RO
	IB_DATAI2[7:0]	7:0		

MCU Register (Bank = 10)

MCU Register (Bank = 10)			
Index (Absolute)	Mnemonic	Bit	Description
00h (1000h)	REG1000	7:0	Default : 0x01 — Access : R/W
	SRAM_START_ADDR_1[7:0]	7:0	SRAM start address[23:16].
00h (1001h)	REG1001	7:0	Default : 0x00 — Access : R/W
	SRAM_START_ADDR_1[15:8]	7:0	Please see description of '1000h'.
01h (1002h)	REG1002	7:0	Default : 0x01 — Access : R/W
	SRAM_END_ADDR_1[7:0]	7:0	SRAM end address[23:16].
01h (1003h)	REG1003	7:0	Default : 0x00 — Access : R/W
	SRAM_END_ADDR_1[15:8]	7:0	Please see description of '1002h'.
02h (1004h)	REG1004	7:0	Default : 0x00 — Access : R/W
	SRAM_START_ADDR_0[7:0]	7:0	SRAM end address[15:0].
02h (1005h)	REG1005	7:0	Default : 0x00 — Access : R/W
	SRAM_START_ADDR_0[15:8]	7:0	Please see description of '1004h'.
03h (1006h)	REG1006	7:0	Default : 0x00 — Access : R/W
	SRAM_END_ADDR_0[7:0]	7:0	SRAM end address[15:0].
03h (1007h)	REG1007	7:0	Default : 0x80 — Access : R/W
	SRAM_END_ADDR_0[15:8]	7:0	Please see description of '1006h'.
04h (1008h)	REG1008	7:0	Default : 0x01 — Access : R/W
	DRAM_START_ADDR_1[7:0]	7:0	DRAM start address[23:16].
04h (1009h)	REG1009	7:0	Default : 0x00 — Access : R/W
	DRAM_START_ADDR_1[15:8]	7:0	Please see description of '1008h'.
05h (100Ah)	REG100A	7:0	Default : 0x0F — Access : R/W
	DRAM_END_ADDR_1[7:0]	7:0	DRAM end address[23:16].
05h (100Bh)	REG100B	7:0	Default : 0x00 — Access : R/W
	DRAM_END_ADDR_1[15:8]	7:0	Please see description of '100Ah'.
06h (100Ch)	REG100C	7:0	Default : 0x00 — Access : R/W
	DRAM_START_ADDR_0[7:0]	7:0	DRAM start address[15:0].
06h (100Dh)	REG100D	7:0	Default : 0x80 — Access : R/W
	DRAM_START_ADDR_0[15:8]	7:0	Please see description of '100Ch'.
07h (100Eh)	REG100E	7:0	Default : 0xFF — Access : R/W
	DRAM_END_ADDR_0[7:0]	7:0	DRAM end address[15:0].
07h	REG100F	7:0	Default : 0xFF

MCU Register (Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
(100Fh)	DRAM_END_ADDR_0[15:8]	7:0	Please see description of '100Eh'.	
08h (1010h)	**REG1010**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_START_ADDR_1[7:0]	7:0	SPI start address[23:16].	
08h (1011h)	**REG1011**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_START_ADDR_1[15:8]	7:0	Please see description of '1010h'.	
09h (1012h)	**REG1012**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_END_ADDR_1[7:0]	7:0	SPI end address[23:16].	
09h (1013h)	**REG1013**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_END_ADDR_1[15:8]	7:0	Please see description of '1012h'.	
0Ah (1014h)	**REG1014**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_START_ADDR_0[7:0]	7:0	SPI start address[15:0].	
0Ah (1015h)	**REG1015**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_START_ADDR_0[15:8]	7:0	Please see description of '1014h'.	
0Bh (1016h)	**REG1016**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SPI_END_ADDR_0[7:0]	7:0	SPI end address[15:0].	
0Bh (1017h)	**REG1017**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SPI_END_ADDR_0[15:8]	7:0	Please see description of '1016h'.	
0Ch (1018h)	**REG1018**	**7:0**	**Default : 0x02**	**Access : R/W**
	MCU_BANK_USE_XFR	7	Use XFR to switch bank.	
	TEST_SEL[2:0]	6:4	Test bus selection.	
	ICACHE_RSTZ	3	ICACHE enable. 0: Disable. 1: Enable.	
	DRAM_EN	2	DRAM enable. 0: Disable. 1: Enable.	
	SPI_EN	1	SPI enable. 0: Disable. 1: Enable.	
	SRAM_EN	0	SRAM enable. 0: Disable. 1: Enable.	
0Ch (1019h)	**REG1019**	**7:0**	**Default : 0x00**	**Access : R/W**
	MCU_BANK_XFR[7:0]	7:0	XFR bank (64KB).	

MCU Register (Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
0Dh (101Ah)	REG101A	7:0	Default : 0x00	Access : R/W
	TWA[7:0]	7:0	REG_TWA for RIU bridge.	
0Dh (101Bh)	REG101B	7:0	Default : 0x00	Access : R/W
	TAW[7:0]	7:0	REG_TAW for RIU bridge.	
0Eh ~ 1Fh (101Ch ~ 103Fh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
20h (1040h)	REG1040	7:0	Default : 0x00	Access : R/W
	P0_OV[7:0]	7:0	P0 override by P0_REG 0: Disable. 1: Enable.	
20h (1041h)	REG1041	7:0	Default : 0x00	Access : R/W
	P0_REG[7:0]	7:0	Data to override P0.	
21h (1042h)	REG1042	7:0	Default : 0x00	Access : R/W
	P1_OV[7:0]	7:0	P1 override by P1_REG 0: Disable. 1: Enable.	
21h (1043h)	REG1043	7:0	Default : 0x00	Access : R/W
	P1_REG[7:0]	7:0	Data to override P1.	
22h (1044h)	REG1044	7:0	Default : 0x00	Access : R/W
	P2_OV[7:0]	7:0	P2 override by P2_REG 0: Disable. 1: Enable.	
22h (1045h)	REG1045	7:0	Default : 0x00	Access : R/W
	P2_REG[7:0]	7:0	Data to override P2.	
23h (1046h)	REG1046	7:0	Default : 0x00	Access : R/W
	P3_OV[7:0]	7:0	P3 override by P3_REG 0: Disable. 1: Enable.	
23h (1047h)	REG1047	7:0	Default : 0x00	Access : R/W
	P3_REG[7:0]	7:0	Data to override P3.	
24h (1048h)	REG1048	7:0	Default : 0x00	Access : R/W
	P0_CTRL[7:0]	7:0	MCU Port 0 output control.	
25h (104Ah)	REG104A	7:0	Default : 0x00	Access : R/W
	P0_OE[7:0]	7:0	MCU Port 0 output enable.	

MCU Register (Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
26h (104Ch)	REG104C	7:0	Default : 0x00	Access : R/W
	P0_IN[7:0]	7:0	MCU Port 0 output enable from output data.	
27h (104Eh)	REG104E	7:0	Default : 0x00	Access : R/W
	P1_CTRL[7:0]	7:0	MCU Port 1 output Enable Control.	
28h (1050h)	REG1050	7:0	Default : 0x00	Access : R/W
	P1_OE[7:0]	7:0	MCU Port 1 output enable.	
29h (1052h)	REG1052	7:0	Default : 0x00	Access : R/W
	P1_IN[7:0]	7:0	MCU Port 1 output enable from output data.	
2Ah (1054h)	REG1054	7:0	Default : 0x00	Access : R/W
	P2_CTRL[7:0]	7:0	MCU Port 2 output control.	
2Bh (1056h)	REG1056	7:0	Default : 0x00	Access : R/W
	P2_OE[7:0]	7:0	MCU Port 2 output enable.	
2Ch (1058h)	REG1058	7:0	Default : 0x00	Access : R/W
	P2_IN[7:0]	7:0	MCU Port 2 output enable from output data.	
2Dh (105Ah)	REG105A	7:0	Default : 0x00	Access : R/W
	P3_CTRL[7:0]	7:0	MCU Port 3 output control.	
2Eh (105Ch)	REG105C	7:0	Default : 0x00	Access : R/W
	P3_OE[7:0]	7:0	MCU Port 3 output enable.	
2Fh (105Eh)	REG105E	7:0	Default : 0x00	Access : R/W
	P3_IN[7:0]	7:0	MCU Port 3 output enable from output data.	
2Fh (105Eh)	REG105E	7:0	Default : 0x00	Access : R/W
	P3_IN[7:0]	7:0	MCU Port 3 output enable from output data.	
30h ~ 3Fh (105Fh ~ 107Fh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
40h (1080h)	REG1080	7:0	Default : 0x55	Access : R/W
	RESET_CPU0[7:0]	7:0	Reset CPU0.	
40h (1081h)	REG1081	7:0	Default : 0xAA	Access : R/W
	RESET_CPU0[15:8]	7:0	Please see description of '1080h'.	
41h (1082h)	REG1082	7:0	Default : 0x55	Access : R/W
	RESET_CPU1[7:0]	7:0	Reset CPU1.	
41h (1083h)	REG1083	7:0	Default : 0xAA	Access : R/W
	RESET_CPU1[15:8]	7:0	Please see description of '1082h'.	

MCU Register (Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
42h (1084h)	REG1084	7:0	Default : 0x00	Access : R/W
	SW_RESET_CPU0[7:0]	7:0	SW reset CPU0 (8051).	
42h (1085h)	REG1085	7:0	Default : 0x00	Access : R/W
	SW_RESET_CPU0[15:8]	7:0	Please see description of '1084h'.	
43h (1086h)	REG1086	7:0	Default : 0x00	Access : R/W
	SW_RESET_CPU1[7:0]	7:0	SW reset CPU1 (aeon).	
43h (1087h)	REG1087	7:0	Default : 0x00	Access : R/W
	SW_RESET_CPU1[15:8]	7:0	Please see description of '1086h'.	
44h ~ 51h (1088h ~ 10A2h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
51h (10A3h)	REG10A3	7:0	Default : 0x00	Access : R/W
	TRIG_IB_A[15:8]	7:0	Please see description of '10A2h'.	
52h (10A4h)	REG10A4	7:0	Default : 0x00	Access : R/W
	TRIG_IB_A[23:16]	7:0	Please see description of '10A2h'.	
53h (10A6h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
53h (10A7h)	REG10A7	7:0	Default : 0x00	Access : R/W
	TRIG_XB_A[15:8]	7:0	Please see description of '10A6h'.	
54h (10A8h)	REG10A8	7:0	Default : 0x00	Access : R/W
	TRIG_XB_A[23:16]	7:0	Please see description of '10A6h'.	
55h ~ 58h (10AAh ~ 10B0h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
58h (10B1h)	REG10B1	7:0	Default : -	Access : RO
	IB_ADDR0[15:8]	7:0	Please see description of '10B0h'.	
59h (10B2h)	REG10B2	7:0	Default : -	Access : RO
	IB_ADDR0[23:16]	7:0	Please see description of '10B0h'.	
59h ~ 5Ah (10B3h ~ 10B4h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
5Ah (10B5h)	REG10B5	7:0	Default : -	Access : RO
	IB_ADDR1[15:8]	7:0	Please see description of '10B4h'.	
5Bh	REG10B6	7:0	Default : -	Access : RO

MCU Register (Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
(10B6h)	IB_ADDR1[23:16]	7:0	Please see description of '10B4h'.	
5Bh ~ 5Ch (10B7h ~ 10B8h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
5Ch (10B9h)	REG10B9	7:0	Default : -	Access : RO
	IB_ADDR2[15:8]	7:0	Please see description of '10B8h'.	
5Dh (10BAh)	REG10BA	7:0	Default : -	Access : RO
	IB_ADDR2[23:16]	7:0	Please see description of '10B8h'.	
5Dh ~ 5Fh (10BBh ~ 10BFh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
60h (10C0h)	REG10C0	7:0	Default : 0x00	Access : RO, R/W
	BUFFER_MUX	7	Use 512 bytes as menu-load buffer.	
	MENULOAD_DONE	6	Menu-load done, and will be cleared when menu-load is enabled.	
	MENULOAD_BUSY	5	Menu-load busy, and will be cleared when menu-load is done.	
	-	4:3	Reserved.	
	MENULOAD_EN_DUMMY	2	Menu-load enables shot.	
	MENULOAD_CTRL_MD[1:0]	1:0	Menu-load triggering SRC select.	
61h (10C2h)	REG10C2	7:0	Default : 0x00	Access : R/W
	MENULOAD_NUMBER[7:0]	7:0	Menu-load numbers.	
62h (10C4h)	REG10C4	7:0	Default : -	Access : RO
	-	7:1	Reserved.	
	MENULOAD_ABORTED_ONCE	0	Menu-load was aborted once.	
63h (10C6h)	REG10C6	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	SYNC_TRIG2_SEL	2	Select negated sync.	
	SYNC_TRIG1_SEL	1	Select negated sync.	
	SYNC_TRIG0_SEL	0	Select negated sync.	
64h (10C8h)	REG10C8	7:0	Default : 0x00	Access : WO
	-	7:1	Reserved.	
	MENULOAD_REALTIME_TRIG	0	Menu-load real-time triggering one shot.	

MCU Register (Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
65h (10CAh)	REG10CA	7:0	Default : 0x00	Access : WO
	-	7:1	Reserved.	
	MENULOAD_ABORT	0	Menu-load aborts one shot.	
66h (10CCh)	REG10CC	7:0	Default : 0x00	Access : WO
	-	7:1	Reserved.	
	MENULOAD_EN	0	Menu-load enables one shot.	
67h ~ 6Fh (10CDh ~ 10DFh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
70h (10E0h)	REG10E0	7:0	Default : 0x00	Access : R/W
	XB_ERAM_LB[7:0]	7:0	ERAM map HK XDATA low boundary (unit: 1k), suggested: 0x14.	
70h (10E1h)	REG10E1	7:0	Default : 0x00	Access : R/W
	XB_ERAM_HB[7:0]	7:0	ERAM map HK XDATA high boundary (unit: 1k), suggested: 0x14.	
72h (10E4h)	REG10E4	7:0	Default : 0x00	Access : R/W
	XD2ERAM_ADRH[7:0]	7:0	ERAM base address (unit: 1k, 0x000-0x3FF).	
73h (10E6h)	REG10E6	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	XD2ERAM_EN	0	Enable ERAM mapping.	

MIU1 Register (Bank = 11)

MIU1 Register (Bank = 11)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (1100h)	REG1100	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	ARBITER_SKIP_OFF	2	Turn off skip empty request function.	
	ARBITER_OFF	1	Turn off arbiter.	
	INIT_MIU	0	Issue initial MIU cycle.	
00h (1101h)	REG1101	7:0	Default : 0x00	Access : RO, R/W
	INIT_DONE	7	Initial done flag.	
	-	6:5	Reserved.	
	TRIG_LMR_EXT	4	Issue one load mode register extend cycle.	
	TRIG_LMR	3	Issue one load mode register cycle.	
	TRIG_REFRESH	2	Issue one refresh cycle.	
	TRIG_PRECHARGE	1	Issue one pre-charge cycle.	
	SINGLE_STEP_ON	0	Turn single step on.	
01h (1102h)	REG1102	7:0	Default : 0x00	Access : R/W
	DDR_DQ	7	For pad select.	
	DDR	6	DDR/SDR select.	
	DRAM_BUS[1:0]	5:4	DRAM bus width, 0:16b, 1:32b, 2:64b.	
	-	3	Reserved.	
	DYNAMIC_CKE	2	Turn on CKE.	
	SELF_REFRESH	1	Enter self refresh cycle.	
	CKE	0	Turn on CKE.	
01h (1103h)	REG1103	7:0	Default : 0x70	Access : R/W
	CS_Z	7	Chip select, low active.	
	ADR_OENZ	6	Address output enable, low active.	
	DQ_OENZ	5	Data output enable, low active.	
	CKE_OENZ	4	CKE output enable, low active.	
	-	3:2	Reserved.	
	9COL	1	0: 8 columns. 1: 9 columns.	
	4BA	0	0: 2 banks. 1: 4 banks.	
02h	REG1104	7:0	Default : 0x40	Access : R/W

MIU1 Register (Bank = 11)

Index (Absolute)	Mnemonic	Bit	Description	
(1104h)	RD_TIMING[3:0]	7:4	Read data cycle.	
	-	3:2	Reserved.	
	RD_MCK_SEL	1	Read data CLK select. 0: Feedback. 1: Internal.	
	RD_IN_PHASE	0	Read data phase. 0: Normal. 1: Inverse.	
02h (1105h)	REG1105	7:0	Default : 0x03	Access : R/W
	-	7	Reserved.	
	RESET_DLL	6	Reset DLL.	
	DRIVE_STRENGTH	5	DRAM drive strength.	
	DISABLE_DLL	4	Disable DRAM DLL.	
	-	3	Reserved.	
	CAS_LATENCY[2:0]	2:0	CAS latency. SDR: 2/3. DDR: 2/6.	
03h (1106h)	REG1106	7:0	Default : 0x00	Access : R/W
	TREFPERIOD[7:0]	7:0	Refresh cycle, unit 16T.	
03h (1107h)	REG1107	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	PRIORITY_SW	6	Switch the priority of group0 and group1.	
	-	5:4	Reserved.	
	SIZE_MASK[3:0]	3:0	Mask high address > DRAM support.	
04h (1108h)	REG1108	7:0	Default : 0xC8	Access : R/W
	TRC[3:0]	7:4	DRAM TRC setting.	
	TRAS[3:0]	3:0	DRAM TRAS setting.	
04h (1109h)	REG1109	7:0	Default : 0x33	Access : R/W
	TRP[3:0]	7:4	DRAM TRP setting.	
	TRCD[3:0]	3:0	DRAM TRCD setting.	
05h (110Ah)	REG110A	7:0	Default : 0x62	Access : R/W
	TWR[3:0]	7:4	DRAM TWR timing.	
	TRRD[3:0]	3:0	DRAM TRRD timing.	
05h	REG110B	7:0	Default : 0x02	Access : R/W

MIU1 Register (Bank = 11)

Index (Absolute)	Mnemonic	Bit	Description	
(110Bh)	-	7:4	Reserved.	
	TMRD[3:0]	3:0	DRAM TMRD timing.	
06h (110Ch)	**REG110C**	**7:0**	**Default : 0x63**	**Access : R/W**
	W2R_OEN_DLY[3:0]	7:4	write to read output enable delay cycle reg_w2r_dly + 3	
	W2R_DLY[3:0]	3:0	Write to read command delay cycle.	
06h (110Dh)	**REG110D**	**7:0**	**Default : 0x86**	**Access : R/W**
	R2W_OEN_DLY[3:0]	7:4	read to write output enable delay cycle R2W_DLY + 2	
	R2W_DLY[3:0]	3:0	Read to write command delay cycle.	
07h (110Eh)	**REG110E**	**7:0**	**Default : 0x0E**	**Access : R/W**
	BA_REORDER[2:0]	7:5	Reorder bank address.	
	TRFC[4:0]	4:0	DRAM TRFC timing.	
08h (1110h)	**REG1110**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEB_SEL[7:0]	7:0	Debug control.	
08h (1111h)	**REG1111**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEB_SEL[15:8]	7:0	Please see description of '1110h'.	
09h (1112h)	**REG1112**	**7:0**	**Default : -**	**Access : RO**
	DEB_BUS[7:0]	7:0	Debug port.	
09h (1113h)	**REG1113**	**7:0**	**Default : -**	**Access : RO**
	DEB_BUS[15:8]	7:0	Please see description of '1112h'.	
0Ah (1114h)	**REG1114**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_SEL0[7:0]	7:0	MIU select for group0 client. 0: External. 1: MCP.	
0Ah (1115h)	**REG1115**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_SEL0[15:8]	7:0	Please see description of '1114h'.	
0Bh (1116h)	**REG1116**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_SEL1[7:0]	7:0	MIU select for group1 client. 0: External. 1: MCP.	
0Bh (1117h)	**REG1117**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_SEL1[15:8]	7:0	Please see description of '1116h'.	
0Ch (1118h)	**REG1118**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_SEL2[7:0]	7:0	MIU select for group2 client.	

Index (Absolute)	Mnemonic	Bit	Description	
			0: External. 1: MCP.	
0Ch (1119h)	**REG1119**	**7:0**	Default : 0x00	Access : R/W
	MIU_SEL2[15:8]	7:0	Please see description of '1118h'.	
0Dh (111Ah)	**REG111A**	**7:0**	Default : 0x00	Access : R/W
	MIU_SEL3[7:0]	7:0	MIU select for group3 client. 0: External. 1: MCP.	
0Dh (111Bh)	**REG111B**	**7:0**	Default : 0x00	Access : R/W
	MIU_SEL3[15:8]	7:0	Please see description of '111Ah'.	
0Eh (111Ch)	**REG111C**	**7:0**	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	MIU_SEL_PROTECT_SW	2	MIU select register write protect by firmware.	
	MIU_SEL_PROTECT_HW	1	MIU select register write protect by hardware.	
	MIU_SEL_PROTECT_EN	0	MIU select register write protect enable.	
0Fh (111Eh)	**REG111E**	**7:0**	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	DFT_ADRMD	1	For DFT coverage.	
	SW_RST_MIU	0	MIU software reset.	
0Fh (111Fh)	**REG111F**	**7:0**	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	MCP_DEB_SEL	4	MCP debug bus selection.	
	-	3	Reserved.	
	MCLK_INV	2	MCP output clock source phase selection.	
	MCLK_DLY_CTRL[1:0]	1:0	MCP output clock source delay selection.	
20h (1140h)	**REG1140**	**7:0**	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	RQ0_GROUP_DEADLINE_EN	5	Group0 deadline enable.	
	RQ0_TIMEOUT_EN	4	Group0 timeout enable.	
	RQ0_GROUP_LIMIT_EN	3	Limit group0 request number enable.	
	RQ0_MEMBER_LIMIT_EN	2	Limit group0 client request number enable.	
	RQ0_SET_PRIORITY	1	Set group0 fix priority.	
	RQ0_ROUND_ROBIN	0	Turn on group0 round robin.	

MIU1 Register (Bank = 11)

Index (Absolute)	Mnemonic	Bit	Description	
20h (1141h)	REG1141	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	RQ0_client6_CTRL_EN	5	Group 0 Client6 flow control enable.	
	RQ0_client5_CTRL_EN	4	Group 0 Client5 flow control enable.	
	RQ0_client4_CTRL_EN	3	Group 0 Client4 flow control enable.	
	RQ0_client3_CTRL_EN	2	Group 0 Client3 flow control enable.	
	RQ0_client2_CTRL_EN	1	Group 0 Client2 flow control enable.	
	RQ0_client1_CTRL_EN	0	Group 0 Client1 flow control enable.	
21h (1142h)	REG1142	7:0	Default : 0x00	Access : R/W
	RQ0_MEMBER_MAX[7:0]	7:0	Limit group0 client request number, unit 4.	
21h (1143h)	REG1143	7:0	Default : 0x00	Access : R/W
	RQ0_GROUP_MAX[7:0]	7:0	Limit group0 client request number, unit 32.	
22h (1144h)	REG1144	7:0	Default : 0x00	Access : R/W
	RQ0_TIMEOUT[7:0]	7:0	Limit group0 timeout number.	
22h (1145h)	REG1145	7:0	Default : 0x00	Access : R/W
	RQ0_TIMEOUT[15:8]	7:0	Please see description of '1144h'.	
23h (1146h)	REG1146	7:0	Default : 0x00	Access : R/W
	RQ0_MASK[7:0]	7:0	Limit group0 request mask.	
23h (1147h)	REG1147	7:0	Default : 0x00	Access : R/W
	RQ0_MASK[15:8]	7:0	Please see description of '1146h'.	
24h (1148h)	REG1148	7:0	Default : 0x00	Access : R/W
	RQ0_HPMASK[7:0]	7:0	Limit group0 high priority request mask.	
24h (1149h)	REG1149	7:0	Default : 0x00	Access : R/W
	RQ0_HPMASK[15:8]	7:0	Please see description of '1148h'.	
25h (114Ah)	REG114A	7:0	Default : 0x10	Access : R/W
	RQ01_PRIORITY[3:0]	7:4	Limit group0 client 1 fix priority number.	
	RQ00_PRIORITY[3:0]	3:0	Limit group0 client 0 fix priority number.	
25h (114Bh)	REG114B	7:0	Default : 0x32	Access : R/W
	RQ03_PRIORITY[3:0]	7:4	Limit group0 client 3 fix priority number.	
	RQ02_PRIORITY[3:0]	3:0	Limit group0 client 2 fix priority number.	
26h (114Ch)	REG114C	7:0	Default : 0x54	Access : R/W
	RQ05_PRIORITY[3:0]	7:4	Limit group0 client 5 fix priority number.	
	RQ04_PRIORITY[3:0]	3:0	Limit group0 client 4 fix priority number.	

MIU1 Register (Bank = 11)

Index (Absolute)	Mnemonic	Bit	Description	
26h (114Dh)	REG114D	7:0	Default : 0x76	Access : R/W
	RQ07_PRIORITY[3:0]	7:4	Limit group0 client 7 fix priority number.	
	RQ06_PRIORITY[3:0]	3:0	Limit group0 client 6 fix priority number.	
27h (114Eh)	REG114E	7:0	Default : 0x98	Access : R/W
	RQ09_PRIORITY[3:0]	7:4	Limit group0 client 9 fix priority number.	
	RQ08_PRIORITY[3:0]	3:0	Limit group0 client 8 fix priority number.	
27h (114Fh)	REG114F	7:0	Default : 0xBA	Access : R/W
	RQ0B_PRIORITY[3:0]	7:4	Limit group0 client b fix priority number.	
	RQ0A_PRIORITY[3:0]	3:0	Limit group0 client a fix priority number.	
28h (1150h)	REG1150	7:0	Default : 0xDC	Access : R/W
	RQ0D_PRIORITY[3:0]	7:4	Limit group0 client d fix priority number.	
	RQ0C_PRIORITY[3:0]	3:0	Limit group0 client c fix priority number.	
28h (1151h)	REG1151	7:0	Default : 0xFE	Access : R/W
	RQ0F_PRIORITY[3:0]	7:4	Limit group0 client f fix priority number.	
	RQ0E_PRIORITY[3:0]	3:0	Limit group0 client e fix priority number.	
29h (1153h)	REG1153	7:0	Default : 0x00	Access : R/W
	RQ0_GROUP_DEADLINE[7:0]	7:0	Group0 deadline, unit 64.	
2Ah (1154h)	REG1154	7:0	Default : 0x00	Access : R/W
	RQ0_CLIENT1_PERIOD[7:0]	7:0	Group0 client1 request flow control counter.	
2Ah (1155h)	REG1155	7:0	Default : 0x00	Access : R/W
	RQ0_CLIENT2_PERIOD[7:0]	7:0	Group0 client2 request flow control counter.	
2Bh (1156h)	REG1156	7:0	Default : 0x00	Access : R/W
	RQ0_CLIENT3_PERIOD[7:0]	7:0	Group0 client3 request flow control counter.	
2Bh (1157h)	REG1157	7:0	Default : 0x00	Access : R/W
	RQ0_CLIENT4_PERIOD[7:0]	7:0	Group0 client4 request flow control counter.	
2Ch (1158h)	REG1158	7:0	Default : 0x00	Access : R/W
	RQ0_CLIENT5_PERIOD[7:0]	7:0	Group0 client5 request flow control counter.	
2Ch (1159h)	REG1159	7:0	Default : 0x00	Access : R/W
	RQ0_CLIENT6_PERIOD[7:0]	7:0	Group0 client6 request flow control counter.	
60h (11C0h)	REG11C0	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	PROTECT0_EN	0	Protect 0 enable.	
60h	REG11C1	7:0	Default : 0x00	Access : R/W

MIU1 Register (Bank = 11)

Index (Absolute)	Mnemonic	Bit	Description	
(11C1h)	-	7:6	Reserved.	
	PROTECT0_ID[5:0]	5:0	Protect 0 id.	
61h (11C2h)	REG11C2	7:0	Default : 0x00	Access : R/W
	PROTECT0_START[7:0]	7:0	Protect 0 start address.	
61h (11C3h)	REG11C3	7:0	Default : 0x00	Access : R/W
	PROTECT0_START[15:8]	7:0	Please see description of '11C2h'.	
62h (11C4h)	REG11C4	7:0	Default : 0x00	Access : R/W
	PROTECT0_END[7:0]	7:0	Protect 0 end address.	
62h (11C5h)	REG11C5	7:0	Default : 0x00	Access : R/W
	PROTECT0_END[15:8]	7:0	Please see description of '11C4h'.	
63h (11C6h)	REG11C6	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	PROTECT1_EN	0	Protect 1 enable.	
63h (11C7h)	REG11C7	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	PROTECT1_ID[5:0]	5:0	Protect 1 id.	
64h (11C8h)	REG11C8	7:0	Default : 0x00	Access : R/W
	PROTECT1_START[7:0]	7:0	Protect 1 start address.	
64h (11C9h)	REG11C9	7:0	Default : 0x00	Access : R/W
	PROTECT1_START[15:8]	7:0	Please see description of '11C8h'.	
65h (11CAh)	REG11CA	7:0	Default : 0x00	Access : R/W
	PROTECT1_END[7:0]	7:0	Protect 1 end address.	
65h (11CBh)	REG11CB	7:0	Default : 0x00	Access : R/W
	PROTECT1_END[15:8]	7:0	Please see description of '11CAh'.	
66h (11CCh)	REG11CC	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	PROTECT2_EN	0	Protect 2 enable.	
66h (11CDh)	REG11CD	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	PROTECT2_ID[5:0]	5:0	Protect 2 ID.	
67h (11CEh)	REG11CE	7:0	Default : 0x00	Access : R/W
	PROTECT2_START[7:0]	7:0	Protect 2 start address.	
67h	REG11CF	7:0	Default : 0x00	Access : R/W

MIU1 Register (Bank = 11)

Index (Absolute)	Mnemonic	Bit	Description	
(11CFh)	PROTECT2_START[15:8]	7:0	Please see description of '11CEh'.	
68h (11D0h)	REG11D0	7:0	Default : 0x00	Access : R/W
	PROTECT2_END[7:0]	7:0	Protect 2 end address.	
68h (11D1h)	REG11D1	7:0	Default : 0x00	Access : R/W
	PROTECT2_END[15:8]	7:0	Please see description of '11D0h'.	
69h (11D2h)	REG11D2	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	PROTECT3_EN	0	Protect 3 enable.	
69h (11D3h)	REG11D3	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	PROTECT3_ID[5:0]	5:0	Protect 3 ID.	
6Ah (11D4h)	REG11D4	7:0	Default : 0x00	Access : R/W
	PROTECT3_START[7:0]	7:0	Protect 3 start address.	
6Ah (11D5h)	REG11D5	7:0	Default : 0x00	Access : R/W
	PROTECT3_START[15:8]	7:0	Please see description of '11D4h'.	
6Bh (11D6h)	REG11D6	7:0	Default : 0x00	Access : R/W
	PROTECT3_END[7:0]	7:0	Protect 3 end address.	
6Bh (11D7h)	REG11D7	7:0	Default : 0x00	Access : R/W
	PROTECT3_END[15:8]	7:0	Please see description of '11D6h'.	
70h (11E0h)	REG11E0	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	RDPTG_EN	3	Functional test: read pattern generator enable.	
	WDCRC_STOP	2	Functional test: CRC test stop.	
	WDCRC_START	1	Functional test: CRC test start.	
	WDCRC_RST	0	Functional test: software reset.	
71h (11E2h)	REG11E2	7:0	Default : 0x00	Access : R/W
	PTN_MODE[7:0]	7:0	Pattern generator mode.	
71h (11E3h)	REG11E3	7:0	Default : 0x00	Access : R/W
	PTN_MODE[15:8]	7:0	Please see description of '11E2h'.	
72h (11E4h)	REG11E4	7:0	Default : 0x00	Access : R/W
	PTN_DATA0[7:0]	7:0	Pattern generator data0.	
72h (11E5h)	REG11E5	7:0	Default : 0x00	Access : R/W
	PTN_DATA0[15:8]	7:0	Please see description of '11E4h'.	

MIU1 Register (Bank = 11)

Index (Absolute)	Mnemonic	Bit	Description	
73h (11E6h)	REG11E6	7:0	Default : 0x00	Access : R/W
	PTN_DATA1[7:0]	7:0	Pattern generator data1.	
73h (11E7h)	REG11E7	7:0	Default : 0x00	Access : R/W
	PTN_DATA1[15:8]	7:0	Please see description of '11E6h'.	
74h (11E8h)	REG11E8	7:0	Default : 0x00	Access : R/W
	PTN_DATA2[7:0]	7:0	Pattern generator data2.	
74h (11E9h)	REG11E9	7:0	Default : 0x00	Access : R/W
	PTN_DATA2[15:8]	7:0	Please see description of '11E8h'.	
75h (11EAh)	REG11EA	7:0	Default : 0x00	Access : R/W
	PTN_DATA3[7:0]	7:0	Pattern generator data3.	
75h (11EBh)	REG11EB	7:0	Default : 0x00	Access : R/W
	PTN_DATA3[15:8]	7:0	Please see description of '11EAh'.	
76h (11ECh)	REG11EC	7:0	Default : -	Access : RO
	ADDR_CRC[7:0]	7:0	CRC result.	
76h (11EDh)	REG11ED	7:0	Default : -	Access : RO
	ADDR_CRC[15:8]	7:0	Please see description of '11ECh'.	
77h (11EEh)	REG11EE	7:0	Default : -	Access : RO
	DATA0_CRC[7:0]	7:0	Word0 CRC.	
77h (11EFh)	REG11EF	7:0	Default : -	Access : RO
	DATA0_CRC[15:8]	7:0	Please see description of '11EEh'.	
78h (11F0h)	REG11F0	7:0	Default : -	Access : RO
	DATA1_CRC[7:0]	7:0	Word1 CRC.	
78h (11F1h)	REG11F1	7:0	Default : -	Access : RO
	DATA1_CRC[15:8]	7:0	Please see description of '11F0h'.	
79h (11F2h)	REG11F2	7:0	Default : -	Access : RO
	DATA2_CRC[7:0]	7:0	Word2 CRC.	
79h (11F3h)	REG11F3	7:0	Default : -	Access : RO
	DATA2_CRC[15:8]	7:0	Please see description of '11F2h'.	
7Ah (11F4h)	REG11F4	7:0	Default : -	Access : RO
	DATA3_CRC[7:0]	7:0	Word3 CRC.	
7Ah (11F5h)	REG11F5	7:0	Default : -	Access : RO
	DATA3_CRC[15:8]	7:0	Please see description of '11F4h'.	
70h ~ 7Ah	-	7:0	Default : -	Access : -

MIU1 Register (Bank = 11)

Index (Absolute)	Mnemonic	Bit	Description
(11E0h ~ 11F5h)	-	7:0	Reserved.

MIU Register (Bank = 12)

MIU Register (Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (1200h)	REG1200	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	ARBITER_SKIP_OFF	2	Turn off skip empty request function.	
	ARBITER_OFF	1	Turn off arbiter.	
	INIT_MIU	0	Issue initial MIU cycle.	
00h (1201h)	REG1201	7:0	Default : 0x00	Access : RO, R/W
	INIT_DONE	7	Initial done flag.	
	-	6:5	Reserved.	
	TRIG_LMR_EXT	4	Issue one load mode register extend cycle.	
	TRIG_LMR	3	Issue one load mode register cycle.	
	TRIG_REFRESH	2	Issue one refresh cycle.	
	TRIG_PRECHARGE	1	Issue one pre-charge cycle.	
	SINGLE_STEP_ON	0	Turn single step on.	
01h (1202h)	REG1202	7:0	Default : 0x00	Access : R/W
	DDR_DQ	7	For pad select.	
	DDR	6	DDR/SDR select.	
	DRAM_BUS[1:0]	5:4	DRAM bus width. 00:16b. 01: 32b. 10: 64b. 11: Reserved.	
	-	3	Reserved.	
	DYNAMIC_CKE	2	Turn on CKE.	
	SELF_REFRESH	1	Enter self refresh cycle.	
	CKE	0	Turn on CKE.	
01h (1203h)	REG1203	7:0	Default : 0x70	Access : R/W
	CS_Z	7	Chip select, low active.	
	ADR_OENZ	6	Address output enable, low active.	
	DQ_OENZ	5	Data output enable, low active.	
	CKE_OENZ	4	CKE output enable, low active.	
	-	3:2	Reserved.	
	9COL	1	0: 8 columns.	

MIU Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
			1:9 columns.	
	4BA	0	0: 2 banks. 1: 4 banks.	
02h (1204h)	REG1204	7:0	Default : 0x40	Access : R/W
	RD_TIMING[3:0]	7:4	Read data cycle.	
	-	3:2	Reserved.	
	RD_MCK_SEL	1	Read data CLK select. 0: Feedback. 1: Internal.	
	RD_IN_PHASE	0	Read data phase. 0: Normal. 1: Inverse.	
02h (1205h)	REG1205	7:0	Default : 0x03	Access : R/W
	FORCE_DDR_RD_ACT	7	Force DDR_RD_ACT.	
	RESET_DLL	6	Reset DLL.	
	DRIVE_STRENGTH	5	DRAM drive strength.	
	DISABLE_DLL	4	Disable DRAM DLL.	
	-	3	Reserved.	
	CAS_LATENCY[2:0]	2:0	CAS latency. SDR: 2/3. DDR: 2/6.	
03h (1206h)	REG1206	7:0	Default : 0x00	Access : R/W
	TREFPERIOD[7:0]	7:0	Refresh cycle, unit 16T.	
03h (1207h)	REG1207	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	PRIORITY_SW	6	Switch the priority of group0 and group1.	
	-	5:4	Reserved.	
	SIZE_MASK[3:0]	3:0	Mask high address > DRAM support.	
04h (1208h)	REG1208	7:0	Default : 0xC8	Access : R/W
	TRC[3:0]	7:4	DRAM TRC setting.	
	TRAS[3:0]	3:0	DRAM TRAS setting.	
04h (1209h)	REG1209	7:0	Default : 0x33	Access : R/W
	TRP[3:0]	7:4	DRAM TRP setting.	
	TRCD[3:0]	3:0	DRAM TRCD setting.	

MIU Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
05h (120Ah)	REG120A	7:0	Default : 0x62	Access : R/W
	TWR[3:0]	7:4	DRAM TWR timing.	
	TRRD[3:0]	3:0	DRAM TRRD timing.	
05h (120Bh)	REG120B	7:0	Default : 0x02	Access : R/W
	-	7:4	Reserved.	
	TMRD[3:0]	3:0	DRAM TMRD timing.	
06h (120Ch)	REG120C	7:0	Default : 0x63	Access : R/W
	W2R_OEN_DLY[3:0]	7:4	write to read output enable delay cycle W2R_DLY + 3	
	W2R_DLY[3:0]	3:0	Write to read command delay cycle.	
06h (120Dh)	REG120D	7:0	Default : 0x86	Access : R/W
	R2W_OEN_DLY[3:0]	7:4	read to write output enable delay cycle R2W_DLY + 2	
	R2W_DLY[3:0]	3:0	Read to write command delay cycle.	
07h (120Eh)	REG120E	7:0	Default : 0x0E	Access : R/W
	BA_REORDER[2:0]	7:5	Reorder bank address.	
	TRFC[4:0]	4:0	DRAM TRFC timing.	
08h (1210h)	REG1210	7:0	Default : 0x00	Access : R/W
	DEB_SEL[7:0]	7:0	Debug control.	
08h (1211h)	REG1211	7:0	Default : 0x00	Access : R/W
	DEB_SEL[15:8]	7:0	Please see description of '1210h'.	
09h (1212h)	REG1212	7:0	Default : -	Access : RO
	DEB_BUS[7:0]	7:0	Debug port.	
09h (1213h)	REG1213	7:0	Default : -	Access : RO
	DEB_BUS[15:8]	7:0	Please see description of '1212h'.	
0Fh (121Eh)	REG121E	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	DFT_ADRMD	1	For DFT coverage.	
	SW_RST_MIU	0	MIU software reset.	
10h (1220h)	REG1220	7:0	Default : 0x09	Access : R/W
	DDFSET[3:0]	7:4	DDR_FREQ (DDR clock frequency) = (MPLL_FREQ*128*LOOP_DIV1*LOOP_DIV2)/ (DDFSET*IN_DIV1*IN_DIV2) DDR Frequency Set. DDFSET[9:0] must be located	

MIU Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
			between 290 and 832(Dec)	
	DDRIP[1:0]	3:2	DDR Clock generator charge pump current. 00: 0.25uA. 01: 0.50uA. 10: 1.5uA. (default). 11: 3.0uA.	
	DDRRP[1:0]	1:0	Reserved for DDR PLL test.	
10h (1221h)	**REG1221**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	DDFSET[9:4]	5:0	Please see description of '1220h'.	
11h (1222h)	**REG1222**	**7:0**	**Default : 0x00**	**Access : R/W**
	DDFSPAN[7:0]	7:0	DDR clock Spread spectrum Period. DDR_SPREAD (DDR spread period) = (4* LOOP_DIV1*LOOP_DIV2*DDFSPAN)/ (DDR_FREQ*IN_DIV1*IN_DIV2).	
11h (1223h)	**REG1223**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ENFRUNZ	4	VCO free-run disable.	
	DDFT[1:0]	3:2	DDR clock generator test mode. 00: Normal operation (default). 01: Synthesizer truncate to integer divide. 10: Synthesizer bypass (equivalent to divide =1). 11: Reserved.	
	DDFSPAN[9:8]	1:0	Please see description of '1222h'.	
12h (1224h)	**REG1224**	**7:0**	**Default : 0x00**	**Access : R/W**
	DDFSTEP[7:0]	7:0	DDR clock spread spectrum step. DDR_SWB (DDR spread bandwidth) = DDR_FREQ* (2*DDFSPAN*DDFSTEP) / (DDFSET*1024).	
12h (1225h)	**REG1225**	**7:0**	**Default : 0x40**	**Access : R/W**
	DDRPLL_LOOP_DIV_1ST[1:0]	7:6	Loop divider1 ratio control 00: Divide by 1. 01: Divide by 2 (default). 10: Divide by 4. 11: Divide by 8.	
	DDRPLL_IN_DIV_1ST[1:0]	5:4	Input divider1 ratio control	

MIU Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
			00: Divide by 1 (default). 01: Divide by 2. 10: Divide by 4. 11: Divide by 8.	
	DDRPLL_RESET	3	DDR PLL reset.	
	DDRPLL_PORST	2	DDR PLL power on reset.	
	DDRPLL_PD	1	DDR PLL power down.	
	DDR_SSC_EN	0	DDR PLL spread spectrum control enable.	
13h (1226h)	REG1226	7:0	Default : 0x00	Access : R/W
	DDRPLL_INPUT_DIV_2ND[7:0]	7:0	Input divider2 ratio (1/N), default: 0 0: N=1. Other: N=IN_DIV[7:0]	
13h (1227h)	REG1227	7:0	Default : 0x00	Access : R/W
	DDRPLL_LOOP_DIV_2ND[7:0]	7:0	Loop divider2 ratio (1/N), default: 0 0: N=1. Other: N=IN_DIV[7:0]	
14H (1228h)	REG1228	7:0	DEFAULT : 0X00	ACCESS : R/W
	DDRAT[7:0]	7:0	DDR CLOCK GENERATOR ANALOG TEST MODES AND RESERVED BITS.	
14H (1229h)	REG1229	7:0	DEFAULT : 0X00	ACCESS : R/W
	DDRAT[15:8]	7:0	PLEASE SEE DESCRIPTION OF '1228H'.	
18h (1230h)	REG1230	7:0	Default : 0x00	Access : R/W
	DQSPH1[3:0]	7:4	DDR DQS1 input phase control; 0.5T/16 steps.	
	DQSPH0[3:0]	3:0	DDR DQS0 input phase control; 0.5T/16 steps.	
19h (1232h)	REG1232	7:0	Default : 0x00	Access : R/W
	DQSPH1_2ND[3:0]	7:4	DDR DQS1_2nd input phase control; 0.5T/16 steps.	
	DQSPH0_2ND[3:0]	3:0	DDR DQS0_2nd input phase control; 0.5T/16 steps.	
1Ah (1234h)	REG1234	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	DQS_IN_SEL[2:0]	6:4	Reserved for internal testing. [0]: DQS_IN_OLD_MODE. [1]: DQS_IN_I_SEL for test mode. [2]: Reserved.	
	-	3:2	Reserved.	
	DQSSEL	1	Reserved for internal testing.	

MIU Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
	DQS_DELAY_MODE	0	Reserved for internal testing.	
1Ah (1235h)	**REG1235**	**7:0**	**Default : 0x00**	**Access : R/W**
	DQS_OEN_MASK[7:0]	7:0	DQS output enable mask.	
1Bh (1236h)	**REG1236**	**7:0**	**Default : 0x60**	**Access : R/W**
	CLK_DRV[2:0]	7:5	DDR CLK IO driving control.	
	DDR_CLK_SWITCH[1:0]	4:3	Source clock select. 00: DDR_CLK. 01: DDR_CLK_INV. 10: DDR_CLK_DLY. 11: DDR_CLK_DLY_INV.	
	CLKPH[2:0]	2:0	DDR output Clock Phase control. 1T/8 steps.	
1Bh (1237h)	**REG1237**	**7:0**	**Default : 0x00**	**Access : R/W**
	MD_DRV[1:0]	7:6	DDR data IO driving control.	
	ADR_DRV[1:0]	5:4	DDR command and address IO driving control.	
	DM_DRV[1:0]	3:2	DDR data mask IO driving control.	
	DQS_DRV[1:0]	1:0	DDR DQS IO driving control.	
1Ch (1238h)	**REG1238**	**7:0**	**Default : 0x00**	**Access : R/W**
	FB_CLK_SEL	7	SDR read data clock select. 0: FBCLK. 1: PLL 2nd PH.	
	CLKPH1[2:0]	6:4	PLL 2nd output clock phase control; 1T/8 steps.	
	-	3:2	Reserved.	
	FORCE_D2A_FIFO_EN	1	Force D2A_FIFO_EN value.	
	FORCE_CKE_IN	0	Force CKE value.	
1Ch (1239h)	**REG1239**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	LADR_DRV[5:0]	5:0	ADDR[2:0] PAD driving strength.	
1Dh (123Ah)	**REG123A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DDR266[4:0]	4:0	TR[2:0], LEG[1:0].	
1Dh (123Bh)	**REG123B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	DDR_LEG2[6:0]	6:0	LEG2 for each byte.	
1Fh	**REG123E**	**7:0**	**DEFAULT : 0X00**	**ACCESS : R/W**

MIU Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
(123Eh)	-	7:3	Reserved.	
	DS_RESTEN	2	Reserved for internal testing; DQS test mode enable.	
	DDR_TEST_CLK_SEL[1:0]	1:0	Reserved for internal testing.	
1Fh (123Fh)	REG123F	7:0	DEFAULT : -	ACCESS : RO
	DDRPLL_LOCK	7	DDR PLL lock status.	
	DDRPLL_SSC_OFF	6	Reserved for internal testing.	
	HIGH_FLAG	5	Reserved for internal testing.	
	-	4:0	Reserved.	
20h (1240h)	REG1240	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	RQ0_GROUP_DEADLINE_EN	5	Group0 deadline enable.	
	RQ0_TIMEOUT_EN	4	Group0 timeout enable.	
	RQ0_GROUP_LIMIT_EN	3	Limit group0 request number enable.	
	RQ0_MEMBER_LIMIT_EN	2	Limit group0 client request number enable.	
	RQ0_SET_PRIORITY	1	Set group0 fix priority.	
	RQ0_ROUND_ROBIN	0	Turn on group0 round robin.	
20h (1241h)	REG1241	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	RQ0_CLIENT6_CTRL_EN	5	Group 0 Client6 flow control enable.	
	RQ0_CLIENT5_CTRL_EN	4	Group 0 Client5 flow control enable.	
	RQ0_CLIENT4_CTRL_EN	3	Group 0 Client4 flow control enable.	
	RQ0_CLIENT3_CTRL_EN	2	Group 0 Client3 flow control enable.	
	RQ0_CLIENT2_CTRL_EN	1	Group 0 Client2 flow control enable.	
	RQ0_CLIENT1_CTRL_EN	0	Group 0 Client1 flow control enable.	
21h (1242h)	REG1242	7:0	Default : 0x00	Access : R/W
	RQ0_MEMBER_MAX[7:0]	7:0	Limit group0 client request number, unit 4.	
21h (1243h)	REG1243	7:0	Default : 0x00	Access : R/W
	RQ0_GROUP_MAX[7:0]	7:0	Limit group0 client request number, unit 32.	
22h (1244h)	REG1244	7:0	Default : 0x00	Access : R/W
	RQ0_TIMEOUT[7:0]	7:0	Limit group0 timeout number.	
22h (1245h)	REG1245	7:0	Default : 0x00	Access : R/W
	RQ0_TIMEOUT[15:8]	7:0	Please see description of '1244h'.	
23h	REG1246	7:0	Default : 0x00	Access : R/W

MIU Register (Bank = 12)				
Index (Absolute)	Mnemonic	Bit	Description	
(1246h)	RQ0_MASK[7:0]	7:0	Limit group0 request mask.	
23h (1247h)	**REG1247**	7:0	Default : 0x00	Access : R/W
	RQ0_MASK[15:8]	7:0	Please see description of '1246h'.	
24h (1248h)	**REG1248**	7:0	Default : 0x00	Access : R/W
	RQ0_HPMASK[7:0]	7:0	Limit group0 high priority request mask.	
24h (1249h)	**REG1249**	7:0	Default : 0x00	Access : R/W
	RQ0_HPMASK[15:8]	7:0	Please see description of '1248h'.	
25h (124Ah)	**REG124A**	7:0	Default : 0x10	Access : R/W
	RQ01_PRIORITY[3:0]	7:4	Limit group0 client 1 fix priority number.	
	RQ00_PRIORITY[3:0]	3:0	Limit group0 client 0 fix priority number.	
25h (124Bh)	**REG124B**	7:0	Default : 0x32	Access : R/W
	RQ03_PRIORITY[3:0]	7:4	Limit group0 client 3 fix priority number.	
	RQ02_PRIORITY[3:0]	3:0	Limit group0 client 2 fix priority number.	
26h (124Ch)	**REG124C**	7:0	Default : 0x54	Access : R/W
	RQ05_PRIORITY[3:0]	7:4	Limit group0 client 5 fix priority number.	
	RQ04_PRIORITY[3:0]	3:0	Limit group0 client 4 fix priority number.	
26h (124Dh)	**REG124D**	7:0	Default : 0x76	Access : R/W
	RQ07_PRIORITY[3:0]	7:4	Limit group0 client 7 fix priority number.	
	RQ06_PRIORITY[3:0]	3:0	Limit group0 client 6 fix priority number.	
27h (124Eh)	**REG124E**	7:0	Default : 0x98	Access : R/W
	RQ09_PRIORITY[3:0]	7:4	Limit group0 client 9 fix priority number.	
	RQ08_PRIORITY[3:0]	3:0	Limit group0 client 8 fix priority number.	
27h (124Fh)	**REG124F**	7:0	Default : 0xBA	Access : R/W
	RQ0B_PRIORITY[3:0]	7:4	Limit group0 client b fix priority number.	
	RQ0A_PRIORITY[3:0]	3:0	Limit group0 client a fix priority number.	
28h (1250h)	**REG1250**	7:0	Default : 0xDC	Access : R/W
	RQ0D_PRIORITY[3:0]	7:4	Limit group0 client d fix priority number.	
	RQ0C_PRIORITY[3:0]	3:0	Limit group0 client c fix priority number.	
28h (1251h)	**REG1251**	7:0	Default : 0xFE	Access : R/W
	RQ0F_PRIORITY[3:0]	7:4	Limit group0 client f fix priority number.	
	RQ0E_PRIORITY[3:0]	3:0	Limit group0 client e fix priority number.	
29h (1253h)	**REG1253**	7:0	Default : 0x00	Access : R/W
	RQ0_GROUP_DEADLINE[7:0]	7:0	Group0 deadline, unit 64.	

MIU Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
2Ah (1254h)	REG1254	7:0	Default : 0x00	Access : R/W
	RQ0_CLIENT1_PERIOD[7:0]	7:0	Group0 client1 request flow control counter.	
2Ah (1255h)	REG1255	7:0	Default : 0x00	Access : R/W
	RQ0_CLIENT2_PERIOD[7:0]	7:0	Group0 client2 request flow control counter.	
2Bh (1256h)	REG1256	7:0	Default : 0x00	Access : R/W
	RQ0_CLIENT3_PERIOD[7:0]	7:0	Group0 client3 request flow control counter.	
2Bh (1257h)	REG1257	7:0	Default : 0x00	Access : R/W
	RQ0_CLIENT4_PERIOD[7:0]	7:0	Group0 client4 request flow control counter.	
2Ch (1258h)	REG1258	7:0	Default : 0x00	Access : R/W
	RQ0_CLIENT5_PERIOD[7:0]	7:0	Group0 client5 request flow control counter.	
2Ch (1259h)	REG1259	7:0	Default : 0x00	Access : R/W
	RQ0_CLIENT6_PERIOD[7:0]	7:0	Group0 client6 request flow control counter.	
30h (1260h)	REG1260	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	RQ1_GROUP_DEADLINE_EN	5	Group1 deadline enable.	
	RQ1_TIMEOUT_EN	4	Group1 timeout enable.	
	RQ1_GROUP_LIMIT_EN	3	Limit group1 request number enable.	
	RQ1_MEMBER_LIMIT_EN	2	Limit group1 client request number enable.	
	RQ1_SET_PRIORITY	1	Set group1 fix priority.	
	RQ1_ROUND_ROBIN	0	Turn on group1 round robin.	
31h (1262h)	REG1262	7:0	Default : 0x00	Access : R/W
	RQ1_MEMBER_MAX[7:0]	7:0	Limit group1 client request number, unit 4.	
31h (1263h)	REG1263	7:0	Default : 0x00	Access : R/W
	RQ1_GROUP_MAX[7:0]	7:0	Limit group1 client request number, unit 32.	
32h (1264h)	REG1264	7:0	Default : 0x00	Access : R/W
	RQ1_TIMEOUT[7:0]	7:0	Limit group1 timeout number.	
32h (1265h)	REG1265	7:0	Default : 0x00	Access : R/W
	RQ1_TIMEOUT[15:8]	7:0	Please see description of '1264h'.	
33h (1266h)	REG1266	7:0	Default : 0x00	Access : R/W
	RQ1_MASK[7:0]	7:0	Limit group1 request mask.	
33h (1267h)	REG1267	7:0	Default : 0x00	Access : R/W
	RQ1_MASK[15:8]	7:0	Please see description of '1266h'.	
34h	REG1268	7:0	Default : 0x00	Access : R/W

MIU Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
(1268h)	RQ1_HPMASK[7:0]	7:0	Limit group1 high priority request mask.	
34h (1269h)	**REG1269**	7:0	**Default : 0x00**	**Access : R/W**
	RQ1_HPMASK[15:8]	7:0	Please see description of '1268h'.	
35h (126Ah)	**REG126A**	7:0	**Default : 0x10**	**Access : R/W**
	RQ11_PRIORITY[3:0]	7:4	Limit group1 client 1 fix priority number.	
	RQ10_PRIORITY[3:0]	3:0	Limit group1 client 0 fix priority number.	
35h (126Bh)	**REG126B**	7:0	**Default : 0x32**	**Access : R/W**
	RQ13_PRIORITY[3:0]	7:4	Limit group1 client 3 fix priority number.	
	RQ12_PRIORITY[3:0]	3:0	Limit group1 client 2 fix priority number.	
36h (126Ch)	**REG126C**	7:0	**Default : 0x54**	**Access : R/W**
	RQ15_PRIORITY[3:0]	7:4	Limit group1 client 5 fix priority number.	
	RQ14_PRIORITY[3:0]	3:0	Limit group1 client 4 fix priority number.	
36h (126Dh)	**REG126D**	7:0	**Default : 0x76**	**Access : R/W**
	RQ17_PRIORITY[3:0]	7:4	Limit group1 client 7 fix priority number.	
	RQ16_PRIORITY[3:0]	3:0	Limit group1 client 6 fix priority number.	
37h (126Eh)	**REG126E**	7:0	**Default : 0x98**	**Access : R/W**
	RQ19_PRIORITY[3:0]	7:4	Limit group1 client 9 fix priority number.	
	RQ18_PRIORITY[3:0]	3:0	Limit group1 client 8 fix priority number.	
37h (126Fh)	**REG126F**	7:0	**Default : 0xBA**	**Access : R/W**
	RQ1B_PRIORITY[3:0]	7:4	Limit group1 client b fix priority number.	
	RQ1A_PRIORITY[3:0]	3:0	Limit group1 client a fix priority number.	
38h (1270h)	**REG1270**	7:0	**Default : 0xDC**	**Access : R/W**
	RQ1D_PRIORITY[3:0]	7:4	Limit group1 client d fix priority number.	
	RQ1C_PRIORITY[3:0]	3:0	Limit group1 client c fix priority number.	
38h (1271h)	**REG1271**	7:0	**Default : 0xFE**	**Access : R/W**
	RQ1F_PRIORITY[3:0]	7:4	Limit group1 client f fix priority number.	
	RQ1E_PRIORITY[3:0]	3:0	Limit group1 client e fix priority number.	
39h (1273h)	**REG1273**	7:0	**Default : 0x00**	**Access : R/W**
	RQ1_GROUP_DEADLINE[7:0]	7:0	Group1 deadline, unit 64.	
40h (1280h)	**REG1280**	7:0	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	RQ2_GROUP_DEADLINE_EN	5	Group2 deadline enable.	
	RQ2_TIMEOUT_EN	4	Group2 timeout enable.	

MIU Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
	RQ2_GROUP_LIMIT_EN	3	Limit group2 request number enable.	
	RQ2_MEMBER_LIMIT_EN	2	Limit group2 client request number enable.	
	RQ2_SET_PRIORITY	1	Set group2 fix priority.	
	RQ2_ROUND_ROBIN	0	Turn on group2 round robin.	
41h (1283h)	**REG1283**	7:0	**Default : 0x00**	Access : R/W
	RQ2_GROUP_MAX[7:0]	7:0	Limit group2 client request number, unit 32.	
42h (1284h)	**REG1284**	7:0	**Default : 0x00**	Access : R/W
	RQ2_TIMEOUT[7:0]	7:0	Limit group2 timeout number.	
42h (1285h)	**REG1285**	7:0	**Default : 0x00**	Access : R/W
	RQ2_TIMEOUT[15:8]	7:0	Please see description of '1284h'.	
43h (1286h)	**REG1286**	7:0	**Default : 0x00**	Access : R/W
	RQ2_MASK[7:0]	7:0	Limit group2 request mask.	
43h (1287h)	**REG1287**	7:0	**Default : 0x00**	Access : R/W
	RQ2_MASK[15:8]	7:0	Please see description of '1286h'.	
44h (1288h)	**REG1288**	7:0	**Default : 0x00**	Access : R/W
	RQ2_HPMASK[7:0]	7:0	Limit group2 high priority request mask.	
44h (1289h)	**REG1289**	7:0	**Default : 0x00**	Access : R/W
	RQ2_HPMASK[15:8]	7:0	Please see description of '1288h'.	
45h (128Ah)	**REG128A**	7:0	**Default : 0x10**	Access : R/W
	RQ21_PRIORITY[3:0]	7:4	Limit group2 client 1 fix priority number.	
	RQ20_PRIORITY[3:0]	3:0	Limit group2 client 0 fix priority number.	
45h (128Bh)	**REG128B**	7:0	**Default : 0x32**	Access : R/W
	RQ23_PRIORITY[3:0]	7:4	Limit group2 client 3 fix priority number.	
	RQ22_PRIORITY[3:0]	3:0	Limit group2 client 2 fix priority number.	
46h (128Ch)	**REG128C**	7:0	**Default : 0x54**	Access : R/W
	RQ25_PRIORITY[3:0]	7:4	Limit group2 client 5 fix priority number.	
	RQ24_PRIORITY[3:0]	3:0	Limit group2 client 4 fix priority number.	
46h (128Dh)	**REG128D**	7:0	**Default : 0x76**	Access : R/W
	RQ27_PRIORITY[3:0]	7:4	Limit group2 client 7 fix priority number.	
	RQ26_PRIORITY[3:0]	3:0	Limit group2 client 6 fix priority number.	
47h (128Eh)	**REG128E**	7:0	**Default : 0x98**	Access : R/W
	RQ29_PRIORITY[3:0]	7:4	Limit group2 client 9 fix priority number.	
	RQ28_PRIORITY[3:0]	3:0	Limit group2 client 8 fix priority number.	

MIU Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
47h (128Fh)	REG128F	7:0	Default : 0xBA	Access : R/W
	RQ2B_PRIORITY[3:0]	7:4	Limit group2 client b fix priority number.	
	RQ2A_PRIORITY[3:0]	3:0	Limit group2 client a fix priority number.	
48h (1290h)	REG1290	7:0	Default : 0xDC	Access : R/W
	RQ2D_PRIORITY[3:0]	7:4	Limit group2 client d fix priority number.	
	RQ2C_PRIORITY[3:0]	3:0	Limit group2 client c fix priority number.	
48h (1291h)	REG1291	7:0	Default : 0xFE	Access : R/W
	RQ2F_PRIORITY[3:0]	7:4	Limit group2 client f fix priority number.	
	RQ2E_PRIORITY[3:0]	3:0	Limit group2 client e fix priority number.	
49h (1293h)	REG1293	7:0	Default : 0x00	Access : R/W
	RQ2_GROUP_DEADLINE[7:0]	7:0	Group2 deadline, unit 64.	
60h (12C0h)	REG12C0	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	PROTECT0_EN	0	Protect 0 enable.	
60h (12C1h)	REG12C1	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	PROTECT0_ID[5:0]	5:0	Protect 0 ID.	
61h (12C2h)	REG12C2	7:0	Default : 0x00	Access : R/W
	PROTECT0_START[7:0]	7:0	Protect 0 start address.	
61h (12C3h)	REG12C3	7:0	Default : 0x00	Access : R/W
	PROTECT0_START[15:8]	7:0	Please see description of '12C2h'.	
62h (12C4h)	REG12C4	7:0	Default : 0x00	Access : R/W
	PROTECT0_END[7:0]	7:0	Protect 0 end address.	
62h (12C5h)	REG12C5	7:0	Default : 0x00	Access : R/W
	PROTECT0_END[15:8]	7:0	Please see description of '12C4h'.	
63h (12C6h)	REG12C6	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	PROTECT1_EN	0	Protect 1 enable.	
63h (12C7h)	REG12C7	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	PROTECT1_ID[5:0]	5:0	Protect 1 ID.	
64h (12C8h)	REG12C8	7:0	Default : 0x00	Access : R/W
	PROTECT1_START[7:0]	7:0	Protect 1 start address.	

MIU Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
64h (12C9h)	REG12C9	7:0	Default : 0x00	Access : R/W
	PROTECT1_START[15:8]	7:0	Please see description of '12C8h'.	
65h (12CAh)	REG12CA	7:0	Default : 0x00	Access : R/W
	PROTECT1_END[7:0]	7:0	Protect 1 end address.	
65h (12CBh)	REG12CB	7:0	Default : 0x00	Access : R/W
	PROTECT1_END[15:8]	7:0	Please see description of '12CAh'.	
66h (12CCh)	REG12CC	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	PROTECT2_EN	0	Protect 2 enable.	
66h (12CDh)	REG12CD	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	PROTECT2_ID[5:0]	5:0	Protect 2 ID.	
67h (12CEh)	REG12CE	7:0	Default : 0x00	Access : R/W
	PROTECT2_START[7:0]	7:0	Protect 2 start address.	
67h (12CFh)	REG12CF	7:0	Default : 0x00	Access : R/W
	PROTECT2_START[15:8]	7:0	Please see description of '12CEh'.	
68h (12D0h)	REG12D0	7:0	Default : 0x00	Access : R/W
	PROTECT2_END[7:0]	7:0	Protect 2 end address.	
68h (12D1h)	REG12D1	7:0	Default : 0x00	Access : R/W
	PROTECT2_END[15:8]	7:0	Please see description of '12D0h'.	
69h (12D2h)	REG12D2	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	PROTECT3_EN	0	Protect 3 enable.	
69h (12D3h)	REG12D3	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	PROTECT3_ID[5:0]	5:0	Protect 3 ID.	
6Ah (12D4h)	REG12D4	7:0	Default : 0x00	Access : R/W
	PROTECT3_START[7:0]	7:0	Protect 3 start address.	
6Ah (12D5h)	REG12D5	7:0	Default : 0x00	Access : R/W
	PROTECT3_START[15:8]	7:0	Please see description of '12D4h'.	
6Bh (12D6h)	REG12D6	7:0	Default : 0x00	Access : R/W
	PROTECT3_END[7:0]	7:0	Protect 3 end address.	
6Bh	REG12D7	7:0	Default : 0x00	Access : R/W

MIU Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
(12D7h)	PROTECT3_END[15:8]	7:0	Please see description of '12D6h'.	
70h (12E0h)	**REG12E0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	FORCE_IN	6	Force read data to TEST_DATA.	
	FORCE_OUT	5	Force write data to TEST_DATA.	
	TEST_LOOP	4	Loop mode.	
	INV_DATA	3	Inverse test data.	
	TEST_MODE[1:0]	2:1	MIU self test mode 00: Address mode. 01: From TEST_DATA. 10: Shift data.	
	TEST_EN	0	MIU self test enable.	
70h (12E1h)	**REG12E1**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	TEST_FINISH	7	Test finish indicator.	
	TEST_FAIL	6	Test fail indicator.	
	TEST_FLAG	5	Test fail indicator.	
	-	4	Reserved.	
	TEST_BYTE[1:0]	3:2	Read back data byte switch.	
	WRITE_ONLY	1	Only issue write command.	
	READ_ONLY	0	Only issue read command.	
71h (12E2h)	**REG12E2**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_BASE[7:0]	7:0	Test base address.	
71h (12E3h)	**REG12E3**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_BASE[15:8]	7:0	Please see description of '12E2h'.	
72h (12E4h)	**REG12E4**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_LENGTH_L[7:0]	7:0	Test length.	
72h (12E5h)	**REG12E5**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_LENGTH_L[15:8]	7:0	Please see description of '12E4h'.	
73h (12E6h)	**REG12E6**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_LENGTH_H[23:16]	7:0	Test length.	
73h (12E7h)	**REG12E7**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_MASK[7:0]	7:0	Test data mask.	
74h	**REG12E8**	**7:0**	**Default : 0x00**	**Access : R/W**

MIU Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
(12E8h)	TEST_DATA[7:0]	7:0	Test data.	
74h (12E9h)	**REG12E9**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_DATA[15:8]	7:0	Please see description of '12E8h'.	
75h (12EAh)	**REG12EA**	**7:0**	**Default : -**	**Access : RO**
	TEST_STATUS[7:0]	7:0	Test status.	
75h (12EBh)	**REG12EB**	**7:0**	**Default : -**	**Access : RO**
	TEST_STATUS[15:8]	7:0	Please see description of '12EAh'.	
76h (12ECh)	**REG12EC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	DCDQSCALMODE[1:0]	5:4	Auto calibration mode.	
	-	3:1	Reserved.	
	DCENAUTOCAL	0	Auto calibration enable.	
76h (12EDh)	**REG12ED**	**7:0**	**Default : 0x00**	**Access : R/W**
	DCVSYNCNEGEDGETIME[3:0]	7:4		
	DCTIMEFORDQSDLYSTEADY[3:0]	3:0		
77h (12EEh)	**REG12EE**	**7:0**	**Default : 0x00**	**Access : R/W**
	DCSTARTADR[7:0]	7:0		
77h (12EFh)	**REG12EF**	**7:0**	**Default : 0x00**	**Access : R/W**
	DCSTARTADR[15:8]	7:0	Please see description of '12EEh'.	
78h (12F0h)	**REG12F0**	**7:0**	**Default : -**	**Access : RO**
	REGCALSTATUS[7:0]	7:0	Auto calibration status.	
79h (12F2h)	**REG12F2**	**7:0**	**Default : -**	**Access : RO**
	CAL_DQSPH1[3:0]	7:4	DQS[1] phase.	
	CAL_DQSPH0[3:0]	3:0	DQS[0] phase.	
79h (12F3h)	**REG12F3**	**7:0**	**Default : -**	**Access : RO**
	CAL_DQSPH3[3:0]	7:4	DQS[3] phase.	
	CAL_DQSPH2[3:0]	3:0	DQS[2] phase.	
7Ah (12F4h)	**REG12F4**	**7:0**	**Default : -**	**Access : RO**
	CAL_DQSPH5[3:0]	7:4	DQS[5] phase.	
	CAL_DQSPH4[3:0]	3:0	DQS[4] phase.	
7Ah (12F5h)	**REG12F5**	**7:0**	**Default : -**	**Access : RO**
	CAL_DQSPH7[3:0]	7:4	DQS[7] phase.	

MIU Register (Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CAL_DQSPH6[3:0]	3:0	DQS[6] phase.	
7Bh (12F6h)	**REG12F6**	**7:0**	**Default : -**	**Access : RO**
	CALSTATUS0[7:0]	7:0	DQS[0] status.	
7Bh (12F7h)	**REG12F7**	**7:0**	**Default : -**	**Access : RO**
	CALSTATUS1[7:0]	7:0	DQS[1] status.	
7Ch (12F8h)	**REG12F8**	**7:0**	**Default : -**	**Access : RO**
	CALSTATUS2[7:0]	7:0	DQS[2] status.	
7Ch (12F9h)	**REG12F9**	**7:0**	**Default : -**	**Access : RO**
	CALSTATUS3[7:0]	7:0	DQS[3] status.	
7Dh (12FAh)	REG12FA	**7:0**	**Default : -**	**Access : RO**
	CALSTATUS4[7:0]	7:0	DQS[4] status.	
7Dh (12FBh)	REG12FB	**7:0**	**Default : -**	**Access : RO**
	CALSTATUS5[7:0]	7:0	DQS[5] status.	
7Eh (12FCh)	REG12FC	**7:0**	**Default : -**	**Access : RO**
	CALSTATUS6[7:0]	7:0	DQS[6] status.	
7Eh (12FDh)	REG12FD	**7:0**	**Default : -**	**Access : RO**
	CALSTATUS7[7:0]	7:0	DQS[7] status.	
7Fh (12FEh)	**REG12FE**	**7:0**	**Default : 0x0C**	**Access : R/W**
	-	7:5	Reserved.	
	SYNC_OUT_THRESHOLD[4:0]	4:0	Sync out FIFO full threshold.	

HK_VD_MCU Register (Bank = 13)

HK_VD_MCU Register (Bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h ~ 06h (1300h ~ 130Bh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
06h (130Ch)	REG130C	7:0	Default : 0x03	Access : R/W
	-	7:2	Reserved.	
	HK2VD_INT	1	House keeping MCU to VDMCU interrupt.	
	VD_MCU_RESET	0	VD MCU Reset.	
06h ~ 27h (130Dh ~ 134Fh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
28h (1350h)	REG1350	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	VD_SPI_EN	2	Code using SPI.	
	VD_DRAM_EN	1	Code using DRAM.	
	VD_SRAM_EN	0	Code using SRAM.	
28h (1351h)	-	7:0	Default : -	Access : -
	-	7:3	Reserved.	
29h (1352h)	REG1352	7:0	Default : 0x00	Access : R/W
	VD_ROM_BANK	7:0	Code ROM bank.	

RF Register (Bank = 14)

RF Register (Bank = 14)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (1400h)	REG1400	7:0	Default : 0x1F	Access : R/W
	-	7	Reserved.	
	TAGC_PWR	6	Tuner AGC power control. 0: Power off. 1: Power on.	
	TAFC_PWR	5	Tuner AFC power control. 0: Power off. 1: Power on.	
	VIF_CBC_PWRS	4	Power on the sound path of central bias circuit. 0: Power off. 1: Power on (VIF_CBC_PWR must =1).	
	VIF_CBC_PWR	3	Power on central bias circuit. 0: Power off. 1: Power on.	
	VIF_PLL_PWR	2	Power on VIF PLL. 0: Power off. 1: Power on.	
	VIF_VCOREG_PWR	1	VCO regulator power on. 0: Power off. 1: Power on.	
	VIF_VCO_PWR	0	VCO power on. 0: Power off. 1: Power on.	
00h (1401h)	REG1401	7:0	Default : 0xFF	Access : R/W
	VIF_PGPWRV	7	PGA1_V power on. 0: Power off. 1: Power on.	
	VIF_MXPWRV	6	MX_V power on. 0: Power off. 1: Power on.	
	VIF_PWR_LPFV	5	LPF_V power on. 0: Power off. 1: Power on.	
	VIF_PWR_PGA2V	4	PGA2_V power on. 0: Power off. 1: Power on.	

RF Register (Bank = 14)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	VIF_PGPWRS	3	PGA1_S power on. 1: Power on. 0: Power off.
	VIF_MXPWRS	2	MX_S power on. 0: Power off. 1: Power on.
	VIF_PWR_LPFS	1	LPF_S power on. 0: Power off. 1: Power on.
	VIF_PWR_PGA2S	0	PGA2_S power on. 0: Power off. 1: Power on.
01h (1402h ~ 1403h)	-	7:0	Default : - Access : -
	-	7:0	Reserved.
02h (1404h)	**REG1404**	7:0	**Default : 0x24** **Access : R/W**
	TAGC_ODMODE	7	TAGC DAC output open-drain mode. 0: 1mA current sink output. 1: Open-drain voltage output.
	TAFC_ODMODE	6	TAFC DAC output open-drain mode. 0: 1mA current sink output. 1: Open-drain voltage output.
	VIF_PLL_MSEL	5	Bypass feedback divider re-sync function. 0: Bypass re-sync. 1: Re-sync.
	VIF_PLL_MTEST	4	Select feedback divider input source. 0: Normal operation. 1: Reference FXTAL input.
	VIF_PLL_M[3:0]	3:0	PLL post divider (divide ratio = 2~15).
02h (1405h)	**REG1405**	7:0	**Default : 0x59** **Access : R/W**
	VIF_PLL_RSEL	7	Bypass reference divider. 0: Normal operation (divide-by-2 or 3). 1: Bypass (divide-by-1).
	VIF_PLL_RDIV	6	PLL reference divider. 0: FXTAL/2. 1: FXTAL/3.
	VIF_PLL_N[5:0]	5:0	PLL feedback divider (divide ratio = 2~63) (Default: Divide-by-25).
03h	**REG1406**	7:0	**Default : 0x05** **Access : R/W**

RF Register (Bank = 14)

Index (Absolute)	Mnemonic	Bit	Description	
(1406h)	VIF_PLL_FBBYP	7	Bypass divid-by-2 in feedback divider. 0: Divide-by-2. 1: Bypass.	
	VIF_PLL_PSEL	6	Select post divider input source. 0: PLL output. 1: Core clock (215MHz) output.	
	VIF_PLL_PBYP	5	Bypass divid-by-2 in post divider. 0: Divide-by-2. 1: Bypass.	
	VIF_PLL_ADD128U	4	Enlarge the charge pump current. 0: Normal current. 1: Additional 128uA.	
	VIF_PLL_LPEX	3	Charge pump current power control. 0: Power on. 1: Power off.	
	VIF_PLL_ICTRL[2:0]	2:0	Charge pump current control; see table 2.	
03h (1407h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
04h (1408h)	REG1408	7:0	Default : 0x44	Access : R/W
	VIF_CAL_START	7	VCO band calibration start. 0: No operation (gen shot). 1: Enable.	
	-	6	Reserved.	
	-	5	Reserved.	
	-	4	Reserved.	
	VIF_PLL_CPINIT_W	3	Override bit for charge pump output open and tied to 1.50V. 0: Normal operation. 1: Charge pump output tied to 1.50V.	
	VIF_VCO_BANK_W[2:0]	2:0	Override bits for VCO bank selection; see table 4.	
04h (1409h)	REG1409	7:0	Default : 0x00	Access : R/W
	VIF_PGA1GAINV_W[3:0]	7:4	Override bits for PGA1_S gain setting low byte; see table 5.	
	VIF_PGA1GAINS_W[3:0]	3:0	Override bits for PGA1_S gain setting low byte; see table 5.	
05h	REG140A	7:0	Default : 0x00	Access : R/W

RF Register (Bank = 14)

Index (Absolute)	Mnemonic	Bit	Description	
(140Ah)	VIF_GAIN_PGA2V_W[3:0]	7:4	Override bits for PGA2_V gain setting high byte; see table 6.	
	VIF_GAIN_PGA2S_W[3:0]	3:0	Override bits for PGA2_S gain setting low byte; see table 6.	
05h (140Bh)	**REG140B**	**7:0**	**Default : 0xAA**	**Access : R/W**
	VIF_CALIB_TUNE	7	LPF calibration enable (power on). 0: Disable. 1: Enable.	
	VIF_FORCE_TUNE	6	LPF tuning override source selection. 0: Self-controlled. 1: I2C override.	
	VIF_RN_TUNE	5	Reset for LPF tuning circuit. 0: Reset (restart calibration after reset finished). 1: Normal operation.	
	VIF_FCODE_EXT[4:0]	4:0	Override bits for LPF corner tuning; see schematics for details.	
06h ~ 08h (140Ch ~ 1411h)	-	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
09h (1412h)	**REG1412**	**7:0**	**Default : 0x00**	**Access : R/W**
	TAGC_W[7:0]	7:0	TAGC DAC (2's complement; double load).	
09h (1413h)	**REG1413**	**7:0**	**Default : 0x00**	**Access : R/W**
	TAGC_W[15:8]	7:0	Please see description of '1412h'.	
0Ah (1414h)	**REG1414**	**7:0**	**Default : 0x00**	**Access : R/W**
	TAFC_W[7:0]	7:0	TAFC DAC (2's complement; double load).	
0Ah (1415h)	**REG1415**	**7:0**	**Default : 0x00**	**Access : R/W**
	TAFC_W[15:8]	7:0	Please see description of '1414h'.	
0Bh (1416h)	**REG1416**	**7:0**	**Default : 0x92**	**Access : R/W**
	TAGC_TAFC_OUTR[1:0]	7:6	1bit DAC output filter resistor setting; see table 16.	
	TAGC_INVCLK	5	Inverse clock for tuner AGC DAC. 0: Normal. 1: Inverse.	
	TAGC_POLARITY	4	Tuner AGC polarity control. 0: Negative logic. 1: Positive logic.	
	TAGC_TEST_EN	3	TAGC DAC input test enable.	

RF Register (Bank = 14)

Index (Absolute)	Mnemonic	Bit	Description
			0: Normal mode. 1: Test mode.
	TAFC_INVCLK	2	Inverse clock for tuner AFC DAC. 0: Normal. 1: Inverse.
	TAFC_POLARITY	1	Tuner AFC polarity control. 0: Negative logic. 1: Positive logic.
	TAFC_TEST_EN	0	TAFC DAC input test enable. 0: Normal mode. 1: Test mode.
0Bh (1417h)	**REG1417**	**7:0**	**Default : 0xD0** Access : R/W
	TAGC_DITHER_EN	7	Dither signal enable. 0: Disable. 1: Enable.
	TAGC_SEL_SECORDER	6	Select 2nd order delta-sigma modulator. 0: 1st order. 1: 2nd order.
	TAGC_DITHER_SHIFT[2:0]	5:3	Dither signal gain setting; 0~7 -> 2^0~2^-7.
	TAGC_SEL_DECIMATE_NUM[2:0]	2:0	Clock division ratio; see table 15.
0Ch (1418h)	**REG1418**	**7:0**	**Default : 0xD0** Access : R/W
	TAFC_DITHER_EN	7	Dither signal enable. 0: Disable. 1: Enable.
	TAFC_SEL_SECORDER	6	Select 2nd order delta-sigma modulator. 0: 1st order. 1: 2nd order.
	TAFC_DITHER_SHIFT[2:0]	5:3	Dither signal gain setting; 0~7 -> 2^0~2^-7.
	TAFC_SEL_DECIMATE_NUM[2:0]	2:0	Clock division ratio; see table 15.
0Ch (1419h)	**REG1419**	**7:0**	**Default : 0x2F** Access : R/W
	-	7:6	Reserved.
	OREN_TAGC	5	TAGC override source selection. 0: BB controlled. 1:I2C override.
	OREN_VCO_BANK	4	VCO_BANK override source selection. 0: BB controlled.

RF Register (Bank = 14)

Index (Absolute)	Mnemonic	Bit	Description	
			1: I2C override.	
	OREN_PGA1_V	3	PGA1_V override source selection. 0: BB controlled. 1: I2C override.	
	OREN_PGA2_V	2	PGA2_V override source selection. 0: BB controlled. 1: I2C override.	
	OREN_PGA1_S	1	PGA1_S override source selection. 0: BB controlled. 1: I2C override.	
	OREN_PGA2_S	0	PGA2_S override source selection. 0: BB controlled. 1: I2C override.	
0Dh (141Ah)	REG141A	7:0	Default : -	Access : RO
	-	7:3	Reserved.	
	VIF_VCO_BANK[2:0]	2:0	VCO bank selection. See Table 4.	
0Dh (141Bh)	REG141B	7:0	Default : -	Access : RO
	VIF_PGA1GAINV[3:0]	7:4	DBB PGA1_V gain setting low byte; see table 5.	
	VIF_PGA1GAINS[3:0]	3:0	DBB PGA1_S gain setting low byte; see table 5.	
0Eh (141Ch)	REG141C	7:0	Default : -	Access : RO
	VIF_GAIN_PGA2V[3:0]	7:4	DBB PGA2_V gain setting high byte; see table 6.	
	VIF_GAIN_PGA2S[3:0]	3:0	DBB PGA2_S gain setting low byte; see table 6.	
0Eh (141Dh)	REG141D	7:0	Default : -	Access : RO
	-	7	Reserved.	
	VIF_CAL_FINISH	6	VCO calibration finish.	
	VIF_STOPCAL_TUNE	5	LPF calibration finished flag. 0: Under LPF calibrating. 1: Finished (disable LPF tuning circuit clock).	
	VIF_FCODE_OUT[4:0]	4:0	LPF cap bank calibration output code.	
0Fh (141Eh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
10h (1420h)	REG1420	7:0	Default : 0x03	Access : R/W
	-	7:2	Reserved.	
	VSYNC_VD_POLARITY	1	It respects to the VSYNC polarity from VD. 0: Low active.	

RF Register (Bank = 14)

Index (Absolute)	Mnemonic	Bit	Description	
			1: High active.	
	VSYNC_VD_MASK	0	1: Mask VSYNC from VD.	
10h ~ 13h (1421h ~ 1426h)	-	7:0	**Default : -**	**Access : -**
	-	7:0	Reserved.	
30h (1460h)	**REG1460**	7:0	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	AUDIO_FIFO_BYPASS	1	1: Audio FIFO bypass.	
	AUDIO_FIFO_RSTZ	0	Audio input front end FIFO reset.	
30h (1461h)	**REG1461**	7:0	**Default : -**	**Access : RO**
	-	7:3	Reserved.	
	AUDIO_FIFO_HALF	2	1: Audio FIFO half.	
	AUDIO_FIFO_FULL	1	1: Audio FIFO full.	
	AUDIO_FIFO_EMPTY	0	1: Audio FIFO empty.	
50h (14A0h)	**REG14A0**	7:0	**Default : 0x02**	**Access : R/W**
	-	7:2	Reserved.	
	PDN_VIFADC	1	1: Power down VIF ADC.	
	VIFADC_ENABLE_VD	0	1: Enable the VIF video part.	
51h (14A2h)	**REG14A2**	7:0	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	VIFADC_GAIN[1:0]	1:0	Gain of VIF ADC.	
51h (14A3h)	**REG14A3**	7:0	**Default : 0x10**	**Access : R/W**
	-	7:5	Reserved.	
	VIFADC_OFFSET[4:0]	4:0	Offset of VIF ADC.	
54h (14A9h)	**REG14A9**	7:0	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	VIF_CVBS_CLAMP_GAIN_EN[13]	5	1: VIF CVBS CLAMP_GAIN enable.	
	-	4:0	Reserved.	
55h (14ABh)	**REG14AB**	7:0	**Default : 0x40**	**Access : R/W**
	-	7	Reserved.	
	PDN_AAF	6	1: VIF ADC GMC power down.	
	AAF_GAIN[1:0]	5:4	VIF ADC GMC gain.	
	-	3:0	Reserved.	

RF Register (Bank = 14)

Index (Absolute)	Mnemonic	Bit	Description	
56h (14ACh)	REG14AC	7:0	Default : 0x00	Access : R/W
	AAF_CTRL_OVERRIDE[7:0]	7:0	VIF ADC GMC override control code.	
56h (14ADh)	REG14AD	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	AAF_CTRL_OREN	0	1: VIF ADC GMC override enable.	
60h (14C0h)	REG14C0	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	VIFDAC_MSB_INV	4	1: DAC data out MSB invert.	
	VIFDAC_ENABLE	3	1: Enable VIF DAC control.	
	VIFDAC_OUT_SEL[2:0]	2:0	3'b000: CVBS out. 3'b001: CVBSx2 out. 3'b010: Ramp data. 3'b011: Force data. 3'b100: Debug bus.	
60h ~ 63h (14C1h ~ 14C7h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	

VIF_PLL_REGR[1:0]	VIF_CBC_BGR0	Vreg for PLL Logic (V)	Note
00	1	1.20	Vref*12/11 (default)
01	1	1.10	Vref
10	1	1.30	Vref*12/10.15
11	1	1.20	Vdd/3*12/11
00	0	1.15	Vref*12/11
01	0	1.05	Vref
10	0	1.25	Vref*12/10.15
11	0	1.20	Vdd/3*12/11

Table-1

VIF_PLL_REGR[1:0]	VIF_PLL_ICTRL[2:0]	CP Current (uA)
0		
0	000	16
0	001	24
0	010	40
0	011	56
0	100	72
0	101	88 (default)
0	110	136
0	111	248
1	000	144
1	001	152
1	010	168
1	011	184
1	100	200
1	101	216
1	110	264
1	111	376

Table-2

VCOREG_R[1:0]	Vreg for VCO (V)	Note
00	2.7	Vref*2.7/1.2 (default)
01	2.6	Vref*2.7/1.246
10	2.8	Vref*2.7/1.157
11	2.7	Vdd*2.7/3.3

Table-3

VCO_BANK[2:0]	FMIN (MHz)	FMAX (MHz)
111	117	165
110	137	194
101	175	230
100	199	261 (default)
011	247	304
010	293	358
001	347	405
000	397	462

Table-4

VIF_PGA1GAINV[3:0], VIF_PGA1GAINS[3:0]	PGA1 Gain (dB)
0000	6 (default)
0001	7
0010	8
0011	9
0100	10
0101	11
0110	12
0111	13
1000	14
1001	15
1010	16
Others	Not allowed

Table-5

VIF_GAIN_PGA2V[3:0], VIF_GAIN_PGA2S[3:0]	PGA2 Gain (dB)
0000	10 (default)
0001	11
0010	12
0011	13
0100	14
0101	15
0110	16
0111	17
1000	18
1001	19
1010	20
1011	21
1100	22
1101	23
1110	24
1111	25

Table-6

VIF_PGCR[1:0]	Ibias for PGA1 (uA)	Note
00	120	36.5uA*40/12 (default)
01	146	36.5uA*40/10
10	104	36.5uA*40/14
11	120	36.5uA*40/12

Table-7   PGA1 Bias Setting

VIF_MXLOR[3:2]	Ibias for LO Buffer (mA)	Note
00	438	Ib*48/4
01	290	Ib*48/6 (default)
10	350	Ib*48/5
11	250	Ib*48/7

Table-8   Mixer LO Buffer Bias Setting

VIF_MXCR[5:4]	Ib1 for MX Load (uA)	Note
00	36.5	36.5uA*4/4
01	54.8	36.5uA*6/4 (default)
10	45.6	36.5uA*5/4
11	63.8	36.5uA*7/4

Table-9   Mixer Load Bias Setting 2

VIF_MXCR[3:2]	Ib1 for MX Load (uA)	Note
00	73	73uA*4/4
01	109	73uA*6/4 (default)
10	91	73uA*5/4
11	127	73uA*7/4

Table-10 Mixer Load Bias Setting 1

VIF_MXCR[1:0]	Ib1 for MX Load (uA)	Note
00	60	Ib*4/4
01	90	Ib*6/4 (default)
10	73	Ib*5/4
11	105	Ib*7/4

Table-11 Mixer Load Bias Setting 0

VIF_ISW_TUNE[1:0]	Ibias for LPF Tuning Circuit (uA)	Note
00	29.2	36.5uA*0.8
01	36.5	36.5uA*1.0 (default)
10	43.8	36.5uA*1.2
11	73.0	36.5uA*2.0

Table-12 LPF Tuning Circuit Bias Setting

VIF_ISW_LPFV[1:0] VIF_ISW_LPFS[1:0]	Ibias for LPF (uA)	Note
00	29.2	36.5uA*0.8
01	36.5	36.5uA*1.0 (default)
10	43.8	36.5uA*1.2
11	73.0	36.5uA*2.0

Table-13 LPF Bias Setting

VIF_ISW_LPF2V[1:0] VIF_ISW_LPF2S[1:0]	Ibias for PGA2 (uA)	Note
00	29.2	36.5uA*0.8
01	36.5	36.5uA*1.0 (default)
10	43.8	36.5uA*1.2
11	73.0	36.5uA*2.0

Table-14 PGA2 Bias Setting

TAGC_REG_SEL_DECIMATE_NUM[2:0] TAFC_REG_SEL_DECIMATE_NUM[2:0]	Clock Division Ratio	Note
000	1	2^0 (default)
001	2	2^1
010	4	2^2
011	8	2^3
100	16	2^4
101	16	2^4
110	16	2^4
111	16	2^4

Table-15 TAGC/TAFC DAC Clock Division Ratio

TAGC_TAFC_OUTR[1:0]	ROUT (ohm)	Note
00	1000	>1.4V
01	700	>1.2V
10	400	>0.8V (default)
11	100	>0.6V

Table-16 TAGC/TAFC DAC Output Series Resistor Setting

DBB1 Register (Bank = 15)

DBB1 Register (Bank = 15)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (1500h)	REG1500	7:0	Default : 0x3F	Access : R/W
	-	7:6	Reserved.	
	AAGC_SOFT_RSTZ	5	AAGC software reset (low active).	
	VDAGC2_SOFT_RSTZ	4	VDAGC2 software reset (low active).	
	VDAGC1_SOFT_RSTZ	3	VDAGC1 software reset (low active).	
	VAGC_SOFT_RSTZ	2	VAGC software reset (low active).	
	FILTER_SOFT_RSTZ	1	Filter software reset (low active).	
	AFC_SOFT_RSTZ	0	AFC software reset (low active).	
01h (1502h)	REG1502	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	MODULATION_TYPE[3]	3	VDAGC2 modulation type. 0: Negative modulation. 1: Positive modulation.	
	MODULATION_TYPE[2]	2	VDAGC1 modulation type.	
	MODULATION_TYPE[1]	1	VAGC modulation type.	
	MODULATION_TYPE[0]	0	Filter modulation type.	
02h (1504h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
10h (1520h)	REG1520	7:0	Default : 0x60	Access : R/W
	-	7	Reserved.	
	AFC_K_SWHW_SEL	6	LF K-parameter select. 0: Hardware. 1: Software.	
	-	5	Reserved.	
	AFC_KD_IN[4:0]	4:0	LF parameter; $2^{-8} \sim 2^{-18}$.	
10h (1521h)	REG1521	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	AFC_KP_IN[3:0]	3:0	LF parameter; $2^{-1} \sim 2^{-11}$.	
11h (1522h)	REG1522	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	AFC_KI_IN[4:0]	4:0	LF parameter; $2^{-11} \sim 2^{-21}$.	
11h	REG1523	7:0	Default : 0x28	Access : R/W

DBB1 Register (Bank = 15)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1523h)	-	7:6	Reserved.	
	AFC_PRE_OFFSET_RATIO[5:0]	5:0	FOE parameter; pre-offset frequency ratio.	
12h (1524h)	**REG1524**	**7:0**	**Default : 0x28**	**Access : R/W**
	AFC_W_VIF_BB[7:0]	7:0	LF parameter; VIF baseband normal frequency (double load).	
12h (1525h)	**REG1525**	**7:0**	**Default : 0x2D**	**Access : R/W**
	-	7	Reserved.	
	AFC_W_VIF_BB[14:8]	6:0	Please see description of '1524h'.	
13h (1526h)	**REG1526**	**7:0**	**Default : 0xAE**	**Access : R/W**
	AFC_FOE_CONST[7:0]	7:0	FOE parameter; frequency offset estimation (double load).	
13h (1527h)	**REG1527**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:2	Reserved.	
	AFC_FOE_CONST[9:8]	1:0	Please see description of '1526h'.	
14h (1528h)	-	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
14h (1529h)	**REG1529**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:3	Reserved.	
	LF1_CONFIG[2:0]	2:0	EPW_LPF1 parameter; FD smoothing filter coefficient. 000: 2^{-15}. 001: 2^{-16}. 010: 2^{-17}. 011: 2^{-18}. 100: 2^{-19}.	
15h (152Ah)	**REG152A**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:3	Reserved.	
	LF2_CONFIG[2:0]	2:0	EPW_LPF2 parameter; lock signal smoothing filter coefficient. 000: 2^{-14}. 001: 2^{-15}. 010: 2^{-16}. 011: 2^{-17}. 100: 2^{-18}.	
15h (152Bh)	**REG152B**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:3	Reserved.	

DBB1 Register (Bank = 15)

Index (Absolute)	Mnemonic	Bit	Description	
	LF3_CONFIG[2:0]	2:0	EPW_LPF3 parameter; lock signal smoothing filter coefficient. 000: 2^-14. 001: 2^-15. 010: 2^-16. 011: 2^-17. 100: 2^-18.	
16h (152Ch)	REG152C	7:0	Default : 0x00	Access : R/W
	AFC_LCK1_THR[7:0]	7:0	CR_LCK1 parameter; CR_LCK1 threshold (double load).	
16h (152Dh)	REG152D	7:0	Default : 0x00	Access : R/W
	AFC_LCK1_THR[15:8]	7:0	Please see description of '152Ch'.	
17h (152Eh)	REG152E	7:0	Default : 0x0C	Access : R/W
	AFC_LCK1_THR[23:16]	7:0	Please see description of '152Ch'.	
17h (152Fh)	REG152F	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	AFC_LCK1_THR[24]	0	Please see description of '152Ch'.	
18h (1530h)	REG1530	7:0	Default : 0x00	Access : R/W
	AFC_LCK1_CNT_TARGET[7:0]	7:0	CR_LCK1 parameter; CR_LCK1 counter target (double load).	
18h (1531h)	REG1531	7:0	Default : 0x80	Access : R/W
	AFC_LCK1_CNT_TARGET[15:8]	7:0	Please see description of '1530h'.	
19h (1532h)	REG1532	7:0	Default : 0x00	Access : R/W
	AFC_LCK1_CNT_TARGET[23:16]	7:0	Please see description of '1530h'.	
19h (1533h)	REG1533	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	AFC_LCK1_CNT_TARGET[24]	0	Please see description of '1530h'.	
1Ah (1534h)	REG1534	7:0	Default : 0x00	Access : R/W
	AFC_LCK2_CNT_TARGET[7:0]	7:0	CR_LCK2 parameter; CR_LCK2 counter target (double load).	
1Ah (1535h)	REG1535	7:0	Default : 0x00	Access : R/W
	AFC_LCK2_CNT_TARGET[15:8]	7:0	Please see description of '1534h'.	
1Bh (1536h)	REG1536	7:0	Default : 0x01	Access : R/W
	AFC_LCK2_CNT_TARGET[23:16]	7:0	Please see description of '1534h'.	
1Bh	REG1537	7:0	Default : 0x00	Access : R/W

DBB1 Register (Bank = 15)

Index (Absolute)	Mnemonic	Bit	Description	
(1537h)	-	7:1	Reserved.	
	AFC_LCK2_CNT_TARGET[24]	0	Please see description of '1534h'.	
1Ch (1538h)	REG1538	7:0	Default : -	Access : RO
	AFC_FOE[7:0]	7:0	Frequency offset estimation (Unit: TUNER_FREQUENCY _STEP/4).	
1Ch (1539h)	REG1539	7:0	Default : -	Access : RO
	-	7:4	Reserved.	
	AFC_LCK2	3	CR_LCK2 lock signal.	
	AFC_LCK1	2	CR_LCK1 lock signal.	
	AFC_FOE[9:8]	1:0	Please see description of '1538h'.	
1Dh (153Ah)	REG153A	7:0	Default : -	Access : RO
	AFC_PWR[7:0]	7:0	Lock signal power.	
1Dh (153Bh)	REG153B	7:0	Default : -	Access : RO
	AFC_PWR[15:8]	7:0	Please see description of '153Ah'.	
1Eh (153Ch)	REG153C	7:0	Default : -	Access : RO
	AFC_PWR[23:16]	7:0	Please see description of '153Ah'.	
1Fh (153Eh)	REG153E	7:0	Default : -	Access : RO
	AFC_LCK_QUAL[7:0]	7:0	Lock signal quality.	
1Fh (153Fh)	REG153F	7:0	Default : -	Access : RO
	AFC_LCK_QUAL[15:8]	7:0	Please see description of '153Eh'.	
20h (1540h)	REG1540	7:0	Default : -	Access : RO
	AFC_LCK_QUAL[23:16]	7:0	Please see description of '153Eh'.	
20h (1541h)	REG1541	7:0	Default : -	Access : RO
	-	7:1	Reserved.	
	AFC_LCK_QUAL[24]	0	Please see description of '153Eh'.	
22h (1544h)	REG1544	7:0	Default : -	Access : RO
	AFC_LF__FF_STATUS[7:0]	7:0	AFC LF FF status.	
22h (1545h)	REG1545	7:0	Default : -	Access : RO
	AFC_LFF_FF_STATUS[15:8]	7:0	Please see description of '1544h'.	
23h (1546h)	REG1546	7:0	Default : -	Access : RO
	AFC_LF_FF_STATUS[23:16]	7:0	Please see description of '1544h'.	
23h (1547h)	REG1547	7:0	Default : -	Access : RO
	-	7:4	Reserved.	

DBB1 Register (Bank = 15)

Index (Absolute)	Mnemonic	Bit	Description	
	AFC_LF_FF_STATUS[27:24]	3:0	Please see description of '1544h'.	
40h (1580h)	REG1580	7:0	Default : 0x80	Access : R/W
	BYPASS_GDE	7	0: Not bypass GDE 1: Bypass GDE.	
	LPF1_NTSC	6	0: PAL. 1: NTSC	
	BYPASS_LPF1	5	0: Not bypass LPF1 1: Bypass LPF1.	
	BYPASS_HPF0	4	0: Not bypass HPF0 1: Bypass HPF0.	
	BYPASS_N_A2	3	0: Not bypass NOTCH filter A2 1: Bypass NOTCH filter A2.	
	BYPASS_N_A1	2	0: Not bypass NOTCH filter A1 1: Bypass NOTCH filter A1.	
	BYPASS_DC	1	0: Not bypass DC_NOTCH on video path 1: Bypass DC_NOTCH on video path.	
	ADC_43M	0	0: Not bypass LPF0 and A_LPF0 (ADC=85.90908MHz). 1: Bypass LPF0 and A_LPF0 (ADC=42.95454MHz).	
40h (1581h)	REG1581	7:0	Default : 0x3C	Access : R/W
	-	7:6	Reserved.	
	BYPASS_N_A3	5	0: Not bypass NOTCH filter A3. 1: bypass NOTCH filter A3.	
	VD_SIGNED_UNSIGNED	4	0: Signed. 1: unsigned.	
	AD_SIGNED_UNSIGNED	3	0: Signed. 1: unsigned.	
	BYPASS_A_NOTCH	2	0: Not bypass A_NOTCH. 1: Bypass A_NOTCH.	
	BYPASS_A_LPF1	1	0: Not bypass A_LPF1. 1: Bypass A_LPF1.	
	BYPASS_A_DC	0	0: Not bypass A_DC_NOTCH on video path. 1: Bypass A_DC_NOTCH on video path.	
41h (1582h)	REG1582	7:0	Default : 0x10	Access : R/W
	DC_C[7:0]	7:0	Coefficient of DC_NOTCH on video path.	
41h	REG1583	7:0	Default : 0x10	Access : R/W

DBB1 Register (Bank = 15)

Index (Absolute)	Mnemonic	Bit	Description	
(1583h)	A_DC_C[7:0]	7:0	Coefficient of A_DC_NOTCH on audio path.	
42h (1584h)	REG1584	7:0	Default : 0xAF	Access : R/W
	N_A1_C0[7:0]	7:0	Coefficient of NOTCH_A1 on video path (double load).	
42h (1585h)	REG1585	7:0	Default : 0x03	Access : R/W
	-	7:3	Reserved.	
	N_A1_C0[10:8]	2:0	Please see description of '1584h'.	
43h (1586h)	REG1586	7:0	Default : 0x3C	Access : R/W
	N_A1_C1[7:0]	7:0	Coefficient of NOTCH_A1 on video path (double load).	
43h (1587h)	REG1587	7:0	Default : 0x06	Access : R/W
	-	7:3	Reserved.	
	N_A1_C1[10:8]	2:0	Please see description of '1586h'.	
44h (1588h)	REG1588	7:0	Default : 0x15	Access : R/W
	N_A1_C2[7:0]	7:0	Coefficient of NOTCH_A1 on video path (double load).	
44h (1589h)	REG1589	7:0	Default : 0x04	Access : R/W
	-	7:3	Reserved.	
	N_A1_C2[10:8]	2:0	Please see description of '1588h'.	
45h (158Ah)	REG158A	7:0	Default : 0x99	Access : R/W
	N_A2_C0[7:0]	7:0	Coefficient of NOTCH_A2 on video path (double load).	
45h (158Bh)	REG158B	7:0	Default : 0x03	Access : R/W
	-	7:3	Reserved.	
	N_A2_C0[10:8]	2:0	Please see description of '158Ah'.	
46h (158Ch)	REG158C	7:0	Default : 0x3C	Access : R/W
	N_A2_C1[7:0]	7:0	Coefficient of NOTCH_A2 on video path (double load).	
46h (158Dh)	REG158D	7:0	Default : 0x06	Access : R/W
	-	7:3	Reserved.	
	N_A2_C1[10:8]	2:0	Please see description of '158Ch'.	
47h (158Eh)	REG158E	7:0	Default : 0x2D	Access : R/W
	N_A2_C2[7:0]	7:0	Coefficient of NOTCH_A2 on video path (double load).	
47h (158Fh)	REG158F	7:0	Default : 0x04	Access : R/W
	-	7:3	Reserved.	
	N_A2_C2[10:8]	2:0	Please see description of '158Eh'.	
48h (1590h)	REG1590	7:0	Default : 0xA6	Access : R/W
	AN_C0[7:0]	7:0	Coefficient of A_NOTCH on audio path (double load).	

DBB1 Register (Bank = 15)

Index (Absolute)	Mnemonic	Bit	Description	
48h (1591h)	REG1591	7:0	Default : 0x03	Access : R/W
	-	7:3	Reserved.	
	AN_C0[10:8]	2:0	Please see description of '1590h'.	
49h (1592h)	REG1592	7:0	Default : 0x4F	Access : R/W
	AN_C1[7:0]	7:0	Coefficient of A_NOTCH on audio path (double load).	
49h (1593h)	REG1593	7:0	Default : 0x06	Access : R/W
	-	7:3	Reserved.	
	AN_C1[10:8]	2:0	Please see description of '1592h'.	
4Ah (1594h)	REG1594	7:0	Default : 0x08	Access : R/W
	AN_C2[7:0]	7:0	Coefficient of A_NOTCH on audio path (double load).	
4Ah (1595h)	REG1595	7:0	Default : 0x04	Access : R/W
	-	7:3	Reserved.	
	AN_C2[10:8]	2:0	Please see description of '1594h'.	
4Bh (1596h)	REG1596	7:0	Default : 0x00	Access : R/W
	GDE_C0[7:0]	7:0	Coefficient of group delay equalizer (double load).	
4Bh (1597h)	REG1597	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	GDE_C0[8]	0	Please see description of '1596h'.	
4Ch (1598h)	REG1598	7:0	Default : 0x98	Access : R/W
	GDE_C1[7:0]	7:0	Coefficient of group delay equalizer (double load).	
4Ch (1599h)	REG1599	7:0	Default : 0x01	Access : R/W
	-	7:1	Reserved.	
	GDE_C1[8]	0	Please see description of '1598h'.	
4Dh (159Ah)	REG159A	7:0	Default : 0x68	Access : R/W
	GDE_C2[7:0]	7:0	Coefficient of group delay equalizer(double load).	
4Dh (159Bh)	REG159B	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	GDE_C2[8]	0	Please see description of '159Ah'.	
4Eh (159Ch)	REG159C	7:0	Default : 0x48	Access : R/W
	GDE_C3[7:0]	7:0	Coefficient of group delay equalizer (double load).	
4Eh (159Dh)	REG159D	7:0	Default : 0x01	Access : R/W
	-	7:1	Reserved.	
	GDE_C3[8]	0	Please see description of '159Ch'.	

DBB1 Register (Bank = 15)

Index (Absolute)	Mnemonic	Bit	Description	
4Fh (159Eh)	REG159E	7:0	Default : 0x00	Access : R/W
	GDE_C4[7:0]	7:0	Coefficient of group delay equalizer (double load).	
4Fh (159Fh)	REG159F	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	GDE_C4[8]	0	Please see description of '159Eh'.	
50h (15A0h)	REG15A0	7:0	Default : 0x00	Access : R/W
	GDE_C5[7:0]	7:0	Coefficient of group delay equalizer (double load).	
50h (15A1h)	REG15A1	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	GDE_C5[8]	0	Please see description of '15A0h'.	
51h (15A2h)	REG15A2	7:0	Default : 0x00	Access : R/W
	GDE_C6[7:0]	7:0	Coefficient of group delay equalizer (double load).	
51h (15A3h)	REG15A3	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	GDE_C6[8]	0	Please see description of '15A2h'.	
52h (15A4h)	REG15A4	7:0	Default : 0x00	Access : R/W
	GDE_C7[7:0]	7:0	Coefficient of group delay equalizer (double load).	
52h (15A5h)	REG15A5	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	GDE_C7[8]	0	Please see description of '15A4h'.	
53h (15A6h)	REG15A6	7:0	Default : 0xAF	Access : R/W
	N_A3_C0[7:0]	7:0	Coefficient of NOTCH_A3 on video path (double load).	
53h (15A7h)	REG15A7	7:0	Default : 0x03	Access : R/W
	-	7:3	Reserved.	
	N_A3_C0[10:8]	2:0	Please see description of '15A6h'.	
54h (15A8h)	REG15A8	7:0	Default : 0x3C	Access : R/W
	N_A3_C1[7:0]	7:0	Coefficient of NOTCH_A3 on video path (double load).	
54h (15A9h)	REG15A9	7:0	Default : 0x06	Access : R/W
	-	7:3	Reserved.	
	N_A3_C1[10:8]	2:0	Please see description of '15A8h'.	
55h (15AAh)	REG15AA	7:0	Default : 0x15	Access : R/W
	N_A3_C2[7:0]	7:0	Coefficient of NOTCH_A3 on video path (double load).	
55h	REG15AB	7:0	Default : 0x04	Access : R/W

DBB1 Register (Bank = 15)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
(15ABh)	-	7:3	Reserved.
	N_A3_C2[10:8]	2:0	Please see description of '15AAh'.

DBB2 Register (Bank = 16)

DBB2 Register (Bank = 16)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (1600h)	REG1600	7:0	Default : 0x04	Access : R/W
	-	7:5	Reserved.	
	VAGC_GAIN_SLOPE	4	0: Negative gain slope. 1: Positive gain slope.	
	VAGC_MEAN_SEL[1:0]	3:2	Select mean. 00: 1 line. 01: 16 line. 1x: 256 line.	
	VAGC_MD	1	Mode for positive modulation. 0: Porch. 1: Sync height (from VDAGC).	
	VAGC_ENABLE	0	0: VAGC disable. 1: VAGC enable. VAGC_ENABLE turn on must after setting ready.	
01h (1602h)	REG1602	7:0	Default : 0x40	Access : R/W
	VAGC_LINE_CNT[7:0]	7:0	Line counter max (double load).	
01h (1603h)	REG1603	7:0	Default : 0x00	Access : R/W
	VAGC_LINE_CNT[15:8]	7:0	Please see description of '1602h'.	
02h (1604h)	REG1604	7:0	Default : 0xE0	Access : R/W
	VAGC_PORCH_CNT[7:0]	7:0	Porch counter max (double load).	
02h (1605h)	REG1605	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	VAGC_PORCH_CNT[8]	0	Please see description of '1604h'.	
03h (1606h)	REG1606	7:0	Default : 0x00	Access : R/W
	VAGC_PEAK_CNT[7:0]	7:0	Peak counter max (double load).	
03h (1607h)	REG1607	7:0	Default : 0x0C	Access : R/W
	-	7:4	Reserved.	
	VAGC_PEAK_CNT[11:8]	3:0	Please see description of '1606h'.	
04h (1608h)	REG1608	7:0	Default : 0x9A	Access : R/W
	VAGC_REF[7:0]	7:0	Reference level (double load).	
04h (1609h)	REG1609	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	VAGC_REF[8]	0	Please see description of '1608h'.	

DBB2 Register (Bank = 16)					
Index (Absolute)	**Mnemonic**	**Bit**	**Description**		
05h (160Ah)	REG160A	7:0	Default : 0x04		Access : R/W
	-	7:3	Reserved.		
	VAGC_K[2:0]	2:0	Loop filter parameter. 0: > 0. 1~7 -> 2^-2~2^-8.		
06h (160Ch)	REG160C	7:0	Default : 0x00		Access : R/W
	-	7:3	Reserved.		
	VAGC_GAIN_OREN[2]	2	VGA override enable.		
	VAGC_GAIN_OREN[1]	1	PGA2 override enable.		
	VAGC_GAIN_OREN[0]	0	PGA1 override enable.		
07h (160Eh)	REG160E	7:0	Default : 0x00		Access : R/W
	-	7:4	Reserved.		
	VAGC_PGA1_OV[3:0]	3:0	PGA1 override value.		
07h (160Fh)	REG160F	7:0	Default : 0x00		Access : R/W
	-	7:4	Reserved.		
	VAGC_PGA2_OV[3:0]	3:0	PGA2 override value.		
08h (1610h)	REG1610	7:0	Default : 0x00		Access : R/W
	VAGC_VGA_OV[7:0]	7:0	VGA override value (double load).		
08h (1611h)	REG1611	7:0	Default : 0x00		Access : R/W
	VAGC_VGA_OV[15:8]	7:0	Please see description of '1610h'.		
09h (1612h)	REG1612	7:0	Default : 0x00		Access : R/W
	-	7:4	Reserved.		
	VAGC_PGA1_MIN[3:0]	3:0	PGA1 min.		
09h (1613h)	REG1613	7:0	Default : 0x0A		Access : R/W
	-	7:4	Reserved.		
	VAGC_PGA1_MAX[3:0]	3:0	PGA1 max.		
0Ah (1614h)	REG1614	7:0	Default : 0x00		Access : R/W
	-	7:4	Reserved.		
	VAGC_PGA2_MIN[3:0]	3:0	PGA2 min.		
0Ah (1615h)	REG1615	7:0	Default : 0x0F		Access : R/W
	-	7:4	Reserved.		
	VAGC_PGA2_MAX[3:0]	3:0	PGA2 max.		
0Bh	REG1616	7:0	Default : 0x00		Access : R/W

DBB2 Register (Bank = 16)

Index (Absolute)	Mnemonic	Bit	Description	
(1616h)	VAGC_VGA_MIN[7:0]	7:0	VGA min (double load).	
0Bh (1617h)	REG1617	7:0	Default : 0x80	Access : R/W
	VAGC_VGA_MIN[15:8]	7:0	Please see description of '1616h'.	
0Ch (1618h)	REG1618	7:0	Default : 0xFF	Access : R/W
	VAGC_VGA_MAX[7:0]	7:0	VGA max (double load).	
0Ch (1619h)	REG1619	7:0	Default : 0x7F	Access : R/W
	VAGC_VGA_MAX[15:8]	7:0	Please see description of '1618h'.	
10h (1620h)	REG1620	7:0	Default : -	Access : RO
	VAGC_MEAN0[7:0]	7:0	Mean: 1 line.	
10h (1621h)	REG1621	7:0	Default : -	Access : RO
	-	7:1	Reserved.	
	VAGC_MEAN0[8]	0	Please see description of '1620h'.	
11h (1622h)	REG1622	7:0	Default : -	Access : RO
	VAGC_MEAN16[7:0]	7:0	Mean: 16 lines.	
11h (1623h)	REG1623	7:0	Default : -	Access : RO
	-	7:1	Reserved.	
	VAGC_MEAN16[8]	0	Please see description of '1622h'.	
12h (1624h)	REG1624	7:0	Default : -	Access : RO
	VAGC_MEAN256[7:0]	7:0	Mean: 256 lines.	
12h (1625h)	REG1625	7:0	Default : -	Access : RO
	-	7:1	Reserved.	
	VAGC_MEAN256[8]	0	Please see description of '1624h'.	
13h (1626h)	REG1626	7:0	Default : -	Access : RO
	VAGC_DIFF[7:0]	7:0	Diff.	
13h (1627h)	REG1627	7:0	Default : -	Access : RO
	-	7:2	Reserved.	
	VAGC_DIFF[9:8]	1:0	Please see description of '1626h'.	
14h (1628h)	REG1628	7:0	Default : -	Access : RO
	VAGC_VGA[7:0]	7:0	Tuner VGA value.	
14h (1629h)	REG1629	7:0	Default : -	Access : RO
	VAGC_VGA[15:8]	7:0	Please see description of '1628h'.	
15h (162Ah)	REG162A	7:0	Default : -	Access : RO
	-	7:4	Reserved.	

DBB2 Register (Bank = 16)

Index (Absolute)	Mnemonic	Bit	Description	
	VAGC_PGA1[3:0]	3:0	PGA1.	
15h (162Bh)	REG162B	7:0	Default : -	Access : RO
	-	7:4	Reserved.	
	VAGC_PGA2[3:0]	3:0	PGA2.	
50h (16A0h)	REG16A0	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	AAGC_ENABLE	0	0: AAGC disable 1: AAGC enable AAGC_ENABLE turn on must after setting ready.	
51h (16A2h)	REG16A2	7:0	Default : 0xFF	Access : R/W
	AAGC_CNT[7:0]	7:0	AAGC counter max (double load).	
51h (16A3h)	REG16A3	7:0	Default : 0x3F	Access : R/W
	AAGC_CNT[15:8]	7:0	Please see description of '16A2h'.	
52h (16A4h)	REG16A4	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	AAGC_GAIN_OREN[1]	1	PGA2 override enable.	
	AAGC_GAIN_OREN[0]	0	PGA1 override enable.	
53h (16A6h)	REG16A6	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	AAGC_PGA1_OV[3:0]	3:0	PGA1 override value.	
53h (16A7h)	REG16A7	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	AAGC_PGA2_OV[3:0]	3:0	PGA2 override value.	
54h (16A8h)	REG16A8	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	AAGC_PGA1_MIN[3:0]	3:0	PGA1 min.	
54h (16A9h)	REG16A9	7:0	Default : 0x0A	Access : R/W
	-	7:4	Reserved.	
	AAGC_PGA1_MAX[3:0]	3:0	PGA1 max.	
55h (16AAh)	REG16AA	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	AAGC_PGA2_MIN[3:0]	3:0	PGA2 min.	
55h	REG16AB	7:0	Default : 0x0F	Access : R/W

DBB2 Register (Bank = 16)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(16ABh)	-	7:4	Reserved.	
	AAGC_PGA2_MAX[3:0]	3:0	PGA2 max.	
56h (16ACh)	REG16AC	7:0	Default : 0x18	Access : R/W
	-	7	Reserved.	
	AAGC_MEAN_MIN[6:0]	6:0	Mean min.	
56h (16ADh)	REG16AD	7:0	Default : 0x30	Access : R/W
	-	7	Reserved.	
	AAGC_MEAN_MAX[6:0]	6:0	Mean max.	
57h (16AEh)	REG16AE	7:0	Default : -	Access : RO
	-	7	Reserved.	
	AAGC_MEAN[6:0]	6:0	Mean.	
58h (16B0h)	REG16B0	7:0	Default : -	Access : RO
	-	7	Reserved.	
	AAGC_PEAKMEAN[6:0]	6:0	Peak mean.	
59h (16B2h)	REG16B2	7:0	Default : -	Access : RO
	-	7:4	Reserved.	
	AAGC_PGA1[3:0]	3:0	PGA1.	
59h (16B3h)	REG16B3	7:0	Default : -	Access : RO
	-	7:4	Reserved.	
	AAGC_PGA2[3:0]	3:0	PGA2.	
70h ~ 71h (16E0h ~ 16E3h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	

DBB3 Register (Bank = 1B)

DBB3 Register (Bank = 1B)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
00h (1B00h)	REG1B00	7:0	Default : 0x02	Access : R/W
	-	7:3	Reserved.
	VDAGC1_GAIN0_FB_EN	2	1: VDAGC1 GAIN0 feedback enable.
	VDAGC1_BYPASS	1	1: VDAGC1 bypass.
	VDAGC1_EN	0	1: VDAGC1 enable.
00h (1B01h)	REG1B01	7:0	Default : 0x02	Access : R/W
	-	7:3	Reserved.
	VDAGC2_GAIN0_FB_EN	2	1: VDAGC2 gain0 feedback enable.
	VDAGC2_BYPASS	1	1: VDAGC2 bypass.
	VDAGC2_EN	0	1: VDAGC2 enable.
01h (1B02h)	REG1B02	7:0	Default : 0x00	Access : R/W
	VDAGC1_GAIN_OVERRIDE[7:0]	7:0	VDAGC1 gain override (double load).
01h (1B03h)	REG1B03	7:0	Default : 0x10	Access : R/W
	-	7	Reserved.
	VDAGC1_OREN	6	1: VDAGC1 override enable.
	VDAGC1_GAIN_OVERRIDE[13:8]	5:0	Please see description of '1B02h'.
02h (1B04h)	REG1B04	7:0	Default : 0x00	Access : R/W
	VDAGC2_GAIN_OVERRIDE[7:0]	7:0	VDAGC2 gain override (double load).
02h (1B05h)	REG1B05	7:0	Default : 0x10	Access : R/W
	-	7	Reserved.
	VDAGC2_OREN	6	1: VDAGC2 override enable.
	VDAGC2_GAIN_OVERRIDE[13:8]	5:0	Please see description of '1B04h'.
03h (1B06h)	REG1B06	7:0	Default : 0x26	Access : R/W
	-	7:6	Reserved.
	VDAGC1_REF[5:0]	5:0	VDAGC1 reference.
03h (1B07h)	REG1B07	7:0	Default : 0x26	Access : R/W
	-	7:6	Reserved.
	VDAGC2_REF[5:0]	5:0	VDAGC2 reference.
04h (1B08h)	REG1B08	7:0	Default : 0x04	Access : R/W
	-	7:3	Reserved.
	VDAGC1_LVL_SHIFT[2:0]	2:0	VDAGC1 level shift.

DBB3 Register (Bank = 1B)

Index (Absolute)	Mnemonic	Bit	Description	
04h (1B09h)	REG1B09	7:0	Default : 0x04	Access : R/W
	-	7:3	Reserved.	
	VDAGC2_LEVEL_SHIFT[2:0]	2:0	VDAGC2 level shift.	
05h (1B0Ah)	REG1B0A	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	VDAGC1_RATIO[2:0]	2:0	VDAGC1 LPF update ratio.	
05h (1B0Bh)	REG1B0B	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	VDAGC2_RATIO[2:0]	2:0	VDAGC2 LPF update ratio.	
06h (1B0Ch)	REG1B0C	7:0	Default : 0x00	Access : R/W
	VDAGC1_PEAK_CNT[7:0]	7:0	VDAGC1 peak counter max (double load).	
06h (1B0Dh)	REG1B0D	7:0	Default : 0x0C	Access : R/W
	-	7:4	Reserved.	
	VDAGC1_PEAK_CNT[11:8]	3:0	Please see description of '1B0Ch'.	
07h (1B0Eh)	REG1B0E	7:0	Default : 0x00	Access : R/W
	VDAGC2_PEAK_CNT[7:0]	7:0	VDAGC2 peak counter max (double load).	
07h (1B0Fh)	REG1B0F	7:0	Default : 0x0C	Access : R/W
	-	7:4	Reserved.	
	VDAGC2_PEAK_CNT[11:8]	3:0	Please see description of '1B0Eh'.	
08h (1B10h)	REG1B10	7:0	Default : 0xF8	Access : R/W
	VDAGC1_PORCH_CNT[7:0]	7:0	VDAGC1 porch counter max (double load).	
08h (1B11h)	REG1B11	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	VDAGC1_PORCH_CNT[8]	0	Please see description of '1B10h'.	
09h (1B12h)	REG1B12	7:0	Default : 0xF8	Access : R/W
	VDAGC2_PORCH_CNT[7:0]	7:0	VDAGC2 porch counter max (double load).	
09h (1B13h)	REG1B13	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	VDAGC2_PORCH_CNT[8]	0	Please see description of '1B12h'.	
0Ah (1B14h)	REG1B14	7:0	Default : -	Access : RO
	VDAGC1_MEAN[7:0]	7:0	VDAGC1 mean.	
0Ah (1B15h)	REG1B15	7:0	Default : -	Access : RO
	VDAGC1_MEAN[15:8]	7:0	Please see description of '1B14h'.	

DBB3 Register (Bank = 1B)

Index (Absolute)	Mnemonic	Bit	Description	
0Bh (1B16h)	REG1B16	7:0	Default : -	Access : RO
	VDAGC1_VAR[7:0]	7:0	VDAGC1 variance.	
0Bh (1B17h)	REG1B17	7:0	Default : -	Access : RO
	VDAGC1_VAR[15:8]	7:0	Please see description of '1B16h'.	
0Ch (1B18h)	REG1B18	7:0	Default : -	Access : RO
	VDAGC2_MEAN[7:0]	7:0	VDAGC2 mean.	
0Ch (1B19h)	REG1B19	7:0	Default : -	Access : RO
	VDAGC2_MEAN[15:8]	7:0	Please see description of '1B18h'.	
0Dh (1B1Ah)	REG1B1A	7:0	Default : -	Access : RO
	VDAGC2_VAR[7:0]	7:0	VDAGC2 variance.	
0Dh (1B1Bh)	REG1B1B	7:0	Default : -	Access : RO
	VDAGC2_VAR[15:8]	7:0	Please see description of '1B1Ah'.	
0Eh (1B1Ch)	REG1B1C	7:0	Default : -	Access : RO
	VDAGC1_GAIN[7:0]	7:0	VDAGC1 internal gain.	
0Eh (1B1Dh)	REG1B1D	7:0	Default : -	Access : RO
	-	7:6	Reserved.	
	VDAGC1_GAIN[13:8]	5:0	Please see description of '1B1Ch'.	
0Fh (1B1Eh)	REG1B1E	7:0	Default : -	Access : RO
	VDAGC2_GAIN[7:0]	7:0	VDAGC2 internal gain.	
0Fh (1B1Fh)	REG1B1F	7:0	Default : -	Access : RO
	-	7:6	Reserved.	
	VDAGC2_GAIN[13:8]	5:0	Please see description of '1B1Eh'.	
10h (1B20h)	REG1B20	7:0	Default : -	Access : RO
	VDAGC1_SYNCHEIGHT[7:0]	7:0	VDAGC1 sync height.	
10h (1B21h)	REG1B21	7:0	Default : -	Access : RO
	-	7:5	Reserved.	
	VDAGC1_VSYNC	4	VDAGC1 VSYNC coast pulse (high active).	
	-	3:1	Reserved.	
	VDAGC1_SYNCHEIGHT[8]	0	Please see description of '1B20h'.	
11h (1B22h)	REG1B22	7:0	Default : -	Access : RO
	VDAGC2_SYNCHEIGHT[7:0]	7:0	VDAGC2 sync height.	
11h (1B23h)	REG1B23	7:0	Default : -	Access : RO
	-	7:5	Reserved.	

DBB3 Register (Bank = 1B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VDAGC2_VSYNC	4	VDAGC2 VSYNC coast pulse (high active).	
	-	3:1	Reserved.	
	VDAGC2_SYNCHEIGHT[8]	0	Please see description of '1B22h'.	
12h (1B24h)	REG1B24	7:0	Default : -	Access : RO
	VDAGC1_LPF_DELAY_0[7:0]	7:0	VDAGC1 LPF delay line first element.	
12h (1B25h)	REG1B25	7:0	Default : -	Access : RO
	-	7:1	Reserved.	
	VDAGC1_LPF_DELAY_0[8]	0	Please see description of '1B24h'.	
13h (1B26h)	REG1B26	7:0	Default : -	Access : RO
	VDAGC2_LPF_DELAY_0[7:0]	7:0	VDAGC2 LPF delay line first element.	
13h (1B27h)	REG1B27	7:0	Default : -	Access : RO
	-	7:1	Reserved.	
	VDAGC2_LPF_DELAY_0[8]	0	Please see description of '1B26h'.	

OSD Register (Bank = 1C)

OSD Register (Bank = 1C)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
00h (1C01h)	**REG1C01**	**7:0**	**Default : 0x00** Access : R/W
	-	7:3	Reserved.
	DBL[1:0]	2:1	Double buffer load. 00: Keep old register value. 01: Load new data (auto reset to 00 when load finish). 10: Automatically load data at VSYNC blanking. 11: Reserved.
	DBE	0	Double buffer enable. 0: Disable. 1: Enable.
01h (1C02h)	**REG1C02**	**7:0**	**Default : 0x00** Access : R/W DB
	OHSTA[7:0]	7:0	OSD window horizontal start position = OHSTA (pixel).
01h (1C03h)	**REG1C03**	**7:0**	**Default : 0x00** Access : R/W DB
	-	7:3	Reserved.
	OHSTA[10:8]	2:0	Please see description of '1C02h'.
02h (1C04h)	**REG1C04**	**7:0**	**Default : 0x00** Access : R/W DB
	OVSTA[7:0]	7:0	OSD window vertical start position = OVSTA (line).
02h (1C05h)	**REG1C05**	**7:0**	**Default : 0x00** Access : R/W DB
	-	7:3	Reserved.
	OVSTA[10:8]	2:0	Please see description of '1C04h'.
03h (1C06h)	**REG1C06**	**7:0**	**Default : 0x00** Access : R/W DB
	-	7	Reserved.
	OSDW[6:0]	6:0	OSD window width = OSDW + 1 (column), maximum 96 columns.
03h (1C07h)	**REG1C07**	**7:0**	**Default : 0x00** Access : R/W DB
	-	7:6	Reserved.
	OSDH[5:0]	5:0	OSD window vertical height = OSDH + 1 (row), maximum 64 rows.
04h (1C08h)	**REG1C08**	**7:0**	**Default : 0x00** Access : R/W
	-	7	Reserved.
	OHSPA[6:0]	6:0	OSD window horizontal space start position = OHSPA + 1 (row).
04h	**REG1C09**	**7:0**	**Default : 0x00** Access : R/W

OSD Register (Bank = 1C)

Index (Absolute)	Mnemonic	Bit	Description	
(1C09h)	-	7:6	Reserved.	
	OVSPA[5:0]	5:0	OSD window vertical space start position = OVSPA + 1 (column).	
05h (1C0Ah)	**REG1C0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSPW[9:2]	7:0	OSD space width = 2 * OSPW (pixel).	
05h (1C0Bh)	**REG1C0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSPH[9:2]	7:0	OSD space height = 2 * OSPH (pixel).	
06h (1C0Ch)	**REG1C0C**	**7:0**	**Default : 0x00**	**Access : R/W, DB**
	OVS[1:0]	7:6	OSD vertical scaling. 00: Vertical normal size. 01: Vertical enlarged x2 by repeated pixels. 10: Vertical enlarged x3 by repeated pixels. 11: Vertical enlarged x4 by repeated pixels.	
	OHS[1:0]	5:4	OSD Horizontal Scaling. 00: Horizontal normal size. 01: Horizontal enlarged x2 by repeated pixels. 10: Horizontal enlarged x3 by repeated pixels. 11: Horizontal enlarged x4 by repeated pixels.	
	-	3:1	Reserved	
	MWIN	0	OSD main window display. 0: Main window off. 1: Main window on.	
06h (1C0Dh)	**REG1C0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MFWZ_EN	7	Mono font width zoom x2 enable.	
	-	6	Reserved.	
	MFHZ_EN	5	Mono font high zoom x2/x4 enable. When this bit is set, AEh[3] will be treated as code index bit9 with Mono Font 1K Mode.	
	MT_EN	4	Mono texture enable.	
	TEX_TRASP_EN	3	Texture transparency enable. 0: Disable. 1: Enable.	
	MF16P	2	OSD mono font uses first 16 colors of 256-color palette. 0: Disable. 1: Enable.	
	C16PT_EN	1	OSD 16-color palette transparency enable.	

OSD Register (Bank = 1C)

Index (Absolute)	Mnemonic	Bit	Description	
			0: Disable. 1: Enable. When this bit is set, color index 0x0F will be treated as transparency.	
	CP_SEL	0	OSD color palette select. 0: 16-color palette. 1: 256-color palette.	
07h (1C0Eh)	**REG1C0E**	**7:0**	**Default : 0x00**	**Access : R/W, DB**
	SDALL	7	Shadow with All OSD direction, co-work with bit 4. 0: Shadow at right/down side. 1: Shadow at all sides.	
	TXEN	6	OSD texture function enable. 0: Disable. 1: Enable.	
	O_BLK	5	Whole OSD blink function enable. 0: Disable. 1: Enable.	
	SDC	4	OSD window shadow control. 0: Off. 1: On.	
	SCLR[3:0]	3:0	OSD window shadow color index. 0000: Color index 0. 0001: Color index 1. ... 1111: Color index 15.	
07h (1C0Fh)	**REG1C0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSDSH[3:0]	7:4	OSD shadow height.	
	OSDSW[3:0]	3:0	OSD shadow width.	
08h (1C10h ~ 1C11h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
09h (1C12h)	**REG1C12**	**7:0**	**Default : 0x00**	**Access : R/W**
	COFFS_SEL	7	OSD code buffer offset select. 0: Use OSDW[6:0] as offset. 1: Use OOFFS[6:0] as offset.	
	OOFFS[6:0]	6:0	OSD code buffer Offset value.	
09h	**REG1C13**	**7:0**	**Default : 0x00**	**Access : R/W, DB**

OSD Register (Bank = 1C)

Index (Absolute)	Mnemonic	Bit	Description	
(1C13h)	OSDBA[7:0]	7:0	OSD code base address.	
0Ah (1C14h)	**REG1C14**	**7:0**	**Default : 0x00**	**Access : R/W, DB**
	-	7:4	Reserved.	
	OSDBA[11:8]	3:0	Please see description of '1C13h'.	
0Ah (1C15h)	**REG1C15**	**7:0**	**Default : 0x00**	**Access : R/W**
	GVS[1:0]	7:6	Gradually color vertical scaling. 00: Vertical normal size. 01: Vertical enlarged x2 by repeated pixels. 10: Vertical enlarged x3 by repeated pixels. 11: Vertical enlarged x4 by repeated pixels.	
	GHS[1:0]	5:4	Gradually color horizontal scaling. 00: Horizontal normal size. 01: Horizontal enlarged x2 by repeated pixels. 10: Horizontal enlarged x3 by repeated pixels. 11: Horizontal enlarged x4 by repeated pixels.	
	GRAD	3	Enable OSD gradually color function. 0: Disable. 1: Enable.	
	GCRNG[2:0]	2:0	Gradually color applied range. 000: OSD sub window 0. 001: OSD sub window 1. 010: OSD sub window 2. 011: OSD sub window 3. 1xx: Full screen.	
0Bh (1C16h)	**GRADCLR**	**7:0**	**Default : 0x00**	**Access : R/W**
	GCS	7	Gradually color source. 0: Use this register bit[5:0] to define color. 1: Use Bank 00 background color to define color.	
	F/B	6	Gradually applied color. 0: Background color. 1: Foreground color.	
	RCLR[1:0]	5:4	Red starting gradually color. 00: Red color is 00h. 01: Red color is 55h. 10: Red color is AAh. 11: Red color is FFh.	
	GCLR[1:0]	3:2	Green starting gradually color.	

OSD Register (Bank = 1C)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
			00: Green color is 00h. 01: Green color is 55h. 10: Green color is AAh. 11: Green color is FFh.
	BCLR[1:0]	1:0	Blue starting gradually color. 00: Blue color is 00h. 01: Blue color is 55h. 10: Blue color is AAh. 11: Blue color is FFh.
0Bh (1C17h)	REG1C17	7:0	Default : 0x00 — Access : R/W
	SR	7	Sign bit of red color. 0: Increase. 1: Decrease.
	IRH	6	Inverse bit of red color. 0: Normal. 1: Invert.
	R_GRADH[5:0]	5:0	Increase/Decrease value of red color.
0Ch (1C18h)	REG1C18	7:0	Default : 0x00 — Access : R/W
	SG	7	Sign bit of green color. 0: Increase. 1: Decrease.
	IGH	6	Inverse bit of green color. 0: Normal. 1: Invert.
	G_GRADH[5:0]	5:0	Increase/Decrease value of green color.
0Ch (1C19)	REG1C19	7:0	Default : 0x00 — Access : R/W
	SB	7	Sign bit of blue color. 0: Increase. 1: Decrease.
	IBH	6	Inverse bit of blue color. 0: Normal. 1: Invert.
	B_GRADH[5:0]	5:0	Increase/Decrease value of blue color.
0Dh (1C1A)	REG1C1A	7:0	Default : 0x00 — Access : R/W
	HGRADSR[7:0]	7:0	Horizontal gradually step of red color.
0Dh	REG1C1B	7:0	Default : 0x00 — Access : R/W

OSD Register (Bank = 1C)

Index (Absolute)	Mnemonic	Bit	Description	
(1C1Bh)	HGRADSG[7:0]	7:0	Horizontal gradually step of green color.	
0Eh (1C1Ch)	REG1C1C	7:0	Default : 0x00	Access : R/W
	HGRADSB[7:0]	7:0	Horizontal gradually step of blue color.	
	For example, of RCLR=0, R_GRADH=16h, and HGRADSR=20h, then Pixel 0 ~ 19 = 0; Pixel 20 ~ 39 = 16; Pixel 40 ~ 59 = 32; ... etc.			
0Eh (1C1Dh)	REG1C1D	7:0	Default : 0x00	Access : R/W
	SR	7	Sign bit of red color. 0: Increase. 1: Decrease.	
	IRV	6	Inverse bit of red color. 0: Normal. 1: Invert.	
	R_GRADV[5:0]	5:0	Increase/Decrease value of red color.	
0Fh (1C1Eh)	REG1C1E	7:0	Default : 0x00	Access : R/W
	SG	7	Sign bit of green color. 0: Increase. 1: Decrease.	
	IGV	6	Inverse bit of green color. 0: Normal. 1: Invert.	
	G_GRADV[5:0]	5:0	Increase/Decrease value of green color.	
0Fh (1C1Fh)	REG1C1F	7:0	Default : 0x00	Access : R/W
	SB	7	Sign bit of blue color. 0: Increase. 1: Decrease.	
	IBV	6	Inverse bit of blue color. 0: Normal. 1: Invert.	
	B_GRADV[5:0]	5:0	Increase/Decrease value of blue color.	
10h (1C20h)	REG1C20	7:0	Default : 0x00	Access : R/W
	VGRADSR[7:0]	7:0	Vertical gradually step of red color.	
10h (1C21h)	REG1C21	7:0	Default : 0x00	Access : R/W
	VGRADSG[7:0]	7:0	Vertical gradually step of green color.	

OSD Register (Bank = 1C)				
Index (Absolute)	Mnemonic	Bit	Description	
11h (1C22h)	REG1C22	7:0	Default : 0x00	Access : R/W
	VGRADSB[7:0]	7:0	Vertical gradually step of blue color.	
11h (1C23h)	REG1C23	7:0	Default : 0x00	Access : R/W, DB
	-	7:2	Reserved.	
	SUB0C	1	OSD sub window 0 color select. 0: From OSD sub window 0 attribute. 1: From attribute RAM.	
	SUB0E	0	Enable OSD sub window 0. 0: Disable. 1: Enable.	
12h (1C24h)	REG1C24	7:0	Default : 0x00	Access : R/W, DB
	-	7	Reserved.	
	SUB0HST[6:0]	6:0	OSD sub window 0 horizontal start position.	
12h (1C25h)	REG1C25	7:0	Default : 0x00	Access : R/W, DB
	-	7	Reserved.	
	SUB0HEND[6:0]	6:0	OSD sub window 0 horizontal end position.	
13h (1C26h)	REG1C26	7:0	Default : 0x00	Access : R/W, DB
	-	7:6	Reserved.	
	SUB0VST[5:0]	5:0	OSD sub window 0 vertical start position.	
13h (1C27h)	SUB0VEND	7:0	Default : 0x00	Access : R/W, DB
	-	7:6	Reserved.	
	SUB0VEND[5:0]	5:0	OSD sub window 0 vertical end position.	
14h (1C28h)	REG1C28	7:0	Default : 0x00	Access : R/W
	FGCLR[3:0]	7:4	OSD sub window 0 foreground color select. 0000: Color index 0. 0001: Color index 1. ... 1110: Color index E. 1111: Color index F.	
	BGCLR[3:0]	3:0	OSD sub window 0 background color select. 0000: Color index 0. 0001: Color index 1. ... 1110: Color index E. 1111: Color index F.	

OSD Register (Bank = 1C)

Index (Absolute)	Mnemonic	Bit	Description	
14h (1C29h)	REG1C29	7:0	Default : 0x00	Access : R/W, DB
	-	7:2	Reserved.	
	SUB1C	1	OSD sub window 1 color select.	
	SUB1E	0	Enable OSD sub window 1.	
15h (1C2Ah)	REG1C2A	7:0	Default : 0x00	Access : R/W, DB
	-	7	Reserved.	
	SUB1HST[6:0]	6:0	Sub window 1 horizontal start position.	
15h (1C2Bh)	REG1C2B	7:0	Default : 0x00	Access : R/W, DB
	-	7	Reserved.	
	SUB1HEND[6:0]	6:0	OSD sub window 1 horizontal end position.	
16h (1C2Ch)	REG1C2C	7:0	Default : 0x00	Access : R/W, DB
	-	7:6	Reserved.	
	SUB1VST[5:0]	5:0	OSD sub window 1 vertical start position.	
16h (1C2Dh)	REG1C2D	7:0	Default : 0x00	Access : R/W, DB
	-	7:6	Reserved.	
	SUB1VEND[5:0]	5:0	OSD sub window 1 vertical end position.	
17h (1C2Eh)	REG1C2E	7:0	Default : 0x00	Access : R/W
	FGCLR[3:0]	7:4	OSD sub window 1 foreground color select. 0000: Color index 0. 0001: Color index 1. ... 1111: Color index F.	
	BGCLR[3:0]	3:0	OSD sub window 1 background color select. 0000: Color index 0. 0001: Color index 1. ... 1110: Color index E. 1111: Color index F.	
17h (1C2Fh)	REG1C2F	7:0	Default : 0x00	Access : R/W, DB
	-	7:2	Reserved.	
	SUB2C	1	OSD sub window 2 color select.	
	SUB2E	0	Enable OSD sub window 2.	
18h (1C30h)	REG1C30	7:0	Default : 0x00	Access : R/W, DB
	-	7	Reserved.	

OSD Register (Bank = 1C)

Index (Absolute)	Mnemonic	Bit	Description	
	SUB2HST[6:0]	6:0	OSD sub window 2 horizontal start position.	
18h (1C31h)	REG1C31	7:0	Default : 0x00	Access : R/W, DB
	-	7	Reserved.	
	SUB2HEND[6:0]	6:0	OSD sub window 2 horizontal end position.	
19h (1C32h)	REG1C32	7:0	Default : 0x00	Access : R/W, DB
	-	7:6	Reserved.	
	SUB2VST[5:0]	5:0	OSD sub window 2 vertical start position.	
19h (1C33h)	REG1C33	7:0	Default : 0x00	Access : R/W, DB
	-	7:6	Reserved.	
	SUB2VEND[5:0]	5:0	OSD sub window 2 vertical end position.	
1Ah (1C34h)	REG1C34	7:0	Default : 0x00	Access : R/W
	FGCLR[3:0]	7:4	OSD sub window 2 foreground color select. 0000: Color index 0. 0001: Color index 1. ... 1111: Color index F.	
	BGCLR[3:0]	3:0	OSD sub window 2 background color select. 0000: Color index 0. 0001: Color index 1. ... 1110: Color index E. 1111: Color index F.	
1Ah (1C35h)	REG1C35	7:0	Default : 0x00	Access : R/W, DB
	-	7:2	Reserved.	
	SUB3C	1	OSD sub window 3 color select.	
	SUB3E	0	Enable OSD sub window 3.	
1Bh (1C36h)	REG1C36	7:0	Default : 0x00	Access : R/W, DB
	-	7	Reserved.	
	SUB3HST[6:0]	6:0	OSD sub window 3 horizontal start position.	
1Bh (1C37h)	REG1C37	7:0	Default : 0x00	Access : R/W, DB
	-	7	Reserved.	
	SUB3HEND[6:0]	6:0	OSD sub window 3 horizontal end position.	
1Ch (1C38h)	REG1C38	7:0	Default : 0x00	Access : R/W, DB
	-	7:6	Reserved.	

OSD Register (Bank = 1C)					
Index (Absolute)	**Mnemonic**	**Bit**	**Description**		
	SUB3VST[5:0]	5:0	OSD sub window 3 vertical start position.		
1Ch (1C39h)	**REG1C39**	**7:0**	**Default : 0x00**	**Access : R/W, DB**	
	-	7:6	Reserved.		
	OSDSUB3VEND[5:0]	5:0	OSD sub window 3 vertical end position.		
1Dh (1C3Ah)	**REG1C3A**	**7:0**	**Default : 0x00**	**Access : R/W**	
	FGCLR[3:0]	7:4	OSD sub window 3 foreground color select. 0000: Color index 0. 0001: Color index 1. ... 1111: Color index F.		
	BGCLR[3:0]	3:0	OSD sub window 3 background color select. 0000: Color index 0. 0001: Color index 1. ... 1110: Color index E. 1111: Color index F.		
1Dh (1C3Bh)	**REG1C3B**	**7:0**	**Default : 0x00**	**Access : R/W**	
	-	7	Reserved.		
	OHSPA2[6:0]	6:0	OSD window horizontal space start position 2 = OHSPA 2+ 1 (row).		
1Eh (1C3Ch)	**REG1C3C**	**7:0**	**Default : 0x00**	**Access : R/W**	
	-	7:6	Reserved.		
	OVSPA2[5:0]	5:0	OSD window vertical space start position 2 = OVSPA 2+ 1 (column).		
1Eh (1C3Dh)	**REG1C3D**	**7:0**	**Default : 0x00**	**Access : R/W**	
	OSPW2[9:2]	7:0	OSD space width 2 = 2 * OSPW2 (pixel).		
1Fh (1C3Eh)	**REG1C3E**	**7:0**	**Default : 0x00**	**Access : R/W**	
	OSPH2[9:2]	7:0	OSD space height 2 = 2 * OSPH2 (pixel).		
1Fh (1C3Fh)	**REG1C3F**	**7:0**	**Default : 0x00**	**Access : R/W**	
	BREN	7	OSD brightness enable.		
	BRDIR	6	OSD brightness direction. 0: Increase. 1: Decrease.		
	DBRVAL[5:0]	5:0	OSD brightness value * 4.		
20h	-	7:0	**Default : -**	**Access : -**	

OSD Register (Bank = 1C)

Index (Absolute)	Mnemonic	Bit	Description	
(1C40h)	-	7:0	Reserved.	
20h (1C41h)	**REG1C42**	**7:0**	**Default : 0x1F**	**Access : R/W**
	BLINKSPD[7:0]	7:0	OSD blink speed, the numbers of VSYNCx2.	
21h (1C42h)	**REG1C43**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCRLSPD[7:0]	7:0	OSD Scroll function speed, the numbers of VSYNCx2.	
21h (1C43h)	**SCRLLINE**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCREN	7	OSD scroll function enable.	
	VSCR_FAST	6	Scroll at every VSYNC.	
	TRUC_EN	5	Truncate code/attribute enable.	
	SCRLLINE	4:0	OSD scroll function, the numbers of scan lines per scroll.	
22h (1C44h)	**REG1C44**	**7:0**	**Default :**	**Access : R/W**
	-	7:6	Reserved.	
	TEXIR[5:0]	5:0	Initial texture row number. Hardware will automatically increase after scrolling. Software must clear this register after scrolling if texture function is used.	
22h (1C45h)	-	7:0	**Default : -**	**Access : -**
	-	7:0	Reserved.	
23h (1C46h)	**REG1C46**	**7:0**	**Default : 0x10**	**Access : R/W**
	FONT_W	7	0: Write font with width 12. 1: Write font with width 16.	
	FONT_H16	6	0: Write font with height 18. 1: Write font with height 16.	
	FNT_W16	5	0: Font width depends on AEh[1]. 1: Force display font width 16.	
	FNT_W12	4	0: Font width depends on AEh[1]. 1: Force display font width 12.	
	FONT_H32	3	0: Write font with height 18. 1: Write font with height 32. Do not simultaneously set bit[6] and bit[3].	
	-	2	Reserved.	
	CFD	1	Color font number double. 0: Disable. 1: Enable. For 4MX16 DDR SDRAM (4Bank, COL8 DDR SDRAM). Color font will be doubled to 256.	

OSD Register (Bank = 1C)

Index (Absolute)	Mnemonic	Bit	Description	
			For 8MX16 DDR SDRAM (4Bank, COL9 DDR SDRAM), color font will be doubled to 512. For 8MX16 SDRAM (4Bank, COL8 SDRAM), color font will be doubled to 256.	
	MFD	0	Mono font number double. 0: Disable. 1: Enable. For 4MX16 DDR SDRAM (4Bank, Col8 DDR SDRAM) or 1MX16 SDRAM (2Bank, Col8 SDRAM), mono font will be doubled to 512. For 8MX16 DDR SDRAM (4Bank, Col9 DDR SDRAM) or 8MX16 SDRAM (4Bank , Col8 SDRAM), mono font will be doubled to 1024. Meanwhile, code index bit9 is AEh[3] when DOSD BK 0Dh[5]=1, code index bit9 is AEh[1] when DOSD BK 0Dh[5]=0.	
23h (1C47h)	**REG1C47**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	DEF_CH_W[3:0]	3:0	The real display font width of font width 16.	
24h (1C48h)	**REG1C48**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:4	Reserved.	
	DEF_CH_H[3:0]	3:0	The display font Height of display OSD (2*(DEF_CH_H +1)).	
24h (1C49h)	**REG1C49**	**7:0**	**Default : 0x31**	**Access : R/W**
	CA_TRC_NUM	7:0	Truncate number of 4k code/attribute, only active when 43h[5] is set.	
25h (1C4Ah)	**REG1C4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DEF_TEX_CLR[3:0]	3:0	When bank 0 REG 76h[7]=1, attribute bit[14:12] is used to define OSD blending level. Then texture color 4 high bits of 256 palette is defined here.	
25h (1C4Bh)	**REG1C4B**	**7:0**	**Default : 0x00**	**Access : R/W**
	ITATLIC_RS_OFST[1:0]	7:6	OSD Italic right shift offset. 00: 1 pixel. 01: 2 pixels. 10: 3 pixels. 11: 4 pixels.	
	ITALIC_1ST_LINE[1:0]	5:4	OSD Italic start scan line. 00: 0 line.	

OSD Register (Bank = 1C)

Index (Absolute)	Mnemonic	Bit	Description	
			01: 1 lines.	
			10: 2 lines.	
			11: 3 lines.	
	ITALIC_LS_STEP[1:0]	3:2	OSD Italic left shift step.	
			00: 0.001 (pixel, binary).	
			01: 0.010 (pixel, binary).	
			10: 0.011 (pixel, binary).	
			11: 0.100 (pixel, binary).	
	ITATLIC_EN	1	OSD Italic function enable.	
	ITALIC_FORCE	0	All mono character force to Italic.	
26h (1C4Ch)	**REG1C4C**	**7:0**	**Default : 0x81**	**Access : R/W**
	UN_LL	7	Under line at last line.	
	UN_LL2	6	Under line at last 2 lines.	
	OSD_MUX_IP_DATA	5	OSD MUX with IP data path.	
			0: Main window.	
			1: Sub window.	
	OSD_IVS_SEL	4	OSD input VSYNC signal select.	
			0: Sample range V signal related.	
			1: VSYNC signal related.	
	-	3:2	Reserved.	
	OSD_EXT	1	OSD 8bit -> 10 bit extend method.	
			0: extend 0.	
			1: extend MSB.	
	DISP_4B	0	Display 4 bits/pixel enable.	
26h ~ 27h (1C4Dh ~ 1C4Eh)	-	7:0	**Default : -**	**Access : -**
	-	7:0	Reserved.	
27h (1C4Fh)	**REG1C4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	ABM[2:0]	2:0	Alpha blending mode.	
			000: No alpha blending.	
			001: Background alpha blending.	
			101: Foreground alpha blending.	
			011: Color key alpha blending.	
			100: Not color key alpha blending.	
			101: Entire OSD alpha blending.	
			11x: Reserved.	

OSD Register (Bank = 1C)

Index (Absolute)	Mnemonic	Bit	Description	
28h (1C50h)	REG1C50	7:0	Default : 0x00	Access : R/W
	OSDCKEY1[7:0]	7:0	OSD color key 1 for 256-color palette.	
28h (1C51h)	REG1C51	7:0	Default : 0x00	Access : R/W
	OSDCKEY2[7:0]	7:0	OSD color key 2 for 256-color palette.	
29h (1C52h)	REG1C52	7:0	Default : 0x00	Access : R/W
	OSDCKEY3[7:0]	7:0	OSD color key 3 for 256-color palette.	
29h (1C53h)	REG1C53	7:0	Default : 0x00	Access : R/W
	OSDCKEY4[7:0]	7:0	OSD color key 4 for 256-color palette.	
2Ah (1C54h)	REG1C54	7:0	Default : 0x00	Access : R/W
	OSDCKEY5[7:0]	7:0	OSD color key 5 for 256-color palette.	
2Ah (1C55h)	REG1C55	7:0	Default : 0x00	Access : R/W
	OSDCKEY6[7:0]	7:0	OSD color key 6 for 256-color palette.	
2Bh (1C56h)	REG1C56	7:0	Default : 0x00	Access : R/W
	OSDCKEY7[7:0]	7:0	OSD color key 7 for 256-color palette.	
2Bh (1C57h)	REG1C57	7:0	Default : 0x00	Access : R/W
	OSDCKEY8[7:0]	7:0	OSD color key 8 for 256-color palette.	
2Ch (1C58h)	REG1C58	7:0	Default : 0x00	Access : R/W
	OSDCKEY9[7:0]	7:0	OSD color key 9 for 256-color palette.	
2Ch (1C59h)	REG1C59	7:0	Default : 0x00	Access : R/W
	OSDCKEY10[7:0]	7:0	OSD color key 10 for 256-color palette.	
2Dh (1C5Ah)	REG1C5A	7:0	Default : 0x00	Access : R/W
	OSDCKEY11[7:0]	7:0	OSD color key 11 for 256-color palette.	
2Dh (1C5Bh)	REG1C5B	7:0	Default : 0x00	Access : R/W
	OSDCKEY12[7:0]	7:0	OSD color key 12 for 256-color palette.	
2Eh (1C5Ch)	REG1C5C	7:0	Default : 0x00	Access : R/W
	OSDCKEY13[7:0]	7:0	OSD color key 13 for 256-color palette.	
2Eh (1C5Dh)	REG1C5D	7:0	Default : 0x00	Access : R/W
	OSDCKEY14[7:0]	7:0	OSD color key 14 for 256-color palette.	
2Fh (1C5Eh)	REG1C5E	7:0	Default : 0x00	Access : R/W
	OSDCKEY15[7:0]	7:0	OSD color key 15 for 256-color palette.	
2Fh (1C5Fh)	REG1C5F	7:0	Default : 0x00	Access : R/W
	OSDCKEY16[7:0]	7:0	OSD color key 16 for 256-color palette.	
30h	REG1C60	7:0	Default : 0x00	Access : R/W

OSD Register (Bank = 1C)

Index (Absolute)	Mnemonic	Bit	Description	
(1C60h)	OBC_DTATA[7:0]	7:0	OSD clear function data.	
30h (1C61h)	**REG1C61**	**7:0**	**Default : 0x00**	**Access : R/W**
	OBC_DTATA[15:8]	7:0	Please see description of '1C60h'.	
31h (1C62h)	**REG1C62**	**7:0**	**Default : 0x00**	**Access : R/W, DB**
	OBC_ADR[7:0]	7:0	OSD clear function start address.	
31h (1C63h)	**REG1C63**	**7:0**	**Default : 0x00**	**Access : R/W, DB**
	OBC_ATR1_EN	7	OSD clear attribute1 enable.	
	OBC_ATR0_EN	6	OSD clear attribute0 enable.	
	OBC_CODE_EN	5	OSD clear code enable.	
	-	4	Reserved.	
	OBC_ADR[11:8]	3:0	Please see description of '1C62h'.	
32h (1C64h)	**REG1C64**	**7:0**	**Default : 0x00**	**Access : R/W, DB**
	-	7	Reserved.	
	OBC_WIDTH	6:0	OSD clear function width.	
32h (1C65h)	**REG1C65**	**7:0**	**Default : 0x00**	**Access : R/W, DB**
	-	7:6	Reserved.	
	HWCSR_OFS[5:0]	5:0	Hardware cursor color palette high byte.	
33h (1C66h)	**OSPHW_LSB**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSPH2[1:0]	7:6	See description for OSPH2.	
	OSPW2[1:0]	5:4	See description for OSPW2.	
	OSPH[1:0]	3:2	See description for OSPH.	
	OSPW[1:0]	1:0	See description for OSPW.	
33h (1C67h)	**REG1C67**	**7:0**	**Default : 0x00**	**Access : R/W**
	OBCT	7	OSD clear function trigger. Setting this bit to "1" will trigger H/W to clear OSD block during VSYNC display period. H/W will set this bit back to "0" when OSD block is cleared.	
	OBC_HIGH	6:0	OSD clear function high.	
34h ~ 38h (1C68h ~ 1C70h)	-	7:0	**Default : -**	**Access : -**
	-	7:0	Reserved.	
38h (1C71h)	**REG1C71**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:5	Reserved.	
	TG_BIT	4	Test pattern resolution.	

OSD Register (Bank = 1C)

Index (Absolute)	Mnemonic	Bit	Description	
			0: 8 bits. 1: 10 bits.	
	-	3	Reserved.	
	NOISE_MD	2:0		
39h (1C73h)	REG1C73	7:0	Default : -	Access : -
	-	7:0	Reserved.	
3Ah (1C74h)	REG1C74	7:0	Default : 0x08	Access : R/W
	-	7	Reserved.	
	SDOSD_SEP	6	SOSD H/VSYNC control separate enable.	
	SOSD_FRONT	5	SOSD mix with input data, only active when SDOSD_SEL=1.	
	SOSD_OHS_SEL	4	SOSD HSYNC select when mix with output data (Only active when SDOSD_SEL = 1). 0: HSYNC related signal is selected. 1: HDE related signal is selected.	
	SOSD_IHS_SEL	3	SOSD HSYNC select when mix with input data (only active when SDOSD_SEL = 1). 0: Sample range H related signal is selected. 1: HSYNC related signal is selected.	
	SOSD_IVS_SEL	2	SOSD VSYNC select when mix with input data (only active when SDOSD_SEL = 1). 0: Sample range V related signal is selected. 1: VSYNC related signal is selected.	
	SOSD_IVS_INV	1	SOSD HSYNC invert when mix with input data (only active when SDOSD_SEL = 1). 0: Disable. 1: Enable.	
	SOSD_SUB_SEL	0	SOSD mix with input sub window data (only active when SDOSD_SEL = 1). 0: Mix with input main window data. 1: Mix with input sub window data.	
3Ah (1C75h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
3Bh (1C76h)	REG1C76	7:0	Default : 0x00	Access : R/W
	BLEND_MD	7	OSD blend mode.	
	BLEND_POL	6	OSD blend polarity.	

OSD Register (Bank = 1C)

Index (Absolute)	Mnemonic	Bit	Description	
	BLEND[5:0]	5:0	OSD blend value.	
3Bh (1C77h)	**REG1C77**	**7:0**	**Default : 0x20**	**Access : RO, R/W**
	-	7:2	Reserved.	
	VERT_FLIP_EN	1	OSD vertical flip enable. 0: Disable. 1: Enable. Before setting this bit to "1", firmware needs to set 13h/14h VERT_FLIP code base address.	
	FONT_SHRINK_EN	0	OSD font shrink enable. 0: Disable. 1: Enable.	
3Ch (1C78h)	**REG1C78**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SHRINK_BG_EN	7	Font shrink back ground enable.	
	ATR1_SRC_SEL	6	ATR1 source select. 0: New ATR request. 1: Original ATR request.	
	OBC_LOAD_INV	5	OBC load invert. 1: Means select start trigger invert.	
	OBC_LOAD_SEL[1:0]	4:3	OBC load select. 00: Select start trigger from VS_PLS. 01: Select start trigger from VDE_END_PLS. 10: Select start trigger from IVS. 11: Select start trigger from CPURW_BLOCK_AREA.	
	WP_FIFO_FULL	2	Write FIFO full (for different type writes, firmware needs to check this bit). 0: Not full. 1: Full.	
	WP_FIFO_EMPTY	1	Write FIFO empty (for different type writes, firmware needs to check this bit). 0: Not empty. 1: Empty.	
	-	0	Reserved.	
3Ch (1C79h)	**REG1C79**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:3	Reserved.	
	RP_BW_FAIL	2	OSD read path bandwidth fail.	
	RP_BW_FAIL_CLR	1	Clear OSD read path bandwidth fail signal.	

OSD Register (Bank = 1C)

Index (Absolute)	Mnemonic	Bit	Description	
	OBC_FORCE_START	0	OBC force start. 1: OBC start trigger from S/W OBCT enable.	
40h (1C80h)	REG1C80	7:0	Default : 0x00	Access : R/W
	WP_CODE_BASADR[7:0]	7:0	OSD write path code base-address.	
40h (1C81h)	REG1C81	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	WP_CODE_BASADR[11:8]	3:0	Please see description of '1C80h'.	
41h (1C82h)	REG1C82	7:0	Default : 0x00	Access : R/W
	WP_ATTRI0_BASADR[7:0]	7:0	OSD write path attribute0 base-address.	
41h (1C83h)	REG1C83	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	WP_ATTRI0_BASADR[11:8]	3:0	Please see description of '1C82h'.	
42h (1C84h)	REG1C84	7:0	Default : 0x00	Access : R/W
	WP_ATTRI1_BASADR[7:0]	7:0	OSD write path attribute1 base-address.	
42h (1C85h)	REG1C85	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	WP_ATTRI1_BASADR[11:8]	3:0	Please see description of '1C84h'.	
43h (1C86h)	REG1C86	7:0	Default : 0x00	Access : R/W
	WP_TEX_GRP_BASADR[7:0]	7:0	OSD write path texture group base-address.	
43h (1C87h)	REG1C87	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	WP_TEX_GRP_BASADR[11:8]	3:0	Please see description of '1C86h'.	
44h (1C88h)	REG1C88	7:0	Default : 0x00	Access : R/W
	WP_FONT1BP_BASADR[7:0]	7:0	OSD write path 1bp font base-address.	
44h (1C89h)	REG1C89	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	WP_FONT1BP_BASADR[11:8]	3:0	Please see description of '1C88h'.	
45h (1C8Ah)	REG1C8A	7:0	Default : 0x00	Access : R/W
	WP_FONT2BP_BASADR[7:0]	7:0	OSD write path 2bp font base-address.	
45h (1C8Bh)	REG1C8B	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	

OSD Register (Bank = 1C)

Index (Absolute)	Mnemonic	Bit	Description	
	WP_FONT2BP_BASADR[11:8]	3:0	Please see description of '1C8Ah'.	
46h (1C8Ch)	REG1C8C	7:0	Default : 0x00	Access : R/W
	WP_FONT4BP_BASADR[7:0]	7:0	OSD write path 4bp font base-address.	
46h (1C8Dh)	REG1C8D	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	WP_FONT4BP_BASADR[11:8]	3:0	Please see description of '1C8Ch'.	
47h (1C8Eh)	REG1C8E	7:0	Default : 0x00	Access : R/W
	WP_FONT8BP_BASADR[7:0]	7:0	OSD write path 8bp font base-address.	
47h (1C8Fh)	REG1C8F	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	WP_FONT8BP_BASADR[11:8]	3:0	Please see description of '1C8Eh'.	
48h (1C90h)	REG1C90	7:0	Default : 0x00	Access : R/W
	RP_CODE_BASADR[7:0]	7:0	OSD read path code base-address.	
48h (1C91h)	REG1C91	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	RP_CODE_BASADR[11:8]	3:0	Please see description of '1C90h'.	
49h (1C92h)	REG1C92	7:0	Default : 0x00	Access : R/W
	RP_ATTRI0_BASADR[7:0]	7:0	OSD read path attribute0 base-address.	
49h (1C93h)	REG1C93	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	RP_ATTRI0_BASADR[11:8]	3:0	Please see description of '1C92h'.	
4Ah (1C94h)	REG1C94	7:0	Default : 0x00	Access : R/W
	RP_ATTRI1_BASADR[7:0]	7:0	OSD read path attribute1 base-address.	
4Ah (1C95h)	REG1C95	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	RP_ATTRI1_BASADR[11:8]	3:0	Please see description of '1C94h'.	
4Bh (1C96h)	REG1C96	7:0	Default : 0x00	Access : R/W
	RP_TEX_GRP_BASADR[7:0]	7:0	OSD read path texture group base-address.	
4Bh (1C97h)	REG1C97	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	

OSD Register (Bank = 1C)

Index (Absolute)	Mnemonic	Bit	Description	
	RP_TEX_GRP_BASADR[11:8]	3:0	Please see description of '1C96h'.	
4Ch (1C98h)	REG1C98	7:0	Default : 0x00	Access : R/W
	RP_FONT1BP_BASADR[7:0]	7:0	OSD read path 1bp font base-address.	
4Ch (1C99h)	REG1C99	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	RP_FONT1BP_BASADR[11:8]	3:0	Please see description of '1C98h'.	
4Dh (1C9Ah)	REG1C9A	7:0	Default : 0x00	Access : R/W
	RP_FONT2BP_BASADR[7:0]	7:0	OSD read path 2bp font base-address.	
4Dh (1C9Bh)	REG1C9B	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	RP_FONT2BP_BASADR[11:8]	3:0	Please see description of '1C9Ah'.	
4Eh (1C9Ch)	REG1C9C	7:0	Default : 0x00	Access : R/W
	RP_FONT4BP_BASADR[7:0]	7:0	OSD read path 4bp font base-address.	
4Eh (1C9Dh)	REG1C9D	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	RP_FONT4BP_BASADR[11:8]	3:0	Please see description of '1C9Ch'.	
4Fh (1C9Eh)	REG1C9E	7:0	Default : 0x00	Access : R/W
	RP_FONT8BP_BASADR[7:0]	7:0	OSD read path 8bp font base-address.	
4Fh (1C9Fh)	REG1C9F	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	RP_FONT8BP_BASADR[11:8]	3:0	Please see description of '1C9Eh'.	
60h (1CC0h)	REG1CC0	7:0	Default : 0x00	Access : R/W
	TOTAL_TEX_GRP0[7:0]	7:0	OSD texture group 0.	
60h (1CC1h)	REG1CC1	7:0	Default : 0x00	Access : R/W
	TOTAL_TEX_GRP0[15:8]	7:0	Please see description of '1CC0h'.	
61h (1CC2h)	REG1CC2	7:0	Default : 0x00	Access : R/W
	TOTAL_TEX_GRP1[7:0]	7:0	OSD texture group 1.	
61h (1CC3h)	REG1CC3	7:0	Default : 0x00	Access : R/W
	TOTAL_TEX_GRP1[15:8]	7:0	Please see description of '1CC2h'.	
62h (1CC4h)	REG1CC4	7:0	Default : 0x00	Access : R/W
	TOTAL_TEX_GRP2[7:0]	7:0	OSD texture group 2.	
62h (1CC5h)	REG1CC5	7:0	Default : 0x00	Access : R/W
	TOTAL_TEX_GRP2[15:8]	7:0	Please see description of '1CC4h'.	

OSD Register (Bank = 1C)

Index (Absolute)	Mnemonic	Bit	Description	
63h (1CC6h)	REG1CC6	7:0	Default : 0x00	Access : R/W
	TOTAL_TEX_GRP3[7:0]	7:0	OSD texture group 3.	
63h (1CC7h)	REG1CC7	7:0	Default : 0x00	Access : R/W
	TOTAL_TEX_GRP3[15:8]	7:0	Please see description of '1CC6h'.	
64h (1CC8h)	REG1CC8	7:0	Default : 0x00	Access : R/W
	TOTAL_TEX_GRP4[7:0]	7:0	OSD texture group 4.	
64h (1CC9h)	REG1CC9	7:0	Default : 0x00	Access : R/W
	TOTAL_TEX_GRP4[15:8]	7:0	Please see description of '1CC8h'.	
65h (1CCAh)	REG1CCA	7:0	Default : 0x00	Access : R/W
	TOTAL_TEX_GRP5[7:0]	7:0	OSD texture group 5.	
65h (1CCBh)	REG1CCB	7:0	Default : 0x00	Access : R/W
	TOTAL_TEX_GRP5[15:8]	7:0	Please see description of '1CCAh'.	
66h (1CCCh)	REG1CCC	7:0	Default : 0x00	Access : R/W
	TOTAL_TEX_GRP6[7:0]	7:0	OSD texture group 6.	
66h (1CCDh)	REG1CCD	7:0	Default : 0x00	Access : R/W
	TOTAL_TEX_GRP6[15:8]	7:0	Please see description of '1CCCh'.	
67h (1CCEh)	REG1CCE	7:0	Default : 0x00	Access : R/W
	TOTAL_TEX_GRP7[7:0]	7:0	OSD texture group 7.	
67h (1CCFh)	REG1CCF	7:0	Default : 0x00	Access : R/W
	TOTAL_TEX_GRP7[15:8]	7:0	Please see description of '1CCEh'.	
68h (1CD0h)	REG1CD0	7:0	Default : 0x00	Access : R/W
	TOTAL_TEX_GRP8[7:0]	7:0	OSD texture group 8.	
68h (1CD1h)	REG1CD1	7:0	Default : 0x00	Access : R/W
	TOTAL_TEX_GRP8[15:8]	7:0	Please see description of '1CD0h'.	
69h (1CD2h)	REG1CD2	7:0	Default : 0x00	Access : R/W
	TOTAL_TEX_GRP9[7:0]	7:0	OSD texture group 9.	
69h (1CD3h)	REG1CD3	7:0	Default : 0x00	Access : R/W
	TOTAL_TEX_GRP9[15:8]	7:0	Please see description of '1CD2h'.	
6Ah (1CD4h)	REG1CD4	7:0	Default : 0x00	Access : R/W
	TOTAL_TEX_GRP10[7:0]	7:0	OSD texture group 10.	
6Ah (1CD5h)	REG1CD5	7:0	Default : 0x00	Access : R/W
	TOTAL_TEX_GRP10[15:8]	7:0	Please see description of '1CD4h'.	
6Bh	REG1CD6	7:0	Default : 0x00	Access : R/W

OSD Register (Bank = 1C)

Index (Absolute)	Mnemonic	Bit	Description	
(1CD6h)	TOTAL_TEX_GRP11[7:0]	7:0	OSD texture group 11.	
6Bh (1CD7h)	REG1CD7	7:0	Default : 0x00	Access : R/W
	TOTAL_TEX_GRP11[15:8]	7:0	Please see description of '1CD6h'.	
6Ch (1CD8h)	REG1CD8	7:0	Default : 0x00	Access : R/W
	TOTAL_TEX_GRP12[7:0]	7:0	OSD texture group 12.	
6Ch (1CD9h)	REG1CD9	7:0	Default : 0x00	Access : R/W
	TOTAL_TEX_GRP12[15:8]	7:0	Please see description of '1CD8h'.	
6Dh (1CDAh)	REG1CDA	7:0	Default : 0x00	Access : R/W
	TOTAL_TEX_GRP13[7:0]	7:0	OSD texture group 13.	
6Dh (1CDBh)	REG1CDB	7:0	Default : 0x00	Access : R/W
	TOTAL_TEX_GRP13[15:8]	7:0	Please see description of '1CDAh'.	
6Eh (1CDCh)	REG1CDC	7:0	Default : 0x00	Access : R/W
	TOTAL_TEX_GRP14[7:0]	7:0	OSD texture group 14.	
6Eh (1CDDh)	REG1CDD	7:0	Default : 0x00	Access : R/W
	TOTAL_TEX_GRP14[15:8]	7:0	Please see description of '1CDCh'.	
6Fh (1CDEh)	REG1CDE	7:0	Default : 0x00	Access : R/W
	TOTAL_TEX_GRP15[7:0]	7:0	OSD texture group 15.	
6Fh (1CDFh)	REG1CDF	7:0	Default : 0x00	Access : R/W
	TOTAL_TEX_GRP15[15:8]	7:0	Please see description of '1CDEh'.	
70h (1CE0h)	REG1CE0	7:0	Default : 0x00	Access : R/W
	TEX32	7	Texture 32 enable.	
	TEX_EN	6	OSD read path texture and font share the same request.	
	FRAME_START_SEL	5	Select frame start signal source. 0: By HW. 1: By SW.	
	FRAME_START	4	Generate frame start signal by SW.	
	DRAM_BUS	3	DRAM bus width. 0: Means DRAM bus width is 16 bits. 1: No-use.	
	DRAM_4BA	2	DRAM bank bits. 0: Means DRAM has 1 bits banks. 1: Means 2 bits banks.	
	DRAM_9COL	1	DRAM column bits. 0: Means DRAM has 8 bits columns.	

OSD Register (Bank = 1C)

Index (Absolute)	Mnemonic	Bit	Description	
			1: Means 9 bits columns.	
	-	0	Reserved.	
70h (1CE1h)	REG1CE1	7:0	Default : 0x30	Access : R/W
	-	7:6	Reserved.	
	FWRESETZ_RP	5	OSD read path SW reset.	
	FWRESETZ_WP	4	OSD write path SW reset.	
	OSD_SEL[1:0]	3:2	OSD select. 00: OSD port0 select OSD2, OSD port1 select OSD1. 01: OSD port0 select OSD1, OSD port1 select OSD1. 10: OSD port0 select OSD2, OSD port1 select OSD2. 11: OSD port0 select OSD1, OSD port1 select OSD2.	
	OSD_RP_PRI	1	1 means OSD2MI_RRDY has higher priority.	
	-	0	Reserved.	
71h (1CE2h)	REG1CE2	7:0	Default : -	Access : RO
	BIST_FAIL_TEX_SRAM_32X64_1	7	Texture SRAM32x64_1 BIST fail status.	
	BIST_FAIL_TEX_SRAM_32X64_0	6	Texture SRAM32x64_0 BIST fail status.	
	BIST_FAIL_ATRI0_SRAM_24X128_1	5	Attribute0 SRAM24x128_1 BIST fail status.	
	BIST_FAIL_ATRI0_SRAM_24X128_0	4	Attribute0 SRAM24x128_0 BIST fail status.	
	BIST_FAIL_FONT_SRAM_96X128_1	3	Font SRAM96x128_1 BIST fail status.	
	BIST_FAIL_FONT_SRAM_96X128_0	2	Font SRAM96x128_0 BIST fail status.	
	BIST_FAIL_CODE_SRAM_24X64_1	1	Code SRAM24x64_1 BIST fail status.	
	BIST_FAIL_CODE_SRAM_24X64_0	0	Code SRAM24x64_0 BIST fail status.	
71h (1CE3h)	REG1CE3	7:0	Default : -	Access : RO
	-	7:5	Reserved.	
	BIST_FAIL_CPRAM	4	CPRAM BIST fail status.	
	BIST_FAIL_FP_SRAM_96X8_1	3	FP SRAM96x8_1 BIST fail status.	

OSD Register (Bank = 1C)

Index (Absolute)	Mnemonic	Bit	Description	
	BIST_FAIL_FP_SRAM_96X8_0	2	FP SRAM96x8_0 BIST fail status.	
	BIST_FAIL_SC_SRAM_96X16_1	1	SC SRAM96x16_1 BIST fail status.	
	BIST_FAIL_SC_SRAM_96X16_0	0	SC SRAM96x16_0 BIST fail status.	
72h (1CE4h)	REG1CE4	7:0	Default : 0x00	Access : R/W
	OSD1_HWCSR_EN	7	1: Hardware cursor to show on OSD1.	
	OSD2_HWCSR_EN	6	1: Hardware cursor to show on OSD2.	
	BW_IMPROVE	5	1: OSD read path has more bandwidth tolerance.	
	OSD2MI_WPTY	4	1: OSD2MI_WRDY has higher priority.	
	HWCSR_LASTLINE	3	Set as "0" if HWCSR_Y_POS = 0; else, set as "1".	
	-	2:0	Reserved.	
72h (1CE5h)	REG1CE5	7:0	Default : 0x00	Access : R/W
	DUMMY_REG1[15:8]	7:0	Please see description of '1CE4h'.	
73h (1CE6h)	REG1CE6	7:0	Default : 0x00	Access : R/W
	DH_IMPROVE	7	1 means OSD double height has more bandwidth tolerance.	
	-	6:0	Reserved.	
73h (1CE7h)	REG1CE7	7:0	Default : 0x00	Access : R/W
	DUMMY_REG2[15:8]	7:0	Please see description of '1CE6h'.	
78h (1CF0h)	REG1CF0	7:0	Default : 0x00	Access : R/W
	HWCSR_V_DUP	7:6	Vertical size up. 00: x1. 01: x2. 10: x3. 11: x4.	
	HWCSR_H_DUP	5:4	Horizontal size up. 00: x1. 01: x2. 10: x3. 11: x4.	
	HC_PRI	3	1: HC2MI_RRDY to has higher priority.	
	HWCSR_BIT	2	Hardware cursor. 0: 2bp.	

OSD Register (Bank = 1C)

Index (Absolute)	Mnemonic	Bit	Description	
			1: 4bp.	
	HWCSR_SIZE	1	Hardware cursor size. 0: 32x32. 1: 64x64.	
	HWCSR_EN	0	Hardware cursor enable.	
78h (1CF1h)	REG1CF1	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	HWCSR_COLOR_OFST[5:0]	5:0	HWCSR_COLOR_OFFSET, for 2bp case, the 8bp HWCSR is HWCSR_COLOR_OFFSET[5:0], HWCSR_BIT[1:0], for 4bp case, the 8bp HWCSR is HWCSR_COLOR_OFFSET[5:2], HWCSR_BIT[3:0].	
79h (1CF2h)	REG1CF2	7:0	Default : 0x00	Access : R/W
	HWCSR_HST[7:0]	7:0	Hardware cursor horizontal start position.	
79h (1CF3h)	REG1CF3	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	HWCSR_HST[11:8]	3:0	Please see description of '1CF2h'.	
7Ah (1CF4h)	REG1CF4	7:0	Default : 0x00	Access : R/W
	HWCSR_VST[7:0]	7:0	Hardware cursor vertical start position.	
7Ah (1CF5h)	REG1CF5	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	HWCSR_VST[11:8]	3:0	Please see description of '1CF4h'.	
7Bh (1CF6h)	REG1CF6	7:0	Default : 0x00	Access : R/W
	HWCSR_BASADR[7:0]	7:0	The base-address for reading out the hardware cursor.	
7Bh (1CF7h)	REG1CF7	7:0	Default : 0x00	Access : R/W
	HWCSR_BASADR[15:8]	7:0	Please see description of '1CF6h'.	

CHIPTOP Register (Bank = 1E)

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (1E00h)	**REG1E00**	**7:0**	**Default : 0x00**	**Access : R/W**
	CHIP_CONFIG_OVW[7:0]	7:0	Chip config overwrite. [0]: SEL_SBUS_OVEN. [1]: SEL_SBUS_OV. [2]: SEL_DBUS_OVEN. [3]: SEL_DBUS_OV. Others: Reserved.	
00h (1E01h)	**REG1E01**	**7:0**	**Default : 0x00**	**Access : R/W**
	CHIP_CONFIG_OVW[15:8]	7:0	Please see description of '1E00h'.	
01h (1E02h)	**REG1E02**	**7:0**	**Default : 0x00**	**Access : R/W**
	UTMI_MD	7	Force crystal clock gated for test machine.	
	-	6:1	Reserved.	
	FORCE_MODPAD	0	Force all MOD pads controlled by PAD_TOP, mainly for test mode.	
01h (1E03h)	**REG1E03**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBSETL	7	Series bus pads set low.	
	SBSETH	6	Series bus pads set high.	
	SETL	5	Digital pads (other than serial and direct bus pads) set low.	
	SETH	4	Digital pads (other than serial and direct bus pads) set high.	
	-	3	Reserved.	
	UART_RX_EN	2	1: Enable UART0 RX. 0: Disable UART0 RX.	
	-	1	Reserved.	
	DHC_DFT	0	0: Disable. 1: Set DHC in DFT mode.	
02h (1E04h)	**REG1E04**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_OUT_MD[1:0]	7:6	PAD_SAR[3:0] control. [0]: 0: Controlled by PAD_TOP. 1: Controlled by SAR_TOP. [1]: Reserved.	
	OSC_MD[1:0]	5:4	Delay chain mode. 0: Low IR drop.	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
			1: Whole chip. 2: High IR drop. 3: Audio DSP.	
	CARD_MS[1:0]	3:2	Specify some pads for card reader MS mode. 0: Disable. Others: See GPIO table.	
	CARD_SD[1:0]	1:0	Specify some pads for card reader SD mode. 0: Disable. Others: See GPIO table.	
02h (1E05h)	REG1E05	7:0	Default : 0x00	Access : RO, R/W
	-	7:6	Reserved.	
	GP_DDCR_SCL_IN	5	C read-back when DDCR_SCL is used as GPIO.	
	GP_DDCR_SDA_IN	4	C read-back when DDCR_SDA is used as GPIO.	
	GP_DDCR_SCL_OEN	3	OEN control when DDCR_SCL is used as GPIO.	
	GP_DDCR_SDA_OUT	2	I control when DDCR_SCL is used as GPIO.	
	GP_DDCR_SDA_OEN	1	OEN control when DDCR_SDA is used as GPIO.	
	GP_DDCR_SDA_OUT	0	I control when DDCR_SDA is used as GPIO.	
03h (1E06h)	REG1E06	7:0	Default : 0x00	Access : R/W
	HPLUG	7	Force direct bus pads switch to TEST_BUS_OUT for test machine.	
	TCOM	6	0: Disable. 1: Specify GPIOB as TCON function.	
	SPI_PAD[5:0]	5:0	SPI pads control registers. PAD_SPI_CK -> C0: REG_SPI_PAD[0]; PAD_SPI_CK -> C1: REG_SPI_PAD[1]; PAD_SPI_CZ -> C0: REG_SPI_PAD[2]; PAD_SPI_CZ -> C1: REG_SPI_PAD[3]; PAD_SPI_DI -> C0: REG_SPI_PAD[4]; PAD_SPI_DI -> C1: REG_SPI_PAD[5].	
03h (1E07h)	REG1E07	7:0	Default : 0xF0	Access : R/W
	PWM_OEN[3:0]	7:4	Output ENABLE_BAR of PWM pads; initial should be input for capturing CHIP_CONFIG during reset.	
	-	3:2	Reserved.	
	DDCROM_GPIO	1	0: Disable. 1: Specify DDCR_XXX pins as GPIO function.	
	DDCROM_EN	0	0: Disable.	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
			1: Specify DDCR_XXX as DDCROM function.	
04h (1E08h)	REG1E08	7:0	Default : 0x00	Access : R/W
	TEST_OUT_H[1:0]	7:6	Set some pads as testing output function; high byte. 0: Disable. Others: See GPIO table.	
	TEST_OUT_M[1:0]	5:4	Please see description of '1E08h'[7:6]; middle byte.	
	TEST_OUT_L[1:0]	3:2	Please see description of '1E08h'[7:6]; low byte.	
	TEST_IN[1:0]	1:0	Set some pads as testing input function. 0: Disable. Others: See GPIO table.	
04h (1E09h)	REG1E09	7:0	Default : 0x00	Access : R/W
	IIC_MST[3:0]	7:4	Set some pads as I^2C master function 0: Disable. others: see GPIO table	
	-	3:0	Reserved.	
05h (1E0Ah)	REG1E0A	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	BT656_OUT[2:0]	6:4	Set some pads as BT.656 out function. 0: Disable. Others: See GPIO table.	
	BT656_10BIT	3	Set some pads as BT.656[9:8] function (for testing purpose). 0: Disable. 1: LHSYNC -> BT.656[8]. LVSYNC -> BT.656[9].	
	BT656_IN[2:0]	2:0	Set some pads as BT.656[7:0] function. 0: Disable. Others: See GPIO table.	
05h (1E0Bh)	REG1E0B	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	UART1[2:0]	6:4	Set some pads as UART1 function. 0: Disable. Others: See GPIO table.	
	UART0[3:0]	3:0	Set some pads as UART0 function. 0: Disable. Others: See GPIO table.	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
06h (1E0Ch)	REG1E0C	7:0	Default : 0x00	Access : R/W
	I2S_OUT1[3:0]	7:4	Set some pads as I^{2}S out1 function. 0: Disable. Others: See GPIO table.	
	I2S_IN[3:0]	3:0	Set some pads as I^{2}S in function. 0: Disable. Others: see GPIO table.	
06h (1E0Dh)	REG1E0D	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	SB_DAT_OUT_OEN	4		
	I2S_MUTE[3:0]	3:0	Set some pads as I^{2}S mute function. 0: Disable. Others: See GPIO table.	
07h (1E0Eh)	REG1E0E	7:0	Default : 0x00	Access : R/W
	GPIO_A	7	0: Disable. 1: Specify ICLK + DI[7:0] as GPIOA.	
	-	6:4	Reserved.	
	HDMI_CEC[3:0]	3:0	Set some pads as HDMI_CEC function. 0: Disable. Others: See GPIO table.	
07h (1E0Fh)	REG1E0F	7:0	Default : 0x00	Access : R/W
	GPIO_T[1:0]	7:6	0: Disable. 1: Use GPIOT[3:0] as GPIOT.	
	GPIO_R	5	0: Disable. 1: Use GPIOR[10:0] as GPIOR.	
	GPIO_M	4	Direct bus pads set low.	
	GPIO_L	3	0: Disable. 1: Use GPIOL[4:0] as GPIOL.	
	GPIO_H	2	Direct bus pads set high.	
	GPIO_D	1	0: Disable. 1: Use GPIOD[18:0] as GPIOD.	
	GPIO_B	0	0: Disable. 1: Use GPIOB[13:0] as GPIOB.	
08h (1E10h)	REG1E10	7:0	Default : 0x00	Access : R/W
	GPIOA_OUT[7:0]	7:0	I-control when setting ICLK + DI[7:0] as GPIOA.	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
08h (1E11h)	REG1E11	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	GPIOL_OUT[4:0]	5:1	I-control when setting GPIOL[4:0] as GPIOL.	
	GPIOA_OUT[8]	0	Please see description of '1E10h'.	
09h (1E12h)	REG1E12	7:0	Default : 0x00	Access : R/W
	GPIOA_OEN[7:0]	7:0	OEN control when setting ICLK + DI[7:0] as GPIOA.	
09h (1E13h)	REG1E13	7:0	Default : 0x3E	Access : R/W
	-	7:6	Reserved.	
	GPIOL_OEN[4:0]	5:1	OEN control when setting GPIOL[4:0] as GPIOL.	
	GPIOA_OEN[8]	0	Please see description of '1E12h'.	
0Ah (1E14h)	REG1E14	7:0	Default : 0x00	Access : R/W
	GPIOB_OUT[7:0]	7:0	I-control when setting GPIOB[15:0] as GPIOB.	
0Ah (1E15h)	REG1E15	7:0	Default : 0x00	Access : R/W
	GPIOB_OUT[15:8]	7:0	Please see description of '1E14h'.	
0Bh (1E16h)	REG1E16	7:0	Default : 0xFF	Access : R/W
	GPIOB_OEN[7:0]	7:0	OEN control when setting GPIOB[15:0] as GPIOB.	
0Bh (1E17h)	REG1E17	7:0	Default : 0xFF	Access : R/W
	GPIOB_OEN[15:8]	7:0	Please see description of '1E16h'.	
0Ch (1E18h)	REG1E18	7:0	Default : 0x00	Access : R/W
	GPIOD_OUT[7:0]	7:0	I-control when setting GPIOD[18:0] as GPIOD.	
0Ch (1E19h)	REG1E19	7:0	Default : 0x00	Access : R/W
	GPIOD_OUT[15:8]	7:0	Please see description of '1E18h'.	
0Dh (1E1Ah)	REG1E1A	7:0	Default : 0x00	Access : R/W
	GPIOM_OUT[3:0]	7:4	I-control when setting GPIOM[3:0] is GPIOM.	
	-	3	Reserved.	
	GPIOD_OUT[18:16]	2:0	Please see description of '1E18h'.	
0Dh (1E1Bh)	REG1E1B	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	GPIOT_OUT[3:0]	3:0	I-control when setting GPIOT[3:0] as GPIOT.	
0Eh (1E1Ch)	REG1E1C	7:0	Default : 0xFF	Access : R/W
	GPIOD_OEN[7:0]	7:0	OEN control when setting GPIOD[18:0] as GPIOD.	
0Eh (1E1Dh)	REG1E1D	7:0	Default : 0xFF	Access : R/W
	GPIOD_OEN[15:8]	7:0	Please see description of '1E1Ch'.	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
0Fh (1E1Eh)	REG1E1E	7:0	Default : 0xF7	Access : R/W
	GPIOM_OEN[3:0]	7:4	OEN control when setting GPIOM[3:0] is GPIOM.	
	-	3	Reserved.	
	GPIOD_OEN[18:16]	2:0	Please see description of '1E1Ch'.	
0Fh (1E1Fh)	REG1E1F	7:0	Default : 0x0F	Access : R/W
	-	7:4	Reserved.	
	GPIOT_OEN[3:0]	3:0	OEN control when setting GPIOT[3:0] as GPIOT.	
10h (1E20h)	REG1E20	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	MCU_QUICK_RST	2	0: Normal. 1: MCU quick reset.	
	MCU_RESET	1	1: MCU reset by s/w.	
	POFF_RST_EN	0	1: Power off reset enable.	
11h (1E22h)	REG1E22	7:0	Default : 0x00	Access : R/W
	STC0_CW_SEL	7	Select STC0 control word from. 0: Register controlled by House Keeping MCU. 1: Reserved.	
	-	6	Reserved.	
	STC0SYN_RST	5	STC0 synthesizer software reset; active high.	
	USBSYN_RST	4	USB synthesizer software reset; active high.	
	DE_ONLY_F2	3	DE only mode for SC_TOP main window.	
	DE_ONLY_F1	2	DE only mode for SC_TOP PIP window.	
	CLK_VD_SEL	1	Select VD clock from ADC1 or ADC2. 0: Select VD_ADC_CLK. 1: Select ADC_CLK.	
	SW_MCU_CLK	0	MCU clock setting. 1'b0: DFT_LIVE. 1'b1: Select output according to REG_CKG_MCU.	
11h (1E23h)	REG1E23	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	UPDATE_DC0_SYNC_CW	6	Update the controlling words of DC0 synthesizer that is synchronized to STC0.	
	-	5:4	Reserved.	
	UPDATE_DC0_FREERUN_CW	3	Update the controlling words of DC0 free-running	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
			synthesizer.	
	-	2	Reserved.	
	UPDATE_STC0_CW	1	Update controlling word of the synthesizer STC0.	
	-	0	Reserved.	
12h (1E24h)	REG1E24	7:0	Default : 0x01	Access : R/W
	CKG_RIU[3:0]	7:4	[0]: CLK_VD_P select from 8*fsc or vif_43m. 0: from 8*fsc. 1: from vif_43m. [1]: CLK_VIF select from vif_43m or vif_86m for CLK_DAC. 0: From vif_43m. 1: From vif_86m. [2]: SBM_SDA_OEZ select. 0: From SBM_SDA_OUT (open drain mode). 1: From SBM_SDA_OEZ. [3]: DI clock selection (for BT.656 in). 0: From CLK_IDCLK_F2 (main window). 1: From CLK_IDCLK_F1 (sub window).	
	-	3:2	Reserved.	
	CKG_USB30[1:0]	1:0	CLK_USB30 clock setting. [0]: Disable clock. [1]: Invert clock.	
12h (1E25h)	REG1E25	7:0	Default : 0x00	Access : R/W
	CKG_MIU[3:0]	7:4	CLK_MIU clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: 200MHz (MEMPLL out). 01: 170MHz. 10: 216MHz. 11: 100MHz (MEMPLL DIV 2).	
	CKG_DDR[3:0]	3:0	CLK_MIU2 clock setting. [0]: Disable clock. [1]: Invert clock. Selection of test clock out for OSD line buffer. [2]: 0 => Select CLK_FT0LB. 1 => Select CLK_FT1LB. [3]: 0 => Select CLK_CA0LB. 1 => Select CLK_CA1LB.	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
13h (1E26h)	REG1E26	7:0	Default : 0x00	Access : R/W
	CKG_AEON[1:0]	7:6	CLK_OSDLB_P clock source setting. 00: From ODCLK. 01: From idclk1 with gating. 10: From idclk2 with gating. 11: Reserved.	
	CKG_TCK[1:0]	5:4	CLK_TCK clock setting. [0]: Disable clock. [1]: Invert clock.	
	CKG_TS0[3:0]	3:0	CLK_MINI clock setting; [0]: Disable clock. [1]: Invert clock. [2]: Select clock source. 1: From CLK_DFT. 0: From CLK_MINI_BUF. clk_miu2 clock setting [3]: Force from CLK_DFT.	
13h (1E27h)	REG1E27	7:0	Default : 0x01	Access : R/W
	CKG_STC0[3:0]	7:4	CLK_MCP clock setting. [3]: 1 => from CLK_DFT. 0 => from CLK_MCP_P. CLK_USB clock setting. [2]: Select clock source. 1: From CLK_DFT. 0: From CLK_USB_BUF. [1]: Invert clock. [0]: Disable clock.	
	CKG_TSP[3:0]	3:0	CLK_FT0LB, CLK_FT1LB, CLK_CA0LB, CLK_CA1LB clock source setting. [3]: 1=> from CLK_DFT. 0 =>from CLK_XXX_P. CLK_MLOAD clock setting. [2]: Select clock source. 1: From CLK_DFT. 0: From CLK_MLOAD_P. [1]: Invert clock. [0]: Disable clock.	
14h	REG1E28	7:0	Default : 0x00	Access : R/W

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
(1E28h)	CKG_MAD_STC[3:0]	7:4	CLK_CA0LB clock setting. [0]: Disable clock. [1]: Invert clock. CLK_CA1LB clock setting. [2]: Disable clock. [3]: Invert clock.	
	-	3:0	Reserved.	
14h (1E29h)	**REG1E29**	**7:0**	**Default : 0x18**	**Access : R/W**
	CKG_MVD[3:0]	7:4	CLK_MCU_MAIL0/CLK_MCU_MAIL1 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Clock source select. for CLK_MCU_MAIL0 　　00: From CLK_HKMCU_P. 　　01: From CLK_VDMCU_P. for CLK_MCU_MAIL1 　　00: From CLK_VDMCU_P. 　　01: From CLK_HKMCU_P. 10: Reserved. 11: From CLK_DFT.	
	CKG_MVD_BOOT[3:0]	3:0	Reserved.	
15h (1E2Ah)	**REG1E2A**	**7:0**	**Default : 0x11**	**Access : R/W**
	CKG_DC0[3:0]	7:4	CLK_FT0LB clock setting. [0]: Disable clock. [1]: Invert clock. CLK_FT1LB clock setting. [2]: Disable clock. [3]: Invert clock.	
	CKG_M4V[3:0]	3:0	CLK_MCP clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 　　00: 200MHz (MEMPLL out). 　　01: 170MHz. 　　10: 123MHz. 　　11: 100MHz (MEMPLL div 2).	
15h (1E2Bh)	**REG1E2B**	**7:0**	**Default : 0x11**	**Access : R/W**
	CKG_GE[3:0]	7:4	CLK_OSD2 clock setting.	

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			[0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 　　　00: IDCLK. 　　　01: ODCLK1 with gating. 　　　10: ODCLK2 with gating. 　　　11: CLK_DFT.	
	CKG_DHC_SBM[3:0]	3:0	CLK_DHC_SBM clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 　　　00: 12MHz. 　　　01: 36MHz. 　　　10: 62MHz. 　　　11: Select XTAL.	
16h (1E2Ch)	REG1E2C	7:0	Default : 0x11	Access : R/W
	CKG_GOPG1[3:0]	7:4	CLK_CA0LB2 clock setting. [0]: Disable clock. [1]: Invert clock. CLK_CA1LB2 clock setting. [2]: Disable clock. [3]: Invert clock.	
	CKG_GOPG0[3:0]	3:0	CLK_FT0LB2 clock setting. [0]: Disable clock. [1]: Invert clock. CLK_FT1LB2 clock setting. [2]: Disable clock. [3]: Invert clock.	
16h (1E2Dh)	REG1E2D	7:0	Default : 0x11	Access : R/W
	CKG_VD[3:0]	7:4	CLK_VD clock setting. [0]: Disable clock. [1]: Invert clock. [3:2] 00: CLK_VD_P. 　　　01: CLK_VIF_43M. 　　　10: Test CLK IN. 　　　11: CLK_DFT.	
	CKG_GOPD[3:0]	3:0	CLK_MIU clock setting. [3]: 1 => From CLK_DFT. 　　0 => From CLK_MIU_P.	

CHIPTOP Register (Bank = 1E)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
			CLK_FT0LB2, CLK_FT1LB2, CLK_CA0LB2, CLK_CA1LB2 clock source setting. [2]: 1 => From CLK_DFT. 0 => From CLK_XXX_P. CLK_OSDLB2_P clock source. [1:0] 00: From ODCLK. 01: From IDCLK1 with gating. 10: From IDCLK2 with gating. 11: Reserved.
17h (1E2Eh)	REG1E2E	7:0	Default : 0x11 · Access : R/W
	CKG_VD200[3:0]	7:4	CLK_VD200 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: 216MHz. 01: 216MHz. 10: 216MHz. 11: Select XTAL.
	CKG_VDMCU[3:0]	3:0	Reserved.
17h (1E2Fh)	REG1E2F	7:0	Default : 0x09 · Access : R/W
	-	7:6	Reserved.
	CKG_DHC[5:0]	5:0	CLK_DHC clock setting. [0]: Disable clock. [1]: Invert clock. [5:2]: Select clock source. 0000: 12MHz. 0001: 54MHz. 0010: 62MHz. 0011: 72MHz. 0100: 86MHz. 0101: 108MHz. 0110: 0. 0111: 0. 1xxx: XTAL.
18h (1E30h)	REG1E30	7:0	Default : 0x10 · Access : R/W
	CKG_FICLK_F2[3:0]	7:4	CLK_FICKL_F2 clock setting. [0]: Disable clock. [1]: Invert clock.

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
			[3:2]: Select clock source. 2b'00: Select CLK_IDCLK2. 01: Select CLK_FCLK. 10: 0. 11: Select XTAL.	
	CKG_FICLK_F1[3:0]	3:0	CLK_FICKL_F1 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 2b'00: Select CLK_IDCLK1. 01: Select CLK_FCLK. 10: 0. 11: Select XTAL.	
18h (1E31h)	REG1E31	7:0	Default : 0x10	Access : R/W
	CKG_PCM[3:0]	7:4	CLK_PCM clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: 27MHz. 01: 27MHz. 10: XTAL. 11: XTAL.	
	-	3:0	Reserved.	
19h (1E32h)	REG1E32	7:0	Default : 0x00	Access : R/W
	CKG_PCI[3:0]	7:4		
	CKG_PCIH[3:0]	3:0		
19h (1E33h)	REG1E33	7:0	Default : 0x11	Access : R/W
	CKG_VEDAC[3:0]	7:4	CLK_VIF_43M clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: Select 43MHz. 01: Select 43MHz. 10: Select 43MHz. 11: Select XTAL.	
	CKG_VE[3:0]	3:0	CLK_VIF_86M clock setting. [0]: Disable clock. [1]: Invert clock.	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
			[3:2]: Select clock source. 00: Select 86MHz. 01: Select 86MHz. 10: Select 86MHz. 11: Select XTAL.	
1Ah (1E34h)	REG1E34	7:0	Default : 0x01	Access : R/W
	CKG_SDR[3:0]	7:4	Reserved.	
	CKG_DAC[3:0]	3:0	CLK_DAC clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: Select ODCLK. 01: Select CLK_VIF. 10: Select CLK_VD. 11: Select XTAL.	
1Ah (1E35h)	REG1E35	7:0	Default : 0x01	Access : R/W
	-	7:6	Reserved.	
	CKG_FCLK[5:0]	5:0	CLK_FCLK clock setting. [0]: Disable clock. [1]: Invert clock. [5:2]: Select clock source. 0000: Select FIX_CLK from MPLL. 0001: Select CLK_MIU. 0010: Select CLK_ODCLK. 0011: Select 216MHz. 0100: Select CLK_IDCLK2. 0101: Select 200MHz. 0110: 0. 0111: Select XTAL. 1xxx: Select XTAL.	
1Bh (1E36h)	REG1E36	7:0	Default : 0x01	Access : R/W
	-	7:6	Reserved.	
	CKG_FMCLK[5:0]	5:0	CLK_FMCLK clock setting. [0]: Disable clock. [1]: Invert clock. [5:2]: Select clock source. 0000: Select CLK_MIU. 0001: Select FIX_CLK from MPLL.	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
			0010: Select CLK_ODCLK.	
			0011: 0.	
			0100: Select CLK_IDCLK2.	
			0101: 0.	
			0110: 0.	
			0111: 0.	
			1xxx: Select DFT_LIVE.	
1Bh (1E37h)	REG1E37	7:0	Default : 0x20	Access : R/W
	-	7:6	Reserved.	
	CKG_ODCLK[5:0]	5:0	CLK_ODCLK clock setting. [0]: Disable clock. [1]: Invert clock. [5:2]: Select clock source. 0000: Select CLK_ADC. 0001: Select CLK_DVI. 0010: Select CLK_VD. 0011: 1. 0100: 1. 0101: Select external DI clock. 0110: Selelct CLK_VD_ADC. 0111: Select CLK_LPLL_BUF. 1xxxx: Select XTAL.	
1Ch (1E38h)	REG1E38	7:0	Default : 0x0D	Access : R/W
	-	7:6	Reserved.	
	CKG_VE_IN[5:0]	5:0	CLK_VDMCU clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: Select clock source. 000: Select CLK_MPLL_DIV. 001: Select 160MHz. 010: Select 144MHz. 011: Select 123MHz. 100: Select 108MHz. 101: MEMPLL_CLK_BUF. 110: MEMPLL_CLK_BUF_DIV2. 111: Select 86MHz. [5]: Reserved.	
1Ch	REG1E39	7:0	Default : 0x01	Access : R/W

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1E39h)	-	7	Reserved.	

	CKG_FCIE[6:0]	6:0	CLK_FCIE clock setting.
			[0]: Disable clock.
			[1]: Invert clock.
			[6:2]: Select clock source.
			        5'b00000: CLK86_DIV256.
			        5'b00001: CLK86_DIV64.
			        5'b00010: CLK86_DIV16.
			        5'b00011: CLK54_DIV4.
			        5'b00100: CLK72_DIV4.
			        5'b00101: CLK86_DIV4.
			        5'b00110: CLK54_DIV2.
			        5'b00111: CLK72_DIV2.
			        5'b01000: CLK86_DIV2.
			        5'b01001: 54MHz.
			        5'b01010: 72MHz.
			        5'b01011: 0.
			        5'b01100: 0.
			        5'b01101: 0.
			        5'b01110: 0.
			        5'b01111: 0.
			        5'b1xxxx: Select XTAL.	

1Dh (1E3Ah)	REG1E3A	7:0	Default : 0x11	Access : R/W
	CKG_TSOUT[3:0]	7:4		
	CKG_TS2[3:0]	3:0		
1Fh (1E3Eh)	REG1E3E	7:0	Default : 0x20	Access : R/W
	-	7:6	Reserved.	

	CKG_IDCLK1[5:0]	5:0	CLK_IDCLK_F1 clock setting.
			[0]: Disable clock.
			[1]: Invert clock.
			[5:2]: Select clock source.
			        0000: Select CLK_ADC.
			        0001: Select CLK_DVI.
			        0010: Select CLK_VD.
			        0011: Select CLK_ODCLK.
			        0100: 1.
			        0101: Select external DI clock.
			        0110: Select CLK_VD_ADC.
			        0111: 0.	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
			1xxx: Select XTAL.	
1Fh (1E3Fh)	REG1E3F	7:0	Default : 0x21	Access : R/W
	-	7:6	Reserved.	

	CKG_IDCLK2[5:0]	5:0	CLK_IDCLK_F2 clock setting.
			[0]: Disable clock.
			[1]: Invert clock.
			[5:2]: Select clock source.
			       0000: Select CLK_ADC.
			       0001: Select CLK_DVI.
			       0010: Select CLK_VD.
			       0011: Select CLK_ODCLK.
			       0100: 1.
			       0101: Select external DI clock
			       0110: Select CLK_VD_ADC.
			       0111: 0.
			       1xxx: Select XTAL.	

20h (1E40h)	REG1E40	7:0	Default : 0x00	Access : R/W
	DC0_NUM[7:0]	7:0	Numerator of the synthesizer of DC0.	
20h (1E41h)	REG1E41	7:0	Default : 0x00	Access : R/W
	DC0_NUM[15:8]	7:0	Please see description of '1E40h'.	
21h (1E42h)	REG1E42	7:0	Default : 0x00	Access : R/W
	DC0_DEN[7:0]	7:0	Denominator of the synthesizer of DC0.	
21h (1E43h)	REG1E43	7:0	Default : 0x00	Access : R/W
	DC0_DEN[15:8]	7:0	Please see description of '1E42h'.	
22h (1E44h)	REG1E44	7:0	Default : 0x01	Access : R/W
	-	7:4	Reserved.	

	CKG_STRLD[3:0]	3:0	CLK_OSD clock setting.
			[0]: Disable clock.
			[1]: Invert clock.
			[3:2]: Select clock source.
			       00: IDCLK.
			       01: ODCLK1 with gating.
			       10: ODCLK2 with gating.
			       11: CLK_DFT.	

22h (1E45h)	REG1E45	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
	CKG_MCU[4:0]	4:0	CLK_MCU clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: 000: 170MHz. 001: 160HMz. 010: 144MHz. 011: 123MHz. 100: 108MHz. 101: MEM_CLOCK. 110: MEM_CLOCK div 2. 111: XTAL div 128.	
24h (1E48h)	REG1E48	7:0	Default : 0x00	Access : R/W
	USBSYN_CW[7:0]	7:0	Control word of the synthesizer for USB PHY.	
24h (1E49h)	REG1E49	7:0	Default : 0x00	Access : R/W
	USBSYN_CW[15:8]	7:0	Please see description of '1E48h'.	
25h (1E4Ah)	REG1E4A	7:0	Default : 0x00	Access : R/W
	USBSYN_CW[23:16]	7:0	Please see description of '1E48h'.	
25h (1E4Bh)	REG1E4B	7:0	Default : 0x00	Access : R/W
	USBSYN_CW[31:24]	7:0	Please see description of '1E48h'.	
26h (1E4Ch)	REG1E4C	7:0	Default : 0x00	Access : R/W
	STC0SYN_CW[7:0]	7:0	Control word of the synthesizer of STC0 clocks.	
26h (1E4Dh)	REG1E4D	7:0	Default : 0x00	Access : R/W
	STC0SYN_CW[15:8]	7:0	Please see description of '1E4Ch'.	
27h (1E4Eh)	REG1E4E	7:0	Default : 0x00	Access : R/W
	STC0SYN_CW[23:16]	7:0	Please see description of '1E4Ch'.	
27h (1E4Fh)	REG1E4F	7:0	Default : 0x00	Access : R/W
	STC0SYN_CW[31:24]	7:0	Please see description of '1E4Ch'.	
2Ah (1E54h)	REG1E54	7:0	Default : 0x00	Access : R/W
	DC0_FREERUN_CW[7:0]	7:0	Control word of the synthesizer of MPEG VOP0 clocks.	
2Ah (1E55h)	REG1E55	7:0	Default : 0x00	Access : R/W
	DC0_FREERUN_CW[15:8]	7:0	Please see description of '1E54h'.	
2Bh (1E56h)	REG1E56	7:0	Default : 0x00	Access : R/W
	DC0_FREERUN_CW[23:16]	7:0	Please see description of '1E54h'.	
2Bh	REG1E57	7:0	Default : 0x00	Access : R/W

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
(1E57h)	DC0_FREERUN_CW[31:24]	7:0	Please see description of '1E54h'.	
2Ch (1E58h)	REG1E58	7:0	Default : 0x05	Access : R/W
	-	7:6	Reserved.	
	CKG_DHC_SYNTH[3:0]	5:2	CKG_DHC_SYNTH clock setting. [0]: Gating. [1]: Inverse. [3:2] = 2_b00: MPLL_VCO_DIV2. [3:2] = 2_b01: MPLL_VCO_DIV2P5. [3:2] = 2_b10: MPLL_VCO_DIV3. [3:2] = 2_b11: MPLL_VCO_DIV4.	
	CKG_DHC_DDR[1:0]	1:0	CKG_DHC_DDR clock setting. [0]: Gating. [1]: Inverse.	
2Ch (1E59h)	REG1E59	7:0	Default : 0x21	Access : R/W
	CKG_DHC_LIVE[1:0]	7:6	CKG_DHC_LIVE clock setting. [0]: Gating. [1]: Inverse.	
	CKG_DHC_MCU[5:0]	5:0	CKG_DHC_MCU clock setting. [0]: Gating. [1]: Inverse. [5:2] = 4_b1xxx: XTALI. [5:2] = 4_b0000: 43. [5:2] = 4_b0001: 54. [5:2] = 4_b0010: 62. [5:2] = 4_b0011: 72. [5:2] = 4_b0100: 86. [5:2] = 4_b0101: 108. [5:2] = Others: Reserved.	
33h ~ 35h (1E66h ~ 1E6Ah)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
36h (1E6Ch)	REG1E6C	7:0	Default : -	Access : RO
	TSO_GPIO_IN[7:0]	7:0	Read-back when the following pads are used as GPIO. [3:0]: PAD_AD[3:0]_C. [4]: PAD_WRZ_C. [5]: PAD_RDZ_C. [6]: PAD_ALE_C. [10:7]: Reserved.	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
36h (1E6Dh)	REG1E6D	7:0	Default : -	Access : RO
	-	7:3	Reserved.	
	TSO_GPIO_IN[10:8]	2:0	Please see description of '1E6Ch'.	
37h (1E6Eh)	REG1E6E	7:0	Default : 0x00	Access : R/W
	TSO_GPIO_OUT[7:0]	7:0	[6:0]: OEN control when the following pads are used as GPIO. [3:0]: PAD_AD[3:0]_OEN. [4]: PAD_WRZ_OEN. [5]: PAD_RDZ_OEN. [6]: PAD_ALE_OEN. [10:7]: Reserved.	
37h (1E6Fh)	REG1E6F	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	TSO_GPIO_OUT[10:8]	2:0	Please see description of '1E6Eh'.	
38h (1E70h)	REG1E70	7:0	Default : 0x00	Access : R/W
	TSO_GPIO_OEN[7:0]	7:0	PAD_GPIOD[1:0] control [0]: PAD_GPIOD0 drive. [1]: PAD_GPIOD0 pull down. [2]: PAD_GPIOD0 pull high. [3]: PAD_GPIOD0 pull high PCI. [4]: PAD_GPIOD1 drive. [5]: PAD_GPIOD1 pull down. [6]: PAD_GPIOD1 pull high. [7]: PAD_GPIOD1 pull high PCI.	
38h (1E71h)	REG1E71	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	TSO_GPIO_OEN[10:8]	2:0	Please see description of '1E70h'.	
39h (1E72h)	REG1E72	7:0	Default : -	Access : RO
	-	7:4	Reserved.	
	TS1_GPIO_IN[3:0]	3:0	[0]: PAD_INT_C read-back when PAD_INT is used as GPIO. [3:1]: reserved	
3Ah (1E74h)	REG1E74	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	TS1_GPIO_OUT[3:0]	3:0	[0]: OEN control when PAD_INT is GPIO. [1]: I control when PAD_INT is GPIO.	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
			[3:2]: Reserved.	
3Bh (1E76h)	REG1E76	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	TS1_GPIO_OEN[3:0]	3:0	PAD_GPIOD2 control. [0]: PAD_GPIOD2 drive. [1]: PAD_GPIOD2 pull down. [2]: PAD_GPIOD2 pull high. [3]: PAD_GPIOD2 pull high PCI.	
3Ch (1E78h)	REG1E78	7:0	Default : -	Access : RO
	DI_GPIO_IN[7:0]	7:0	Reserved.	
3Ch (1E79h)	REG1E79	7:0	Default : -	Access : RO
	-	7:1	Reserved.	
	DI_GPIO_IN[8]	0	Please see description of '1E78h'.	
3Dh (1E7Ah)	REG1E7A	7:0	Default : 0x00	Access : R/W
	DI_GPIO_OUT[7:0]	7:0	[6:0]: I control when the following pads are used as GPIO. [3:0]: PAD_AD[3:0]_I. [4]: PAD_WRZ_I. [5]: PAD_RDZ_I. [6]: PAD_ALE_I. [8:7]: Reserved.	
3Dh (1E7Bh)	REG1E7B	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	DI_GPIO_OUT[8]	0	Please see description of '1E7Ah'.	
3Eh (1E7Ch)	REG1E7C	7:0	Default : 0x00	Access : R/W
	DI_GPIO_OEN[7:0]	7:0	PAD_GPIOD[4:3] control. [0]: PAD_GPIOD3 drive. [1]: PAD_GPIOD3 pull down. [2]: PAD_GPIOD3 pull high. [3]: PAD_GPIOD3 pull high PCI. [4]: PAD_GPIOD4 drive. [5]: PAD_GPIOD4 pull down. [6]: PAD_GPIOD4 pull high. [7]: PAD_GPIOD4 pull high PCI. [8]: Reserved.	
3Eh (1E7Dh)	REG1E7D	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
	DI_GPIO_OEN[8]	0	Please see description of '1E7Ch'.	
3Fh (1E7Eh)	REG1E7E	7:0	Default : -	Access : RO
	I2S_GPIO_IN[7:0]	7:0	[3:0]: PAD_SAR[3:0]_C read-back when PAD_SAR[3:0] is GPIO. [7:4]: Reserved.	
3Fh (1E7Fh)	REG1E7F	7:0	Default : -	Access : RO
	-	7:1	Reserved.	
	I2S_GPIO_IN[8]	0	Please see description of '1E7Eh'.	
40h (1E80h)	REG1E80	7:0	Default : 0x00	Access : R/W
	I2S_GPIO_OUT[7:0]	7:0	[3:0]: OEN control when PAD_SAR[3:0] is GPIO. [7:4]: I-control when PAD_SAR[3:0] is GPIO. [8]: PAD_INT is GPIO.	
40h (1E81h)	REG1E81	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	I2S_GPIO_OUT[8]	0	Please see description of '1E80h'.	
41h (1E82h)	REG1E82	7:0	Default : 0x00	Access : R/W
	I2S_GPIO_OEN[7:0]	7:0	PAD_GPIOD[6:5] control [0]: PAD_GPIOD5 drive. [1]: PAD_GPIOD5 pull down. [2]: PAD_GPIOD5 pull high. [3]: PAD_GPIOD5 pull high PCI. [4]: PAD_GPIOD6 drive. [5]: PAD_GPIOD6 pull down. [6]: PAD_GPIOD6 pull high. [7]: PAD_GPIOD6 pull high PCI. [8]: Reserved.	
41h (1E83h)	REG1E83	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	I2S_GPIO_OEN[8]	0	Please see description of '1E82h'.	
42h (1E84h)	REG1E84	7:0	Default : -	Access : RO
	PCI_GPIO_IN[7:0]	7:0	[3:0] PAD_PWM[3:0]_C read-back when PAD_PWM is GPIO [8]: PAD_LCK_C read-back when PAD_LCK (GPIOE[3]) is GPIO. [9]: PAD_LHSYNC_C read-back when PAD_LHSYNC (GPIOE[1]) is GPIO.	

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			[10]: PAD_LVSYNC_C Read-back when PAD_LVSYNC (GPIOE[0]) is GPIO. [11]: PAD_LDE_C read back when PAD_LDE (GPIOE[2]) is GPIO. Others: Reserved	
42h (1E85h)	REG1E85	7:0	Default : -	Access : RO
	PCI_GPIO_IN[15:8]	7:0	Please see description of '1E84h'.	
43h (1E86h)	REG1E86	7:0	Default : -	Access : RO
	PCI_GPIO_IN[23:16]	7:0	Please see description of '1E84h'.	
43h (1E87h)	REG1E87	7:0	Default : -	Access : RO
	PCI_GPIO_IN[31:24]	7:0	Please see description of '1E84h'.	
44h (1E88h)	REG1E88	7:0	Default : -	Access : RO
	-	7:2	Reserved.	
	PCI_GPIO_IN[33:32]	1:0	Please see description of '1E84h'.	
45h (1E8Ah)	REG1E8A	7:0	Default : 0x00	Access : R/W
	PCI_GPIO_OUT[7:0]	7:0	[3:0]: OEN control when PAD_PWM[3:0] is GPIO. [7:4]: I control when PAD_PWM[3:0] is GPIO. [10:8]: OEN control when PAD_LVSYNC (GPIOE[0]), PAD_LHSYNC (GPIOE[1]), PAD_LCK (GPIOE[3]) is GPIO. [11]: OEN control when PAD_LDE (GPIOE[2]) is GPIO. [14:12]: I control when PAD_LVSYNC(GPIOE[0]), PAD_LHSYNC (GPIOE[1]), PAD_LCK (GPIOE[3]) is GPIO. Others: Reserved.	
45h (1E8Bh)	REG1E8B	7:0	Default : 0x00	Access : R/W
	PCI_GPIO_OUT[15:8]	7:0	Please see description of '1E8Ah'.	
46h (1E8Ch)	REG1E8C	7:0	Default : 0x00	Access : R/W
	PCI_GPIO_OUT[23:16]	7:0	Please see description of '1E8Ah'.	
46h (1E8Dh)	REG1E8D	7:0	Default : 0x00	Access : R/W
	PCI_GPIO_OUT[31:24]	7:0	Please see description of '1E8Ah'.	
47h (1E8Eh)	REG1E8E	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	PCI_GPIO_OUT[33:32]	1:0	Please see description of '1E8Ah'.	
48h (1E90h)	REG1E90	7:0	Default : 0x00	Access : R/W
	PCI_GPIO_OEN[7:0]	7:0	PAD_GPIOD7 control. [0]: PAD_GPIOD7 drive.	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
			[1]: PAD_GPIOD7 pull down.	
			[2]: PAD_GPIOD7 pull high.	
			[3]: PAD_GPIOD7 pull high PCI.	
			PAD_AD0 control.	
			[4]: PAD_AD0 drive.	
			[5]: PAD_AD0 pull down.	
			[6]: PAD_AD0 pull high.	
			[7]: PAD_AD0 pull high PCI.	
			PAD_AD1 control.	
			[8]: PAD_AD1 drive.	
			[9]: PAD_AD1 pull down.	
			[10]: PAD_AD1 pull high.	
			[11]: PAD_AD1 pull high PCI.	
			PAD_AD2 control.	
			[12]: PAD_AD2 drive.	
			[13]: PAD_AD2 pull down.	
			[14]: PAD_AD2 pull high.	
			[15]: PAD_AD2 pull high PCI.	
			[33:16]: Reserved.	
48h (1E91h)	REG1E91	7:0	Default : 0x00	Access : R/W
	PCI_GPIO_OEN[15:8]	7:0	Please see description of '1E90h'.	
49h (1E92h)	REG1E92	7:0	Default : 0x00	Access : R/W
	PCI_GPIO_OEN[23:16]	7:0	Please see description of '1E90h'.	
49h (1E93h)	REG1E93	7:0	Default : 0xFC	Access : R/W
	PCI_GPIO_OEN[31:24]	7:0	Please see description of '1E90h'.	
4Ah (1E94h)	REG1E94	7:0	Default : 0x03	Access : R/W
	-	7:2	Reserved.	
	PCI_GPIO_OEN[33:32]	1:0	Please see description of '1E90h'.	
4Bh (1E96h)	REG1E96	7:0	Default : 0x00	Access : RO, R/W
	TCON_GPIO_OUT[3:0]	7:4	Reserved.	
	TCON_GPIO_IN[3:0]	3:0	[0]: Read-back status of INT_PWR is no good. others: reserved	
4Bh (1E97h)	REG1E97	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	TCON_GPIO_OEN[3:0]	3:0		
50h	REG1EA0	7:0	Default : 0x00	Access : R/W

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
(1EA0h)	I2S_OUT2[3:0]	7:4	Selection of specify the following pads as I2S out2 function 0: Disable. Others: See GPIO table.	
	SPDIF[3:0]	3:0	Selection of specify the following pads as SPDIF function 0: Disable. Others: See GPIO table.	
50h (1EA1h)	REG1EA1	7:0	Default : 0x00	Access : R/W
	USB2_DRVVBUS[3:0]	7:4	Selection of specify the following pads as USB2.0 DRVVBUS function. 0: Disable. Others: See GPIO table.	
	USB1_DRVVBUS[3:0]	3:0	Selection of specify the following pads as USB1.1 DRVVBUS function. 0: Disable. Others: See GPIO table.	
53h (1EA6h)	REG1EA6	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	DHC_RESET	2	DHC reset signal, active high.	
	-	1:0	Reserved.	
54h (1EA8h)	REG1EA8	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	DI_CLK_INV	5	DI_CLK invert.	
	SEL_DI_DDR	4	DIN DDR select. 0: Select SDR signals. 1: Select DDR signals.	
	DI_CLK_SEL[3:0]	3:0	DI_CLK delay level selection.	
54h (1EA9h)	REG1EA9	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	DO_CLK_INV	5	DOUT_CLK invert.	
	DOUT_SRC_SEL	4	DOUT DDR select. 0: Select SDR signals. 1: Select DDR signals.	
	DO_CLK_SEL[3:0]	3:0	DOUT_CLK delay level selection.	
55h (1EAAh)	REG1EAA	7:0	Default : 0x20	Access : R/W
	UART_SEL1[2:0]	7:5	UART select1. 000: HK_51 UART0.	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
			001: HK_51 UART1.	
			010: VD_51 UART0.	
			011: VD51.	
			100: MCP_UART0.	
			Others: Reserved.	
	UART_SEL0[2:0]	4:2	UART select0.	
			000: HK_51 UART0.	
			001: HK_51 UART1.	
			010: VD_51 UART0.	
			011: VD_51.	
			100: MCP_UART0.	
			Others: Reserved.	
	-	1:0	Reserved.	
56h (1EACh)	**REG1EAC**	**7:0**	**Default : -**	**Access : RO**
	GPIOA_IN[7:0]	7:0	Read-back of GPIOA_C.	
56h (1EADh)	**REG1EAD**	**7:0**	**Default : -**	**Access : RO**
	-	7:6	Reserved.	
	GPIOL_IN[4:0]	5:1	Read-back of GPIOL_C.	
	GPIOA_IN[8]	0	Please see description of '1EACh'.	
57h (1EAEh)	**REG1EAE**	**7:0**	**Default : -**	**Access : RO**
	GPIOB_IN[7:0]	7:0	Read-back of GPIOB_C.	
57h (1EAFh)	**REG1EAF**	**7:0**	**Default : -**	**Access : RO**
	GPIOB_IN[15:8]	7:0	Please see description of '1EAEh'.	
58h (1EB0h)	**REG1EB0**	**7:0**	**Default : -**	**Access : RO**
	GPIOD_IN[7:0]	7:0	Read-back of GPIOD_C.	
58h (1EB1h)	**REG1EB1**	**7:0**	**Default : -**	**Access : RO**
	GPIOD_IN[15:8]	7:0	Please see description of '1EB0h'.	
59h (1EB2h)	**REG1EB2**	**7:0**	**Default : -**	**Access : RO**
	GPIOM_IN[3:0]	7:4	Read-back of GPIOM_C.	
	-	3	Reserved.	
	GPIOD_IN[18:16]	2:0	Please see description of '1EB0h'.	
59h (1EB3h)	**REG1EB3**	**7:0**	**Default : -**	**Access : RO**
	-	7:4	Reserved.	
	GPIOT_IN[3:0]	3:0	Read-back of GPIOT_C.	
5Ah	**REG1EB4**	**7:0**	**Default : -**	**Access : RO**

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
(1EB4h)	GPIOR_IN[7:0]	7:0	Read-back of GPIOR_C.	
5Ah (1EB5h)	REG1EB5	7:0	Default : -	Access : RO
	-	7:3	Reserved.	
	GPIOR_IN[10:8]	2:0	Please see description of '1EB4h'.	
62h (1EC4h)	REG1EC4	7:0	Default : 0x00	Access : R/W
	VDD2LOW_CTRL[7:0]	7:0	VDD2LOW control. [5:0]: Power off period selection. 0 => pwroff with 2.2us. 1 => pwroff with 4.4us. 2 => pwroff with 9.0us. 3 => pwroff with 17.9us. 4 => pwroff with 39.8us. 5 => pwroff with 71.6us. [6]: Enable power too low reset. [7]: Clear interrupt of "power is no good".	
63h (1EC6h)	REG1EC6	7:0	Default : 0x00	Access : R/W
	BOND_OV_KEY[7:0]	7:0	Set bonding overwrite key.	
63h (1EC7h)	REG1EC7	7:0	Default : 0x00	Access : R/W
	BOND_OV_KEY[15:8]	7:0	Please see description of '1EC6h'.	
65h (1ECAh)	REG1ECA	7:0	Default : -	Access : RO
	-	7:4	Reserved.	
	CHIP_CONFIG_STAT[3:0]	3:0	CHIP_CONFIG status.	
66h (1ECCh)	REG1ECC	7:0	Default : -	Access : RO
	DEVICE_ID[7:0]	7:0	Device ID.	
66h (1ECDh)	REG1ECD	7:0	Default : -	Access : RO
	DEVICE_ID[15:8]	7:0	Please see description of '1ECCh'.	
67h (1ECEh)	REG1ECE	7:0	Default : -	Access : RO
	CHIP_VERSION[7:0]	7:0	Chip version.	
67h (1ECFh)	REG1ECF	7:0	Default : -	Access : RO
	CHIP_REVISION[7:0]	7:0	Chip revision.	
68h (1ED0h)	REG1ED0	7:0	Default : 0x00	Access : R/W
	BOND_OV_EN[7:0]	7:0	Bonding overwrite enable.	
68h (1ED1h)	REG1ED1	7:0	Default : 0x00	Access : R/W
	BOND_OV_EN[15:8]	7:0	Please see description of '1ED0h'.	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
69h (1ED2h)	REG1ED2	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	BOND_OV_EN[16]	0	Please see description of '1ED0h'.	
6Ah (1ED4h)	REG1ED4	7:0	Default : 0x00	Access : R/W
	BOND_OV[7:0]	7:0	Bonding overwrite value.	
6Ah (1ED5h)	REG1ED5	7:0	Default : 0x00	Access : R/W
	BOND_OV[15:8]	7:0	Please see description of '1ED4h'.	
6Bh (1ED6h)	REG1ED6	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	BOND_OV[16]	0	Please see description of '1ED4h'.	
6Ch (1ED8h)	REG1ED8	7:0	Default : -	Access : RO
	STAT_BOND[7:0]	7:0	Bonding status read-back.	
6Ch (1ED9h)	REG1ED9	7:0	Default : -	Access : RO
	STAT_BOND[15:8]	7:0	Please see description of '1ED8h'.	
6Dh (1EDAh)	REG1EDA	7:0	Default : -	Access : RO
	-	7:1	Reserved.	
	STAT_BOND[16]	0	Please see description of '1ED8h'.	
70h (1EE0h)	REG1EE0	7:0	Default : 0x00	Access : R/W
	GPIOR_OUT[7:0]	7:0	I-control when setting GPIOR pins as GPIOR.	
70h (1EE1h)	REG1EE1	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	GPIOR_OUT[10:8]	2:0	Please see description of '1EE0h'.	
71h (1EE2h)	REG1EE2	7:0	Default : 0xFF	Access : R/W
	GPIOR_OEN[7:0]	7:0	OEN control when setting GPIOR as GPIOR.	
71h (1EE3h)	REG1EE3	7:0	Default : 0x07	Access : R/W
	-	7:3	Reserved.	
	GPIOR_OEN[10:8]	2:0	Please see description of '1EE2h'.	
72h (1EE4h)	REG1EE4	7:0	Default : 0x00	Access : R/W
	SPARE_A[7:0]	7:0	[0]: Set PAD_AD0 as GPIO. [1]: Set PAD_AD1 as GPIO. [2]: Set PAD_AD2 as GPIO. [3]: Set PAD_AD3 as GPIO. [4]: Set PAD_WRZ as GPIO. [5]: Set PAD_RDZ as GPIO.	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
			[6]: Set PAD_ALE as GPIO. [7]: Reserved. [11:8]: Set PAD_SAR[3:0] as GPIO. [15:12]: Set PAD_PWM[3:0] as GPIO.	
72h (1EE5h)	REG1EE5	7:0	Default : 0x00	Access : R/W
	SPARE_A[15:8]	7:0	Please see description of '1EE4h'.	
73h (1EE6h)	REG1EE6	7:0	Default : 0x00	Access : R/W
	SPARE_B[7:0]	7:0	[0]: Set PAD_LVSYNC (GPIOE[0]) as GPIO. [1]: Set PAD_LHSYNC (GPIOE[1]) ad GPIO. [2]: Set PAD_LCK (GPIOE[3]) as GPIO. [3]: Set PAD_LDE (GPIOE[2]) as GPIO. Others: Reserved.	
73h (1EE7h)	REG1EE7	7:0	Default : 0x00	Access : R/W
	SPARE_B[15:8]	7:0	Please see description of '1EE6h'.	
74h (1EE8h)	REG1EE8	7:0	Default : 0x00	Access : R/W
	SPARE_C[7:0]	7:0	Spare registers C.	
74h (1EE9h)	REG1EE9	7:0	Default : 0x00	Access : R/W
	SPARE_C[15:8]	7:0	Please see description of '1EE8h'.	
75h (1EEAh)	REG1EEA	7:0	Default : 0x00	Access : R/W
	TEST_RB	7	Setting for the data arrangement on test bus.	
	TEST_GB	6	Setting for the data arrangement on test bus.	
	TEST_RG	5	Setting for the data arrangement on test bus.	
	-	4	Reserved.	
	SWAPTEST12BIT	3	Swap MSB 12bits with LSB 12bits of test bus.	
	CLK_OUT_SEL[2:0]	2:0	Select TEST_CLK_OUT source. 000: TEST_CLK_OUT = TEST_BUS_GB[0]; 001: TEST_CLK_OUT = TEST_BUS_GB[1]; 010: TEST_CLK_OUT = TEST_BUS_GB[2]; 011: TEST_CLK_OUT = TEST_BUS_GB[3]; 100: TEST_CLK_OUT = TEST_BUS_GB[4]; 101: TEST_CLK_OUT = TEST_BUS_GB[5]; 110: TEST_CLK_OUT = TEST_BUS_GB[6]; 111: TEST_CLK_OUT = TEST_BUS_GB[7].	
75h (1EEBh)	REG1EEB	7:0	Default : 0x00	Access : R/W
	ROSC_IN_SEL	7	Select the input source of ring oscillator in CHIP_CONF. 0: Open-loop (input from external digital input).	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description
			1: Close-loop (enable ring oscillator).
	TESTBUS_EN	6	Enable test bus output.
	TESTCLK_MD	5	TESTCLK mode used in TEST_CTRL.
	TEST_BUS24B_SEL[4:0]	4:0	Select TEST_BUS[23:0] source. 5'd1: TEST_BUS = LPLL_TEST_OUT. 5'd2: TEST_BUS = CLK_TEST_OUT[23:0]. 5'd3: TEST_BUS = CLK_TEST_OUT[47:24]. 5'd4: TEST_BUS = ROSC_OUT, CLK_TEST_OUT[70:48]. 5'd5: TEST_BUS = 0. 5'd6: TEST_BUS = 0. 5'd7: TEST_BUS = 0. 5'd8: TEST_BUS = VD_TEST_OUT. 5'd9: TEST_BUS = SAR_TEST_OUT. 5'd10: TEST_BUS = AUDIO_TEST_OUT. 5'd11: TEST_BUS = 0. 5'd12: TEST_BUS = ADCDVI_TEST_OUT. 5'd13: TEST_BUS = SC_TEST_OUT. 5'd14: TEST_BUS = MIU_TEST_OUT. 5'd15: TEST_BUS = MCU_TEST_OUT. 5'd16: TEST_BUS = 0. 5'd17: TEST_BUS = 0. 5'd18: TEST_BUS = FCIE_TEST_OUT. 5'd19: TEST_BUS = UHC_TEST_OUT. 5'd20: TEST_BUS = UTMI_TEST_OUT. 5'd21: TEST_BUS = BIST_TEST_OUT. 5'd22: TEST_BUS = 0. 5'd23: TEST_BUS = 0. 5'd24: TEST_BUS = PIU_TEST_OUT. 5'd25: TEST_BUS = 0. 5'd26: TEST_BUS = 0. 5'd27: TEST_BUS = 0. 5'd28: TEST_BUS = VIF_TEST_OUT. 5'd29: TEST_BUS = DHC_TEST_OUT. 5'd30: TEST_BUS = DIDOMUX_TEST_OUT. Others: TEST_BUS = PIXEL_FUNC[29:22], PIXEL_FUNC[19:12], PIXEL_FUNC[9:2].
76h (1EECh)	REG1EEC	7:0	Default : 0x00 — Access : R/W
	-	7:3	Reserved.

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description

	SINGLE_CLK_OUT_SEL[2:0]	2:0	Select single CLK_OUT.
			001: TEST_BUS[11] = TEST_CLK_OUT_d2.
			      TEST_BUS[10] = TEST_CLK_OUT.
			010: TEST_BUS[11] = TEST_CLK_OUT_d2.
			      TEST_BUS[10] = TEST_CLK_OUT_d4.
			011: TEST_BUS[11] = TEST_CLK_OUT_d2.
			      TEST_BUS[10] = TEST_CLK_OUT_d8.
			100: TEST_BUS[11] = TEST_CLK_OUT_d2.
			      TEST_BUS[10] = TEST_CLK_OUT_d16.
			Others: No TEST_CLK_OUT.

FCIE Register (Bank = 20)

FCIE Register (Bank = 20)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
00h (2000h)	REG2000	7:0	Default : 0x00 — Access : R/W
	SDIO_INT	7	SDIO interrupt event.
	-	6:4	Reserved.
	MS_DATA_END	3	MS/MSPro data transaction complete event.
	SD_DATA_END	2	SD/MMC data transaction complete event.
	SD_CMD_END	1	SD/MMC card command and response transaction complete event.
	MMA_DATA_END	0	MMA data transaction complete event.
01h (2002h)	REG2002	7:0	Default : 0x00 — Access : R/W
	SDIO_INT_EN	7	SDIO_INT interrupt enable. 0: Disable. 1: Enable.
	-	6:4	Reserved.
	MS_DATA_ENDE	3	MS_DATA_END interrupt enable. 0: Disable. 1: Enable.
	SD_DATA_END_EN	2	SD_DATA_END interrupt enable. 0: Disable. 1: Enable.
	SD_CMD_END_EN	1	SD_CMD_END interrupt enable. 0: Disable. 1: Enable.
	MMA_DATA_EN	0	MMA_DATA_END interrupt enable. 0: Disable. 1: Enable.
02h (2004h)	REG2004	7:0	Default : 0x00 — Access : R/W
	-	7:3	Reserved.
	JOB_RW_DIR	2	Specific that this DMA cycle is read or write. 0: Read from card (data written to DRAM). 1: Write to card (data read from DRAM).
	MMA_W_PRIORITY	1	MIU write request priority. 0: Low priority. 1: High priority.
	MMA_R_PRIORITY	0	MIU read request priority. 0: Low priority.

FCIE Register (Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
			1: High priority.	
03h (2006h)	REG2006	7:0	Default : 0x00	Access : R/W
	DMA_ADDR_23_16[7:0]	7:0	Used to represent DMA address[23:16].	
04h (2008h)	REG2008	7:0	Default : 0x00	Access : R/W
	DMA_ADDR_15_0[7:0]	7:0	Used to represent DMA address[15:0].	
04h (2009h)	REG2009	7:0	Default : 0x00	Access : R/W
	DMA_ADDR_15_0[15:8]	7:0	Please see description of '2008h'.	
05h (200Ah)	REG200A	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	SD_PWR_OC_CHG	5	SD card power over current status change.	
	-	4:2	Reserved.	
	MS_STS_CHG	1	MS/MSPro card plug-in or remove status change.	
	SD_STS_CHG	0	SD/MMC Card plug-in or remove status change.	
06h (200Ch)	REG200C	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	SD_PWR_OCDER_EN	5	SD card power over current detection status change interrupt enable. 0: Disable. 1: Enable.	
	-	4:2	Reserved.	
	MS_STS_EN	1	MS/MSPro card status change interrupt enable. 0: Disable. 1: Enable.	
	SD_STS_EN	0	SD Card status change interrupt enable. 0: Disable. 1: Enable.	
07h (200Eh)	REG200E	7:0	Default : -	Access : RO
	-	7:6	Reserved.	
	SD_OCDET_STS	5	SD card power over current detection status.	
	-	4:2	Reserved.	
	MS_DET_N	1	MS/MSPro card detection.	
	SD_DET_N	0	SD/MMC card detection.	
08h (2010h)	REG2010	7:0	Default : 0x05	Access : R/W, WO
	-	7:3	Reserved.	

FCIE Register (Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
	SD_PWR_PAD_OEN	2	SD card power pad control 0: Output. 1: Input.	
	-	1	Reserved.	
	SD_PWR_ON	0	SD/MMC/MS/MSPro/SM/XD card power on signal. 0: Power on. 1: Power off.	
09h (2012h)	REG2012	7:0	Default : 0x00	Access : R/W
	F_SDIO_INT	7	Force SDIO_INT interrupt active, for testing.	
	-	6:4	Reserved.	
	F_MS_DATA_END	3	Force MS_DATA_END interrupt active, for testing.	
	F_SD_DATA_END	2	Force SD_DATA_END interrupt active, for testing.	
	F_SD_CMD_END	1	Force SD_CMD_END interrupt active, for testing.	
	F_MMA_DATA_END	0	Force MMA_DATA_END interrupt active, for testing.	
09h (2013h)	REG2013	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	F_SD_OC_STS_CHG	5	Force SD_OC_STS_CHG interrupt active, for testing.	
	-	4:2	Reserved.	
	F_MS_STS_CHG	1	Force MS_STS_CHG interrupt active, for testing.	
	F_SD_STS_CHG	0	Force SD_STS_CHG interrupt active, for testing.	
0Ah (2014h)	REG2014	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	MS_EN	2	MS card interface enable. 0: Disable. 1: Enable.	
	SD_EN	1	SD/MMC card interface enable. 0: Disable. 1: Enable.	
	MMA_EN	0	MIU DMA enable, job finish auto clear. (Note: Before setting the bit, make sure "JOB_BL_CNT", "MIU_DMA1", "JOB_RW_DIR", and "MIU_DMA0" are updated.)	
0Bh (2016h)	REG2016	7:0	Default : 0x00	Access : R/W
	JOB_BL_CNT[7:0]	7:0	Total block counts for this job (Unit: sector).	
0Ch	REG2018	7:0	Default : 0x00	Access : RO

FCIE Register (Bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2018h)	TR_BK_CNT[7:0]	7:0	Real time number of sectors remained to be transferred.	
0Dh (201Ah)	**REG201A**	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	CIF_RSP[6:0]	6:0	The expected response size (byte count) for SD/MMC card. The expected register read size (byte count) for MS/MSPro card. 'h01 = 1, 'h40 = 64 bytes	
0Eh (201Ch)	**REG201C**	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	CIF_CMD[6:0]	6:0	The command transfer size (byte count) for SD/MMC and MS/MSPro card. 'h01 = 1, 'h40 = 64 bytes.	
0Fh (201Eh)	**REG201E**	7:0	Default : 0x00	Access : R/W
	CARD_WD_CNT[7:0]	7:0	Expect data word count that transferred through CIF FIFO. 0x00 represents 256 words. (CMD6 for SD card, CMD8/14/19 for MMC card)	
10h (2020h)	**REG2020**	7:0	Default : 0x00	Access : R/W
	MMC_BUS_TEST	7	Test MMC bus type through CIF Data FIFO.	
	SD_DATSYNC	6	Synchronize data bus, for SD1.1 specification.	
	SD_DEST	5	SD/MMC data transfer destination 0: Data FIFO. 1: CIF FIFO.	
	SD_CS_EN	4	Set to enable clock auto-stop feature, which will stop CLK between read blocks when Data FIFO is full. 0: Auto-stop is disabled. 1: Auto-stop is enabled.	
	SDDRL	3	Firmware writes "1" to SD interface drive low.	
	SD_DAT_LINE1	2	10: Use DAT7-0 line. 11: Reserved.	
	SD_DAT_LINE0	1	00: Use DAT0 line. 01: Use DAT3-0 line.	
	SD_CLK_EN	0	SD MIF output clock enable.	
10h (2021h)	**REG2021**	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	SDIO_RDWAIT	0	When read block data, and data FIFO busy. Hardware will	

FCIE Register (Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
			drive SD_DAT1 to low to inform card controller that host is busy; high active.	
11h (2022h)	REG2022	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	SD_DTRX_DIR	4	SD/MMC data transfer direction. 0: Read from card. 1: Write to card.	
	SD_DTRX_EN	3	SD/MMC data transmit/receive enable (job finish, auto clear). 0: Disable. 1: Enable.	
	SD_CMD_EN	2	SD/MMC transmit command enable (job finish, auto clear). 0: Disable. 1: Enable.	
	SD_RSP_EN	1	SD/MMC receive command response enable. 0: Disable. 1: Enable.	
	SD_RSPR2_EN	0	SD/MMC receives command response for R2 type.	
11h (2023h)	REG2023	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	SDIO_DET_ON	2	SDIO interrupt detect function switch; high active.	
	SDIO_INT_MOD1	1	SDIO_INT_MOD. 10: Single block read/write interrupt detect. 11: Multi blocks read/write interrupt detect.	
	SDIO_INT_MOD0	0	00: Continuous interrupt detect. 01: CMD12 or IO abort command interrupt detect.	
12h (2024h)	REG2024	7:0	Default : 0x00	Access : RO, R/W
	-	7:6	Reserved.	
	SD_WR_PRO_N	5	Used for SD card write protected.	
	SD_CMDRSP_CERR	4	Received command phase: response CRC error event.	
	SD_CMD_NORSP	3	Transmitted command phase: response timeout event. Time out = 64 clocks, there is no response on CMD line.	
	SD_DAT_STSNEG	2	Transmitted data phase: "CRC status = negative" from SD/MMC card, it's meaning transmission error. Host need to resend data again.	
	SD_DAT_STSERR	1	Transmitted data phase: "CRC status = error" from	

FCIE Register (Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
			SD/MMC card, its meaning flash program error. SD/MMC card has error.	
	SD_DAT_CERR	0	Received data phase CRC error event.	
12h (2025h)	**REG2025**	7:0	Default : -	Access : RO
	SD_DAT[7:0]	7:0	SD DATA Line [7:0].	
13h (2026h)	**REG2026**	7:0	Default : 0x00	Access : R/W
	BS_DLY2_1_0	7:5	MSPro BS line output delay selected.	
	DAT_DLY2_1_0	4:2	MSPro data lines output delay selected.	
	MS_DAT_LINE1	1	2'b01: Use DAT3- 0 line.	
	MS_DAT_LINE0	0	2'b00: Use DAT0 line.	
13h (2027h)	**REG2027**	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	TPC3_2_1_0	3:0	MS/MSPro transfer protocol command register.	
14h (2028h)	**REG2028**	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	MS_DEST	4	Setting with MS_DTRX_EN. 0: Page data (512 bytes) transfer to Data FIFO 1: Page data (512bytes) transfer to CIF FIFO.	
	MS_BURST	3	MS/MSPro burst mode enable. 0: Disable. 1: Enable.	
	MS_BUS_DIR	2	MS/MSPro transfer bus direction 0: Read form card. 1: Write to card. (must set with MS_REGTRX_EN or MS_DTRX_EN).	
	MS_DTRX_EN	1	MS/MSPro data transfer enable. 0: Disable. 1: Enable. (job finish, auto clear)	
	MS_REGTRX_EN	0	MS/MSPro register transfer enable. 0: Disable. 1: Enable. (job finish, auto clear)	
15h (202Ah)	**REG202A**	7:0	Default : 0x00	Access : RO, R/W
	-	7:6	Reserved.	

FCIE Register (Bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MS_CERR	5	MS/MSPro data bus CRC error.	
	MS_TOUT	4	MS/MSPro response handshaking timeout.	
	MS_DAT3	3	MSPro data line 3 status.	
	MS_DAT2	2	MSPro data line 2 status.	
	MS_DAT1	1	MSPro data line 1 status.	
	MS_DAT0	0	MS/MSPro data line 0 status.	
30h (2060h)	REG2060	7:0	Default : 0x00	Access : RO
	-	7:4	Reserved.	
	CIFD_BISTFAIL	3	CIF FIFO_D 512Bytes BIST test fail.	
	CIFC_BISTFAIL	2	CIF FIFO_C 64Bytes BIST test fail.	
	DBFB_BISTFAIL	1	Data FIFO_B 512Bytes BIST test fail.	
	DBFA_BISTFAIL	0	Data FIFO_A 512Bytes BIST test fail.	
30h (2061h)	REG2061	7:0	Default : 0x10	Access : R/W
	-	7:6	Reserved.	
	ENDIAN_SEL	5	Endian select. Low for little endian, and high for big endian.	
	FCIE_SOFT_RST	4	FCIE module software reset; low active; up program.	
	SD_MS_COBUS	3	SD and MS interface share bus, 4 bits mode bus. MS 4 bits data bus share with SD 4 bits bus, and MS_BS share with SD_CMD. High active.	
	DEBUG_MOD2_1_0	2:0	DEBUG_MOD [2:0] definition => 0: N.C. 1: SD. 2: MS serial mode. 3: MS parallel mode. 4: CF mode. 5: SM mode.	

USB Host Register (Bank = 24)

USB Host Register (Bank = 24)					
Index (Absolute)	**Mnemonic**	**Bit**	**Description**		
00h (2400h)	HCCAP	7:0	Default : -		Access : RO
	CAPLENGTH	7:0	Capability register length; this register is used as an offset added to register base to find out the beginning of the operational register space.		
00h (2401h)	-	7:0	Default : -		Access : -
	-	7:0	Reserved.		
01h (2402h)	HCCAP	7:0	Default : -		Access : RO
	HCIVERSION[7:0]	7:0	Host controller interface version number; this register is a two-byte register containing a BCD encoding of the EHCI revision number supported by the host controller.		
01h (2403h)	HCCAP	7:0	Default : -		Access : RO
	HCIVERSION[15:8]	7:0	Please see description of '2402h'.		
02h (2404h)	HCSPARAMS	7:0	Default : -		Access : RO
	-	7:4	Reserved.		
	N_PORTS	3:0	Number of ports; this field specifies the number of physical downstream ports implemented on the host controller.		
02h ~ 03h (2405h ~ 2407h)	-	7:0	Default : -		Access : -
	-	7:0	Reserved.		
04h (2408h)	HCCPARAMS	7:0	Default : -		Access : RO
	-	7:3	Reserved.		
	ASYN_SCH_PARK_CAP	2	Asynchronous schedule park capability. When this bit is set to 1b, system software can specify and use a smaller frame list and configure the host controller via the frame list size field of USBCMD register. This requirement ensures the frame list is always physically contiguous.		
	PROG_FR_LIST_FLAG	1	Programmable frame list flag. When this bit is set to 1b, system software can specify and use a smaller frame list and configure the host controller via frame list size field of USBCMD register. This requirement ensures the frame list is always physically contiguous.		
	-	0	Reserved.		
04h ~ 07h (2409h ~	-	7:0	Default : -		Access : -
	-	7:0	Reserved.		

USB Host Register (Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description	
240Fh)				
08h (2410h)	USBCMD	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	INT_OAAD	6	Interrupt on asynchronous advance doorbell. This bit is used as a doorbell by software to ring the host controller to issue an interrupt at the next advance of asynchronous schedule.	
	ASCH_EN	5	Asynchronous schedule enable. This bit controls whether the host controller skips the processing of asynchronous schedule. 0: Do not process asynchronous schedule. 1: Use the ASYNCLISTADDR register to access the asynchronous schedule.	
	PSCH_EN	4	Periodic schedule enable. This bit controls whether the host controller skips the processing of periodic schedule. 0: Do not process periodic schedule. 1: Use the PERIODICKISTBASE register to access the periodic schedule.	
	FRL_SIZE	3:2	Frame list size. This field specifies the size of the frame list. 00: 1024 elements (4096 bytes; default value). 01: 512 elements (2048 bytes). 10: 256 elements (1024 bytes). 11: Reserved.	
	HC_RESET	1	Host controller reset. This control bit is used by software to reset the host controller.	
	RS	0	Run/Stop; when this bit is set to 1b, the host controller proceeds with the execution of schedule. 0: Stop. 1: Run.	
08h (2411h)	USBCMD	7:0	Default : 0x0b	Access : R/W
	-	7:4	Reserved.	
	ASYN_PK_EN	3	Asynchronous schedule park mode enable. Software uses this register to enable or disable the park mode. When this register is set to '1', the park mode is enabled.	
	-	2	Reserved.	

USB Host Register (Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description	
	ASYN_PK_CNT	1:0	Asynchronous schedule park mode count. This field contains a count for the number of successive transactions that the host controller is allowed to execute from a high-speed queue head on asynchronous schedule.	
09h (2412h)	USBCMD	7:0	Default : 0x08	Access : R/W
	INT_THRC	7:0	Interrupt threshold control. This field is used by system software to select the maximum rate at which the host controller will issue interrupts. The only valid values are described as below: Value Maximum Interrupt Interval for High Speed 00h Reserved. 01h 1 micro-frame. 02h 2 micro-frames. 04h 4 micro-frames. 08h 8 micro-frames (default, equals to 1ms). 10h 16 micro-frames (2 ms). 20h 32 micro-frames (4 ms). 40h 64 micro-frames (8 ms). Note: For full speed, these registers are reserved.	
09h (2413h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
0Ah (2414h)	USBSTS	7:0	Default : 0x00	Access : R/WC
	-	7:6	Reserved.	
	INT_OAA	5	Interrupt on async advance. This status bit indicates the assertion of interrupt on async advance doorbell.	
	H_SYSERR	4	Host system error. The host controller sets this bit to '1' when a serious error occurred during a host system access involving the host controller module.	
	FRL_ROL	3	Frame List Rollover. The host controller sets this bit to '1' when the Frame List Index rolls over from its maximum value to zero.	
	PO_CHG_DET	2	Port Change Detect. The host controller sets this bit to '1' when any port has a change bit transition from '0' to '1'. In addition, this bit is loaded with the OR of all of the PORTSC change bits.	
	USBERR_INT	1	USB Error Interrupt.	

USB Host Register (Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description	
			The host controller sets this bit to '1' when the completion of a USB transaction results in an error condition.	
	USB_INT	0	USB Interrupt. The host controller sets this bit to '1' upon the completion of a USB transaction.	
0Ah (2415h)	**USBSTS**	**7:0**	**Default : 0x10**	**Access : RO**
	ASCH_STS	7	Asynchronous Schedule Status. This bit reports the actual status of Asynchronous Schedule.	
	PSCH_STS	6	Periodic Schedule Status. This bit reports the actual status of Periodic Schedule.	
	RECLAMATION	5	Reclamation. This is a read-only status bit, and is used to detect an empty of Asynchronous Schedule.	
	HCHALTED	4	Host controller halted. This bit is a zero whenever the run/stop bit is set to '1'. The host controller sets this bit to '1' after it has stopped the executing as a result of the Run/Stop bit being set to 0b.	
	-	3:0	Reserved.	
0Bh (2416h ~ 2417h)	-	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
0Ch (2418h)	**USBINTR**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	INT_OAA_EN	5	Interrupt on async advance enable. When this bit is set to '1', and the interrupt on async advance bit in the USBSTS register is set to '1' also, the host controller will issue an interrupt at the next interrupt threshold.	
	H_SYSERR_EN	4	Host system error enable. When this bit is set to '1', and the host system error status bit I the USBSTS register is set to '1' also, the host controller will issue an interrupt.	
	FRL_ROL_EN	3	Frame list rollover enable. When this bit is set to '1', and the frame list rollover bit in the USBSTS register is set to '1' also, the host controller will issue an interrupt.	
	PO_CHG_INT_EN	2	Port change interrupt enable. When this bit is set to '1', and the port change detect bit in the USBSTS register is	

USB Host Register (Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description	
			set to '1' also, the host controller will issue an interrupt.	
	USBERR_INT_EN	1	USB error interrupt enable. When this bit is set to '1', and the USBERRINT bit in the USBSTS register is set to '1' also, the host controller will issue an interrupt at the next interrupt threshold.	
	USB_INT_EN	0	USB interrupt enable. When this bit is set to '1', and the USBINT bit in the USBSTS register is set to '1' also, the host controller will issue an interrupt at the next interrupt threshold.	
0Ch ~ 0Dh (2419h ~ 241Bh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
0Eh (241Ch)	**FRINDEX**	7:0	Default : 0x00	Access : R/W
	FRINDEX[7:0]	7:0	Frame index. This register is used by the host controller to index the frame into the periodic frame list. It updates every 125 microseconds. This register cannot be written unless the host controller is in the halted state.	
0Eh (241Dh)	**FRINDEX**	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	FRINDEX[13:8]	5:0	Please see description of '1Ch'.	
0Fh ~ 12h (241Eh ~ 2424h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
12h (2425h)	**PERIODICLISTBASE**	7:0	Default : 0x00	Access : R/W
	PERI_BASADR[15:12]	7:4	Periodic frame list base address. This register contains the beginning address of the periodic frame list in the system memory. These bits correspond to memory address signals [31:12].	
	-	3:0	Reserved.	
13h (2426h)	**PERIODICLISTBASE**	7:0	Default : 0x00	Access : R/W
	PERI_BASADR[23:16]	7:0	Please see description of '25h'.	
13h (2427h)	**PERIODICLISTBASE**	7:0	Default : 0x00	Access : R/W
	PERI_BASADR[31:24]	7:0	Please see description of '25h'.	
14h (2428h)	**ASYNCLISTADDR**	7:0	Default : 0x00	Access : R/W
	ASYNC_LADR[7:5]	7:5	Current asynchronous list address. This register contains the address of the next asynchronous queue head to be	

USB Host Register (Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description	
			executed. These bits correspond to memory address signals [31:5].	
	-	4:0	Reserved.	
14h (2429h)	**ASYNCLISTADDR**	7:0	Default : 0x00	Access : R/W
	ASYNC_LADR[15:8]	7:0	Please see description of '28h'.	
15h (242Ah)	**ASYNCLISTADDR**	7:0	Default : 0x00	Access : R/W
	ASYNC_LADR[23:16]	7:0	Please see description of '28h'.	
15h (242Bh)	**ASYNCLISTADDR**	7:0	Default : 0x00	Access : R/W
	ASYNC_LADR[31:24]	7:0	Please see description of '28h'.	
16h ~ 17h (242Ch ~ 242Fh)	-	7:0	Default : -	Access :-
	-	7:0	Reserved	
18h (2430h)	**PORTSC**	7:0	Default : 0x00	Access : R/W, R/WC, RO
	PO_SUSP	7	Port suspend (R/W). 1: Port is in suspend state. 0: Port is not in suspend state. The port enable bit and suspend bit of this register define the port state as follows: Bits [Port Enable, Suspend] Port State 0X Disable 10 Enable 11 Suspend During the suspend state, downstream propagation of data is blocked on this port, except for port reset. While in the suspend state, the port is sensitive to resume detection. Writing a zero to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a zero when: • The software sets force port resume bit to a zero (from a one) • The software sets port reset bit to a one (from a zero) Note: Before setting this bit, RUN/STOP bit should be set to 0.	
	F_PO_RESM	6	Force port resume (R/W). 1: Resume detected/driven on port. 0: No resume detected/driven on port. Software sets this bit to a one to resume signaling. The	

USB Host Register (Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description	
			host controller sets this bit to a one if a J-to-K transition is detected while the port is in the suspend state. When this bit transits to a one for the detection of a J-to-K transition, the port change detect bit in USBSTS register is also set to a one.	
	-	5:4	Reserved.	
	PO_EN_CHG	3	Port enable/disable change (R/WC). 1: Port enable/disable status has changed. 0: No change.	
	PO_EN	2	Port enable/disable (R/W). 1: Enable. 0: Disable. Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a one to this field.	
	CONN_CHG	1	Connect status change (R/WC). 1: Change current connect status. 0: No change. This bit indicates a change has occurred in the port's current connect status.	
	CONN_STS	0	Current connect status (RO). 1: Device is present on the port. 0: No device is present. This value reflects the current state of the port, and may not correspond directly to cause the connect status change bit to be set. When TST_FORCEEN is set to '1', this signal is the output of U_HDISCON.	
18h (2431h)	PORTSC	7:0	Default : 0x00	Access : R/W, RO
	-	7:4	Reserved.	
	LINE_STS	3:2	Line status (RO). These bits reflect the current logical levels of the D+ and D- signal lines.	
	-	1	Reserved.	
	PO_RESET	0	Port reset. 1: Port is in reset. 0: Port is not in reset. When the software writes a one to this bit, the bus reset sequence as defined in the USB spec. is started. Software writes a zero to this bit to terminate the bus	

USB Host Register (Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description	
			reset sequence. Software must keep this bit at a one long enough to ensure the reset sequence. Note: Before setting this bit, RUN/STOP bit should be set to 0.	
19h (2432h ~ 2433h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
1Ah (2434h)	HCMISC	7:0	Default : 0x40	Access : R/W
	-	7	Reserved.	
	U_SUSP_N	6	Transceiver suspend mode. Active LOW places the transceiver in suspend mode that draws minimal power from power supplies. This is part of the power management.	
	EOF2_TIME	5:4	EOF 2 timing points, controlling EOF 2 timing point before next SOF. High-Speed EOF2 Time: 00: 2 clocks (30 MHz) = 66ns. 01: 4 clocks (30 MHz) = 133ns. 10: 8 clocks (30 MHz) = 266ns. 11: 16 clocks (30 MHz) = 533ns. Full-Speed EOF2 Time: 00: 20 clocks (30 MHz) = 666ns. 01: 40 clocks (30 MHz) = 1.333us. 10: 80 clocks (30 MHz) = 2.66us. 11: 160 clocks (30 MHz) = 5.3us. Low-Speed EOF2 Time: 00: 40 clocks (30 MHz) = 1.33us. 01: 80 clocks (30 MHz) = 2.66us. 10: 160 clocks (30 MHz) = 5.33us. 11: 320 clocks (30 MHz) = 10.66us.	
	EOF1_TIME	3:2	EOF 1 timing points, controlling EOF 1 timing point before next SOF. This value should be adjusted according to the maximum packet size. High-speed EOF1 time: 00: 540 clocks (30 MHz) = 18us. 01: 360 clocks (30 MHz) = 12us. 10: 180 clocks (30 MHz) = 6us. 11: 720 clocks (30 MHz) = 24us. Full-speed EOF1 time:	

USB Host Register (Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description	
			00: 1600 clocks (30 MHz) = 53.3us. 01: 1400 clocks (30 MHz) = 46.6us. 10: 1200 clocks (30 MHz) = 40us. 11: 21000 clocks (30 MHz) = 700us. Low-speed EOF1 time: 00: 3750 clocks (30 MHz) = 125us. 01: 3500 clocks (30 MHz) = 116us. 10: 3250 clocks (30 MHz) = 108us. 11: 4000 clocks (30 MHz) = 133us.	
	ASYN_SCH_SLPT	1:0	Asynchronous schedule sleep timer, controlling the asynchronous schedule sleep timer. 00: 5us. 01: 10us. 10: 15us. 11: 20us.	
1Ah ~ 1Fh (2435h ~ 243Fh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
20h (2440h)	BMCS	7:0	Default : 0x10	Access : R/W
	-	7:5	Reserved (must be set to '0' at all times).	
	VBUS_OFF	4	VBUS off. This bit controls the voltage on VBUS ON/OFF (Default is OFF) or in other words, the signal U_DRVBUS. 1'b0: VBUS On. 1'b1: VBUS Off.	
	INT_POLARITY	3	Control the polarity of system interrupt signal YS_INT_N. 0: Active LOW (default). 1: Active HIGH.	
	HALF_SPEED	2	Half speed enable. 1: FIFO controller asserts ACK to DMA once every two clock cycles. 0: FIFO controller asserts ACK to DMA continuously. This bit is set to '1' while doing FPGA implementation.	
	HDISCON_FLT_SEL	1	Select a timer to filter out noise of HDISCON from UTMI+. 0: Approximated to 135 us. 1: Approximated to 270 us.	
	VBUS_FLT_SEL	0	Select a timer to filter out noise of VBUS_VLD from	

USB Host Register (Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description	
			UTMI+. This signal is valid when signal U_VBUSVLD is connected. 0: Approximated to 135 us. 1: Approximated to 472 us.	
20h (2441h)	BMCS	7:0	Default : -	Access : RO
	-	7:3	Reserved.	
	HOST_SPD_TYP	2:1	Host speed type, indicating speed type of the attached device. 2'b10: HS. 2'b00: FS. 2'b01: LS. 2'b11: Reserved.	
	VBUS_VLD	0	VBUS valid. When the voltage on VBUS is above the valid VBUS threshold, this signal is valid when U_VBUSVLD is connected.	
21h (2442h ~ 2443h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
22h (2444h)	BUSMONINTSTS	7:0	Default : 0x00	Access : R/WC
	-	7:5	Reserved.	
	DMA_ERROR	4	DMA error interrupt. DMA operation cannot be finished normally, and an error signal is received. When CPU initiates DMA to fill up or read out device's FIFO, and DMA controller gets error response from system bus, this bit will be set. This bit can only be cleared by firmware. It is not affected by USB bus reset.	
	DMA_CMPLT	3	DMA completion interrupt. DMA operation is finished normally. When CPU initiates DMA to fill up or read out device's FIFO, this bit will be set after mission completion. This bit can only be cleared by firmware. It is not affected by USB bus reset.	
	DPLGRMV	2	Device plug remove. This register is set to '1' once the device plug is removed. Writing '1' clears this register and writing '0' takes no effect.	
	OVC	1	Over current detection. This register is set to '1' when the VBUS does not reach VBUS_VLD within the expected time. Writing '1' clears this register and writing '0' takes	

USB Host Register (Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description	
			no effect. This signal is valid when signal U_VBUSVLD is connected.	
	VBUS_ERR	0	VBUS error. This register is set to '1' when the Bus Monitor state machine moves to "VBUS_ERROR" state. Writing '1' clears this register and writing '0' takes no effect. This signal is valid when signal U_VBUSVLD is connected.	
22h ~ 23h (2445h ~ 2447h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
24h (2448h)	**BUSMONINTEN**	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	DMA_ERROR_EN	4	DMA_ERROR interrupt enable.	
	DMA_CMPLT_EN	3	DMA_CMPLT interrupt enable.	
	BPLGRMV_EN	2	BPLGRMV interrupt enable.	
	OVC_EN	1	OVC interrupt enable.	
	A_VBUS_ERR_EN	0	A_VBUS_ERR interrupt enable.	
24h ~ 27h) (2449h ~ 244Fh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
28h (2450h)	TST	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	TST_LOOPBK	4	FIFO loop back mode. A '1' turns on the loop-back mode. When this bit is set to '1', the host controller will enter the loop-back mode. During the loop-back mode, the host controller will use manual setting of DMA control to trigger DMA master.	
	TST_MOD	3	Test mode. A '1' turns on the test mode. When this bit is set to '1', the host controller will enter the test mode. This test mode can save simulation time. In normal mode, the host controller uses a counter for 10 ms detection of USB reset. The count is a large number. In test mode, the host controller will use a smaller number counter for USB reset detection to save the test cycle on test machine.	
	TST_PKT	2	Test mode for packet. Upon writing a '1' to this bit, the	

USB Host Register (Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description	
			host controller repetitively sends the packet defined in UTMI spec. to transceiver. Please also enable run/stop bit to enable the function.	
	TST_KSTA	1	Upon writing a '1', the D+/D- is set to the high-speed K state.	
	TST_JSTA	0	Upon writing a '1', the D+/D- is set to the high-speed J state.	
28h ~ 37h (2451h ~ 246Fh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
38h (2470h)	DMACTLPARA1	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	DMA_IO	3	DMA IO to IO. Force DMA controller not to toggle address. This bit is set when the DMA target is not a system memory but an I/O device. If this register is set to '1', the 'DMA_LEN' must be an integer multiple of DWORD (4 byes), and the 'DMA_MADDR' must align to the boundary of DWORD (4 bytes).	
	-	2	Reserved.	
	DMA_TYPE	1	DMA type, the transfer type of data moving. 0: FIFO to memory. 1: Memory to FIFO.	
	DMA_START	0	DMA Start, informing DMA controller to initiate DMA transfer. This bit is set to start the transfer and cleared when the DMA operation is completed. Note that this bit cannot be cleared by software; it can only be cleared by hardware in the case of either DMA completion or DMA error. Note that if DMA_LEN and DMA_START are set at the same time, the DMA_LEN will take effect immediately.	
38h (2471h)	DMACTLPARA1	7:0	Default : 0x00	Access : R/W
	DMA_LEN[7:0]	7:0	DMA length. The total bytes the DMA controller will move. The unit is byte. The maximum length could be 1024B-1.	
39h (2472h)	DMACTLPARA1	7:0	Default : 0x00	Access : R/W
	DMA_LEN[15:8]	7:0	Please see description of '71h'.	
39h	DMACTLPARA1	7:0	Default : 0x00	Access : R/W

USB Host Register (Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description	
(2473h)	-	7:1	Reserved.	
	DMA_LEN[16]	0	Please see description of '71h'.	
3Ah (2474h)	DMACTLPARA2	7:0	Default : 0x00	Access : R/W
	DMA_MADDR[7:0]	7:0	DMA memory address. The starting address of memory to request DMA transfer.	
3Ah (2475h)	DMACTLPARA2	7:0	Default : 0x00	Access : R/W
	DMA_MADDR[15:8]	7:0	Please see description of '74h'.	
3Bh (2476h)	DMACTLPARA2	7:0	Default : 0x00	Access : R/W
	DMA_MADDR[23:16]	7:0	Please see description of '74h'.	
3Bh (2477h)	DMACTLPARA2	7:0	Default : 0x00	Access : R/W
	DMA_MADDR[31:24]	7:0	Please see description of '74h'.	

ADC_ATOP Register (Bank = 25)

ADC_ATOP Register (Bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2500h)	REG2500	7:0	Default : 0x40	Access : R/W
	-	7	Reserved.	
	VD_AMUX	6	0/1: Select ADC RGB/CYU for VD.	
	-	5	Reserved.	
	VD_YC_EN	4	1: Enable S-Video input function.	
	VD_EN	3	1: Enable VD function.	
	DVI_EN	2	1: Enable DVI function.	
	ADC_ENB	1	1: Enable ADC_B RGB function.	
	ADC_ENA	0	1: Enable ADC_A RGB function.	
01h (2502h)	REG2502	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	AMUXB[1:0]	3:2	Select ADC_B RGB channel, VDA FB mode RGB channel. 00: Select input channel 0 for ADCB. 01: Select input channel 1 for ADCB. 10: Select input channel 2 for ADCB.	
	AMUXA[1:0]	1:0	Select ADC_A RGB channel, VDB FB mode RGB channel. 00: Select input channel 0 for ADCA. 01: Select input channel 1 for ADCA. 10: Select input channel 2 for ADCA.	
02h (2504h)	REG2504	7:0	Default : 0xFF	Access : R/W
	VD_CMUX[3:0]	7:4	Select VD CVBS/C channel. 0000: CVBS0. 0001: CVBS1. 0010: CVBS2. 0011: CVBS3. 0100: CVBS4 (Y0). 0101: CVBS6 (Y1). 0110: CVBS5 (C0). 0111: CVBS7 (C1). 1000: SOG0. 1001: SOG1. 1010: SOG2. Other: None.	
	VD_YMUX[3:0]	3:0	Select VD CVBS/Y channel. 0000: CVBS0.	

ADC_ATOP Register (Bank = 25)

Index (Absolute)	Mnemonic	Bit	Description	
			0001: CVBS1. 0010: CVBS2. 0011: CVBS3. 0100: CVBS4 (Y0). 0101: CVBS6 (Y1). 0110: CVBS5 (C0). 0111: CVBS7 (C1). 1000: SOG0. 1001: SOG1. 1010: SOG2. Other: None.	
04h (2508h)	REG2508	7:0	Default : 0xFF	Access : R/W
	PDN_ADCREF	7	1: Power down ADC voltage reference.	
	PDN_VREF	6	1: Power down voltage reference.	
	PDN_ADCR	5	1: Power down ADC_R.	
	PDN_ADCG	4	1: Power down ADC_G.	
	PDN_ADCB	3	1: Power down ADC_B.	
	PDN_PHD	2	1: Power down phase digitizer.	
	PDN_PLL	1	1: Power down ADC PLL.	
	PDN_DPLBG	0	1: Power down DPL band-gap.	
04h (2509h)	REG2509	7:0	Default : 0xFF	Access : R/W
	PDN_ICLP_Y	7	1: Power down I-clamp on Y channel.	
	PDN_ICLP_C	6	1: Power down I-clamp on C channel.	
	PDN_ADCU	5	1: Power down ADC_U.	
	PDN_ADCY	4	1: Power down ADC_Y.	
	PDN_ADCC	3	1: Power down ADC_C.	
	PDN_PHD2	2	1: Power down VD PLL phase digitizer.	
	PDN_PLL2	1	1: Power down VD PLL.	
	PDN_DPLBG2	0	1: Power down VD PLL band-gap.	
05h (250Ah)	REG250A	7:0	Default : 0xFF	Access : R/W
	PDN_HSYNC[2:0]	7:5	1: Power down HSYNC[2:0] comparator.	
	GMC_BYPASS	4	1: Enable GMC bypass mode.	
	PDN_GMC_TUNE	3	1: Power down GMC tune.	
	PDN_GMC_BIAS	2	1: Power down GMC bias circuit.	
	PDN_GMC_Y	1	1: Power down GMC on Y channel.	

ADC_ATOP Register (Bank = 25)

Index (Absolute)	Mnemonic	Bit	Description	
	PDN_GMC_C	0	1: Power down GMC on C channel.	
06h (250Ch)	REG250C	7:0	Default : 0xFF	Access : R/W
	PD_CLK[7:0]	7:0	Clock power down control. [0]: PD_CLKXTAL. [1]: PD_CLK200. [2]: PD_CLKPLLA. [3]: PD_CLKADCA. [4]: PD_CLKPLLB. [5]: PD_CLKADCB. [6]: PD_CLKD_VD. [7]: PD_CLKGMC. [8]: PD_CLK_DVI. [9]: PD_CLK_HDCP. [10]: PD_AUTO_HDCP. [11]: PD_CLK_HDMI. [12]: PD_AUTO_HDMI. [13]: PD_ICLK. [14]: PD_CLK200_FB. [15]: PD_DVIDETCLK.	
06h (250Dh)	REG250D	7:0	Default : 0xFF	Access : R/W
	PD_CLK[15:8]	7:0	Please see description of '250Ch'.	
07h (250Eh)	REG250E	7:0	Default : 0x00	Access : R/W
	SOFTRST[7:0]	7:0	1: Soft reset for adcdvipll blocks. [15:8]: Reserved. [7]: Soft-reset atop control. [6]: Soft-reset HDMI. [5]: Soft-reset HDCP. [4]: Soft-reset DVI. [3]: Soft-reset PLL_DIG_B. [2]: Soft-reset ADC_VD. [1]: Soft-reset PLL_DIG_A. [0]: Soft-reset ADC_DIG_A.	
07h (250Fh)	REG250F	7:0	Default : 0x00	Access : R/W
	SOFTRST[15:8]	7:0	Please see description of '250Eh'.	
08h (2510h)	REG2510	7:0	Default : 0x76	Access : R/W
	MPLL_PDIV	7	Select MPLL post divider. 0: DIV3. 1: DIV2.5.	

ADC_ATOP Register (Bank = 25)

Index (Absolute)	Mnemonic	Bit	Description	
	MPLL_PORST	6	1: MPLL power-on reset.	
	MPLL_RESET	5	1: MPLL reset.	
	MPLL_PD	4	1: MPLL power down.	
	MPLL_VCO_OFFSET	3	MPLL VCO offset.	
	MPLL_ICTRL[2:0]	2:0	MPLL current control.	
08h ~ 09h (2511h ~ 2513h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
0Ah (2514h)	REG2514	7:0	Default : 0x24	Access : R/W
	MPLL_LOOP_DIV2[7:0]	7:0	Select MPLL loop second divider. 0, 1: DIV1. N: DIVN.	
0Ah (2515h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
0Bh (2516h)	REG2516	7:0	Default : 0x7F	Access : R/W
	-	7	Reserved.	
	MPLL_PD_VIFCLK	6	1: Power down MPLL output divider clock for VIF ADC.	
	MPLL_OUTDIV_PD[5:0]	5:0	1: Power down MPLL output divider clocks. [0]: PD USB CLK. [1]: PD DIV7. [2]: PD DIV5. [3]: PD DIV3. [4]: PD DIV2. [5]: PD DIV3.5.	
0Bh (2517h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
0Ch (2518h)	REG2518	7:0	Default : 0x01	Access : R/W
	-	7	Reserved.	
	-	6	Reserved.	
	ADC_PLL_PDIV[2:0]	5:3	ADC PLL clock post divider. #b000: DIV1. #b001: DIV2. #b011: DIV4. #b111: DIV8. #others: Reserved.	
	ADC_PLL_MULT[2:0]	2:0	ADC PLL clock multiplier: N+1.	

ADC_ATOP Register (Bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Dh ~ 11h (251Ah ~ 2523h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
12h (2524h)	REG2524	7:0	Default : 0x01	Access : R/W
	-	7	Reserved.	
	-	6	Reserved.	
	VD_PLL_PDIV[2:0]	5:3	VD (ADCB) PLL clock post divider. #b000: DIV1. #b001: DIV2. #b011: DIV4. #b111: DIV8. #others: Reserved.	
	VD_PLL_MULT[2:0]	2:0	VD (ADCB) PLL clock multiplier = N+1.	
13h ~ 1Bh (2526h ~ 2537h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
1Ch (2538h)	REG2538	7:0	Default : 0x08	Access : R/W
	-	7:6	Reserved.	
	SOG_DISA	5	1: Disable active SOG comparator.	
	SOG_THA[4:0]	4:0	Select SOG comparator threshold, step = 10mv.	
1Ch (2539h)	REG2539	7:0	Default : 0x00	Access : R/W
	ADCBWA[3:0]	7:4	Select ADC input filter bandwidth. 0000: 260MHz. 0001: 190MHz. 0010: 150MHz. 0011: 120MHz. 0100: 60MHz. 0101: 30MHz. 0110: 25MHz. 0111: 23MHz. 1000: 21MHz. 1001: 20MHz. 1010: 18MHz. 1011: 17MHz. 1100: 16MHz. 1101: 15MHz. 1110: 14MHz.	

ADC_ATOP Register (Bank = 25)

Index (Absolute)	Mnemonic	Bit	Description	
			1111: 6MHz.	
	SOG_OPTFIRA	3	0/1: Disable/enable SOG input low bandwidth filter.	
	SOG_BWA[2:0]	2:0	Select SOG input filter bandwidth.	
1Dh ~ 1Eh (253Ah ~ 253Dh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
1Fh (253Eh)	REG253E	7:0	Default : 0x08	Access : R/W
	-	7:6	Reserved.	
	SOG_DISB	5	1: Disable active SOG comparator.	
	SOG_THB[4:0]	4:0	Select SOG comparator threshold, step = 10mv.	
1Fh (253Fh)	REG253F	7:0	Default : 0x00	Access : R/W
	ADCBWB[3:0]	7:4	Select ADC input filter bandwidth.	
	SOG_OPTFIRB	3	0/1: Disable/enable SOG input low bandwidth filter.	
	SOG_BWB[2:0]	2:0	Select SOG input filter bandwidth.	
20h (2540h)	REG2540	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	-	5:3	Reserved.	
	HSYNC_LVL[2:0]	2:0	Select HSYNC trigger level. 000 : VIH = 1.54V, VIL=1.10V. 001 : VIH = 1.54V, VIL=0.88V. 010 : VIH = 1.76V, VIL=1.10V. 011 : VIH = 1.76V, VIL=0.88V. 100 : VIH = 1.87V, VIL=1.10V. 101 : VIH = 1.87V, VIL=0.88V. 110 : VIH = 1.76V, VIL=1.32V. 111 : VIH = 1.87V, VIL=1.32V.	
20h ~ 22h (2541h ~ 2545h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
23h (2546h)	REG2546	7:0	Default : 0x38	Access : R/W
	-	7	Reserved.	
	-	6	Reserved.	
	-	5	Reserved.	
	XTAL_SEL[1:0]	4:3	Select XTAL driving strength.	

ADC_ATOP Register (Bank = 25)

Index (Absolute)	Mnemonic	Bit	Description	
	VDD2LO_EN	2	1: Enable VDD too low reset.	
	-	1:0	Reserved.	
23h (2547h)	REG2547	7:0	Default : 0x30	Access : R/W
	XTAL_FREQ[7:0]	7:0	Set XTAL frequency for timing detection normalization (default: 12MHz, format: 6.2 MHz, XTAL_FREQ=fxtal * 4).	
24h ~ 25h (2548h ~ 254Bh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
26h (254Ch)	REG254C	7:0	Default : 0x58	Access : R/W
	-	7	Reserved.	
	REF_SEL_VD	6	Select ADC reference DAC for VD function (suggest DAC1 assigned to VD).	
	REF_SEL[5:0]	5:0	Select ADC reference DAC for ADC U, Y, C, B, G, and R. 0: DAC0. 1: DAC1.	
26h ~ 29h (254Dh ~ 2553h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
2Ah (2554h)	REG2554	7:0	Default : 0x00	Access : RO, R/W, WO
	-	7:5	Reserved.	
	CLROVF_YC	4	Write "1" to clear ADC_YC overflow flags.	
	OVF_YC[3:0]	3:0	ADC overflow flags, OVFY, UNFY, OVFC, and UNFC.	
2Ch (2558h)	REG2558	7:0	Default : 0x04	Access : R/W
	-	7	Reserved.	
	VMID_SELA	6	Select VMID mode. 0: Controlled by ADCB gain. 1: Constant voltage.	
	BSEL_CVA[1:0]	5:4	Select VCLAMP voltage for ADC B input. 00: Clamp to GND. 01: Clamp to VP3. 1x: Clamp to VMID.	
	GSEL_CVA[1:0]	3:2	Select VCLAMP voltage for ADC G input. 00: Clamp to GND. 01: Clamp to VP3. 1x: Clamp to VMID.	
	RSEL_CVA[1:0]	1:0	Select VCLAMP voltage for ADC R input.	

ADC_ATOP Register (Bank = 25)

Index (Absolute)	Mnemonic	Bit	Description	
			00: Clamp to GND. 01: Clamp to VP3. 1x: Clamp to VMID.	
2Ch (2559h)	REG2559	7:0	Default : 0x04	Access : R/W
	-	7	Reserved.	
	VMID_SELB	6	Select VMID mode. 0: Controlled by ADCU gain. 1: Constant voltage.	
	BSEL_CVB[1:0]	5:4	Select VCLAMP voltage for ADCB B input. 00: Clamp to GND. 01: Clamp to VP3. 1x: Clamp to VMID.	
	GSEL_CVB[1:0]	3:2	Select VCLAMP voltage for ADCB G input. 00: Clamp to GND. 01: Clamp to VP3. 1x: Clamp to VMID.	
	RSEL_CVB[1:0]	1:0	Select VCLAMP voltage for ADCB R input. 00: Clamp to GND. 01: Clamp to VP3. 1x: Clamp to VMID.	
2Dh (255Ah)	REG255A	7:0	Default : 0x10	Access : R/W
	-	7:5	Reserved.	
	ADC_INMSEL	4	0/1: Select ADC INM pins, differential/shared mode.	
	SVCLP[3:0]	3:0	Select GMC VCLAMP voltage level. 0000: 1.15V. 0001: 1.2V. 0010: 0.85V. 0011: 0.90V. 0100: 0.95V. 0101: 1.00V. 0110: 1.05V. 0111: 1.10V. 1000: 1.5V. 1001: 1.55V. 1010: 1.6V. 1011: 0.6V. 1100: 0.7V. 1101: 0.8V.	

ADC_ATOP Register (Bank = 25)

Index (Absolute)	Mnemonic	Bit	Description	
			1110: 1.45V.	
			1111: 1.4V.	
2Eh (255Ch)	REG255C	7:0	Default : 0x00	Access : R/W
	ICLP_M1[1:0]	7:6	Select I-clamp current range for Y channel.	
	ICLP_M0[1:0]	5:4	Select I-clamp current range for C channel.	
	SEL_ICLAMP[3:0]	3:0	Select I-clamp bias current.	
30h ~ 37h (2560h ~ 256Fh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
38h (2570h)	REG2570	7:0	Default : 0x0F	Access : R/W
	-	7	Reserved.	
	CVBSO_MUXEN[2:0]	6:4	CVBS buffer input channel enable. [6]: 1: CP channel enable. [5]: 1: YN channel enable. [4]: 1: YP channel enable.	
	PDN_CVBSO_CPOS	3	1: CP channel clamp power down.	
	PDN_CVBSO_YPOS	2	1: YP channel clamp power down.	
	PDN_CVBSO_LSH	1	1: Power down CVBS output buffer level shift.	
	PDN_CVBSO	0	1: Power down CVBS output buffer.	
39h (2572h)	REG2572	7:0	Default : 0x00	Access : R/W
	CVBSO_YNMUX[3:0]	7:4	Select YN channel input. 0000: VCOM0. 0001: VCOM1. 0010: VCOM1. 0011: VCOM1. 0100: VCOM2. 0101: VCOM2. 0110: VCOM2. 0111: VCOM2. 1000: VCOM2. 1001: VCOM2. 1010: VCOM2. 1011: CVBS_DACM.	
	CVBSO_YPMUX[3:0]	3:0	Select YP channel input. 0000: CVBS0. 0001: CVBS1. 0010: CVBS2.	

ADC_ATOP Register (Bank = 25)

Index (Absolute)	Mnemonic	Bit	Description
			0011: CVBS3. 0100: CVBS4 (Y0). 0101: CVBS5 (C0). 0110: CVBS6 (Y1). 0111: CVBS7 (C1). 1000: SOG0. 1001: SOG1. 1010: SOG2. 1011: CVBS DAC.
39h (2573h)	REG2573	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	CVBSO_CPMUX[3:0]	3:0	Select CP channel input. 0000: CVBS0. 0001: CVBS1. 0010: CVBS2. 0011: CVBS3. 0100: CVBS4 (Y0). 0101: CVBS5 (C0). 0110: CVBS6 (Y1). 0111: CVBS7 (C1). 1000: R0. 1001: R1. 1010: R2. 1011: CVBS DAC.
3Ah (2574h)	REG2574	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	CVBSO_ISINK[2:0]	5:3	Select CVBSO clamp sink current.
	CVBSO_HISOURCE	2	1: Enable CVBSO clamp high sourcing current.
	CVBSO_CBW[1:0]	1:0	C channel clamp bandwidth.
3Bh (2576h ~ 2577h)	-	7:0	Default : - Access : -
	-	7:0	Reserved.
3Ch (2578h)	REG2578	7:0	Default : 0x0F Access : R/W
	-	7	Reserved.
	CVBSO2_MUXEN[2:0]	6:4	CVBS buffer input channel enable. [6]: 1: CP channel enable. [5]: 1: YN channel enable. [4]: 1: YP channel enable.

ADC_ATOP Register (Bank = 25)

Index (Absolute)	Mnemonic	Bit	Description	
	PDN_CVBSO2_CPOS	3	1: CP channel clamp power down.	
	PDN_CVBSO2_YPOS	2	1: YP channel clamp power down.	
	PDN_CVBSO2_LSH	1	1: Power down CVBS output buffer level shift.	
	PDN_CVBSO2	0	1: Power down CVBS output buffer.	
3Dh (257Ah)	REG257A	7:0	Default : 0x00	Access : R/W
	CVBSO2_YNMUX[3:0]	7:4	Select YN channel input. 0000: VCOM0. 0001: VCOM1. 0010: VCOM1. 0011: VCOM1. 0100: VCOM2. 0101: VCOM2. 0110: VCOM2. 0111: VCOM2. 1000: VCOM2. 1001: VCOM2. 1010: VCOM2. 1011: CVBS_DACM.	
	CVBSO2_YPMUX[3:0]	3:0	Select YP channel input. 0000: CVBS0. 0001: CVBS1. 0010: CVBS2. 0011: CVBS3. 0100: CVBS4 (Y0). 0101: CVBS5 (C0). 0110: CVBS6 (Y1). 0111: CVBS7 (C1). 1000: SOG0. 1001: SOG1. 1010: SOG2. 1011: CVBS DAC.	
3Dh (257Bh)	REG257B	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	CVBSO2_CPMUX[3:0]	3:0	Select CP channel input. 0000: CVBS0. 0001: CVBS1. 0010: CVBS2. 0011: CVBS3.	

ADC_ATOP Register (Bank = 25)

Index (Absolute)	Mnemonic	Bit	Description	
			0100: CVBS4 (Y0).	
			0101: CVBS5 (C0).	
			0110: CVBS6 (Y1).	
			0111: CVBS7 (C1).	
			1000: R0.	
			1001: R1.	
			1010: R2.	
			1011: CVBS DAC.	
3Eh (257Ch)	REG257C	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	CVBSO2_ISINK[2:0]	5:3	Select CVBSO clamp sink current.	
	CVBSO2_HISOURCE	2	1: Enable CVBSO clamp high sourcing current.	
	CVBSO2_CBW[1:0]	1:0	C channel clamp bandwidth.	
3Fh (257Eh ~ 257Fh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
46h (258Ch)	REG258C	7:0	Default : 0x00	Access : R/W
	CVBS_DAC_EN	7	1: Enable CVBS DAC.	
	-	6:0	Reserved.	
46h (258Dh)	REG258D	7:0	Default : 0x00	Access : R/W
	CVBS_DAC_GAIN[3:0]	7:4	CVBS DAC gain control.	
	CVBS_DAC_OFFSET[3:0]	3:0	CVBS DAC offset control.	
54h (25A8h)	REG25A8	7:0	Default : 0xC8	Access : R/W
	ATTEN_CLPENR	7	1: Force a clamp duration when attenuator on.	
	ATTEN_CLPENF	6	1: Force a clamp duration when attenuator off.	
	ATTEN_CLPDUR[5:0]	5:0	Select clamp duration when switch from/to attenuator, N*1024 CLKFSC.	
54h (25A9h)	REG25A9	7:0	Default : 0x40	Access : R/W
	ATTEN_SWDLY[1:0]	7:6	Select enable attenuator to switch MUX delay, N*64 CLKFSC.	
	ATTEN_OV[5:0]	5:0	Override CVBS input attenuator. [5]: Override attenuator Y enable. [4]: Enable attenuator Y input MUX. [3]: Enable attenuator Y. [2]: Override attenuator C enable. [1]: Enable attenuator C input MUX.	

ADC_ATOP Register (Bank = 25)

Index (Absolute)	Mnemonic	Bit	Description	
			[0]: Enable attenuator C.	
55h (25AAh)	REG25AA	7:0	Default : 0x08	Access : RO, R/W
	-	7	Reserved.	
	AGC_COARSE[2:0]	6:4	VD coarse gain status.	
	ATTEN_SVCLP[3:0]	3:0	Select clamp level when attenuator enable.	
56h (25ACh ~ 25BAh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
60h (25C0h)	REG25C0	7:0	Default : 0xFF	Access : R/W
	PDN_DVIPLL	7	1: Power down DVI PLL.	
	PDN_DVIPLLBG	6	1: Power down DVI PLL band-gap.	
	PDN_DVIPLLREG	5	1: Power down DVI PLL regulator.	
	PDN_DMIBEX	4	1: Power down DVI output bias current.	
	PDN_DVICK	3	1: Power down DVI clock receiver.	
	PDN_DM[2:0]	2:0	1: Power down DVI de-multiplexer.	
60h (25C1h)	REG25C1	7:0	Default : 0x7F	Access : R/W
	-	7	Reserved.	
	PDN_DVIRCK[1]	6	1: Power down DVI_B clock channels pull-up resistors.	
	PDN_DVIRCK[0]	5	1: Power down DVI_A clock channels pull-up resistors.	
	PDN_DVIRD[1]	4	1: Power down DVI_B data channels pull-up resistors.	
	PDN_DVIRD[0]	3	1: Power down DVI_A data channels pull-up resistors.	
	PDN_DPLMXR[2:0]	2:0	1: Power down DPL mixer [2:0].	
61h (25C2h)	REG25C2	7:0	Default : 0x35	Access : R/W
	-	7:4	Reserved.	
	SWCKB	3	1: Enable CLKB input switch.	
	SWCKA	2	1: Enable CLKA input switch.	
	SWB	1	1: Enable DATA_B input switch.	
	SWA	0	1: Enable DATA_A input switch.	
61h (25C3h)	REG25C3	7:0	Default : 0x10	Access : R/W
	HR_SEL[2:0]	7:5	Select DVI pull-up resistor.	
	-	4:0	Reserved.	
62h ~ 67h (25C4h ~ 25CFh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	

ADC_ATOP Register (Bank = 25)

Index (Absolute)	Mnemonic	Bit	Description	
68h (25D0h)	REG25D0	7:0	Default : 0xC0	Access : RO, R/W
	HOTPLUGB_OEN	7	0: HotplugB GPIO output enable. (from Lola 2DVI part)	
	HOTPLUGA_OEN	6	0: HotplugA GPIO output enable.	
	HOTPLUGB	5	Write hotplugB GPIO output value. Read hotplugB GPIO input value (from Lola 2DVI part).	
	HOTPLUGA	4	Write HotplugA GPIO output value. Read HotplugA GPIO input value.	
	-	3:0	Reserved.	
70h (25E0h)	REG25E0	7:0	Default : -	Access : RO
	ADCDVI_IRQ_STATUS[7:0]	7:0	ADCDVI IRQ status. 4'b0: HDMI_MODE_CHG, DVI_CK_CHG.	
70h (25E1h)	REG25E1	7:0	Default : 0x00	Access : R/W
	ADCDVI_IRQ_MASK[7:0]	7:0	ADCDVI IRQ mask control.	
71h (25E2h)	REG25E2	7:0	Default : 0x00	Access : R/W
	ADCDVI_IRQ_FORCE[7:0]	7:0	ADCDVI IRQ force control.	
71h (25E3h)	REG25E3	7:0	Default : 0x00	Access : R/W
	ADCDVI_IRQ_CLR[7:0]	7:0	ADCDVI IRQ clear control.	

ADC_DTOP Register (Bank = 26)

ADC_DTOP Register (Bank = 26)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2600h)	REG2600	7:0	Default : 0x95	Access : R/W
	PLLDIV[7:0]	7:0	ADC PLL divider ratio (htotal-3), (write sequence LSB -> MSB).	
00h (2601h)	REG2601	7:0	Default : 0x06	Access : R/W
	-	7:5	Reserved.	
	PLLDIV[12:8]	4:0	Please see description of '2600h'.	
01h (2602h)	REG2602	7:0	Default : 0x82	Access : R/W
	BWCOEF[7:0]	7:0	ADC PLL bandwidth coefficient.	
01h (2603h)	REG2603	7:0	Default : 0x09	Access : R/W
	FREQCOEF[7:0]	7:0	ADC PLL frequency coefficient.	
02h (2604h)	REG2604	7:0	Default : 0x05	Access : R/W
	DAMPCOEF[7:0]	7:0	ADC PLL damping coefficient.	
03h (2606h)	REG2606	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	PHASE_CC[5:0]	5:0	Select ADC sampling clock phase.	
03h (2607h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
04h (2608h)	REG2608	7:0	Default : 0x05	Access : R/W
	PLL_STATUS_SEL[2:0]	7:5	Select PLL digital status.	
	PHD_CAL_DIS	4	Disable phase digitalizer calibration.	
	SETTLE_CNT[3:0]	3:0	Select phase digitalizer settling time.	
04h (2609h)	REG2609	7:0	Default : 0xC6	Access : R/W
	WDOG_TOL[1:0]	7:6	Select PLL watch dog reset tolerance.	
	IQCLR_TH[2:0]	5:3	PLL lock to unlock threshold.	
	IQSET_TH[2:0]	2:0	PLL unlock to lock threshold.	
05h (260Ah)	REG260A	7:0	Default : -	Access : RO
	PLL_STATUS[7:0]	7:0	PLL digital status 000: LOCK, IQ, SLOW, FAST, FREERUN, 3'b000	
06h (260Ch ~ 260Dh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
07h	REG260E	7:0	Default : 0x8A	Access : R/W

ADC_DTOP Register (Bank = 26)

Index (Absolute)	Mnemonic	Bit	Description	
(260Eh)	HSYNC_POL	7	Input HSYNC polarity 0: Low active. 1: High active.	
	SOG_EN	6	Select PLL locking source. 0: HSYNC. 1: SOG.	
	HSYNC_EDGE	5	Select PLL locking edge. 0: HSYNC leading edge. 1: HSYNC trailing edge.	
	CLAMP_EDGE	4	select clamp reference edge 0: HSYNC trailing edge 1: HSYNC leading edge	
	CCDIS	3	1: Disable clamp during coast region.	
	WDOG_DIS	2	1: Disable ADC PLL watch dog.	
	COAST_POL	1	Select coast polarity. 0: Low active. 1: High active.	
	-	0	Reserved.	
07h (260Fh)	**REG260F**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSOUT_PW[7:0]	7:0	Select extended HSOUT pulse width.	
08h (2610h)	**REG2610**	**7:0**	**Default : 0x80**	**Access : R/W**
	GAIN_R[7:0]	7:0	ADC R channel gain control.	
08h (2611h)	**REG2611**	**7:0**	**Default : 0x80**	**Access : R/W**
	OFFSET_R[7:0]	7:0	ADC R channel offset control.	
09h (2612h)	**REG2612**	**7:0**	**Default : 0x80**	**Access : R/W**
	GAIN_G[7:0]	7:0	ADC G channel gain control.	
09h (2613h)	**REG2613**	**7:0**	**Default : 0x80**	**Access : R/W**
	OFFSET_G[7:0]	7:0	ADC G channel offset control.	
0Ah (2614h)	**REG2614**	**7:0**	**Default : 0x80**	**Access : R/W**
	GAIN_B[7:0]	7:0	ADC B channel gain control.	
0Ah (2615h)	**REG2615**	**7:0**	**Default : 0x80**	**Access : R/W**
	OFFSET_B[7:0]	7:0	ADC B channel offset control.	
0Bh (2616h)	**REG2616**	**7:0**	**Default : 0x05**	**Access : R/W**
	CLAMP_DLY[7:0]	7:0	Select clamp pulse start position relative to input HSYNC edge.	

ADC_DTOP Register (Bank = 26)

Index (Absolute)	Mnemonic	Bit	Description	
0Bh (2617h)	REG2617	7:0	Default : 0x05	Access : R/W
	CLAMP_DUR[7:0]	7:0	Select clamp pulse duration.	
0Ch (2618h)	REG2618	7:0	Default : 0x24	Access : R/W
	HSOUT_GEN	7	1: Enable HSOUT pulse extension.	
	-	6	Reserved.	
	RGB_SWAP[5:0]	5:0	Select RGB data to scalar. [1:0]: SEL R. [3:2]: SEL G. [5:4]: SEL B. 00: R. 01: G. 10: B. 11: Blank.	
0Ch ~ 0Dh (2619h ~ 261Bh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
0Eh (261Ch)	REG261C	7:0	Default : 0x40	Access : R/W
	TIMEOUT_H[7:0]	7:0	HSYNC activity timeout period (100us).	
0Eh (261Dh)	REG261D	7:0	Default : 0x64	Access : R/W
	TIMEOUT_V[7:0]	7:0	VSYNC activity timeout period (ms).	
0Fh (261Eh)	REG261E	7:0	Default : -	Access : RO
	-	7:3	Reserved.	
	SOG_TOG	2	1: Active channel SOG toggle status.	
	VSYNC_TOG	1	1: Active channel VSYNC toggle status.	
	HSYNC_TOG	0	1: active channel HSYNC toggle status.	
10h (2620h)	REG2620	7:0	Default : 0x00	Access : R/W, WO
	CALG_TRIG	7	Write "1" to start gain CAL procedure.	
	CALO_TRIG	6	Write "1" to start offset CAL procedure.	
	CALG_EN	5	1: Enable gain auto CAL procedure.	
	CALO_EN	4	1: Enable offset auto CAL procedure.	
	-	3:2	Reserved.	
	-	1:0	Reserved.	
10h (2621h)	REG2621	7:0	Default : 0x04	Access : R/W
	CALO_BLK	7	Select offset CAL target DOUT code.	

ADC_DTOP Register (Bank = 26)

Index (Absolute)	Mnemonic	Bit	Description	
			0: 0. 1: 16.	
	CAL_STOP	6	1: stop CAL procedure.	
	-	5:0	Reserved.	
11h (2622h ~ 2627h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
14h (2628h)	REG2628	7:0	Default : 0x00	Access : R/W
	CAL_EDGE0	7	0/1: Select CAL start from HSYNC leading/trailing edge for CAL to reference.	
	CAL_DLY0[6:0]	6:0	CAL pulse start delay (N+1).	
15h (262Ah)	REG262A	7:0	Default : 0x10	Access : R/W
	CAL_SMPDLY0[7:0]	7:0	CAL sample data delay (N+1).	
15h (262Bh)	REG262B	7:0	Default : 0x10	Access : R/W
	CAL_SMPDUR0[7:0]	7:0	CAL sample data duration (N+1).	
16h ~ 1Ch (262Ch ~ 2639h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
1Dh (263Ah)	REG263A	7:0	Default : 0x00	Access : RO, WO
	-	7	Reserved.	
	CLROVF_RGB	6	Write "1" to clear ADC_RGB overflow flags.	
	OVF_RGB[5:0]	5:0	ADC overflow flags, OVFB, UNFB, OVFG, UNFG, OVFR and UNFR.	
1Eh ~ 1Fh (263Ch ~ 263Fh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
ADC_DTOP Registers for ADCB				
20h (2640h)	REG2640	7:0	Default : 0x95	Access : R/W
	PLLDIV[7:0]	7:0	ADC PLL divider ratio (htotal-3), (write sequence LSB -> MSB).	
20h (2641h)	REG2641	7:0	Default : 0x06	Access : R/W
	-	7:5	Reserved.	
	PLLDIV[12:8]	4:0	Please see description of '2640h'.	
21h (2642h)	REG2642	7:0	Default : 0x82	Access : R/W
	BWCOEF[7:0]	7:0	ADC PLL bandwidth coefficient.	

ADC_DTOP Register (Bank = 26)

Index (Absolute)	Mnemonic	Bit	Description	
21h (2643h)	**REG2643**	**7:0**	**Default : 0x09**	Access : R/W
	FREQCOEF[7:0]	7:0	ADC PLL frequency coefficient.	
22h (2644h)	**REG2644**	**7:0**	**Default : 0x05**	Access : R/W
	DAMPCOEF[7:0]	7:0	ADC PLL damping coefficient.	
23h (2646h)	**REG2646**	**7:0**	**Default : 0x00**	Access : R/W
	-	7:6	Reserved.	
	PHASE_CC[5:0]	5:0	Select ADC sampling clock phase.	
23h (2647h)	-	7:0	**Default : -**	Access : -
	-	7:0	Reserved.	
24h (2648h)	**REG2648**	**7:0**	**Default : 0x05**	Access : R/W
	PLL_STATUS_SEL[2:0]	7:5	Select PLL digital status.	
	PHD_CAL_DIS	4	Disable phase digitalizer calibration.	
	SETTLE_CNT[3:0]	3:0	Select phase digitalizer settling time.	
24h (2649h)	**REG2649**	**7:0**	**Default : 0xC6**	Access : R/W
	WDOG_TOL[1:0]	7:6	Select PLL watch dog reset tolerance.	
	IQCLR_TH[2:0]	5:3	PLL lock to unlock threshold.	
	IQSET_TH[2:0]	2:0	PLL unlock to lock threshold.	
25h (264Ah)	**REG264A**	**7:0**	**Default : -**	Access : RO
	PLL_STATUS[7:0]	7:0	PLL digital status 000: LOCK, IQ, SLOW, FAST, FREERUN, 3'b000	
26h (264Ch ~ 264Dh)	-	7:0	**Default : -**	Access : -
	-	7:0	Reserved.	
27h (264Eh)	**REG264E**	**7:0**	**Default : 0x8A**	Access : R/W
	HSYNC_POL	7	Input HSYNC polarity 0: Low active. 1: High active.	
	SOG_EN	6	Select PLL locking source. 0: HSYNC. 1: SOG.	
	HSYNC_EDGE	5	Select PLL locking edge. 0: HSYNC leading edge. 1: HSYNC trailing edge.	
	CLAMP_EDGE	4	select clamp reference edge 0: HSYNC trailing edge	

ADC_DTOP Register (Bank = 26)

Index (Absolute)	Mnemonic	Bit	Description	
			1: HSYNC leading edge	
	CCDIS	3	1: Disable clamp during coast region.	
	WDOG_DIS	2	1: Disable ADC PLL watch dog.	
	COAST_POL	1	select coast polarity 0: Low active 1: High active	
	-	0	Reserved.	
27h (264Fh)	REG264F	7:0	Default : 0x00	Access : R/W
	HSOUT_PW[7:0]	7:0	Select extended HSOUT pulse width.	
28h (2650h)	REG2650	7:0	Default : 0x80	Access : R/W
	GAIN_R[7:0]	7:0	ADC R channel gain control.	
28h (2651h)	REG2651	7:0	Default : 0x80	Access : R/W
	OFFSET_R[7:0]	7:0	ADC R channel offset control.	
29h (2652h)	REG2652	7:0	Default : 0x80	Access : R/W
	GAIN_G[7:0]	7:0	ADC G channel gain control.	
29h (2653h)	REG2653	7:0	Default : 0x80	Access : R/W
	OFFSET_G[7:0]	7:0	ADC G channel offset control.	
2Ah (2654h)	REG2654	7:0	Default : 0x80	Access : R/W
	GAIN_B[7:0]	7:0	ADC B channel gain control.	
2Ah (2655h)	REG2655	7:0	Default : 0x80	Access : R/W
	OFFSET_B[7:0]	7:0	ADC B channel offset control.	
2Bh (2656h)	REG2656	7:0	Default : 0x05	Access : R/W
	CLAMP_DLY[7:0]	7:0	Select clamp pulse start position relative to input HSYNC edge.	
2Bh (2657h)	REG2657	7:0	Default : 0x05	Access : R/W
	CLAMP_DUR[7:0]	7:0	Select clamp pulse duration.	
2Ch (2658h)	REG2658	7:0	Default : 0x24	Access : R/W
	HSOUT_GEN	7	1: Enable HSOUT pulse extension.	
	-	6	Reserved.	
	RGB_SWAP[5:0]	5:0	Select RGB data to scalar. [1:0]: SEL R. [3:2]: SEL G. [5:4]: SEL B. 00: R.	

ADC_DTOP Register (Bank = 26)

Index (Absolute)	Mnemonic	Bit	Description	
			01: G. 10: B. 11: Blank.	
2Ch ~ 2Dh (2659h ~ 265Bh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
2Eh (265Ch)	**REG265C**	7:0	**Default : 0x40**	**Access : R/W**
	TIMEOUT_H[7:0]	7:0	HSYNC activity timeout period (100us).	
2Eh (265Dh)	**REG265D**	7:0	**Default : 0x64**	**Access : R/W**
	TIMEOUT_V[7:0]	7:0	VSYNC activity timeout period (ms).	
2Fh (265Eh)	**REG265E**	7:0	**Default : -**	**Access : RO**
	-	7:3	Reserved.	
	SOG_TOG	2	1: Active channel SOG toggle status.	
	VSYNC_TOG	1	1: Active channel VSYNC toggle status.	
	HSYNC_TOG	0	1: active channel HSYNC toggle status.	
30h (2660h)	**REG2660**	7:0	**Default : 0x00**	**Access : R/W, WO**
	CALG_TRIG	7	Write "1" to start gain CAL procedure.	
	CALO_TRIG	6	Write "1" to start offset CAL procedure.	
	CALG_EN	5	1: Enable gain auto CAL procedure.	
	CALO_EN	4	1: Enable offset auto CAL procedure.	
	-	3:2	Reserved.	
	-	1:0	Reserved.	
30h (2661h)	**REG2661**	7:0	**Default : 0x04**	**Access : R/W**
	CALO_BLK	7	Select offset CAL target DOUT code. 0: 0. 1: 16.	
	CAL_STOP	6	1: stop CAL procedure.	
	-	5:0	Reserved.	
31h (2662h ~ 2667h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
34h (2668h)	**REG2668**	7:0	**Default : 0x00**	**Access : R/W**
	CAL_EDGE0	7	0/1: Select CAL start from HSYNC leading/trailing edge for CAL to reference.	

ADC_DTOP Register (Bank = 26)

Index (Absolute)	Mnemonic	Bit	Description	
	CAL_DLY0[6:0]	6:0	CAL pulse start delay (N+1).	
35h (266Ah)	**REG266A**	**7:0**	**Default : 0x10**	**Access : R/W**
	CAL_SMPDLY0[7:0]	7:0	CAL sample data delay (N+1).	
35h (266Bh)	**REG266B**	**7:0**	**Default : 0x10**	**Access : R/W**
	CAL_SMPDUR0[7:0]	7:0	CAL sample data duration (N+1).	
36h ~ 3Ch (266Ch ~ 2679h)	-	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
3Dh (267Ah)	**REG267A**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	-	7	Reserved.	
	CLROVF_RGB	6	Write "1" to clear ADC_RGB overflow flags.	
	OVF_RGB[5:0]	5:0	ADC overflow flags, OVFB, UNFB, OVFG, UNFG, OVFR and UNFR.	
3Eh (267Ch ~ 267Fh)	-	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	

HDMI Register (Bank = 27h)

HDMI Register (Bank = 27h)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2700h ~ 2701h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
01h (2702h)	HDMIST1_L	7:0	Default : -	Access : RO
	-	7:5	Reserved.	
	ONEBIT_AU_PKT	4	One bit audio packet received. NOTE: All bits in HDMIST1 register represent, when reading back 1, one or more than one packets have been received by the HDMI receiver engine between the previous read and current read. No packet was received since last read if a bit is read back 0. (Write 1 to clear)	
	ACP_PKT	3	ACP packet received. (Write 1 to clear)	
	ISRC1_PKT	2	ISRC1 packet received. (Write 1 to clear)	
	ISRC2_PKT	1	ISRC2 packet received. (Write 1 to clear)	
	NULL_PKT	0	NULL packet received. (Write 1 to clear)	
01h (2703h)	HDMIST1_H	7:0	Default : -	Access : RO
	VS_PKT	7	Vendor specific packet or user specified packet received. (Write 1 to clear)	
	ACR_PKT	6	Audio clock regeneration packet received. (Write 1 to clear)	
	ASAMPLE_PKT	5	Audio sample packet received. (Write 1 to clear)	
	GC_PKT	4	General control packet received. (Write 1 to clear)	
	AVI_PKT	3	AVI InfoFrame packet received. (Write 1 to clear)	
	SPD_PKT	2	SPD InfoFrame packet received. (Write 1 to clear)	
	AUI_PKT	1	Audio InfoFrame packet received. (Write 1 to clear)	
	MPEG_PKT	0	MPEG InfoFrame packet received.	

HDMI Register (Bank = 27h)

Index (Absolute)	Mnemonic	Bit	Description	
			(Write 1 to clear)	
02h ~ 03h (2704h ~ 2707h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
04h (2708h)	**HDMI_ERR1**	7:0	**Default : 0x00**	**Access : RO/WC**
	DC_FIFO_UDF	7	Deep color FIFO underflow. (Write 1 to clear)	
	DC_FIFO_OVF	6	Deep color FIFO overflow. (Write 1 to clear)	
	AS_PBIT_ERR	5	Audio sample parity bit error detected. (Write 1 to clear)	
	ASAMPLE_ERR	4	Audio sample packet receives error occurred; sample repeated. (Write 1 to clear)	
	UNSUPPKT	3	Unsupported packet received. (Write 1 to clear)	
	CHECKSUM_ERR	2	Checksum error occurred; packet discarded. (Write 1 to clear)	
	BCHPRTY_ERR	1	BCH parity error occurred; packet discarded. (Write 1 to clear)	
	BCHERR_CORRECTED	0	Single bit BCH parity error occurred and corrected. (Write 1 to clear)	
04h (2709h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
05h (270Ah)	**HDMI_PLL_STS**	7:0	**Default : -**	**Access : RO**
	-	7:3	Reserved.	
	HDMI_PLL_LCK_RAW	2	HDMI PLL locks raw flag.	
	HDMI_PLL_HI_FLAG	1	HDMI PLL output flag for VCO supply voltage too high.	
	HDMI_PLL_LCK	0	HDMI PLL locks flag. Set REG_CLK_CFG[5] (0x2CAE[14]) to enable this status output.	
05h (270Bh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
06h (270Ch)	**HDMI_CONFIG1**	7:0	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	

HDMI Register (Bank = 27h)

Index (Absolute)	Mnemonic	Bit	Description	
	RST_CTS_FIFO	6	Reset CTS FIFO. 0: No action. 1: Reset.	
	AFIFO_TH	5:4	Audio FIFO start operation threshold. 00: Immediately. 01: After 1/4 fullness. 10: After 1/2 fullness. 11: After 3/4 fullness.	
	-	3:2	Reserved.	
	ENUSRPKT	1	Enable User Specified Packet based on header type defined at PKTTYPE register.	
	-	0	Reserved.	
06h ~ 08h (270Dh ~ 2711h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
09h (2712h)	**HDMI_CONFIG4_L**	7:0	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	AFIFORST	6	Reset Audio FIFO/ (clear FIFO contents); all channels. 0: Normal. 1: Reset audio FIFO.	
	ENVMUTE	5	Enable Video mute. 0: No video mute. 1: Mute video display when AVMUTE signal is received.	
	ENVMUTEBLANK	4	Blank display during AVMUTE 0: Picture is frozen during AVMUTE. 1: Blank picture is shown during AVMUTE.	
	EN_HDMI_AUTOEN	3	Enable HDMI/DVI mode detection. 0: HDMI/DVI mode is set by F/W. 1: HDMI/DVI mode is detected by hardware automatically.	
	-	2	Reserved.	
	-	1	Reserved.	
	-	0	Reserved.	
09h (2713h)	**HDMI_CONFIG4_H**	7:0	**Default : 0x00**	**Access : R/W**
	MAN_AP_SEL	7	Manual adjust phase select. 0: Write MANUAL_ADJUST_PHASE bit to shift one phase.	

HDMI Register (Bank = 27h)

Index (Absolute)	Mnemonic	Bit	Description	
			1: Adjust phase by default phase.	
	MAN_ADJ_PHASE	6	Write this bit to trigger an action of phase adjustment. It will shift one phase; only valid when EN_DEEP_COLOR=1.	
	DIS_NO_GCP_QUIT	5	Disable the function that if the sink does not receive a GCP with non-zero CD for more than 4 consecutive video fields, it should exit deep color mode. 0: Enable. 1: Disable.	
	REG_MAN_CD	4:3	Manual deep color depth. These bits are valid only if EN_DEEP_COLOR = 1. 00: Disable. 01: 30 bits. 10: 36 bits. 11: Reserved.	
	EN_DF_ADJ	2	Enable adjust phase by default phase in deep color mode. 0: Disable. 1: Enable.	
	AUTO_RST_DC_FIFO	1	Auto reset deep color FIFO if overflow or underflow occurs. 0: Disable. 1: Enable.	
	EN_DEEP_COLOR	0	Enable deep color mode. 0: Disable. 1: Enable.	
0Ah (2714h)	HDMI_CLK_CFG	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	HDMI_PLL_DCLK_INV	3	Invert HDMI audio PLL DCLK clock. 0: Normal. 1: Invert.	
	HDMI_PLL_DCLK_EN	2	Enable HDMI audio PLL DCLK clock. 0: Disable. 1: Enable.	
	HDMI_PLL_FBCLK_INV	1	Invert HDMI audio PLL FBCLK clock. 0: Normal. 1: Invert.	

HDMI Register (Bank = 27h)

Index (Absolute)	Mnemonic	Bit	Description	
	HDMI_PLL_FBCLK_EN	0	Enable HDMI audio PLL FBCLK clock. 0: Disable. 1: Enable.	
0Ah ~ 0Bh (2715h ~ 2717h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
0Ch (2718h)	FREQ_CMPVAL1_L	7:0	Default : 0x15	Access : R/W
	CMPVAL50[7:0]	7:0	50MHz count value; for pixel frequency detection; low byte.	
0Ch (2719h)	FREQ_CMPVAL1_H	7:0	Default : 0x02	Access : R/W
	CMPVAL50[15:8]	7:0	100MHz count value; for pixel frequency detection; low byte.	
0Dh (271Ah)	FREQ_CMPVAL2_L	7:0	Default : 0x04	Access : R/W
	CMPVAL100[7:0]	7:0	100MHz count value; for pixel frequency detection; high byte.	
0Dh (271Bh)	FREQ_CMPVAL2_H	7:0	Default : 0x04	Access : R/W
	CMPVAL100[15:8]	7:0	100MHz count value; for pixel frequency detection; low byte.	
0Eh (271Ch)	FREQ_CMPVAL3_L	7:0	Default : 0x55	Access : R/W
	CMPVAL200[7:0]	7:0	200MHz count value; for pixel frequency detection; low byte.	
0Eh (271Dh)	FREQ_CMPVAL3_H	7:0	Default : 0x08	Access : R/W
	CMPVAL200[15:8]	7:0	200MHz count value; for pixel frequency detection; high byte.	
0Fh (271Eh ~ 271Fh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
10h (2720h)	PKT_TYPE	7:0	Default : -	Access : RO
	PKT_TYPE[7:0]	7:0	Used for vendor specific packet capture.	
10h (2721h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
10h (2720h)	PCLK_FREQ_L	7:0	Default : -	Access : RO
	CNT_VAL[7:0]	7:0	Counter outputs plus overflow.	
10h (2721h)	PCLK_FREQ_H	7:0	Default : -	Access : RO
	AUPLL_LOCK	7	Audio PLL lock status.	

HDMI Register (Bank = 27h)

Index (Absolute)	Mnemonic	Bit	Description	
	FIN[1:0]	6:5	PIXCLK frequency. 00: Frequency < 50MHz. 01: Frequency = 50 ~ 100MHz. 10: Frequency = 100 ~ 200MHz. 11: Frequency > 200MHz.	
	CNT_VAL[12:8]	4:0	Counter outputs plus overflow.	
12h (2724h)	**AUDIO_CLK0_L**	**7:0**	**Default : 0x1A**	**Access : R/W**
	CTS[7:0]	7:0	CTS value received from audio clock regeneration packet; write this register to load CTS and N values.	
12h (2725h)	**AUDIO_CLK0_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	CTS[15:8]	7:0	See description for CTS[7:0].	
13h (2726h)	**AUDIO_CLK1_L**	**7:0**	**Default : -**	**Access : RO**
	N[7:0]	7:0	N value received from audio clock regeneration packet.	
13h (2727h)	**AUDIO_CLK1_H**	**7:0**	**Default : -**	**Access : RO**
	N[15:8]	7:0	See description for N[7:0].	
14h (2728h)	**AUDIO_CLK2**	**7:0**	**Default : -**	**Access : RO**
	N[19:16]	7:4	See description for N[7:0].	
	CTS[19:16]	3:0	See description for CTS[7:0].	
14h (2729h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
15h (272Ah)	**GCONTROL_L**	**7:0**	**Default : -**	**Access : RO**
	-	7:5	Reserved.	
	LAST_PP	4:2	Reflects RX last packing phase for each video period. 000: Phase 0 (10P0, 12P0, 16P0) 001: Phase 1 (10P1, 12P1, 16P1) 010: Phase 2 (10P2, 12P2) 011: Phase 3 (10P3) 100: Phase 4 (10P4) 101~111: Reversed	
	DEFAULT_PHASE	1	DEFAULT_PHASE in GCP sub-packet byte 2.	
	AVMUTE	0	AVMUTE received from general control packet or written by MCU. 0: Clear AVMUTE. 1: Set AVMUTE.	
15h	**GCONTROL_H**	**7:0**	**Default : -**	**Access : RO**

HDMI Register (Bank = 27h)

Index (Absolute)	Mnemonic	Bit	Description	
(272Bh)	PP_VAL[3:0]	7:4	Pixel packing phase in GCP sub-packet byte 1.	
	CD_VAL[3:0]	3:0	Color depth in GCP sub-packet byte 1.	
16h (272Ch)	ACP_HB1	7:0	Default : -	Access : RO
	ACP_TYPE[7:0]	7:0	Content protection type field from Audio Content Protection (ACP) packet. Header byte 1. 0x00: Generic Audio. 0x01: IEC 60958-Identified Audio. 0x02: DVD-Audio. 0x03: Reserved for Super Audio CD (SACD). 0x04~0xFF: Reserved.	
16h (272Dh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
17h (272Eh)	ACP_DATA0_L	7:0	Default : -	Access : RO
	ACP_0	7:0	ACP byte 0.	
17h (272Fh)	ACP_DATA0_H	7:0	Default : -	Access : RO
	ACP_1	7:0	ACP packet payload ACP_DATA0 to ACP_DATA15; ACP byte 1.	
18h (2730h)	ACP_DATA1_L	7:0	Default : -	Access : RO
	ACP_2	7:0	ACP byte 2.	
18h (2731h)	ACP_DATA1_H	7:0	Default : -	Access : RO
	ACP_3	7:0	ACP byte 3.	
19h (2732h)	ACP_DATA2_L	7:0	Default : -	Access : RO
	ACP_4	7:0	ACP byte 4.	
19h (2733h)	ACP_DATA2_H	7:0	Default : -	Access : RO
	ACP_5	7:0	ACP byte 5.	
1Ah (2734h)	ACP_DATA3_L	7:0	Default : -	Access : RO
	ACP_6	7:0	ACP byte 6.	
1Ah (2735h)	ACP_DATA3_H	7:0	Default : -	Access : RO
	ACP_7	7:0	ACP byte 7.	
1Bh (2736h)	ACP_DATA4_L	7:0	Default : -	Access : RO
	ACP_8	7:0	ACP byte 8.	
1Bh (2737h)	ACP_DATA4_H	7:0	Default : -	Access : RO
	ACP_9	7:0	ACP byte 9.	

HDMI Register (Bank = 27h)

Index (Absolute)	Mnemonic	Bit	Description	
1Ch (2738h)	**ACP_DATA5_L**	**7:0**	**Default : -**	**Access : RO**
	ACP_10	7:0	ACP byte 10.	
1Ch (2739h)	**ACP_DATA5_H**	**7:0**	**Default : -**	**Access : RO**
	ACP_11	7:0	ACP byte 11.	
1Dh (273Ah)	**ACP_DATA6_L**	**7:0**	**Default : -**	**Access : RO**
	ACP_12	7:0	ACP byte 12.	
1Dh (273Bh)	**ACP_DATA6_H**	**7:0**	**Default : -**	**Access : RO**
	ACP_13	7:0	ACP byte 13.	
1Eh (273Ch)	**ACP_DATA7_L**	**7:0**	**Default : -**	**Access : RO**
	ACP_14	7:0	ACP byte 14.	
1Eh (273Dh)	**ACP_DATA7_H**	**7:0**	**Default : -**	**Access : RO**
	ACP_15	7:0	ACP byte 15.	
1Fh (273Eh)	**ISRC_HB1**	**7:0**	**Default : -**	**Access : RO**
	ISRC_CONR	7	ISRC continued.	
	ISRC_VALID	6	ISRC valid.	
	-	5:3	Reserved.	
	ISRC_STS[2:0]	2:0	ISRC status. 001: Starting position. 010: Intermediate position. 100: Ending position.	
1Fh (273Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
20h (2740h)	**ISRC_DATA0_L**	**7:0**	**Default : -**	**Access : RO**
	UPC_EAN_ISRC_0	7:0	UPC/EAN or ISRC byte 0.	
20h (2741h)	**ISRC_DATA0_H**	**7:0**	**Default : -**	**Access : RO**
	UPC_EAN_ISRC_1	7:0	UPC/EAN or ISRC byte 1.	
21h (2742h)	**ISRC_DATA1_L**	**7:0**	**Default : -**	**Access : RO**
	UPC_EAN_ISRC_2	7:0	UPC/EAN or ISRC byte 2.	
21h (2743h)	**ISRC_DATA1_H**	**7:0**	**Default : -**	**Access : RO**
	UPC_EAN_ISRC_3	7:0	UPC/EAN or ISRC byte 3.	
22h (2744h)	**ISRC_DATA2_L**	**7:0**	**Default : -**	**Access : RO**
	UPC_EAN_ISRC_4	7:0	UPC/EAN or ISRC byte 4.	
22h	**ISRC_DATA2_H**	**7:0**	**Default : -**	**Access : RO**

HDMI Register (Bank = 27h)

Index (Absolute)	Mnemonic	Bit	Description	
(2745h)	UPC_EAN_ISRC_5	7:0	UPC/EAN or ISRC byte 5.	
23h	ISRC_DATA3_L	7:0	Default : -	Access : RO
(2746h)	UPC_EAN_ISRC_6	7:0	UPC/EAN or ISRC byte 6.	
23h	ISRC_DATA3_H	7:0	Default : -	Access : RO
(2747h)	UPC_EAN_ISRC_7	7:0	UPC/EAN or ISRC byte 7.	
24h	ISRC_DATA4_L	7:0	Default : -	Access : RO
(2748h)	UPC_EAN_ISRC_8	7:0	UPC/EAN or ISRC byte 8.	
24h	ISRC_DATA4_H	7:0	Default : -	Access : RO
(2749h)	UPC_EAN_ISRC_9	7:0	UPC/EAN or ISRC byte 9.	
25h	ISRC_DATA5_L	7:0	Default : -	Access : RO
(274Ah)	UPC_EAN_ISRC_10	7:0	UPC/EAN or ISRC byte 0.	
25h	ISRC_DATA5_H	7:0	Default : -	Access : RO
(274Bh)	UPC_EAN_ISRC_11	7:0	UPC/EAN or ISRC byte 11.	
26h	ISRC_DATA6_L	7:0	Default : -	Access : RO
(274Ch)	UPC_EAN_ISRC_12	7:0	UPC/EAN or ISRC byte 12.	
26h	ISRC_DATA6_H	7:0	Default : -	Access : RO
(274Dh)	UPC_EAN_ISRC_13	7:0	UPC/EAN or ISRC byte 13.	
27h	ISRC_DATA7_L	7:0	Default : -	Access : RO
(274Eh)	UPC_EAN_ISRC_14	7:0	UPC/EAN or ISRC byte 14.	
27h	ISRC_DATA7_H	7:0	Default : -	Access : RO
(274Fh)	UPC_EAN_ISRC_15	7:0	UPC/EAN or ISRC byte 15.	
28h	ISRC_DATA8_L	7:0	Default : -	Access : RO
(2750h)	UPC_EAN_ISRC_16	7:0	UPC/EAN or ISRC byte 16.	
28h	ISRC_DATA8_H	7:0	Default : -	Access : RO
(2751h)	UPC_EAN_ISRC_17	7:0	UPC/EAN or ISRC byte 17.	
29h	ISRC_DATA9_L	7:0	Default : -	Access : RO
(2752h)	UPC_EAN_ISRC_18	7:0	UPC/EAN or ISRC byte 18.	
29h	ISRC_DATA9_H	7:0	Default : -	Access : RO
(2753h)	UPC_EAN_ISRC_19	7:0	UPC/EAN or ISRC byte 19.	
2Ah	ISRC_DATA10_L	7:0	Default : -	Access : RO
(2754h)	UPC_EAN_ISRC_20	7:0	UPC/EAN or ISRC byte 20.	
2Ah	ISRC_DATA10_H	7:0	Default : -	Access : RO

HDMI Register (Bank = 27h)

Index (Absolute)	Mnemonic	Bit	Description	
(2755h)	UPC_EAN_ISRC_21	7:0	UPC/EAN or ISRC byte 21.	
2Bh (2756h)	ISRC_DATA11_L	7:0	Default : -	Access : RO
	UPC_EAN_ISRC_22	7:0	UPC/EAN or ISRC byte 22.	
2Bh (2757h)	ISRC_DATA11_H	7:0	Default : -	Access : RO
	UPC_EAN_ISRC_23	7:0	UPC/EAN or ISRC byte 23.	
2Ch (2758h)	ISRC_DATA12_L	7:0	Default : -	Access : RO
	UPC_EAN_ISRC_24	7:0	UPC/EAN or ISRC byte 24.	
2Ch (2759h)	ISRC_DATA12_H	7:0	Default : -	Access : RO
	UPC_EAN_ISRC_25	7:0	UPC/EAN or ISRC byte 25.	
2Dh (275Ah)	ISRC_DATA13_L	7:0	Default : -	Access : RO
	UPC_EAN_ISRC_26	7:0	UPC/EAN or ISRC byte 26.	
2Dh (275Bh)	ISRC_DATA13_H	7:0	Default : -	Access : RO
	UPC_EAN_ISRC_27	7:0	UPC/EAN or ISRC byte 27.	
2Eh (275Ch)	ISRC_DATA14_L	7:0	Default : -	Access : RO
	UPC_EAN_ISRC_28	7:0	UPC/EAN or ISRC byte 28.	
2Eh (275Dh)	ISRC_DATA14_H	7:0	Default : -	Access : RO
	UPC_EAN_ISRC_29	7:0	UPC/EAN or ISRC byte 29.	
2Fh (275Eh)	ISRC_DATA15_L	7:0	Default : -	Access : RO
	UPC_EAN_ISRC_30	7:0	UPC/EAN or ISRC byte 30.	
2Fh (275Fh)	ISRC_DATA15_H	7:0	Default : -	Access : RO
	UPC_EAN_ISRC_31	7:0	UPC/EAN or ISRC byte 31.	
30h (2760h)	VS_HDR0_L	7:0	Default : -	Access : RO
	VS_HDR0[7:0]	7:0	Vender specific packet header byte 0.	
30h (2761h)	VS_HDR0_H	7:0	Default : -	Access : RO
	VS_HDR1[7:0]	7:0	Vender specific packet header byte 1.	
31h (2762h)	VS_HDR1	7:0	Default : -	Access : RO
	VS_HDR2[7:0]	7:0	Vender specific packet header byte 2.	
31h (2763h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
32h (2764h)	VS_IF0_L	7:0	Default : -	Access : RO
	PB0[7:0]	7:0	Vender specific InfoFrame packet payload data port VS_IF0~VS_IF13.	

HDMI Register (Bank = 27h)

Index (Absolute)	Mnemonic	Bit	Description	
			Payload byte 0 – Check sum.	
32h (2765h)	VS_IF0_H	7:0	Default : -	Access: RO
	PB1[7:0]	7:0	Payload byte 1 – IEEE registration ID[7:0].	
33h (2766h)	VS_IF1_L	7:0	Default : -	Access: RO
	PB2[7:0]	7:0	Payload byte 2 – IEEE registration ID[15:8].	
33h (2767h)	VS_IF1_H	7:0	Default : -	Access: RO
	PB3[7:0]	7:0	Payload byte 3 – IEEE registration ID[23:16].	
34h (2768h)	VS_IF2_L	7:0	Default : -	Access: RO
	PB4[7:0]	7:0	Payload byte 4.	
34h (2769h)	VS_IF2_H	7:0	Default : -	Access: RO
	PB5[7:0]	7:0	Payload byte 5.	
35h (276Ah)	VS_IF3_L	7:0	Default : -	Access: RO
	PB6[7:0]	7:0	Payload byte 6.	
35h (276Bh)	VS_IF3_H	7:0	Default : -	Access: RO
	PB7[7:0]	7:0	Payload byte 7.	
36h (276Ch)	VS_IF4_L	7:0	Default : -	Access: RO
	PB8[7:0]	7:0	Payload byte 8.	
36h (276Dh)	VS_IF4_H	7:0	Default : -	Access: RO
	PB9[7:0]	7:0	Payload byte 9.	
37h (276Eh)	VS_IF5_L	7:0	Default : -	Access: RO
	PB10[7:0]	7:0	Payload byte 10.	
37h (276Fh)	VS_IF5_H	7:0	Default : -	Access: RO
	PB11[7:0]	7:0	Payload byte 11.	
38h (2770h)	VS_IF6_L	7:0	Default : -	Access: RO
	PB12[7:0]	7:0	Payload byte 12.	
38h (2771h)	VS_IF6_H	7:0	Default : -	Access: RO
	PB13[7:0]	7:0	Payload byte 13.	
39h (2772h)	VS_IF7_L	7:0	Default : -	Access: RO
	PB14[7:0]	7:0	Payload byte 14.	
39h (2773h)	VS_IF7_H	7:0	Default : -	Access: RO
	PB15[7:0]	7:0	Payload byte 15.	
3Ah	VS_IF8_L	7:0	Default : -	Access: RO

HDMI Register (Bank = 27h)

Index (Absolute)	Mnemonic	Bit	Description	
(2774h)	PB16[7:0]	7:0	Payload byte 16.	
3Ah (2775h)	VS_IF8_H	7:0	Default : -	Access: RO
	PB17[7:0]	7:0	Payload byte 17.	
3Bh (2776h)	VS_IF9_L	7:0	Default : -	Access: RO
	PB18[7:0]	7:0	Payload byte 18.	
3Bh (2777h)	VS_IF9_H	7:0	Default : -	Access: RO
	PB19[7:0]	7:0	Payload byte 19.	
3Ch (2778h)	VS_IF10_L	7:0	Default : -	Access: RO
	PB20[7:0]	7:0	Payload byte 20.	
3Ch (2779h)	VS_IF10_H	7:0	Default : -	Access: RO
	PB21[7:0]	7:0	Payload byte 21.	
3Dh (277Ah)	VS_IF11_L	7:0	Default : -	Access: RO
	PB22[7:0]	7:0	Payload byte 22.	
3Dh (277Bh)	VS_IF11_H	7:0	Default : -	Access: RO
	PB23[7:0]	7:0	Payload byte 23.	
3Eh (277Ch)	VS_IF12_L	7:0	Default : -	Access: RO
	PB24[7:0]	7:0	Payload byte 24.	
3Eh (277Dh)	VS_IF12_H	7:0	Default : -	Access: RO
	PB25[7:0]	7:0	Payload byte 25.	
3Fh (277Eh)	VS_IF13_L	7:0	Default : -	Access: RO
	PB26[7:0]	7:0	Payload byte 26.	
3Fh (277Fh)	VS_IF13_H	7:0	Default : -	Access: RO
	PB27[7:0]	7:0	Payload byte 27.	
40h (2780h)	AVI_IF0_L	7:0	Default : -	Access : RO
	VERSION	7	Version. 0: Version 1. 1: Version 2.	
	Y[1:0]	6:5	RGB or YCbCr. 00: RGB. 01: YCbCr 4:2:2. 10: YCbCr 4:4:4. 11: Reserved.	
	A	4	Active format info present. 0: No Data.	

HDMI Register (Bank = 27h)

Index (Absolute)	Mnemonic	Bit	Description	
			1: Active Format Information Active.	
	B[1:0]	3:2	Bar info. 00: Bar Data not valid. 01: Vertical Bar information valid. 10: Horizontal Bar information valid. 11: Vertical and Horizontal Bar information valid.	
	S[1:0]	1:0	Scan info. 00: No data. 01: Over-scanned (television). 10: Under-scanned (computer). 11: Reserved.	
40h (2781h)	AVI_IF0_H	7:0	Default : -	Access : RO
	C[1:0]	7:6	Colorimetry. 00: No data. 01: SMPTE 170M or ITU601. 10: ITU709. 11: Reserved.	
	M[1:0]	5:4	Picture aspect ratio. 00: No data. 01: 4:3. 10: 16:9. 11: Reserved.	
	R[3:0]	3:0	Active format aspect ratio. 1000: Same as picture aspect ratio. 1001: 4:3 (Center). 1010: 16:9 (Center). 1011: 14:9 (Center). Other values: Per DVB AFD active_format field in DVB specification.	
41h (2782h)	AVI_IF1_L	7:0	Default : -	Access : RO
	ITC	7	IT content.	
	EC[2:0]	6:4	Extended colorimetry.	
	Q[1:0]	3:2	Quantization range.	
	SC[1:0]	1:0	Non-conforming picture scaling. 00: No known non-uniform scaling. 01: Picture has been scaled horizontally. 10: Picture has been scaled vertically.	

HDMI Register (Bank = 27h)

Index (Absolute)	Mnemonic	Bit	Description	
			11: Picture has been scaled horizontally and vertically.	
41h (2783h)	**AVI_IF1_H**	7:0	Default : -	Access : RO
	-	7	Reserved.	
	VIC[6:0]	6:0	Video identification code; refer to EIA/CEA 861B specification.	
42h (2784h)	**AVI_IF2_L**	7:0	Default : -	Access : RO
	-	7:4	Reserved.	
	PR[3:0]	3:0	Pixel repetition; pixel sent (PR+1) times.	
42h (2785h)	**AVI_IF2_L**	7:0	Default : -	Access : RO
	LNTOP[7:0]	7:0	Line number of end of the top bar.	
43h (2786h)	**AVI_IF3_L**	7:0	Default : -	Access: RO
	LNTOP[15:8]	7:0	See description for LNTOP[7:0].	
43h (2787h)	**AVI_IF3_H**	7:0	Default : -	Access: RO
	LNBOT[7:0]	7:0	Line number of start of bottom bar.	
44h (2788h)	**AVI_IF4_L**	7:0	Default : -	Access: RO
	LNBOT[15:8]	7:0	See description for LNBOT[7:0].	
44h (2789h)	**AVI_IF4_H**	7:0	Default : -	Access: RO
	PNLEFT[7:0]	7:0	Pixel number of end of left bar.	
45h (278Ah)	**AVI_IF5_L**	7:0	Default : -	Access: RO
	PNLEFT[15:8]	7:0	See description for PNLEFT[7:0].	
45h (278Bh)	**AVI_IF5_H**	7:0	Default : -	Access: RO
	PNRIGHT[7:0]	7:0	Pixel number of end of right bar.	
46h (278Ch)	**AVI_IF6_L**	7:0	Default : -	Access: RO
	PNRIGHT[15:8]	7:0	See description for PNRIGHT[7:0].	
46h (278Dh)	-	7:0	Default : -	Access: -
	-	7:0	Reserved.	
47h (278Eh)	**SPD_IF0_L**	7:0	Default : -	Access : RO
	-	7	Reserved.	
	VN1[6:0]	6:0	Vendor name character 1.	
47h (278Fh)	**SPD_IF0_H**	7:0	Default : -	Access : RO
	-	7	Reserved.	
	VN2[6:0]	6:0	Vendor name character 2.	
48h	**SPD_IF1_L**	7:0	Default : -	Access : RO

HDMI Register (Bank = 27h)

Index (Absolute)	Mnemonic	Bit	Description	
(2790h)	-	7	Reserved.	
	VN3[6:0]	6:0	Vendor name character 3.	
48h (2791h)	SPD_IF1_H	7:0	Default : -	Access : RO
	-	7	Reserved.	
	VN4[6:0]	6:0	Vendor name character 4.	
49h (2792h)	SPD_IF2_L	7:0	Default : -	Access : RO
	-	7	Reserved.	
	VN5[6:0]	6:0	Vendor name character 5.	
49h (2793h)	SPD_IF2_H	7:0	Default : -	Access : RO
	-	7	Reserved.	
	VN6[6:0]	6:0	Vendor name character 6.	
4Ah (2794h)	SPD_IF3_L	7:0	Default : -	Access : RO
	-	7	Reserved.	
	VN7[6:0]	6:0	Vendor name character 7.	
4Ah (2795h)	SPD_IF3_H	7:0	Default : -	Access : RO
	-	7	Reserved.	
	VN8[6:0]	6:0	Vendor name character 8.	
4Bh (2796h)	SPD_IF4_L	7:0	Default : -	Access : RO
	-	7	Reserved.	
	PD1[6:0]	6:0	Product description character 1.	
4Bh (2797h)	SPD_IF4_H	7:0	Default : -	Access : RO
	-	7	Reserved.	
	PD2[6:0]	6:0	Product description character 2.	
4Ch (2798h)	SPD_IF5_L	7:0	Default : -	Access : RO
	-	7	Reserved.	
	PD3[6:0]	6:0	Product description character 3.	
4Ch (2799h)	SPD_IF5_H	7:0	Default : -	Access : RO
	-	7	Reserved.	
	PD4[6:0]	6:0	Product description character 4.	
4Dh (279Ah)	SPD_IF6_L	7:0	Default : -	Access : RO
	-	7	Reserved.	
	PD5[6:0]	6:0	Product description character 5.	

HDMI Register (Bank = 27h)

Index (Absolute)	Mnemonic	Bit	Description	
4Dh (279Bh)	SPD_IF6_H	7:0	Default : -	Access : RO
	-	7	Reserved.	
	PD6[6:0]	6:0	Product description character 6.	
4Eh (279Ch)	SPD_IF7_L	7:0	Default : -	Access : RO
	-	7	Reserved.	
	PD7[6:0]	6:0	Product description character 7.	
4Eh (279Dh)	SPD_IF7_H	7:0	Default : -	Access : RO
	-	7	Reserved.	
	PD8[6:0]	6:0	Product description character 8.	
4Fh (279Eh)	SPD_IF8_L	7:0	Default : -	Access : RO
	-	7	Reserved.	
	PD9[6:0]	6:0	Product description character 9.	
4Fh (279Fh)	SPD_IF8_H	7:0	Default : -	Access : RO
	-	7	Reserved.	
	PD10[6:0]	6:0	Product description character 10.	
50h (27A0h)	SPD_IF9_L	7:0	Default : -	Access : RO
	-	7	Reserved.	
	PD11[6:0]	6:0	Product description character 11.	
50h (27A1h)	SPD_IF9_H	7:0	Default : -	Access : RO
	-	7	Reserved.	
	PD12[6:0]	6:0	Product description character 12.	
51h (27A2h)	SPD_IF10_L	7:0	Default : -	Access : RO
	-	7	Reserved.	
	PD13[6:0]	6:0	Product description character 13.	
51h (27A3h)	SPD_IF10_H	7:0	Default : -	Access : RO
	-	7	Reserved.	
	PD14[6:0]	6:0	Product description character 14.	
52h (27A4h)	SPD_IF11_L	7:0	Default : -	Access : RO
	-	7	Reserved.	
	PD15[6:0]	6:0	Product description character 15.	
52h (27A5h)	SPD_IF11_H	7:0	Default : -	Access : RO
	-	7	Reserved.	

HDMI Register (Bank = 27h)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	PD16[6:0]	6:0	Product description character 16.
53h (27A6h)	**SPD_IF12**	**7:0**	**Default : -**	**Access : RO**
	SDI[7:0]	7:0	Source device information.
53h (27A7h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.
54h (27A8h)	**AUDIO_IF0_L**	**7:0**	**Default : -**	**Access: RO**
	CT[3:0]	7:4	Audio coding type. 0000: Refer to stream header. 0001: IEC60958 PCM. 0010: AC-3. 0011: MPEG1 (Layers 1&2). 0100: MP3 (MPEG1 Layer 3). 0101: MPEG2 (multichannel). 0110: AAC. 0111: DTS. 1000: ATRAC. Other values: Reserved.
	-	3	Reserved.
	CC[2:0]	2:0	Audio channel count. 000: Refer to stream header. 001: 2 channels. 010: 3 channels. 011: 4 channels. 100: 5 channels. 101: 6 channels. 110: 7 channels. 111: 8 channels.
54h (27A9h)	**AUDIO_IF0_H**	**7:0**	**Default : -**	**Access : RO**
	-	7:5	Reserved.
	SF[2:0]	4:2	Sampling frequency. 000: Refer to stream header. 001: 32 kHz. 010: 44.1 kHz (CD). 011: 48 kHz. 100: 88.2 kHz. 101: 96 kHz. 110: 176.4 kHz.

HDMI Register (Bank = 27h)

Index (Absolute)	Mnemonic	Bit	Description	
			111: 192 kHz.	
	SS[1:0]	1:0	Sample size. 00: Refer to stream header. 01: 16-bit. 10: 20-bit. 11: 24-bit.	
55h (27AAh)	AUDIO_IF1_L	7:0	Default : -	Access : RO
	MBR[7:0]	7:0	Max bit rate depending on coding type.	
55h (27ABh)	AUDIO_IF1_H	7:0	Default : -	Access : RO
	CA[7:0]	7:0	Channel allocation; refer to EIA/CEA 861B specification.	
56h (27ACh)	AUDIO_IF2	7:0	Default : -	Access : RO
	DM_INH	7	Down-mix inhibit flag. 0: Permitted or no information about any assertion of this. 1: Prohibited.	
	LSV[3:0]	6:3	Level shift value; LSV dB.	
	-	2:0	Reserved.	
56h (27ADh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
57h (27AEh)	MPEG_IF0_L	7:0	Default : -	Access : RO
	MB[7:0]	7:0	MPEG Source InfoFrame packet MPEG_IF0~MPEG_IF2. MPEG Bit Rate.	
57h (27AFh)	MPEG_IF0_H	7:0	Default : -	Access : RO
	MB[15:8]	7:0	See description of MB[7:0].	
58h (27B0h)	MPEG_IF1_L	7:0	Default : -	Access : RO
	MB[23:16]	7:0	See description of MB[7:0].	
58h (27B1h)	MPEG_IF1_H	7:0	Default : -	Access : RO
	MB[31:24]	7:0	See description of MB[7:0].	
59h (27B2h)	MPEG_IF2	7:0	Default : -	Access : RO
	-	7:5	Reserved.	
	MPG_FR	4	MPEG field repeat (for 3:2 pull-down).	
	-	3:2	Reserved.	
	MF[1:0]	1:0	MPEG frame.	
59h	-	7:0	Default : -	Access : -

HDMI Register (Bank = 27h)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
(27B3h)	-	7:0	Reserved.
5Ah (27B4h)	**HDMI_CS0_L**	**7:0**	**Default : -**	**Access : RO**
	HDMI_CS[7:0]	7:0	HDMI audio channel status.
5Ah (27B5h)	**HDMI_CS0_H**	**7:0**	**Default : -**	**Access : RO**
	HDMI_CS[15:8]	7:0	See description of HDMI_CS[7:0].
5Bh (27B6h)	**HDMI_CS1_L**	**7:0**	**Default : -**	**Access : RO**
	HDMI_CS[23:16]	7:0	See description of HDMI_CS[7:0].
5Bh (27B7h)	**HDMI_CS1_H**	**7:0**	**Default : -**	**Access : RO**
	HDMI_CS[31:24]	7:0	See description of HDMI_CS[7:0].
5Ch (27B8h)	**HDMI_CS2**	**7:0**	**Default : -**	**Access : RO**
	HDMI_CS[31:24]	7:0	See description of HDMI_CS[7:0].
5Ch (27B9h)	-	7:0	**Default : -**	**Access : -**
	-	7:0	Reserved.
5Dh (27BAh)	**HDMI_PLL_CTRL1_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAN_PLL_DIV	7	Enable PLL divider controlled by registers. 0: Disable. 1: Enable.
	PLL_PORST	6	HDMI audio PLL reset. 0: Normal. 1: Reset (all analog front-end and dividers).
	RESET_TP	5	HDMI PLL post clock divider reset (KP). 0: Normal. 1: Reset.
	RESET_TF	4	HDMI PLL feedback clock divider reset (FBDIV & KM). 0: Normal. 1: Reset.
	RESET_TI	3	HDMI PLL input clock divider reset (DDIV & KN). 0: Normal. 1: Reset.
	VCO_OFFSET	2	Enable VCO free running. 0: Enable. 1: Disable.
	PLL_RESET	1	PLL reset. 0: No reset. 1: Reset.

HDMI Register (Bank = 27h)

Index (Absolute)	Mnemonic	Bit	Description	
	PWRDOWN	0	HDMI PLL power down. 0: No action. 1: Power down.	
5Dh (27BBh)	HDMI_PLL_CTRL1_H	7:0	Default : 0x09	Access : R/W
	KN[1:0]	7:6	HDMI PLL KN divider ratio for new mode. 00: /1. 01: /2. 10: /4. 11: /4.	
	RCTRL	5:3	HDMI PLL loop filter resistor control. 000: 23.1K ohm. 001: 26.4K ohm. 010: 29.7K ohm. ….. 111: 42.9K ohm.	
	ICTRL	2:0	HDMI PLL charge pump current control. 000: 0.65 uA. 001: 1.29 uA. 010: 1.935 uA. 011: 2.58 uA. 100: 3.225 uA. 101: 3.87 uA. 110: 5.16 uA. 111: 10.32 uA.	
5Eh (27BCh)	HDMI_PLL_CTRL2_L	7:0	Default : 0x31	Access : R/W
	KP[3:0]	7:4	HDMI PLL Post divider ratio (KP) for new mode. 0000: / 1. 0001: / 2. 0010: / 4. .... 1001: / 512. 1010: / 1024. 1011: / 1024. .... 1111: / 1024.	
	KM[3:0]	3:0	HDMI PLL KM divider ratio for new mode. 0000: /1. 0001: /2.	

HDMI Register (Bank = 27h)

Index (Absolute)	Mnemonic	Bit	Description	
			0010: /4. .... 1001: / 128. 1010: / 256. 1011: / 256. .... 1111: / 256.	
5Eh (27BDh)	HDMI_PLL_CTRL2_H	7:0	Default : 0x22	Access : R/W
	DDIV[3:0]	7:4	HDMI PLL input over-write divider value from noise-shape quantizer for new mode. 0000: N.A. (/16). 0001: N.A. (/17). 0010: /2. 0011: /3. .... 1111: /15.	
	FBDIV[3:0]	3:0	HDMI PLL feedback overwrite divider value from noise-shape quantizer for new mode. 0000: N.A. (/16). 0001: N.A. (/17). 0010: /2. 0011: /3. .... 1111: /15.	
5Fh (27BEh 27BFh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
60h (27C0h)	INT_MSK_L	7:0	Default : 0x00	Access : R/W
	INT_CEC_RX_MSK	7	Mask CEC interrupt that message is received successfully. 0: Unmask. 1: Mask.	
	INT_BCHERR_MSK	6	Mask BCH error interrupt. 0: Unmask (generate an interrupt when a BCH error occurs). 1: Mask.	
	INT_ISRC_MSK	5	Mask ISRC packet reception update interrupt. 0: Unmask (generate an interrupt when a new ISRC	

HDMI Register (Bank = 27h)

Index (Absolute)	Mnemonic	Bit	Description	
			packet is received and it is different from the previous received ISRC packet). 1: Mask.	
	INT_ACP_MSK	4	Mask ACP packet reception update interrupt. 0: Unmask (generate an interrupt when a new ACP packet is received and it is different from the previous received ACP packet). 1: Mask.	
	INT_MPG_MSK	3	Mask MPEG InfoFrame packet reception update interrupt. 0: Unmask (generate an interrupt when a new MPEG InfoFrame packet is received and it is different from the previous received MPEG InfoFrame packet). 1: Mask.	
	INT_AUD_MSK	2	Mask Audio InfoFrame packet reception update interrupt. 0: Unmask (generate an interrupt when a new Audio InfoFrame packet is received and it is different from the previous received Audio InfoFrame packet). 1: Mask.	
	INT_AVI_MSK	1	MASK AVI InfoFrame packet reception updates interrupt. 0: Unmask (generate an interrupt when a new AVI InfoFrame packet is received and it is different from the previous received AVI InfoFrame packet). 1: Mask.	
	INT_GCP_MSK	0	Mask General Control packet reception update interrupt. 0: Unmask (generate an interrupt when a new general control packet is received and it is different from the previous received general control packet). 1: Mask.	
60h (27C1h)	INT_MSK_H	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	INT_CEC_LOST_ABT_MSK	2	Mask CEC lost arbitration interrupt. 0: Unmask. 1: Mask.	
	INT_CEC_RF_MSK	1	Mask interrupt that CSC retry fail and up to the MAX times. 0: Unmask.	

HDMI Register (Bank = 27h)

Index (Absolute)	Mnemonic	Bit	Description	
			1: Mask.	
	INT_CEC_TX_MSK	0	Mask CEC interrupt that massage is sent successfully. 0: Unmask. 1: Mask.	
61h (27C2h)	**INT_STS_L**	7:0	**Default : -**	**Access : RO**
	INT_CEC_RX_STS	7	Event status for receiving a CEC message successfully.	
	INT_BCHERR_STS	6	Event status for BCH error interrupt. 0: No event. 1: Event has occurred.	
	INT_ISRC_STS	5	Event status for ISRC1/ISRC2 packet reception updates interrupt. 0: No event. 1: Event has occurred.	
	INT_ACP_STS	4	Event status for ACP packet reception updates interrupt. 0: No event. 1: Event has occurred.	
	INT_MPG_STS	3	Event status for MPEG InfoFrame packet reception updates interrupt. 0: No event. 1: Event has occurred.	
	INT_AUD_STS	2	Event status for Audio InfoFrame packet reception updates Interrupt. 0: No event. 1: Event has occurred.	
	INT_AVI_STS	1	Event status for AVI InfoFrame packet reception updates interrupt. 0: No event. 1: Event has occurred.	
	INT_GCP_STS	0	Event status for General Control packet reception updates interrupt. 0: No event. 1: Event has occurred.	
61h (27C3h)	**INT_STS_H**	7:0	**Default : -**	**Access : RO**
	-	7:3	Reserved.	
	INT_CEC_LOST_ABT	2	Event status for CEC losing arbitration to a second initiator.	

HDMI Register (Bank = 27h)

Index (Absolute)	Mnemonic	Bit	Description	
	INT_CEC_RF	1	Event status that CEC retry fail and up the MAX times. Please try the next request.	
	INT_CEC_TX_STS	0	Event status for sending a CEC message successfully.	
62h (27C4h)	**INT_FORCE_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	INT_CEC_RX_FORCE	7	Force CEC RX interrupt.	
	INT_BCHERR_FORCE	6	Force BCH error interrupt.	
	INT_ISRC_FORCE	5	Force ISRC packet reception update interrupt.	
	INT_ACP_FORCE	4	Force ACP packet reception update interrupt.	
	INT_MPG_FORCE	3	Force MPEG InfoFrame packet reception update interrupt.	
	INT_AUD_FORCE	2	Force Audio InfoFrame packet reception update interrupt.	
	INT_AVI_FORCE	1	Force AVI InfoFrame packet reception update interrupt.	
	INT_GCP_FORCE	0	Force general control packet reception update interrupt.	
62h (27C5h)	**INT_FORCE_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	INT_CEC_LOST_ABT_FORCE	2	Force CEC to lose arbitration interrupt.	
	INT_CEC_RF_FORCE	1	Force CEC to retry fail interrupt.	
	INT_CEC_TX_FORCE	0	Force the CEC TX interrupt.	
63h (27C6h)	**INT_CLEAR_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	INT_CEC_RX_CLR	7	Clear CEC RX interrupt.	
	INT_BCHERR_CLR	6	Clear BCH error interrupt.	
	INT_ISRC_CLR	5	Clear ISRC packet reception update interrupt.	
	INT_ACP_CLR	4	Clear ACP packet reception update interrupt.	
	INT_MPG_CLR	3	Clear MPEG InfoFrame packet reception update interrupt.	
	INT_AUD_CLR	2	Clear Audio InfoFrame packet reception update interrupt.	
	INT_AVI_CLR	1	Clear AVI InfoFrame packet reception update interrupt.	
	INT_GCP_CLR	0	Clear general control packet reception update interrupt.	
63h (27C7h)	**INT_CLEAR_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reversed	
	INT_CEC_LOST_ABT_CLR	2	Clear CEC lost arbitration interrupt.	

HDMI Register (Bank = 27h)

Index (Absolute)	Mnemonic	Bit	Description	
	INT_CEC_RF_CLR	1	Clear CEC retry fail interrupt.	
	INT_CEC_TX_CLR	0	Clear CEC TX interrupt.	
64h (27C8h)	**RESET_PACKET**	7:0	**Default : 0x00**	**Access : R/W**
	RESET_HDMI_STS	7	Reset HDMI status registers. Asserting this bit resets HDMI_ST[1:3], HDMI_ERR[1:2], AVI_IF[1:12], AUDIO_IF[1:5], SPD_IF[1:25], MPEG[1:5], VS_HDR[0:2], VS_IF[1:28], ACP_HB1, ACP_[0:1], ISRC_HB1, ISRC_[0:31] registers. 0: No reset. 1: Reset.	
	-	6	Reserved.	
	RESET_DC_FIFO	5	Reset deep color FIFO. 0: No reset. 1: Reset.	
	RESET_DC_VAL	4	Reset CD, PP, and default phase value of GCP packet. 0: No reset. 1: Reset.	
	-	3	Reserved.	
	RESET_PR	2	Reset pixel repetition register at AVI_IF4: PR[3:0]. 0: No reset. 1: Reset PR to 0 (no repetition).	
	RESET_COLOR	1	Reset Y (Color format) register at AVI_IF1: Y[1:0]. 0: No reset. 1: Reset PR to 00 (RGB format)	
	RESET_AVMUTE	0	Reset AVMUTE register at GCONTROL: AVMUTE. 0: No reset. 1: Reset AVMUTE to 0 (Clear AVMUTE).	
64h (27C9h)	-	7:0	**Default : -**	**Access : -**
	-	7:0	Reserved.	
65h (27CAh)	**AUTO_MD**	7:0	**Default : 0x00**	**Access : R/W**
	FRAME_RP_MD	7	Frame repetition mode. 0: Auto mode. 1: Manual mode.	
	FRAME_RP_MANUAL_VAL	6:4	Frame repetition value for manual mode. Allowed values: 1, 2, and 4.	
	AUTO_DSD	3	DSD auto detection.	

HDMI Register (Bank = 27h)

Index (Absolute)	Mnemonic	Bit	Description	
			0: Disable. 1: Enable.	
	MANUAL_DSD	2	Manual DSD. 0: Normal. 1: DSD.	
	AUTO_NPCM	1	Non-PCM auto detection. 0: Disable. 1: Enable.	
	MANUAL_NPCM	0	Manual non-PCM. 0: Normal. 1: Non-PCM.	
65h (27CBh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
66h (27CCh)	**FRAME_RP_VAL**	7:0	Default : -	Access : RO
	-	7:3	Reserved	
	FRAME_RP_VAL	2:0	Frame repetition value.	
66h (27CDh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
67h (27CEh)	**CEC_CONFIG1**	7:0	Default: 0x00	Access : R/W
	TX_LEN	7:4	The number byte of data that initiator want to send. Write this register to trigger a new TX request. 0: Only header block is to send.	
	RX_LEN	3:0	The length of received message (Read only). 0: Only header block is received.	
67h (27CFh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
68h (27D0h)	**CEC_CONFIG2_L**	7:0	Default: 0xF5	Access : R/W
	CEC_SAMPLE_SEL	7:5	Sample times select for CEC line high/low detection. If all of samples are the same logic, level "1" or "0" is confirmed (glitch remove). 000: 1X. 001: 2X. 010: 4X. .... 110: 12X. 111: 14X.	

HDMI Register (Bank = 27h)

Index (Absolute)	Mnemonic	Bit	Description	
	TX_LOW_BIT_SEL	4:3	The period select for follower generating a low bit period when the current received bit is too short to be a valid bit. 00: 1X nominal data bit period (2.4ms). 01: 1.4X nominal data bit period (3.4ms). 10: 1.5X nominal data bit period (3.5ms). 11: 1.6X nominal data bit period (3.8ms).	
	RETRY_CNT	2:0	The retry times for re-transmitting a message (MAX).	
68h (27D1h)	CEC_CONFIG2_H	7:0	Default : 0x80	Access : R/W
	CEC_CLK_XTAL_GATE	7	CEC main clock input is gated or not. 0: No gate. 1: Gate.	
	TX_FALL_SHIFT_SEL	6:4	TX falling edge is shifted backward (0~4)*50us. 000: 0us. 001: 50us. 010: 100us. 011: 150us. 100~111: 200us.	
	TX_RISE_SHIFT_SEL	3:1	TX rising or rising edge is shifted backward (0~4)*50us. 000: 0us. 001: 50us. 010: 100us. 011: 150us. 100~111: 200us.	
	TX_REQ_SEL	0	Wait for a period for new TX request. 0: Normal. 1: Wait for a period $\geq$ 7 nominal data bit periods.	
69h (27D2h)	CEC_CONFIG3_L	7:0	Default : 0x03	Access : R/W
	FREE_BIT_CNT2	7:4	The necessary free bit period when new initiator wants to send a frame.	
	FREE_BIT_CNT1	3:0	The necessary free bit period when pervious attempt to send frame unsuccessful.	
69h (27D3h)	CEC_CONFIG3_H	7:0	Default : 0x57	Access : R/W
	LOCAL_ADDR	7:4	Device local address.	
	FREE_BIT_CNT3	3:0	The necessary free bit period when present initiator wants to send another frame immediately after its previous frame.	

HDMI Register (Bank = 27h)

Index (Absolute)	Mnemonic	Bit	Description	
6Ah (27D4h)	CEC_CONFIG4_L	7:0	Default : 0x8F	Access : R/W
	CNT_10US_VALUE[7:0]	7:0	Number of counts to achieve 10us (integer part). 0: 256 clock cycles. 1: 1 clock cycle. 2: 2 clock cycles. ...... 255: 255 clock cycles. (Unit: clock cycle)	
6Ah (27D5h)	CEC_CONFIG4_H	7:0	Default : 0x03	Access : R/W
	-	7:4	Reversed.	
	F_CNT_10US_VALUE[3:0]	3:0	Number of counts to achieve 10us (fractional part). This part is useless when CNT_10US_VALUE=1 (clock cycle). (Unit: 0.0625 clock cycle)	
6Bh (27D6h)	CEC_CONFIG5	7:0	Default : 0x00	Access : R/W
	-	7:6	Reversed.	
	CEC_OVERRIDE_FUN	5	Force CEC line low. 0: Disable. 1: Enable.	
	RX_TEST_MD	4	RX test mode. 0: Normal. 1: Receive all valid messages. (Don't check header block.)	
	CEC_DIS_EH	3	Disable error handling before header block is received. 0: Enable. 1: Disable.	
	TX_LOST_ABT_SEL	2	Cancel TX request or retry if TX lost arbitration to a second initiator. 0: Retry. 1: Cancel.	
	RX_BOUND_SHIFT	1:0	00: Normal. 01: RX upper/lower bound is shifted forward/backward 10us. 1X: RX upper bound is shifted forward 250us.	
6Bh (27D7h)	-	7:0	Default : -	Access : -
	-	7:5	Reversed.	
6Ch	CEC_STS1_L	7:0	Default : -	Access : R/WC

HDMI Register (Bank = 27h)

Index (Absolute)	Mnemonic	Bit	Description	
(27D8h)	-	7:3	Reversed.	
	BIT_TOO_LONG	2	Indicate the received bit period is too long. 0: Normal. 1: Received bit period is too long. (Write 1 to clear)	
	BIT_TOO_SHORT	1	Indicate the received bit period is too short. 0: Normal. 1: Received bit period is too short. (Write 1 to clear)	
	NACK_STS	0	Follower NACK status. 0: No NACK. 1: NACK. (Write 1 to clear)	
6Ch (27D9h)	CEC_STS1_H	7:0	Default : -	Access : RO
	-	7:2	Reversed	
	CEC_LINE_GR	1	CEC line status after removing glitch.	
	CEC_LINE	0	CEC line status.	
6Dh ~ 6Fh (27DA ~ 27DFh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
70h (27E0h)	CEC_TX_DATA0_L	7:0	Default : 0x00	Access : R/W
	INITIATOR_A	7:4	The initiator logical address field.	
	DESTINATION_A	3:0	The destination logical address field.	
70h (27E1h)	CEC_TX_DATA0_H	7:0	Default : 0x00	Access : R/W
	DATA_BLOCK1	7:0	Data block 1.	
71h (27E2h)	CEC_TX_DATA1_L	7:0	Default : 0x00	Access : R/W
	DATA_BLOCK2	7:0	Data block 2.	
71h (27E3h)	CEC_TX_DATA1_H	7:0	Default : 0x00	Access : R/W
	DATA_BLOCK3	7:0	Data block 3.	
72h (27E4h)	CEC_TX_DATA2_L	7:0	Default : 0x00	Access : R/W
	DATA_BLOCK4	7:0	Data block 4.	
72h (27E5h)	CEC_TX_DATA2_H	7:0	Default : 0x00	Access : R/W
	DATA_BLOCK5	7:0	Data block 5.	
73h (27E6h)	CEC_TX_DATA3_L	7:0	Default : 0x00	Access : R/W
	DATA_BLOCK6	7:0	Data block 6.	

HDMI Register (Bank = 27h)

Index (Absolute)	Mnemonic	Bit	Description	
73h (27E7h)	CEC_TX_DATA3_H	7:0	Default : 0x00	Access : R/W
	DATA_BLOCK7	7:0	Data block 7.	
74h (27E8h)	CEC_TX_DATA4_L	7:0	Default : 0x00	Access : R/W
	DATA_BLOCK8	7:0	Data block 8.	
74h (27E9h)	CEC_TX_DATA4_H	7:0	Default : 0x00	Access : R/W
	DATA_BLOCK9	7:0	Data block 9.	
75h (27EAh)	CEC_TX_DATA5_L	7:0	Default : 0x00	Access : R/W
	DATA_BLOCK10	7:0	Data block 10.	
75h (27EBh)	CEC_TX_DATA5_H	7:0	Default : 0x00	Access : R/W
	DATA_BLOCK11	7:0	Data block 11.	
76h (27ECh)	CEC_TX_DATA6_L	7:0	Default : 0x00	Access : R/W
	DATA_BLOCK12	7:0	Data block 12.	
76h (27EDh)	CEC_TX_DATA6_H	7:0	Default : 0x00	Access : R/W
	DATA_BLOCK13	7:0	Data block 13.	
77h (27EEh)	CEC_TX_DATA7_L	7:0	Default : 0x00	Access : R/W
	DATA_BLOCK14	7:0	Data block 14.	
77h (27EFh)	CEC_TX_DATA7_H	7:0	Default : 0x00	Access : R/W
	DATA_BLOCK15	7:0	Data block 15.	
78h (27F0h)	CEC_RX_DATA0_L	7:0	Default : -	Access : RO
	HEADER_BLOCK	7:0	Header block.	
78h (27F1h)	CEC_RX_DATA0_H	7:0	Default : -	Access : RO
	DATA_BLOCK1	7:0	Data block 1.	
79h (27F2h)	CEC_RX_DATA1_L	7:0	Default : -	Access : RO
	DATA_BLOCK2	7:0	Data block 2.	
79h (27F3h)	CEC_RX_DATA1_H	7:0	Default : -	Access : RO
	DATA_BLOCK3	7:0	Data block 3.	
7Ah (27F4h)	CEC_RX_DATA2_L	7:0	Default : -	Access : RO
	DATA_BLOCK4	7:0	Data block 4.	
7Ah (27F5h)	CEC_RX_DATA2_H	7:0	Default : -	Access : RO
	DATA_BLOCK5	7:0	Data block 5.	
7Bh (27F6h)	CEC_RX_DATA3_L	7:0	Default : -	Access : RO
	DATA_BLOCK6	7:0	Data block 6.	

HDMI Register (Bank = 27h)

Index (Absolute)	Mnemonic	Bit	Description	
7Bh (27F7h)	CEC_RX_DATA3_H	7:0	Default : -	Access : RO
	DATA_BLOCK7	7:0	Data block 7.	
7Ch (27F8h)	CEC_RX_DATA4_L	7:0	Default : -	Access : RO
	DATA_BLOCK8	7:0	Data block 8.	
7Ch (27F9h)	CEC_RX_DATA4_H	7:0	Default : -	Access : RO
	DATA_BLOCK9	7:0	Data block 9.	
7Dh (27FAh)	CEC_RX_DATA5_L	7:0	Default : -	Access : RO
	DATA_BLOCK10	7:0	Data block 10.	
7Dh (27FBh)	CEC_RX_DATA5_H	7:0	Default : -	Access : RO
	DATA_BLOCK11	7:0	Data block 11.	
7Eh (27FCh)	CEC_RX_DATA6_L	7:0	Default : -	Access : RO
	DATA_BLOCK12	7:0	Data block 12.	
7Eh (27FDh)	CEC_RX_DATA6_H	7:0	Default : -	Access : RO
	DATA_BLOCK13	7:0	Data block 13.	
7Fh (27FEh)	CEC_RX_DATA7_L	7:0	Default : -	Access : RO
	DATA_BLOCK14	7:0	Data block 14.	
7Fh (27FFh)	CEC_RX_DATA7_H	7:0	Default : -	Access : RO
	DATA_BLOCK15	7:0	Data block 15.	

IRQ/ICACHE/XDMIU Register (Bank = 2B)

IRQ/ICACHE/XDMIU Register (Bank = 2B)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
00h (2B00h)	REG2B00	7:0	Default : 0xFF	Access : R/W
	C_FIQ_MASK[7:0]	7:0	Mask for FIQ, bit[31:0] 1: Mask. 0: Not mask.
00h (2B01h)	REG2B01	7:0	Default : 0xFF	Access : R/W
	C_FIQ_MSK[15:8]	7:0	Please see description of '2B00h'.
01h (2B02h)	REG2B02	7:0	Default : 0xFF	Access : R/W
	C_FIQ_MSK[23:16]	7:0	Please see description of '2B00h'.
01h (2B03h)	REG2B03	7:0	Default : 0xFF	Access : R/W
	C_FIQ_MSK[31:24]	7:0	Please see description of '2B00h'.
02h (2B04h)	REG2B04	7:0	Default : 0x00	Access : R/W
	C_FIQ_FORCE[7:0]	7:0	Force for FIQ, bit[31:0]. 1: Force. 0: Not force.
02h (2B05h)	REG2B05	7:0	Default : 0x00	Access : R/W
	C_FIQ_FORCE[15:8]	7:0	Please see description of '2B04h'.
03h (2B06h)	REG2B06	7:0	Default : 0x00	Access : R/W
	C_FIQ_FORCE[23:16]	7:0	Please see description of '2B04h'.
03h (2B07h)	REG2B07	7:0	Default : 0x00	Access : R/W
	C_FIQ_FORCE[31:24]	7:0	Please see description of '2B04h'.
04h (2B08h)	REG2B08	7:0	Default : 0x00	Access : R/W
	C_FIQ_CLR[7:0]	7:0	Clear for FIQ, bit[31:0]. 1: Clear. 0: Not clear.
04h (2B09h)	REG2B09	7:0	Default : 0x00	Access : R/W
	C_FIQ_CLR[15:8]	7:0	Please see description of '2B08h'.
05h (2B0Ah)	REG2B0A	7:0	Default : 0x00	Access : R/W
	C_FIQ_CLR[23:16]	7:0	Please see description of '2B08h'.
05h (2B0Bh)	REG2B0B	7:0	Default : 0x00	Access : R/W
	C_FIQ_CLR[31:24]	7:0	Please see description of '2B08h'.
06h (2B0Ch)	REG2B0C	7:0	Default : -	Access : RO
	FIQ_RAW_STS[7:0]	7:0	FIQ raw status, bit[31:0]. Interrupt source status for FIQ.

IRQ/ICACHE/XDMIU Register (Bank = 2B)

Index (Absolute)	Mnemonic	Bit	Description	
06h (2B0Dh)	REG2B0D	7:0	Default : -	Access : RO
	FIQ_RAW_STS[15:8]	7:0	Please see description of '2B0Ch'.	
07h (2B0Eh)	REG2B0E	7:0	Default : -	Access : RO
	FIQ_RAW_STS[23:16]	7:0	Please see description of '2B0Ch'.	
07h (2B0Fh)	REG2B0F	7:0	Default : -	Access : RO
	FIQ_RAW_STS[31:24]	7:0	Please see description of '2B0Ch'.	
08h (2B10h)	REG2B10	7:0	Default : -	Access : RO
	FIQ_FINAL_STS[7:0]	7:0	FIQ final status, bit[31:0]. Finial interrupt status for FIQ.	
08h (2B11h)	REG2B11	7:0	Default : -	Access : RO
	FIQ_FINAL_STS[15:8]	7:0	Please see description of '2B10h'.	
09h (2B12h)	REG2B12	7:0	Default : -	Access : RO
	FIQ_FINAL_STS[23:16]	7:0	Please see description of '2B10h'.	
09h (2B13h)	REG2B13	7:0	Default : -	Access : RO
	FIQ_FINAL_STS[31:24]	7:0	Please see description of '2B10h'.	
0Ah (2B14h)	REG2B14	7:0	Default : 0x00	Access : R/W
	C_FIQ_SEL_HL_TRGR[7:0]	7:0	Select H or L trigger, bit[31:0]. Inverse source polarity for FIQ.	
0Ah (2B15h)	REG2B15	7:0	Default : 0x00	Access : R/W
	C_FIQ_SEL_HL_TRGR[15:8]	7:0	Please see description of '2B14h'.	
0Bh (2B16h)	REG2B16	7:0	Default : 0x00	Access : R/W
	C_FIQ_SEL_HL_TRGR[23:16]	7:0	Please see description of '2B14h'.	
0Bh (2B17h)	REG2B17	7:0	Default : 0x00	Access : R/W
	C_FIQ_SEL_HL_TRGR[31:24]	7:0	Please see description of '2B14h'.	
0Ch (2B18h)	REG2B18	7:0	Default : 0xFF	Access : R/W
	C_IRQ_MSK[7:0]	7:0	Mask for IRQ, bit[31:0]. 1: Mask. 0: Not mask.	
0Ch (2B19h)	REG2B19	7:0	Default : 0xFF	Access : R/W
	C_IRQ_MSK[15:8]	7:0	Please see description of '2B18h'.	
0Dh (2B1Ah)	REG2B1A	7:0	Default : 0xFF	Access : R/W
	C_IRQ_MSK[23:16]	7:0	Please see description of '2B18h'.	
0Dh (2B1Bh)	REG2B1B	7:0	Default : 0xFF	Access : R/W
	C_IRQ_MSK[31:24]	7:0	Please see description of '2B18h'.	

IRQ/ICACHE/XDMIU Register (Bank = 2B)

Index (Absolute)	Mnemonic	Bit	Description	
0Eh (2B1Ch)	REG2B1C	7:0	Default : 0x00	Access : R/W
	C_IRQ_FORCE[7:0]	7:0	Force for IRQ, bit[31:0]. 1: Force. 0: Not force.	
0Eh (2B1Dh)	REG2B1D	7:0	Default : 0x00	Access : R/W
	C_IRQ_FORCE[15:8]	7:0	Please see description of '2B1Ch'.	
0Fh (2B1Eh)	REG2B1E	7:0	Default : 0x00	Access : R/W
	C_IRQ_FORCE[23:16]	7:0	Please see description of '2B1Ch'.	
0Fh (2B1Fh)	REG2B1F	7:0	Default : 0x00	Access : R/W
	C_IRQ_FORCE[31:24]	7:0	Please see description of '2B1Ch'.	
10h (2B20h)	REG2B20	7:0	Default : 0x00	Access : R/W
	C_IRQ_SEL_HL_TRGR[7:0]	7:0	Select H or L trigger, bit[31:0]. Inverse source polarity for IRQ.	
10h (2B21h)	REG2B21	7:0	Default : 0x00	Access : R/W
	C_IRQ_SEL_HL_TRGR[15:8]	7:0	Please see description of '2B20h'.	
11h (2B22h)	REG2B22	7:0	Default : 0x00	Access : R/W
	C_IRQ_SEL_HL_TRGR[23:16]	7:0	Please see description of '2B20h'.	
11h (2B23h)	REG2B23	7:0	Default : 0x00	Access : R/W
	C_IRQ_SEL_HL_TRGR[31:24]	7:0	Please see description of '2B20h'.	
12h (2B24h)	REG2B24	7:0	Default : -	Access : RO
	IRQ_RAW_STS[7:0]	7:0	IRQ raw status, bit[31:0]. Interrupt source status for IRQ.	
12h (2B25h)	REG2B25	7:0	Default : -	Access : RO
	IRQ_RAW_STS[15:8]	7:0	Please see description of '2B24h'.	
13h (2B26h)	REG2B26	7:0	Default : -	Access : RO
	IRQ_RAW_STS[23:16]	7:0	Please see description of '2B24h'.	
13h (2B27h)	REG2B27	7:0	Default : -	Access : RO
	IRQ_RAW_STS[31:24]	7:0	Please see description of '2B24h'.	
14h (2B28h)	REG2B28	7:0	Default : -	Access : RO
	IRQ_FINAL_STS[7:0]	7:0	IRQ final status, bit[31:0]. Finial interrupt status for IRQ.	
14h (2B29h)	REG2B29	7:0	Default : -	Access : RO
	IRQ_FINAL_STS[15:8]	7:0	Please see description of '2B28h'.	
15h	REG2B2A	7:0	Default : -	Access : RO

IRQ/ICACHE/XDMIU Register (Bank = 2B)

Index (Absolute)	Mnemonic	Bit	Description	
(2B2Ah)	IRQ_FINAL_STS[23:16]	7:0	Please see description of '2B28h'.	
15h	**REG2B2B**	**7:0**	**Default : -**	**Access : RO**
(2B2Bh)	IRQ_FINAL_STS[31:24]	7:0	Please see description of '2B28h'.	
16h ~ 3Fh	-	**7:0**	**Default : -**	**Access : -**
(2B2Ch ~ 2BFFh)	-	7:0	Reserved.	
40h	**REG2B80**	**7:0**	**Default : 0x00**	**Access : R/W**
(2B80h)	SDRAM_CODE_MAP[7:0]	7:0	SDRAM code map address; unit: 64Kbyte.	
40h	**REG2B81**	**7:0**	**Default : 0x00**	**Access : R/W**
(2B81h)	SDRAM_CODE_MAP[15:8]	7:0	Please see description of '2B80h'.	
41h	**REG2B82**	**7:0**	**Default : -**	**Access : RO**
(2B82h)	CPU_ADR_L[7:0]	7:0	CPU address[15:0].	
41h	**REG2B83**	**7:0**	**Default : -**	**Access : RO**
(2B83h)	CPU_ADR_L[15:8]	7:0	Please see description of '2B82h'.	
42h	**REG2B84**	**7:0**	**Default : -**	**Access : RO**
(2B84h)	CPU_ADR_H[7:0]	7:0	CPU address[23:0].	
42h	**REG2B85**	**7:0**	**Default : -**	**Access : RO**
(2B85h)	CPU_ADR_H[15:8]	7:0	Please see description of '2B84h'.	
43h	**REG2B86**	**7:0**	**Default : -**	**Access : RO**
(2B86h)	CPU_ROM_DATA0[7:0]	7:0	Icache return data[15:0] to CPU.	
43h	**REG2B87**	**7:0**	**Default : -**	**Access : RO**
(2B87h)	CPU_ROM_DATA0[15:8]	7:0	Please see description of '2B86h'.	
44h	**REG2B88**	**7:0**	**Default : -**	**Access : RO**
(2B88h)	CPU_ROM_DATA1[7:0]	7:0	Icache return data[31:16] to CPU.	
44h	**REG2B89**	**7:0**	**Default : -**	**Access : RO**
(2B89h)	CPU_ROM_DATA1[15:8]	7:0	Please see description of '2B88h'.	
45h	REG2B8A	**7:0**	**Default : -**	**Access : RO**
(2B8Ah)	CACHE_MISS_COUNT[7:0]	7:0	Cache miss counter.	
45h	REG2B8B	**7:0**	**Default : -**	**Access : RO**
(2B8Bh)	CACHE_MISS_COUNT[15:8]	7:0	Please see description of '2B8Ah'.	
46h	REG2B8C	**7:0**	**Default : -**	**Access : RO**
(2B8Ch)	CACHE_HIT_COUNT[7:0]	7:0	Cahce hit counter.	
46h	REG2B8D	**7:0**	**Default : -**	**Access : RO**

IRQ/ICACHE/XDMIU Register (Bank = 2B)

Index (Absolute)	Mnemonic	Bit	Description	
(2B8Dh)	CACHE_HIT_COUNT[15:8]	7:0	Please see description of '2B8Ch'.	
47h (2B8Eh)	REG2B8E	7:0	Default : -	Access : RO
	-	7:2	Reserved.	
	CPU_WAIT	1	CPU wait flag. 0: Hit. 1: Wait.	
	CACHE_MISS_FLAG	0	Cache miss flag. 0: Hit. 1: Miss.	
48h (2B90h)	REG2B90	7:0	Default : -	Access : RO
	-	7:4	Reserved.	
	CACHE_FSM[3:0]	3:0	Cache FSM.	
4Ah ~ 4Fh (2B94h ~ 2B9Fh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
50h (2BA0h)	REG2BA0	7:0	Default : 0x01	Access : R/W
	-	7:1	Reserved.	
	CACHE_BY_PASS	0	Cache by pass mode.	
50h ~ 5Fh (2BA1h ~ 2BBF)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
60h (2BC0h)	REG2BC0	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	SOFTWARE_RST	0	Set 1 to reset HK_MCU XDATA2MIU.	
61h (2BC2h ~ 2BC3h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
62h (2BC4h)	REG2BC4	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	XB_SDR_MAP_EN	2	Set 1 to enable the mapping of HK_MCU XDATA to MIU.	
	XD2MIU_WPRI	1	XDATA2MIU write priority.	
	XD2MIU_RPRI	0	XDATA2MIU read priority.	
63h (2BC6h)	REG2BC6	7:0	Default : 0x00	Access : R/W
	XB_ADDR[7:0]	7:0	The low bound address of MCU XDATA mapping to	

IRQ/ICACHE/XDMIU Register (Bank = 2B)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
			MIU (unit: 1k bytes). The XDATA address is hit if (REG_XB_ADDR[15:8] > XDATA_ADDR[15:10] >= REG_XB_ADDR[7:0]).
63h (2BC7h)	REG2BC7	7:0	Default : 0x00
			Access : R/W
	XB_ADDR[15:8]	7:0	Please see description of '2BC6h'.
64h (2BC8h)	REG2BC8	7:0	Default : 0x00
			Access : R/W
	SDR_XD_MAP[7:0]	7:0	The low byte address to access XDATA from MIU. The granularity is 64k bytes. The actual address[26:0] to MIU would be SDR_XD_MAP[10:8], SDR_XD_MAP[7:0], XDATA_ADDR[15:0], where XDATA_ADDR[15:0] is MCU XDATA address of 64k bytes.
64h (2BC9h)	REG2BC9	7:0	Default : 0x00
			Access : R/W
	SDR_XD_MAP[15:8]	7:0	Please see description of '2BC8h'.
65h (2BCAh)	REG2BCA	7:0	Default : 0x00
			Access : R/W
	XB_ADDR_1[7:0]	7:0	The low bound address of MCU XDATA mapping to MIU. (unit: 1k bytes). The XDATA address is hit if (REG_XB_ADDR_1[15:8] > XDATA_ADDR[15:10] >= REG_XB_ADDR_1[7:0]).
65h (2BCBh)	REG2BCB	7:0	Default : 0x00
			Access : R/W
	XB_ADDR_1[15:8]	7:0	Please see description of '2BCAh'.
66h (2BCCh)	REG2BCC	7:0	Default : 0x00
			Access : R/W
	SDR_XD_MAP_1_0[7:0]	7:0	The low byte address to access XDATA from MIU. The granularity is 1k bytes. The actual address[26:0] to MIU would be SDR_XD_MAP_1_1[0], SDR_XD_MAP_1_0[15:8], SDR_XD_MAP_1_0[7:0], XDATA_ADDR[9:0], where XDATA_ADDR[15:0] is MCU XDATA address of 64k bytes.
66h (2BCDh)	REG2BCD	7:0	Default : 0x00
			Access : R/W
	SDR_XD_MAP_1_0[15:8]	7:0	Please see description of '2BCCh'.
67h (2BCEh)	REG2BCE	7:0	Default : 0x00
			Access : R/W
	SDR_XD_MAP_1_1[7:0]	7:0	The low byte address to access XDATA from MIU. The granularity is 1k bytes. The actual address[26:0] to MIU would be SDR_XD_MAP_1_1[0], SDR_XD_MAP_1_0[15:8], SDR_XD_MAP_1_0[7:0], XDATA_ADDR[9:0],

IRQ/ICACHE/XDMIU Register (Bank = 2B)

Index (Absolute)	Mnemonic	Bit	Description	
			where XDATA_ADDR[15:0] is MCU XDATA address of 64k bytes.	
67h (2BCFh)	REG2BCF	7:0	Default : 0x00	Access : R/W
	SDR_XD_MAP_1_1[15:8]	7:0	Please see description of '2BCEh'.	
7Eh (2BFCh)	REG2BFC	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	CPU0_2_CPU1_IRQ	0	CPU0 to CPU1 interrupt.	
7Fh (2BFEh)	REG2BFE	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	CPU1_2_CPU0_IRQ	0	CPU1 to CPU0 interrupt.	

Audio 0 Register (Bank = 2C)

Audio 0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2C00h)	REG2C00	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	CLKGEN_RESET	1	Audio engine CLKGEN reset. 0: Normal. 1: Reset.	
	SOFTWARE_RESET	0	Audio engine software reset. 0: Normal. 1: Reset. Note: This command cannot reset register value.	
00h (2C01h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
01h (2C02h)	REG2C02	7:0	Default : 0x00	Access : R/W
	EN_CARD_READER_FIX_SYNTH	7	Enable card reader audio sample frequency fixed synthesizer module. 0: Disable. 1: Enable (256Fs).	
	EN_DVB_FIX_SYNTH	6	Enable DVB audio sample frequency fixed synthesizer module. 0: Disable. 1: Enable (256Fs).	
	EN_DVB_SYNC_SYNTH	5	Enable DVB audio sample frequency synthesizer module, synchronous to 27MHz clock. 0: Disable. 1: Enable (256Fs).	
	I2S_IN_FMT	4	Configure input I2S interface format. 0: I2S-justified (standard format). 1: Left-justified.	
	EN_I2S_SYNTH	3	Enable I2S audio sample frequency synthesizer module. 0: Disable. 1: Enable (256Fs).	
	EN_SIF_SYNTH	2	Enable SIF audio sample frequency synthesizer module. 0: Disable. 1: Enable (256Fs).	
	EN_SPDIF_CDR	1	Enable S/PDIF input Clock Data Recovery module.	

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
			0: Disable. 1: Enable (256Fs).	
	EN_ADC_SYNTH	0	Enable ADC audio sample frequency synthesizer module. 0: Disable. 1: Enable (256Fs).	
01h (2C03h)	REG2C03	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	EN_768_FS_SYNTH	4	Enable 768 fs audio sample frequency synthesizer module. 0: Disable. 1: Enable (256Fs).	
	-	3	Reserved.	
	DVB_PLL_LOCK_CURRENT_FREQ	2	Force lock current DVB SYNC synthesizer frequency. 0: Disable. 1: Enable.	
	DVB_FREQ_GAIN	1	Audio DVB SYNC synthesizer Cs gain selection. 0: Normal. 1: Enhancement (smaller Cs).	
	DVB_PHASE_GAIN	0	Audio DVB SYNC synthesizer Cp gain selection. 0: Normal. 1: Enhancement (smaller Cp).	
02h (2C04h)	REG2C04	7:0	Default : -	Access : RO
	DVB_SYNC_FREQ[7:0]	7:0	Audio DVB SYNC synthesizer Frequency value.	
02h (2C05h)	REG2C05	7:0	Default : -	Access : RO
	DVB_SYNC_NO_SIGNAL	7	Audio DVB SYNC synthesizer input signal detect. 0: Signal detected. 1: No signal input.	
	DVB_SYNC_FREQ[14:8]	6:0	Please see description of '2C04h'.	
03h (2C06h)	REG2C06	7:0	Default : -	Access : RO
	I2S_FREQ[7:0]	7:0	Audio I2S Clock Data Recovery Frequency value.	
03h (2C07h)	REG2C07	7:0	Default : -	Access : RO
	I2S_NO_SIGNAL	7	Audio I2S Clock Data Recovery input signal detect. 0: Signal detected. 1: No signal input.	
	I2S_FREQ[14:8]	6:0	Please see description of '2C06h'.	

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
04h (2C08h)	REG2C08	7:0	Default : -	Access : RO
	SIF_FREQ[7:0]	7:0	Audio SIF Clock Data Recovery Frequency value.	
04h (2C09h)	REG2C09	7:0	Default : -	Access : RO
	SIF_NO_SIGNAL	7	Audio SIF Clock Data Recovery input signal detect. 0: Signal detected. 1: No input signal.	
	SIF_FREQ[14:8]	6:0	Please see description of '2C08h'.	
05h (2C0Ah)	REG2C0A	7:0	Default : 0x30	Access : R/W
	COARSE_K[3:0]	7:4	Audio S/PDIF CDR Coarse Frequency Detection threshold K value (locked range detection offset value). 0000: Reserved. 0001: Minimum range. &&& 1111: Maximum range. 0011: Suggested value.	
	PHASE_OFFSET[3:0]	3:0	Audio S/PDIF CDR output clock phase select (1 sampling phase = 5ns). 0111: Delay 7 sampling phase offset. & 0000: Delay 0 sampling phase offset. 1000: Early 0 sampling phase offset. 1001: Early 1 sampling phase offset. & 1111: Early 7 sampling phase offset.	
05h (2C0Bh)	REG2C0B	7:0	Default : 0x13	Access : R/W
	FDC_KD[3:0]	7:4	Audio S/PDIF CDR frequency detect coarse Kd(Gain) select (protect CDR from harmonic locking). 0000: Special use for S/W. 0001: Minimum gain. & 1111: Maximum gain.	
	PHASE_TRACKER	3	Audio S/PDIF CDR phase tracking mode select. 0: Normal mode (tracking while in locked range). 1: Turbo mode (always tracking).	
	PD_RESOLUTION[2:0]	2:0	Audio S/PDIF CDR phase tracking band width control. 000: Phase tracking fastest. &	

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
			111: Phase tracking slowest. (011: Suggested value)	
06h (2C0Ch)	REG2C0C	7:0	Default : -	Access : RO
	HDMI_MODE[1:0]	7:6	Status of audio stream from HDMI input interface. 00: PCM audio. 01: Non-PCM (Compressed) audio. 10: One bit audio. 11: Reserved.	
	HDMI_AUDIO_MUTE	5	Status of HDMI audio decoder (pre-setting error event). 0: Normal. 1: Mute.	
	HDMI_AVMUTE	4	Decoded AVMUTE bit from HDMI received general control packet. 0: Clear AVMUTE. 1: Set AVMUTE.	
	SPDIF_NON_PCM_LOCK	3	Status of Non-PCM audio preamble lock. 0: Unlocked. 1: Locked.	
	SPDIF_PLL_LOCK	2	Status of audio S/PDIF CDR (coarse normal). 0: Unlocked. 1: Locked.	
	SPDIF_NON_PCM	1	Status of audio stream from S/PDIF input interface (from channel status bit 1). 0: PCM audio. 1: Non-PCM audio.	
	SPDIN_ERROR	0	S/PDIF input decoder status. 0: Normal. 1: Un-synced, missing framing bits.	
06h (2C0Dh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
07h (2C0Eh)	REG2C0E	7:0	Default : -	Access : RO
	SPDIF_FREQ[7:0]	7:0	Audio S/PDIF clock data recovery frequency value.	
07h (2C0Fh)	REG2C0F	7:0	Default : -	Access : RO
	SPDIF_NO_SIGNAL	7	Audio S/PDIF clock data recovery input signal detect. 0: Signal detected. 1: No signal input.	

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
	SPDIF_FREQ[14:8]	6:0	Please see description of '2C0Eh'.	
08h (2C10h)	**REG2C10**	**7:0**	**Default : -**	**Access : RO**
	SPDIF_CS0[7:6]	7:6	Channel status mode. 00: Mode zero. Others: Reserved.	
	SPDIF_CS0[5:3]	5:3	Emphasis. 000: Emphasis not indicated. 100: Emphasis_CD-type. Others: Reserved.	
	SPDIF_CS0[2]	2	Copyright. 0: Asserted. 1: Not asserted.	
	SPDIF_CS0[1]	1	S/PDIF input channel status consumer format. 0: PCM. 1: Non-PCM format.	
	SPDIF_CS0[0]	0	S/PDIF input channel status consumer format. 0: Consumer. 1: Professional format.	
08h (2C11h)	-	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
09h (2C12h)	**REG2C12**	**7:0**	**Default : -**	**Access : RO**
	SPDIF_CS1[7:0]	7:0	S/PDIF input channel status [8:15] consumer format. Bit 8-15 = category code. 1000 0000: CD player. 1100 000L: DAT player. 1100 001L: DCC player. 1001 001L: Mini disc. L-bit carries information about generation status of the material.	
09h (2C13h)	-	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
0Ah (2C14h)	**REG2C14**	**7:0**	**Default : -**	**Access : RO**
	SPDIF_CS2[7:0]	7:0	S/PDIF input channel status [16:23] consumer format. Bit 16-19 = Source number (bit 16 is LSB). Bit 20-23 = Channel number (bit 20 is LSB).	
0Ah	-	**7:0**	**Default : -**	**Access : -**

Audio 0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2C15h)	-	7:0	Reserved.	
0Bh (2C16h)	REG2C16	7:0	Default : -	Access : RO
	SPDIF_CS3[7:0]	7:0	S/PDIF input channel status [24:31] consumer format. Bit 24-27 = Sampling frequency. 0000: 44.1 kHz. 0100: 48 kHz. 1100: 32 kHz. Bit 28-29 = Clock accuracy. 00: Level II, +-1000ppm. 01: Level III, variable pitch shifted. 10: Level I, +-50ppm. Bit 30-31: Reserved.	
0Bh (2C17h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
0Ch (2C18h)	REG2C18	7:0	Default : -	Access : RO
	SPDIF_CS4[7:0]	7:0	S/PDIF input channel status [32:39] consumer format. Bit 32 = Word length (field size). 0: Maximum length 20 bits. 1: Maximum length 24 bits. Bit 33-35 = Word length. 000: Not indicated. 101: 24 bits (if bit 32 = 1) or 20 bits (if bit 32 = 0). 001: 23 bits (if bit 32 = 1) or 19 bits (if bit 32 = 0). 010: 22 bits (if bit 32 = 1) or 18 bits (if bit 32 = 0). 011: 21 bits (if bit 32 = 1) or 17 bits (if bit 32 = 0). 100: 20 bits (if bit 32 = 1) or 16 bits (if bit 32 = 0). Bit 36-39: Reserved.	
0Ch (2C19h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
0Dh (2C1Ah)	REG2C1A	7:0	Default : -	Access : RO
	STATUS_SPDIF_IN_PC[7:0]	7:0	SPDIF input non-PCM preamble Pc.	
0Dh (2C1Bh)	REG2C1B	7:0	Default : -	Access : RO
	STATUS_SPDIF_IN_PC[15:8]	7:0	Please see description of '2C1Ah'.	
0Eh (2C1Ch)	REG2C1C	7:0	Default : -	Access : RO
	STATUS_SPDIF_IN_PD[7:0]	7:0	SPDIF input non-PCM preamble Pd.	

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
0Eh (2C1Dh)	REG2C1D	7:0	Default : -	Access : RO
	STATUS_SPDIF_IN_PD[15:8]	7:0	Please see description of '2C1Ch'.	
0Fh (2C1Eh ~ 2C1Fh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
10h (2C20h)	REG2C20	7:0	Default : 0x3A	Access : R/W
	HDMIPLL_CTRL1_RESET	7	HDMI audio PLL reset. 0: No action. 1: Reset.	
	HDMIPLL_CTRL1_ICTRL[2:0]	6:4	Audio HDMI CODEC PLL charge pump current control. 000: 0.25 uA. 001: 0.75 uA. 010: 1.5 uA. 011: 2.5 uA. 100: 4 uA. 101: 6 uA. 110: 9 uA. 111: 13 uA.	
	HDMIPLL_CTRL1_PWRDOWN	3	HDMI audio PLL power-down. 0: No action. 1: Power-down.	
	HDMIPLL_CTRL1_CTRL[2:0]	2:0	Audio HDMI CODEC PLL loop filter resistor control. $R = 15 + 5 \times RCTRL$ (k ohm)	
10h (2C21h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
11h (2C22h)	REG2C22	7:0	Default : 0x00	Access : R/W
	HDMIPLL_CRTL2_TEST7	7	Bypass divider DDIV & KN before phase frequency detector. 0: Normal. 1: Bypass.	
	HDMIPLL_CRTL2_TEST6	6	Bypass VCO clamping diode. 0: Normal. 1: Bypass.	
	HDMIPLL_CRTL2_TEST5	5	Reserved.	
	HDMIPLL_CRTL2_TEST4	4	Enable DCLK1 output (reserved for future). 0: Disable.	

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
			1: Enable.	
	HDMIPLL_CRTL2_TEST3	3	Enable TEST_OUT1 output from reference clock divided by KN. 0: Disable. 1: Enable (to duty cycle test block).	
	HDMIPLL_CRTL2_TEST2	2	Enable TEST_OUT1 output from reference clock divided by FBDIV. 0: Disable. 1: Enable (to duty cycle test block).	
	HDMIPLL_CRTL2_TEST1	1	Enable CLK_OUT1(to Digital block) from CLK_TEST (external). 0: Disable. 1: Enable.	
	HDMIPLL_CRTL2_TEST0	0	Reserved.	
11h (2C23h)	**REG2C23**	7:0	**Default : 0x00**	**Access : R/W**
	HDMIPLL_CRTL2_TEST15_8[7:0]	7:0	HDMI audio PLL test input MSB [15:8]. TEST_IN register is for testing only.	
12h (2C24h)	**REG2C24**	7:0	**Default : 0x20**	**Access : R/W**
	HDMIPLL_CRTL3[7]	7	Enable VCO free running. 0: Enable. 1: Disable.	
	HDMIPLL_CRTL3[6]	6	Enable intercept audio driver in HDMI PLL synthesizer. 0: Normal. 1: Enable.	
	HDMIPLL_CRTL3[5]	5	Enable HDMI PLL 2x output clock. 0: Disable. 1: Enable.	
	HDMIPLL_CRTL3[4]	4	Enable TMDS PLL lock detection. 0: Disable 1: Enable	
	HDMIPLL_CRTL3[3]	3	HDMI audio PLL reset. 0: Normal. 1: Reset (all analog front-end & dividers).	
	HDMIPLL_CRTL3[2]	2	HDMI audio PLL post clock divider reset (KP). 0: Normal. 1: Reset.	

Audio 0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	HDMIPLL_CRTL3[1]	1	HDMI audio PLL feedback clock divider reset (FBDIV & KM). 0: Normal. 1: Reset.	
	HDMIPLL_CRTL3[0]	0	HDMI audio PLL input clock divider reset (DDIV & KN). 0: Normal. 1: Reset.	
12h (2C25h)	-	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
13h (2C26h)	**REG2C26**	**7:0**	**Default : 0x33**	**Access : R/W**
	HDMIPLL_CRTL4[7:4]	7:4	HDMI PLL post divider ratio (KP) for new mode. 0000: / 1. 0001: / 2. 0010: / 4. & 1001: / 512. 1010: / 1024. 1011: / 1024. & 1111: / 1024.	
	HDMIPLL_CRTL4[3:0]	3:0	HDMI PLL KM divider ratio for new mode. 0000: / 1. 0001: / 2. 0010: / 4. & 0111: / 128. 1000: / 256. 1001: / 256. & 1111: / 256.	
13h (2C27h)	**REG2C27**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	HDMIPLL_CRTL4[9:8]	1:0	HDMI PLL KN divider ratio for new mode. 00: /1. 01: /2. 10: /4. 11: /4.	

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
14h (2C28h)	REG2C28	7:0	Default : 0x00	Access : R/W
	HDMIPLL_CRTL5[7:4]	7:4	HDMI PLL input overwrite divider value from noise-shape quantizer for new mode. 0000: Reserved (/256). 0001: Reserved (/256). 0010: /2. 0011: /3. & 1111: /15.	
	HDMIPLL_CRTL5[3:0]	3:0	HDMI PLL feedback overwrite divider value from noise-shape quantizer for new mode. 0000: Reserved (/256). 0001: Reserved (/256). 0010: /2. 0011: /3. & 1111: /15.	
14h (2C29h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
15h (2C2Ah)	REG2C2A	7:0	Default : 0x00	Access : R/W
	HDMI_SYNTH_CFG1[7]	7	Audio HDMI CTS-N synthesizer control. 0: Idle. 1: Enable (never disable HDMI CTS-N synthesizer after it is enabled).	
	HDMI_SYNTH_CFG1[6]	6	Audio HDMI CTS FIFO bypass control. 0: Normal. 1: Bypass CTS FIFO.	
	-	5	Reserved.	
	HDMI_SYNTH_CFG1[4]	4	S/PDIF 256 fs synthesizer clock pulse expander. 0: Normal (1T width). 1: Expander (2T width).	
	HDMI_SYNTH_CFG1[3]	3	Audio HDMI CTS-N synthesizer lock current frequency. 0: Normal. 1: Lock.	
	HDMI_SYNTH_CFG1[2]	2	Audio HDMI CTS-N synthesizer Cs gain selection. 0: Normal. 1: Enhancement (smaller Cs).	

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
	HDMI_SYNTH_CFG1[1]	1	Audio HDMI CTS-N synthesizer Cp gain selection. 0: Normal. 1: Enhancement (smaller Cp).	
	HDMI_SYNTH_CFG1[0]	0	Audio HDMI CTS-N synthesizer CTS REF selection. 0: Select CTS FIFO out valid. 1: Select CTS[19:0].	
15h (2C2Bh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
16h (2C2Ch)	REG2C2C	7:0	Default : -	Access : RO
	HDMI_FREQ_STATUS[7:0]	7:0	Audio HDMI CTS-N synthesizer frequency value.	
16h (2C2Dh)	REG2C2D	7:0	Default : -	Access : RO
	HDMI_FREQ_STATUS[15]	7	Audio HDMI CTS-N synthesizer input signal detect. 0: Signal detected. 1: No input signal.	
	HDMI_FREQ_STATUS[14:8]	6:0	Please see description of '2C2Ch'.	
17h ~ 1Fh (2C2Eh ~ 2C3Fh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
20h (2C40h)	REG2C40	7:0	Default : -	Access : RO
	STATUS_HDMI_PC[7:0]	7:0	HDMI input Non-PCM preamble Pc.	
20h (2C41h)	REG2C41	7:0	Default : -	Access : RO
	STATUS_HDMI_PC[15:8]	7:0	Please see description of '2C40h'.	
21h (2C42h)	REG2C42	7:0	Default : -	Access : RO
	STATUS_HDMI_PD[7:0]	7:0	HDMI input non-PCM preamble Pd.	
21h (2C43h)	REG2C43	7:0	Default : -	Access : RO
	STATUS_HDMI_PD[15:8]	7:0	Please see description of '2C42h'.	
22h (2C44h)	REG2C44	7:0	Default : 0x10	Access : R/W
	HDMI_MATRIX0[7:0]	7:0	Reserved.	
	HDMI_MATRIX0[6:4]	6:4	HDMI audio channel 2 matrix. 000: mapped from channel 1. 001: mapped from channel 2. 010: mapped from channel 3. 011: mapped from channel 4 100: mapped from channel 5. 101: mapped from channel 6. 110: mapped from channel 7.	

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
			111: mapped from channel 8.	
	-	3	Reserved.	
	HDMI_MATRIX0[2:0]	2:0	HDMI audio channel 1 matrix. 000: mapped from channel 1. 001: mapped from channel 2. 010: mapped from channel 3. 011: mapped from channel 4. 100: mapped from channel 5. 101: mapped from channel 6. 110: mapped from channel 7. 111: mapped from channel 8.	
22h (2C45h)	REG2C45	7:0	Default : 0x32	Access : R/W
	-	7	Reserved.	
	HDMI_MATRIX0[14:12]	6:4	HDMI audio channel 4 matrix. 000: mapped from channel 1. 001: mapped from channel 2. 010: mapped from channel 3. 011: mapped from channel 4. 100: mapped from channel 5. 101: mapped from channel 6. 110: mapped from channel 7. 111: mapped from channel 8.	
	-	3	Reserved.	
	HDMI_MATRIX0[10:8]	2:0	HDMI audio channel 3 matrix. 000: mapped from channel 1. 001: mapped from channel 2. 010: mapped from channel 3. 011: mapped from channel 4. 100: mapped from channel 5. 101: mapped from channel 6. 110: mapped from channel 7. 111: mapped from channel 8.	
23h (2C46h)	REG2C46	7:0	Default : 0x54	Access : R/W
	HDMI_MATRIX1[7:0]	7:0	Reserved.	
	HDMI_MATRIX1[6:4]	6:4	HDMI audio channel 6 matrix. 000: mapped from channel 1. 001: mapped from channel 2. 010: mapped from channel 3.	

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			011: mapped from channel 4 100: mapped from channel 5. 101: mapped from channel 6. 110: mapped from channel 7. 111: mapped from channel 8.
	-	3	Reserved.
	HDMI_MATRIX1[2:0]	2:0	HDMI audio channel 5 matrix. 000: mapped from channel 1. 001: mapped from channel 2. 010: mapped from channel 3. 011: mapped from channel 4. 100: mapped from channel 5. 101: mapped from channel 6. 110: mapped from channel 7. 111: mapped from channel 8.
23h (2C47h)	REG2C47	7:0	Default : 0x76 Access : R/W
	-	7	Reserved.
	HDMI_MATRIX1[14:12]	6:4	HDMI audio channel 8 matrix. 000: mapped from channel 1. 001: mapped from channel 2. 010: mapped from channel 3. 011: mapped from channel 4. 100: mapped from channel 5. 101: mapped from channel 6. 110: mapped from channel 7. 111: mapped from channel 8.
	-	3	Reserved.
	HDMI_MATRIX1[10:8]	2:0	HDMI audio channel 7 matrix. 000: mapped from channel 1. 001: mapped from channel 2. 010: mapped from channel 3. 011: mapped from channel 4. 100: mapped from channel 5. 101: mapped from channel 6. 110: mapped from channel 7. 111: mapped from channel 8.
24h (2C48h)	REG2C48	7:0	Default : 0x00 Access : R/W
	DOWN_SAMPLE[7:6]	7:6	Input DVB down sampling ratio.

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
			00: Normal (from 1x to 1x). 01: Down sample from 2x to 1x. 10: Down sample from 4x to 1x. 11: Reserved.	
	DOWN_SAMPLE[5:4]	5:4	Input I2S down sampling ratio. 00: Normal (from 1x to 1x). 01: Down sample from 2x to 1x. 10: Down sample from 4x to 1x. 11: Reserved.	
	DOWN_SAMPLE[3:2]	3:2	Input SPDIF down sampling ratio. 00: Normal (from 1x to 1x). 01: Down sample from 2x to 1x. 10: Down sample from 4x to 1x. 11: Reserved.	
	DOWN_SAMPLE[1:0]	1:0	Input HDMI down sampling ratio. 00: Normal (from 1x to 1x). 01: Down sample from 2x to 1x. 10: Down sample from 4x to 1x. 11: Reserved.	
24h ~ 2Fh (2C49h ~ 2C5Fh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
30h (2C60h)	REG2C60	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	DECODER1_CFG[1:0]	1:0	DSP decoder input function selection. 00: DVB (MPEG / AC3). 01: JPEG / MP3/AAC (card reader). 10: S/PDIF non-PCM. 11: SIF.	
30h (2C61h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
31h (2C62h)	REG2C62	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	DECODER2_CFG[3]	3	Bypass mode for AUDIO_SPDIF_PACKER.	
	DECODER2_CFG[2]	2	Bypass mode for AUDIO_SPDIF_NONPCM_DECODER.	
	DECODER2_CFG[1:0]	1:0	DSP decoder input function selection. 00: HDMI non-PCM.	

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
			01: JPEG/MP3/AAC (card reader). 10: S/PDIF non-PCM. 11: SIF.	
31h (2C63h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
32h (2C64h)	REG2C64	7:0	Default : 0x00	Access : R/W
	CH1_CFG[7]	7	Audio output channel 1 enable setting. 0: Idle (power saving). 1: Enable.	
	CH1_CFG[6]	6	Audio output channel 1 source clock selection. 0: Normal. 1: synchronous to codec PLL. (while codec PLL ref clock is the same as this channel)	
	CH1_CFG[5]	5	Audio output channel 1 sampling rate converter setting. 0: Normal. 1: SRC mode.	
	CH1_CFG[4]	4	Audio output channel 1 over sampling rate setting. 0: 128 fs. 1: 256 fs.	
	CH1_CFG[3]	3	Audio output channel 1 sigma delta modulator enable setting. 0: Idle (power saving). 1: Enable.	
	CH1_CFG[2:0]	2:0	Audio output channel 1 source selection. 000: From DSP decoder1 output. 001: From DSP decoder2 output. 010: From audio ADC. 011: From input S/PDIF interface. 100: From input I2S interface. 101: From HDMI (sample stream 1 & 2). 110: From HDMI (sample stream 1 & 2). 111: From HDMI (sample stream 1 & 2).	
32h (2C65h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
33h	REG2C66	7:0	Default : 0x00	Access : R/W

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
(2C66h)	CH2_CFG[7]	7	Audio output channel 2 enable setting. 0: Idle (power saving). 1: Enable.	
	CH2_CFG[6]	6	Audio output channel 2 source clock selection. 0: Normal. 1: synchronous to codec PLL. (while codec PLL ref clock is the same as this channel)	
	CH2_CFG[5]	5	Audio output channel 2 sampling rate converter setting. 0: Normal. 1: SRC mode.	
	CH2_CFG[4]	4	Audio output channel 2 over sampling rate setting. 0: 128 fs. 1: 256 fs.	
	CH2_CFG[3]	3	Audio output channel 2 sigma delta modulator enable setting. 0: Idle (power saving). 1: Enable.	
	CH2_CFG[2:0]	2:0	Audio output channel 2 source selection. 000: from DSP decoder1 output. 001: from DSP decoder2 output.	
33h (2C67h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
34h (2C68h)	REG2C66	7:0	Default : 0x00	Access : R/W
	CH3_CFG[7]	7	Audio output channel 3 enable setting. 0: Idle (power saving). 1: Enable.	
	CH3_CFG[6]	6	Audio output channel 3 source clock selection. 0: Normal. 1: synchronous to codec PLL. (while codec PLL ref clock is the same as this channel)	
	CH3_CFG[5]	5	Audio output channel 3 sampling rate converter setting. 0: Normal. 1: SRC mode.	
	CH3_CFG[4]	4	Audio output channel 3 over sampling rate setting.	

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			0: 128 fs. 1: 256 fs.
	CH3_CFG[3]	3	Audio output channel 3 sigma delta modulator enable setting. 0: Idle (power saving). 1: Enable.
	CH3_CFG[2:0]	2:0	Audio output channel 3 source selection. 000: from DSP decoder1 output. 001: from DSP decoder2 output. 010: from audio ADC. 011: from input S/PDIF interface. 100: from input I2S interface. 101: from HDMI (sample stream 5 & 6). 110: from HDMI (sample stream 5 & 6). 111: from HDMI (sample stream 5 & 6).
34h (2C69h)	REG2C69	7:0	Default : - |||| Access : -
	-	7:0	Reserved.
35h (2C6Ah)	REG2C6A	7:0	Default : 0x00	Access : R/W
	CH4_CFG[7]	7	Audio output channel 4 enable setting. 0: Idle (power saving). 1: Enable.
	CH4_CFG[6]	6	Audio output channel 4 source clock selection. 0: Normal. 1: synchronous to codec PLL. (while codec PLL ref clock is the same as this channel)
	CH4_CFG[5]	5	Audio output channel 4 sampling rate converter setting. 0: Normal. 1: SRC mode.
	CH4_CFG[4]	4	Audio output channel 4 over sampling rate setting. 0: 128 fs. 1: 256 fs.
	CH4_CFG[3]	3	Audio output channel 4 sigma delta modulator enable setting. 0: Idle (power saving). 1: Enable.
	CH4_CFG[2:0]	2:0	Audio output channel 4 source selection.

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
			000: from DSP decoder1 output. 001: from DSP decoder2 output. 010: from audio ADC. 011: from input S/PDIF interface. 100: from input I2S interface. 101: from HDMI (sample stream 7 & 8). 110: from HDMI (sample stream 7 & 8). 111: from HDMI (sample stream 7 & 8).	
35h (2C6Bh)	REG2C6B	7:0	Default : -	Access : -
	-	7:0	Reserved.	
36h (2C6Ch)	REG2C6C	7:0	Default : 0x00	Access : R/W
	INPUT_REGEN_CFG[7]	7	HDMI clock auto re-generator function enable. 0: Disable. 1: Enable.	
	INPUT_REGEN_CFG[6]	6	SIF clock auto re-generator function enable. 0: Disable. 1: Enable.	
	INPUT_REGEN_CFG[5]	5	I2S clock auto re-generator function enable. 0: Disable. 1: Enable.	
	INPUT_REGEN_CFG[4]	4	S/PDIF clock auto re-generator function enable. 0: Disable. 1: Enable.	
	INPUT_REGEN_CFG[3]	3	DVB clock auto re-generator function enable. 0: Disable. 1: Enable.	
	-	2:0	Reserved.	
36h ~ 3Fh (2C6Dh ~ 2C7Fh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
40h (2C80h)	REG2C80	7:0	Default : 0x00	Access : R/W
	SPDIF_OUT_CS0[7:0]	7:0	S/PDIF output channel status [0:7] (refer to CR04.4).	
40h (2C81h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
41h (2C82h)	REG2C82	7:0	Default : 0x00	Access : R/W
	SPDIF_OUT_CS1[7:0]	7:0	S/PDIF output channel status [8:15] (refer to CR04.4).	

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
41h (2C83h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
42h (2C84h)	REG2C84	7:0	Default : 0x00	Access : R/W
	SPDIF_OUT_CS2[7:0]	7:0	S/PDIF output channel status [16:23] (refer to CR04.4).	
42h (2C85h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
43h (2C86h)	REG2C86	7:0	Default : 0x00	Access : R/W
	SPDIF_OUT_CS3[7:0]	7:0	S/PDIF output channel status [24:31] (refer to CR04.4).	
43h (2C87h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
44h (2C88h)	REG2C88	7:0	Default : 0x00	Access : R/W
	SPDIF_OUT_CS4[7:0]	7:0	S/PDIF output channel status [32:39] (refer to CR04.4).	
44h (2C89h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
45h (2C8Ah)	REG2C8A	7:0	Default : 0x00	Access : R/W
	SPDIF_OUT_CFG[7]	7	Audio output channel S/PDIF enable setting. 0: Idle (power saving). 1: Enable.	
	SPDIF_OUT_CFG[6]	6	Reset S/PDIF output modules. This bit shall be toggled after data or clock is changed for S/PDIF output modules. 0: Normal. 1: Reset (synchronous input Fs and output Fs).	
	SPDIF_OUT_CFG[5]	5	Audio output channel S/PDIF sampling rate converter setting. 0: Normal. 1: SRC mode.	
	SPDIF_OUT_CFG[4]	4	Enable channel status insertion for output S/PDIF module. 0: Disable (refer from S/PDIF / HDMI input channel status). 1: Enable (refer from SPDIF_OUT_CS0..4).	
	SPDIF_OUT_CFG[3]	3	Audio output channel 1/2/3/4 test source selection.	

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
			0: Normal (16 bits). 1: From DSP output 24 bit interface (only without SRC) (only for SEL_SPDIF_CH[1:0]).	
	SPDIF_OUT_CFG[2:0]	2:0	Audio output channel S/PDIF source selection (16/24 bits). 000: From audio output channel 1. 001: From audio output channel 2. 010: From audio output channel 3. 011: From audio output channel 4. 100: HDMI bypass. 101: DVB non-PCM output. 11x: Reserved.	
45h (2C8Bh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
46h (2C8Ch)	REG2C8C	7:0	Default : 0x00	Access : R/W
	I2S_OUT1_CFG[7:0]	7	Automatically synchronize input and output timing of the I2S1 encoder. 0: Disable. 1: Enable.	
	I2S_OUT1_CFG[6:4]	6:4	Clock frequency select for AUMCKO output pin (I2S MCLK). 000: Synthesizer 64 Fs. 001: Synthesizer 128 Fs. 010: Synthesizer 256 Fs. 011: Test clock (only for VLSI designer). 100: PLL 64 Fs. 101: PLL 128 Fs. 110: PLL 256 Fs. 111: PLL 384 Fs.	
	I2S_OUT1_CFG[3]	3	Output I2S interface format. 0: I2S-justified (standard format). 1: Left-justified.	
	I2S_OUT1_CFG[2:0]	2:0	Output I2S interface encoder word width (bit rate). 000: Synthesizer 16 clock cycles per sample word (16 bit). 001: PLL 24 clock cycles per sample word (24 bit). 010: Synthesizer 32 clock cycles per sample word (32 bit).	

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
			011: Synthesizer 64 clock cycles per sample word (test). 100: PLL 16 clock cycles per sample word (16 bit). 101: PLL 24 clock cycles per sample word (24 bit). 110: PLL 32 clock cycles per sample word (32 bit). 111: PLL 64 clock cycles per sample word (test).	
46h (2C8Dh)	REG2C8D	7:0	Default : 0x00	Access : R/W
	I2S_OUT1_CFG[15]	7	Audio output channel I2S enable setting. 0: Idle (power saving). 1: Enable.	
	I2S_OUT1_CFG[14]	6	Reset I2S output modules. This bit shall be toggled after data or clock is changed for I2S output modules. 0: Normal. 1: Reset (synchronous input Fs and output Fs).	
	-	5	Reserved.	
	I2S_OUT1_CFG[12]	4	Automatically synchronize input and output timing of the S/PDIF encoder. Set to 0 in SRC mode. 0: Disable. 1: Enable.	
	I2S_OUT1_CFG[11]	3	Audio output channel 1/2/3/4 test source selection. 0: Normal (16 bits). 1: From DSP output 24 bit interface (only without SRC) (only for SEL_I2S_CH[1:0]).	
	I2S_OUT1_CFG[10]	2	Audio output channel I2S source selection (24 bits). 0: Normal (following SEL_I2S_CH[1:0]). 1: From HDMI audio link.	
	I2S_OUT1_CFG[9:8]	1:0	Audio output channel I2S source selection (16/24 bits). 00: From audio output channel 1. 01: From audio output channel 2. 10: From audio output channel 3. 11: From audio output channel 4.	
47h (2C8Eh)	REG2C8E	7:0	Default : 0x00	Access : R/W
	I2S_OUT2_CFG[7]	7	Automatically synchronize input and output timing of the I2S2 encoder. 0: Disable. 1: Enable.	

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
	I2S_OUT2_CFG[6:4]	6:4	Clock frequency select for AUMCKO output pin (I2S MCLK). 000: Synthesizer 64 Fs. 001: Synthesizer 128 Fs. 010: Synthesizer 256 Fs. 011: PLL 384 Fs. 100: PLL 64 Fs. 101: PLL 128 Fs. 110: PLL 256 Fs. 111: PLL 384 Fs.	
	I2S_OUT2_CFG[3]	3	Output I2S interface format. 0: I2S-justified (standard format). 1: Left-justified.	
	I2S_OUT2_CFG[2:0]	2:0	Output I2S interface encoder word width (bit rate). 000: Synthesizer 16 clock cycles per sample word (16 bit). 001: PLL 24 clock cycles per sample word (24 bit). 010: Synthesizer 32 clock cycles per sample word (32 bit). 011: Reserved. 100: PLL 16 clock cycles per sample word (16 bit). 101: PLL 24 clock cycles per sample word (24 bit). 110: PLL 32 clock cycles per sample word (32 bit). 111: Reserved.	
47h (2C8Fh)	REG2C8F	7:0	Default : 0x00	Access : R/W
	I2S_OUT2_CFG[15]	7:0	Audio output channel I2S enable setting. 0: Idle (power saving). 1: Enable.	
	I2S_OUT2_CFG[14]	6	Reset I2S output modules. This bit shall be toggled after data or clock is changed for I2S output modules. 0: Normal. 1: Reset (synchronous input Fs and output Fs).	
	-	5:4	Reserved.	
	I2S_OUT2_CFG[11]	3	Audio output channel 1/2/3/4 test source selection. 0: Normal (16 bits). 1: From DSP output 24 bit interface (only without SRC) (only for SEL_I2S_CH[1:0]).	

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
	-	2	Reserved.	
	I2S_OUT2_CFG[9:8]	1:0	Audio output channel I2S source selection (16/24 bits). 00: From audio output channel 1. 01: From audio output channel 2. 10: From audio output channel 3. 11: From audio output channel 4.	
48h (2C90h)	REG2C90	7:0	Default : 0x0F	Access : R/W
	PAD_CFG[7:6]	7:6	I2S output mux control. 00: Two 2-ch I2S interfaces. 01: One 8-ch I2S interface. 10: DSD output interface. 11: Reserved.	
	-	5:3	Reserved.	
	PAD_CFG[2]	2	Output enable for the second I2S interface pins. 0: Enable. 1: Tri-stated.	
	PAD_CFG[1]	1	Output enable for the first I2S interface pins. 0: Enable. 1: Tri-stated.	
	PAD_CFG[0]	0	Output enable for SPDIFO output pin (S/PDIF output). 0: Enable. 1: Tri-stated.	
48h (2C91h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
49h (2C92h)	REG2C92	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	MUTE_CFG[5:4]	5:4	Select source for output AUMUTE pin (audio mute). 00: From audio DSP channel 1 mute control. 01: From audio DSP channel 2 mute control. 10: From audio DSP channel 3 mute control. 11: From audio DSP channel 4 mute control.	
	-	3	Reserved.	
	MUTE_CFG[2]	2	Mute function setting on AUMUTE pin (audio mute). 0: Disable. 1: Output is active.	

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
	MUTE_CFG[1]	1	Configure AUMUTE output polarity (audio mute). 0: Active-low for mute. 1: Active-high for mute.	
	MUTE_CFG[0]	0	Output enable for AUMUTE output pin (audio mute). 0: Enable. 1: Tri-stated.	
49h (2C93h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
4Ah (2C94h)	REG2C94	7:0	Default : 0x00	Access : R/W
	MUTE_CTRL1[7:0]	7	Enable audio DSP channel 1 mute from SIF mute. 0: Disable. 1: Enable.	
	MUTE_CTRL1[6]	6	Enable audio DSP channel 1 mute when DSD audio stream is received from HDMI receiver. 0: Disable. 1: Enable.	
	MUTE_CTRL1[5]	5	Enable audio DSP channel 1 mute from HDMI (flat sample, decode error, PLL unlock, etc). 0: Disable. 1: Enable.	
	MUTE_CTRL1[4]	4	Enable audio DSP channel 1 mute when AVMUTE signal is received from HDMI receiver. 0: Disable. 1: Enable.	
	MUTE_CTRL1[3]	3	Enable audio DSP channel 1 mute when non-PCM audio stream is received from HDMI receiver. 0: Disable. 1: Enable.	
	MUTE_CTRL1[2]	2	Enable audio DSP channel 1 mute when SPDIF input decoding error occurs. 0: Disable. 1: Enable.	
	MUTE_CTRL1[1]	1	Enable audio DSP channel 1 mute when non-PCM audio stream is received from SPDIF input. 0: Disable. 1: Enable.	
	MUTE_CTRL1[0]	0	Enable audio DSP channel 1 force mute control. 0: Mute.	

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
			1: Normal.	
4Ah (2C95h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
4Bh (2C96h)	REG2C96	7:0	Default : 0x00	Access : R/W
	MUTE_CTRL2[7:0]	7	Enable audio DSP channel 2 mute from SIF mute. 0: Disable. 1: Enable.	
	MUTE_CTRL2[6]	6	Enable audio DSP channel 2 mute when DSD audio stream is received from HDMI receiver. 0: Disable. 1: Enable.	
	MUTE_CTRL2[5]	5	Enable audio DSP channel 2 mute from HDMI (flat sample, decode error, PLL unlock, etc). 0: Disable. 1: Enable.	
	MUTE_CTRL2[4]	4	Enable audio DSP channel 2 mute when AVMUTE signal is received from HDMI receiver. 0: Disable. 1: Enable.	
	MUTE_CTRL2[3]	3	Enable audio DSP channel 2 mute when non-PCM audio stream is received from HDMI receiver. 0: Disable. 1: Enable.	
	MUTE_CTRL2[2]	2	Enable audio DSP channel 2 mute when SPDIF input decoding error occurs. 0: Disable. 1: Enable.	
	MUTE_CTRL2[1]	1	Enable audio DSP channel 2 mute when non-PCM audio stream is received from SPDIF input. 0: Disable. 1: Enable.	
	MUTE_CTRL2[0]	0	Enable audio DSP channel 2 force mute control. 0: Mute. 1: Normal.	
4Bh (2C97h)	REG2C97	7:0	Default : -	Access : -
	-	7:0	Reserved.	
4Ch	REG2C98	7:0	Default : 0x00	Access : R/W

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
(2C98h)	MUTE_CTRL3[7:0]	7	Enable audio DSP channel 3 mute from SIF mute. 0: Disable. 1: Enable.	
	MUTE_CTRL3[6]	6	Enable audio DSP channel 3 mute when DSD audio stream is received from HDMI receiver. 0: Disable. 1: Enable.	
	MUTE_CTRL3[5]	5	Enable audio DSP channel 3 mute from HDMI (flat sample, decode error, PLL unlock, etc). 0: Disable. 1: Enable.	
	MUTE_CTRL3[4]	4	Enable audio DSP channel 3 mute when AVMUTE signal is received from HDMI receiver. 0: Disable. 1: Enable.	
	MUTE_CTRL3[3]	3	Enable audio DSP channel 3 mute when non-PCM audio stream is received from HDMI receiver. 0: Disable. 1: Enable.	
	MUTE_CTRL3[2]	2	Enable audio DSP channel 3 mute when SPDIF input decoding error occurs. 0: Disable. 1: Enable.	
	MUTE_CTRL3[1]	1	Enable audio DSP channel 3 mute when non-PCM audio stream is received from SPDIF input. 0: Disable. 1: Enable.	
	MUTE_CTRL3[0]	0	Enable audio DSP channel 3 force mute control. 0: mute. 1: Normal.	
4Ch (2C99h)	REG2C99	7:0	Default : -	Access : -
	-	7:0	Reserved.	
4Dh (2C9Ah)	REG2C9A	7:0	Default : 0x00	Access : R/W
	MUTE_CTRL4[7:0]	7	Enable audio DSP channel 4 mute from SIF mute. 0: Disable. 1: Enable.	
	MUTE_CTRL4[6]	6	Enable audio DSP channel 4 mute when DSD audio stream is received from HDMI receiver.	

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
			0: Disable. 1: Enable.	
	MUTE_CTRL4[5]	5	Enable audio DSP channel 4 mute from HDMI (flat sample, decode error, PLL unlock, etc). 0: Disable. 1: Enable.	
	MUTE_CTRL4[4]	4	Enable audio DSP channel 4 mute when AVMUTE signal is received from HDMI receiver. 0: Disable. 1: Enable.	
	MUTE_CTRL4[3]	3	Enable audio DSP channel 4 mute when non-PCM audio stream is received from HDMI receiver. 0: Disable. 1: Enable.	
	MUTE_CTRL4[2]	2	Enable audio DSP channel 4 mute when SPDIF input decoding error occurs. 0: Disable. 1: Enable.	
	MUTE_CTRL4[1]	1	Enable audio DSP channel 4 mute when non-PCM audio stream is received from SPDIF input. 0: Disable. 1: Enable.	
	MUTE_CTRL4[0]	0	Enable audio DSP channel 4 force mute control. 0: mute. 1: Normal.	
4Dh (2C9Bh)	REG2C9B	7:0	Default : -	Access : -
	-	7:0	Reserved.	
4Dh ~ 4Fh (2C9Ch ~ 2C9Fh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
50h (2CA0h)	REG2CA0	7:0	Default : 0xA9	Access : R/W
	CODEC_SYNTH[7:0]	7:0	CODEC synthesizer N.f = 6.10; 256fs = 214 / N.f.	
50h (2CA1h)	REG2CA1	7:0	Default : 0x45	Access : R/W
	CODEC_SYNTH[15:8]	7:0	Please see description of '2CA0h'.	
51h (2CA2h)	REG2CA2	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	PLL_REF_CFG[3]	3	Audio codec PLL reference clock control.	

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
			0: Stop. 1: Enable.	
	PLL_REF_CFG[2:0]	3:0	Audio codec PLL reference clock selection. 000: From DSP decoder1 input. 001: From DSP decoder2 input. 010: From audio ADC. 011: From input S/PDIF interface. 100: From input I2S interface. 101: From HDMI. 110: From HDMI. 111: From HDMI.	
51h (2CA3h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
52h (2CA4h)	**REG2CA4**	7:0	**Default : 0x00**	**Access : R/W**
	CLK_CFG0[7:6]	7:6	Audio SIF FM demodulator clock source selection. 00: 214/4. 01: 214/2. 10: CLK_ADC. 11: CLK_CIC.	
	CLK_CFG0[5]	5	Audio SIF I-clamp clock selection. 0: Following DSP230 clock. 1: 25 MHz (214/8).	
	CLK_CFG0[4]	4	Audio INV_CLK_256FS_PCM_DELAY invert setting. 0: Normal. 1: Invert.	
	CLK_CFG0[3]	3	Audio SIF channel enable setting. 0: Idle (power saving). 1: Enable.	
	CLK_CFG0[2]	2	Audio HDMI ACR engine selection. 0: Normal mode. 1: Test mode (CTS_N digital synthesizer).	
	CLK_CFG0[1:0]	1:0	Audio codec PLL post divider stage 2 selection. 00: Divide by 1. 01: Divide by 2. 10: Divide by 3. 11: Divide by 4.	
52h (2CA5h)	**REG2CA5**	7:0	**Default : 0x00**	**Access : R/W**
	CLK_CFG0[15]	7	Audio CLK_150MHZ_ZR_MAC selection.	

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			0: SIF PLL 8X /2.5. 1: SIF PLL 8X /3.
	CLK_CFG0[14:13]	6:5	Audio CLK_256FS_ADC_IN selection. 00: Codec synthesizer 128 FS. 01: Codec synthesizer 256 FS. 10: Codec PLL 128 FS. 11: Codec PLL 256 FS.
	CLK_CFG0[12]	4	Audio CLK_SPDIF_SYNTH selection. 0: 214 MHz. 1: 107 MHz.
	CLK_CFG0[11]	3	Audio CLK_I2S_SYNTH selection. 0: 214 MHz. 1: 107 MHz.
	CLK_CFG0[10]	2	Audio CLK_SIF_SYNTH selection. 0: 214 MHz. 1: 107 MHz.
	CLK_CFG0[9]	1	Audio CLK_CODEC_SYNTH selection. 0: 214 MHz. 1: 107 MHz.
	CLK_CFG0[8]	0	Audio CLK_HDMI_SYNTH selection. 0: 214 MHz. 1: 107 MHz.
53h (2CA6h)	REG2CA6	7:0	Default : 0x00 — Access : R/W
	CLK_CFG1[7:0]	7	Audio CLK_SIF_ADC_R2B invert setting. 0: Normal. 1: Invert.
	CLK_CFG1[6]	6	Audio CLK_SIF_ADC_R2B_FIFO invert setting. 0: Normal. 1: Invert.
	CLK_CFG1[5]	5	Audio CLK_SIF_ADC_CIC invert setting. 0: Normal. 1: Invert.
	CLK_CFG1[4]	4	Audio CLK_DSP_230 invert setting. 0: Normal. 1: Invert.
	CLK_CFG1[3]	3	Audio CLK_HDMI_DECODER invert setting. 0: Normal. 1: Invert.

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
	CLK_CFG1[2]	2	Audio CLK_64FS_HDMI_DSD invert setting. 0: Normal. 1: Invert.	
	CLK_CFG1[1]	1	Audio CLK_BCLK_I2S_DECODER invert setting. 0: Normal. 1: Invert.	
	CLK_CFG1[0]	0	Audio CLK_BCLK_I2S_ENCODER invert setting. 0: Normal. 1: Invert.	
53h (2CA7h)	REG2CA7	7:0	Default : 0x00	Access : R/W
	CLK_CFG1[15:8]	7	Audio CLK_MCLK_I2S_ENCODER invert setting. 0: Normal. 1: Invert.	
	CLK_CFG1[14]	6	Audio CLK_SPDIF_ENCODER invert setting. 0: Normal. 1: Invert.	
	CLK_CFG1[13]	5	Audio CLK_SPDIF_DECODER invert setting. 0: Normal. 1: Invert.	
	CLK_CFG1[12]	4	Audio CLK_SPDIF_SYNTH invert setting. 0: Normal. 1: Invert.	
	CLK_CFG1[11]	3	Audio CLK_I2S_SYNTH invert setting. 0: Normal. 1: Invert.	
	CLK_CFG1[10]	2	Audio CLK_SIF_SYNTH invert setting. 0: Normal. 1: Invert.	
	CLK_CFG1[9]	1	Audio CLK_CODEC_SYNTH invert setting. 0: Normal. 1: Invert.	
	CLK_CFG1[8]	0	Audio CLK_HDMI_SYNTH invert setting. 0: Normal. 1: Invert.	
54h (2CA8h)	REG2CA8	7:0	Default : 0x00	Access : R/W
	CLK_CFG2[7]	7:0	Audio CLK_256FS_CH4_IN invert setting. 0: Normal.	

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
			1: Invert.	
	CLK_CFG2[6]	6	Audio CLK_256FS_CH3_IN invert setting. 0: Normal. 1: Invert.	
	CLK_CFG2[5]	5	Audio CLK_256FS_CH2_IN invert setting. 0: Normal. 1: Invert.	
	CLK_CFG2[4]	4	Audio CLK_256FS_CH1_IN invert setting. 0: Normal. 1: Invert.	
	CLK_CFG2[3]	3	Audio CLK_214M_CH4_SRC invert setting. 0: Normal. 1: Invert.	
	CLK_CFG2[2]	2	Audio CLK_214M_CH3_SRC invert setting. 0: Normal. 1: Invert.	
	CLK_CFG2[1]	1	Audio CLK_214M_CH2_SRC invert setting. 0: Normal. 1: Invert.	
	CLK_CFG2[0]	0	Audio CLK_214M_CH1_SRC invert setting. 0: Normal. 1: Invert.	
54h (2CA9h)	REG2CA9	7:0	Default : 0x00	Access : R/W
	CLK_CFG2[15]	7	Audio CLK_256FS_CH4_OUT invert setting. 0: Normal. 1: Invert.	
	CLK_CFG2[14]	6	Audio CLK_256FS_CH3_OUT invert setting. 0: Normal. 1: Invert.	
	CLK_CFG2[13]	5	Audio CLK_256FS_CH2_OUT invert setting. 0: Normal. 1: Invert.	
	CLK_CFG2[12]	4	Audio CLK_256FS_CH1_OUT invert setting. 0: Normal. 1: Invert.	
	CLK_CFG2[11]	3	Audio CLK_214M_I2S_SRC invert setting. 0: Normal.	

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
			1: Invert.	
	CLK_CFG2[10]	2	Audio CLK_214M_SPDIF_SRC invert setting. 0: Normal. 1: Invert.	
	CLK_CFG2[9]	1	Audio CLK_256FS_ADC_IN invert setting. 0: Normal. 1: Invert.	
	CLK_CFG2[8]	0	Audio CLK_CODEC_PLL_REF invert setting. 0: Normal. 1: Invert.	
55h (2CAAh)	**REG2CAA**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLK_CFG3[7]	7	Audio CLK_ICE_DSP_230 enable setting. 0: Idle (power saving). 1: Enable.	
	CLK_CFG3[6]	6	Audio CLK_25MHZ_I_CLAMP enable setting. 0: Idle (power saving). 1: Enable.	
	CLK_CFG3[5]	5	Audio CLK_SPDIF_DECODER enable setting. 0: Idle (power saving). 1: Enable.	
	CLK_CFG3[4]	4	Audio CLK_SPDIF_SYNTH enable setting. 0: Idle (power saving). 1: Enable.	
	CLK_CFG3[3]	3	Audio CLK_I2S_SYNTH enable setting. 0: Idle (power saving). 1: Enable.	
	CLK_CFG3[2]	2	Audio CLK_SIF_SYNTH enable setting. 0: Idle (power saving). 1: Enable.	
	CLK_CFG3[1]	1	Audio CLK_CODEC_SYNTH enable setting. 0: Idle (power saving). 1: Enable.	
	CLK_CFG3[0]	0	Audio CLK_HDMI_SYNTH enable setting. 0: Idle (power saving). 1: Enable.	
55h (2CABh)	**REG2CAB**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLK_CFG3[15]	7	Audio CLK_DSP_230 enable setting.	

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			0: Idle (power saving). 1: Enable.
	CLK_CFG3[14]	6	Audio CLK_HDMI_DECODER enable setting. 0: Idle (power saving). 1: Enable.
	CLK_CFG3[13]	5	Audio CLK_64FS_HDMI_DSD enable setting. 0: Idle (power saving). 1: Enable.
	CLK_CFG3[12]	4	Audio CLK_BCLK_I2S_DECODER enable setting. 0: Idle (power saving). 1: Enable.
	CLK_CFG3[11]	3	Audio CLK_150MHZ_ZR_MAC enable setting. 0: Idle (power saving). 1: Enable.
	CLK_CFG3[10]	2	Audio CLK_256FS_ADC_IN enable setting. 0: Idle (power saving). 1: Enable.
	CLK_CFG3[9]	1	Audio DAC clock force enable setting. 0: Normal. 1: Force enable clock (only for testing).
	CLK_CFG3[8]	0	Audio test clock enable setting. 0: Idle (power saving). 1: Enable.
56h (2CACh)	REG2CAC	7:0	Default : 0x00 Access : R/W
	-	7	Reserved.
	CLK_CFG4[6]	6	Audio CLK_CARD_READER_SYNTH selection. 0: 214 MHz. 1: 107 MHz.
	CLK_CFG4[5]	5	Audio CLK_ CLK_CARD_READER_SYNTH invert setting. 0: Normal. 1: Invert.
	CLK_CFG4[4]	4	Audio CLK_CARD_READER_SYNTH enable setting. 0: Idle (power saving). 1: Enable.
	CLK_CFG4[3]	3	Audio DAC output SRC clock source selection. 0: Select codec PLL output clock 256 fs.

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
			1: Select codec PLL reference clock 256 fs.	
	CLK_CFG4[2]	2	Audio CLK_214M_I2S_OUT2_SRC invert setting. 0: Normal. 1: Invert.	
	CLK_CFG4[1]	1	Audio CLK_BCLK_I2S_OUT2_ENCODER invert setting. 0: Normal. 1: Invert.	
	CLK_CFG4[0]	0	Audio CLK_MCLK_I2S_OUT2_ENCODER invert setting. 0: Normal. 1: Invert.	
56h (2CADh)	REG2CAD	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	CLK_CFG4[14]	6	Audio 768fs clock system source selection. 0: Analog codec PLL. 1: Digital 768fs synthesizer.	
	CLK_CFG4[13]	5	Audio DAC SRC clock 256fs selection. 0: From 768fs clock system. 1: From Xtal 14.31818MHz.	
	CLK_CFG4[12]	4	Audio CLK_768FS_PLL_SYNTH selection. 0: 214 MHz. 1: 107 MHz.	
	CLK_CFG4[11]	3	Audio CLK_DVB_FIX_SYNTH selection. 0: 214 MHz. 1: 107 MHz.	
	CLK_CFG4[10]	2	Audio CLK_DVB_SYNC_SYNTH selection. 0: 214 MHz. 1: 107 MHz.	
	CLK_CFG4[9]	1	Audio CLK_27MHZ_DVB_REF source selection. 0: 27 MHz. 1: 13.5 MHz.	
	CLK_CFG4[8]	0	Audio DVB clock source selection. 0: Sync mode (following system clock). 1: Fix mode (DSP N.f mode).	
57h (2CAEh)	REG2CAE	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	CLK_CFG5[6]	6	Audio CLK_768FS_PLL_SYNTH invert setting.	

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
			0: Normal. 1: Invert.	
	CLK_CFG5[5]	5	Audio CLK_128FS_SPDIF_NON_PCM_TRUE invert setting. 0: Normal. 1: Invert.	
	CLK_CFG5[4]	4	Audio CLK_256FS_DVB_SYNC_SYNTH_TRUE invert setting. 0: Normal. 1: Invert.	
	CLK_CFG5[3]	3	Audio CLK_214MHZ_DVB_FIX_SYNTH invert setting. 0: Normal. 1: Invert.	
	CLK_CFG5[2]	2	Audio CLK_214MHZ_DVB_SYNC_SYNTH invert setting. 0: Normal. 1: Invert.	
	CLK_CFG5[1]	1	Audio CLK_256FS_DVB_TIMING_GEN invert setting (INV_DSP_DECODER1_ TIMING_GEN). 0: Normal. 1: Invert.	
	CLK_CFG5[0]	0	Audio CLK_256FS_SIF_TIMING_GEN invert setting (INV_DSP_DECODER2_ TIMING_GEN). 0: Normal. 1: Invert.	
57h (2CAFh)	REG2CAF	7:0	Default : 0x00	Access : R/W
	CLK_CFG5[15]	7	Enable external clock.	
	CLK_CFG5[14]	6	Audio CLK_14318KHZ_FREE enable setting. 0: Idle (power saving). 1: Enable.	
	-	5	Reserved.	
	CLK_CFG5[12]	4	Audio CLK_ALL_768FS_SYNTH enable setting. 0: Idle (power saving). 1: Enable.	
	CLK_CFG5[11]	3	Audio CLK_214MHZ_DVB_FIX_SYNTH enable setting. 0: Idle (power saving). 1: Enable.	

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
	CLK_CFG5[10]	2	Audio CLK_ALL_DVB_SYNC_SYNTH enable setting (214 Mhz / 256 fs feedback / 270 Mhz). 0: Idle (power saving). 1: Enable.	
	CLK_CFG5[9]	1	Audio CLK_256FS_DVB_TIMING_GEN enable setting (Audio CLK_ DSP_DECODER1_TIMING_GEN enable setting). 0: Idle (power saving). 1: Enable.	
	CLK_CFG5[8]	0	Audio CLK_256FS_SIF_TIMING_GEN enable setting (Audio CLK_ DSP_DECODER2_TIMING_GEN enable setting). 0: Idle (power saving). 1: Enable.	
58h (2CB0h)	REG2CB0	7:0	Default : 0x00	Access : R/W
	CLK_CFG6[7:6]	7:6	Audio test clock post divider selection. 00: /1. 01: /2. 10: /4. 11: /8.	
	CLK_CFG6[5:0]	5:0	Audio test clock selection. 00h: CLK_50MHZ_SIF_ADC_R2B_Z. 01h: CLK_50MHZ_SIF_ADC_R2B_FIFO_OUT_Z. 02h: CLK_100MHZ_SIF_ADC_CIC_Z. 03h: CLK_150MHZ_DSP_230_Z. 04h: CLK_ICE_DSP_230_Z. 05h: CLK_25MHZ_I_CLAMP_Z. 06h: CLK_150MHZ_ZR_MAC_GATE_Z. 07h: CLK_BCLK_I2S_DECODER_Z. 08h: CLK_BCLK_I2S_ENCODER_Z. 09h: CLK_150MHZ_ZR_MAC_FREE_Z. 0Ah: CLK_128FS_SPDIF_ENCODER_Z. 0Bh: CLK_128FS_SPDIF_DECODER_Z. 0Ch: CLK_214MHZ_SPDIF_SYNTH_Z. 0Dh: CLK_214MHZ_I2S_SYNTH_Z. 0Eh: CLK_214MHZ_SIF_SYNTH_Z. 0Fh: CLK_214MHZ_CODEC_SYNTH_Z.	

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			10h: CLK_256FS_CHANNEL_1_IN_Z.
			11h: CLK_256FS_CHANNEL_2_IN_Z.
			12h: CLK_256FS_CHANNEL_3_IN_Z.
			13h: CLK_256FS_CHANNEL_4_IN_Z.
			14h: CLK_214MHZ_CHANNEL_1_SRC_Z.
			15h: CLK_214MHZ_CHANNEL_2_SRC_Z.
			16h: CLK_214MHZ_CHANNEL_3_SRC_Z.
			17h: CLK_214MHZ_CHANNEL_4_SRC_Z.
			18h: CLK_256FS_CHANNEL_1_OUT_Z.
			19h: CLK_256FS_CHANNEL_2_OUT_Z.
			1Ah: CLK_256FS_CHANNEL_3_OUT_Z.
			1Bh: CLK_256FS_CHANNEL_4_OUT_Z.
			1Ch: CLK_256FS_ADC_IN_Z.
			1Dh: CLK_256FS_REF_CODEC_PLL_Z.
			1Eh: CLK_128FS_HDMI_Z.
			1Fh: CLK_100MHZ_BIU_WR9_GATE_Z.
			20h: CLK_100MHZ_FREE_Z.
			21h: CLK_214MHZ_CHANNEL_I2S_SRC_Z.
			22h: CLK_214MHZ_CHANNEL_SPDIF_SRC_Z.
			23h: CLK_214MHZ_HDMI_SYNTH_Z.
			24h: CLK_64FS_HDMI_DSD_Z.
			25h: CLK_128FS_HDMI_TRUE_Z.
			26h: CLK_128FS_SPDIF_DECODER_TRUE_Z.
			27h: CLK_256FS_PCM_DELAY_Z.
			28h: CLK_FM_DEMODULATOR_Z.
			29h: CLK_BCLK_I2S_OUT2_ENCODER_Z.
			2Ah: CLK_MCLK_I2S_OUT2_ENCODER_Z.
			2Bh: CLK_214MHZ_CHANNEL_I2S_OUT2_SRC_Z.
			2Ch: CLK_214MHZ_DVB_FIX_SYNTH_Z.
			2Dh: CLK_214MHZ_DVB_SYNC_SYNTH_Z.
			2Eh: CLK_256FS_DVB_SYNC_SYNTH_TRUE_Z.
			2Fh: CLK_256FS_DVB_TIMING_GEN_Z.
			30h: CLK_256FS_SIF_TIMING_GEN_Z.
			31h: CLK_256FS_CHANNEL_2_OUT_DAC_X1_Z.
			32h: CLK_128FS_SPDIF_NON_PCM_TRUE_Z.
			33h: CLK_270MHZ_DVB_REF_Z.

Audio 0 Register (Bank = 2C)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
			34h: CLK_14318KHZ_FREE_Z.
			35h: CLK_214MHZ_768FS_PLL_SYNTH_Z.
			36h: CLK_768FS_SYNTH_FEED_BACK_256_FS_DIV6_Z.
			37h: CLK_768FS_PLL_REF_128_Z.
			38h: CLK_128FS_CTS_N_SYNTH_FEED_BACK_Z.
			39h: CLK_214MHZ_CARD_READER_FIX_SYNTH_Z.
			3Ah~3Fh: Reserved.
58h (2CB1h)	REG2CB1	7:0	Default : 0x00 — Access : R/W
	-	7:6	Reserved.
	CLK_CFG6[13]	5	Audio CLK_DSP_216 enable setting. 0: Idle (power saving). 1: Enable.
	CLK_CFG6[12]	4	Audio CLK_ CLK_DSP_216 invert setting. 0: Normal. 1: Invert.
	CLK_CFG6[11:10]	3:2	Audio SIF DSP 216 clock source selection. 00: SIF PLL 8X/2. 01: SIF PLL 8X/2.5. 10: SIF PLL 8X/3. 11: SIF PLL 8X/4.
	CLK_CFG6[9:8]	1:0	Audio SIF DSP 216 clock source selection. 00: SIF PLL 8X/2. 01: SIF PLL 8X/2.5. 10: SIF PLL 8X/3. 11: SIF PLL 8X/4.
59h (2CB2h)	REG2CB2	7:0	Default : 0x00 — Access : R/W
	SYNTH_EXPANDER[7]	7	Lock current frequency of I2S synthesizer. 0: Normal. 1: Lock current frequency.
	SYNTH_EXPANDER[6]	6	CARD_READER 256 fs synthesizer clock pulse expander. 0: Normal (1T width). 1: Expander (2T width).
	SYNTH_EXPANDER[5]	5	DVB_FIX 256 fs synthesizer clock pulse expander. 0: Normal (1T width). 1: Expander (2T width).

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
	SYNTH_EXPANDER[4]	4	DVB_SYNC 256 fs synthesizer clock pulse expander. 0: Normal (1T width). 1: Expander (2T width).	
	SYNTH_EXPANDER[3]	3	Band width of I2S synthesizer. 0: Low band width. 1: High band width.	
	SYNTH_EXPANDER[2]	2	S/PDIF 256 fs synthesizer clock pulse expander. 0: Normal (1T width). 1: Expander (2T width).	
	SYNTH_EXPANDER[1]	1	CODEC 256 fs synthesizer clock pulse expander. 0: Normal (1T width). 1: Expander (2T width).	
	SYNTH_EXPANDER[0]	0	Band width of SIF 32k synthesizer. 0: Low band width. 1: High band width.	
59h (2CB3h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
5Ah (2CB4h)	REG2CB4	7:0	Default : 0x00	Access : R/W
	SYNTH_768_CONFIG_0[7:0]	7:0	Synthesizer 768 fs PDF frequency setting X=M=N.	
5Ah (2CB5h)	REG2CB5	7:0	Default : 0x00	Access : R/W
	SYNTH_768_CONFIG_0[15:8]	7:0	Please see description of '2CB4h'.	
5Bh (2CB6h)	REG2CB6	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	SYNTH_768_CONFIG_1[2]	2	Lock current frequency of SYNTH_768 synthesizer. 0: Normal. 1: Lock current frequency.	
	SYNTH_768_CONFIG_1[1]	1	Audio SYNTH_768 synthesizer Cs gain selection. 0: Normal. 1: Enhancement (smaller Cs).	
	SYNTH_768_CONFIG_1[0]	0	Audio SYNTH_768 synthesizer Cp gain selection. 0: Normal. 1: Enhancement (smaller Cp).	
5Bh (2CB7h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
5Ch (2CB8h)	REG2CB8	7:0	Default : -	Access : RO
	STS_SYNTH_768_FREQ[7:0]	7:0	Audio SYNTH_768 frequency value.	

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
5Ch (2CB9h)	REG2CB9	7:0	Default : -	Access : RO
	STS_SYNTH_768_FREQ[15]	7	Audio SYNTH_768 input signal detect. 0: Signal detected. 1: No signal input.	
	STS_SYNTH_768_FREQ[14:8]	6:0	Audio SYNTH_768 frequency value.	
60h (2CC0h)	REG2CC0	7:0	Default : 0x00	Access : R/W
	ASIF_CONFIG0[7:4]	7:4	Reserved.	
	ASIF_CONFIG0[3]	3	Audio SIF ADC control. 0: Normal. 1: Power-down.	
	ASIF_CONFIG0[2]	2	Audio SIF I-clamp control. 0: Normal. 1: Power-down.	
	ASIF_CONFIG0[1]	1	Audio SIF ADC 8 bits voltage dither mode (test mode). 0: Disable. 1: Enable. Note: LSB 3-bit dither summation (1, ½, ¼).	
	ASIF_CONFIG0[0]	0	Gain calibration reference voltage source select. 0: 0.1V. 1: 0.6V (only for VLSI designer).	
60h (2CC1h)	REG2CC1	7:0	Default : 0x00	Access : R/W
	ASIF_CONFIG0[15:14]	7:6	Audio SIF ADC bias generator reference current selection. 00: 20uA. 01: 15uA. 10: 30uA. 11: 25uA.	
	ASIF_CONFIG0[13]	5	Audio SIF ADC band-gap chopping control (ADC clock /8). 0: Disable. 1: Enable.	
	ASIF_CONFIG0[12]	4	Audio SIF ADC GMC filter control. 0: Enable. 1: Power-down.	
	ASIF_CONFIG0[11]	3	Audio SIF ADC GMC filter bias control. 0: Enable.	

Audio 0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			1: Power-down.	
	-	2	Reserved.	
	ASIF_CONFIG0[9]	1	Audio SIF ADC mode control. 0: Test mode. 1: Audio SIF mode (mid clamp).	
	-	0	Reserved.	
61h (2CC2h)	REG2CC2	7:0	Default : 0x00	Access : R/W
	ASIF_CONFIG1[7:4]	7:4	Audio SIF ADC voltage clamp Vref selection. 0000: 1.15 V. 0001: 1.20 V. 0010: 0.85 V. 0011: 0.90 V. 0100: 0.95 V. 0101: 1.00 V. 0110: 1.05 V. 0111: 1.10 V. 1000: 0.30 V. 1001: 0.40 V. 1010: 0.50 V. 1011: 0.60 V. 1100: 0.70 V. 1101: 0.80 V. 111x: Reserved.	
	ASIF_CONFIG1[3:2]	3:2	Audio SIF ADC I-clamp bias current Control (I = 2.5uA). 00: 1* I. 01: 2* I. 10: 3* I. 11: 4* I.	
	ASIF_CONFIG1[1]	1	Audio SIF ADC Vref generator DAC bias current control. 0: Normal. 1: Power-down.	
	ASIF_CONFIG1[0]	0	Audio SIF ADC Vref generator DAC resister stream control. 0: Normal. 1: Power-down.	
61h	REG2CC3	7:0	Default : 0x00	Access : R/W

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
(2CC3h)	-	7:3	Reserved.	
	ASIF_CONFIG1[10:8]	2:0	Audio SIF ADC GMC filter gain control. 000: 1. 001: 2. 010: 4. 011: 8. 100: 16. 101: 4. 110: 6. 111: 12.	
62h (2CC4h)	REG2CC4	7:0	Default : 0x00	Access : R/W
	ASIF_CONFIG2[7]	7	Audio SIF ADC GMC filter auto tuning control. 0: GMC filter auto tuning from AAF_CTL[7:0]. 1: GMC filter auto tuning from audio SIF DSP230.	
	-	6	Reserved.	
	ASIF_CONFIG2[5:4]	5:4	SIF ADC resolution selection. 00: 10 bits. 01: 8 bits. 10: 6 bits. 11: 6 bits.	
	ASIF_CONFIG2[3]	3	Audio SIF ADC GMC Vref buffer control. 0: Normal. 1: Disable GMC Vref buffer.	
	ASIF_CONFIG2[2:0]	2:0	Audio SIF ADC GMC filter common mode Vref setting. 000: 1.15625 V. 001: 1.18750 V. 010: 1.21875 V. 011: 1.25000 V. 100: 1.25000 V. 101: 1.09375 V. 110: 1.06250 V. 111: 1.03125 V.	
62h (2CC5h)	REG2CC5	7:0	Default : 0x00	Access : R/W
	ASIF_CONFIG2[15]	7	Audio SIF ADC GMC filter gain control driver. 0: DSP core control GMC filter gain (coarse gain). 1: MCU overwrite GMC filter gain.	
	ASIF_CONFIG2[14]	6	Audio SIF ADC I-clamp delta-sigma modulation control.	

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
			0: Disable current clamp delta-sigma modulation. 1: Enable current clamp delta-sigma modulation.	
	ASIF_CONFIG2[13]	5	Audio SIF ADC I-clamp delta-sigma modulation clock select. 0: 1/4 SIF2x clock for current clamp reference select. 1: 1/8 SIF2x clock for current clamp reference select.	
	ASIF_CONFIG2[12]	4	Audio SIF ADC fine gain control driver. 0: select DSP control ADC fine gain value. 1: select MUC to overwrite ADC fine gain value.	
	ASIF_CONFIG2[11]	3	Audio SIF ADC gain-shift control. 0: 12/13 to 28/13. 1: 6/13 to 22/13.	
	-	2	Reserved.	
	ASIF_CONFIG2[9]	1	Audio SIF ADC 10 bits voltage dither mode. 0: Disable. 1: Enable. Note: LSB 2-bit dither summation (½, ¼).	
	ASIF_CONFIG2[8]	0	Audio SIF ADC dither source selection. 0: ADC dither toggle for 00, 01, 10, 11. 1: ADC dither toggle 10 or 01.	
63h (2CC6h)	REG2CC6	7:0	Default : 0x00	Access : R/W
	ASIF_CONFIG3[7:0]	7:0	GMC filter fine tune value to define PGA cut-off frequency. Bit 7: Reserved. Bit 6: 19.20260 x 2 f-F (addition). Bit 5: 20.25815 x 2 f-F (addition). Bit 4: 42.59300 x 1 f-F (addition). Bit 3: 22.6600 x 1 f-F (addition). Bit 2: 12.41510 x 1 f-F (addition). Bit 1: 7.24688 x 1 f-F (addition). Bit 0: 4.28975 x 1 f-F (addition).	
63h (2CC7h)	REG2CC7	7:0	Default : 0x00	Access : R/W
	ASIF_CONFIG3[15:8]	7:0	Audio SIF ADC gain control value. 00: 12/13 (Min). 01: 12/13 + (16/13 * 1/256). 02: 12/13 + (16/13 * 2/256). &	

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description		
			FF = 12/13 + (16/13 * 255/256). Note: FF = Max		
64h (2CC8h)	REG2CC8	7:0	Default : 0x00		Access : R/W
	ASIF_CONFIG4[7:0]	7:0	Audio SIF ADC offset control value. 00: 5/13 * 0.5 V (min). 01: (5/13 + (16/13 * 1/256)) * 0.5 V. 02: (5/13 + (16/13 * 2/256)) * 0.5 V. & FF = (5/13 + (16/13 * 255/256)) * 0.5 V. Note: FF = Max.		
64h (2CC9h)	REG2CC9	7:0	Default : 0x00		Access : R/W
	ASIF_CONFIG4[15]	7	Audio SIF ADC GMC filter DC test mode control. 0: Normal. 1: Enable DC test mode.		
	ASIF_CONFIG4[14]	6	Audio SIF ADC GMC filter bias test mode control. 0: Normal. 1: Enable self bias setting for test mode.		
	ASIF_CONFIG4[13]	5	Audio SIF ADC GMC filter 3rd order test mode control. 0: Normal mode (3rd). 1: Enable half-bypass mode (3rdè1st).		
	ASIF_CONFIG4[12]	4	Audio SIF ADC GMC filter output stage source follow test mode control. 0: Normal. 1: Reserved.		
	ASIF_CONFIG4[11]	3	Audio SIF ADC GMC filter comparator test mode control. 0: Normal. 1: Reserved.		
	ASIF_CONFIG4[10]	2	Audio SIF ADC GMC filter Gm-cell internal control. 0: Normal. 1: Reserved.		
	ASIF_CONFIG4[9:8]	1:0	Audio SIF ADC GMC filter Gm I-bias control. 00: 50 uA. 01: 62.5 uA. 10: 37.5 uA. 11: 50 uA.		
65h	REG2CCA	7:0	Default : 0x00		Access : R/W

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
(2CCAh)	ASIF_ICTRL[7:6]	7:6	Audio SIF ADC PGA front-end buffer bias current control. 00: 20 uA (normal). 01: 40 uA. 10: 60 uA. 11: 80 uA.	
	ASIF_ICTRL[5:4]		Audio SIF ADC PGA bias current control. 00: 20 uA (normal). 01: 40 uA. 10: 60 uA. 11: 80 uA.	
	ASIF_ICTRL[3:2]		Audio SIF ADC Stage-1 OP amp and comparator bias current control. 00: 20 uA (normal). 01: 40 uA. 10: 60 uA. 11: 80 uA.	
	ASIF_ICTRL[1:0]		Audio SIF ADC Stage-2 OP amp and comparator bias current control. 00: 20 uA (normal). 01: 40 uA. 10: 60 uA. 11: 80 uA.	
65h (2CCBh)	REG2CCB	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	ASIF_ICTRL[9:8]	1:0	Audio SIF ADC VRP/G/M OP amp bias current control. 00: 20 uA (normal). 01: 40 uA. 10: 60 uA. 11: 80 uA.	
66h (2CCCh)	REG2CCC	7:0	Default : 0x00	Access : R/W
	ASIF_AMUX[7]	7	SIF ADC FIFO enable control source selection. 0: FIFO enable controlled by MCU. 1: FIFO enable controlled by DSP.	
	ASIF_AMUX[6]	6	0: Select 2-stage FIFO. 1: Select 4-stage FIFO.	
	ASIF_AMUX[5]	5	0: Disable FIFO operation. 1: Set to start FIFO operate for synchronization.	

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
	ASIF_AMUX[4]	4	Audio SIF input selection; ADC input selection. 0: SIF[0] is the input of ADC. 1: SIF[1] is the input of ADC.
	ASIF_AMUX[3:2]	3:2	Audio SIF ADC V-clamp selection of IN-M. 00: V-clamp to VP0 (while CR64[6]=1). 01: V-clamp to middle pull resister. 10: V-clamp to weak pull resister. 11: V-clamp to VP1 (while CR64[6]=1).
	ASIF_AMUX[1:0]	1:0	Audio SIF ADC V-clamp selection of IN-P. In each case, I-clamp can be enabled. But I-clamp only can function normally when there is no V-clamp. 00: No V-clamp. 01: V-clamp to middle pull resister. 10: V-clamp to weak pull resister. 11: No V-clamp.
66h (2CCDh)	REG2CCD	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	ASIF_AMUX[11]	3	Analog part. 0: SIF mode 1: VIF mode.
	ASIF_AMUX[10]	2	AU_TOP clock select. 0: SIF clock. 1: VIF clock.
	ASIF_AMUX[9]	1	Digital part. 0: SIF mode. 1: VIF mode.
	ASIF_AMUX[8]	0	SIF I/Q selection by down-converter enable option. 0: I/Q select by down-converter enable only once. 1: I/Q select by DATA_LATEN in SIF FIFO out dynamically.
67h (2CCEh)	REG2CCE	7:0	Default : 0x00 Access : R/W
	ASIF_TST[8:7]	7	00: Normal. 01: Select VRP (ADC Vref top) output to ATEST_1. 10: Select VRG (ADC Vref common) output to ATEST_1. 11: Select VRM (ADC Vref bottom) output to ATEST_1.
	ASIF_TST[6:5]	6:5	Audio SIF ADC internal I-ref source selection.

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			00: From band-gap (normal). 01: Select band-gap I output to ATEST_1. 10: From ATEST_1 PAD. 11: Select band-gap I output to ATEST_1 & from ATEST_1 PAD.
	ASIF_TST[4:3]	4:3	Audio SIF ADC Internal V-ref source selection. 00: From band-gap (normal). 01: Select band-gap V output to ATEST_2. 10: From ATEST_2 PAD. 11: Select band-gap V output to ATEST_2 & from ATEST_2 PAD.
	ASIF_TST[2:0]	2:0	Audio SIF ADC I-bias adjustment. 000: 62.5 uA. 001: 75.0 uA. 010: 87.5 uA. 011: 100 uA. 100: 12.5 uA. 101: 25.0 uA. 110: 37.5 uA. 111: 50.0 uA.
67h (2CCFh)	REG2CCF	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	ASIF_TST[13]	5	I-clamp path to SIF input. 0: Normal (I-clamp to input, write CR54[2] for choice). 1: Disable I-clamp.
	ASIF_TST[12]	4	Audio SIF GMC filter bypass enable. 0: Normal (use GMC). 1: Bypass (no GMC, direct to ADC).
	ASIF_TST[11]	3	Disable input select. 0: Normal (choose one input to GMC or ADC, write CR54[2] for choice). 1: No input go to GMC or ADC.
	ASIF_TST[10:9]	2:1	00: Normal. 01: Select PGA output to ATEST_1 & ATEST_2. 10: Increase ADC clock no-overlap interval. 11: Increase ADC clock no-overlap interval.
	ASIF_TST[8]	0	Please see description of '2CCEh[7]'.

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
68h (2CD0h)	REG2CD0	7:0	Default : 0x00	Access : R/W
	ASIF_ADCREF[11:0]	7:0	Audio SIF ADC Vref range control (central voltage = 1.5V). 000h: 0.25V. 001h: 0.25 + 1/4096. 002h: 0.25 + 2/4096. & FFFh: 0.25 + 4095/4096.	
68h (2CD1h)	REG2CD1	7:0	Default : 0x00	Access : R/W
	ASIF_ADCREF[15:12]	7:4	Reserved.	
	ASIF_ADCREF[11:0]	3:0	Please see description of '2CD0h'.	
69h (2CD2h)	REG2CD2	7:0	Default : 0x31	Access : R/W
	-	7	Reserved.	
	SIFPLL_CTRL[6]	6	SIF PLL reset (only reset input divider, feedback divider, and output clock, dsp4x excluded). 0: Normal. 1: Reset.	
	SIFPLL_CTRL[5]	5	SIF PLL power on reset (only reset charge pump and output clock, dsp2x and dsp4x excluded). 0: Normal. 1: Power on reset.	
	SIFPLL_CTRL[4]	4	SIF PLL power-down. 0: Normal. 1: Power-down.	
	SIFPLL_CTRL[3]	3	SIF PLL post-divider enable for output clock. 0: No divider (default). 1: Divider by 2.	
	SIFPLL_CTRL[2:0]	2:0	SIF PLL charge pump current. 000: 2.8u. 001: 5.7u. 010: 8.6u. 011: 11.4u. 100: 14.3u. 101: 17.1u. 110: 22.9u. 111: 45.7u.	
69h	REG2CD3	7:0	Default : 0x00	Access : R/W

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
(2CD3h)	SIFPLL_CTRL[15]	7	Select ASIF_PLL_LOCK OR ASIF_PLL_FLAG.	
	-	6:3	Reserved.	
	SIFPLL_CTRL[10]	2	0: Normal. 1: Enable SIF ADC work in CLKADC divided by 2.	
	SIFPLL_CTRL[9]	1	0: Normal. 1: Power-down PLL divider 3.	
	SIFPLL_CTRL[8]	0	0: Normal. 1: Power-down PLL divider 2.5.	
6Ah (2CD4h)	REG2CD4	7:0	Default : 0x05	Access : R/W
	ASIFPLL_MN[7:0]	7:0	SIF PLL input reference divider ratio. Divider ratio = SIFPLL_N + 1	
6Ah (2CD5h)	REG2CD5	7:0	Default : 0x08	Access : R/W
	ASIFPLL_MN[15:8]	7:0	SIF PLL feedback clock divider ratio. Divider ratio = SIFPLL_M + 1	
6Bh (2CD6h)	REG2CD6	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	SIFPLL_TEST[4]	4	Output SIF PLL testing clock (1x) to video atop. 1: Output enable. 0: Output disable.	
	SIFPLL_TEST[3]	3	Enable freerun for charge pump. 1: Enable. 0: Disable.	
	SIFPLL_TEST[2:1]	2:1	SIF PLL additional feedback divider ratio. 00: /4. 01: /2. 10: /2. 11: /1.	
	SIFPLL_TEST[0]	0	Select feedback clock to feedback divider. 0: Normal feedback clock. 1: REFCLK.	
6Bh (2CD7h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
6Ch (2CD8h)	REG2CD8	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	SIFPLL_EXT[3]	3	SIF Ch1 and Ch2 use the same enable signal. 0: Use the respective enable signal.	

Audio 0 Register (Bank = 2C)			
Index (Absolute)	Mnemonic	Bit	Description
			1: Both use the Ch1 enable signal.
	SIFPLL_EXT[2]	2	Another input for ASIF AMUX Bit 4.
	SIFPLL_EXT[1]	1	ASIF AMUX Bit 4 selection. 0: Keep Original. 1: Use the above _ASIF_AMUX_4_OPTION_.
	SIFPLL_EXT[0]	0	SIF PLL output enable (only for clkcc,clkadc,clk2x). 0: Disable. 1: Enable.
6Ch (2CD9h)	**REG2CD9**	**7:0**	**Default : 0x00** · **Access : R/W**
	SIFPLL_EXT[15:8]	7:0	Reserved.
6Dh (2CDAh)	**REG2CDA**	**7:0**	**Default : -** · **Access : RO**
	-	7:1	Reserved.
	ASIF_PLL_LOCK_OR_FLAG	0	ASIF_PLL_LOCK OR ASIF_PLL_FLAG is selected.
6Dh ~ 6Fh (2CDBh ~ 2CDFh)	-	7:0	**Default : -** · **Access : -**
	-	7:0	Reserved.
70h (2CE0h)	**REG2CE0**	**7:0**	**Default : 0x00** · **Access : R/W**
	CODEC_CFG0[7:0]	7:6	Audio reference voltage generator OPamp bias control. 00: 20uA. 01: 15uA. 10: 30uA. 11: 25uA.
	CODEC_CFG0[5:4]	5:4	Reserved current control (for future). 00: 20uA. 01: 15uA. 10: 30uA. 11: 25uA.
	CODEC_CFG0[3:2]	3:2	Audio ADC output duty cycle test. 00: Select GND. 01: Select GND. 10: Select left channel ADC output. 11: Select right channel ADC output.
	-	1	Reserved.
	CODEC_CFG0[0]	0	Reset FF #16 in DAC. 0: Normal function. 1: Reset.

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
70h (2CE1h)	REG2CE1	7:0	Default : 0x00	Access : R/W
	CODEC_CFG0[15:14]	7:6	AA OPamp bias current. 00: 20uA. 01: 15uA. 10: 30uA. 11: 25uA.	
	CODEC_CFG0[13:12]	5:4	ADC input mixer (anti-aliasing filter) OPamp bias current. 00: 20uA. 01: 15uA. 10: 30uA. 11: 25uA.	
	CODEC_CFG0[11:10]	3:2	ADC integrator OPamp bias current. 00: 20uA. 01: 15uA. 10: 30uA. 11: 25uA.	
	CODEC_CFG0[9:8]	1:0	Audio DAC OPamp bias current. 00: 20uA. 01: 15uA. 10: 30uA. 11: 25uA.	
71h (2CE2h)	REG2CE2	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	CODEC_CFG1[5]	5	Power-on reference current generator. 0: Power-down. 1: Power on (.OR. Gated with DSP).	
	CODEC_CFG1[4]	4	Power-on reference voltage generator. 0: Power-down. 1: Power on (.OR. Gated with DSP).	
	CODEC_CFG1[3]	3	Power-on all bias current sources. 0: Power-down. 1: Power on (.OR. Gated with DSP).	
	-	2:1	Reserved.	
	CODEC_CFG1[0]	0	AUSDM Vref soft-discharge enable. 0: Disable soft-discharge. 1: Enable soft-discharge.	
71h	REG2CE3	7:0	Default : 0x00	Access : R/W

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
(2CE3h)	CODEC_CFG1[15]	7	Audio ADC left channel dithering. 0: Disable. 1: Enable.	
	CODEC_CFG1[14]	6	Audio ADC integrator of left channel reset. 0: Normal. 1: Reset active.	
	CODEC_CFG1[13]	5	Audio ADC left dithering amount reduce. 0: Normal. 1: Reduce (50%).	
	CODEC_CFG1[12]	4	Audio ADC right channel dithering. 0: Disable. 1: Enable.	
	CODEC_CFG1[11]	3	Audio ADC integrator of right channel reset. 0: Normal. 1: Reset active.	
	CODEC_CFG1[10]	2	Audio ADC right dithering amount reduce. 0: Normal. 1: Reduce (50%).	
	-	1:0	Reserved.	
72h (2CE4h)	REG2CE4	7:0	Default : 0x00	Access : R/W
	CODEC_CFG2[7:6]	7:6	Audio SDMADC left channel internal feedback coefficient. 00: 0.300 pF. 01: 0.225 pF. 10: 0.270 pF. 11: 0.345 pF.	
	CODEC_CFG2[5:4]	5:4	Audio SDMADC right channel internal feedback coefficient. 00: 0.300 pF. 01: 0.225 pF. 10: 0.270 pF. 11: 0.345 pF.	
	-	3:0	Reserved.	
72h (2CE5h)	REG2CE5	7:0	Default : 0x00	Access : R/W
	CODEC_CFG2[15]	7	Power-down right channel ADC. 0: Normal. 1: Power-down.	

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
	CODEC_CFG2[14]	6	Power-down left channel ADC. 0: Normal. 1: Power-down.	
	CODEC_CFG2[13]	5	Power-down audio ADC input clock. 0: Normal. 1: Power-down.	
	CODEC_CFG2[12]	4	Select audio ADC input clock source. 0: From clock generator. 1: From external PAD (Video VSYNC_0).	
	CODEC_CFG2[11:9]	3:1	SDMADC clock delay (unit = inverter buffer 70ps). 000: Delay 0 time unit. 001: Delay 4 time unit. 010: Delay 8 time unit. 011: Delay 12 time unit. 100: Delay 16 time unit. 101: Delay 20 time unit. 110: Delay 24 time unit. 111: Delay 28 time unit.	
	-	0	Reserved.	
73h (2CE6h)	REG2CE6	7:0	Default : 0x00	Access : R/W
	CODEC_CFG3[7]	7	Power-down audio ADC input mixer (anti-alias filter) OPamp. 0: Normal. 1: Power-down.	
	CODEC_CFG3[6:3]	6:3	Audio ADC input mixer source select. 0000: LINE_IN[0]. 0001: LINE_IN[1]. 0010: LINE_IN[2]. 0011: LINE_IN[3]. 0100: MONOIN. 0101: GND. 0110: DAC1 left & right. 0111: DAC0 left & right. 1000: DAC2 left & right. 1001: DAC3 left & right. 1010: AA0 left & right. 1011: AA1 left & right. 1100: GND. Others: N.A.	

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
	CODEC_CFG3[2:0]	2:0	Audio ADC input mixer (anti alias filter) gain control. 000: 0 dB. 001: -3 dB. 010: -6 dB. 011: +3 dB. 100: +6 dB. 101: +9 dB. 110: +12 DB.
73h (2CE7h)	**REG2CE7**	7:0	**Default : 0x28** **Access : R/W**
	CODEC_CFG3[15]	7	DE_POP AA0 amplifier control (feedback R = 0). 0: Normal. 1: Mute.
	CODEC_CFG3[14:11]	6:3	Audio AA0 input source select. 0000: LINE_IN[0]. 0001: LINE_IN [1]. 0010: LINE_IN [2]. 0011: LINE_IN [3]. 0100: MONOIN. 0101: GND. 0110: DAC1 left & right. 0111: DAC0 left & right. 1000: DAC2 left & right. 1001: DAC3 left & right. 101x: GND. 1100: GND. Others: N.A.
	CODEC_CFG3[10:9]	2:1	Audio AA0 gain control. 00: 0 dB. 01: -3 dB. 10: -6 dB. 11: +3 dB.
	CODEC_CFG3[8]	0	Audio ADC input mixer (anti alias filter) OPamp control. 0: Normal anti alias filter OPamp. 1: Mute anti alias filter OPamp (feedback R = 0).
74h (2CE8h)	**REG2CE8**	7:0	**Default : 0x00** **Access : R/W**
	CODEC_CFG4[7]	7	Audio AA0R channel amplifier driving strength. 0: Normal. 1: Reduce to 1%.

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
	CODEC_CFG4[6]	6	Audio AA0L channel amplifier driving strength. 0: Normal. 1: Reduce to 1%.	
	CODEC_CFG4[5]	5	Audio AA0R channel amplifier low power mode. 0: Normal. 1: Low power mode (50% bias current).	
	CODEC_CFG4[4]	4	Audio AA0L channel amplifier low power mode. 0: Normal. 61: Low power mode (50% bias current).	
	-	3	Reserved.	
	CODEC_CFG4[2]	2	Disable DAC2 re-latch clock. 0: Normal. 1: Clock disabled.	
	CODEC_CFG4[1]	1	Disable DAC0 re-latch clock. 0: Normal. 1: Clock disabled.	
	CODEC_CFG4[0]	0	Disable DAC1 re-latch clock. 0: Normal. 1: Clock disabled.	
74h (2CE9h)	**REG2CE9**	**7:0**	**Default : 0x28**	**Access : R/W**
	CODEC_CFG4[15]	7	DE_POP AA1 amplifier control (feedback R = 0). 0: Normal. 1: Mute.	
	CODEC_CFG4[14:11]	6:3	Audio AA1 input source select. 0000: LINE_IN[0]. 0001: LINE_IN[1]. 0010: LINE_IN[2]. 0011: LINE_IN[3]. 0100: MONOIN. 0101: GND. 0110: DAC1 left & right. 0111: DAC0 left & right. 1000: DAC2 left & right. 1001: DAC3 left & right. 101x: GND. 1100: GND. Others: N.A.	
	CODEC_CFG4[10:9]	2:1	Audio AA1 gain control.	

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
			00: 0 dB. 01: -3 dB. 10: -6 dB. 11: +3 dB.	
	-	0	Reserved.	
75h (2CEAh)	**REG2CEA**	**7:0**	**Default : 0x00**	**Access : R/W**
	CODEC_CFG5[7]	7	Audio AA1R channel amplifier driving strength. 0: Normal. 1: Reduce to 1%.	
	CODEC_CFG5[6]	6	Audio AA1R channel amplifier driving strength. 0: Normal. 1: Reduce to 1%.	
	CODEC_CFG5[5]	5	Audio AA1R channel amplifier low power mode. 0: Normal. 1: Low power mode (50% bias current).	
	CODEC_CFG5[4]	4	Audio AA1R channel amplifier low power mode. 0: Normal. 1: Low power mode (50% bias current).	
	CODEC_CFG5[3]	3	Mute audio AA1 (input floating). 0: Normal. 1: Mute.	
	CODEC_CFG5[2]	2	Mute audio AA0 (input floating). 0: Normal. 1: Mute.	
	CODEC_CFG5[1]	1	Power-on audio AA1. 0: Power-down. 1: Power-on (or gated with DSP).	
	CODEC_CFG5[0]	0	Power-on audio AA0. 0: Power-down. 1: Power-on (or gated with DSP).	
75h (2CEBh)	**REG2CEB**	**7:0**	**Default : 0x00**	**Access : R/W**
	CODEC_CFG5[15]	7	Audio DAC1R low power mode. 0: Normal. 1: Low power mode (50%).	
	CODEC_CFG5[14]	6	Audio DAC1R amplifier driving strength. 0: Normal. 1: Reduce to 1%.	

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
	CODEC_CFG5[13]	5	Audio DAC1L low power mode. 0: Normal. 1: Low power mode (50%).	
	CODEC_CFG5[12]	4	Audio DAC1L amplifier driving strength. 0: Normal. 1: Reduce to 1%.	
	CODEC_CFG5[11]	3	Reset DAC3 re-latch flip-flip. 0: Normal. 1: Reset (or gated with DSP).	
	CODEC_CFG5[10]	2	Reset DAC2 re-latch flip-flip. 0: Normal. 1: Reset (or gated with DSP).	
	CODEC_CFG5[9]	1	Reset DAC0 re-latch flip-flip. 0: Normal. 1: Reset or gated with DSP).	
	CODEC_CFG5[8]	0	Reset DAC1 Re-latch Flip-flip. 0: Normal. 1: Reset (or gated with DSP).	
76h (2CECh)	REG2CEC	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	CODEC_CFG6[5]	5	Power-on audio DAC1R driving OPamp. 0: Power-down. 1: Power-on (or gated with DSP).	
	CODEC_CFG6[4]	4	Power-on audio DAC1R Vref OPamp. 0: Power-down. 1: Power-on (or gated with DSP).	
	CODEC_CFG6[3]	3	Audio DAC data latching mode select. 0: Negative edge select. 1: Positive edge select.	
	CODEC_CFG6[2]	2	Power audio DAC reference current generator. 0: Power-down. 1: Power-on (or gated with DSP).	
	CODEC_CFG6[1]	1	Audio DAC reference current test mode. 0: Normal. 1: Bypass test current to PAD (SOG_[1:0] = Test [1:0]).	
	-	0	Reserved.	

Audio 0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
76h (2CEDh)	REG2CED	7:0	Default : 0x00	Access : R/W
	CODEC_CFG6[15]	7	Audio DAC0R low power mode. 0: Normal. 1: Low power mode (50%).	
	CODEC_CFG6[14]	6	Audio DAC0R amplifier driving strength. 0: Normal. 1: Reduce to 1%.	
	CODEC_CFG6[13]	5	Power-on audio DAC1L Driving OPamp. 0: Power-down. 1: Power-on (or gated with DSP).	
	CODEC_CFG6[12]	4	Power-on audio DAC1L Vref OPamp. 0: Power-down. 1: Power-on (or gated with DSP).	
	CODEC_CFG6[11]	3	Audio DAC0L low power mode. 0: Normal. 1: Low power mode (50%).	
	CODEC_CFG6[10]	2	Audio DAC0L amplifier driving strength. 0: Normal. 1: Reduce to 1%.	
	CODEC_CFG6[9]	1	Power-on audio DAC0 driving OPamp. 0: Power-down. 1: Power-on (or gated with DSP).	
	CODEC_CFG6[8]	0	Power-on audio DAC0 Vref OPamp. 0: Power-down. 1: Power-on (or gated with DSP).	
77h (2CEEh)	REG2CEE	7:0	Default : 0x00	Access : R/W
	CODEC_CFG7[7]	7:0	Audio DAC2R low power mode. 0: Normal. 1: low power mode (50%).	
	CODEC_CFG7[6]	6	Audio DAC2R amplifier driving strength. 0: Normal. 1: Reduce to 1%.	
	CODEC_CFG7[5]	5	Power-down audio DAC2 driving OPamp. 0: Power-down. 1: Power-on (or gated with DSP).	
	CODEC_CFG7[4]	4	Power-down audio DAC2 Vref OPamp. 0: Power-down.	

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
			1: Power-on (or gated with DSP).	
	CODEC_CFG7[3]	3	Audio DAC2L low power mode. 0: Normal. 1: Low power mode (50%).	
	CODEC_CFG7[2]	2	Audio DAC2L amplifier driving strength. 0: Normal. 1: Reduce to 1%.	
	-	1:0	Reserved.	
77h (2CEFh)	**REG2CEF**	7:0	**Default : 0x00**	**Access : R/W**
	CODEC_CFG7[15]	7	Audio DAC3R low power mode. 0: Normal. 1: Low power mode (50%).	
	CODEC_CFG7[14]	6	Audio DAC3R amplifier driving strength. 0: Normal. 1: Reduce to 1%.	
	CODEC_CFG7[13]	5	Power down audio DAC3 driving OPamp. 0: Power down. 1: Power on (or gated with DSP).	
	CODEC_CFG7[12]	4	Power down audio DAC3 Vref OPamp. 0: Power down. 1: Power on (or gated with DSP).	
	CODEC_CFG7[11]	3	Audio DAC3L low power mode. 0: Normal. 1: Low power mode (50%).	
	CODEC_CFG7[10]	2	Audio DAC3L amplifier driving strength. 0: Normal. 1: Reduce to 1%.	
	CODEC_CFG7[9]	1	DAC discharge control. 0: Disable. 1: Enable (or gated with DSP).	
	CODEC_CFG7[8]	0	VREF discharge control. 0: Disable. 1: Enable (or gated with DSP).	
78h ~ 7Dh (2CF0h ~ 2CFBh)	-	7:0	**Default : -**	**Access : -**
	-	7:0	Reserved.	
7Eh	**REG2CFC**	7:0	**Default : -**	**Access : RO**

Audio 0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
(2CFCh)	TEST_BUS_OUT_L[7:0]	7:0	Test bus output LSB.	
7Eh (2CFDh)	REG2CFD	7:0	Default : -	Access : RO
	TEST_BUS_OUT_L[15:8]	7:0	Please see description of '2CFCh'.	
7Fh (2CFEh)	REG2CFE	7:0	Default : -	Access : RO
	TEST_BUS_OUT_H[7:0]	7:0	Test bus output MSB.	
7Fh (2CFFh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	

Audio 1 Register (Bank = 2D)

Audio 1 Register (Bank = 2D)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (2D00h)	REG2D00	7:0	Default : 0x03	Access : RO, R/W
	-	7:6	Reserved.	
	INT_TRIGGER	5	MIPS Trigger DSP PIO[8] interrupt. 0: De-assert DSP PIO[8] interrupt. 1: Assert DSP PIO[8] interrupt.	
	IDMA_WR_CMD_STA	4	IDMA write command status. 0: IDMA write command finish. 1: IDMA write on going (busy).	
	IDMA_RD_CMD_STA	3	IDMA read command/status Command: 0: Reserved. 1: Set IDMA read command and auto-clear when finished. Status: 0: Read command finished (status). 1: Read command busy (status).	
	IDMA_WR2ND	2	IDMA needs to write 2nd data. 0: IDMA write data finished. 1: IDMA needs to write 2nd data. Note : Write 0 to clear.	
	IDMA_BOOT_MODE	1	DSP IDMA BOOT mode enable. 0: Disable. 1: Enable.	
	DSP_SOFT_RST	0	DSP audio software reset. 0: Reset. 1: Normal.	
01h (2D02h)	REG2D02	7:0	Default : 0x00	Access : WO
	DSP_BRG_DATA[7:0]	7:0	Host download DSP data port. 24-bit mode: 1. Write high 2 bytes DATA[23:8]. 2. Write low byte 8_b0, DATA[7:0]. 3. Loop to step 1.	
01h (2D03h)	REG2D03	7:0	Default : 0x00	Access : WO
	DSP_BRG_DATA[15:8]	7:0	Please see description of '2D02h'.	
02h (2D04h)	REG2D04	7:0	Default : 0x00	Access : R/W
	IDMA_WRBASE_ADDR[7:0]	7:0	Channel 1 IDMA address base IAD.	

Audio 1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description	
02h (2D05h)	REG2D05	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	CH1_MEM_SEL	6	Channel 1 IDMA address base PM/CM/DM control. 0: Select PM / CM. 1: Select DM.	
	IDMA_WRBASE_ADDR[13:8]	5:0	Please see description of '2D04h'.	
03h (2D06h)	REG2D06	7:0	Default : 0x00	Access : R/W
	CH1IDMA_ATR_SIZE[7:0]	7:0	IDMA CH1 ATR size.	
03h (2D07h)	REG2D07	7:0	Default : 0x00	Access : RO, R/W
	-	7	Reserved.	
	CH1IDMA_CIRCULAR_BUF	6	Disable IDMA CH2 circular buffer. 0: Enable circular buffer. 1: Disable circular buffer.	
	CH1IDMA_ATR_SIZE[13:8]	5:0	Please see description of '2D06h'.	
04h (2D08h)	REG2D08	7:0	Default : 0x00	Access : R/W
	IDMA_RDBASE_ADDR[7:0]	7:0	Channel 2 IDMA address base IAD.	
04h (2D09h)	REG2D09	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	CH2_MEM_SEL	6	Channel 2 IDMA address base PM/CM/DM control. 0: Select PM / CM. 1: Select DM.	
	IDMA_RDBASE_ADDR[13:8]	5:0	Please see description of '2D08h'.	
05h (2D0Ah)	REG2D0A	7:0	Default : 0x00	Access : R/W
	CH2IDMA_ATR_SIZEH[7:0]	7:0	IDMA CH2 ATR size.	
05h (2D0Bh)	REG2D0B	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	CH2IDMA_ATR_SIZEH_DIS	6	Disable IDMA CH2 circular buffer. 0: Enable. 1: Disable.	
	CH2IDMA_ATR_SIZEH[13:8]	5:0	Please see description of '2D0Ah'.	
06h (2D0Ch)	REG2D0C	7:0	Default : -	Access : RO
	IDMA_RDDATA_H[7:0]	7:0	IDMA CH2 MIPS read DSP DATA_PORT[23:8] for transferring data from DSP to MIPS.	
06h	REG2D0D	7:0	Default : -	Access : RO

Audio 1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description	
(2D0Dh)	IDMA_RDDATA_H[15:8]	7:0	Please see description of '2D0Ch'.	
07h (2D0Eh)	**REG2D0E**	**7:0**	**Default : -**	**Access : RO**
	IDMA_RDDATA_L[7:0]	7:0	IDMA CH2 4 MIPS read DSP DATA_PORT[7:0] for transferring data from DSP to MIPS.	
08h (2D10h)	**REG2D10**	**7:0**	**Default : 0x00**	**Access : R/W**
	DSP_ICACHE_BASE[7:0]	7:0	FD230 I-Cache MIU base address[23:16].	
08h (2D11h)	**REG2D11**	**7:0**	**Default : 0x00**	**Access : R/W**
	DSP_ICACHE_BASE[15:8]	7:0	Please see description of '2D10h'.	
09h (2D12h)	**REG2D12**	**7:0**	**Default : 0x00**	**Access : R/W**
	MCU2DSP_MAILBOX_CFG[3:0]	7:4	MCU to DSP mailbox config. 0000: M2D_MAILBOX_0. 0001: M2D_MAILBOX_1. 0010: M2D_MAILBOX_2. 0011: M2D_MAILBOX_3. 0100: M2D_MAILBOX_4. 0101: M2D_MAILBOX_5. 0110: M2D_MAILBOX_6. 0111: M2D_MAILBOX_7.	
	DSP2MCU_MAILBOX_CFG[3:0]	3:0	DSP to MCU mailbox configuration. 0000: D2M_MAILBOX_0. 0001: D2M_MAILBOX_1. 0010: D2M_MAILBOX_2. 0011: D2M_MAILBOX_3. 0100: D2M_MAILBOX_4. 0101: D2M_MAILBOX_5. 0110: D2M_MAILBOX_6. 0111: D2M_MAILBOX_7.	
0Ah (2D14h)	**REG2D14**	**7:0**	**Default : 0x00**	**Access : R/W**
	MCU2DSP_MAILBOX[7:0]	7:0	MCU to DSP MAILBOX; indirect MAILBOX write to DSP port.	
0Ah (2D15h)	**REG2D15**	**7:0**	**Default : 0x00**	**Access : R/W**
	MCU2DSP_MAILBOX[15:8]	7:0	Please see description of '2D14h'.	
0Bh (2D16h)	**REG2D16**	**7:0**	**Default : -**	**Access : RO**
	DSP2MCU_MAILBOX[7:0]	7:0	DSP to MCU MAILBOX; indirect MAILBOX read from DSP port.	
0Bh	**REG2D17**	**7:0**	**Default : -**	**Access : RO**

Audio 1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description	
(2D17h)	DSP2MCU_MAILBOX[15:8]	7:0	Please see description of '2D16h'.	
10h (2D20h)	REG2D20	7:0	Default : 0x00	Access : R/W
	STD_SEL_SET	7	Audio SIF standard set command. 0: Manual. 1: Auto.	
	STD_SEL[6:0]	6:0	SIF audio standard selection. 00h: Standard not found. 01h: AU_SYS_M_BTSC. 02h: AU_SYS_M_ EIAJ. 03h: AU_SYS_M_A2. 04h: AU_SYS_BG_A2. 05h: AU_SYS_DK1_A2. 06h: AU_SYS_DK2_A2. 07h: AU_SYS_DK3_A2. 0Ch: AU_SYS_FM_RADIO.	
11h (2D22h)	REG2D22	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	STD_PRE45[1:0]	2:1	Preference in automatic standard selection of 4.5MHz carrier. 00: Standard M (Korea). 01: Standard M (BTSC). 10: Standard M (Japan). 11: Not a sound carrier.	
	STD_PRE65	0	Preference in automatic standard selection of 6.5MHz carrier. 0: Standard L (SECAM). 1: Standard D/K.	
12h (2D24h)	REG2D24	7:0	Default : 0x00	Access : R/W
	SIF_SOUND_MOD1[7:0]	7:0	SIF BTSC/A2 demodulator automatic/manual sound mode output select. 0xxxxxxx: Manual sound select. 0000: 0000: BTSC Mono. 00000001: BTSC Stereo. 00000010: BTSC SAP. 00000100: A2 Mono. 00000101: A2 Stereo. 00000110: A2 Dual B. 00000111: A2 Dual A+B.	

Audio 1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description	
			1xxxxxxx: Auto sound select. 10000000: BTSC Mono <-> Mute. 10000001: BTSC Stereo <-> Mono <-> Mute. 10000010: BTSC SAP<-> Mono <-> Mute. 10000100: A2 Mono <-> Mute. 10000101: A2 Stereo <->Mono <-> Mute. 10000110: A2 Dual B <->Mono <-> Mute. 10000111: A2 Dual B <->Stereo->Mono <-> Mute.	
13h (2D26h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
15h (2D2Ah)	REG2D2A	7:0	Default : 0x00	Access : R/W
	DBG_CMD[7:0]	7:0	SIF common command: 0x00: No action. 0x01: Common command get_firmware version. 0x02: Common command set memory data. 0x03: Common command set DM memory address. 0x04: Common command set PM memory address. 0x03: Common command read DM memory address. BTSC command: 0x10: BTSC_CMD_UPDATE_PILOT_ON_THR Pilot off to on threshold update command. 0x11: BTSC_CMD_UPDATE_PILOT_OFF_THR Pilot on to off threshold update command. 0x12: BTSC_CMD_UPDATE_CARRIER_ON_THR Carrier off to on threshold update command. 0x13: BTSC_CMD_UPDATE_CARRIER_OFF_THR Carrier on to off threshold update command. 0x14: BTSC_CMD_UPDATE_SAP_ON_THR SAP off to on threshold update command. 0x15: BTSC_CMD_UPDATE_SAP_OFF_THR SAP on to off threshold update command. A2 Command: 0x20: A2_CMD_UPDATE_CARRIER_ON_THR Carrier off to on threshold update command. 0x21: A2_CMD_UPDATE_CARRIER_OFF_THR Carrier on to off threshold update command.	

Audio 1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description	

			0x22: A2_CMD_UPDATE_MONO_ON_THR
			      Mono off to on threshold update command.
			0x23: A2_CMD_UPDATE_MONO_OFF_THR
			      Mono on to off threshold update command.
			0x24: A2_CMD_UPDATE_STEREO_DUAL_THR
			      Stereo/Dual threshold update command.
			0x30: A2_CMD_GET_CARRIER_1_AMP
			      Carrier 1 amplitude output command.
			0x31: A2_CMD_GET_CARRIER_1_VAR.
			0x32: A2_CMD_GET_CARRIER_2_AMP
			      Carrier 2 amplitude output command.
			0x33: A2_CMD_GET_CARRIER_2_VAR.
			0x34: A2_CMD_GET_MONO_AMP
			      mono amplitude output command.
			0x35: A2_CMD_GET_STEREO_AMP
			      stereo amplitude output command.
			0x36: A2_CMD_GET_DUAL_AMP
			      dual amplitude output command.	

15h (2D2Bh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
16h (2D2Ch)	REG2D2C	7:0	Default : 0x00	Access : R/W
	DBG_DATA_H[7:0]	7:0	Data-hi, from 8051 to DSP, need to match command (0x85).	
16h (2D2Dh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
17h (2D2Eh)	REG2D2E	7:0	Default : 0x00	Access : R/W
	DBG_DATA_L[7:0]	7:0	Data-lo, from 8051 to DSP, need to match command (0x85).	
17h (2D2Fh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
18h (2D30h)	REG2D30	7:0	Default : 0x00	Access : R/W
	DEBUG_REG_0[7:0]	7:0	8 bytes for software utilization.	
19h (2D31h)	REG2D32	7:0	Default : 0x00	Access : R/W
	DEBUG_REG_1[7:0]	7:0	8 bytes for software utilization.	
19h (2D32h ~ 2D33h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	

Audio 1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description	
1Ah (2D34h)	REG2D34	7:0	Default : 0x00	Access : R/W
	DEBUG_REG_2[7:0]	7:0	8 bytes for software utilization.	
1Ah (2D35h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
1Bh (2D36h)	REG2D36	7:0	Default : 0x00	Access : R/W
	DEBUG_REG_3[7:0]	7:0	8 bytes for software utilization.	
1Bh (2D37h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
1Ch (2D38h)	REG2D38	7:0	Default : 0x00	Access : R/W
	DEBUG_REG_4[7:0]	7:0	8 bytes for software utilization.	
1Ch (2D39h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
1Dh (2D3Ah)	REG2D3A	7:0	Default : 0x00	Access : R/W
	DEBUG_REG_5[7:0]	7:0	8 bytes for software utilization.	
1Dh (2D3Bh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
1Eh (2D3Ch)	REG2D3C	7:0	Default : 0x00	Access : R/W
	DEBUG_REG_6[7:0]	7:0	8 bytes for software utilization.	
1Eh (2D3Dh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
1Fh (2D3Eh)	REG2D3E	7:0	Default : 0x00	Access : R/W
	DEBUG_REG_7[7:0]	7:0	8 bytes for software utilization.	
1Fh (2D3Fh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
20h (2D40h)	REG2D40	7:0	Default : -	Access : RO
	STD_RESULT_FINISH	7	Audio SIF standard detection Flag. 0: Standard detection finished. 1: Standard detection not finished.	
	STD_RESULT[6:0]	6:0	SIF standard detect result. 00h: Standard not found. 01h: AU_SYS_M_BTSC. 02h: AU_SYS_M_KOREA. 03h: AU_SYS_M_JAPAN. 04h: AU_SYS_BG_A2.	

Audio 1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description	
			05h: AU_SYS_DK1_A2. 06h: AU_SYS_DK2_A2. 07h: AU_SYS_DK3_A2. 0Ch: AU_SYS_FM_RADIO.	
20h ~ 21h (2D41h ~ 2D43h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
22h (2D44h)	REG2D44	7:0	Default : -	Access : RO
	STATUS_MOD[7:0]	7:0	Sound mod status. Bit 0: BTSC mono exists. Bit 1: BTSC stereo exists. Bit 2: BTSC sap exists. Bit 3: A2 carrier 1 exists. Bit 4: A2 carrier 2 exists. Bit 5: A2 stereo exists. Bit 6: A2 dual exists. Bit 7: A2 mono exists.	
22h ~ 24h (2D45h ~ 2D49h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
25h (2D4Ah)	REG2D4A	7:0	Default : -	Access : RO
	DBG_OUTPUT_L[7:0]	7:0	Debugging data port; direct output date from DSP230 I/O write command.	
25h (2D4Bh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
26h (2D4Ch)	REG2D4C	7:0	Default : -	Access : RO
	DBG_OUTPUT_H[7:0]	7:0	Debugging data port; direct output date from DSP230 I/O write command.	
26h (2D4Dh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
27h (2D4Eh)	REG2D4E	7:0	Default : -	Access : RO
	INC_COUNTER[7:0]	7:0	DSP sample counter SIF PCM output sample counter.	
27h (2D4Fh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
28h	REG2D50	7:0	Default : -	Access : RO

Audio 1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description	
(2D50h)	MAIL_BOX_0[7:0]	7:0	DSP to MCU MailBox data.	
28h (2D51h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
29h (2D52h)	REG2D52	7:0	Default : -	Access : RO
	MAIL_BOX_1[7:0]	7:0	DSP to MCU MailBox data.	
29h (2D53h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
2Ah (2D54h)	REG2D54	7:0	Default : -	Access : RO
	MAIL_BOX_2[7:0]	7:0	DSP to MCU MailBox data.	
2Dh (2D55h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
2Bh (2D56h)	REG2D56	7:0	Default : -	Access : RO
	MAIL_BOX_3[7:0]	7:0	DSP to MCU MailBox data.	
27h (2D57h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
2Ch (2D58h)	REG2D58	7:0	Default : -	Access : RO
	MAIL_BOX_4[7:0]	7:0	DSP to MCU MailBox data.	
2Ch (2D59h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
2Dh (2D5Ah)	REG2D5A	7:0	Default : -	Access : RO
	MAIL_BOX_5[7:0]	7:0	DSP to MCU MailBox data.	
2Dh (2D5Bh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
2Eh (2D5Ch)	REG2D5C	7:0	Default : -	Access : RO
	MAIL_BOX_6[7:0]	7:0	DSP to MCU MailBox data.	
2Eh (2D5Dh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
2Fh (2D5Eh)	REG2D5E	7:0	Default : -	Access : RO
	MAIL_BOX_7[7:0]	7:0	DSP to MCU MailBox data.	
2Fh (2D5Fh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
30h (2D60h)	REG2D60	7:0	Default : 0x00	Access : RO, R/W
	DWA_RST	7	Reset DWA.	

Audio 1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description	
			0: Normal. 1: DWA output all ZERO to analog.	
	INIT_DATA_SRAM	6	Initialize DATA SRAM (8051 software control). 0: Normal. 1: Initial time (>512 * MAC_CLK).	
	MAC_OVL	5	MAC is over loaded. 0: Normal. 1: Over loading.	
	MOD_ENABLE	4	Modulator input test mode setting. 1: Normal. 0: Input 16h8000 to modulator.	
	DAC_TEST	3	DAC test mode. 0: Normal. 1: Test mode for mass production.	
	-	2:1	Reserved.	
	DSD_IRQ_MASK	0	DSD IRQ mask (only for ZR MAC).	
30h (2D61h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
31h (2D62h)	**REG2D62**	7:0	**Default : 0x00**	**Access : R/W**
	DAC_CH4_MAC_IRQ_MASK	7	CH4 IRQ mask (only for ZR MAC). 0: IRQ valid. 1: Mask.	
	DAC_CH3_MAC_IRQ_MASK	6	CH3 IRQ mask (only for ZR MAC). 0: IRQ valid. 1: Mask.	
	DAC_CH2_MAC_IRQ_MASK	5	CH2 IRQ mask (only for ZR MAC). 0: IRQ valid. 1: Mask.	
	DAC_CH1_MAC_IRQ_MASK	4	CH1 IRQ mask (only for ZR MAC). 0: IRQ valid. 1: Mask.	
	DAC_CH4_FD230_BYPASS	3	CH4 FD230 bypass mode (hardware). 0: Normal. 1: Mask FD230 IRQ & hardware bypass.	
	DAC_CH3_FD230_BYPASS	2	CH3 FD230 bypass mode (hardware). 0: Normal. 1: Mask FD230 IRQ & hardware bypass.	

Audio 1 Register (Bank = 2D)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	DAC_CH2_FD230_BYPASS	1	CH2 FD230 bypass mode (hardware). 0: Normal. 1: Mask FD230 IRQ & hardware bypass.
	DAC_CH1_FD230_BYPASS	0	CH1 FD230 bypass mode (hardware). 0: Normal. 1: Mask FD230 IRQ & hardware bypass.
31h (2D63h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.
32h (2D64h)	**REG2D64**	7:0	**Default : 0x00**	**Access : R/W**
	ADC1_MAC_IRQ_MASK	7	ADC1 IRQ mask (only for ZR MAC). 0: IRQ valid. 1: Mask.
	ADC1_FD230_BYPASS	6	ADC1 FD230 bypass mode. 0: Normal. 1: Mask FD230 IRQ & hardware bypass.
	ADC2_MAC_IRQ_MASK	5	ADC2 IRQ mask (only for ZR MAC). 0: IRQ valid. 1: Mask.
	ADC2_FD230_BYPASS	4	ADC2 FD230 bypass mode. 0: Normal. 1: Mask FD230 IRQ & hardware bypass.
	-	3	Reserved.
	SRC_OSZOH_TEST	2	SRC interpolation function control. 0: Normal (linear interpolation). 1: sample and hold (disable interpolation).
	SRC_FS_TEST	1	SRC interpolation ratio selection. 0: Normal SRC Interpolation Mode (8fs to 256fs). 1: SRC interpolation test mode (fs to 256fs).
	ZRMAC_CLKON_ALWAYS	0	0: ZR MAC CLK auto power-down mode. 1: Disable ZR MAC CLK auto power-down mode.
32h (2D65h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.
33h (2D66h)	**REG2D66**	7:0	**Default : 0x00**	**Access : R/W**
	DWA_TEST	7	DWA function turn-off test. 0: DWA turned on. 1: DWA turned off.

Audio 1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description	
	-	6:5	Reserved.	
	FORCE_2ND_ORDER	4	Modulator order. 0: 1st order. 1: 2nd order.	
33h (2D67h)	-	7:0	**Default : -**	**Access : -**
	-	7:0	Reserved.	
34h (2D68h)	**REG2D68**	7:0	**Default : 0x00**	**Access : RO, R/W**
	CLEAR_FIFO_STATUS	7	Clear FIFO status bits. 0: Normal. 1: Clear CH 1/2/3/4 FIFO status.	
	FIFO_STATUS_6	6	ADC right FIFO status. 0: Balance. 1: Overflow or under-run.	
	FIFO_STATUS_5	5	ADC left FIFO status. 0: Balance. 1: Overflow or under-run.	
	FIFO_STATUS_4	4	CH3 left FIFO status. 0: Balance. 1: Overflow or under-run.	
	FIFO_STATUS_3	3	CH2 right FIFO status. 0: Balance. 1: Overflow or under-run.	
	FIFO_STATUS_2	2	CH2 left FIFO status. 0: Balance. 1: Overflow or under-run.	
	FIFO_STATUS_1	1	CH1 right FIFO status. 0: Balance. 1: Overflow or under-run.	
	FIFO_STATUS_0	0	CH1 left FIFO status. 0: Balance. 1: Overflow or under-run.	
34h ~ 35h (2D69h ~ 2D6Bh)	-	7:0	**Default : -**	**Access : -**
	-	7:0	Reserved.	
36h (2D6Ch)	**REG2D6C**	7:0	**Default : 0x00**	**Access : R/W**
	AUTO_RESET_EN	7	DAC FIFO auto reset enable for channel 1, 2, 3 & 4.	

Audio 1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description	
			0: Disable. 1: Enable.	
	MANUAL_RESET_EN	6	DAC FIFO manual reset enable for channel 1, 2, 3 & 4. 0: Disable. 1: Enable.	
	RIU_DACFIFO_RESET[3:0]	5:2	RIU control DAC FIFO manual reset. DAC FIFO channel 1 reset: (RIU_DACFIFO_RESET[0] == 1) or (DSP DM_IO4189[4] ==1). DAC FIFO channel 2 reset: (RIU_DACFIFO_RESET[1] == 1) or (DSP DM_IO4189[5] ==1). DAC FIFO channel 3 reset: (RIU_DACFIFO_RESET[2] == 1) or (DSP DM_IO4189[6] ==1). DAC FIFO channel 4 reset: (RIU_DACFIFO_RESET[3] == 1) or (DSP DM_IO4189[7] ==1).	
	-	1:0	Reserved.	
36h ~ 3Fh (2D6Dh ~ 2D7Fh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
40h (2D80h)	REG2D80	7:0	Default : 0x00	Access : R/W
	CH1_PRESCALE[7:0]	7:0	Pre-scale value for channel 1 gain control. 00h: Off (mute). & 19h: 0 dB (suggested). & 7Fh: +14 dB (-0.13725 dB per step).	
40h (2D81h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
41h (2D82h)	REG2D82	7:0	Default : 0x00	Access : R/W
	STEREO_SOURCE	7	Audio source setting (combine with CRB1.2). 0: Mono. 1: Stereo.	
	SNDEFFECT_ON	6	Sound effect function for channel 1 global control. 0: Disable (software bypass). 1: Enable.	

Audio 1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description	
	-	5	Reserved.	
	AVC	4	Auto volume control function setting. 0: Disable. 1: Enable.	
	TONE	3	TONE (bass/treble) effect control. 0: Disable. 1: Enable.	
	SPATIAL	2	Spatial surround function control. 0: Disable. 1: Enable. Note: 1. Dependent on bit 7 while enabled. 2. Bit 7 = 0, do mono to stereo. 3. Bit 7 = 1, do surrounding effect.	
	VOLUME_BALANCE	1	Volume and balance function control. 0: Disable. 1: Enable.	
	SUBWOOFER	0	Enable subwoofer function. 0: Disable. 1: Enable.	
41h (2D83h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
42h (2D84h)	REG2D84	7:0	Default : 0x00	Access : R/W
	CH1_GRAPHICEQ	7	Enable CH1 graphic EQ. 0: Disable. 1: Enable (higher priority than tone effect).	
	CH1_LOUDNESS	6	Enable CH1 loudness. 0: Disable. 1: Enable.	
	CH1_LOUDNESS_MANUALMODE	5	Enable Loudness Manual mode. 0: Auto mode. 1: Manual mode (see 0xB2[3:2]).	
	-	4	Reserved.	
	CH1_LOUDNES_MODE[1:0]	3:2	Loudness mode (valid while 0xB2.5 = 1). 00: Mode 0 (low slope). 01: Mode 1. 10: Mode 2.	

Audio 1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description	
			11: Mode 3 (high slope).	
	CH1_AVC_MODE[1:0]	1:0	Response time selection for auto volume control function. 00: Mode 0 (-20dB/-6dB). 01: Mode 1 (-20dB/-6dB). 10: Mode 2 (-20dB/-6dB). 11: Mode 3 (-20dB/-6dB).	
42h (2D85h)	-	7:0	**Default : -**	**Access : -**
	-	7:0	Reserved.	
43h (2D86h)	**REG2D86**	7:0	**Default : 0x00**	**Access : R/W**
	CH1_BASS[7:0]	7:0	Bass effect select. 0: 0000: +00db. 0: 0001: +01db. 0: 0010: +02db. 0: 0011: +03db. 0: 0100: +04db. 0: 0101: +05db. 0: 0110: +06db. 0: 0111: +07db. 0: 1000: +08db. 0: 1001: +09db. 0: 1010: +10db. 0: 1011: +11db. 0: 1100: +12db. 0: 1101: +13db. 0: 1110: +14db. 0: 1111: +15db. 1: 0000: -16db. 1: 0001: -15db. 1: 0010: -14db. 1: 0011: -13db. 1: 0100: -12db. 1: 0101: -11db. 1: 0110: -10db. 1: 0111: -09db. 1: 1000: -08db. 1: 1001: -07db. 1: 1010: -06db. 1: 1011: -05db.	

Audio 1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description	
			1: 1100: -04db.	
			1: 1101: -03db.	
			1: 1110: -02db.	
			1: 1111: -01db.	
43h (2D87h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
44h (2D88h)	REG2D88	7:0	Default : 0x00	Access : R/W
	CH1_TREBLE[7:0]	7:0	Treble effect select.	
			0: 0000: +00db.	
			0: 0001: +01db.	
			0: 0010: +02db.	
			0: 0011: +03db.	
			0: 0100: +04db.	
			0: 0101: +05db.	
			0: 0110: +06db.	
			0: 0111: +07db.	
			0: 1000: +08db.	
			0: 1001: +09db.	
			0: 1010: +10db.	
			0: 1011: +11db.	
			0: 1100: +12db.	
			0: 1101: +13db.	
			0: 1110: +14db.	
			0: 1111: +15db.	
			1: 0000: -16db.	
			1: 0001: -15db.	
			1: 0010: -14db.	
			1: 0011: -13db.	
			1: 0100: -12db.	
			1: 0101: -11db.	
			1: 0110: -10db.	
			1: 0111: -09db.	
			1: 1000: -08db.	
			1: 1001: -07db.	
			1: 1010: -06db.	
			1: 1011: -05db.	
			1: 1100: -04db.	
			1: 1101: -03db.	
			1: 1110: -02db.	

Audio 1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description	
			1: 1111: -01db.	
44h (2D89h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
45h (2D8Ah)	REG2D8A	7:0	Default : 0x01	Access : R/W
	-	7:6	Reserved.	
	CH1_MONO2STEREO_MODE[1:0]	5:4	Mode selection for mono to stereo. 00: Virtual 40 degree source. 01: Virtual 20 degree source. 10: Virtual -20 degree source. 11: Virtual -40 degree source.	
	-	3:2	Reserved.	
	CH1_SURROUND_MODE[1:0]	1:0	Mode selection for surround. 00: Mountain mode. 01: Champaign mode. 10: City mode. 11: Theater mode.	
45h (2D8Bh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
46h (2D8Ch)	REG2D8C	7:0	Default : 0x81	Access : R/W
	CH1_SOFTMUTE	7	Software mute channel 1. 0: Normal. 1: Mute.	
	CH1_VOLUME[6:0]	6:0	Volume control. Gain setting = 12db _ N*1.0 dB (+12db ~ -114db) N = 0 ~ 11 (+12 ~ +1db) N = 12 (0db) N = 13 ~ 126 (-1 ~ -114db) N = 127, mute	
46h (2D8Dh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
47h (2D8Eh)	REG2D8E	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	CH1_BALANCEL[3:0]	3:0	Left channel attenuation level. 0000: 0 db. 0001: -1 db. 0010: -2 db.	

Audio 1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description	
			0011: -3 db.	
			0100: -4 db.	
			0101: -5 db.	
			0110: -6 db.	
			0111: -7 db.	
			1000: -8 db.	
			1001: -9 db.	
			1010: -10 db.	
			1011: -11 db.	
			1100: -12 db.	
			1101: -13 db.	
			1110: -14 db.	
			1111: Mute.	
47h (2D8Fh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
48h (2D90h)	REG2D90	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	CH1_BALANCER[3:0]	3:0	Right channel attenuation level. 0000: 0 db. 0001: -1 db. 0010: -2 db. 0011: -3 db. 0100: -4 db. 0101: -5 db. 0110: -6 db. 0111: -7 db. 1000: -8 db. 1001: -9 db. 1010: -10 db. 1011: -11 db. 1100: -12 db. 1101: -13 db. 1110: -14 db. 1111: Mute.	
48h (2D91h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
49h (2D92h)	REG2D92	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	

Audio 1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description	
	CH1_SUBWOFER[3:0]	3:0	Cut-frequency selection for subwoofer. 0000: 50 Hz. 0001: 100 Hz. 0010: 150 Hz. 0011: 200 Hz. 0100: 250 Hz. 0101: 300 Hz. 0110: 350 Hz. 0111: 400 Hz. 1000: 450 Hz. 1001: 500 Hz. 1010: 550 Hz. 1011: 600 Hz. 1100: 650 Hz. 1101: 700 Hz. 1110: 750 Hz. 1111: 800 Hz.	
49h (2D93h)	-	7:0	**Default : -**	**Access : -**
	-	7:0	Reserved.	
4Ah (2D94h)	REG2D94	7:0	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CH1_GRAPHIC_EQ_BAND1[4:0]	4:0	Center frequency is 120Hz. 00000: -12 db. 00001: -11 db. 00010: -10 db. 00011: - 9 db. 00100: - 8 db. 00101: - 7 db. 00110: - 6 db. 00111: - 5 db. 01000: - 4 db. 01001: - 3 db. 01010: - 2 db. 01011: - 1 db. 01100: 0 db. 01101: 1 db. 01110: 2 db. 01111: 3 db. 10000: 4 db.	

Audio 1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description	
			10001: 5 db. 10010: 6 db. 10011: 7 db. 10100: 8 db. 10101: 9 db. 10110: 10 db. 10111: 11 db. 11000: 12 db.	
4Ah (2D95h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
4Bh (2D96h)	REG2D96	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CH1_GRAPHIC_EQ_BAND2[4:0]	4:0	Center frequency is 500Hz; gain setting is the same as 0xBA.	
4Bh (2D97h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
4Ch (2D98h)	REG2D98	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CH1_GRAPHIC_EQ_BAND3[4:0]	4:0	Center frequency is 1.5KHz; gain setting is the same as 0xBA.	
4Ch (2D99h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
4Dh (2D9Ah)	REG2D9A	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CH1_GRAPHIC_EQ_BAND4[4:0]	4:0	Center frequency is 5KHz; gain setting is the same as 0xBA.	
4Dh (2D9Bh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
4Eh (2D9Ch)	REG2D9C	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CH1_GRAPHIC_EQ_BAND5[4:0]	4:0	Center frequency is 10KHz; gain setting is the same as 0xBA.	
4Eh ~ 4Fh (2D9Dh ~ 2D9Fh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	

Audio 1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description	
50h (2DA0h)	REG2DA0	7:0	Default : 0x00	Access : R/W
	CH2_SOFTMUTE	7	Software mute channel 2. 0: Normal. 1: Mute.	
	-	6	Reserved.	
	CH3_SOFTMUTE	5	Software mute channel 3. 0: Normal. 1: Mute.	
	-	4	Reserved.	
	CH4_SOFTMUTE	3	Software Mute channel 4. 0: Normal. 1: Mute.	
	-	2:0	Reserved.	
50h (2DA1h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
51h (2DA2h)	REG2DA2	7:0	Default : 0x00	Access : R/W
	CH2_PRESCALE[7:0]	7:0	Pre-scale value for channel 2 gain control. 00h: Off (mute). & 19h: 0 dB (suggested). & 7Fh: +14 dB (-0.13725 dB per step).	
51h (2DA3h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
52h (2DA4h)	REG2DA4	7:0	Default : 0x00	Access : R/W
	CH3_PRESCALE[7:0]	7:0	Pre-scale value for channel 3 gain control. 00h: Off (mute). & 19h: 0 dB (suggested). & 7Fh: +14 dB (-0.13725 dB per step).	
52h (2DA5h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
53h (2DA6h)	REG2DA6	7:0	Default : 0x00	Access : R/W
	CH4_PRESCALE[7:0]	7:0	Pre-scale value for channel 4 gain control. 00h: Off (mute).	

Audio 1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description	
			& 19h: 0 dB (suggested). & 7Fh: +14 dB (-0.13725 dB per step).	
53h (2DA7h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
54h (2DA8h)	REG2DA8	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	CH1_VOLUME_FRAC[2:0]	6:4	Fraction volume control of CH1. Gain setting = 0.125db * N (0~0.875db) N = 000, 0db N = 001, 0.125db N = 010, 0.250db N = 011, 0.375db N = 100, 0.500db N = 101, 0.625db N = 110, 0.750db N = 111, 0.875db	
	-	3:0	Reserved.	
54h ~ 55h (2DA9h ~ 2DABh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
56h (2DACh)	REG2DAC	7:0	Default : 0x00	Access : R/W
	CH1_DAC_POWER_DOWN	7	DAC power-down enable. 0: Normal mode. 1: Power-down mode.	
	CH1_SWITCH_SOURCE	6	Channel switch. 0: Channel not switched. 1: Channel switched.	
	CH2_DAC_POWER_DOWN	5	DAC power-down enable. 0: Normal mode. 1: Power-down mode.	
	CH2_SWITCH_SOURCE	4	Channel switch. 0: Channel not switched. 1: Channel switched.	
	CH3_DAC_POWER_DOWN	3	DAC power-down enable. 0: Normal mode.	

Audio 1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description	
			1: Power-down mode.	
	CH3_SWITCH_SOURCE	2	Channel switch. 0: Channel not switched. 1: Channel switched.	
	CH4_DAC_POWER_DOWN	1	DAC power-down enable. 0: Normal mode. 1: Power-down mode.	
	CH4_SWITCH_SOURCE	0	Channel switch. 0: Channel not switched. 1: Channel switched.	
56h (2DADh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
57h (2DAEh)	REG2DAE	7:0	Default : 0x00	Access : R/W
	FM_RESERVED_REG[7:0]	7:0	For firmware application.	
57h ~ 5Fh (2DAFh ~ 2DBFh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
60h (2DC0h)	REG2DC0	7:0	Default : -	Access : RO
	-	7:5	Reserved.	
	DSP_DAC_CURRENT[4:0]	4:0	Audio DAC current selection (L/R/LFE). 0-0000: minimum current. & 1-1111: maximum current.	
60h (2DC1h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
61h (2DC2h)	REG2DC2	7:0	Default : 0x00	Access : RO
	DSP_FD230_CODE_VER[7:0]	7:0	DSP FD230 code version.	
61h ~ 63h (2DC3h ~ 2DC7h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
64h (2DC8h)	REG2DC8	7:0	Default : 0x00	Access : RO
	EN_AUDIO_L_VMID	7	Enable control of L-channel VMID buffer. 0: Power-down L-channel VMID buffer. 1: Power-up L-channel VMID buffer.	
	EN_AUDIO_S_VMID	6	Enable control of S-channel VMID buffer. 0: Power-down of S-channel VMID buffer.	

Audio 1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description	
			1: Power-up of S-channel VMID buffer.	
	EN_AUDIO_R_BUFFER	5	Enable control of R-channel output buffer. 0: Power-down R-channel output buffer. 1: Power-up R-channel output buffer.	
	EN_AUDIO_L_BUFFER	4	Enable control of L-channel output buffer. 0: Power-down L-channel output buffer. 1: Power-up L-channel output buffer.	
	EN_AUDIO_S_BUFFER	3	Enable control of LFE-channel output buffer. 0: Power-down LFE-channel output buffer. 1: Power-up LFE-channel output buffer.	
	EN_AUDIO_VREF	2	Enable control of Vref generator. 0: Power-down Vref generator. 1: Power-up Vref generator.	
	EN_AUDIO_VREF_BIAS	1	Enable control of bias current generator. 0: Power-down bias current generator. 1: Power-up bias current generator.	
	EN_AUDIO_BANDGAP	0	Enable control of audio band-gap. 0: Power-down audio band-gap. 1: Power-up audio band-gap.	
64h (2DC9h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
65h (2DCAh)	REG2DCA	7:0	Default : -	Access : RO
	-	7:5	Reserved.	
	EN_AUDIO_I_REF	4	Enable control of audio current mirror. 0: Power-down audio current mirror. 1: Power-up audio current mirror.	
	-	3:2	Reserved.	
	EN_AUDIO_DAC_BIAS	1	Enable control of audio DAC bias circuit. 0: Power-down audio DAC bias circuit. 1: Power-up audio DAC bias circuit.	
	EN_AUDIO_R_VMID	0	Enable control of R-channel VMID buffer. 0: Power-down R-channel VMID buffer. 1: Power-up R-channel VMID buffer.	
65h ~ 66h (2DCBh ~ 2DCDh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
67h	REG2DCE	7:0	Default : 0x00	Access : RO, R/W

Audio 1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description	
(2DCEh)	CH1_DWA_RST	7	Reset DWA. 0: Normal. 1: DWA output all ZERO to analog.	
	CH1_DAC_CLK_ENABLE	6	DAC clock gate. 0: Normal. 1: Enable DAC clock.	
	CH1_FORCE_2ND_ORDER	5	Modulator order. 0: 1st order. 1: 2nd order.	
	CH1_DAC_MODULATOR_ENABLE	4	DAC modulation enable. 0: Enable. 1: Disable.	
	CH2_DWA_RST	3	Reset DWA. 0: Normal. 1: DWA output all ZERO to analog.	
	CH2_DAC_CLK_ENABLE	2	DAC clock gate. 0: Normal. 1: Enable DAC clock.	
	CH2_FORCE_2ND_ORDER	1	Modulator order. 0: 1st Order. 1: 2nd Order.	
	CH2_DAC_MODULATOR_ENABLE	0	DAC modulation enable. 0: Enable. 1: Disable.	
67h (2DCFh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
68h (2DD0h)	REG2DD0	7:0	Default : 0x00	Access : RO, R/W
	CH3_DWA_RST	7	Reset DWA. 0: Normal. 1: DWA output all ZERO to analog.	
	CH3_DAC_CLK_ENABLE	6	DAC clock gate. 0: Normal. 1: Enable DAC clock.	
	CH3_FORCE_2ND_ORDER	5	Modulator order. 0: 1st order. 1: 2nd order.	
	CH3_DAC_MODULATOR_ENABLE	4	DAC modulation enable.	

Audio 1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description	
			0: Enable. 1: Disable.	
	CH4_DWA_RST	3	Reset DWA. 0: Normal. 1: DWA output all ZERO to analog.	
	CH4_DAC_CLK_ENABLE	2	DAC clock gate. 0: Normal. 1: Enable DAC clock.	
	CH4_FORCE_2ND_ORDER	1	Modulator order. 0: 1st order. 1: 2nd order.	
	CH4_DAC_MODULATOR_ENABLE	0	DAC modulation enable. 0: Enable. 1: Disable.	
68h ~ 6Fh (2DD1h ~ 2DDFh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
70h (2DE0h)	REG2DE0	7:0	Default : 0x00	Access : R/W
	AUD_RST_MAD	7	Reset MPEG audio decoder module. 0: Normal. 1: Software reset MAD module.	
	AUD_DIS_DMA	6	Disable MIU DMA request. 0: Normal. 1: Disable (stop accessing DRAM).	
	AUD_CLR_FIFO_STA	5	Clear ES/ PCMI/ PCMO FIFO status (combine with DSP). 0: Normal. 1: Clear.	
	AUD_SEL	4	0: MPEG. 1: AC3.	
	-	3:0	Reserved.	
70h (2DE1h)	REG2DE1	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	AUD_RST_PAS	1	MIPS reset audio PAS. 0: Normal. 1: Software reset audio PAS.	
	AUD_SEL_INTR	0	Select interrupt PIO[7] interrupt source. 0: stream type change.	

Audio 1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description	
			1: SAR detect.	
71h (2DE2h)	REG2DE2	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	STR_TYPE	0	DVB audio stream type, to DSP.	
71h (2DE3h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
72h (2DE4h)	REG2DE4	7:0	Default : 0x00	Access : R/W
	MAD_OFFSET_BASE[7:0]	7:0	MAD memory, including ES, SIF and PCM, buffer base[31:16].	
72h (2DE5h)	REG2DE5	7:0	Default : 0x00	Access : R/W
	MAD_OFFSET_BASE[15:8]	7:0	Please see description of '2DE4h'.	
73h (2DE6h)	REG2DE6	7:0	Default : 0x00	Access : R/W
	MBASE[7:0]	7:0	Indirect configuration, must set MEM_CFG first. Memory buffer base[23:16].	
73h (2DE7h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
74h (2DE8h)	REG2DE8	7:0	Default : 0xFF	Access : R/W
	MSIZE_H[7:0]	7:0	Indirect configuration, must set MEM_CFG first. memory buffer end [15:8] memory buffer end [7:0] = 0xFF actual buffer size = MSIZE + 1	
74h (2DE9h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
75h (2DEAh)	REG2DEA	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	MEM_CFG[2:0]	2:0	Indirect configuration of 0x03 and 0x04 memory space. 000: SIF-ch1 memory configuration. 001: SIF-ch2 memory configuration. 010: ES-ch1 memory configuration. 011: ES-ch2 memory configuration. 100: PCM-ch1 memory configuration. 101: PCM-ch2 memory configuration. 11x: DSP data memory configuration.	
75h (2DEBh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	

Audio 1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description	
76h (2DECh)	REG2DEC	7:0	Default : 0xFF	Access : R/W
	P_AUD_OUT_MODE[1:0]	7:6	DVB audio PCM output mode. 00: Stereo. 01: Left channel. 10: Right channel. 11: Mute.	
	P_AUD_TYPE	5	1: Free run. 0: AV sync.	
	P_AUD_MODE_CMD[4:0]	4:0	System command. 0-0000: Stop (mute). 0-0001: Play. 0-0010: Play file (MHEG5/MP3). Others: reserved.	
76h (2DEDh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
77h (2DEEh)	REG2DEE	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	DSPDMA_CMD_STA	5	Command/status. 0: Idle/finish. 1: Assert to start DMA, auto-cleared when work is finished.	
	DSPDMA_CLR_CNT	4	Clear memory counter. Clear read/write pointer. Update DMA address to base address.	
	DSPDMA_SET_PRIORITY	3	MIU Priority. 0: Low priority. 1: High priority.	
	DSPDMA_WIDTH_SEL	2	Data width. 0: 16 bits. 1: 24 bits.	
	DSPDMA_BURST_LENGTH[1:0]	1:0	Burst length. 00: Reserved. 01: 2 * 64 bits. 10: 3 * 64 bits. 11: 6 * 64 bits. In 24-bit mode, it must align to 3 burst length.	
77h	-	7:0	Default : -	Access : -

Audio 1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description	
(2DEFh)	-	7:0	Reserved.	
78h (2DF0h)	REG2DF0	7:0	Default : 0x00	Access : R/W
	DSPDMA_MIU_ADDR[7:0]	7:0	MIU start address for DMA transfer. Auto-increasing when DMA is working. Auto-wrapping to based address when counted to end address.	
78h (2DF1h)	REG2DF1	7:0	Default : 0x00	Access : R/W
	DSPDMA_MIU_ADDR[15:8]	7:0	Please see description of '2DF0h'.	
79h (2DF2h)	REG2DF2	7:0	Default : 0x00	Access : R/W
	DSPDMA_DSP_ADDR[7:0]	7:0	IDMA address IAD.	
79h (2DF3h)	REG2DF3	7:0	Default : 0x00	Access : R/W
	DSPDMA_DSP_RW	7	DSP IDMA read/write DRAM. 0: Read. 1: Write.	
	DSPDMA_DSP_MEM_SEL	6	DSP IDMA start address for DMA transfer. Auto-increasing when DMA is working. 0: Select PM / CM. 1: Select DM.	
	DSPDMA_DSP_ADDR[13:8]	5:0	Please see description of '2DF2h'.	
7Ah (2DF4h)	REG2DF4	7:0	Default : 0x00	Access : R/W
	DSPDMA_DMA_SIZE[7:0]	7:0	DMA transfer size; unit: 128 bits. It must align to burst length.	
7Ah (2DF5h)	REG2DF5	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	DSPDMA_DMA_SIZE[11:8]	3:0	Please see description of '2DF4h'.	
7Bh (2DF6h)	REG2DF6	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	DSPDMA_CFG[1:0]	1:0	0x58F7 ~ 0x58FA configuration. 00: DMA1. 01: DMA2. 10: DMA3. 11: DMA4.	
7Bh ~ 7Fh (2DF7h ~ 2DFFh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	

DISP_IPMUX Register (Bank = 2E)

DISP_IPMUX Register (Bank = 2E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (2E02h)	REG2E02	7:0	Default : 0x00	Access : R/W
	IPMUX_SEL2[3:0]	7:4	Input source select. 0000: ADC A. 0001: DVI. 0010: VD. 0011: Capture. 0100: Reserved. 0101: Ext VD. 0110: ADC B.	
	IPMUX_SEL1[3:0]	3:0	Input source select. 0000: ADC A. 0001: DVI. 0010: VD. 0011: Capture. 0100: Reserved. 0101: Ext VD. 0110: ADC B.	
02h (2E04h)	REG2E04	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	IPMUX_SEL3[3:0]	3:0	Input source select. 0000: ADC A. 0001: DVI. 0010: VD. 0011: Capture. 0100: Reserved. 0101: Ext VD. 0110: ADC B.	

GOP_INT Register (Bank = 2F, Sub-Bank = 00)

GOP_INT Register (Bank = 2F, Sub-Bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
02h (2F04h)	REG2F04	7:0	Default : 0x00	Access : R/W
	SWRST1[7:0]	7:0	Reset control REG_SWRST1[7]: OSCCLK.	

GOP_INT Register (Bank = 2F, Sub-Bank = 00)

Index (Absolute)	Mnemonic	Bit	Description	
			REG_SWRST1[6]: FCLK domain. REG_SWRST1[5]: REG_SWRST1[4]: IP, include F1 and F2. REG_SWRST1[3]: OP, include OP1, VIP and VOP. REG_SWRST1[2]: IP_F2. REG_SWRST1[1]: IP_F1. REG_SWRST1[0]: All engines.	
03h (2F06h)	REG2F06	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	PDMD[1:0]	1:0	Power-down mode. 1: IDCLK. Other: IDCLK and ODCLK.	
04h (2F08h)	REG2F08	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	VSINT_EDGE	1	OP2 vs INT edge. 1: Tailing. 0: Leading.	
	IPVSINT_EDGE	0	IP vs INT edge. 1: Tailing. 0: Leading.	
04h (2F09h)	REG2F09	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	WDT_INT_ORI	2	Watch dog timer INT for mode detect.	
	WDT_HICNT_EN	1	WDT HICNT enable pulse.	
	CHG_HMD	0	H change mode for INT. 0: Only in leading/tailing of CHG period. 1: Every line gen INT pulse during CHG period.	
05h (2F0Ah)	REG2F0A	7:0	Default : 0x00	Access : R/W
	SYNC_TO_GOP1[1:0]	7:6	Sync signal to GOP_1. 01: IP channel 1. 10: IP channel 2.	
	GOP_SEL_F1[1:0]	5:4	Select GOP source for channel 1. 01: GOP 1. 10: GOP 2.	
	-	3:0	Reserved.	
05h	REG2F0B	7:0	Default : 0x00	Access : R/W

GOP_INT Register (Bank = 2F, Sub-Bank = 00)

Index (Absolute)	Mnemonic	Bit	Description	
(2F0Bh)	SYNC_TO_GOP2[1:0]	7:6	Sync signal to GOP_2. 01: IP channel 1. 10: IP channel 2.	
	GOP_SEL_F2[1:0]	5:4	Select GOP source for channel 2. 01: GOP 1. 10: GOP 2.	
	-	3:0	Reserved.	
06h (2F0Dh)	REG2F0D	7:0	Default : 0x00	Access : R/W
	COP_EN	7	Enable COP for VOP2.	
	GOP2_EN	6	Enable GOP_2 for VOP2.	
	GOP1_EN	5	Enable GOP_1 for VOP2.	
	-	4:0	Reserved.	
10h (2F20h)	REG2F20	7:0	Default : -	Access : RO
	IRQ_FINAL_STS[7:0]	7:0	The final status of interrupt in SC_TOP. ATG_READY_INT_F1, ATG_READY_INT_F2, ATP_READY_INT_F1, ATP_READY_INT_F2, ATS_READY_INT_F1, ATS_READY_INT_F2, CSOG_INT_F1, CSOG_INT_F2, DVI_CK_LOSE_INT_F1, DVI_CK_LOSE_INT_F2, HS_LOSE_INT_F1, HS_LOSE_INT_F2, HTT_CHG_INT_F1, HTT_CHG_INT_F2, IPHCS1_DET_INT_F1, IPHCS1_DET_INT_F2, IPHCS_DET_INT_F1, IPHCS_DET_INT_F2, IPVS_SB_INT_F1, IPVS_SB_INT_F2, JITTER_INT_F1, JITTER_INT_F2, VS_LOSE_INT_F1, VS_LOSE_INT_F2,	

GOP_INT Register (Bank = 2F, Sub-Bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			VTT_CHG_INT_F1, VTT_CHG_INT_F2, VSINT, TUNE_FAIL_P, 4'h0.	
10h (2F21h)	REG2F21	7:0	Default : -	Access : RO
	IRQ_FINAL_STS[15:8]	7:0	Please see description of '2F20h'.	
11h (2F22h)	REG2F22	7:0	Default : -	Access : RO
	IRQ_FINAL_STS[23:16]	7:0	Please see description of '2F20h'.	
11h (2F23h)	REG2F23	7:0	Default : -	Access : RO
	IRQ_FINAL_STS[31:24]	7:0	Please see description of '2F20h'.	
12h (2F24h)	REG2F24	7:0	Default : 0x00	Access : R/W
	IRQ_CLEAR[7:0]	7:0	Clear interrupt.	
12h (2F25h)	REG2F25	7:0	Default : 0x00	Access : R/W
	IRQ_CLEAR[15:8]	7:0	Please see description of '2F24h'.	
13h (2F26h)	REG2F26	7:0	Default : 0x00	Access : R/W
	IRQ_CLEAR[23:16]	7:0	Please see description of '2F24h'.	
13h (2F27h)	REG2F27	7:0	Default : 0x00	Access : R/W
	IRQ_CLEAR[31:24]	7:0	Please see description of '2F24h'.	
14h (2F28h)	REG2F28	7:0	Default : 0xFF	Access : R/W
	IRQ_MSK[7:0]	7:0	Mask IRQ.	
14h (2F29h)	REG2F29	7:0	Default : 0xFF	Access : R/W
	IRQ_MSK[15:8]	7:0	Please see description of '2F28h'.	
15h (2F2Ah)	REG2F2A	7:0	Default : 0xFF	Access : R/W
	IRQ_MSK[23:16]	7:0	Please see description of '2F28h'.	
15h (2F2Bh)	REG2F2B	7:0	Default : 0xFF	Access : R/W
	IRQ_MSK[31:24]	7:0	Please see description of '2F28h'.	
16h (2F2Ch)	REG2F2C	7:0	Default : 0x00	Access : R/W
	IRQ_FORCE[7:0]	7:0	Force a fake interrupt.	
16h (2F2Dh)	REG2F2D	7:0	Default : 0x00	Access : R/W
	IRQ_FORCE[15:8]	7:0	Please see description of '2F2Ch'.	
17h (2F2Eh)	REG2F2E	7:0	Default : 0x00	Access : R/W
	IRQ_FORCE[23:16]	7:0	Please see description of '2F2Ch'.	
17h	REG2F2F	7:0	Default : 0x00	Access : R/W

GOP_INT Register (Bank = 2F, Sub-Bank = 00)

Index (Absolute)	Mnemonic	Bit	Description	
(2F2Fh)	IRQ_FORCE[31:24]	7:0	Please see description of '2F2Ch'.	
18h (2F30h)	REG2F30	7:0	Default : -	Access : RO
	IRQ_RAW_STS[7:0]	7:0	The raw status of interrupt source.	
18h (2F31h)	REG2F31	7:0	Default : -	Access : RO
	IRQ_RAW_STS[15:8]	7:0	Please see description of '2F30h'.	
19h (2F32h)	REG2F32	7:0	Default : -	Access : RO
	IRQ_RAW_STS[23:16]	7:0	Please see description of '2F30h'.	
19h (2F33h)	REG2F33	7:0	Default : -	Access : RO
	IRQ_RAW_STS[31:24]	7:0	Please see description of '2F30h'.	
20h (2F40h)	REG2F40	7:0	Default : -	Access : RO
	BIST_FAIL_0[7:0]	7:0	BIST fail status for LBI.	
20h (2F41h)	REG2F41	7:0	Default : -	Access : RO
	-	7:3	Reserved.	
	BIST_FAIL_0[10:8]	2:0	Please see description of '2F40h'.	
21h (2F42h)	REG2F42	7:0	Default : -	Access : RO
	-	7	Reserved.	
	BIST_FAIL_1[6:0]	6:0	BIST fail status for OP1.	
22h (2F44h)	REG2F44	7:0	Default : -	Access : RO
	BIST_FAIL_2[7:0]	7:0	BIST fail status for VOP, VIP.	
22h (2F45h)	REG2F45	7:0	Default : -	Access : RO
	-	7:5	Reserved.	
	BIST_FAIL_2[12:8]	4:0	Please see description of '2F44h'.	
23h (2F46h)	REG2F46	7:0	Default : -	Access : RO
	BIST_FAIL_3[7:0]	7:0	BIST fail status for SCF.	
23h (2F47h)	REG2F47	7:0	Default : -	Access : RO
	-	7:1	Reserved.	
	BIST_FAIL_3[8]	0	Please see description of '2F46h'.	
24h (2F48h)	REG2F48	7:0	Default : -	Access : RO
	BIST_FAIL_4[7:0]	7:0	BIST fail status for OD.	
24h (2F49h)	REG2F49	7:0	Default : -	Access : RO
	-	7:6	Reserved.	
	BIST_FAIL_4[13:8]	5:0	Please see description of '2F48h'.	

IP1_M Register (Bank = 2F, Sub-Bank = 01)

IP1_M Register (Bank = 2F, Sub-Bank = 01)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
02h (2F04h)	REG2F04	7:0	Default : 0x83 · Access : R/W
	NO_SIGNAL	7	Input source enable. 0: Enable. 1: Disable; output is free-run.
	AUTO_DETSRC[1:0]	6:5	Input sync type. 00: Auto detected. 01: Input is separated HSYNC and VSYNC. 10: Input is composite sync. 11: Input is sync-on-green (SOG).
	COMP_SRC	4	CSYNC/SOG select (only useful when STYPE = 00). 0: CSYNC. 1: SOG.
	CSC_EN	3	Input CSC function. 0: Disable (RGB -> RGB, default). 1: Enable (RGB -> YCbCr).
	SOURCE_SEL[2:0]	2:0	Input source select. 000: Analog 1. 001: Analog 2. 010: Analog 3. 011: DVI. 100: Video. 101: HDTV. 111: HDMI.
02h (2F05h)	REG2F05	7:0	Default : 0x00 · Access : R/W
	FVDO_DIVSEL	7	Force input clock divide function. 0: Disable (auto selected by h/W, used when input is video, default). 1: Enable (use 02h[14:12] as divider).
	-	6	Reserved.
	VD_PORT_SEL	5	External VD port 0: Port 0. 1: Port 1.
	VD_ITU	4	VD ITU656 out, and Digital In for scaler.
	VDEXT_SYNMD	3	External VD using sync. 0: Sync is generated from data internally. 1: Sync from external source.

IP1_M Register (Bank = 2F, Sub-Bank = 01)

Index (Absolute)	Mnemonic	Bit	Description	
	YCBCR_EN	2	Input source is YPbPr format.	
	VIDEO_SEL[1:0]	1:0	Video port select. 00: External 8/10 bits video port. 01: Internal video decoder mode A. 10: External 16/20 bits video port. 11: Internal video decoder mode B.	
03h (2F06h)	REG2F06	7:0	Default : 0x18	Access : R/W
	DIRECT_DE	7	Digital input horizontal sample range. 0: Use DE as sample range, only V position can be adjusted. 1: Use SPRHST and SPRHDC as sample range, both H and V position can be adjusted.	
	DE_ONLY_ORI	6	DE only; HSYNC and VSYNC are ignored. 0: Disable. 1: Enable.	
	VS_DLYMD	5	Input VSYNC delay select. 0: Delay 1/4 input HSYNC. 1: No delay.	
	HS_REFEG	4	Input HSYNC reference edge select. 0: From HSYNC leading edge. 1: From HSYNC tailing edge.	
	VS_REFEG	3	Input VSYNC reference edge select. 0: From VSYNC leading edge. 1: From VSYNC tailing edge.	
	EXTEND_EARLY_LN	2	Early sample line select. 0: 8 lines. 1: 16 lines.	
	VWRAP	1	Input image vertical wrap. 0: Disable. 1: Enable.	
	HWRAP	0	Input image horizontal wrap. 0: Disable. 1: Enable.	
03h (2F07h)	REG2F07	7:0	Default : 0x80	Access : R/W
	FRCV	7	Source sync enable. 0: Display free run, if display select this source. 1: Display will adaptive follow the source, if display select this source.	

IP1_M Register (Bank = 2F, Sub-Bank = 01)

Index (Absolute)	Mnemonic	Bit	Description	
	AUTO_UNLCK	6	Auto lost sync detect enable. When mode change, the sync process for this window will be stopped until setting the source sync enable = 1 again. This is the backup solution for coast.	
	FREE_FOLLOW	5	No memory bank control (used when FRCV=1).	
	FRC_FREEMD	4	Force output odd/even toggle when 2DDi for interlace input.	
	DATA10BIT	3	10 bit input mode.	
	DATA8_ROUND	2	8 bit input mode use rounding.	
	VD16_C_AHEAD	1	Video 16 bit mode fine tune Y/C order.	
	-	0	Reserved.	
04h (2F08h)	REG2F08	7:0	Default : 0x01	Access : R/W
	SPRANGE_VST[7:0]	7:0	Image vertical sample start point, count by input HSYNC.	
04h (2F09h)	REG2F09	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	SPRANGE_VST[10:8]	2:0	Please see description of '2F08h'.	
05h (2F0Ah)	REG2F0A	7:0	Default : 0x01	Access : R/W
	SPRANGE_HST[7:0]	7:0	Image horizontal sample start point, count by input HSYNC.	
05h (2F0Bh)	REG2F0B	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	SPRANGE_HST[10:8]	2:0	Please see description of '2F0Ah'.	
06h (2F0Ch)	REG2F0C	7:0	Default : 0x10	Access : R/W
	SPRANGE_VDC[7:0]	7:0	Image vertical resolution (vertical display enable area count by line).	
06h (2F0Dh)	REG2F0D	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	SPRANGE_VDC[10:8]	2:0	Please see description of '2F0Ch'.	
07h (2F0Eh)	REG2F0E	7:0	Default : 0x10	Access : R/W
	SPRANGE_HDC[7:0]	7:0	Image horizontal resolution (vertical display enable area count by line).	
07h (2F0Fh)	REG2F0F	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	SPRANGE_HDC[10:8]	2:0	Please see description of '2F0Eh'.	

IP1_M Register (Bank = 2F, Sub-Bank = 01)

Index (Absolute)	Mnemonic	Bit	Description	
08h (2F10h)	REG2F10	7:0	Default : 0x20	Access : R/W
	FOSVDCNT_MD	7	Force Ext VD count adjustment Mode. 0: Disable. 1: Enable.	
	VDCNT[1:0]	6:5	VD count for adjusting order of UV, count from HSYNC to first pixel UV order. 00: Normal. 01: 1. 10: 2. 11: 3.	
	VD_NOMSK	4	EAV/SAV mask for video. 0: Mask. 1: No mask.	
	IHSU	3	Input HSYNC usage. When ISEL = 000 or 001 or 010:(ADC) 0: Use HSYNC to perform mode detection, HSOUT from ADC to sample pixel. 1: Use HSYNC only. When ISEL = 011:(DVI) 0: Normal. 1: Enable DE ahead/delay adjust. When ISEL = 100:(VD) 0: Normal. 1: Output Black at blanking.	
	INTLAC_LCKAVG	2	Field time average (interlace lock position average).	
	VDO_YC_SWAP	1	Y/C swap (only useful for 16/20-bit video inputs). 0: Normal. 1: Y/C swap.	
	VDO_ML_SWAP	0	MSB/LSB swap. 0: Normal. 1: MSB/LSB swap.	
08h (2F11h)	REG2F11	7:0	Default : 0x00	Access : R/W
	VDCLK_INV	7	External VD port 0 clock inverse.	
	-	6	Reserved.	
	YPBPR_HS_SEPMD	5	YPbPr HSYNC select mode to mode detector. 0: Use separate HS for coast period. 1: Use PLL HSOUT for coast period.	
	-	4	Reserved.	

IP1_M Register (Bank = 2F, Sub-Bank = 01)

Index (Absolute)	Mnemonic	Bit	Description	
	VDCLK_DLY[3:0]	3:0	External VD port 0 clock delay.	
09h (2F12h)	REG2F12	7:0	Default : 0x00	Access : R/W
	CSC_DITHEN	7	CSC dithering enable when 02h[3]=1.	
	INTLAC_DET_EDGE	6	Interlace detect reference edge. 0: Leading edge. 1: Tailing edge.	
	FILED_ABSMD	5	Interlace detect using middle point method (03h[5]=0 is better).	
	INTLAC_AUTO	4	Interlace/progressive manual switch mode. 0: Auto switch VST(04), VDC (06). 1: Disable auto switch VST(04), VDC(06).	
	Y_LCK[3:0]	3:0	Early sample line for capture port frame information switch. 0000: 8 line ahead from SPRANGE_VST. 0001: 1 line ahead from SPRANGE_VST. 0010: 2 line ahead from SPRANGE_VST. 0011: 3 line ahead from SPRANGE_VST. … 1111: 15 line ahead from SPRANGE_VST.	
0Ah (2F14h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
0Bh (2F17h)	REG2F17	7:0	Default : 0x00	Access : R/W
	H_MIR	7	H mirror enable.	
	-	6:0	Reserved.	
0Ch (2F18h)	REG2F18	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	AUTO_INTLAC_INV	1	Auto filed switch mode filed inverse.	
	AUTO_INTLAC_MD	0	Auto field switch mode for VTT = 2N+1 and 4N+1.	
0Ch (2F19h)	REG2F19	7:0	Default : 0x00	Access : R/W
	CS_DET_CNT[7:0]	7:0	Composite sync separate decision count. 0: HW auto decide. Other: SW program.	
0Dh (2F1Ah)	REG2F1A	7:0	Default : 0x00	Access : R/W
	OVERSAP_EN	7	FIR down sample enable, for FIR double rate 2x -> 1x after FIR purpose. 0: No down, 5 tap support.	

IP1_M Register (Bank = 2F, Sub-Bank = 01)

Index (Absolute)	Mnemonic	Bit	Description	
			1: Down enable, ratio / tap depend on 0D[3:0].	
	OVERSAP_PHS[2:0]	6:4	FIR down sample divider phase.	
	OVERSAP_CNT[3:0]	3:0	FIR down sample divider, for FIR double rate 2x -> 1x after FIR purpose. 0: No down, 5 tap. 1: 2 to 1 down, 11 tap. Other: Reserved. For EXTVD is BT.656, set to 0 and OVERSAP_EN = 1 will do 2X oversample.	
0Eh (2F1Ch)	REG2F1C	7:0	Default : 0x00	Access : RO, R/W
	ATG_HIR	7	Max value flag for R channel (Read Only). 0: Normal. 1: Max value (255) value when ATG_Data_MD = 0. Output over max value (255) when ATG_Data_MD = 1.	
	ATG_HIG	6	Max value flag for G channel (Read Only). 0: Normal. 1: Max value (255) value when ATG_Data_MD = 0. Output over max value (255) when ATG_Data_MD = 1.	
	ATG_HIB	5	Max value flag for B channel (Read Only). 0: Normal. 1: Max value (255) value when ATG_Data_MD = 0. Output over max value (255) when ATG_Data_MD = 1.	
	ATG_CALMD	4	ADC calibration enable. 0: Disable. 1: Reserved.	
	ATG_DATA_MD	3	Auto gain result selection. 0: Output has max/min value. 1: Output is overflow/underflow.	
	ATG_HISMD	2	Auto gain mode. 0: Normal mode (result will be cleared every frame). 1: History mode (result remains not cleared till ATG_EN = 0).	
	ATG_RDY	1	Auto gain result ready. 0: Result not ready. 1: Result ready.	
	ATG_EN	0	Auto gain function enable. 0: Disable. 1: Enable.	

IP1_M Register (Bank = 2F, Sub-Bank = 01)

Index (Absolute)	Mnemonic	Bit	Description	
0Eh (2F1Dh)	REG2F1D	7:0	Default : 0x00	Access : RO, R/W
	-	7	Reserved.	
	AV_DET	6	AV detect for Cb Cr. 0: CbCr range is defined by 03[2]; YCBCR_EN. 1: Cb Cr min. is defined in 89 ATP_GTH; Cb Cr max is define in 8A ATP_TH.	
	-	5:3	Reserved.	
	ATG_UPR	2	Min value flag for R channel. 0: Normal. 1: Min value present when ATG_CALMD = 0, ATG_DATA_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
	ATG_UPG	1	Min value flag for G channel. 0: Normal. 1: Min. value present when ATG_CALMD = 0, ATG_DATA_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
	ATG_UPB	0	Min value flag for B channel. 0: Normal. 1: Min value present when ATG_CALMD = 0, ATG_DATA_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
0Fh (2F1Eh)	REG2F1E	7:0	Default : 0x00	Access : R/W
	AUTO_COAST	7	Auto coast enable when mode change. 0: Disable. 1: Enable.	
	OP2_COAST	6	Coast status (Read only). 0: Coast is inactive. 1: Coast is active (free run).	
	ATPSEL[1:0]	5:4	Auto phase value select (read from registers 0x8C~0x8F). 00: R/G/B total value. 01: Only R value. 10: Only G value. 11: Only B value.	
	PIP_SW_DOUBLE	3	Double sample for:	

IP1_M Register (Bank = 2F, Sub-Bank = 01)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
			1. VD,
			2. Ext VD 656 format,
			3. Ext 444 format,
			The purpose is to provide 2X pixel rate for FIR down sample, and give 11 TAP filter.
	ATGSEL[2:0]	2:0	Select auto gain report for Reg 7D. 000: Minimum R value. 001: Minimum G value. 010: Minimum G value. 011: Maximum R value. 100: Maximum G value. 101: Maximum B value. 11x: Reserved.
10h (2F20h)	REG2F20	7:0	Default : 0x00 Access : RO, R/W
	JIT_R	7	Jitter function left/right result for 86h and 87h. 0: Left result. 1: Right result.
	JIT_SWCLR_SB	6	Jitter software clear. 0: Not clear. 1: Clear.
	-	5	Reserved.
	JITTER_HISMD	4	Jitter function mode. 0: Update every frame. 1: Keep the history value.
	JITTER	3	Jitter function result. 0: No jitter. 1: Jitter present.
	ATS_HISMD	2	Auto position function mode. 0: Update every frame. 1: Keep the history value.
	ATS_RDY	1	Auto position result ready. 0: Result ready. 1: Result not ready.
	ATS_EN	0	Auto position function enable. 0: Disable. 1: Enable. Disable-to-enable needs at least 2 frame apart for ready bit to settle.

IP1_M Register (Bank = 2F, Sub-Bank = 01)

Index (Absolute)	Mnemonic	Bit	Description	
10h (2F21h)	REG2F21	7:0	Default : 0x00	Access : R/W
	THOLD[3:0]	7:4	Auto position valid data value. 0000: Valid if data >= 0000 0000. 0001: Valid if data >= 0001 0000. 0010: Valid if data >= 0010 0000. & & 1111: Valid if data >= 1111 0000.	
	-	3:1	Reserved.	
	ATS_PIXMD	0	Auto position force pixel mode. 0: DE or pixel decide by the source. 1: Force pixel mode.	
11h (2F22h)	REG2F22	7:0	Default : -	Access : RO
	ATGSEL_VALUE[7:0]	7:0	Auto gain value (selected by register 0Fh[2:0]).	
12h (2F24h)	REG2F24	7:0	Default : -	Access : RO
	ATS_VSTDBUF[7:0]	7:0	Auto position detected result vertical starting point.	
12h (2F25h)	REG2F25	7:0	Default : -	Access : RO
	-	7:3	Reserved.	
	ATS_VSTDBUF[10:8]	2:0	Please see description of '2F24h'.	
13h (2F26h)	REG2F26	7:0	Default : -	Access : RO
	ATS_HSTDBUF[7:0]	7:0	Auto position detected result horizontal starting point.	
13h (2F27h)	REG2F27	7:0	Default : -	Access : RO
	-	7:4	Reserved.	
	ATS_HSTDBUF[11:8]	3:0	Please see description of '2F26h'.	
14h (2F28h)	REG2F28	7:0	Default : -	Access : RO
	ATS_VEDDBUF[7:0]	7:0	Auto position detected result vertical end point.	
14h (2F29h)	REG2F29	7:0	Default : -	Access : RO
	-	7:3	Reserved.	
	ATS_VEDDBUF[10:8]	2:0	Please see description of '2F28h'.	
15h (2F2Ah)	REG2F2A	7:0	Default : -	Access : RO
	ATS_HEDDBUF[7:0]	7:0	Auto position detected result horizontal end point.	
15h (2F2Bh)	REG2F2B	7:0	Default : -	Access : RO
	-	7:4	Reserved.	
	ATS_HEDDBUF[11:8]	3:0	Please see description of '2F2Ah'.	
16h	REG2F2C	7:0	Default : -	Access : RO

IP1_M Register (Bank = 2F, Sub-Bank = 01)

Index (Absolute)	Mnemonic	Bit	Description	
(2F2Ch)	REG_JLST[7:0]	7:0	Jitter function detected left/right most point state (previous frame) depend on Reg_10h[7] (default = 7ffh).	
16h (2F2Dh)	**REG2F2D**	**7:0**	**Default : -**	**Access : RO**
	-	7:4	Reserved.	
	REG_JLST[11:8]	3:0	Please see description of '2F2Ch'.	
17h (2F2Eh)	**REG2F2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	L12_LMT_EN	5	Background noise reduction enable. 0: Disable. 1: Enable.	
	HIPX_LMT_EN	4	High level noise reduction enable. 0: Disable. 1: Enable.	
	-	3	Reserved.	
	PIX_TH[2:0]	2:0	Auto noise level. 111: Noise level = 16.	
18h (2F30h)	**REG2F30**	**7:0**	**Default : 0x01**	**Access : R/W**
	ATP_GTH[7:0]	7:0	Auto phase gray scale threshold for ATP[23:16] when ATPN[31:24] = 0.	
18h (2F31h)	**REG2F31**	**7:0**	**Default : 0x10**	**Access : R/W**
	ATP_TH[7:0]	7:0	Auto phase text threshold for ATP[31:24] .	
19h (2F32h)	**REG2F32**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	ATP_GRY	6	Auto phase gray scale detect (Read Only).	
	ATP_TXT	5	Auto phase text detect (Read Only).	
	ATPMSK[2:0]	4:2	Auto phase noise mask. 000: Mask 0 bit, default value. 001: Mask 1 bit. 010: Mask 2 bit. 011: Mask 3 bit. 100: Mask 4 bit. 101: Mask 5 bit. 110: Mask 6 bit. 111: Mask 7 bit.	
	ATP_RDY	1	Auto phase result ready. 0: Result not ready.	

IP1_M Register (Bank = 2F, Sub-Bank = 01)

Index (Absolute)	Mnemonic	Bit	Description	
			1: Result ready.	
	ATP_EN	0	Auto phase function enable. 0: Disable. 1: Enable.	
1Ah (2F34h)	**REG2F34**	**7:0**	**Default : 0x00**	**Access : R/W**
	ATP[7:0]	7:0	Auto phase value.	
1Ah (2F35h)	**REG2F35**	**7:0**	**Default : 0x00**	**Access : R/W**
	ATP[15:8]	7:0	Please see description of '2F34h'.	
1Bh (2F36h)	**REG2F36**	**7:0**	**Default : 0x00**	**Access : R/W**
	ATP[23:16]	7:0	Please see description of '2F34h'.	
1Bh (2F37h)	**REG2F37**	**7:0**	**Default : 0x00**	**Access : R/W**
	ATP[31:24]	7:0	Please see description of '2F34h'.	
1Ch (2F38h)	**REG2F38**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	LB_TUNE_RDY	7	Input VSYNC blanking status. 0: In display. 1: In blanking.	
	DELAYLN_NUM[2:0]	6:4	Delay line after sample V start for input trigger point.	
	-	3:2	Reserved.	
	UNDERRUN	1	Under run status for FIFO.	
	OVERRUN	0	Over run status for FIFO.	
1Dh (2F3Ah)	**REG2F3A**	**7:0**	**Default : 0x05**	**Access : R/W**
	-	7	Reserved.	
	HSTOL[6:0]	6:0	HSYNC tolerance for mode change. 5: Default value.	
1Dh (2F3Bh)	**REG2F3B**	**7:0**	**Default : 0x01**	**Access : R/W**
	VDO_VEDGE	7	Interlace mode VSYNC reference edge.	
	RAW_VSMD	6	Bypass mode raw VSYNC output from SYNC separator.	
	HTT_FILTERMD	5	Auto No signal filter mode. 0: Disable. 1: Enable (update HTT after 4 sequential lines over tolerance).	
	AUTO_NO_SIGNAL	4	Auto no signal enable. This will auto set current bank 02[7] = 1 during mode change.	
	VS_TOL[3:0]	3:0	VSYNC tolerance for mode change. 1: Default value.	

IP1_M Register (Bank = 2F, Sub-Bank = 01)

Index (Absolute)	Mnemonic	Bit	Description	
1Eh (2F3Ch)	**REG2F3C**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SOG_OFFMUX[1:0]	7:6	Off Line SOG source select. 00: Select analog 1 SOG. 01: Select analog 2 SOG. 10: Select analog 3 SOG.	
	IPHCS0_ACT	5	Analog 1 HSYNC pin active.	
	IPHCS1_ACT	4	Analog 2 HSYNC pin active.	
	IPHS_SB_S	3	Input normalized HSYNC pin monitor. Show input HSYNC pin directly. (Active Low)	
	IPVS_SB_S	2	Input normalized VSYNC pin monitor. Show input VSYNC pin directly. (Active Low)	
	OPHS	1	Output normalized HSYNC pin monitor. Show output HSYNC pin directly. (Active Low)	
	OPVS	0	Output normalized VSYNC pin monitor. Show output VSYNC pin directly. (Active Low)	
1Eh (2F3Dh)	**REG2F3D**	**7:0**	**Default : -**	**Access : RO**
	IPVS_ACT	7	Input on line source VSYNC active. 0: Not active. 1: Active.	
	IPHS_ACT	6	Input on line source HSYNC active. 0: Not active. 1: Active.	
	CS_DET	5	Composite sync detected status. 0: Input is not composite sync. 1: Input is detected as composite sync.	
	SOG_DET	4	Sync-On-Green detected status. 0: Input is not SOG. 1: Input is detected as SOG.	
	INTLAC_DET	3	Interlace/non-interlace detecting result by this chip. 0: Non-interlace. 1: Interlace.	
	FLD_DET	2	Input odd/even field detecting result by this chip. 0: Even.	

IP1_M Register (Bank = 2F, Sub-Bank = 01)

Index (Absolute)	Mnemonic	Bit	Description	
			1: Odd.	
	HSPOL	1	Input on line source HSYNC polarity detecting result by this chip. 0: Active low. 1: Active high.	
	VSPOL	0	Input on line source VSYNC polarity detecting result by this chip. 0: Active low. 1: Active high.	
1Fh (2F3Eh)	**REG2F3E**	**7:0**	**Default : 0x00**	**Access : R/W**
	VTT[7:0]	7:0	Input vertical total, count by HSYNC.	
1Fh (2F3Fh)	**REG2F3F**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_PW_VDOMD	7	VSYNC raw pulse width for measurement.	
	-	6	Reserved.	
	HSPW_SEL	5	VSYNC pulse width read enable. The report is shown in current bank 22.	
	-	4:3	Reserved.	
	VTT[10:8]	2:0	Please see description of '2F3Eh'.	
20h (2F40h)	**REG2F40**	**7:0**	**Default : 0x00**	**Access : R/W**
	HTT_FOR_READ[7:0]	7:0	Input horizontal period, count by reference clock.	
20h (2F41h)	**REG2F41**	**7:0**	**Default : 0x00**	**Access : R/W**
	LN4_DETMD	7	Input HSYNC period detect mode. 0: 1 line. 1: 8 lines.	
	TEST_CSHTT	6	Report sync separator HTT by E5, E4. 0: HTT report by mode detector. 1: HTT report by sync separator.	
	HTT_FOR_READ[13:8]	5:0	Please see description of '2F40h'.	
21h (2F42h)	**REG2F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	FLD_SWMD	7	Shift line method during field switch. 0: Old method. 1: New method.	
	COAST_HS_SEPMD	6	HSYNC in coast for data capture. 0: HSOUT (recommended). 1: Re-shaped HSYNC.	
	USR_VSPOL	5	User defined input VSYNC polarity, active when	

IP1_M Register (Bank = 2F, Sub-Bank = 01)

Index (Absolute)	Mnemonic	Bit	Description	
			USR_VSPOLMD =1. 0: Active low. 1: Active high.	
	USR_VSPOLMD	4	Input VSYNC polarity judgment. 0: Use result of internal circuit detection. 1: Defined by user (USR_VSPOL).	
	USR_HSPOL	3	User defined input HSYNC Polarity, active when USR_HSPOLMD =1. 0: Active low. 1: Active high.	
	USR_HSPOLMD	2	Input HSYNC polarity judgment. 0: Use result of internal circuit detection. 1: Defined by user (USR_HSPOL).	
	USR_INTLAC	1	User defined non-interlace/interlace, active when USR_INTLACMD = 1. 0: Non-interlace. 1: Interlace.	
	USR_INTLACMD	0	Interlace judgment. 0: Use result of internal circuit detection. 1: Defined by user (USR_INTLAC).	
21h (2F43h)	REG2F43	7:0	Default : 0x00	Access : R/W
	MEMSYN_TO_VS[1:0]	7:6	Memory control switch method. 00: Sample V end. 01: Sample V start. 10: Sample V start ahead by current Bank 09[3:0]. 11: Sample V start ahead by current Bank 09[3:0] x 2.	
	DE_ONLY_HTT_CHGMD	5	DE only mode HTT change status mode. 0: Mode change provide in data clock domain. 1: Mode change provide in data clock and fix clock domain (Recommended).	
	DE_ONLY_HTT_SRC	4	DE only mode HTT report source. 0: Form input DE. 1: From re-generated DE.	
	ADC_VIDEO_FINV	3	Component video field inversion when ADC_VIDEO = 1 for data align. 0: Normal. 1: Invert.	
	EXT_FLDMD	2	Video external field.	

IP1_M Register (Bank = 2F, Sub-Bank = 01)

Index (Absolute)	Mnemonic	Bit	Description	
			0: Use result of internal circuit detection. 1: Use external field.	
	FLD_DETMD	1	Interlace field detect method select. 0: Use the HSYNC numbers of a field to judge. 1: Use the relationship of VSYNC and HSYNC to judge.	
	FLD_INV	0	Interlace field invert. 0: Normal. 1: Invert.	
22h (2F44h)	REG2F44	7:0	Default : 0x00	Access : RO
	HSPW[7:0]	7:0	Pulse width report If current bank HSPW_SEL (1F[13]) = 0, report HSYNC. If current bank HSPW_SEL (1F[13]) = 1, report VSYNC.	
23h (2F46h)	REG2F46	7:0	Default : 0x1E	Access : R/W
	DVICK_WIDTH[7:0]	7:0	DVI clock detection threshold, see CAH for usage (default 0x1E). CAH[6] = 0: DVI clock is OK, Freq(DVI) > Freq(XTAL) * 23h/128. CAH[6] = 1: DVI clock is missing, Freq(DVI) < Freq(XTAL) * 23h/128. Where EBH default to 0x1E(30).	
23h (2F47h)	REG2F47	7:0	Default : 0x00	Access : RO, R/W
	VD_FREE	7	Video in free-run mode (Read Only).	
	MIN_VTT[6:0]	6:0	Minimum VTT. When detected VTT < MIN_VTT[6:0] x 16, into the video interlace free-run mode.	
24h (2F48h)	REG2F48	7:0	Default : 0x00	Access : R/W
	VS_SEP_SEL	7	SYNC separates VSYNC for mode detect. 0: RAW VSYNC (H/V relationship is kept for interlace detect). 1: HSYNC align VSYNC (H/V relationship is lost for interlace detect).	
	VIDEO_D1L_H	6	Component video delay line. (VIDEO_D1L_H + VIDEO_D1L_L) = 00: Delay 1 line for another field. 01: Delay 2 line for another field. 10: Delay 3 line for another field. 11: Delay 4 line for another field.	

IP1_M Register (Bank = 2F, Sub-Bank = 01)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	ADC_VIDEO	5	ADC input select. 0: PC source. 1: Component video.
	VIDEO_D1L_L	4	Component video delay line. (VIDEO_D1L_H + VIDEO_D1L_L) = 00: Delay 1 line for another field. 01: Delay 2 line for another field. 10: Delay 3 line for another field. 11: Delay 4 line for another field.
	CS_CUT_MD	3	Composite SYNC cut mode (for testing). 0: Disable. 1: Enable.
	EXTVS_SEPINV	2	External VSYNC polarity (only used when COAST_SRCS is 1). 0: Normal. 1: Invert.
	COAST_SRC	1	Coast VSYNC select. 0: Separates VSYNC internally (Default). 1: External VSYNC (for testing).
	COAST_POL	0	Coast polarity to PAD.
24h (2F49h)	**REG2F49**	**7:0**	**Default : 0x00** Access : R/W
	COAST_FBD[7:0]	7:0	Front tuning. 00: Coast start from 1 HSYNC leading edge. 01: Coast start from 2 HSYNC leading edge, default value. & 254: Coast start from 255 HSYNC leading edge. 255: Coast start from 256 HSYNC leading edge.
25h (2F4Ah)	**REG2F4A**	**7:0**	**Default : 0x00** Access : R/W
	COAST_BBD[7:0]	7:0	End tuning. 00: Coast end at 1 HSYNC leading edge. 01: Coast end at 2 HSYNC leading edge, default value. & 254: Coast end at 255 HSYNC leading edge. 255: Coast end at 256 HSYNC leading edge.
26h (2F4Ch)	**REG2F4C**	**7:0**	**Default : 0x00** Access : R/W
	GR_DE_EN	7	DE or HSYNC post glitch removal function enable. 0: Disable. 1: Enable.

IP1_M Register (Bank = 2F, Sub-Bank = 01)

Index (Absolute)	Mnemonic	Bit	Description	
	FILTER_NUM[2:0]	6:4	DE or HSYNC post glitch removal range. Analog: 000: 0 XTAL clock. 001: 1 XTAL clock. 010: 2 XTAL clock. 111: 7 XTAL clock. DVI: 000: 0x8 input clock. 001: 1x8 input clock. 010: 2x8 input clock. 111: 7x8 input clock.	
	GR_HS_VIDEO	3	Input HSYNC filter. When input source is analog: 0: Filter off. 1: Filter on. When input source is DVI: 0: Normal. 1: More tolerance for unstable DE.	
	GR_EN	2	Input sync sample mode. 0: Normal. 1: Glitch-removal.	
	HVTT_LOSE_MD	1	HTT/VTT lost mode for INT. 0: By counter overflow. 1: By counter overflow + Active Detect IPVS_ACT, IPHS_ACT (E1[7:6]) (Recommended).	
	IDCLK_INV	0	Capture port sample CLK invert. 0: Normal. 1: Invert.	
27h (2F4Eh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
29h (2F52h)	REG2F52	7:0	Default : 0x00	Access : RO, R/W
	VS_SEP_SEL_1	7	New interlace detect method by big and small line counts for a field.	
	VS_SEP_SEL_0	6	Hardware auto VSYNC start line method select.	
	INTLAC_DET_MD[1:0]	5:4	Interlace detect mode. 00: Off. 01: Only for line total number is even. 10: All case.	

IP1_M Register (Bank = 2F, Sub-Bank = 01)

Index (Absolute)	Mnemonic	Bit	Description	
			11: Off.	
	EUP_AU_HDTV_DET	3	Europe/Australia 1080i HDTV detect.	
	EUP_HDTV_DET	2	Europe 1080i HDTV detect.	
	EUP_AUTOFLD	1	EUR/AUS 1080i HDTV auto field mode.	
	EUP_HDTV	0	EUR/AUS 1080i HDTV force field mode.	
29h (2F53h)	REG2F53	7:0	Default : 0x00	Access : RO, R/W
	LCK2LCK_RPT[3:0]	7:4	Check lock to lock line count for interlace auto-correct.	
	-	3:1	Reserved.	
	ATRANGE_EN	0	Auto range enable. 0: Define automatically. 1: Define by current Bank 2a-2b.	
2Ah (2F54h)	REG2F54	7:0	Default : 0x00	Access : R/W
	ATRANGE_VST[7:0]	7:0	Auto function (position, gain phase) vertical start point, count by input HSYNC.	
2Ah (2F55h)	REG2F55	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	ATRANGE_VST[10:8]	2:0	Please see description of '2F54h'.	
2Bh (2F56h)	REG2F56	7:0	Default : 0x00	Access : R/W
	ATRANGE_HST[7:0]	7:0	Auto function (position, gain phase) horizontal start point, count by input dot clock.	
2Bh (2F57h)	REG2F57	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	ATRANGE_HST[10:8]	2:0	Please see description of '2F56h'.	
2Ch (2F58h)	REG2F58	7:0	Default : 0x00	Access : R/W
	ATRANGE_VDC[7:0]	7:0	Auto function (position, gain phase) vertical resolution, count by input HSYNC.	
2Ch (2F59h)	REG2F59	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	ATRANGE_VDC[10:8]	2:0	Please see description of '2F58h'.	
2Dh (2F5Ah)	REG2F5A	7:0	Default : 0x00	Access : R/W
	ATRANGE_HDC[7:0]	7:0	Auto function (position, gain phase) horizontal resolution, count by input dot clock.	
2Dh (2F5Bh)	REG2F5B	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	

IP1_M Register (Bank = 2F, Sub-Bank = 01)

Index (Absolute)	Mnemonic	Bit	Description	
	ATRANGE_HDC[10:8]	2:0	Please see description of '2F5Ah'.	
2Eh (2F5Ch)	REG2F5C	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	GOP_CLK_FREE	1	GOP clock gating enable 0: Can gate the GOP clock. 1: Don't gate the GOP clock.	
	IP2_CLK_GATE_EN	0	IP2 clock gating enable 0: Don't gate the IDCLK. 1: Can gate the IDCLK.	
30h (2F60h)	REG2F60	7:0	Default : 0x00	Access : R/W
	INSERT_NUM[7:0]	7:0	VSYNC insert number offset.	
30h (2F61h)	REG2F61	7:0	Default : 0x00	Access : R/W
	INSERT_SEL	7	VSYNC insert number offset enable.	
	-	6:3	Reserved.	
	INSERT_NUM[10:8]	2:0	Please see description of '2F60h'.	
31h (2F62h)	REG2F62	7:0	Default : 0x00	Access : R/W
	LCK_NUM[7:0]	7:0	VSYNC lock number offset.	
31h (2F63h)	REG2F63	7:0	Default : 0x00	Access : R/W
	LCK_SEL	7	VSYNC lock number offset enable.	
	-	6:3	Reserved.	
	LCK_NUM[10:8]	2:0	Please see description of '2F62h'.	
32h (2F64h)	REG2F64	7:0	Default : 0x00	Access : R/W
	VLCK[7:0]	7:0	V-lock.	
32h (2F65h)	REG2F65	7:0	Default : 0x00	Access : R/W
	VLCK[15:8]	7:0	Please see description of '2F64h'.	

IP2_M Register (Bank = 2F, Sub-Bank = 02)

IP2_M Register (Bank = 2F, Sub-Bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (2F02h)	REG2F02	7:0	Default : 0x00	Access : R/W
	VFAC_SHT	7	VSD factor shift enable.	
	VFAC_SHT_INV	6	VSD field inverse.	
	IP2_F422EN	5	Force IP 442 format enable.	
	IP2_F422	4	0: IP 444. 1: IP 422.	
	-	3:2	Reserved.	
	VSD_DITHEN	1	VSD dither function enable.	
	HSD_DITHEN	0	HSD dither function enable.	
02h (2F04h)	REG2F04	7:0	Default : 0x00	Access : R/W
	HFAC_SET_IP[7:0]	7:0	HSD initial factor.	
02h (2F05h)	REG2F05	7:0	Default : 0x00	Access : R/W
	HFAC_SET_IP[15:8]	7:0	Please see description of '2F04h'.	
03h (2F06h)	REG2F06	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	HFAC_SET_IP[19:16]	3:0	Please see description of '2F04h'.	
04h (2F08h)	REG2F08	7:0	Default : 0x00	Access : R/W
	HFACIN0[7:0]	7:0	HSD factor, format [3.20].	
04h (2F09h)	REG2F09	7:0	Default : 0x00	Access : R/W
	HFACIN0[15:8]	7:0	Please see description of '2F08h'.	
05h (2F0Ah)	REG2F0A	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	HFACIN1[22:16]	6:0	HSD factor, format [3.20].	
05h (2F0Bh)	REG2F0B	7:0	Default : 0x00	Access : R/W
	IP2HSDEN	7	H scaling-down enable.	
	PREHSDMD	6	0: Accumulator mode, FAC = OUT/IN (format [0.20]). 1: 6TapY/4TapC filter mode, FAC = IN/OUT (format [3.20]).	
	-	5:0	Reserved.	
06h (2F0Ch)	REG2F0C	7:0	Default : 0x00	Access : R/W
	VFAC_SET_IP[7:0]	7:0	VSD initial factor.	
06h	REG2F0D	7:0	Default : 0x00	Access : R/W

IP2_M Register (Bank = 2F, Sub-Bank = 02)

Index (Absolute)	Mnemonic	Bit	Description	
(2F0Dh)	VFAC_SET_IP[15:8]	7:0	Please see description of '2F0Ch'.	
07h (2F0Eh)	REG2F0E	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	VFAC_SET_IP[19:16]	3:0	Please see description of '2F0Ch'.	
08h (2F10h)	REG2F10	7:0	Default : 0x00	Access : R/W
	VFACIN0[7:0]	7:0	VSD factor, format [0.20].	
08h (2F11h)	REG2F11	7:0	Default : 0x00	Access : R/W
	VFACIN0[15:8]	7:0	Please see description of '2F10h'.	
09h (2F12h)	REG2F12	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	VFACIN1[19:16]	3:0	VSD factor, format [0.20].	
09h (2F13h)	REG2F13	7:0	Default : 0x00	Access : R/W
	PRE_VDOWN	7	V scaling-down enable.	
	-	6:0	Reserved.	
0Ah (2F14h)	REG2F14	7:0	Default : 0x00	Access : R/W
	C_FILTER[2:0]	7:5	444 to 422 filter.	
	YDELAY_EN	4	Y delay enable.	
	YCDELAY_STEP[3:0]	3:0	Y/C delay pipe step.	
16h (2F2Ch)	REG2F2C	7:0	Default : 0xF2	Access : R/W
	HSD_YT0_C0[7:0]	7:0	Up-sample 1st pix (oxxx) coef. Y0. Format: S7. of 2's complement (-31 <= Y0 <= 31).	
17h (2F2Eh)	REG2F2E	7:0	Default : 0x1F	Access : R/W
	HSD_YT0_C1[7:0]	7:0	Up-sample 1st pix (oxxx) coef. Y1. Format: S7. of 2's complement (-63 <= Y1 <= 63).	
18h (2F30h)	REG2F30	7:0	Default : 0x5E	Access : R/W
	HSD_YT0_C2[7:0]	7:0	Up-sample 1st pix (oxxx) coef. Y2. Format: fix 8. (0 <= Y2 <= 255)	
19h (2F32h)	REG2F32	7:0	Default : 0xF4	Access : R/W
	HSD_YT1_C0[7:0]	7:0	Up-sample 2nd pix (xoxx) coef. Y0. Format: S7. of 2's complement (-31 <= Y0 <= 31).	
1Ah (2F34h)	REG2F34	7:0	Default : 0x0C	Access : R/W
	HSD_YT1_C1[7:0]	7:0	Up-sample 2nd pix (xoxx) coef. Y1. Format: S7. of 2's complement (-63 <= Y1 <= 63).	
1Bh	REG2F36	7:0	Default : 0x5A	Access : R/W

IP2_M Register (Bank = 2F, Sub-Bank = 02)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
(2F36h)	HSD_YT1_C2[7:0]	7:0	Up-sample 2nd pix (xoxx) coef. Y2. Format : fix 8.(0 <= Y2 <= 255).
1Ch (2F38h)	REG2F38	7:0	Default : 0x37	Access : R/W
	HSD_YT1_C3[7:0]	7:0	Up-sample 2nd pix (xoxx) coef. Y3. Format: fix 8.(0 <= Y3 <= 255).
1Dh (2F3Ah)	REG2F3A	7:0	Default : 0xF5	Access : R/W
	HSD_YT1_C4[7:0]	7:0	Up-sample 2nd pix (xoxx) coef. Y4. Format: S7. of 2's complement (-63 <= Y4 <= + 63).
1Eh (2F3Ch)	REG2F3C	7:0	Default : 0xFA	Access : R/W
	HSD_YT1_C5[7:0]	7:0	Up-sample 2nd pix (xoxx) coef. Y5. Format: S7. of 2's complement (-31 < Y5 <= 31).
1Fh (2F3Eh)	REG2F3E	7:0	Default : 0xF7	Access : R/W
	HSD_YT2_C0[7:0]	7:0	Up-sample 3rd pix (xxox) coef. Y0. Format: S7. of 2's complemen (-15 <= Y0 <= 15).
20h (2F40h)	REG2F40	7:0	Default : 0xFE	Access : R/W
	HSD_YT2_C1[7:0]	7:0	Up-sample 3rd pix (xxox) coef. Y1. Format: S7. of 2's complement (-63 <= Y1 <= 63).
21h (2F42h)	REG2F42	7:0	Default : 0x4B	Access : R/W
	HSD_YT2_C2[7:0]	7:0	Up-sample 3rd pix (xxox) coef. Y2. Format: fix 8.(0 <= Y2 <= 127).
2Ch (2F58h)	REG2F58	7:0	Default : 0x44	Access : R/W
	-	7	Reserved.
	CTI_STEP[2:0]	6:4	CTI filter step.
	-	3	Reserved.
	CTI_LPF_COEF[2:0]	2:0	CTI low-pass filter coefficient.
2Ch (2F59h)	REG2F59	7:0	Default : 0x3F	Access : R/W
	-	7:6	Reserved.
	CTI_BAND_COEF[5:0]	5:0	CTI band-pass filter coefficient.
2Dh (2F5Ah)	REG2F5A	7:0	Default : 0x88	Access : R/W
	CTI_MEDIAN_EN	7	CTI median filter enable.
	-	6:4	Reserved.
	CTI_CORING_THRD[3:0]	3:0	CTI coring threshold.
2Dh (2F5Bh)	REG2F5B	7:0	Default : 0x00	Access : R/W
	CTI_EN	7	CTI enable.

IP2_M Register (Bank = 2F, Sub-Bank = 02)

Index (Absolute)	Mnemonic	Bit	Description
	-	6:4	Reserved.
	CTI_AUTO_NO_MED	3	CTI auto-turn-off median mode.
	-	2:0	Reserved.

IP1_S Register (Bank = 2F, Sub-Bank = 03)

IP1_S Register (Bank = 2F, Sub-Bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
02h (2F04h)	REG2F04	7:0	Default : 0x83	Access : R/W
	NO_SIGNAL	7	Input source enable. 0: Enable. 1: Disable; output is free-run.	
	AUTO_DETSRC[1:0]	6:5	Input sync type. 00: Auto detected. 01: Input is separated HSYNC and VSYNC. 10: Input is composite sync. 11: Input is sync-on-green (SOG).	
	COMP_SRC	4	CSYNC/SOG select (only useful when STYPE = 00). 0: CSYNC. 1: SOG.	
	CSC_EN	3	Input CSC function. 0: Disable (RGB -> RGB, default). 1: Enable (RGB -> YCbCr).	
	SOURCE_SEL[2:0]	2:0	Input source select. 000: Analog 1. 001: Analog 2. 010: Analog 3. 011: DVI. 100: Video. 101: HDTV. 111: HDMI.	
02h (2F05h)	REG2F05	7:0	Default : 0x00	Access : R/W
	FVDO_DIVSEL	7	Force input clock divide function. 0: Disable (Default: auto selected by H/W, used when input is video). 1: Enable (use 02h[14:12] as divider).	

IP1_S Register (Bank = 2F, Sub-Bank = 03)

Index (Absolute)	Mnemonic	Bit	Description	
	-	6	Reserved.	
	VD_PORT_SEL	5	External VD port. 0: Port 0. 1: Port 1.	
	VD_ITU	4	VD BT.656 out, and digital in for scaler.	
	VDEXT_SYNMD	3	External VD using sync. 0: Sync is generated from data internally. 1: Sync from external source.	
	YCBCR_EN	2	Input source is YPbPr format.	
	VIDEO_SEL[1:0]	1:0	Video port select. 00: External 8/10 bits video port. 01: Internal video decoder mode A. 10: External 16/20 bits video port. 11: Internal video decoder mode B.	
03h (2F06h)	REG2F06	7:0	Default : 0x18	Access : R/W
	DIRECT_DE	7	Digital input horizontal sample range. 0: Use DE as sample range, only V position can be adjusted. 1: Use SPRHST and SPRHDC as sample range, both H and V position can be adjusted.	
	DE_ONLY_ORI	6	DE only; HSYNC and VSYNC are ignored. 0: Disable. 1: Enable.	
	VS_DLYMD	5	Input VSYNC delay select. 0: Delay 1/4 input HSYNC. 1: No delay.	
	HS_REFEG	4	Input HSYNC reference edge select. 0: From HSYNC leading edge. 1: From HSYNC tailing edge.	
	VS_REFEG	3	Input VSYNC reference edge select. 0: From VSYNC leading edge. 1: From VSYNC tailing edge.	
	EXTEND_EARLY_LN	2	Early sample line select. 0: 8 lines. 1: 16 lines.	
	VWRAP	1	Input image vertical wrap. 0: Disable.	

IP1_S Register (Bank = 2F, Sub-Bank = 03)

Index (Absolute)	Mnemonic	Bit	Description	
			1: Enable.	
	HWRAP	0	Input image horizontal wrap. 0: Disable. 1: Enable.	
03h (2F07h)	REG2F07	7:0	Default : 0x80	Access : R/W
	FRCV	7	Source sync enable. 1: Display will be adaptive following the source if display select this source. 0: Display free-run if display select this source.	
	AUTO_UNLCK	6	Auto lost sync detect enable. During mode change, the sync process for this window will be stop until setting the source sync enable = 1 again. This is the backup solution for coast.	
	FREE_FOLLOW	5	No memory bank control (used when FRCV=1).	
	FRC_FREEMD	4	Force output odd/even toggle when 2DDi for interlace input.	
	DATA10BIT	3	10 bit input mode.	
	DATA8_ROUND	2	8 bit input mode use rounding.	
	VD16_C_AHEAD	1	Video 16 bit mode fine tune Y/C order.	
	-	0	Reserved.	
04h (2F08h)	REG2F08	7:0	Default : 0x01	Access : R/W
	SPRANGE_VST[7:0]	7:0	Image vertical sample start point, count by input HSYNC.	
04h (2F09h)	REG2F09	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	SPRANGE_VST[10:8]	2:0	Please see description of '2F08h'.	
05h (2F0Ah)	REG2F0A	7:0	Default : 0x01	Access : R/W
	SPRANGE_HST[7:0]	7:0	Image horizontal sample start point, count by input HSYNC.	
05h (2F0Bh)	REG2F0B	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	SPRANGE_HST[10:8]	2:0	Please see description of '2F0Ah'.	
06h (2F0Ch)	REG2F0C	7:0	Default : 0x10	Access : R/W
	SPRANGE_VDC[7:0]	7:0	Image vertical resolution (vertical display enable area count by line).	
06h	REG2F0D	7:0	Default : 0x00	Access : R/W

IP1_S Register (Bank = 2F, Sub-Bank = 03)

Index (Absolute)	Mnemonic	Bit	Description	
(2F0Dh)	-	7:3	Reserved.	
	SPRANGE_VDC[10:8]	2:0	Please see description of '2F0Ch'.	
07h (2F0Eh)	**REG2F0E**	**7:0**	**Default : 0x10**	**Access : R/W**
	SPRANGE_HDC[7:0]	7:0	Image horizontal resolution (vertical display enable area count by line).	
07h (2F0Fh)	**REG2F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SPRANGE_HDC[10:8]	2:0	Please see description of '2F0Eh'.	
08h (2F10h)	**REG2F10**	**7:0**	**Default : 0x20**	**Access : R/W**
	FOSVDCNT_MD	7	Force ext. VD count adjustment mode. 0: Disable. 1: Enable.	
	VDCNT[1:0]	6:5	VD count for adjusting order of UV, count from HSYNC to first pixel UV order. 00: Normal. 01: 1. 10: 2. 11: 3.	
	VD_NOMSK	4	EAV/SAV mask for video. 0: Mask. 1: No mask.	
	IHSU	3	Input HSYNC usage. When ISEL = 000 or 001 or 010:(ADC). 0: Use HSYNC to perform mode detection, HSOUT from ADC to sample pixel. 1: Use HSYNC only. When ISEL = 011:(DVI) 0: Normal. 1: Enable DE ahead/delay adjust. When ISEL = 100:(VD) 0: Normal. 1: Output black at blanking.	
	INTLAC_LCKAVG	2	Field time average (interlace lock position average).	
	VDO_YC_SWAP	1	Y/C swap (only useful for 16/20-bit video inputs). 0: Normal. 1: Y/C swap.	
	VDO_ML_SWAP	0	MSB/LSB swap.	

IP1_S Register (Bank = 2F, Sub-Bank = 03)

Index (Absolute)	Mnemonic	Bit	Description	
			0: Normal. 1: MSB/LSB swap.	
08h (2F11h)	REG2F11	7:0	Default : 0x00	Access : R/W
	VDCLK_INV	7	External VD port 0 clock inverse.	
	-	6	Reserved.	
	YPBPR_HS_SEPMD	5	YPbPr HSYNC select mode to mode detector. 0: Use separate HS for coast period. 1: Use PLL HSOUT for coast period.	
	-	4	Reserved.	
	VDCLK_DLY[3:0]	3:0	External VD port 0 clock delay.	
09h (2F12h)	REG2F12	7:0	Default : 0x00	Access : R/W
	CSC_DITHEN	7	CSC dithering enable when 02h[3]=1.	
	INTLAC_DET_EDGE	6	Interlace detect reference edge. 0: Leading edge. 1: Tailing edge.	
	FILED_ABSMD	5	Interlace detect using middle point method (03h[5]=0 is better).	
	INTLAC_AUTO	4	Interlace/progressive manual switch mode. 0: Auto switch VST(04), VDC (06). 1: Disable auto switch VST(04), VDC(06).	
	Y_LCK[3:0]	3:0	Early sample line for capture port frame information switch. 0000: 8 line ahead from SPRANGE_VST. 0001: 1 line ahead from SPRANGE_VST. 0010: 2 line ahead from SPRANGE_VST. 0011: 3 line ahead from SPRANGE_VST. … 1111: 15 line ahead from SPRANGE_VST.	
0Ah (2F14h)	REG2F14	7:0	Default : 0x00	Access : R/W
	IP_INT_SEL[7:0]	7:0	No load (Reserved).	
0Bh (2F17h)	REG2F17	7:0	Default : 0x00	Access : R/W
	H_MIR	7	H mirror enable.	
	-	6:0	Reserved.	
0Ch (2F18h)	REG2F18	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	AUTO_INTLAC_INV	1	Auto filed switch mode filed inverse.	

IP1_S Register (Bank = 2F, Sub-Bank = 03)

Index (Absolute)	Mnemonic	Bit	Description	
	AUTO_INTLAC_MD	0	Auto field switch mode for VTT = 2N+1 and 4N+1.	
0Ch (2F19h)	**REG2F19**	**7:0**	**Default : 0x00**	**Access : R/W**
	CS_DET_CNT[7:0]	7:0	Composite sync separate decision count. 0: HW auto decide. Others: SW program	
0Dh (2F1Ah)	**REG2F1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	OVERSAP_EN	7	FIR down sample enable, for FIR double rate 2x -> 1x after FIR purpose. 0: No down, 5 tap support. 1: Down enable, ratio/tap depend on 0D[3:0].	
	OVERSAP_PHS[2:0]	6:4	FIR down sample divider phase.	
	OVERSAP_CNT[3:0]	3:0	FIR down sample divider, for FIR double rate 2x -> 1x after FIR purpose. 0: No down, 5 tap. 1: 2 to 1 down, 11 tap. Others: Reserved. For EXTVD is BT.656, set to 0 and OVERSAP_EN = 1 will do 2X oversample.	
0Eh (2F1Ch)	**REG2F1C**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	ATG_HIR	7	Max value flag for R channel (Read Only). 0: Normal. 1: Max value (255) value when ATG_DATA_MD = 0. Output over max value (255) when ATG_DATA_MD = 1.	
	ATG_HIG	6	Max value flag for G channel (Read Only). 0: Normal. 1: Max value (255) value when ATG_DATA_MD = 0. Output over max value (255) when ATG_DATA_MD = 1.	
	ATG_HIB	5	Max value flag for B channel (Read Only). 0: Normal. 1: Max value (255) value when ATG_DATA_MD = 0. Output over max value (255) when ATG_DATA_MD = 1.	
	ATG_CALMD	4	ADC calibration enable. 0: Disable. 1: Reserved.	
	ATG_DATA_MD	3	Auto gain result selection. 0: Output has max/min value. 1: Output is overflow/underflow.	

IP1_S Register (Bank = 2F, Sub-Bank = 03)

Index (Absolute)	Mnemonic	Bit	Description	
	ATG_HISMD	2	Auto gain mode. 0: Normal mode (result will be cleared every frame). 1: History mode (result remains not cleared till ATG_EN = 0).	
	ATG_RDY	1	Auto gain result ready. 0: Result not ready. 1: Result ready.	
	ATG_EN	0	Auto gain function enable. 0: Disable. 1: Enable.	
0Eh (2F1Dh)	REG2F1D	7:0	Default : 0x00	Access : RO, R/W
	-	7	Reserved.	
	AV_DET	6	AV Detect for Cb Cr 0: CbCr range is defined by 03[2]; YCBCR_EN. 1: Cb Cr min. is defined in 89 ATP_GTH, Cb Cr max is defined in 8A ATP_TH.	
	-	5:3	Reserved.	
	ATG_UPR	2	Min value flag for R channel. 0: Normal. 1: Min value present when ATG_CALMD = 0, ATG_DATA_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
	ATG_UPG	1	Min value flag for G channel. 0: Normal. 1: Min value present when ATG_CALMD = 0, ATG_DATA_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
	ATG_UPB	0	Min value flag for B channel. 0: Normal. 1: Min value present when ATG_CALMD = 0, ATG_DATA_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
0Fh (2F1Eh)	REG2F1E	7:0	Default : 0x00	Access : R/W
	AUTO_COAST	7	Auto coast enable when mode change. 0: Disable.	

IP1_S Register (Bank = 2F, Sub-Bank = 03)

Index (Absolute)	Mnemonic	Bit	Description	
			1: Enable.	
	OP2_COAST	6	Coast status (Read only). 0: Coast is inactive. 1: Coast is active (free-run).	
	ATPSEL[1:0]	5:4	Auto phase value select (read from registers 0x8C~0x8F). 00: R/G/B total value. 01: Only R value. 10: Only G value. 11: Only B value.	
	PIP_SW_DOUBLE	3	Double sample for 1. VD, 2. Ext VD 656 format, 3. Ext 444 format. The purpose is to provide 2X pixel rate for FIR down sample, and give 11 TAP filter.	
	ATGSEL[2:0]	2:0	Select auto gain report for Reg. 7Dh. 000: Minimum R value. 001: Minimum G value. 010: Minimum G value. 011: Maximum R value. 100: Maximum G value. 101: Maximum B value. 11x: Reserved.	
10h (2F20h)	REG2F20	7:0	Default : 0x00	Access : RO, R/W
	JIT_R	7	Jitter function left/right result for 86h and 87h. 0: Left result. 1: Right result.	
	JIT_SWCLR_SB	6	Jitter software clear. 0: Not clear. 1: Clear.	
	-	5	Reserved.	
	JITTER_HISMD	4	Jitter function mode. 0: Update every frame. 1: Keep the history value.	
	JITTER	3	Jitter function result. 0: No jitter. 1: Jitter present.	
	ATS_HISMD	2	Auto position function mode.	

IP1_S Register (Bank = 2F, Sub-Bank = 03)

Index (Absolute)	Mnemonic	Bit	Description	
			0: Update every frame. 1: Keep the history value.	
	ATS_RDY	1	Auto position result ready. 0: Result ready. 1: Result not ready.	
	ATS_EN	0	Auto position function enable. 0: Disable. 1: Enable. Disable-to-enable needs at least 2 frame apart for ready bit to settle.	
10h (2F21h)	REG2F21	7:0	Default : 0x00	Access : R/W
	THOLD[3:0]	7:4	Auto position valid data value. 0000: Valid if data >= 0000 0000. 0001: Valid if data >= 0001 0000. 0010: Valid if data >= 0010 0000. & 1111: Valid if data >= 1111 0000.	
	-	3:1	Reserved.	
	ATS_PIXMD	0	Auto position force pixel mode. 0: DE or pixel decide by the source. 1: Force pixel mode.	
11h (2F22h)	REG2F22	7:0	Default : -	Access : RO
	ATGSEL_VALUE[7:0]	7:0	Auto gain value (selected by register 0Fh[2:0]).	
12h (2F24h)	REG2F24	7:0	Default : -	Access : RO
	ATS_VSTDBUF[7:0]	7:0	Auto position detected result vertical starting point.	
12h (2F25h)	REG2F25	7:0	Default : -	Access : RO
	-	7:3	Reserved.	
	ATS_VSTDBUF[10:8]	2:0	Please see description of '2F24h'.	
13h (2F26h)	REG2F26	7:0	Default : -	Access : RO
	ATS_HSTDBUF[7:0]	7:0	Auto position detected result horizontal starting point.	
13h (2F27h)	REG2F27	7:0	Default : -	Access : RO
	-	7:4	Reserved.	
	ATS_HSTDBUF[11:8]	3:0	Please see description of '2F26h'.	
14h (2F28h)	REG2F28	7:0	Default : -	Access : RO
	ATS_VEDDBUF[7:0]	7:0	Auto position detected result vertical end point.	

IP1_S Register (Bank = 2F, Sub-Bank = 03)

Index (Absolute)	Mnemonic	Bit	Description	
14h (2F29h)	REG2F29	7:0	Default : -	Access : RO
	-	7:3	Reserved.	
	ATS_VEDDBUF[10:8]	2:0	Please see description of '2F28h'.	
15h (2F2Ah)	REG2F2A	7:0	Default : -	Access : RO
	ATS_HEDDBUF[7:0]	7:0	Auto position detected result horizontal end point.	
15h (2F2Bh)	REG2F2B	7:0	Default : -	Access : RO
	-	7:4	Reserved.	
	ATS_HEDDBUF[11:8]	3:0	Please see description of '2F2Ah'.	
16h (2F2Ch)	REG2F2C	7:0	Default : -	Access : RO
	REG_JLST[7:0]	7:0	Jitter function detected left/right most point state (previous frame) depend on Reg_10h[7] (default = 7ffh).	
16h (2F2Dh)	REG2F2D	7:0	Default : -	Access : RO
	-	7:4	Reserved.	
	REG_JLST[11:8]	3:0	Please see description of '2F2Ch'.	
17h (2F2Eh)	REG2F2E	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	L12_LMT_EN	5	Background noise reduction enable. 0: Disable. 1: Enable.	
	HIPX_LMT_EN	4	High level noise reduction enable. 0: Disable. 1: Enable.	
	-	3	Reserved.	
	PIX_TH[2:0]	2:0	Auto noise level. 111: Noise level = 16.	
18h (2F30h)	REG2F30	7:0	Default : 0x01	Access : R/W
	ATP_GTH[7:0]	7:0	Auto phase gray scale threshold for ATP[23:16] when ATPN[31:24] = 0.	
18h (2F31h)	REG2F31	7:0	Default : 0x10	Access : R/W
	ATP_TH[7:0]	7:0	Auto phase text threshold for ATP[31:24] .	
19h (2F32h)	REG2F32	7:0	Default : 0x00	Access : RO, R/W
	-	7	Reserved.	
	ATP_GRY	6	Auto phase gray scale detect (Read Only).	
	ATP_TXT	5	Auto phase text detect (Read Only).	

IP1_S Register (Bank = 2F, Sub-Bank = 03)

Index (Absolute)	Mnemonic	Bit	Description	
	ATPMSK[2:0]	4:2	Auto phase nose mask. 000: Mask 0 bit, default value. 001: Mask 1 bit. 010: Mask 2 bit. 011: Mask 3 bit. 100: Mask 4 bit. 101: Mask 5 bit. 110: Mask 6 bit. 111: Mask 7 bit.	
	ATP_RDY	1	Auto phase result ready. 0: Result not ready. 1: Result ready.	
	ATP_EN	0	Auto phase function enable. 0: Disable. 1: Enable.	
1Ah (2F34h)	REG2F34	7:0	Default : 0x00	Access : R/W
	ATP[7:0]	7:0	Auto phase value.	
1Ah (2F35h)	REG2F35	7:0	Default : 0x00	Access : R/W
	ATP[15:8]	7:0	Please see description of '2F34h'.	
1Bh (2F36h)	REG2F36	7:0	Default : 0x00	Access : R/W
	ATP[23:16]	7:0	Please see description of '2F34h'.	
1Bh (2F37h)	REG2F37	7:0	Default : 0x00	Access : R/W
	ATP[31:24]	7:0	Please see description of '2F34h'.	
1Ch (2F38h)	REG2F38	7:0	Default : 0x00	Access : RO, R/W
	LB_TUNE_RDY	7	Input VSYNC blanking status. 0: In display. 1: In blanking.	
	DELAYLN_NUM[2:0]	6:4	Delay line after sample V start for input trigger point.	
	-	3:2	Reserved.	
	UNDERRUN	1	Under run status for FIFO.	
	OVERRUN	0	Over run status for FIFO.	
1Dh (2F3Ah)	REG2F3A	7:0	Default : 0x05	Access : R/W
	-	7	Reserved.	
	HSTOL[6:0]	6:0	HSYNC tolerance for mode change 5: Default value.	
1Dh	REG2F3B	7:0	Default : 0x01	Access : R/W

IP1_S Register (Bank = 2F, Sub-Bank = 03)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
(2F3Bh)	VDO_VEDGE	7	Interlace mode VSYNC reference edge.
	RAW_VSMD	6	Bypass mode raw VSYNC output from SYNC separator.
	HTT_FILTERMD	5	Auto no signal filter mode. 0: Disable. 1: Enable (update HTT after 4 sequential lines over tolerance).
	AUTO_NO_SIGNAL	4	Auto no signal enable. This will auto set current Bank 02[7] = 1 if mode change.
	VS_TOL[3:0]	3:0	VSYNC tolerance for mode change. 1: Default value.
1Eh (2F3Ch)	**REG2F3C**	**7:0**	**Default : 0x00** — **Access : RO, R/W**
	SOG_OFFMUX[1:0]	7:6	Off line SOG source select. 00: Select analog 1 SOG. 01: Select analog 2 SOG. 10: Select analog 3 SOG.
	IPHCS0_ACT	5	Analog 1 HSYNC pin active.
	IPHCS1_ACT	4	Analog 2 HSYNC pin active.
	IPHS_SB_S	3	Input normalized HSYNC pin monitor. Show input HSYNC pin directly (Active Low).
	IPVS_SB_S	2	Input normalized VSYNC pin monitor. Show input VSYNC pin directly (Active Low).
	OPHS	1	Output normalized HSYNC pin monitor. Show output HSYNC pin directly (Active Low).
	OPVS	0	Output normalized VSYNC pin monitor. Show output VSYNC pin directly (Active Low).
1Eh (2F3Dh)	**REG2F3D**	**7:0**	**Default : -** — **Access : RO**
	IPVS_ACT	7	Input on line source VSYNC active. 0: Not active. 1: Active.
	IPHS_ACT	6	Input on line source HSYNC active. 0: Not active. 1: Active.
	CS_DET	5	Composite sync detected status. 0: Input is not composite sync. 1: Input is detected as composite sync.
	SOG_DET	4	Sync-On-Green detected status.

IP1_S Register (Bank = 2F, Sub-Bank = 03)

Index (Absolute)	Mnemonic	Bit	Description	
			0: Input is not SOG. 1: Input is detected as SOG.	
	INTLAC_DET	3	Interlace/non-interlace detecting result by this chip. 0: Non-interlace. 1: Interlace.	
	FLD_DET	2	Input odd/even field detecting result by this chip. 0: Even. 1: Odd.	
	HSPOL	1	Input on line source HSYNC polarity detecting result by this chip. 0: Active low. 1: Active high.	
	VSPOL	0	Input on line source VSYNC polarity detecting result by this chip. 0: Active low. 1: Active high.	
1Fh (2F3Eh)	REG2F3E	7:0	Default : 0x00	Access : R/W
	VTT[7:0]	7:0	Input vertical total, count by HSYNC.	
1Fh (2F3Fh)	REG2F3F	7:0	Default : 0x00	Access : R/W
	VS_PW_VDOMD	7	VSYNC raw pulse width for measurement.	
	-	6	Reserved.	
	HSPW_SEL	5	VSYNC pulse width read enable. The report is shown in current Bank 22.	
	-	4:3	Reserved.	
	VTT[10:8]	2:0	Please see description of '2F3Eh'.	
20h (2F40h)	REG2F40	7:0	Default : 0x00	Access : R/W
	HTT_FOR_READ[7:0]	7:0	Input horizontal period, count by reference clock.	
20h (2F41h)	REG2F41	7:0	Default : 0x00	Access : R/W
	LN4_DETMD	7	Input HSYNC period detect mode. 0: 1 line. 1: 8 lines.	
	TEST_CSHTT	6	Report sync separator HTT by E5, E4. 0: HTT report by mode detector. 1: HTT report by sync separator.	
	HTT_FOR_READ[13:8]	5:0	Please see description of '2F40h'.	
21h	REG2F42	7:0	Default : 0x00	Access : R/W

IP1_S Register (Bank = 2F, Sub-Bank = 03)

Index (Absolute)	Mnemonic	Bit	Description	
(2F42h)	FLD_SWMD	7	Shift line method during field switch. 0: Old method. 1: New method.	
	COAST_HS_SEPMD	6	HSYNC in coast for data capture. 0: HSOUT (recommended). 1: Re-shaped HSYNC.	
	USR_VSPOL	5	User defined input VSYNC polarity, active when USR_VSPOLMD = 1. 0: Active low. 1: Active high.	
	USR_VSPOLMD	4	Input VSYNC polarity judgment. 0: Use result of internal circuit detection. 1: Defined by user (USR_VSPOL).	
	USR_HSPOL	3	User defined input HSYNC polarity, active when USR_HSPOLMD =1. 0: Active low. 1: Active high.	
	USR_HSPOLMD	2	Input HSYNC polarity judgment. 0: Use result of internal circuit detection. 1: Defined by user (USR_HSPOL).	
	USR_INTLAC	1	User defined non-interlace/interlace, active when USR_INTLACMD = 1. 0: Non-interlace. 1: Interlace.	
	USR_INTLACMD	0	Interlace judgment. 0: Use result of internal circuit detection. 1: Defined by user (USR_INTLAC).	
21h (2F43h)	REG2F43	7:0	Default : 0x00	Access : R/W
	MEMSYN_TO_VS[1:0]	7:6	Memory control switch method. 00: Sample V end. 01: Sample V start. 10: Sample V start ahead by current Bank 09[3:0]. 11: Sample V start ahead by current Bank 09[3:0] x 2.	
	DE_ONLY_HTT_CHGMD	5	DE only mode HTT change status mode. 0: Mode change provide in data clock domain. 1: Mode change provide in data clock and fix clock domain (Recommended).	
	DE_ONLY_HTT_SRC	4	DE only mode HTT report source.	

IP1_S Register (Bank = 2F, Sub-Bank = 03)

Index (Absolute)	Mnemonic	Bit	Description	
			0: Form input DE. 1: From re-generated DE.	
	ADC_VIDEO_FINV	3	Component video field inversion when ADC_VIDEO = 1 for data align. 0: Normal. 1: Invert.	
	EXT_FLDMD	2	Video external field. 0: Use result of internal circuit detection. 1: Use external field.	
	FLD_DETMD	1	Interlace field detect method select. 0: Use the HSYNC numbers of a field to judge. 1: Use the relationship of VSYNC and HSYNC to judge.	
	FLD_INV	0	Interlace field invert. 0: Normal. 1: Invert.	
22h (2F44h)	REG2F44	7:0	Default : -	Access : RO
	HSPW[7:0]	7:0	Pulse width report. If current Bank HSPW_SEL (1F[13]) = 0, report HSYNC. If current Bank HSPW_SEL (1F[13]) = 1, report VSYNC.	
23h (2F46h)	REG2F46	7:0	Default : 0x1E	Access : R/W
	DVICK_WIDTH[7:0]	7:0	DVI clock detection threshold, see CAh for usage (default 0x1E). CAh[6] = 0: DVI clock is OK, Freq(DVI) > Freq(XTAL) * 23h/128. CAh[6] = 1: DVI clock is missing, Freq(DVI) < Freq(XTAL) * 23h/128. Where EBh default to 0x1E(30).	
23h (2F47h)	REG2F47	7:0	Default : 0x00	Access : RO, R/W
	VD_FREE	7	Video in free-run mode (Read Only).	
	MIN_VTT[6:0]	6:0	Minimum VTT. When detected VTT < MIN_VTT[6:0] x 16, into the video interlace free-run mode.	
24h (2F48h)	REG2F48	7:0	Default : 0x00	Access : R/W
	VS_SEP_SEL	7	Sync separator VSYNC for mode detect. 0: Raw VSYNC (H/V relationship is kept for interlace detect). 1: HSYNC align VSYNC (H/V relationship is lost for	

IP1_S Register (Bank = 2F, Sub-Bank = 03)

Index (Absolute)	Mnemonic	Bit	Description	
			interlace detect).	
	VIDEO_D1L_H	6	Component video delay line. (VIDEO_D1L_H + VIDEO_D1L_L) = 00: Delay 1 line for another field. 01: Delay 2 line for another field. 10: Delay 3 line for another field. 11: Delay 4 line for another field.	
	ADC_VIDEO	5	ADC input select. 0: PC source. 1: Component video.	
	VIDEO_D1L_L	4	Component video delay line. (VIDEO_D1L_H + VIDEO_D1L_L) = 00: Delay 1 line for another field. 01: Delay 2 line for another field. 10: Delay 3 line for another field. 11: Delay 4 line for another field.	
	CS_CUT_MD	3	Composite SYNC cut mode (for testing). 0: Disable. 1: Enable.	
	EXTVS_SEPINV	2	External VSYNC polarity (only used when COAST_SRCS is 1). 0: Normal. 1: Invert.	
	COAST_SRC	1	Coast VSYNC select. 0: Internal separated VSYNC (Default). 1: External VSYNC (for testing).	
	COAST_POL	0	Coast polarity to PAD.	
24h (2F49h)	REG2F49	7:0	Default : 0x00	Access : R/W
	COAST_FBD[7:0]	7:0	Front tuning. 00: Coast start from 1 HSYNC leading edge. 01: Coast start from 2 HSYNC leading edge, default value. & 254: Coast start from 255 HSYNC leading edge. 255: Coast start from 256 HSYNC leading edge.	
25h (2F4Ah)	REG2F4A	7:0	Default : 0x00	Access : R/W
	COAST_BBD[7:0]	7:0	End tuning. 00: Coast end at 1 HSYNC leading edge. 01: Coast end at 2 HSYNC leading edge, default value.	

IP1_S Register (Bank = 2F, Sub-Bank = 03)

Index (Absolute)	Mnemonic	Bit	Description	
			& 254: Coast end at 255 HSYNC leading edge. 255: Coast end at 256 HSYNC leading edge.	
26h (2F4Ch)	REG2F4C	7:0	Default : 0x00	Access : R/W
	GR_DE_EN	7	DE or HSYNC post glitch removal function enable. 0: Disable. 1: Enable.	
	FILTER_NUM[2:0]	6:4	DE or HSYNC post glitch removal range. Analog: 000: 0 XTAL clock. 001: 1 XTAL clock. 010: 2 XTAL clock. 111: 7 XTAL clock. DVI: 000: 0x8 input clock. 001: 1x8 input clock. 010: 2x8 input clock. 111: 7x8 input clock.	
	GR_HS_VIDEO	3	Input HSYNC filter. When input source is analog: 0: Filter off. 1: Filter on. When input source is DVI: 0: Normal. 1: More tolerance for unstable DE.	
	GR_EN	2	Input sync sample mode. 0: Normal. 1: Glitch-removal.	
	HVTT_LOSE_MD	1	HTT/VTT lost mode for INT. 0: By counter overflow. 1: By counter overflow + active detect IPVS_ACT, IPHS_ACT (E1[7:6]) (Recommend).	
	IDCLK_INV	0	Capture port sample CLK invert. 0: Normal. 1: Invert.	
27h (2F4Eh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
29h	REG2F52	7:0	Default : 0x00	Access : RO, R/W

IP1_S Register (Bank = 2F, Sub-Bank = 03)

Index (Absolute)	Mnemonic	Bit	Description	
(2F52h)	VS_SEP_SEL_1	7	New interlace detect method by big and small line counts for a field.	
	VS_SEP_SEL_0	6	Hardware auto VSYNC start line method select.	
	INTLAC_DET_MD[1:0]	5:4	Interlace detect mode. 00: Off. 01: Only for line total number is even. 10: All case. 11: Off.	
	EUP_AU_HDTV_DET	3	Europe/Australia 1080i HDTV detect.	
	EUP_HDTV_DET	2	Europe 1080i HDTV detect.	
	EUP_AUTOFLD	1	EUR/AUS 1080i HDTV auto field mode.	
	EUP_HDTV	0	EUR/AUS 1080i HDTV force field mode.	
29h (2F53h)	REG2F53	7:0	Default : 0x00	Access : RO, R/W
	LCK2LCK_RPT[3:0]	7:4	Check lock to lock line count for interlace auto-correct.	
	-	3:1	Reserved.	
	ATRANGE_EN	0	Auto range enable 0: Define automatically. 1: Define by current Bank 2A-2B.	
2Ah (2F54h)	REG2F54	7:0	Default : 0x00	Access : R/W
	ATRANGE_VST[7:0]	7:0	Auto function (position, gain phase) vertical start point, count by input HSYNC.	
2Ah (2F55h)	REG2F55	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	ATRANGE_VST[10:8]	2:0	Please see description of '2F54h'.	
2Bh (2F56h)	REG2F56	7:0	Default : 0x00	Access : R/W
	ATRANGE_HST[7:0]	7:0	Auto function (position, gain phase) horizontal start point, count by input dot clock.	
2Bh (2F57h)	REG2F57	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	ATRANGE_HST[10:8]	2:0	Please see description of '2F56h'.	
2Ch (2F58h)	REG2F58	7:0	Default : 0x00	Access : R/W
	ATRANGE_VDC[7:0]	7:0	Auto function (position, gain phase) vertical resolution, count by input HSYNC.	
2Ch (2F59h)	REG2F59	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	

IP1_S Register (Bank = 2F, Sub-Bank = 03)

Index (Absolute)	Mnemonic	Bit	Description	
	ATRANGE_VDC[10:8]	2:0	Please see description of '2F58h'.	
2Dh (2F5Ah)	REG2F5A	7:0	Default : 0x00	Access : R/W
	ATRANGE_HDC[7:0]	7:0	Auto Function (position, gain phase) horizontal resolution, count by input dot clock.	
2Dh (2F5Bh)	REG2F5B	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	ATRANGE_HDC[10:8]	2:0	Please see description of '2F5Ah'.	
2Eh (2F5Ch)	REG2F5C	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	GOP_CLK_FREE	1	GOP clock gating enable. 0: Can gate the GOP clock. 1: Don't gate the GOP clock.	
	IP2_CLK_GATE_EN	0	IP2 clock gating enable. 0: Don't gate the IDCLK. 1: Can gate the IDCLK.	
30h (2F60h)	REG2F60	7:0	Default : 0x00	Access : R/W
	INSERT_NUM[7:0]	7:0	VSYNC insert number offset.	
30h (2F61h)	REG2F61	7:0	Default : 0x00	Access : R/W
	INSERT_SEL	7	VSYNC insert number offset enable.	
	-	6:3	Reserved.	
	INSERT_NUM[10:8]	2:0	Please see description of '2F60h'.	
31h (2F62h)	REG2F62	7:0	Default : 0x00	Access : R/W
	LCK_NUM[7:0]	7:0	VSYNC lock number offset.	
31h (2F63h)	REG2F63	7:0	Default : 0x00	Access : R/W
	LCK_SEL	7	VSYNC lock number offset enable.	
	-	6:3	Reserved.	
	LCK_NUM[10:8]	2:0	Please see description of '2F62h'.	
32h (2F64h)	REG2F64	7:0	Default : 0x00	Access : R/W
	VLCK[7:0]	7:0	V-lock.	
32h (2F65h)	REG2F65	7:0	Default : 0x00	Access : R/W
	VLCK[15:8]	7:0	Please see description of '2F64h'.	

IP2_S Register (Bank = 2F, Sub-Bank = 04)

IP2_S Register (Bank = 2F, Sub-Bank = 04)				
Index (Absolute)	Mnemonic	Bit	Description	
01h (2F02h)	REG2F02	7:0	Default : 0x00	Access : R/W
	VFAC_SHT	7	VSD factor shift enable.	
	VFAC_SHT_INV	6	VSD field inverse.	
	IP2_F422EN	5	Force IP 442 format enable.	
	IP2_F422	4	0: IP 444. 1: IP 422.	
	-	3:2	Reserved.	
	VSD_DITHEN	1	VSD dither function enable.	
	HSD_DITHEN	0	HSD dither function enable.	
02h (2F04h)	REG2F04	7:0	Default : 0x00	Access : R/W
	HFAC_SET_IP[7:0]	7:0	HSD initial factor.	
02h (2F05h)	REG2F05	7:0	Default : 0x00	Access : R/W
	HFAC_SET_IP[15:8]	7:0	Please see description of '2F04h'.	
03h (2F06h)	REG2F06	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	HFAC_SET_IP[19:16]	3:0	Please see description of '2F04h'.	
04h (2F08h)	REG2F08	7:0	Default : 0x00	Access : R/W
	HFACIN0[7:0]	7:0	HSD factor, format [3.20].	
04h (2F09h)	REG2F09	7:0	Default : 0x00	Access : R/W
	HFACIN0[15:8]	7:0	Please see description of '2F08h'.	
05h (2F0Ah)	REG2F0A	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	HFACIN1[22:16]	6:0	HSD factor, format [3.20].	
05h (2F0Bh)	REG2F0B	7:0	Default : 0x00	Access : R/W
	IP2HSDEN	7	H scaling-down enable.	
	PREHSDMD	6	0: Accumulator mode, FAC = OUT/IN (format [0.20]). 1: 6TapY/4TapC filter mode, FAC = IN/OUT (format [3.20]).	
	-	5:0	Reserved.	
06h (2F0Ch)	REG2F0C	7:0	Default : 0x00	Access : R/W
	VFAC_SET_IP[7:0]	7:0	VSD initial factor.	
06h	REG2F0D	7:0	Default : 0x00	Access : R/W

IP2_S Register (Bank = 2F, Sub-Bank = 04)

Index (Absolute)	Mnemonic	Bit	Description	
(2F0Dh)	VFAC_SET_IP[15:8]	7:0	Please see description of '2F0Ch'.	
07h (2F0Eh)	REG2F0E	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	VFAC_SET_IP[19:16]	3:0	Please see description of '2F0Ch'.	
08h (2F10h)	REG2F10	7:0	Default : 0x00	Access : R/W
	VFACIN0[7:0]	7:0	VSD factor, format [0.20].	
08h (2F11h)	REG2F11	7:0	Default : 0x00	Access : R/W
	VFACIN0[15:8]	7:0	Please see description of '2F10h'.	
09h (2F12h)	REG2F12	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	VFACIN1[19:16]	3:0	VSD factor, format [0.20].	
09h (2F13h)	REG2F13	7:0	Default : 0x00	Access : R/W
	PRE_VDOWN	7	V scaling-down enable.	
	-	6:0	Reserved.	
0Ah (2F14h)	REG2F14	7:0	Default : 0x00	Access : R/W
	C_FILTER[2:0]	7:5	444 to 422 filter.	
	YDELAY_EN	4	Y delay enable.	
	YCDELAY_STEP[3:0]	3:0	Y/C delay pipe step.	
16h (2F2Ch)	REG2F2C	7:0	Default : 0xF2	Access : R/W
	HSD_YT0_C0[7:0]	7:0	Up-sample 1st pix (oxxx) coef. Y0. Format: S7. of 2's complement (-31 <= Y0 <= 31)	
17h (2F2Eh)	REG2F2E	7:0	Default : 0x1F	Access : R/W
	HSD_YT0_C1[7:0]	7:0	Up-sample 1st pix (oxxx) coef. Y1 Format: S7. of 2's complement (-63 <= Y1 <= 63).	
18h (2F30h)	REG2F30	7:0	Default : 0x5E	Access : R/W
	HSD_YT0_C2[7:0]	7:0	Up-sample 1st pix (oxxx) coef. Y2. Format: fix 8. (0 <= Y2 <= 255).	
19h (2F32h)	REG2F32	7:0	Default : 0xF4	Access : R/W
	HSD_YT1_C0[7:0]	7:0	Up-sample 2nd pix (xoxx) coef. Y0. Format: S7. of 2's complement (-31 <= Y0 <= 31).	
1Ah (2F34h)	REG2F34	7:0	Default : 0x0C	Access : R/W
	HSD_YT1_C1[7:0]	7:0	Up-sample 2nd pix (xoxx) coef. Y1. Format: S7. of 2's complement (-63 <= Y1 <= 63).	
1Bh	REG2F36	7:0	Default : 0x5A	Access : R/W

IP2_S Register (Bank = 2F, Sub-Bank = 04)

Index (Absolute)	Mnemonic	Bit	Description	
(2F36h)	HSD_YT1_C2[7:0]	7:0	Up-sample 2nd pix (xoxx) coef. Y2. Format: fix 8.(0 <= Y2 <= 255).	
1Ch (2F38h)	REG2F38	7:0	Default : 0x37	Access : R/W
	HSD_YT1_C3[7:0]	7:0	Up-sample 2nd pix (xoxx) coef. Y3. Format: fix 8.(0 <= Y3 <= 255).	
1Dh (2F3Ah)	REG2F3A	7:0	Default : 0xF5	Access : R/W
	HSD_YT1_C4[7:0]	7:0	Up-sample 2nd pix (xoxx) coef. Y4. Format: S7. of 2's complement (-63 <= Y4 <= + 63).	
1Eh (2F3Ch)	REG2F3C	7:0	Default : 0xFA	Access : R/W
	HSD_YT1_C5[7:0]	7:0	Up-sample 2nd pix (xoxx) coef. Y5. Format: S7. of 2's complement (-31 < Y5 <= 31).	
1Fh (2F3Eh)	REG2F3E	7:0	Default : 0xF7	Access : R/W
	HSD_YT2_C0[7:0]	7:0	Up-sample 3rd pix (xxox) coef. Y0. Format: S7. of 2's complemen (-15 <= Y0 <= 15).	
20h (2F40h)	REG2F40	7:0	Default : 0xFE	Access : R/W
	HSD_YT2_C1[7:0]	7:0	Up-sample 3rd pix (xxox) coef. Y1. Format: S7. of 2's complement (-63 <= Y1 <= 63).	
21h (2F42h)	REG2F42	7:0	Default : 0x4B	Access : R/W
	HSD_YT2_C2[7:0]	7:0	Up-sample 3rd pix (xxox) coef. Y2. Format: fix 8.(0 <= Y2 <= 127).	
2Ch (2F58h)	REG2F58	7:0	Default : 0x44	Access : R/W
	-	7	Reserved.	
	CTI_STEP[2:0]	6:4	CTI filter step.	
	-	3	Reserved.	
	CTI_LPF_COEF[2:0]	2:0	CTI low-pass filter coefficient.	
2Ch (2F59h)	REG2F59	7:0	Default : 0x3F	Access : R/W
	-	7:6	Reserved.	
	CTI_BAND_COEF[5:0]	5:0	CTI band-pass filter coefficient.	
2Dh (2F5Ah)	REG2F5A	7:0	Default : 0x88	Access : R/W
	CTI_MEDIAN_EN	7	CTI median filter enable.	
	-	6:4	Reserved.	
	CTI_CORING_THRD[3:0]	3:0	CTI coring threshold.	
2Dh (2F5Bh)	REG2F5B	7:0	Default : 0x00	Access : R/W
	CTI_EN	7	CTI enable.	

IP2_S Register (Bank = 2F, Sub-Bank = 04)

Index (Absolute)	Mnemonic	Bit	Description
	-	6:4	Reserved.
	CTI_AUTO_NO_MED	3	CTI auto-turn-off median mode.
	-	2:0	Reserved.

OPM Register (Bank = 2F, Sub-Bank = 05)

Index (Absolute)	Mnemonic	Bit	Description	
01h (2F02h)	REG2F02	7:0	Default : 0x00	Access : R/W
	RATIOYC_FB1[1:0]	7:6	Sub window motion ratio.	
	RATIODIV_MD_F1[2:0]	5:3	Sub window ratio divider.	
	RATIO_MD_F1[2:0]	2:0	Sub window motion ratio mode.	
03h (2F06h)	REG2F06	7:0	Default : 0x02	Access : R/W
	FD_MOT_CNTTH_F1[7:0]	7:0	Sub window field detect field threshold.	
03h (2F07h)	REG2F07	7:0	Default : 0x00	Access : R/W
	FD_MOT_CNTTH_9_8_F1[1:0]	7:6	Sub window field detect field threshold.	
	-	5	Reserved.	
	ZZ_MADI_MD_F1	4	Sub window ZR MODi mode. 0: Disable. 1: Enable.	
	F22_BOUNDARYMD_F1	3	MW field detect boundary mode.	
	ZIG_ZAG_DETMD_F1[2:0]	2:0	Zigzag detect mode.	
04h (2F09h)	REG2F09	7:0	Default : 0x00	Access : R/W
	F32_LCKMD_F1[7:0]	7:0	Sub window Film 32 lock mode.	
05h (2F0Ah)	REG2F0A	7:0	Default : 0x00	Access : R/W
	F22_LCKMD_F1[7:0]	7:0	Sub window Film 22 lock mode.	
06h (2F0Ch)	REG2F0C	7:0	Default : 0x00	Access : R/W
	BASE_ADDR_F1_1[7:0]	7:0	Sub window MIU base address 0.	
06h (2F0Dh)	REG2F0D	7:0	Default : 0x00	Access : R/W
	BASE_ADDR_F1_1[15:8]	7:0	Please see description of '2F0Ch'.	
07h (2F0Eh)	REG2F0E	7:0	Default : 0x00	Access : R/W
	BASE_ADDR_F1_1[23:16]	7:0	Please see description of '2F0Ch'.	
08h	REG2F10	7:0	Default : 0x00	Access : R/W

OPM Register (Bank = 2F, Sub-Bank = 05)

Index (Absolute)	Mnemonic	Bit	Description	
(2F10h)	BASE_ADDR_F1_2[7:0]	7:0	Sub window MIU base address 1.	
08h (2F11h)	REG2F11	7:0	Default : 0x00	Access : R/W
	BASE_ADDR_F1_2[15:8]	7:0	Please see description of '2F10h'.	
09h (2F12h)	REG2F12	7:0	Default : 0x00	Access : R/W
	BASE_ADDR_F1_2[23:16]	7:0	Please see description of '2F10h'.	
10h (2F20h)	REG2F20	7:0	Default : 0x00	Access : R/W
	OFFSET_F1[7:0]	7:0	Sub widow MIU offset (pixel units).	
10h (2F21h)	REG2F21	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	OFFSET_F1[11:8]	3:0	Please see description of '2F20h'.	
11h (2F22h)	REG2F22	7:0	Default : 0x10	Access : R/W
	FETCH_NUM_F1[7:0]	7:0	Sub widow MIU fetch number (pixel units).	
11h (2F23h)	REG2F23	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	FETCH_NUM_F1[11:8]	3:0	Please see description of '2F22h'.	
13h (2F26h)	REG2F26	7:0	Default : 0x00	Access : R/W
	FRAME4_TOGGLE_F1	7	Sub window force 4 frames when progressive.	
	PNR_ENY_F1	6	Sub window post noise reduction for Y.	
	PNR_ENC_F1	5	Sub window post noise reduction for C.	
	PCNR_EN_F1	4	Sub window post CNR enable.	
	-	3:1	Reserved.	
	PRE_32_F1	0	Sub window film 32 detect. 0: Post 32. 1: Pre 32.	
15h (2F2Ah)	REG2F2A	7:0	Default : 0x00	Access : R/W
	Y_CBR_MUX_F1[2:0]	7:5	Sub window YCbCr mux.	
	-	4:2	Reserved.	
	POS_CCS_EN_F1	1	Sub window POS CCS enable.	
	POS_CCS_FLT_F1	0	Sub window POS CCS filter.	
15h (2F2Bh)	REG2F2B	7:0	Default : 0x00	Access : R/W
	CCS_LUT_TH_F1[7:0]	7:0	Sub window CCS look up table threshold.	
16h (2F2Ch)	REG2F2C	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	

OPM Register (Bank = 2F, Sub-Bank = 05)

Index (Absolute)	Mnemonic	Bit	Description	
	NOR_DIFF_WEIGHT_F1[5:0]	5:0	Sub window difference weighting.	
16h (2F2Dh)	REG2F2D	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	NOR_DIFF_CNR_RAW_WEIGHT_F1[5:0]	5:0	Sub window difference weighting.	
17h (2F2Eh)	REG2F2E	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	NOR_DIFF_Y_CNR_WEIGHT_F1[5:0]	5:0	Sub window difference weighting.	
18h (2F30h)	REG2F30	7:0	Default : 0x00	Access : R/W
	Y_CBR_MUX_HMD_F1[2:0]	7:5	Sub window YCbCr mux.	
	-	4:3	Reserved.	
	PNR_IIR_RESETZ_F1_DFT	2	Sub window PNR reset signal.	
	POS_HMD_EN_F1	1	Sub window POS HMD enable.	
	POS_HMD_FLT_F1	0	Sub window POS HMD filter.	
18h (2F31h)	REG2F31	7:0	Default : 0x00	Access : R/W
	HMD_LUT_TH_F1[7:0]	7:0	Sub window HMD look up table threshold.	
19h (2F32h)	REG2F32	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	NOR_DIFFC_WEIGHT_F1[5:0]	5:0	Sub window difference weighting.	
19h (2F33h)	REG2F33	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	NOR_DIFF_HMD_RAW_WT_F1[5:0]	5:0	Sub window C motion difference weighting for HMD.	
1Ah (2F34h)	REG2F34	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	NOR_DIFF_C_HMD_WT_F1[5:0]	5:0	Sub window Y raw difference weighting for HMD.	
1Bh (2F36h)	REG2F36	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	PNR_FORCE_DISABLE_F1	2	Sub window PNR force disable.	
	PNR_RATIOC_F100_F1	1	Current C value completely taken from pre-pixel when ratio=4'hf when blending in sub window.	
	PNR_RATIOY_F100_F1	0	Current Y value completely taken from pre-pixel when	

OPM Register (Bank = 2F, Sub-Bank = 05)

Index (Absolute)	Mnemonic	Bit	Description	
			ratio=4'hf when blending in sub window.	
1Bh (2F37h)	REG2F37	7:0	Default : -	Access : RO
	MOT_CNTH_STS_F1[7:0]	7:0	Sub window motion count status.	
1Ch (2F38h)	REG2F38	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	FILM_BLENDING_MD_F1	1	Sub window film mode blending mode.	
	EN_FILM_BLENDING_F1	0	Sub window film mode blending enable.	
1Ch (2F39h)	REG2F39	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	NR_TH2C_F1[2:0]	6:4	Sub window NR threshold for C.	
	NR_TH2Y_F1[3:0]	3:0	Sub window NR threshold for Y.	
1Dh (2F3Ah)	REG2F3A	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	SW_FILM32_CNT_F1[2:0]	6:4	Sub window film 32 count SW setting.	
	-	3:2	Reserved.	
	SW_FILM32_ACT_F1	1	Sub window film 32 active SW setting.	
	-	0	Reserved.	
1Dh (2F3Bh)	REG2F3B	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	SW_FILM22_CNT_F1[1:0]	5:4	Sub window film 22 count SW setting.	
	-	3:2	Reserved.	
	SW_FILM22_ACT_F1	1	Sub window film 22 active SW setting.	
	-	0	Reserved.	
1Fh (2F3Eh)	REG2F3E	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	LBI_W_OFFSET_EN_F2	5	Main window image shift enable.	
	LBI_W_OFFSET_EN_F1	4	Sub window image shift enable.	
	LBI_W_OFFSET	3:0	The pixel number of image shifts.	
23h (2F46h)	REG2F46	7:0	Default : 0x02	Access : R/W
	FD_MOT_CNTTH_F2_0[7:0]	7:0	Main window field detect field threshold.	
23h (2F47h)	REG2F47	7:0	Default : 0x00	Access : R/W
	FD_MOT_CNTTH_F2_1[1:0]	7:6	Main window field detect field threshold.	
	-	5	Reserved.	

OPM Register (Bank = 2F, Sub-Bank = 05)

Index (Absolute)	Mnemonic	Bit	Description	
	ZZ_MADI_MD_F2	4	Main window ZR MODi mode. 0: Disable. 1: Enable.	
	F22_BOUNDARYMD_F2	3	Main window MW field detect boundary mode.	
	ZIG_ZAG_DETMD_F2[2:0]	2:0	Main window zigzag detect mode.	
24h (2F49h)	REG2F49	7:0	Default : 0x00	Access : R/W
	F32_LCKMD_F2[7:0]	7:0	Main window film 32 lock mode.	
25h (2F4Ah)	REG2F4A	7:0	Default : 0x00	Access : R/W
	F22_LCKMD_F2[7:0]	7:0	Main window film 22 lock mode.	
25h (2F4Bh)	REG2F4B	7:0	Default : 0x00	Access : R/W
	RATIOYC_FB2[1:0]	7:6	Main window motion ratio.	
	RATIODIV_MD_F2[2:0]	5:3	Main window ratio divider.	
	RATIO_MD_F2[2:0]	2:0	Main window motion ratio mode.	
26h (2F4Ch)	REG2F4C	7:0	Default : 0x00	Access : R/W
	BASE_ADDR_F2_1[7:0]	7:0	Main window MIU base address 0.	
26h (2F4Dh)	REG2F4D	7:0	Default : 0x00	Access : R/W
	BASE_ADDR_F2_1[15:8]	7:0	Please see description of '2F4Ch'.	
27h (2F4Eh)	REG2F4E	7:0	Default : 0x00	Access : R/W
	BASE_ADDR_F2_1[23:16]	7:0	Please see description of '2F4Ch'.	
28h (2F50h)	REG2F50	7:0	Default : 0x00	Access : R/W
	BASE_ADDR_F2_2[7:0]	7:0	Main window MIU base address 1.	
28h (2F51h)	REG2F51	7:0	Default : 0x00	Access : R/W
	BASE_ADDR_F2_2[15:8]	7:0	Please see description of '2F50h'.	
29h (2F52h)	REG2F52	7:0	Default : 0x00	Access : R/W
	BASE_ADDR_F2_2[23:16]	7:0	Please see description of '2F50h'.	
2Ah (2F54h)	REG2F54	7:0	Default : 0x00	Access : R/W
	OFFSET_F2[7:0]	7:0	Main window MIU offset (pixel units).	
2Ah (2F55h)	REG2F55	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	OFFSET_F2[11:8]	3:0	Please see description of '2F54h'.	
2Bh (2F56h)	REG2F56	7:0	Default : 0x10	Access : R/W
	FETCH_NUM_F2[7:0]	7:0	Sub window MIU fetch number (pixel units).	
2Bh	REG2F57	7:0	Default : 0x00	Access : R/W

OPM Register (Bank = 2F, Sub-Bank = 05)

Index (Absolute)	Mnemonic	Bit	Description	
(2F57h)	-	7:4	Reserved.	
	FETCH_NUM_F2[11:8]	3:0	Please see description of '2F56h'.	
30h (2F60h)	REG2F60	7:0	Default : 0x00	Access : R/W
	REG_MODE6_CHANGE_OFF_F1	7	Sub window de-pack mode6 with y ration enable.	
	R_OPM_2READ_EN_F1	6	Sub window 2-read mode enable.	
	REG_OPM_REDUCE_C_F1	5	Sub window reduce mode enable.	
	R_OPM_M_MD_USER_EN_F1	4	Sub window user defined frame buffer mode enable.	
	R_OPM_M_MD_USER_F1[3:0]	3:0	Sub window Frame Buffer Mode.	
30h (2F61h)	REG2F61	7:0	Default : 0x00	Access : R/W
	REG_MODE6_CHANGE_OFF_F2	7	Main window de-pack mode6 with y ration enable.	
	R_OPM_2READ_EN_F2	6	Main window 2-read mode enable.	
	REG_OPM_REDUCE_C_F2	5	Main window reduce mode enable.	
	R_OPM_M_MD_USER_EN_F2	4	Main window user defined frame buffer mode enable.	
	R_OPM_M_MD_USER_F2[3:0]	3:0	Main window frame buffer mode.	
31h (2F62h)	REG2F62	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	R_OPM_PON_SEL_NOC_INVERT	4	3: Field 2-read mode NOC_SEL signal invert enable.	
	R_OPM_CUR_OR_NEXT_SEL_F1	3	Sub window 3-field current and pre-pixel exchange.	
	R_OPM_4F_2READ_MIU_RATION_EN_F1	2	Sub window 4-field 2-read mode ratio read from MIU enable.	
	R_OPM_MEMRBANK_OFST_F1[1:0]	1:0	Sub window memory-read-bank offset.	
31h (2F63h)	REG2F63	7:0	Default : 0x00	Access : R/W
	R_OPM_PON_SEL_2READ_F2	7	Main window 3-field 2-read mode dotted line cycle read present or next field select.	
	R_FILM_HIGH_PRI_F2	6	Main window 3-field 2-read mode NOC_SEL signal high priority enable.	
	R_OPM_PON_SEL_2READ_F1	5	Sub window 3-field 2-read mode dotted line cycle read present or next field select.	
	R_FILM_HIGH_PRI_F1	4	Sub window 3-field 2-read mode NOC_SEL signal high priority enable.	

OPM Register (Bank = 2F, Sub-Bank = 05)

Index (Absolute)	Mnemonic	Bit	Description	
	R_OPM_CUR_OR_NEXT_SEL_F2	3	Main window 3-field current and pre-pixel exchange.	
	R_OPM_4F_2READ_MIU_RATION_EN_F2	2	Main window 4-field 2-read mode ratio read from MIU enable.	
	R_OPM_MEMRBANK_OFFSET_F2[1:0]	1:0	Main window memory-read-bank offset.	
33h (2F66h)	REG2F66	7:0	Default : 0x00	Access : R/W
	FRAME4_TOGGLE_F2	7	Main window force 4 frames when progressive.	
	PNR_ENY_F2	6	Main window post noise reduction for Y.	
	PNR_ENC_F2	5	Main window post noise reduction for C.	
	PCNR_EN_F2	4	Main window post CNR enable.	
	-	3:1	Reserved.	
	PRE_32_F2	0	Main window film 32 detect. 0: Post 32. 1: Pre 32.	
35h (2F6Ah)	REG2F6A	7:0	Default : 0x00	Access : R/W
	Y_CBR_MUX_F2[2:0]	7:5	Main window YCbCr mux.	
	-	4:2	Reserved.	
	POS_CCS_EN_F2	1	Main window POS CCS enable.	
	POS_CCS_FLT_F2	0	Main window POS CCS filter.	
35h (2F6Bh)	REG2F6B	7:0	Default : 0x00	Access : R/W
	CCS_LUT_TH_F2[7:0]	7:0	Main window CCS look up table threshold.	
36h (2F6Ch)	REG2F6C	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	NOR_DIFF_WT_F2[5:0]	5:0	Main window difference weighting.	
36h (2F6Dh)	REG2F6D	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	NOR_DIFF_CNR_RAW_WT_F2[5:0]	5:0	Main window difference weighting.	
37h (2F6Eh)	REG2F6E	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	NOR_DIFF_Y_CNR_WT_F2[5:0]	5:0	Main window difference weighting.	
38h	REG2F70	7:0	Default : 0x00	Access : R/W

OPM Register (Bank = 2F, Sub-Bank = 05)				
Index (Absolute)	Mnemonic	Bit	Description	
(2F70h)	Y_CBR_MUX_HMD_F2[2:0]	7:5	Main window YCbCr mux.	
	-	4:3	Reserved.	
	PNR_IIR_RESETZ_F2_DFT	2	Main window PNR reset signal.	
	POS_HMD_EN_F2	1	Main window POS HMD enable.	
	POS_HMD_FLT_F2	0	Main window POS HMD filter.	
38h (2F71h)	REG2F71	7:0	Default : 0x00	Access : R/W
	HMD_LUT_TH_F2[7:0]	7:0	Main window HMD look up table threshold.	
39h (2F72h)	REG2F72	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	NOR_DIFFC_WT_F2[5:0]	5:0	Main window difference weighting.	
39h (2F73h)	REG2F73	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	NOR_DIFF_HMD_RAW_WT_F2[5:0]	5:0	Main window difference weighting.	
3Ah (2F74h)	REG2F74	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	NOR_DIFF_C_HMD_WT_F2[5:0]	5:0	Main window difference weighting.	
3Bh (2F76h)	REG2F76	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	PNR_FORCE_DISABLE_F2	2	Main window PNR force disable.	
	PNR_RATIOC_F100_F2	1	Current C value completely taken from pre-pixel when ratio=4'hf when blending in main window.	
	PNR_RATIOY_F100_F2	0	Current Y value completely taken from pre-pixel when ratio=4'hf when blending in main window.	
3Bh (2F77h)	REG2F77	7:0	Default : -	Access : RO
	MOT_CNTH_STS_F2[7:0]	7:0	Main window motion count status.	
3Ch (2F78h)	REG2F78	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	FILM_BLENDING_MD_F2	1	Main window film mode blending mode.	
	EN_FILM_BLENDING_F2	0	Main window Film mode blending enable.	
3Ch (2F79h)	REG2F79	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	NR_TH2C_F2[2:0]	6:4	Main window NR threshold for C.	

OPM Register (Bank = 2F, Sub-Bank = 05)

Index (Absolute)	Mnemonic	Bit	Description	
	NR_TH2Y_F2[3:0]	3:0	Main window NR threshold for Y.	
3Dh (2F7Ah)	REG2F7A	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	SW_FILM32_CNT_F2[2:0]	6:4	Main window film 32 count SW setting.	
	-	3:2	Reserved.	
	SW_FILM32_ACT_F2	1	Main window film 32 active SW setting.	
	-	0	Reserved.	
3Dh (2F7Bh)	REG2F7B	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	SW_FILM22_CNT_F2[1:0]	5:4	Main window film 22 count SW setting.	
	-	3:2	Reserved.	
	SW_FILM22_ACT_F2	1	Main window film 22 active SW setting.	
	-	0	Reserved.	
41h (2F82h)	REG2F82	7:0	Default : 0x02	Access : R/W
	-	7:2	Reserved.	
	MEMBK_FB_SEL	1	Bank select (main or sub window R/W bank).	
	-	0	Reserved.	
41h (2F83h)	REG2F83	7:0	Default : -	Access : RO
	MEMBK_REG[7:0]	7:0	Bank information.	
48h (2F90h)	REG2F90	7:0	Default : 0x00	Access : R/W
	F32_FASTMD	7	Film 32 fast-enter mode.	
	F32_SETBACK	6	Option for film 32 backward to previous version. 0: New algorithm. 1: Old algorithm.	
	-	5	Reserved.	
	F32_STATE_CNT[4:0]	4:0	Film 32 low to low count.	
48h (2F91h)	REG2F91	7:0	Default : 0x00	Access : R/W
	F22_FASTMD	7	Film 22 fast-enter mode.	
	F22_SETBACK	6	Option for film 32 backward to previous version. 0: New algorithm. 1: Old algorithm.	
	F22_WITH_FLDMD	5	F22 with field mode.	
	F22_WITH_FLDMD_INV	4	F22 with field mode invert.	
	-	3:0	Reserved.	

OPM Register (Bank = 2F, Sub-Bank = 05)

Index (Absolute)	Mnemonic	Bit	Description	
49h (2F92h)	REG2F92	7:0	Default : 0x00	Access : R/W
	TDDI_ADDCTRL[7:0]	7:0	C 3DDi parameter.	
49h (2F93h)	REG2F93	7:0	Default : 0x00	Access : R/W
	TDDI_CTRLBUS[3:0]	7:4	3DDi control.	
	TDDI_FMFLT[1:0]	3:2	3DDi frame mode filter.	
	TDDI_FMMD	1	3DDi frame mode.	
	TDDI_EDGEMD	0	3DDi edge mode.	
4Ah (2F94h)	REG2F94	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	MOTION_TH3[2:0]	6:4	3DDi motion threshold for F mode.	
	FM_3DDI_PIXTH[3:0]	3:0	3DDi F pixel threshold.	
4Ah (2F95h)	REG2F95	7:0	Default : 0x00	Access : R/W
	FM_3DDI_THA[7:0]	7:0	3DDi FM threshold A.	
4Bh (2F96h)	REG2F96	7:0	Default : 0x00	Access : R/W
	FM_3DDI_THB[7:0]	7:0	3DDi FM threshold B.	
4Bh (2F97h)	REG2F97	7:0	Default : 0x00	Access : R/W
	FM_3DDI_THC[7:0]	7:0	3DDi FM threshold C.	
4Ch (2F98h)	REG2F98	7:0	Default : 0x00	Access : R/W
	FM_DIVB[3:0]	7:4	3DDi FM DIV B.	
	FM_DIVA[3:0]	3:0	3DDi FM DIV A.	
4Ch (2F99h)	REG2F99	7:0	Default : 0x00	Access : R/W
	FM_DIVD[3:0]	7:4	3DDi FM DIV D.	
	FM_DIVC[3:0]	3:0	3DDi FM DIV C.	
4Dh (2F9Ah)	REG2F9A	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	OFST_MD	3	Offset mode.	
	-	2:0	Reserved.	
4Eh (2F9Ch)	REG2F9C	7:0	Default : 0x00	Access : R/W
	KS_BASE_ADDR[7:0]	7:0	Key stone base address.	
4Eh (2F9Dh)	REG2F9D	7:0	Default : 0x00	Access : R/W
	KS_BASE_ADDR[15:8]	7:0	Please see description of '2F9Ch'.	
4Fh (2F9Eh)	REG2F9E	7:0	Default : 0x01	Access : R/W
	KS_BASE_ADDR[23:16]	7:0	Please see description of '2F9Ch'.	

OPM Register (Bank = 2F, Sub-Bank = 05)

Index (Absolute)	Mnemonic	Bit	Description	
50h (2FA0h)	REG2FA0	7:0	Default : 0x10	Access : R/W
	KS_FETCH_NUM[7:0]	7:0	Key stone fetch number.	
50h (2FA1h)	REG2FA1	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	KST_BANDWITH	0	Indicate bandwidth.	
51h (2FA2h)	REG2FA2	7:0	Default : 0x10	Access : R/W
	EXPIRE_THD[7:0]	7:0	Maximum fetch number threshold of each request.	
51h (2FA3h)	REG2FA3	7:0	Default : 0x10	Access : R/W
	PRIORITY_THD[7:0]	7:0	MIU request priority threshold.	
52h (2FA4h)	REG2FA4	7:0	Default : 0x18	Access : R/W
	REQ_THD[7:0]	7:0	Threshold of start to access MIU.	
52h (2FA5h)	REG2FA5	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	SET_RBANK[2:0]	6:4	Read memory bank number for main window and sub window	
	FORCE_RBANK_F2	3	Force main window read memory bank.	
	FORCE_RBANK_F1	2	Force sub window read memory bank.	
	FLD_INV_F2	1	Main window field invert for memory.	
	FLD_INV_F1	0	Sub window field invert for memory.	
54h (2FA8h)	REG2FA8	7:0	Default : 0x02	Access : R/W
	UV_IIR_MD[1:0]	7:6	PNR CCS UV IIR mode.	
	Y_IIR_MD[1:0]	5:4	PNR CCS Y IIR mode.	
	-	3	Reserved.	
	QUALIFY_DISABLE	2	PNR force disable when low.	
	BURST_LENGTH[1:0]	1:0	Burst length of OPM request to MIU.	
58h (2FB0h)	REG2FB0	7:0	Default : 0x00	Access : R/W
	PNR_TABLECCS[7:0]	7:0	PNR CCS table.	
58h (2FB1h)	REG2FB1	7:0	Default : 0x00	Access : R/W
	PNR_TABLECCS[15:8]	7:0	Please see description of '2FB0h'.	
59h (2FB2h)	REG2FB2	7:0	Default : 0x00	Access : R/W
	PNR_TABLECCS[23:16]	7:0	Please see description of '2FB0h'.	
59h (2FB3h)	REG2FB3	7:0	Default : 0x00	Access : R/W
	PNR_TABLECCS[31:24]	7:0	Please see description of '2FB0h'.	

OPM Register (Bank = 2F, Sub-Bank = 05)

Index (Absolute)	Mnemonic	Bit	Description	
5Ah (2FB4h)	REG2FB4	7:0	Default : 0x00	Access : R/W
	PNR_TABLECCS[39:32]	7:0	Please see description of '2FB0h'.	
5Ah (2FB5h)	REG2FB5	7:0	Default : 0x00	Access : R/W
	PNR_TABLECCS[47:40]	7:0	Please see description of '2FB0h'.	
5Bh (2FB6h)	REG2FB6	7:0	Default : 0x00	Access : R/W
	PNR_TABLECCS[55:48]	7:0	Please see description of '2FB0h'.	
5Bh (2FB7h)	REG2FB7	7:0	Default : 0x00	Access : R/W
	PNR_TABLECCS[63:56]	7:0	Please see description of '2FB0h'.	
5Ch (2FB8h)	REG2FB8	7:0	Default : 0x00	Access : R/W
	PNR_TABLECCS[71:64]	7:0	Please see description of '2FB0h'.	
5Ch (2FB9h)	REG2FB9	7:0	Default : 0x00	Access : R/W
	PNR_TABLECCS[79:72]	7:0	Please see description of '2FB0h'.	
5Dh (2FBAh)	REG2FBA	7:0	Default : 0x00	Access : R/W
	PNR_TABLECCS[87:80]	7:0	Please see description of '2FB0h'.	
5Dh (2FBBh)	REG2FBB	7:0	Default : 0x00	Access : R/W
	PNR_TABLECCS[95:88]	7:0	Please see description of '2FB0h'.	
5Eh (2FBCh)	REG2FBC	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	PNR_TABLECCS[99:96]	3:0	Please see description of '2FB0h'.	
60h (2FC0h)	REG2FC0	7:0	Default : 0x00	Access : R/W
	PNR_TABLEC[7:0]	7:0	PNR table C.	
60h (2FC1h)	REG2FC1	7:0	Default : 0x00	Access : R/W
	PNR_TABLEC[15:8]	7:0	Please see description of '2FC0h'.	
61h (2FC2h)	REG2FC2	7:0	Default : 0x00	Access : R/W
	PNR_TABLEC[23:16]	7:0	Please see description of '2FC0h'.	
61h (2FC3h)	REG2FC3	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	PNR_TABLEC[27:24]	3:0	Please see description of '2FC0h'.	
62h (2FC4h)	REG2FC4	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	UV_IIR_MD_HMD[1:0]	3:2	PNR HMD UV IIR mode.	
	Y_IIR_MD_HMD[1:0]	1:0	PNR HMD Y IIR mode.	
66h	REG2FCC	7:0	Default : 0x00	Access : R/W

OPM Register (Bank = 2F, Sub-Bank = 05)

Index (Absolute)	Mnemonic	Bit	Description	
(2FCCh)	PNR_TABLEHMD[7:0]	7:0	PNR HMD table.	
66h (2FCDh)	REG2FCD	7:0	Default : 0x00	Access : R/W
	PNR_TABLEHMD[15:8]	7:0	Please see description of '2FCCh'.	
67h (2FCEh)	REG2FCE	7:0	Default : 0x00	Access : R/W
	PNR_TABLEHMD[23:16]	7:0	Please see description of '2FCCh'.	
67h (2FCFh)	REG2FCF	7:0	Default : 0x00	Access : R/W
	PNR_TABLEHMD[31:24]	7:0	Please see description of '2FCCh'.	
68h (2FD0h)	REG2FD0	7:0	Default : 0x00	Access : R/W
	PNR_TABLEHMD[39:32]	7:0	Please see description of '2FCCh'.	
68h (2FD1h)	REG2FD1	7:0	Default : 0x00	Access : R/W
	PNR_TABLEHMD[47:40]	7:0	Please see description of '2FCCh'.	
69h (2FD2h)	REG2FD2	7:0	Default : 0x00	Access : R/W
	PNR_TABLEHMD[55:48]	7:0	Please see description of '2FCCh'.	
69h (2FD3h)	REG2FD3	7:0	Default : 0x00	Access : R/W
	PNR_TABLEHMD[63:56]	7:0	Please see description of '2FCCh'.	
6Ah (2FD4h)	REG2FD4	7:0	Default : 0x00	Access : R/W
	PNR_TABLEHMD[71:64]	7:0	Please see description of '2FCCh'.	
6Ah (2FD5h)	REG2FD5	7:0	Default : 0x00	Access : R/W
	PNR_TABLEHMD[79:72]	7:0	Please see description of '2FCCh'.	
6Bh (2FD6h)	REG2FD6	7:0	Default : 0x00	Access : R/W
	PNR_TABLEHMD[87:80]	7:0	Please see description of '2FCCh'.	
6Bh (2FD7h)	REG2FD7	7:0	Default : 0x00	Access : R/W
	PNR_TABLEHMD[95:88]	7:0	Please see description of '2FCCh'.	
6Ch (2FD8h)	REG2FD8	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	PNR_TABLEHMD[99:96]	3:0	Please see description of '2FCCh'.	
6Dh (2FDAh)	REG2FDA	7:0	Default : 0x00	Access : R/W
	PNR_TABLEY[7:0]	7:0	PNR table Y.	
6Dh (2FDBh)	REG2FDB	7:0	Default : 0x00	Access : R/W
	PNR_TABLEY[15:8]	7:0	Please see description of '2FDAh'.	
6Eh (2FDCh)	REG2FDC	7:0	Default : 0x00	Access : R/W
	PNR_TABLEY[23:16]	7:0	Please see description of '2FDAh'.	
6Eh	REG2FDD	7:0	Default : 0x00	Access : R/W

OPM Register (Bank = 2F, Sub-Bank = 05)

Index (Absolute)	Mnemonic	Bit	Description	
(2FDDh)	-	7:4	Reserved.	
	PNR_TABLEY[27:24]	3:0	Please see description of '2FDAh'.	
70h (2FE0h)	REG2FE0	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	EN_FILM32CNT_FRONT	2	Refer to film 32 detection result of DNR.	
	EN_LOCALMIN_FUN	1	Use local-min method for un-match determination.	
	EN_GAIN_HP_FUN	0	Use weighted motion ratio for film mode detection.	
71h (2FE2h)	REG2FE2	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	FILML2L[4:0]	4:0	Period of film-lock to film-lock.	
71h (2FE3h)	REG2FE3	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	FILMMTCNT[3:0]	3:0	Film 32 count threshold in lock.	
72h (2FE4h)	REG2FE4	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	EN_SW_FILM22	1	Enable software film 22.	
	EN_SW_FILM32	0	Enable software film 32.	
73h (2FE6h)	REG2FE6	7:0	Default : 0x00	Access : R/W
	FILM_RATIOB_TH[7:0]	7:0	Ratio B threshold for film mode.	
74h (2FE8h)	REG2FE8	7:0	Default : -	Access : RO
	-	7:5	Reserved.	
	MIN_NUM_RECORD[4:0]	4:0	Minimum data counts record in FIFO.	
75h ~ 76h (2FEAh ~ 2FEDh)	-	7:0	Default : 0x00	Access : R/W
	-	7:0	Reserved.	
77h (2FEEh)	REG2FEE	7:0	Default : 0x00	Access : R/W
	3DDI_RATIO_TABLE[7:0]	7:0	3DDi ratio table.	
77h (2FEFh)	REG2FEF	7:0	Default : 0x00	Access : R/W
	3DDI_RATIO_TABLE[15:8]	7:0	Please see description of '2FEEh'.	
78h (2FF0h)	REG2FF0	7:0	Default : 0x00	Access : R/W
	3DDI_RATIO_TABLE[23:16]	7:0	Please see description of '2FEEh'.	
78h (2FF1h)	REG2FF1	7:0	Default : 0x00	Access : R/W
	3DDI_RATIO_TABLE[31:24]	7:0	Please see description of '2FEEh'.	

OPM Register (Bank = 2F, Sub-Bank = 05)

Index (Absolute)	Mnemonic	Bit	Description	
79h (2FF2h)	REG2FF2	7:0	Default : 0x00	Access : R/W
	3DDI_RATIO_TABLE[39:32]	7:0	Please see description of '2FEEh'.	
79h (2FF3h)	REG2FF3	7:0	Default : 0x00	Access : R/W
	3DDI_RATIO_TABLE[47:40]	7:0	Please see description of '2FEEh'.	
7Ah (2FF4h)	REG2FF4	7:0	Default : 0x00	Access : R/W
	3DDI_RATIO_TABLE[55:48]	7:0	Please see description of '2FEEh'.	
7Ah (2FF5h)	REG2FF5	7:0	Default : 0x00	Access : R/W
	3DDI_RATIO_TABLE[63:56]	7:0	Please see description of '2FEEh'.	
7Bh (2FF6h)	REG2FF6	7:0	Default : 0x00	Access : R/W
	3DDI_RATIO_TABLE[71:64]	7:0	Please see description of '2FEEh'.	
7Bh (2FF7h)	REG2FF7	7:0	Default : 0x00	Access : R/W
	3DDI_RATIO_TABLE[79:72]	7:0	Please see description of '2FEEh'.	
7Ch (2FF8h)	REG2FF8	7:0	Default : 0x00	Access : R/W
	3DDI_RATIO_TABLE[87:80]	7:0	Please see description of '2FEEh'.	
7Ch (2FF9h)	REG2FF9	7:0	Default : 0x00	Access : R/W
	3DDI_RATIO_TABLE[95:88]	7:0	Please see description of '2FEEh'.	
7Dh (2FFAh)	REG2FFA	7:0	Default : 0x00	Access : R/W
	3DDI_RATIO_TABLE[103:96]	7:0	Please see description of '2FEEh'.	
7Dh (2FFBh)	REG2FFB	7:0	Default : 0x00	Access : R/W
	3DDI_RATIO_TABLE[111:104]	7:0	Please see description of '2FEEh'.	
7Eh (2FFCh)	REG2FFC	7:0	Default : 0x00	Access : R/W
	3DDI_RATIO_TABLE[119:112]	7:0	Please see description of '2FEEh'.	
7Eh (2FFDh)	REG2FFD	7:0	Default : 0x00	Access : R/W
	3DDI_RATIO_TABLE[127:120]	7:0	Please see description of '2FEEh'.	
7Fh (2FFEh)	REG2FFE	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	EN_3DDI_RATIO_TABLE	0	Enable use 3DDi ratio table.	

DNR Register (Bank = 2F, Sub-Bank = 06)

DNR Register (Bank = 2F, Sub-Bank = 06)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
01h (2F02h)	REG2F02	7:0	Default : 0x02	Access : R/W
	FM_MOT_CNTTH_F1[7:0]	7:0	F1 frame detect frame threshold.
01h (2F03h)	REG2F03	7:0	Default : 0x00	Access : R/W
	PRE_NR8_FORCE	7	F1 force pre-NR8 enable.
	MOTION_TH1_F1[2:0]	6:4	F1 motion threshold for normal case.
	STILLMD_F1	3	F1 freeze image.
	DIMD_FB1_REG[2:0]	2:0	F1 de-interface mode.
02h (2F04h)	REG2F04	7:0	Default : 0x00	Access : R/W
	DNREG_BASE0_F1[7:0]	7:0	F1 frame buffer base address 0.
02h (2F05h)	REG2F05	7:0	Default : 0x00	Access : R/W
	DNREG_BASE0_F1[15:8]	7:0	Please see description of '2F04h'.
03h (2F06h)	REG2F06	7:0	Default : 0x00	Access : R/W
	DNREG_BASE0_F1[23:16]	7:0	Please see description of '2F04h'.
03h (2F07h)	REG2F07	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.
	DNR_M_MD_USER_EN_F1	4	F1 user-defined memory arrangement mode enable.
	DNR_M_MD_USER_F1[3:0]	3:0	F1 user-defined memory arrangement mode.
04h (2F08h)	REG2F08	7:0	Default : 0x00	Access : R/W
	DNREG_BASE1_F1[7:0]	7:0	F1 frame buffer base address 1.
04h (2F09h)	REG2F09	7:0	Default : 0x00	Access : R/W
	DNREG_BASE1_F1[15:8]	7:0	Please see description of '2F08h'.
05h (2F0Ah)	REG2F0A	7:0	Default : 0x00	Access : R/W
	DNREG_BASE1_F1[23:16]	7:0	Please see description of '2F08h'.
06h (2F0Ch)	REG2F0C	7:0	Default : 0x00	Access : R/W
	DNREG_OFFSET_F1[7:0]	7:0	F1 frame buffer line offset (pixel unit).
06h (2F0Dh)	REG2F0D	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.
	DNREG_OFST_F1[11:8]	3:0	Please see description of '2F0Ch'.
07h (2F0Eh)	REG2F0E	7:0	Default : 0x10	Access : R/W
	DNREG_FET_NUM_F1[7:0]	7:0	F1 fetch pixel number of one line.
07h	REG2F0F	7:0	Default : 0x00	Access : R/W

DNR Register (Bank = 2F, Sub-Bank = 06)

Index (Absolute)	Mnemonic	Bit	Description	
(2F0Fh)	-	7:4	Reserved.	
	DNREG_FET_NUM_F1[11:8]	3:0	Please see description of '2F0Eh'.	
08h (2F10h)	**REG2F10**	**7:0**	**Default : 0x00**	Access : R/W
	DNREG_VCNT_LMT_F1[7:0]	7:0	F1 MIU line count limit for FB write.	
08h (2F11h)	**REG2F11**	**7:0**	**Default : 0x00**	Access : R/W
	-	7:5	Reserved.	
	DNREG_VCNT_LMT_EN_F1	4	F1 MIU write limit enable.	
	DNREG_VCNT_LMT_F1[11:8]	3:0	Please see description of '2F10h'.	
09h (2F12h)	**REG2F12**	**7:0**	**Default : 0x10**	Access : R/W
	DNREG_REG_THRD_F1[7:0]	7:0	F1 FIFO threshold for read request.	
09h (2F13h)	**REG2F13**	**7:0**	**Default : 0x14**	Access : R/W
	DNREG_REG_HPRI_F1[7:0]	7:0	F1 high priority threshold for read request.	
0Ah (2F14h)	**REG2F14**	**7:0**	**Default : 0x10**	Access : R/W
	DNREG_W_THRD_F1[7:0]	7:0	F1 FIFO threshold for write request.	
0Ah (2F15h)	**REG2F15**	**7:0**	**Default : 0x14**	Access : R/W
	DNREG_W_HPRI_F1[7:0]	7:0	F1 high priority threshold for write request.	
0Bh (2F16h)	**REG2F16**	**7:0**	**Default : 0x00**	Access : R/W
	DNREG_EDGECMD_F1	7	F1 DNR C edge mode.	
	DNREG_FORCE_DISABLE_F1	6	F1 Force DNR function disable.	
	-	5:4	Reserved.	
	DNREG_PRECIIREG_EN_F1	3	F1 previous C IIR enable.	
	DNREG_CIIREG_EN_F1	2	F1 Current C IIR enable.	
	DNREG_PREYIIREG_EN_F1	1	F1 previous Y IIR enable.	
	DNREG_YIIREG_EN_F1	0	F1 Current Y IIR enable.	
0Bh (2F17h)	**REG2F17**	**7:0**	**Default : 0x00**	Access : R/W
	CCS_F1	7	F1 CCS enable.	
	MADI_EDGEMD_F1	6	F1 MADi edge mode.	
	DNREG_OLD_HMD_F1	5	F1 use old HMD method.	
	PRE_HMD_EN_F1	4	F1 previous HMD enable.	
	PRE_HMD_FLT_F1	3	F1 previous HMD filter select.	
	DNREG_OLD_CCS_F1	2	F1 use old CCS method.	
	PRE_CCS_EN_F1	1	F1 previous CCS enable.	
	PRE_CCS_FLT_F1	0	F1 previous CCS filter select.	

DNR Register (Bank = 2F, Sub-Bank = 06)

Index (Absolute)	Mnemonic	Bit	Description	
0Ch (2F18h)	REG2F18	7:0	Default : 0x00	Access : R/W
	TDDI_SEPC_FB1	7	F1 3DDi C motion TH separate with Y.	
	MOTION_THC_FB1[2:0]	6:4	F1 C motion threshold.	
	-	3	Reserved.	
	MOTION_TH2_F1[2:0]	2:0	F1 Y motion threshold.	
0Ch (2F19h)	REG2F19	7:0	Default : 0x00	Access : R/W
	FORCE_PRENREG_FB1	7	F1 Force Pre NR for no MADi mode.	
	FORCE10BIT_FB1	6	F1 Force 10bits data mode.	
	FLD_AVG_EN_FB1	5	Field average mode for 3 alpha and 4 alpha/beta.	
	NREG_EN_F1	4	F1 NR enable.	
	-	3	Reserved.	
	DNREG_EN_F1	2	F1 Dynamic NR enable.	
	-	1:0	Reserved.	
0Dh (2F1Ah)	REG2F1A	7:0	Default : 0x02	Access : R/W
	FILM32_EN_F1	7	F1 Film 32 mode detect enable.	
	FILM22_EN_F1	6	F1 Film 22 mode detect enable.	
	-	5:4	Reserved.	
	FD_MOT_PIXTH_SEL_F1[1:0]	3:2	F1 Frame motion pixel threshold select.	
	FM_MOT_PIXTH_SEL_F1[1:0]	1:0	F1 Frame motion pixel threshold select.	
0Dh (2F1Bh)	REG2F1B	7:0	Default : -	Access : RO
	-	7:6	Reserved.	
	FILM32_ACT_F1	5	F1 Film32 active flag.	
	FILM22_ACT_F1	4	F1 Film22 active flag.	
	-	3:0	Reserved.	
0Eh (2F1Ch)	REG2F1C	7:0	Default : 0xA0	Access : R/W
	W_LENGTH_SEL_F1[1:0]	7:6	F1 write request number unit.	
	REG_LENGTH_SEL_F1[1:0]	5:4	F1 read request number unit.	
	-	3:2	Reserved.	
	DNREG_CNT_CLREG_F1	1	F1 MIU status registers clear.	
	DNREG_WREQ_OFF_F1	0	F1 write request disable.	
0Fh (2F1Eh)	REG2F1E	7:0	Default : 0x10	Access : R/W
	DNREG_REG_THRD1_F1[7:0]	7:0	F1 read request max number.	
0Fh	REG2F1F	7:0	Default : 0x10	Access : R/W

DNR Register (Bank = 2F, Sub-Bank = 06)

Index (Absolute)	Mnemonic	Bit	Description	
(2F1Fh)	DNREG_W_THRD1_F1[7:0]	7:0	F1 write request max number.	
11h (2F22h)	REG2F22	7:0	Default : 0x02	Access : R/W
	FM_MOT_CNTTH_F2[7:0]	7:0	F2 frame detect frame threshold.	
11h (2F23h)	REG2F23	7:0	Default : 0x00	Access : R/W
	PRE_NR8_FORCE_F2	7	F2 force pre-NR8 enable.	
	MOTION_TH1_F2[2:0]	6:4	F2 motion threshold for normal case.	
	STILLMD_F2	3	F2 freeze image.	
	DIMD_FB2_REG[2:0]	2:0	F2 de-interface mode.	
12h (2F24h)	REG2F24	7:0	Default : 0x00	Access : R/W
	DNR_BASE0_F2[7:0]	7:0	F2 frame buffer base address 0.	
12h (2F25h)	REG2F25	7:0	Default : 0x00	Access : R/W
	DNR_BASE0_F2[15:8]	7:0	Please see description of '2F24h'.	
13h (2F26h)	REG2F26	7:0	Default : 0x00	Access : R/W
	DNR_BASE0_F2[23:16]	7:0	Please see description of '2F24h'.	
13h (2F27h)	REG2F27	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	DNR_RBANK_MAP[1:0]	6:5	Rbank map select for 3-field mode.	
	DNR_M_MD_USER_EN_F2	4	F2 user-defined memory arrangement mode enable.	
	DNR_M_MD_USER_F2[3:0]	3:0	F2 user-defined memory arrangement mode.	
14h (2F28h)	REG2F28	7:0	Default : 0x00	Access : R/W
	DNR_BASE1_F2[7:0]	7:0	F2 frame buffer base address 1.	
14h (2F29h)	REG2F29	7:0	Default : 0x00	Access : R/W
	DNR_BASE1_F2[15:8]	7:0	Please see description of '2F28h'.	
15h (2F2Ah)	REG2F2A	7:0	Default : 0x00	Access : R/W
	DNR_BASE1_F2[23:16]	7:0	Please see description of '2F28h'.	
16h (2F2Ch)	REG2F2C	7:0	Default : 0x00	Access : R/W
	DNR_OFFSET_F2[7:0]	7:0	F2 frame buffer line offset (pixel unit).	
16h (2F2Dh)	REG2F2D	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	DNR_OFFSET_F2[11:8]	3:0	Please see description of '2F2Ch'.	
17h (2F2Eh)	REG2F2E	7:0	Default : 0x10	Access : R/W
	DNR_FET_NUM_F2[7:0]	7:0	F2 fetch pixel number of one line.	
17h	REG2F2F	7:0	Default : 0x00	Access : R/W

DNR Register (Bank = 2F, Sub-Bank = 06)

Index (Absolute)	Mnemonic	Bit	Description	
(2F2Fh)	-	7:4	Reserved.	
	DNR_FET_NUM_F2[11:8]	3:0	Please see description of '2F2Eh'.	
18h (2F30h)	REG2F30	7:0	Default : 0x00	Access : R/W
	DNR_VCNT_LMT_F2[7:0]	7:0	F2 MIU line count limit for FB write.	
18h (2F31h)	REG2F31	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	DNR_VCNT_LMT_EN_F2	4	F2 MIU write limit enable.	
	DNR_VCNT_LMT_F2[11:8]	3:0	Please see description of '2F30h'.	
19h (2F32h)	REG2F32	7:0	Default : 0x10	Access : R/W
	DNR_R_THRD_F2[7:0]	7:0	F2 FIFO threshold for read request.	
19h (2F33h)	REG2F33	7:0	Default : 0x14	Access : R/W
	DNR_R_HPRI_F2[7:0]	7:0	F2 high priority threshold for read request.	
1Ah (2F34h)	REG2F34	7:0	Default : 0x10	Access : R/W
	DNR_W_THRD_F2[7:0]	7:0	F2 FIFO threshold for write request.	
1Ah (2F35h)	REG2F35	7:0	Default : 0x14	Access : R/W
	DNR_W_HPRI_F2[7:0]	7:0	F2 high priority threshold for write request.	
1Bh (2F36h)	REG2F36	7:0	Default : 0x00	Access : R/W
	DNR_EDGECMD_F2	7	F2 DNR C edge mode.	
	DNR_FORCE_DISABLE_F2	6	F2 Force DNR function disable.	
	-	5:4	Reserved.	
	DNR_PRECIIR_EN_F2	3	F2 previous C IIR enable.	
	DNR_CIIR_EN_F2	2	F2 Current C IIR enable.	
	DNR_PREYIIR_EN_F2	1	F2 previous Y IIR enable.	
	DNR_YIIR_EN_F2	0	F2 Current Y IIR enable.	
1Bh (2F37h)	REG2F37	7:0	Default : 0x00	Access : R/W
	CCS_F2	7	F2 CCS enable.	
	MADI_EDGEMD_F2	6	F2 MADi edge mode.	
	DNR_OLD_HMD_F2	5	F2 use old HMD method.	
	PRE_HMD_EN_F2	4	F2 previous HMD enable.	
	PRE_HMD_FLT_F2	3	F2 previous HMD filter select.	
	DNR_OLD_CCS_F2	2	F2 use old CCS method.	
	PRE_CCS_EN_F2	1	F2 previous CCS enable.	
	PRE_CCS_FLT_F2	0	F2 previous CCS filter select.	

DNR Register (Bank = 2F, Sub-Bank = 06)

Index (Absolute)	Mnemonic	Bit	Description	
1Ch (2F39h)	REG2F39	7:0	Default : 0x00	Access : R/W
	FORCE_PRENREG_FB2	7	F2 Force Pre NR for no MADi mode.	
	FORCE10BIT_FB2	6	F2 Force 10bits data mode.	
	FLD_AVG_EN_FB2	5	Field average mode for 3 alpha and 4 alpha/beta.	
	NREG_EN_F2	4	F2 NR enable.	
	-	3:0	Reserved.	
1Dh (2F3Ah)	REG2F3A	7:0	Default : 0x02	Access : R/W
	FILM32_EN_F2	7	F2 Film 32 mode detect enable.	
	FILM22_EN_F2	6	F2 Film 22 mode detect enable.	
	-	5:4	Reserved.	
	FD_MOT_PIXTH_F2_SEL[1:0]	3:2	F2 frame motion pixel threshold select.	
	FM_MOT_PIXTH_F2_SEL[1:0]	1:0	F2 Frame motion pixel threshold select.	
1Dh (2F3Bh)	REG2F3B	7:0	Default : -	Access : RO
	-	7:6	Reserved.	
	FILM32_ACT_F2	5	F2 Film32 active flag.	
	FILM22_ACT_F2	4	F2 Film22 active flag.	
	-	3:0	Reserved.	
1Eh (2F3Ch)	REG2F3C	7:0	Default : 0xA0	Access : R/W
	W_LENGTH_SEL_F2[1:0]	7:6	F2 write request number unit.	
	LENGTH_SEL_F2[1:0]	5:4	F2 read request number unit.	
	-	3:2	Reserved.	
	DNREG_CNT_CLREG_F2	1	F2 MIU status registers clear.	
	DNREG_WREQ_OFF_F2	0	F2 write request disable.	
1Fh (2F3Eh)	REG2F3E	7:0	Default : 0x10	Access : R/W
	DNREG_REG_THRD1_F2[7:0]	7:0	F2 read request max number.	
1Fh (2F3Fh)	REG2F3F	7:0	Default : 0x10	Access : R/W
	DNR_W_THRD1_F2[7:0]	7:0	F2 write request max number.	
20h (2F40h)	REG2F40	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	DNR_IIR_PREY_ALPHA[2:0]	6:4	Previous Y & IIR Y blending weighting.	
	-	3	Reserved.	
	DNR_IIR_Y_ALPHA[2:0]	2:0	Current Y & IIR Y blending weighting.	
20h	REG2F41	7:0	Default : 0x00	Access : R/W

DNR Register (Bank = 2F, Sub-Bank = 06)					
Index (Absolute)	**Mnemonic**	**Bit**	**Description**		
(2F41h)	-	7	Reserved.		
	DNR_IIR_PREC_ALPHA[2:0]	6:4	Previous C & IIR C blending weighting.		
	-	3	Reserved.		
	DNR_IIR_C_ALPHA[2:0]	2:0	Current C & IIR C blending weighting.		
21h (2F42h)	REG2F42	7:0	Default : 0x00		Access : R/W
	DNR_TABLE_YIIR_0[7:0]	7:0	Current Y IIR table.		
21h (2F43h)	REG2F43	7:0	Default : 0x00		Access : R/W
	DNR_TABLE_YIIR_0[15:8]	7:0	Please see description of '2F42h'.		
22h (2F44h)	REG2F44	7:0	Default : 0x00		Access : R/W
	DNR_TABLE_YIIR_1[7:0]	7:0	Current Y IIR table.		
22h (2F45h)	REG2F45	7:0	Default : 0x00		Access : R/W
	DNR_TABLE_YIIR_1[15:8]	7:0	Please see description of '2F44h'.		
23h (2F46h)	REG2F46	7:0	Default : 0x00		Access : R/W
	DNR_TABLE_YIIR_2[7:0]	7:0	Current Y IIR table.		
23h (2F47h)	REG2F47	7:0	Default : 0x00		Access : R/W
	DNR_TABLE_YIIR_2[15:8]	7:0	Please see description of '2F46h'.		
24h (2F48h)	REG2F48	7:0	Default : 0x00		Access : R/W
	DNR_TABLE_YIIR_3[7:0]	7:0	Current Y IIR table.		
24h (2F49h)	REG2F49	7:0	Default : 0x00		Access : R/W
	DNR_TABLE_YIIR_3[15:8]	7:0	Please see description of '2F48h'.		
25h (2F4Ah)	REG2F4A	7:0	Default : 0x00		Access : R/W
	-	7:4	Reserved.		
	DNR_TABLE_YIIR_4[3:0]	3:0	Current Y IIR table.		
26h (2F4Ch)	REG2F4C	7:0	Default : 0x00		Access : R/W
	DNR_TABLE_PREYIIR_0[7:0]	7:0	Previous Y IIR table.		
26h (2F4Dh)	REG2F4D	7:0	Default : 0x00		Access : R/W
	DNR_TABLE_PREYIIR_0[15:8]	7:0	Please see description of '2F4Ch'.		
27h (2F4Eh)	REG2F4E	7:0	Default : 0x00		Access : R/W
	DNR_TABLE_PREYIIR_1[7:0]	7:0	Previous Y IIR table.		
27h (2F4Fh)	REG2F4F	7:0	Default : 0x00		Access : R/W
	DNR_TABLE_PREYIIR_1[15:8]	7:0	Please see description of '2F4Eh'.		
28h (2F50h)	REG2F50	7:0	Default : 0x00		Access : R/W
	DNR_TABLE_PREYIIR_2[7:0]	7:0	Previous Y IIR table.		

DNR Register (Bank = 2F, Sub-Bank = 06)

Index (Absolute)	Mnemonic	Bit	Description	
28h (2F51h)	REG2F51	7:0	Default : 0x00	Access : R/W
	DNR_TABLE_PREYIIR_2[15:8]	7:0	Please see description of '2F50h'.	
29h (2F52h)	REG2F52	7:0	Default : 0x00	Access : R/W
	DNR_TABLE_PREYIIR_3[7:0]	7:0	Previous Y IIR table.	
29h (2F53h)	REG2F53	7:0	Default : 0x00	Access : R/W
	DNR_TABLE_PREYIIR_3[15:8]	7:0	Please see description of '2F52h'.	
2Ah (2F54h)	REG2F54	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	DNR_TABLE_PREYIIR_4[3:0]	3:0	Previous Y IIR table.	
2Bh (2F56h)	REG2F56	7:0	Default : 0x00	Access : R/W
	DNR_TABLE_CIIR_0[7:0]	7:0	Current C IIR table.	
2Bh (2F57h)	REG2F57	7:0	Default : 0x00	Access : R/W
	DNR_TABLE_CIIR_0[15:8]	7:0	Please see description of '2F56h'.	
2Ch (2F58h)	REG2F58	7:0	Default : 0x00	Access : R/W
	DNR_TABLE_CIIR_1[7:0]	7:0	Current C IIR table.	
2Ch (2F59h)	REG2F59	7:0	Default : 0x00	Access : R/W
	DNR_TABLE_CIIR_1[15:8]	7:0	Please see description of '2F58h'.	
2Dh (2F5Ah)	REG2F5A	7:0	Default : 0x00	Access : R/W
	DNR_TABLE_CIIR_2[7:0]	7:0	Current C IIR table.	
2Dh (2F5Bh)	REG2F5B	7:0	Default : 0x00	Access : R/W
	DNR_TABLE_CIIR_2[15:8]	7:0	Please see description of '2F5Ah'.	
2Eh (2F5Ch)	REG2F5C	7:0	Default : 0x00	Access : R/W
	DNR_TABLE_CIIR_3[7:0]	7:0	Current C IIR table.	
2Eh (2F5Dh)	REG2F5D	7:0	Default : 0x00	Access : R/W
	DNR_TABLE_CIIR_3[15:8]	7:0	Please see description of '2F5Ch'.	
2Fh (2F5Eh)	REG2F5E	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	DNR_TABLE_CIIR_4[3:0]	3:0	Current C IIR table.	
30h (2F60h)	REG2F60	7:0	Default : 0x00	Access : R/W
	DNR_TABLE_PRECIIR_0[7:0]	7:0	Previous C IIR table.	
30h (2F61h)	REG2F61	7:0	Default : 0x00	Access : R/W
	DNR_TABLE_PRECIIR_0[15:8]	7:0	Please see description of '2F60h'.	
31h	REG2F62	7:0	Default : 0x00	Access : R/W

DNR Register (Bank = 2F, Sub-Bank = 06)

Index (Absolute)	Mnemonic	Bit	Description	
(2F62h)	DNR_TABLE_PRECIIR_1[7:0]	7:0	Previous C IIR table.	
31h (2F63h)	REG2F63	7:0	Default : 0x00	Access : R/W
	DNR_TABLE_PRECIIR_1[15:8]	7:0	Please see description of '2F62h'.	
32h (2F64h)	REG2F64	7:0	Default : 0x00	Access : R/W
	DNR_TABLE_PRECIIR_2[7:0]	7:0	Previous C IIR table.	
32h (2F65h)	REG2F65	7:0	Default : 0x00	Access : R/W
	DNR_TABLE_PRECIIR_2[15:8]	7:0	Please see description of '2F64h'.	
33h (2F66h)	REG2F66	7:0	Default : 0x00	Access : R/W
	DNR_TABLE_PRECIIR_3[7:0]	7:0	Previous C IIR table.	
33h (2F67h)	REG2F67	7:0	Default : 0x00	Access : R/W
	DNR_TABLE_PRECIIR_3[15:8]	7:0	Please see description of '2F66h'.	
34h (2F68h)	REG2F68	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	DNR_TABLE_PRECIIR_4[3:0]	3:0	Previous C IIR table.	
35h (2F6Ah)	REG2F6A	7:0	Default : 0x08	Access : R/W
	-	7:6	Reserved.	
	DNR_NOR_DIFF_WT[5:0]	5:0	CurY & PreY difference weighting.	
35h (2F6Bh)	REG2F6B	7:0	Default : 0x08	Access : R/W
	-	7:6	Reserved.	
	DNR_NOR_DIFF_CNR_RAW_WT[5:0]	5:0	CurC, PreC & CIIR difference weighting.	
36h (2F6Ch)	REG2F6C	7:0	Default : 0x08	Access : R/W
	-	7:6	Reserved.	
	DNR_NOR_DIFF_Y_CNR_WEIGHT[5:0]	5:0	Y difference weighting.	
36h (2F6Dh)	REG2F6D	7:0	Default : 0x00	Access : R/W
	DNR_CCS_LUT_TH[7:0]	7:0	CCS look up table threshold.	
37h (2F6Eh)	REG2F6E	7:0	Default : 0x00	Access : R/W
	DNR_TABLECCS_0[7:0]	7:0	CNR table.	
37h (2F6Fh)	REG2F6F	7:0	Default : 0x00	Access : R/W
	DNR_TABLECCS_0[15:8]	7:0	Please see description of '2F6Eh'.	
38h (2F70h)	REG2F70	7:0	Default : 0x00	Access : R/W
	DNR_TABLECCS_1[7:0]	7:0	CNR table.	

DNR Register (Bank = 2F, Sub-Bank = 06)

Index (Absolute)	Mnemonic	Bit	Description	
38h (2F71h)	REG2F71	7:0	Default : 0x00	Access : R/W
	DNR_TABLECCS_1[15:8]	7:0	Please see description of '2F70h'.	
39h (2F72h)	REG2F72	7:0	Default : 0x00	Access : R/W
	DNR_TABLECCS_2[7:0]	7:0	CNR table.	
39h (2F73h)	REG2F73	7:0	Default : 0x00	Access : R/W
	DNR_TABLECCS_2[15:8]	7:0	Please see description of '2F72h'.	
3Ah (2F74h)	REG2F74	7:0	Default : 0x00	Access : R/W
	DNR_TABLECCS_3[7:0]	7:0	CNR table.	
3Ah (2F75h)	REG2F75	7:0	Default : 0x00	Access : R/W
	DNR_TABLECCS_3[15:8]	7:0	Please see description of '2F74h'.	
3Bh (2F76h)	REG2F76	7:0	Default : 0x00	Access : R/W
	DNR_TABLECCS_4[7:0]	7:0	CNR table.	
3Bh (2F77h)	REG2F77	7:0	Default : 0x00	Access : R/W
	DNR_TABLECCS_4[15:8]	7:0	Please see description of '2F76h'.	
3Ch (2F78h)	REG2F78	7:0	Default : 0x00	Access : R/W
	DNR_TABLECCS_5[7:0]	7:0	CNR table.	
3Ch (2F79h)	REG2F79	7:0	Default : 0x00	Access : R/W
	DNR_TABLECCS_5[15:8]	7:0	Please see description of '2F78h'.	
3Dh (2F7Ah)	REG2F7A	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	DNR_TABLECCS_6[3:0]	3:0	CNR table.	
3Eh (2F7Ch)	REG2F7C	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	Y_CBR_MUX[2:0]	2:0		
3Fh (2F7Eh)	REG2F7E	7:0	Default : 0x00	Access : R/W
	DNR_TABLEC_0[7:0]	7:0	DNR table C.	
3Fh (2F7Fh)	REG2F7F	7:0	Default : 0x00	Access : R/W
	DNR_TABLEC_0[15:8]	7:0	Please see description of '2F7Eh'.	
40h (2F80h)	REG2F80	7:0	Default : 0x00	Access : R/W
	DNR_TABLEC_1[7:0]	7:0	DNR table C.	
40h (2F81h)	REG2F81	7:0	Default : 0x00	Access : R/W
	DNR_TABLEC_1[15:8]	7:0	Please see description of '2F80h'.	
41h	REG2F82	7:0	Default : 0x00	Access : R/W

DNR Register (Bank = 2F, Sub-Bank = 06)

Index (Absolute)	Mnemonic	Bit	Description	
(2F82h)	DNR_TABLEC_2[7:0]	7:0	DNR table C.	
41h (2F83h)	**REG2F83**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEC_2[15:8]	7:0	Please see description of '2F82h'.	
42h (2F84h)	**REG2F84**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEC_3[7:0]	7:0	DNR table C.	
42h (2F85h)	**REG2F85**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DNR_TABLEC_3[11:8]	3:0	Please see description of '2F84h'.	
43h (2F86h)	**REG2F86**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:6	Reserved.	
	DNR_NOR_DIFF_C_WT[5:0]	5:0	CurC & PreC difference weighting.	
43h (2F87h)	**REG2F87**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:6	Reserved.	
	DNR_NOR_DIFF_HMD_RAW_WT[5:0]	5:0	CurY, PreY & YIIR difference weighting.	
44h (2F88h)	**REG2F88**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:6	Reserved.	
	DNR_NOR_DIFF_C_HMD_WT[5:0]	5:0	C difference weighting.	
44h (2F89h)	**REG2F89**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_HMD_LUT_TH[7:0]	7:0	HMD look up table threshold.	
45h (2F8Ah)	REG2F8A	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEHMD_0[7:0]	7:0	HMD table.	
45h (2F8Bh)	REG2F8B	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEHMD_0[15:8]	7:0	Please see description of '2F8Ah'.	
46h (2F8Ch)	REG2F8C	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEHMD_1[7:0]	7:0	HMD table.	
46h (2F8Dh)	REG2F8D	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEHMD_1[15:8]	7:0	Please see description of '2F8Ch'.	
47h (2F8Eh)	REG2F8E	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEHMD_2[7:0]	7:0	HMD table.	
47h (2F8Fh)	REG2F8F	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEHMD_2[15:8]	7:0	Please see description of '2F8Eh'.	

DNR Register (Bank = 2F, Sub-Bank = 06)

Index (Absolute)	Mnemonic	Bit	Description	
48h (2F90h)	REG2F90	7:0	Default : 0x00	Access : R/W
	DNR_TABLEHMD_3[7:0]	7:0	HMD table.	
48h (2F91h)	REG2F91	7:0	Default : 0x00	Access : R/W
	DNR_TABLEHMD_3[15:8]	7:0	Please see description of '2F90h'.	
49h (2F92h)	REG2F92	7:0	Default : 0x00	Access : R/W
	DNR_TABLEHMD_4[7:0]	7:0	HMD table.	
49h (2F93h)	REG2F93	7:0	Default : 0x00	Access : R/W
	DNR_TABLEHMD_4[15:8]	7:0	Please see description of '2F92h'.	
4Ah (2F94h)	REG2F94	7:0	Default : 0x00	Access : R/W
	DNR_TABLEHMD_5[7:0]	7:0	HMD table.	
4Ah (2F95h)	REG2F95	7:0	Default : 0x00	Access : R/W
	DNR_TABLEHMD_5[15:8]	7:0	Please see description of '2F94h'.	
4Bh (2F96h)	REG2F96	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	DNR_TABLEHMD_6[3:0]	3:0	HMD table.	
4Ch (2F98h)	REG2F98	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	Y_CBR_MUX_HMD[2:0]	2:0		
4Dh (2F9Ah)	REG2F9A	7:0	Default : 0x00	Access : R/W
	DNR_TABLEY_0[7:0]	7:0	DNR table Y.	
4Dh (2F9Bh)	REG2F9B	7:0	Default : 0x00	Access : R/W
	DNR_TABLEY_0[15:8]	7:0	Please see description of '2F9Ah'.	
4Eh (2F9Ch)	REG2F9C	7:0	Default : 0x00	Access : R/W
	DNR_TABLEY_1[7:0]	7:0	DNR table Y.	
4Eh (2F9Dh)	REG2F9D	7:0	Default : 0x00	Access : R/W
	DNR_TABLEY_1[15:8]	7:0	Please see description of '2F9Ch'.	
4Fh (2F9Eh)	REG2F9E	7:0	Default : 0x00	Access : R/W
	DNR_TABLEY_2[7:0]	7:0	DNR table Y.	
4Fh (2F9Fh)	REG2F9F	7:0	Default : 0x00	Access : R/W
	DNR_TABLEY_2[15:8]	7:0	Please see description of '2F9Eh'.	
50h (2FA0h)	REG2FA0	7:0	Default : 0x00	Access : R/W
	DNR_TABLEY_3[7:0]	7:0	DNR table Y.	
50h	REG2FA1	7:0	Default : 0x00	Access : R/W

DNR Register (Bank = 2F, Sub-Bank = 06)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2FA1h)	-	7:4	Reserved.	
	DNR_TABLEY_3[11:8]	3:0	Please see description of '2FA0h'.	
51h (2FA2h)	**REG2FA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MSK_HIS_WT[2:0]	6:4	History ratio weighting.	
	-	3:1	Reserved.	
	EN_DET_CHANGE_SCENE	0	Detect scene change enable.	
51h (2FA3h)	**REG2FA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CHANGE_SCENE_TH[6:0]	6:0	Scene change threshold.	
60h (2FC0h)	**REG2FC0**	**7:0**	**Default : 0x7F**	**Access : R/W**
	-	7	Reserved.	
	FBLALL_FILEDMD	6	FBLALL field bypass mode (FBL_ONLY = 1).	
	YCBCR_422_F1	5	F1. 0: YCbCr422. 1: 444.	
	FBL_422	4	FBL 422 (FBLALL -= 1'b1).	
	FBLALL	3	FBLALL mode; support EODi with 2DDi.	
	UXGA444	2	UXGA444, FB case.	
	PCFB_ONLY	1	Main window is PC 444 format.	
	FBL_ONLY	0	Frame buffer less enable.	
60h (2FC1h)	**REG2FC1**	**7:0**	**Default : 0x00**	**Access : R/W**
	LINEARADD_EN_F2	7	F2 FB linear address mode.	
	LINEARADD_EN_F1	6	F1 FB linear address mode.	
	-	5	Reserved.	
	MIU_DLYMD	4	During main window FBL, sub window must force into MADi mode.	
	FBL_BPMIU	3	Without PIP, reduce MCLK when little memory access to save power.	
	-	2	Reserved.	
	NR_Y_ROUND[1:0]	1:0	Y rounding bits for NR.	
62h (2FC4h)	**REG2FC4**	**7:0**	**Default : 0x00**	**Access : R/W**
	AUTO_VD_PAUSE	7	Auto VD pause.	
	-	6	Reserved.	

DNR Register (Bank = 2F, Sub-Bank = 06)

Index (Absolute)	Mnemonic	Bit	Description	
	FORCE22_F2	5	F2 Force film 22 active.	
	FORCE22_F1	4	F1 Force film 22 active.	
	-	3:0	Reserved.	
63h (2FC6h)	REG2FC6	7:0	Default : 0x0B	Access : R/W
	CCS_HISMD	7	DNR CCS mode.	
	-	6	Reserved.	
	CCS_DEPTH[1:0]	5:4	CCS depth.	
	POSTCCS_HISMD	3	Post CCS history mode.	
	PCNR_CAVG_MAX[1:0]	2:1	PCNR_ADD[2:1] == 2'b11.	
	PCNR_ADD_BIT0	0	De-pack U/V cycle inverse.	
63h (2FC7h)	REG2FC7	7:0	Default : 0x00	Access : R/W
	CCS_TH[4:0]	7:3	CCS threshold.	
	-	2	Reserved.	
	CCS_MD	1	CCS mode. 0: In DNR. 1: Post FIR CNR.	
	-	0	Reserved.	
64h (2FC8h)	REG2FC8	7:0	Default : 0x00	Access : R/W
	F32_NEWTH_EN	7	Frame motion pixel TH (user define enable).	
	F32_NEWTH[2:0]	6:4	Frame motion pixel TH (user define threshold).	
	-	3:0	Reserved.	
64h (2FC9h)	REG2FC9	7:0	Default : -	Access : -
	-	7:0	Reserved.	
65h (2FCAh)	REG2FCA	7:0	Default : 0xEF	Access : R/W
	HIS_WT[2:0]	7:5	History ratio weighting.	
	DNR_HIS_LMT[4:0]	4:0	DNR history ratio limit number.	
65h (2FCBh)	REG2FCB	7:0	Default : 0xFF	Access : R/W
	NR_MOTION_MD	7	NR decide motion mode.	
	TDDI_HIS_YMAX	6	MADi history Y max mode.	
	MADI_EDGE_DEPTH[1:0]	5:4	MADi edge depth.	
	MADI_EDGE_TH[3:0]	3:0	MADi edge threshold.	
66h (2FCDh)	REG2FCD	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	

DNR Register (Bank = 2F, Sub-Bank = 06)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	NR_QLFY_DISABLE	0	NR qualify disable.
68h (2FD0h)	REG2FD0	**7:0**	**Default : -** Access : RO
	DNR_WQ_WAIT_CNT_F1[7:0]	7:0	F1 DNR to MIU status information.
68h (2FD1h)	REG2FD1	**7:0**	**Default : -** Access : RO
	-	7:2	Reserved.
	DNR_WQ_WAIT_CNT_F1[9:8]	1:0	Please see description of '2FD0h'.
69h (2FD2h)	REG2FD2	**7:0**	**Default : -** Access : RO
	DNR_RQ_WAIT_CNT_F1[7:0]	7:0	F1 DNR to MIU status information.
69h (2FD3h)	REG2FD3	**7:0**	**Default : -** Access : RO
	-	7:2	Reserved.
	DNR_RQ_WAIT_CNT_F1[9:8]	1:0	Please see description of '2FD2h'.
6Ah (2FD4h)	REG2FD4	**7:0**	**Default : -** Access : RO
	DNR_C_WAIT_MAX_CNT_F1 [7:0]	7:0	F1 DNR to MIU status information.
6Ah (2FD5h)	REG2FD5	**7:0**	**Default : -** Access : RO
	-	7:3	Reserved.
	DNR_C_WAIT_MAX_CNT_F1 [10:8]	2:0	Please see description of '2FD4h'.
6Bh (2FD6h)	REG2FD6	**7:0**	**Default : -** Access : RO
	DNR_WQ_WAIT_CNT_F2[7:0]	7:0	F2 DNR to MIU status information.
6Bh (2FD7h)	REG2FD7	**7:0**	**Default : -** Access : RO
	-	7:2	Reserved.
	DNR_WQ_WAIT_CNT_F2[9:8]	1:0	Please see description of '2FD6h'.
6Ch (2FD8h)	REG2FD8	**7:0**	**Default : -** Access : RO
	DNR_RQ_WAIT_CNT_F2[7:0]	7:0	F2 DNR to MIU status information (Read Only).
6Ch (2FD9h)	REG2FD9	**7:0**	**Default : -** Access : RO
	-	7:2	Reserved.
	DNR_RQ_WAIT_CNT_F2[9:8]	1:0	Please see description of '2FD8h'.
6Dh (2FDAh)	REG2FDA	**7:0**	**Default : -** Access : RO
	DNR_C_WAIT_MAX_CNT_F2[7:0]	7:0	F2 DNR to MIU status information (Read Only).
6Dh (2FDBh)	REG2FDB	**7:0**	**Default : -** Access : RO
	-	7:3	Reserved.

DNR Register (Bank = 2F, Sub-Bank = 06)

Index (Absolute)	Mnemonic	Bit	Description	
	DNR_C_WAIT_MAX_CNT_F2[10:8]	2:0	Please see description of '2FDAh'.	
6Eh (2FDCh)	REG2FDC	7:0	Default : -	Access : RO
	-	7:6	Reserved.	
	BW_NOT_ENOUGH_F2	5	F2 Bandwidth not enough.	
	CURRDY_PREEMPTY_F2	4	F2 Current data ready, Previous not ready.	
	DNR_WFF_FULL_F2	3	F2 Write FIFO status.	
	BW_NOT_ENOUGH_F1	2	F1 Bandwidth not enough.	
	CURRDY_PREEMPTY_F1	1	F1 Current data ready, Previous not ready.	
	DNR_WFF_FULL_F1	0	F1 Write FIFO status.	
6Eh (2FDDh)	REG2FDD	7:0	Default : 0x00	Access : R/W
	DNR_IIR_RESET	7	Reset DNR IIR state.	
	CLAMP_EN	6	Clamp enable.	
	-	5:0	Reserved.	
6Fh (2FDEh)	REG2FDE	7:0	Default : 0x00	Access : R/W
	CHANGE_SCENE_TH_LO[7:0]	7:0	Scene change threshold.	
70h (2FE0h)	REG2FE0	7:0	Default : 0x00	Access : R/W
	OCONFIGMEN_FB2	7	F2 output data configuration user define enable.	
	OCONFIGM_FB2[2:0]	6:4	F2 output data configuration user define.	
	OCONFIGMEN_FB1	3	F1 output data configuration user define enable.	
	OCONFIGM_FB1[2:0]	2:0	F1 output data configuration user define.	
70h (2FE1h)	REG2FE1	7:0	Default : 0x00	Access : R/W
	ICONFIGMEN_FB2	7	F2 input data configuration user define enable.	
	ICONFIGM_FB2[2:0]	6:4	F2 input data configuration user define.	
	ICONFIGMEN_FB1	3	F1 input data configuration user define enable.	
	ICONFIGM_FB1[2:0]	2:0	F1 input data configuration user define.	
71h (2FE2h)	REG2FE2	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	LINEAR_MD_CTRL	0	FB linear mode control.	
71h (2FE3h)	REG2FE3	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	HIS_FILTER_MD	4	History ratio mode.	
	HIS_RATIO_OFFSET[3:0]	3:0	History ratio offset.	

DNR Register (Bank = 2F, Sub-Bank = 06)

Index (Absolute)	Mnemonic	Bit	Description	
7Ch (2FF8h)	REG2FF8	7:0	Default : 0x00	Access : R/W
	WADR_BOUNDARY_F1[7:0]	7:0	DNR write limit boundary for f1.	
7Ch (2FF9h)	REG2FF9	7:0	Default : 0x00	Access : R/W
	WADR_BOUNDARY_F1[15:8]	7:0	Please see description of '2FF8h'.	
7Dh (2FFAh)	REG2FFA	7:0	Default : 0x00	Access : R/W
	WADR_BOUNDARY_F2[7:0]	7:0	DNR write limit boundary for f2.	
7Dh (2FFBh)	REG2FFB	7:0	Default : 0x00	Access : R/W
	WADR_BOUNDARY_F2[15:8]	7:0	Please see description of '2FFAh'.	
7Eh (2FFCh)	REG2FFC	7:0	Default : 0x00	Access : R/W
	WADR_BOUNDARY_EN_F1	7	DNR write limit enable for f1.	
	-	6:4	Reserved.	
	WADR_BOUNDARY_19_16_F1 [3:0]	3:0	DNR write limit boundary for f1.	
7Eh (2FFDh)	REG2FFD	7:0	Default : 0x00	Access : R/W
	WADR_BOUNDARY_EN_F2	7	DNR write limit enable for f2.	
	-	6:4	Reserved.	
	WADR_BOUNDARY_19_16_F2 [3:0]	3:0	DNR write limit boundary for f2.	

OP1 Register (Bank = 2F, Sub-Bank = 07)

OP1 Register (Bank = 2F, Sub-Bank = 07)				
Index (Absolute)	Mnemonic	Bit	Description	
01h (2F02h)	REG2F02	7:0	Default : 0x00	Access : R/W
	MAIN_ACC	7	MWE window enable.	
	CSC_EN_MWE	6	Sub window or MWE window RGB to YCbCr enable.	
	-	5:3	Reserved.	
	NL_SEL	2	Nonlinear scaling select. 0: Horizontal. 1: Vertical.	
	NL_EN	1	Nonlinear scaling enable.	
	CSC_EN_MAIN	0	Main window RGB to YCbCr enable.	
01h	-	7:0	Default : -	Access : -

OP1 Register (Bank = 2F, Sub-Bank = 07)				
Index (Absolute)	Mnemonic	Bit	Description	
(2F03h)	-	7:0	Reserved.	
02h (2F04h)	**REG2F04**	7:0	Default : 0x00	Access : R/W
	ZDC0_H[7:0]	7:0	Nonlinear scaling section 0 dot count divided by 2.	
02h (2F05h)	**REG2F05**	7:0	Default : 0x00	Access : R/W
	ZDC1_H[7:0]	7:0	Nonlinear scaling section 1 dot count divided by 2.	
03h (2F06h)	**REG2F06**	7:0	Default : 0x00	Access : R/W
	ZDC2_H[7:0]	7:0	Nonlinear scaling section 2 dot count divided by 2.	
04h (2F08h)	**REG2F08**	7:0	Default : 0x00	Access : R/W
	SIGN_INIH	7	Nonlinear scaling section initial offset sign. 0: Positive value. 1: Negative value.	
	DELTA_INIH[6:0]	6:0	Nonlinear scaling section initial offset.	
05h (2F0Ah)	**REG2F0A**	7:0	Default : 0x00	Access : R/W
	DELTA0_H[7:0]	7:0	Nonlinear scaling delta for section 0, bit 7 is sign bit.	
05h (2F0Bh)	**REG2F0B**	7:0	Default : 0x00	Access : R/W
	DELTA1_H[7:0]	7:0	Nonlinear scaling delta for section 1, bit 7 is sign bit.	
06h (2F0Ch)	**REG2F0C**	7:0	Default : 0x00	Access : R/W
	SRH[7:0]	7:0	Horizontal scaling ratio (2 bits integer, 20 bits fraction) for scaling-down to 1/3.9999. xx.xxxxxxxxxxxxxxxxxxxx	
06h (2F0Dh)	**REG2F0D**	7:0	Default : 0x00	Access : R/W
	SRH[15:8]	7:0	Please see description of '2F0Ch'.	
07h (2F0Eh)	**REG2F0E**	7:0	Default : 0x00	Access : R/W
	SENH	7	Horizontal scaling enable. 0: Disable. 1: Enable.	
	-	6	Reserved.	
	SRH[21:16]	5:0	Please see description of '2F0Ch'.	
08h (2F10h)	**REG2F10**	7:0	Default : 0x00	Access : R/W
	SRV[7:0]	7:0	Vertical scaling ratio (2 bits integer, 20 bits fraction) for scaling-down to 1/2.9999. xx.xxxxxxxxxxxxxxxxxxxx	
08h (2F11h)	**REG2F11**	7:0	Default : 0x00	Access : R/W
	SRV[15:8]	7:0	Please see description of '2F10h'.	

OP1 Register (Bank = 2F, Sub-Bank = 07)

Index (Absolute)	Mnemonic	Bit	Description	
09h (2F12h)	REG2F12	7:0	Default : 0x00	Access : R/W
	SENV	7	Vertical scaling enable. 0: Disable. 1: Enable.	
	VFMD	6	Vertical scaling factor mode. 0: N-1/M-1 for horizontal scaling factor. 1: N/M for horizontal scaling factor.	
	SRV[21:16]	5:0	Please see description of '2F10h'.	
0Ah (2F14h)	REG2F14	7:0	Default : 0x00	Access : R/W
	YRAMH_SEL	7	Y/G horizontal scaling SRAM select. 0: SRAM 1. 1: SRAM 2.	
	YRAMH_EN	6	Y/G horizontal scaling using SRAM. 0: Disable. 1: Enable.	
	CRAMH_SEL	5	C/RB horizontal scaling SRAM select. 0: SRAM 1. 1: SRAM 2.	
	CRAMH_EN	4	C/RB horizontal scaling using SRAM. 0: Disable. 1: Enable.	
	MD_H[3:0]	3:0	Mode H.	
0Ah (2F15h)	REG2F15	7:0	Default : 0x00	Access : R/W
	YRAMV_SEL	7	Y/G vertical scaling SRAM select. 0: SRAM 1. 1: SRAM 2.	
	YRAMV_EN	6	Y/G vertical scaling using SRAM. 0: Disable. 1: Enable.	
	CRAMV_SEL	5	C/RB vertical scaling SRAM select. 0: SRAM 1. 1: SRAM 2.	
	CRAMV_EN	4	C/RB vertical scaling using SRAM. 0: Disable. 1: Enable.	
	MD_V[3:0]	3:0	Mode V.	
0Ch	REG2F18	7:0	Default : 0x00	Access : R/W

OP1 Register (Bank = 2F, Sub-Bank = 07)

Index (Absolute)	Mnemonic	Bit	Description	
(2F18h)	HSP_DITH	7	Dither for HSP.	
	OPCSC_DITH_EN	6	Display side RGB to YCbCr dithering enable.	
	-	5:0	Reserved.	
0Dh (2F1Ah)	**REG2F1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	VRAM_WREN	7	VRAM write enable.	
	POS_CBHDOWN_PIPE	6	Pos-CBHDown pipe option.	
	HBCTRL	5	Horizontal boundary control.	
	VBCTRL	4	Vertical boundary control.	
	POSCBVDOWN	3	Pos-CBVDown.	
	POSCBHDOWN	2	Pos-CBHDown.	
	BLK_IN_BLANK	1	Black in blanking.	
	FL_FLD_FACMD	0	Field average for 2DDi.	
0Dh (2F1Bh)	**REG2F1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	LB_CLK_MD[1:0]	7:6	LB clock mode.	
	FCLK_MPLL_SEL	5	LB clock select MPLL CLK.	
	FL_MCLK_SEL	4	LB clock select MCLK.	
	FCLK_SRC[1:0]	3:2	FCLK source. 00: Fix clock control by Bank 0 D1[7]. 01: MCLK. 10: Display clock.	
	-	1	Reserved.	
	FCLK_DIV	0	Divide by 2 when FCLK_SRC = 0 to save power.	
0Eh (2F1Ch)	**REG2F1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_DITH	7	Dither for VSP.	
	VFAC_HALF	6	VFAC 0.5 x. 0: Disable. 1: Enable.	
	-	5:0	Reserved.	
10h (2F20h)	**REG2F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	RATIO_C_MIN[3:0]	7:4	Minimum ratio C.	
	422_TO_444F	3	422 to 444 filter.	
	INDEP_C_RATIO	2	Independent C ratio.	
	SW_422_TO_444F	1	Sub window 422 to 444 filter.	
	-	0	Reserved.	

OP1 Register (Bank = 2F, Sub-Bank = 07)

Index (Absolute)	Mnemonic	Bit	Description	
10h (2F21h)	REG2F21	7:0	Default : 0x00	Access : R/W
	FILM_EODI	7	Film mode with EODi.	
	FILM_3DDI	6	Film mode with 3DDi.	
	FILM_3DDI_FMMD	5	Film mode with 3DDi frame mode.	
	-	4	Reserved.	
	F3DDI_RATIO_B[1:0]	3:2	Film mode 3DDi ratio B.	
	F3DDI_RATIO_A[1:0]	1:0	Film mode 3DDi ratio A.	
13h (2F26h)	REG2F26	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	WB_MSK_SEL	3	Write back mask window select.	
	WB_DOTLINE_POL	2	Write back dot line polarity.	
	WB_MSK_CTL[1:0]	1:0	Write back mask function select.	
15h (2F2Ah)	REG2F2A	7:0	Default : 0x00	Access : R/W
	RATIO_CDIV_SEP	7	Ratio C DIV separate mode.	
	-	6:3	Reserved.	
	RATIO_CDIV[2:0]	2:0	Ratio C DIV (when bit[7] = 1).	
15h (2F2Bh)	REG2F2B	7:0	Default : 0x00	Access : R/W
	MW_YCBCR444	7	Main window is YCbCr 444 format at display side for boundary process.	
	DISP_RA_CNT[6:0]	6:0	Display request ahead counter (divide by 4).	
16h (2F2Ch)	REG2F2C	7:0	Default : 0x00	Access : R/W
	HFRAC_INI__KSTHINI1[7:0]	7:0	H scaling fraction, initial value.	
16h (2F2Dh)	REG2F2D	7:0	Default : 0x00	Access : R/W
	COR_EN_YH	7	Y/G coring enable for HSP.	
	LH_LMT_EN_YH	6	Y/G LH limit enable for HSP.	
	COR_EN_CH	5	C/RB coring enable for HSP.	
	LH_LMT_EN_CH	4	Y/G LH limit enable for HSP.	
	-	3:0	Reserved.	
17h (2F2Eh)	REG2F2E	7:0	Default : 0x00	Access : R/W
	L_LMT_YH[7:0]	7:0	Low limit for Y/G, horizontal scaling.	
17h (2F2Fh)	REG2F2F	7:0	Default : 0x00	Access : R/W
	H_LMT_YH[7:0]	7:0	High limit for Y/G, horizontal scaling.	
18h	REG2F30	7:0	Default : 0x00	Access : R/W

OP1 Register (Bank = 2F, Sub-Bank = 07)

Index (Absolute)	Mnemonic	Bit	Description	
(2F30h)	L_LMT_CH[7:0]	7:0	Low limit for C/RB, horizontal scaling.	
18h (2F31h)	**REG2F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_LMT_CH[7:0]	7:0	High limit for C/RB, horizontal scaling.	
19h (2F32h)	**REG2F32**	**7:0**	**Default : 0x00**	**Access : R/W**
	COR_TH_YH[7:0]	7:0	Coring threshold for Y/G, horizontal scaling.	
19h (2F33h)	**REG2F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	COR_TH_CH[7:0]	7:0	Coring threshold for C/RB, horizontal scaling.	
1Ah (2F34h)	**REG2F34**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFRAC_INI[7:0]	7:0	V scaling fraction, initial value.	
1Ah (2F35h)	**REG2F35**	**7:0**	**Default : 0x00**	**Access : R/W**
	COR_EN_YV	7	Y/G coring enable for VSP.	
	LH_LMT_EN_YV	6	Y/G LH limit enable for VSP.	
	COR_EN_CV	5	C/RB coring enable for VSP.	
	LH_LMT_EN_CV	4	C/RB LH limit enable for VSP.	
	-	3:0	Reserved.	
1Bh (2F36h)	**REG2F36**	**7:0**	**Default : 0x00**	**Access : R/W**
	L_LMT_YV[7:0]	7:0	Low limit for Y/G, vertical scaling.	
1Bh (2F37h)	**REG2F37**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_LMT_YV[7:0]	7:0	High limit for Y/G, vertical scaling.	
1Ch (2F38h)	**REG2F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	L_LMT_CV[7:0]	7:0	Low limit for C/RB, vertical scaling.	
1Ch (2F39h)	**REG2F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_LMT_CV[7:0]	7:0	High limit for C/RB, vertical scaling.	
1Dh (2F3Ah)	REG2F3A	**7:0**	**Default : 0x00**	**Access : R/W**
	COR_TH_YV[7:0]	7:0	Coring threshold for Y/G, vertical scaling.	
1Dh (2F3Bh)	REG2F3B	**7:0**	**Default : 0x00**	**Access : R/W**
	COR_TH_CV[7:0]	7:0	Coring threshold for C/RB, vertical scaling.	
1Eh (2F3Ch)	REG2F3C	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	VER_C_LPF_EN_SUB	5	Sub window vertical C low pass filter enable.	
	SPK_NR_EN_SUB	4	Sub window spike NR enable.	
	-	3:2	Reserved.	
	VER_C_LPF_EN	1	Vertical C low pass filter enable.	

OP1 Register (Bank = 2F, Sub-Bank = 07)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	SPK_NR_EN	0	Spike NR enable.
1Eh (2F3Dh)	**REG2F3D**	**7:0**	**Default : 0x00** Access : R/W
	PTH0[7:0]	7:0	P threshold 0.
1Fh (2F3Eh)	**REG2F3E**	**7:0**	**Default : 0x00** Access : R/W
	-	7:5	Reserved.
	PTH1[4:0]	4:0	P threshold 1.
1Fh (2F3Fh)	**REG2F3F**	**7:0**	**Default : 0x00** Access : R/W
	PTH2[7:0]	7:0	P threshold 2.
20h (2F40h)	**REG2F40**	**7:0**	**Default : 0x00** Access : R/W
	PTH3[7:0]	7:0	P threshold 3.
20h (2F41h)	**REG2F41**	**7:0**	**Default : 0x00** Access : R/W
	D11_21_STEP[2:0]	7:5	Spike NR D11_21 step.
	-	4	Reserved.
	SPK_NR_COEF[3:0]	3:0	Spike NR coefficient.
21h (2F42h)	**REG2F42**	**7:0**	**Default : 0x00** Access : R/W
	D31_STEP[2:0]	7:5	Spike NR D31 step.
	-	4:0	Reserved.
21h (2F43h)	**REG2F43**	**7:0**	**Default : 0x00** Access : R/W
	YP22_STEP[2:0]	7:5	Spike NR YP22 step.
	-	4:0	Reserved.
28h (2F50h)	**REG2F50**	**7:0**	**Default : 0x00** Access : R/W
	RDATA_BB_OFF[1:0]	7:6	RDATA BB offset.
	RDATA_BC_OFF[1:0]	5:4	RDATA BC offset.
	RDATA_BA_OFF[3:0]	3:0	RDATA BA offset.
28h (2F51h)	**REG2F51**	**7:0**	**Default : 0x28** Access : R/W
	RADDR_B_OFFS[7:0]	7:0	Read address B offset.
29h (2F52h)	**REG2F52**	**7:0**	**Default : 0x30** Access : R/W
	PIPE_CTRL2[7:0]	7:0	Internal pipe control 2. 30h: Recommended settings. Other value: Not recommended, for testing only.
2Ah (2F54h)	**REG2F54**	**7:0**	**Default : 0x00** Access : R/W
	VLEN[7:0]	7:0	Vertical length after pre-scaling down in memory.
2Ah	**REG2F55**	**7:0**	**Default : 0x00** Access : R/W

OP1 Register (Bank = 2F, Sub-Bank = 07)

Index (Absolute)	Mnemonic	Bit	Description	
(2F55h)	-	7:3	Reserved.	
	VLEN[10:8]	2:0	Please see description of '2F54h'.	
2Bh (2F56h)	**REG2F56**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_VLEN[7:0]	7:0	Sub window vertical length after pre-scaling down in memory.	
2Bh (2F57h)	**REG2F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SW_VLEN[10:8]	2:0	Please see description of '2F56h'.	
2Fh (2F5Fh)	**REG2F5F**	**7:0**	**Default : 0x00**	**Access : R/W**
	3DDI_ETHA[7:0]	7:0	3DDi E threshold A; EDIV1[3:0], EDIV0[3:0] (when E DIV SEL = 1).	
30h (2F60h)	**REG2F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	3DDI_ETHB[7:0]	7:0	3DDi E threshold B; EDIV3[3:0], EDIV2[3:0] (when E DIV SEL = 1).	
30h (2F61h)	**REG2F61**	**7:0**	**Default : 0x00**	**Access : R/W**
	3DDI_ETHC[7:0]	7:0	3DDi E Threshold C; EDIV5[3:0], EDIV4[3:0] (when E DIV SEL = 1).	
31h (2F62h)	**REG2F62**	**7:0**	**Default : 0x00**	**Access : R/W**
	3DDI_EDIVB[3:0]	7:4	3DDi E divider B.	
	3DDI_EDIVA[3:0]	3:0	3DDi E divider D.	
31h (2F63h)	**REG2F63**	**7:0**	**Default : 0x00**	**Access : R/W**
	3DDI_EDIVD[3:0]	7:4	3DDi EG divider A.	
	3DDI_EDIVC[3:0]	3:0	3DDi E divider C.	
32h (2F64h)	**REG2F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	DS_LMT_EN_F1	7	DS MAX limit enable for F1 window.	
	DS_MAX_LMT1[5:0]	6:1	DS MAX limit value for F1 window.	
	DS_EN_F1	0	DS enable for F1 window.	
32h (2F65h)	**REG2F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	DS_LMT_EN_F2	7	DS MAX limit enable for F2 window.	
	DS_MAX_LMT2[5:0]	6:1	DS MAX limit value for F2 window.	
	DS_EN_F2	0	DS enable for F2 window.	
33h (2F66h)	**REG2F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	DS_DET_TH1[7:0]	7:0	DS detect TH 1 for F1 window.	
33h	**REG2F67**	**7:0**	**Default : 0x00**	**Access : R/W**

OP1 Register (Bank = 2F, Sub-Bank = 07)

Index (Absolute)	Mnemonic	Bit	Description	
(2F67h)	DS_PCT_TH1[7:0]	7:0	DS PCT TH 1 for F1 window.	
34h (2F68h)	**REG2F68**	**7:0**	Default : 0x00	Access : R/W
	DS_DET_TH2[7:0]	7:0	DS Detect TH 2 for F2 window.	
34h (2F69h)	**REG2F69**	**7:0**	Default : 0x00	Access : R/W
	DS_PCT_TH2[7:0]	7:0	DS PCT TH 2 for F2 window.	
35h (2F6Ah)	**REG2F6A**	**7:0**	Default : 0x00	Access : R/W
	FCLK_GWAITCNT[3:0]	7:4	FCLK gating wait counter for power saving.	
	FCLKH1_GEN[1:0]	3:2	FCLKH1 clock gating option.	
	FCLK1_GEN[1:0]	1:0	FCLK clock gating option.	
35h (2F6Bh)	**REG2F6B**	**7:0**	Default : 0x00	Access : R/W
	FCLK_ELA_GEN[1:0]	7:6	FCLK ELA clock gating option.	
	ODCLK_GEN[1:0]	5:4	Output dot clock gate enable. 00: No gating. 01: V. 10: H+V.	
	-	3	Reserved.	
	MCLK_APP_GEN	2	MCLK APP clock gating option.	
	MCLK_APPO_GEN	1	MCLK APP out clock gating option.	
	MCLK_APPI_GEN	0	MCLK APP in clock gating option.	
36h (2F6Ch)	**REG2F6C**	**7:0**	Default : 0x00	Access : R/W
	-	7	Reserved.	
	IDGCLK_VGEN_F2	6	IDCLK V blanking power saving.	
	IDGCLK_HGEN_F2	5	IDCLK H blanking power saving.	
	NO_SIGNAL_GEN_F2	4	No signal self-power down for IDCLK.	
	-	3	Reserved.	
	IDGCLK_VGEN_F1	2	Sub window IDCLK V blanking power saving.	
	IDGCCLK_HGEN_F1	1	Sub window IDCLK H blanking power saving.	
	NO_SIGNAL_GEN_F1	0	Sub window no signal self-power down for IDCLK.	
37h (2F6Eh)	**REG2F6E**	**7:0**	Default : 0x00	Access : R/W
	SW_SRH[7:0]	7:0	Sub window horizontal scaling ratio (2 bits integer, 20 bits fraction) for scaling down to 1/3.9999. xx.xxxxxxxxxxxxxxxxxxxx	
37h (2F6Fh)	**REG2F6F**	**7:0**	Default : 0x00	Access : R/W
	SW_SRH[15:8]	7:0	Please see description of '2F6Eh'.	

OP1 Register (Bank = 2F, Sub-Bank = 07)

Index (Absolute)	Mnemonic	Bit	Description	
38h (2F70h)	REG2F70	7:0	Default : 0x00	Access : R/W
	SW_SENH	7	Sub window horizontal scaling enable. 0: Disable. 1: Enable.	
	SW_NL_EN	6	Sub window nonlinear scaling enable.	
	SW_SRH[21:16]	5:0	Please see description of '2F6Eh'.	
39h (2F72h)	REG2F72	7:0	Default : 0x00	Access : R/W
	SW_SRV[7:0]	7:0	Sub window vertical scaling ratio (2 bits integer, 20 bits fraction) for scaling down to 1/2.9999. xx.xxxxxxxxxxxxxxxxxxxx	
39h (2F73h)	REG2F73	7:0	Default : 0x00	Access : R/W
	SW_SRV[15:8]	7:0	Please see description of '2F72h'.	
3Ah (2F74h)	REG2F74	7:0	Default : 0x00	Access : R/W
	SW_SENV	7	Sub window vertical scaling enable. 0: Disable. 1: Enable.	
	SW_VFMD	6	Sub window vertical scaling factor mode. 0: N-1/M-1 for horizontal scaling factor. 1: N/M for horizontal scaling factor.	
	SW_SRV[21:16]	5:0	Please see description of '2F72h'.	
3Bh (2F76h)	REG2F76	7:0	Default : 0x00	Access : R/W
	SW_YRAMH_SEL	7	Sub window Y/G horizontal scaling SRAM select. 0: SRAM 1. 1: SRAM 2.	
	SW_YRAMH_EN	6	Sub window Y/G horizontal scaling using SRAM. 0: Disable. 1: Enable.	
	SW_CRAMH_SEL	5	Sub window C/RB horizontal scaling SRAM select. 0: SRAM 1. 1: SRAM 2.	
	SW_CRAMH_EN	4	Sub window C/RB horizontal scaling using SRAM. 0: Disable. 1: Enable.	
	SW_MDH[3:0]	3:0	Sub window mode H.	
3Bh (2F77h)	REG2F77	7:0	Default : 0x00	Access : R/W
	SW_YRAMV_SEL	7	Sub window Y/G vertical scaling SRAM select.	

OP1 Register (Bank = 2F, Sub-Bank = 07)

Index (Absolute)	Mnemonic	Bit	Description
			0: SRAM 1. 1: SRAM 2.
	SW_YRAMV_EN	6	Sub window Y/G vertical scaling using SRAM. 0: Disable. 1: Enable.
	SW_CRAMV_SEL	5	Sub window C/RB vertical scaling SRAM select. 0: SRAM 1. 1: SRAM 2.
	SW_CRAMV_EN	4	Sub window C/RB vertical scaling using SRAM. 0: Disable. 1: Enable.
	SW_MDV[3:0]	3:0	Sub window mode V.
3Dh (2F7Ah)	REG2F7A	7:0	Default : 0x00 Access : R/W
	SW_HSP_DITH	7	Sub window dither for HSP.
	-	6:0	Reserved.
3Eh (2F7Ch)	REG2F7C	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	SW_POSCBVDOWN	3	Sub window Pos_CBVDown.
	SW_POSCBHDOWN	2	Sub window Pos_CBHDown.
	SW_BLK_IN_BLANK	1	Sub window black in blanking.
	-	0	Reserved.
3Fh (2F7Eh)	REG2F7E	7:0	Default : 0x00 Access : R/W
	SW_VSP_DITH	7	Sub window dither for VSP.
	SW_VFAC_HALF	6	Sub window VFAC 0.5 x. 0: Disable. 1: Enable.
	-	5:0	Reserved.
40h (2F80h)	REG2F80	7:0	Default : 0x00 Access : R/W
	SW_HFRAC_INI__KSTHINI1[7:0]	7:0	Sub window H scaling fraction, initial value.
40h (2F81h)	REG2F81	7:0	Default : 0x00 Access : R/W
	SW_COR_EN_YH	7	Sub window Y/G coring enable for HSP.
	SW_LH_LMT_EN_YH	6	Sub window Y/G LH limit enable for HSP.
	SW_COR_EN_CH	5	Sub window C/RB coring enable for HSP.
	SW_LH_LMT_EN_CH	4	Sub window Y/G LH limit enable for HSP.

OP1 Register (Bank = 2F, Sub-Bank = 07)

Index (Absolute)	Mnemonic	Bit	Description	
	-	3:0	Reserved.	
41h (2F82h)	REG2F82	7:0	Default : 0x00	Access : R/W
	SW_L_LMT_YH[7:0]	7:0	Sub window low limit for Y/G, horizontal scaling.	
41h (2F83h)	REG2F83	7:0	Default : 0x00	Access : R/W
	SW_H_LMT_YH[7:0]	7:0	Sub window high limit for Y/G, horizontal scaling.	
42h (2F84h)	REG2F84	7:0	Default : 0x00	Access : R/W
	SW_L_LMT_CH[7:0]	7:0	Sub window low limit for C/RB, horizontal scaling.	
42h (2F85h)	REG2F85	7:0	Default : 0x00	Access : R/W
	SW_H_LMT_CH[7:0]	7:0	Sub window high limit for C/RB, horizontal scaling.	
43h (2F86h)	REG2F86	7:0	Default : 0x00	Access : R/W
	SW_COR_TH_YH[7:0]	7:0	Sub window coring threshold for Y/G, horizontal scaling.	
43h (2F87h)	REG2F87	7:0	Default : 0x00	Access : R/W
	SW_COR_TH_CH[7:0]	7:0	Sub window coring threshold for C/RB, horizontal scaling.	
44h (2F88h)	REG2F88	7:0	Default : 0x00	Access : R/W
	SW_VFRAC_INI[7:0]	7:0	Sub window V scaling fraction, initial value.	
44h (2F89h)	REG2F89	7:0	Default : 0x00	Access : R/W
	SW_COR_EN_YV	7	Sub window Y/G coring enable for VSP.	
	SW_LH_LMT_EN_YV	6	Sub window Y/G LH limit enable for VSP.	
	SW_COR_EN_CV	5	Sub window C/RB coring enable for VSP.	
	SW_LH_LMT_EN_CV	4	Sub window C/RB LH limit enable for VSP.	
	-	3:0	Reserved.	
45h (2F8Ah)	REG2F8A	7:0	Default : 0x00	Access : R/W
	SW_L_LMT_YV[7:0]	7:0	Sub window low limit for Y/G, vertical scaling.	
45h (2F8Bh)	REG2F8B	7:0	Default : 0x00	Access : R/W
	SW_H_LMT_YV[7:0]	7:0	Sub window high limit for Y/G, vertical scaling.	
46h (2F8Ch)	REG2F8C	7:0	Default : 0x00	Access : R/W
	SW_L_LMT_CV[7:0]	7:0	Low limit for C/RB, vertical scaling.	
46h (2F8Dh)	REG2F8D	7:0	Default : 0x00	Access : R/W
	SW_H_LMT_CV[7:0]	7:0	Sub window high limit for C/RB, vertical scaling.	
47h (2F8Eh)	REG2F8E	7:0	Default : 0x00	Access : R/W
	SW_COR_TH_YV[7:0]	7:0	Sub window coring threshold for Y/G, vertical scaling.	
47h	REG2F8F	7:0	Default : 0x00	Access : R/W

OP1 Register (Bank = 2F, Sub-Bank = 07)

Index (Absolute)	Mnemonic	Bit	Description		
(2F8Fh)	SW_COR_TH_CV[7:0]	7:0	Sub window coring threshold for C/RB, vertical scaling.		
48h (2F90h)	REG2F90	7:0	Default : 0x07		Access : R/W
	-	7:4	Reserved.		
	VSP_Y234_SEL	3	VSP alpha coring line select.		
	VSP_CALPHACOR_DISABLE	2	VSP C alpha coring disable.		
	VSP_YALPHACOR_DISABLE	1	VSP Y alpha coring disable.		
	VSP_GAIN_DISABLE	0	VSP gain function disable.		
49h (2F92h)	REG2F92	7:0	Default : 0x00		Access : R/W
	VSP_TBL_YALPHA_L[7:0]	7:0	VSP table Y alpha; 0x4B[7:0], 0x4A[15:0], 0x49[15:0].		
49h (2F93h)	REG2F93	7:0	Default : 0x00		Access : R/W
	VSP_TBL_YALPHA_L[15:8]	7:0	Please see description of '2F92h'.		
4Ah (2F94h)	REG2F94	7:0	Default : 0x00		Access : R/W
	VSP_TBL_YALPHA_M[7:0]	7:0	VSP table Y alpha; 0x4B[7:0], 0x4A[15:0], 0x49[15:0].		
4Ah (2F95h)	REG2F95	7:0	Default : 0x00		Access : R/W
	VSP_TBL_YALPHA_M[15:8]	7:0	Please see description of '2F94h'.		
4Bh (2F96h)	REG2F96	7:0	Default : 0x00		Access : R/W
	VSP_TBL_YALPHA_H[7:0]	7:0	VSP table Y alpha; 0x4B[7:0], 0x4A[15:0], 0x49[15:0].		
4Bh (2F97h)	REG2F97	7:0	Default : 0x00		Access : R/W
	VSP_TBL_CALPHA_L[7:0]	7:0	VSP table C alpha; 0x4D[15:0], 0x4C[15:0], 0x4B[15:7].		
4Ch (2F98h)	REG2F98	7:0	Default : 0x00		Access : R/W
	VSP_TBL_CALPHA_M[7:0]	7:0	VSP table C alpha; 0x4D[15:0], 0x4C[15:0], 0x4B[15:7].		
4Ch (2F99h)	REG2F99	7:0	Default : 0x00		Access : R/W
	VSP_TBL_CALPHA_M[15:8]	7:0	Please see description of '2F98h'.		
4Dh (2F9Ah)	REG2F9A	7:0	Default : 0x00		Access : R/W
	VSP_TBL_CALPHA_H[7:0]	7:0	VSP table C alpha; 0x4D[15:0], 0x4C[15:0], 0x4B[15:7].		
4Dh (2F9Bh)	REG2F9B	7:0	Default : 0x00		Access : R/W
	VSP_TBL_CALPHA_H[15:8]	7:0	Please see description of '2F9Ah'.		
4Eh (2F9Ch)	REG2F9C	7:0	Default : 0x07		Access : R/W
	-	7:4	Reserved.		
	SW_VSP_Y234_SEL	3	Sub window VSP alpha coring line select.		
	SW_VSP_CALPHACOR_ DISABLE	2	Sub window VSP C alpha coring disable.		
	SW_VSP_YALPHACOR_	1	Sub window VSP Y alpha coring disable.		

OP1 Register (Bank = 2F, Sub-Bank = 07)

Index (Absolute)	Mnemonic	Bit	Description	
	DISABLE			
	SW_VSP_GAIN_DISABLE	0	Sub window VSP gain function disable.	
4Fh (2F9Eh)	REG2F9E	7:0	Default : 0x00	Access : R/W
	VSP_TBL_GAIN[7:0]	7:0	VSP table gain.	
4Fh (2F9Fh)	REG2F9F	7:0	Default : 0x00	Access : R/W
	VSP_TBL_GAIN[15:8]	7:0	Please see description of '2F9Eh'.	
50h (2FA0h)	REG2FA0	7:0	Default : 0x00	Access : R/W
	VSP_TBL_GAIN[23:16]	7:0	Please see description of '2F9Eh'.	
50h (2FA1h)	REG2FA1	7:0	Default : 0x00	Access : R/W
	VSP_TBL_GAIN[31:24]	7:0	Please see description of '2F9Eh'.	
51h (2FA2h)	REG2FA2	7:0	Default : 0x00	Access : R/W
	VSP_TBL_GAIN[39:32]	7:0	Please see description of '2F9Eh'.	
51h (2FA3h)	REG2FA3	7:0	Default : 0x00	Access : R/W
	VSP_TBL_GAIN[47:40]	7:0	Please see description of '2F9Eh'.	
52h (2FA4h)	REG2FA4	7:0	Default : 0x00	Access : R/W
	VSP_TBL_GAIN[55:48]	7:0	Please see description of '2F9Eh'.	
52h (2FA5h)	REG2FA5	7:0	Default : 0x00	Access : R/W
	VSP_TBL_GAIN[63]	7	Please see description of '2F9Eh'.	
	BOUNDARY_MD_INDP	6	Independent boundary mode.	
	HSP_BOUND_F1	5	Sub window horizontal boundary control.	
	VSP_BOUND_F1	4	Sub window vertical boundary control.	
	VSP_TBL_GAIN[59:56]	3:0	Please see description of '2F9Eh'.	

OP1PIP Register (Bank = 2F, Sub-Bank = 08)

Index (Absolute)	Mnemonic	Bit	Description	
01h (2F02h)	REG2F02	7:0	Default : 0x00	Access : R/W
	LCKF1	7	Frame lock with F1 window enable.	
	FRC_AUTO	6	Auto mode in frame lock.	
	F1_IS_SUB	5	F1 window is sub.	
	F2_IS_SUB	4	F2 window is sub.	

OP1PIP Register (Bank = 2F, Sub-Bank = 08)

Index (Absolute)	Mnemonic	Bit	Description	
	-	3	Reserved.	
	F2_ONTOP	2	F2 window is on top.	
	PIP_STS[1:0]	1:0	PIP status. 00: F2 only. 01: F1 only. 1x: PIP.	
02h (2F04h)	**REG2F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SUBVSTMSK[2:0]	2:0	Sub VST mask 0-5 when sub is enable.	
02h (2F05h)	**REG2F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SUBVEDMSK[2:0]	2:0	Sub VED mask 0-5 when sub is enable.	
03h (2F06h)	**REG2F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIP_CASESW_EN	7	PIP case software enable.	
	-	6	Reserved.	
	PIP_CASE[1:0]	5:4	PIP case reported.	
	-	3:2	Reserved.	
	TUNE_RQ_STS[1:0]	1:0	Tune request status reported.	
05h (2F0Bh)	**REG2F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	PIP_VT[2:0]	2:0	PIP_VT[2:0] shift count/PIP_VTED[2:0].	
06h (2F0Ch)	**REG2F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIP_2SA_EN	7	PIP 2Side A to AA request delay enable.	
	PIP_2SA_CNT[6:0]	6:0	PIP 2Side A to AA request delay count.	
06h (2F0Dh)	**REG2F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIP_SUB2D_PULSE2	7	PIP pulse twice for 2DDi mode.	
	PIP_SUB2D_DIV2	6	PIP V-length divided by 2 for 2DDi mode.	
	NONLINEAR_PIPEFIX	5	Non-linear pipe option.	
	PIP_HFACB_FIX	4	PIP HFAC fix for turn-around cycle.	
	PIP_BINI_PLUS[1:0]	3:2	PIP Line buffer address initial offset value.	
	-	1:0	Reserved.	
07h (2F0Eh)	**REG2F0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIP_STATUS_DBL	7	PIP status double buffer.	

OP1PIP Register (Bank = 2F, Sub-Bank = 08)

Index (Absolute)	Mnemonic	Bit	Description	
	MSK_VDOWN_TUNE	6	PIP PosVDown mask when tuning.	
	-	5:2	Reserved.	
	FBL_PIP_A42VLEN	1	PIP FBL mask signal control.	
	PIP_ATP_KEEP	0	PIP auto tune keep old path.	
09h (2F13h)	-	7:0	Default : -	Access : -
	-	7:4	Reserved.	
0Ah (2F14h)	REG2F15	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	PIP_ATP_EN	0	PIP auto tune enable.	
0Ah (2F15h)	-	7:0	Default : -	Access : -
	-	7:4	Reserved.	
0Bh (2F16h)	REG2F16	7:0	Default : 0x00	Access : R/W
	PIP_AL[7:0]	7:0	PIP align value.	
0Bh (2F17h)	REG2F17	7:0	Default : 0x00	Access : R/W
	PIP_A[7:0]	7:0	PIP A overlap.	
0Ch (2F18h)	-	7:0	Default : -	Access : -
	-	7:4	Reserved.	
0Dh (2F1Ah)	REG2F1A	7:0	Default : 0x00	Access : R/W
	PIP_X[7:0]	7:0	PIP X position reported.	
0Dh (2F1Bh)	REG2F1B	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	PIP_X[10:8]	2:0	Please see description of '2F1Ah'.	
0Eh (2F1Ch)	REG2F1C	7:0	Default : 0x00	Access : R/W
	PIP_X_FOR_READ[7:0]	7:0	PIP X for software read.	
0Eh (2F1Dh)	REG2F1D	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	PIP_X_FOR_READ[10:8]	2:0	Please see description of '2F1Ch'.	
10h (2F20h)	REG2F20	7:0	Default : 0x00	Access : R/W
	PIP_Y[7:0]	7:0	PIP Y position reported.	
10h (2F21h)	REG2F21	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	PIP_Y[10:8]	2:0	Please see description of '2F20h'.	
11h	REG2F22	7:0	Default : 0x00	Access : R/W

OP1PIP Register (Bank = 2F, Sub-Bank = 08)

Index (Absolute)	Mnemonic	Bit	Description	
(2F22h)	PIP_Y_FOR_READ[7:0]	7:0	PIP Y for software read.	
11h (2F23h)	REG2F23	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	PIP_Y_FOR_READ[10:8]	2:0	Please see description of '2F22h'.	
12h (2F24h)	REG2F24	7:0	Default : 0x00	Access : R/W
	PIP_SVP[7:0]	7:0	PIP SVP reported.	
12h (2F25h)	REG2F25	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	PIP_SVP[10:8]	2:0	Please see description of '2F24h'.	
13h (2F26h)	REG2F26	7:0	Default : 0x00	Access : R/W
	SVP_FOR_READ[7:0]	7:0	PIP SVP for software read.	
13h (2F27h)	REG2F27	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	SVP_FOR_READ[10:8]	2:0	Please see description of '2F26h'.	
14h (2F28h)	REG2F28	7:0	Default : 0x00	Access : R/W
	PIP_SVQ[7:0]	7:0	PIP SVQ reported.	
14h (2F29h)	REG2F29	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	PIP_SVQ[11:8]	3:0	Please see description of '2F28h'.	
15h (2F2Ah)	REG2F2A	7:0	Default : 0x00	Access : R/W
	PIP_SVQ_FOR_READ[7:0]	7:0	PIP SVQ for software read.	
15h (2F2Bh)	REG2F2B	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	PIP_SVQ_FOR_READ[10:8]	2:0	Please see description of '2F2Ah'.	
16h (2F2Ch)	REG2F2C	7:0	Default : 0x00	Access : R/W
	PIP_SVR[7:0]	7:0	PIP SVR reported.	
16h (2F2Dh)	REG2F2D	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	PIP_SVR[10:8]	2:0	Please see description of '2F2Ch'.	
17h (2F2Eh)	REG2F2E	7:0	Default : 0x00	Access : R/W
	PIP_SVR_FOR_READ[7:0]	7:0	PIP SVR for software read.	
17h (2F2Fh)	REG2F2F	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	

OP1PIP Register (Bank = 2F, Sub-Bank = 08)

Index (Absolute)	Mnemonic	Bit	Description	
	PIP_SVR_FOR_READ[10:8]	2:0	Please see description of '2F2Eh'.	
18h (2F30h)	REG2F30	7:0	Default : 0x00	Access : R/W
	PIP_SVPM[7:0]	7:0	PIP SVPM reported.	
18h (2F31h)	REG2F31	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	PIP_SVPM[10:8]	2:0	Please see description of '2F30h'.	
19h (2F32h)	REG2F32	7:0	Default : 0x00	Access : R/W
	PIP_SVPM_FOR_READ[7:0]	7:0	PIP SVPM for software read.	
19h (2F33h)	REG2F33	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	PIP_SVPM_FOR_READ[10:8]	2:0	Please see description of '2F32h'.	
1Ah (2F34h)	REG2F34	7:0	Default : 0x00	Access : R/W
	PIP_SVQM[7:0]	7:0	PIP SVQM reported.	
1Ah (2F35h)	REG2F35	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	PIP_SVQM[10:8]	2:0	Please see description of '2F34h'.	
1Bh (2F36h)	REG2F36	7:0	Default : 0x00	Access : R/W
	PIP_SVQM_FOR_READ[7:0]	7:0	PIP SVQM for software read.	
1Bh (2F37h)	REG2F37	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	PIP_SVQM_FOR_READ[10:8]	2:0	Please see description of '2F36h'.	
1Ch (2F38h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
1Ch (2F39h)	REG2F39	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	PIP_MO[1:0]	1:0	PIP modulus selection.	
1Dh (2F3Ah)	REG2F3A	7:0	Default : 0x00	Access : R/W
	PIP_CD[7:0]	7:0	PIP address C diff.	
1Eh (2F3Ch)	REG2F3C	7:0	Default : 0x00	Access : R/W
	PIP_2S_OSET[7:0]	7:0	PIP 2 sides offset.	
1Eh (2F3Dh)	REG2F3D	7:0	Default : 0x00	Access : R/W
	PIP_2SIDE_EN	7	PIP 2 sides enable.	
	PIP_ATP_NO_BUF	6	PIP auto position no double buffer for enable bit.	

OP1PIP Register (Bank = 2F, Sub-Bank = 08)

Index (Absolute)	Mnemonic	Bit	Description	
	-	5:4	Reserved.	
	PIP_2S_OSET[11:8]	3:0	Please see description of '2F3Ch'.	
1Fh (2F3Eh)	REG2F3E	7:0	Default : 0x00	Access : R/W
	PIP_HFAC[7:0]	7:0	PIP H fraction.	
1Fh (2F3Fh)	REG2F3F	7:0	Default : 0x00	Access : R/W
	PIP_HFAC[15:8]	7:0	Please see description of '2F3Eh'.	
20h (2F40h)	REG2F40	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	PIP_HSHIFT	4	PIP H integer.	
	PIP_HFAC[19:16]	3:0	Please see description of '2F3Eh'.	
21h (2F42h)	REG2F42	7:0	Default : 0x00	Access : R/W
	PIP_HFAC_SW[7:0]	7:0	PIP H fraction for software read.	
21h (2F43h)	REG2F43	7:0	Default : 0x00	Access : R/W
	PIP_HFAC_SW[15:8]	7:0	Please see description of '2F42h'.	
22h (2F44h)	REG2F44	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	PIP_HFAC_SW[19:16]	3:0	Please see description of '2F42h'.	
23h (2F46h)	REG2F46	7:0	Default : 0x00	Access : R/W
	PIP_OFFSET[7:0]	7:0	Offset B.	
23h (2F47h)	REG2F47	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	PIP_OFFSET[10:8]	2:0	Please see description of '2F46h'.	
24h (2F48h)	REG2F48	7:0	Default : 0x00	Access : R/W
	PIP_OFFSET_FOR_READ[7:0]	7:0	PIP offset B for software read.	
24h (2F49h)	REG2F49	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	PIP_OFFSET_FOR_READ[10:8]	2:0	Please see description of '2F48h'.	
25h (2F4Ah)	REG2F4A	7:0	Default : 0x00	Access : R/W
	F1A[7:0]	7:0	PIP F1A reported.	
25h (2F4Bh)	REG2F4B	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	F1A[10:8]	2:0	Please see description of '2F4Ah'.	
26h	REG2F4C	7:0	Default : 0x00	Access : R/W

OP1PIP Register (Bank = 2F, Sub-Bank = 08)

Index (Absolute)	Mnemonic	Bit	Description	
(2F4Ch)	F1A_FOR_READ[7:0]	7:0	PIP F1A for software read.	
26h (2F4Dh)	REG2F4D	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	F1A_FOR_READ[10:8]	2:0	Please see description of '2F4Ch'.	
27h (2F4Eh)	REG2F4E	7:0	Default : 0x00	Access : R/W
	F1AA[7:0]	7:0	PIP F1AA reported.	
27h (2F4Fh)	REG2F4F	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	F1AA[10:8]	2:0	Please see description of '2F4Eh'.	
28h (2F50h)	REG2F50	7:0	Default : 0x00	Access : R/W
	F1AA_FOR_READ[7:0]	7:0	PIP F1AA for software read.	
28h (2F51h)	REG2F51	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	F1AA_FOR_READ[10:8]	2:0	Please see description of '2F50h'.	
29h (2F52h)	REG2F52	7:0	Default : 0x00	Access : R/W
	F1B[7:0]	7:0	PIP F1B reported.	
29h (2F53h)	REG2F53	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	F1B[10:8]	2:0	Please see description of '2F52h'.	
2Ah (2F54h)	REG2F54	7:0	Default : 0x00	Access : R/W
	F1B_FOR_READ[7:0]	7:0	PIP F1B for software read.	
2Ah (2F55h)	REG2F55	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	F1B_FOR_READ[10:8]	2:0	Please see description of '2F54h'.	
2Bh (2F56h)	REG2F56	7:0	Default : 0x00	Access : R/W
	F2A[7:0]	7:0	PIP F2A reported.	
2Bh (2F57h)	REG2F57	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	F2A[10:8]	2:0	Please see description of '2F56h'.	
2Ch (2F58h)	REG2F58	7:0	Default : 0x00	Access : R/W
	F2A_FOR_READ[7:0]	7:0	PIP F2A for software read.	
2Ch (2F59h)	REG2F59	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	

OP1PIP Register (Bank = 2F, Sub-Bank = 08)

Index (Absolute)	Mnemonic	Bit	Description	
	F2A_FOR_READ[10:8]	2:0	Please see description of '2F58h'.	
2Dh (2F5Ah)	REG2F5A	7:0	Default : 0x00	Access : R/W
	F2AA[7:0]	7:0	PIP F2AA reported.	
2Dh (2F5Bh)	REG2F5B	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	F2AA[10:8]	2:0	Please see description of '2F5Ah'.	
2Eh (2F5Ch)	REG2F5C	7:0	Default : 0x00	Access : R/W
	F2AA_FOR_READ[7:0]	7:0	PIP F2AA for software read.	
2Eh (2F5Dh)	REG2F5D	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	F2AA_FOR_READ[10:8]	2:0	Please see description of '2F5Ch'.	
2Fh (2F5Eh)	REG2F5E	7:0	Default : 0x00	Access : R/W
	F2B[7:0]	7:0	PIP F2B reported.	
2Fh (2F5Fh)	REG2F5F	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	F2B[10:8]	2:0	Please see description of '2F5Eh'.	
30h (2F60h)	REG2F60	7:0	Default : 0x00	Access : R/W
	F2B_FOR_READ[7:0]	7:0	PIP F2B for software read.	
30h (2F61h)	REG2F61	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	F2B_FOR_READ[10:8]	2:0	Please see description of '2F60h'.	
31h (2F62h)	REG2F62	7:0	Default : 0x00	Access : R/W
	DIS_ATVLEN1L	7	Auto vertical length minus 1 isable.	
	-	6:5	Reserved.	
	OVL_VED_SUB[4:0]	4:0	For PIP_MFETCH to become Big A.	
31h (2F63h)	REG2F63	7:0	Default : 0x00	Access : R/W
	ELA_WBM[7:0]	7:0	ELA WB clear mask.	
32h (2F64h)	REG2F64	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	OVL_NEW	6	0: Keep old. 1: New.	
	OVL_MSK_F2	5	OVL mask target F2.	
	OVL_MSK_F1	4	OVL mask target F1.	

OP1PIP Register (Bank = 2F, Sub-Bank = 08)

Index (Absolute)	Mnemonic	Bit	Description	
	SUB_MSK_F2_SEL	3	Window leaving mask F2 selection.	
	SUB_MSK_F1_SEL	2	Window leaving mask F1 selection.	
	OVL_WOP2MSK_F2	1	OVL WOP2 mask F2 selection.	
	OVL_WOP2MSK_F1	0	OVL WOP2 mask F1 selection.	
33h (2F66h)	REG2F66	7:0	Default : 0x00	Access : R/W
	SYNC_MIU_OP1	7	OP1 fetch count using MIU fetch count.	
	-	6:5	Reserved.	
	NOSIGNAL_OP1_MSK	4	Mask no signal for OP1.	
	OVL_WBM[3:0]	3:0	OVL write back mask.	
33h (2F67h)	REG2F67	7:0	Default : 0x00	Access : R/W
	FCLK_GWAITCNT_MSB	7	FCLK gating wait counter for power saving (MSB).	
	-	6:5	Reserved.	
	DIS_WB_ODD	4	Disable write back for odd case.	
	UV_LOAD_EN	3	UV load enable for odd case.	
	UV_LOAD_POL	2	UV load polarity selection.	
	SPDUP_PC_F2	1	Speed up F2 for 444 mode.	
	SPDUP_PC_F1	0	Speed up F1 for 444 mode.	
35h (2F6Ah)	REG2F6A	7:0	Default : 0x00	Access : R/W
	FL_VMSK_OFF	7	FL vertical mask disable.	
	-	6:0	Reserved.	
36h (2F6Ch)	REG2F6C	7:0	Default : 0x00	Access : R/W
	PIP_ATP1[7:0]	7:0	PIP ATP1 reported.	
36h (2F6Dh)	REG2F6D	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	PIP_ATP1[10:8]	2:0	Please see description of '2F6Ch'.	
37h (2F6Eh)	REG2F6E	7:0	Default : 0x00	Access : R/W
	PIP_ATP2[7:0]	7:0	PIP ATP2 reported.	
37h (2F6Fh)	REG2F6F	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	PIP_ATP2[10:8]	2:0	Please see description of '2F6Eh'.	
38h (2F70h)	REG2F70	7:0	Default : 0x00	Access : R/W
	PIP_ATP3[7:0]	7:0	PIP ATP3 reported.	
38h	REG2F71	7:0	Default : 0x00	Access : R/W

OP1PIP Register (Bank = 2F, Sub-Bank = 08)

Index (Absolute)	Mnemonic	Bit	Description	
(2F71h)	-	7:3	Reserved.	
	PIP_ATP3[10:8]	2:0	Please see description of '2F70h'.	
39h (2F72h)	REG2F72	7:0	Default : 0x00	Access : R/W
	PIP_ATP4[7:0]	7:0	PIP ATP4 reported.	
39h (2F73h)	REG2F73	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	PIP_ATP4[10:8]	2:0	Please see description of '2F72h'.	
3Ah (2F74h)	REG2F74	7:0	Default : 0x00	Access : R/W
	PIP_ATP5[7:0]	7:0	PIP ATP5 reported.	
3Ah (2F75h)	REG2F75	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	PIP_ATP5[10:8]	2:0	Please see description of '2F74h'.	
3Bh (2F76h)	REG2F76	7:0	Default : 0x00	Access : R/W
	PIP_ATP6[7:0]	7:0	PIP ATP6 reported.	
3Bh (2F77h)	REG2F77	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	PIP_ATP6[10:8]	2:0	Please see description of '2F76h'.	
3Ch (2F78h)	REG2F78	7:0	Default : 0x00	Access : R/W
	PIP_ATP7[7:0]	7:0	PIP ATP7 reported.	
3Ch (2F79h)	REG2F79	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	PIP_ATP7[10:8]	2:0	Please see description of '2F78h'.	
3Dh (2F7Ah)	REG2F7A	7:0	Default : 0x00	Access : R/W
	PIP_ATP8[7:0]	7:0	PIP ATP8 reported.	
3Dh (2F7Bh)	REG2F7B	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	PIP_ATP8[10:8]	2:0	Please see description of '2F7Ah'.	
3Eh (2F7Ch)	REG2F7C	7:0	Default : 0x00	Access : R/W
	PIP_ATP9[7:0]	7:0	PIP ATP9 reported.	
3Eh (2F7Dh)	REG2F7D	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	PIP_ATP9[10:8]	2:0	Please see description of '2F7Ch'.	
3Fh	REG2F7E	7:0	Default : 0x00	Access : R/W

OP1PIP Register (Bank = 2F, Sub-Bank = 08)

Index (Absolute)	Mnemonic	Bit	Description	
(2F7Eh)	PIP_ATP10[7:0]	7:0	PIP ATP10 reported.	
3Fh (2F7Fh)	REG2F7F	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	PIP_ATP10[10:8]	2:0	Please see description of '2F7Eh'.	
40h (2F80h)	REG2F80	7:0	Default : 0x00	Access : R/W
	PIP_ATP11[7:0]	7:0	PIP ATP11 reported.	
40h (2F81h)	REG2F81	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	PIP_ATP11[10:8]	2:0	Please see description of '2F80h'.	

OP1AH Register (Bank = 2F, Sub-Bank = 09)

Index (Absolute)	Mnemonic	Bit	Description	
05h (2F0Ah)	REG2F0A	7:0	Default : 0x00	Access : R/W
	SW_TDDI_DE_PIPE[1:0]	7:6	Sub window TDDI data enable pipe control.	
	TDDI_DE_PIPE[1:0]	5:4	TDDI data enable pipe control.	
	-	3:2	Reserved.	
	POSCBVDOWN_FIX	1	POSCBVDOWN_FIX for POS_CBVDOWN mode.	
	POSVD_MSK	0	POSVD_MASK for POS_VDOWN mode.	
09h (2F12h)	REG2F12	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	POSVDOWN_FIX2	1	POSVDOWN_FIX2 for POS_VDOWN mode.	
	POSVDOWN_FIX1	0	POSVDOWN_FIX1 for POS_VDOWN mode.	
0Fh (2F1Eh)	REG2F1E	7:0	Default : -	Access : RO
	OP1_OVER	7	OP request status reported.	
	-	6:0	Reserved.	
17h (2F2Eh)	REG2F2E	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	MSKY_EN	6	Mask Y for offset B enable.	
	-	5:0	Reserved.	
3Ch	REG2F78	7:0	Default : 0x00	Access : R/W

OP1AH Register (Bank = 2F, Sub-Bank = 09)

Index (Absolute)	Mnemonic	Bit	Description	
(2F78h)	-	7:3	Reserved.	
	SCALEUPV_POL	2	V scale up polarity select.	
	SCALEUPV_BK_SEL	1	V scale up bank select.	
	SCALEUPV_OEMD_EN	0	V scale up OE mode enable.	
3Dh (2F7Ah)	REG2F7A	7:0	Default : 0x00	Access : R/W
	YRAMV_SEL_OE	7	Y/G vertical scaling SRAM select. 0: SRAM 1. 1: SRAM 2.	
	YRAMV_EN_OE	6	Y/G vertical scaling using SRAM. 0: Disable. 1: Enable.	
	CRAMV_SEL_OE	5	C/RB Vertical Scaling SRAM Select. 0: SRAM 1. 1: SRAM 2.	
	CRAMV_EN_OE	4	C/RB vertical scaling using SRAM. 0: Disable. 1: Enable.	
	MDV_OE[3:0]	3:0	Mode V.	
43h (2F86h)	REG2F86	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	NOSIGNAL_OP1_MSK	4	Mask no signal for OP1.	
	-	3:0	Reserved.	
70h (2FE0h)	REG2FE0	7:0	Default : 0x00	Access : R/W
	HTOTAL_EXTEND_L[7:0]	7:0	H total extend[7:0].	
71h (2FE2h)	REG2FE2	7:0	Default : 0x00	Access : R/W
	HTOT_EXT_EN	7	H total extend enable.	
	-	6:4	Reserved.	
	HTOTAL_EXTEND_H[3:0]	3:0	H total extend[11:8].	
72h (2FE4h)	REG2FE4	7:0	Default : 0x00	Access : R/W
	EXTLINE_U1[3:0]	7:4	Before extend line base on F1 window start.	
	EXTLINE_D1[3:0]	3:0	After extend line base on F1 window start.	
73h (2FE6h)	REG2FE6	7:0	Default : 0x00	Access : R/W
	EXTLINE_U2[3:0]	7:4	Before extend line base on F1 window end.	
	EXTLINE_D2[3:0]	3:0	After extend line base on F1 window end.	

OP1AH Register (Bank = 2F, Sub-Bank = 09)

Index (Absolute)	Mnemonic	Bit	Description	
74h (2FE8h)	REG2FE8	7:0	Default : 0x00	Access : R/W
	HFDEEND_EXTEND_L[7:0]	7:0	H FDE end extend [7:0].	
75h (2FEAh)	REG2FEA	7:0	Default : 0x00	Access : R/W
	HFDEEND_EXT_EN	7	H FDE end extend enable.	
	-	6:4	Reserved.	
	HFDEEND_EXTEND_H[3:0]	3:0	H FDE end extend.	
76h (2FECh)	REG2FEC	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	VIP_PSEUDO_EN	0	VIP pseudo DE enable.	
78h (2FF0h)	REG2FF0	7:0	Default : 0x00	Access : R/W
	SW_OP2RQ_START_AHEAD[7:0]	7:0	Sub window OP2 request start ahead numbers.	
79h (2FF2h)	REG2FF2	7:0	Default : 0x00	Access : R/W
	SW_OP2RQ_END_AHEAD[7:0]	7:0	Sub window OP2 request end ahead numbers.	
7Ah (2FF4h)	REG2FF4	7:0	Default : 0x00	Access : R/W
	OP2RQ_START_AHEAD[7:0]	7:0	OP2 request start ahead numbers.	
7Bh (2FF6h)	REG2FF6	7:0	Default : 0x00	Access : R/W
	OP2RQ_END_AHEAD[7:0]	7:0	OP2 request end ahead numbers.	
7Dh (2FFAh)	REG2F78	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	SW_SCALEUPV_POL	2	Sub window V scale up polarity select.	
	SW_SCALEUPV_BK_SEL	1	Sub window V scale up bank select.	
	SW_SCALEUPV_OEMD_EN	0	Sub window V scale up OE mode enable.	
7Eh (2FFCh)	REG2F7A	7:0	Default : 0x00	Access : R/W
	SW_YRAMV_SEL_OE	7	Sub window Y/G vertical scaling SRAM select. 0: SRAM 1. 1: SRAM 2.	
	SW_YRAMV_EN_OE	6	Sub window Y/G vertical scaling using SRAM. 0: Disable. 1: Enable.	
	SW_CRAMV_SEL_OE	5	Sub window C/RB vertical scaling SRAM select. 0: SRAM 1. 1: SRAM 2.	

OP1AH Register (Bank = 2F, Sub-Bank = 09)

Index (Absolute)	Mnemonic	Bit	Description
	SW_CRAMV_EN_OE	4	Sub window C/RB vertical scaling using SRAM. 0: Disable. 1: Enable.
	SW_MDV_OE[3:0]	3:0	Sub window mode V.

OP1_ZZ Register (Bank = 2F, Sub-Bank = 0A)

Index (Absolute)	Mnemonic	Bit	Description	
03h (2F06h)	REG2F06	7:0	Default : 0x00	Access : R/W
	RATIO_EODI_A2_MSK[7:4]	7:4	Ratio EODi A2 mask in 3DDI protect mode.	
	TDDI_FMEG_EN_Y_FB2	3	3DDi frame/edge mode enable for main window on Y.	
	TDDI_FMEG_EN_Y_FB1	2	3DDi frame/edge mode enable for sub on Y.	
	TDDI_FMEG_EN_C_FB2	1	3DDi frame/edge mode enable.	
	TDDI_FMEG_EN_C_FB1	0	3DDi frame/edge mode enable for sub on C.	
04h (2F08h)	REG2F08	7:0	Default : 0x00	Access : R/W
	PRO_BOND_3DDI	7	3DDi protect.	
	EN_FILM_ZZRM	6	Enable zigzag removing function in film mode.	
	EN_LOCALMIN22	5	Enable local minimum check when checking un-match condition in film22.	
	EN_LOCALMIN32	4	Enable local minimum check when checking un-match condition in film32.	
	F22_SETBACK_ANYWAY	3	Enable un-match check in locking film22.	
	F32_SETBACK_ANYWAY	2	Enable un-match check in locking film32.	
	EN_FILM32CNT_FRONT	1	Enable pre MIU film32 counter.	
	EN_HIGH_FREQ_DETECT	0	Enable horizontal high freq. detect when calculating motion.	
05h (2F0Ah)	REG2F0A	7:0	Default : 0x00	Access : R/W
	EN_MIN_RATIO	7	Enable minimum motion ratio mode.	
	REG_EN_100I_FB2	6	Enable FRCx2 3DDI blending on main.	
	REG_EN_100I_FB1	5	Enable FRCx2 3DDI blending on sub.	
	DET_FIELD_SEL_LC	4	0: Select LY line buffer in field detection. 1: Select LC line buffer in field detection.	
	-	3	Reserved.	

OP1_ZZ Register (Bank = 2F, Sub-Bank = 0A)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	EN_SW_FILM22	2	Enable software controlling film22.
	EN_SW_FILM32	1	Enable software controlling film32.
	EN_STATIC_ANALYSIS	0	Enable static analysis function.
06h (2F0Ch)	REG2F0C	7:0	Default : 0x00	Access : R/W
	FD_MOT_PIXTH_MIN_F32[7:0]	7:0	Pixel minimum threshold for checking FD_UNMATCH in film32.
07h (2F0Eh)	REG2F0E	7:0	Default : 0x00	Access : R/W
	FD_MOT_PIXTH_MAX_F32[7:0]	7:0	Pixel maximum threshold for checking FD_UNMATCH in film32.
08h (2F10h)	REG2F10	7:0	Default : 0x00	Access : R/W
	FD_MOT_PIXTH_MIN_F22[7:0]	7:0	Pixel minimum threshold for checking FD_UNMATCH in film22.
09h (2F12h)	REG2F12	7:0	Default : 0x00	Access : R/W
	FD_MOT_PIXTH_MAX_F22[7:0]	7:0	Pixel maximum threshold for checking FD_UNMATCH in film22.
0Ah (2F14h)	REG2F14	7:0	Default : 0x00	Access : R/W
	FD_MOT_PIXTH_MIN_FZZ[7:0]	7:0	Pixel minimum threshold for detecting zigzag.
0Bh (2F16h)	REG2F16	7:0	Default : 0x00	Access : R/W
	FD_MOT_PIXTH_MAX_FZZ[7:0]	7:0	Pixel maximum threshold for detecting zigzag.
0Ch (2F18h)	REG2F18	7:0	Default : 0x00	Access : R/W
	FD_MOT_CNTTH_F32[7:0]	7:0	Frame count threshold for checking FD_UNMATCH in film32.
0Dh (2F1Ah)	REG2F1A	7:0	Default : 0x00	Access : R/W
	FD_MOT_CNTTH_F22[7:0]	7:0	Frame count threshold for checking FD_UNMATCH in film22.
0Eh (2F1Ch)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.

EODI Register (Bank = 2F, Sub-Bank = 0B)

EODI Register (Bank = 2F, Sub-Bank = 0B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Fh (2F1Eh)	REG2F1E	7:0	Default : 0x12	Access : R/W
	-	7:2	Reserved.	
	RLN_AVG_OUT	1	1: Real line force vertical interpolation. 0: Real line also pass EODi engine.	
	WB_ADDR_DIV2	0	WB SRAM initial address divided by 2.	
10h ~ 1Eh (2F20h ~ 2F3Ch)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
1Fh (2F3Eh)	REG2F3E	7:0	Default : 0x40	Access : R/W
	M_EODI_EN	7	Main window EODi enable. 1: Enable. 0: Disable.	
	M_WB_DISABLE	6	Main window WB disabled in up-scaling non-carry period 1: Disable in up-scaling non-carry period. 0: Enable all time.	
	-	5:0	Reserved.	
1Fh ~ 4Eh (2F3Fh ~ 2F9Ch)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
4Fh (2F9Eh)	REG2F9E	7:0	Default : 0x40	Access : R/W
	S_EODI_EN	7	Sub window EODi enable. 1: Enable. 0: Disable.	
	-	6	Reserved.	
	-	5:0	Reserved.	

SNR Register (Bank = 2F, Sub-Bank = 0C)

SNR Register (Bank = 2F, Sub-Bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (2F20h)	REG2F20	7:0	Default : 0x00	Access : R/W
	DBK_TEST_EN	7	De-blocking test mode.	
	DBK_EN_V_F1	6	Vertical de-blocking enable F1.	
	DBK_EN_H_F1	5	Horizontal de-blocking enable F1.	
	DBK_EN_F1	4	De-blocking enable F1.	
	-	3	Reserved.	
	DBK_EN_V_F2	2	Vertical de-blocking enable F2.	
	DBK_EN_H_F2	1	Horizontal de-blocking enable F2.	
	DBK_EN_F2	0	De-blocking enable F2.	
10h (2F21h)	REG2F21	7:0	Default : 0x05	Access : R/W
	DBK_STD_LOW_THRD[7:0]	7:0	De-blocking active threshold.	
11h (2F22h)	REG2F22	7:0	Default : 0x10	Access : R/W
	DBK_ALPHA_STEP[2:0]	7:5	De-blocking alpha step.	
	DBK_STRN_GAIN_F2[4:0]	4:0	De-blocking strength F2.	
11h (2F23h)	REG2F23	7:0	Default : 0x10	Access : R/W
	-	7:5	Reserved.	
	DBK_STRN_GAIN_F1[4:0]	4:0	De-blocking strength F1.	
12h (2F24h)	REG2F24	7:0	Default : 0x00	Access : R/W
	DBK_H_CONSTANT_1[7:0]	7:0	PIP Section B fine tune constant[7:0].	
12h (2F25h)	REG2F25	7:0	Default : 0x00	Access : R/W
	DBK_H_CONSTANT_2[7:0]	7:0	PIP Section B fine tune constant[15:8].	
13h (2F26h)	REG2F26	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	DBK_H_CONSTANT_3[3:0]	3:0	PIP Section B fine tune constant[19:16].	
13h (2F27h)	REG2F27	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	DBK_H_CONSTANT_4[4:0]	4:0	PIP Section B fine tune constant[24:20].	
14h (2F28h)	REG2F28	7:0	Default : 0xEF	Access : R/W
	DBK_TABLE_01[7:0]	7:0	De-blocking LUT_01.	
14h (2F29h)	REG2F29	7:0	Default : 0xCD	Access : R/W
	DBK_TABLE_23[7:0]	7:0	De-blocking LUT_23.	

SNR Register (Bank = 2F, Sub-Bank = 0C)

Index (Absolute)	Mnemonic	Bit	Description	
15h (2F2Ah)	REG2F2A	7:0	Default : 0xAB	Access : R/W
	DBK_TABLE_45[7:0]	7:0	De-blocking LUT_45.	
15h (2F2Bh)	REG2F2B	7:0	Default : 0x89	Access : R/W
	DBK_TABLE_67[7:0]	7:0	De-blocking LUT_67.	
16h (2F2Ch)	REG2F2C	7:0	Default : 0x67	Access : R/W
	DBK_TABLE_89[7:0]	7:0	De-blocking LUT_89.	
16h (2F2Dh)	REG2F2D	7:0	Default : 0x45	Access : R/W
	DBK_TABLE_AB[7:0]	7:0	De-blocking LUT_AB.	
17h (2F2Eh)	REG2F2E	7:0	Default : 0x23	Access : R/W
	DBK_TABLE_CD[7:0]	7:0	De-blocking LUT_CD.	
17h (2F2Fh)	REG2F2F	7:0	Default : 0x01	Access : R/W
	DBK_TABLE_EF[7:0]	7:0	De-blocking LUT_EF.	
18h (2F30h)	REG2F30	7:0	Default : 0x00	Access : R/W
	DBK_H_INIT_1_F2[7:0]	7:0	De-blocking H counter initial value[7:0] F2.	
18h (2F31h)	REG2F31	7:0	Default : 0x00	Access : R/W
	DBK_H_INIT_2_F2[7:0]	7:0	De-blocking H counter initial value[15:8] F2.	
19h (2F32h)	REG2F32	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	DBK_H_INIT_3_F2[3:0]	3:0	De-blocking H counter initial value[19:16] F2.	
19h (2F33h)	REG2F33	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	DBK_H_INIT_4_F2[4:0]	4:0	De-blocking H counter initial value[24:20] F2.	
1Ah (2F34h)	REG2F34	7:0	Default : 0x00	Access : R/W
	DBK_V_INIT_1_F2[7:0]	7:0	De-blocking V counter initial value[7:0] F2.	
1Ah (2F35h)	REG2F35	7:0	Default : 0x00	Access : R/W
	DBK_V_INIT_2_F2[7:0]	7:0	De-blocking V counter initial value[15:8] F2.	
1Bh (2F36h)	REG2F36	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	DBK_V_INIT_3_F2[3:0]	3:0	De-blocking V counter initial value[19:16] F2.	
1Bh (2F37h)	REG2F37	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	DBK_V_INIT_4_F2[4:0]	4:0	De-blocking V counter initial value[24:20] F2.	
1Ch	REG2F38	7:0	Default : 0x00	Access : R/W

SNR Register (Bank = 2F, Sub-Bank = 0C)

Index (Absolute)	Mnemonic	Bit	Description	
(2F38h)	DBK_H_RATIO_1_F2[7:0]	7:0	De-blocking H counter ratio[7:0] F2.	
1Ch (2F39h)	REG2F39	7:0	Default : 0x00	Access : R/W
	DBK_H_RATIO_2_F2[7:0]	7:0	De-blocking H counter ratio[15:8] F2.	
1Dh (2F3Ah)	REG2F3A	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	DBK_H_RATIO_3_F2[3:0]	3:0	De-blocking H counter ratio[19:16] F2.	
1Dh (2F3Bh)	REG2F3B	7:0	Default : 0x01	Access : R/W
	-	7:5	Reserved.	
	DBK_H_RATIO_4_F2[4:0]	4:0	De-blocking H counter ratio[24:20] F2.	
1Eh (2F3Ch)	REG2F3C	7:0	Default : 0x00	Access : R/W
	DBK_V_RATIO_1_F2[7:0]	7:0	De-blocking V counter ratio[7:0] F2.	
1Eh (2F3Dh)	REG2F3D	7:0	Default : 0x00	Access : R/W
	DBK_V_RATIO_2_F2[7:0]	7:0	De-blocking V counter ratio[15:8] F2.	
1Fh (2F3Eh)	REG2F3E	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	DBK_V_RATIO_3_F2[3:0]	3:0	De-blocking V counter ratio[19:16] F2.	
1Fh (2F3Fh)	REG2F3F	7:0	Default : 0x01	Access : R/W
	-	7:5	Reserved.	
	DBK_V_RATIO_4_F2[4:0]	4:0	De-blocking V counter ratio[24:20] F2.	
20h (2F40h)	REG2F40	7:0	Default : 0x00	Access : R/W
	DBK_H_INIT_1_F1[7:0]	7:0	De-blocking H counter initial value[7:0] F1.	
20h (2F41h)	REG2F41	7:0	Default : 0x00	Access : R/W
	DBK_H_INIT_2_F1[7:0]	7:0	De-blocking H counter initial value[15:8] F1.	
21h (2F42h)	REG2F42	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	DBK_H_INIT_3_F1[3:0]	3:0	De-blocking H counter initial value[19:16] F1.	
21h (2F43h)	REG2F43	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	DBK_H_INIT_4_F1[4:0]	4:0	De-blocking H counter initial value[24:20] F1.	
22h (2F44h)	REG2F44	7:0	Default : 0x00	Access : R/W
	DBK_V_INIT_1_F1[7:0]	7:0	De-blocking V counter initial value[7:0] F1.	
22h (2F45h)	REG2F45	7:0	Default : 0x00	Access : R/W
	DBK_V_INIT_2_F1[7:0]	7:0	De-blocking V counter initial value[15:8] F1.	

SNR Register (Bank = 2F, Sub-Bank = 0C)

Index (Absolute)	Mnemonic	Bit	Description	
23h (2F46h)	REG2F46	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	DBK_V_INIT_3_F1[3:0]	3:0	De-blocking V counter initial value[19:16] F1.	
23h (2F47h)	REG2F47	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	DBK_V_INIT_4_F1[4:0]	4:0	De-blocking V counter initial value[24:20] F1.	
24h (2F48h)	REG2F48	7:0	Default : 0x00	Access : R/W
	DBK_H_RATIO_1_F1[7:0]	7:0	De-blocking H counter ratio[7:0] F1.	
24h (2F49h)	REG2F49	7:0	Default : 0x00	Access : R/W
	DBK_H_RATIO_2_F1[7:0]	7:0	De-blocking H counter ratio[15:8] F1.	
25h (2F4Ah)	REG2F4A	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	DBK_H_RATIO_3_F1[3:0]	3:0	De-blocking H counter ratio[19:16] F1.	
25h (2F4Bh)	REG2F4B	7:0	Default : 0x01	Access : R/W
	-	7:5	Reserved.	
	DBK_H_RATIO_4_F1[4:0]	4:0	De-blocking H counter ratio[24:20] F1.	
26h (2F4Ch)	REG2F4C	7:0	Default : 0x00	Access : R/W
	DBK_V_RATIO_1_F1[7:0]	7:0	De-blocking V counter ratio[7:0] F1.	
26h (2F4Dh)	REG2F4D	7:0	Default : 0x00	Access : R/W
	DBK_V_RATIO_2_F1[7:0]	7:0	De-blocking V counter ratio[15:8] F1.	
27h (2F4Eh)	REG2F4E	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	DBK_V_RATIO_3_F1[3:0]	3:0	De-blocking V counter ratio[19:16] F1.	
27h (2F4Fh)	REG2F4F	7:0	Default : 0x01	Access : R/W
	-	7:5	Reserved.	
	DBK_V_RATIO_4_F1[4:0]	4:0	De-blocking V counter ratio[24:20] F1.	
28h (2F50h)	REG2F50	7:0	Default : 0x08	Access : R/W
	-	7:5	Reserved.	
	DBK_H_BLK_W_F2[4:0]	4:0	H block width F2.	
28h (2F51h)	REG2F51	7:0	Default : 0x08	Access : R/W
	-	7:5	Reserved.	
	DBK_V_BLK_W_F2[4:0]	4:0	V block width F2.	
29h	REG2F52	7:0	Default : 0x06	Access : R/W

SNR Register (Bank = 2F, Sub-Bank = 0C)

Index (Absolute)	Mnemonic	Bit	Description	
(2F52h)	-	7:5	Reserved.	
	DBK_H_BNDRY_LEFT_F2[4:0]	4:0	H block left boundary F2.	
29h (2F53h)	REG2F53	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	DBK_H_BNDRY_RIGHT_F2[4:0]	4:0	H block right boundary F2.	
2Ah (2F54h)	REG2F54	7:0	Default : 0x06	Access : R/W
	-	7:5	Reserved.	
	DBK_V_BNDRY_UP_F2[4:0]	4:0	V block up boundary F2.	
2Ah (2F55h)	REG2F55	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	DBK_V_BNDRY_DOWN_F2[4:0]	4:0	V block down boundary F2.	
2Ch (2F58h)	REG2F58	7:0	Default : 0x08	Access : R/W
	-	7:5	Reserved.	
	DBK_H_BLCK_W_F1[4:0]	4:0	H block width F1.	
2Ch (2F59h)	REG2F59	7:0	Default : 0x08	Access : R/W
	-	7:5	Reserved.	
	DBK_V_BLCK_W_F1[4:0]	4:0	V block width F1.	
2Dh (2F5Ah)	REG2F5A	7:0	Default : 0x06	Access : R/W
	-	7:5	Reserved.	
	DBK_H_BNDRY_L_F1[4:0]	4:0	H block left boundary F1.	
2Dh (2F5Bh)	REG2F5B	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	DBK_H_BNDRY_R_F1[4:0]	4:0	H block right boundary F1.	
2Eh (2F5Ch)	REG2F5C	7:0	Default : 0x06	Access : R/W
	-	7:5	Reserved.	
	DBK_V_BNDRY_UP_F1[4:0]	4:0	V block up boundary F1.	
2Eh (2F5Dh)	REG2F5D	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	DBK_V_BNDRY_DWN_F1[4:0]	4:0	V block down boundary F1.	
30h (2F60h)	REG2F60	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	

SNR Register (Bank = 2F, Sub-Bank = 0C)

Index (Absolute)	Mnemonic	Bit	Description	
	SNR_EN_F1	4	SNR enable F1.	
	-	3:1	Reserved.	
	SNR_EN_F2	0	SNR enable F2.	
30h (2F61h)	**REG2F61**	**7:0**	**Default : 0x0A**	**Access : R/W**
	SNR_STD_LOW_THRD[7:0]	7:0	SNR active threshold.	
31h (2F62h)	**REG2F62**	**7:0**	**Default : 0x48**	**Access : R/W**
	SNR_ALPHA_STEP[2:0]	7:5	SNR alpha step.	
	SNR_STRN_GAIN_F2[4:0]	4:0	SNR strength F2.	
31h (2F63h)	**REG2F63**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:5	Reserved.	
	SNR_STRN_GAIN_F1[4:0]	4:0	SNR strength F1.	
34h (2F68h)	**REG2F68**	**7:0**	**Default : 0xCF**	**Access : R/W**
	SNR_TABLE_01[7:0]	7:0	SNR LUT_01.	
34h (2F69h)	**REG2F69**	**7:0**	**Default : 0x69**	**Access : R/W**
	SNR_TABLE_23[7:0]	7:0	SNR LUT_23.	
35h (2F6Ah)	**REG2F6A**	**7:0**	**Default : 0x24**	**Access : R/W**
	SNR_TABLE_45[7:0]	7:0	SNR LUT_45.	
35h (2F6Bh)	**REG2F6B**	**7:0**	**Default : 0x01**	**Access : R/W**
	SNR_TABLE_67[7:0]	7:0	SNR LUT_67.	
36h (2F6Ch)	**REG2F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_TABLE_89[7:0]	7:0	SNR LUT_89.	
36h (2F6Dh)	**REG2F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_TABLE_AB[7:0]	7:0	SNR LUT_AB.	
37h (2F6Eh)	**REG2F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_TABLE_CD[7:0]	7:0	SNR LUT_CD.	
37h (2F6Fh)	**REG2F6F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_TABLE_EF[7:0]	7:0	SNR LUT_EF.	
40h (2F80h)	**REG2F80**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MOTION_RATIO_LPF_EN	6	De-flicker motion ratio low pass enable.	
	DFK_MOT_RATIO_EN_F1	5	De-flicker motion ratio enable F1.	
	DFK_EN_F1	4	De-flicker enable F1.	
	DFK_H_LPF_EN	3	De-flicker horizontal low pass enable.	

SNR Register (Bank = 2F, Sub-Bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DFK_HOR_LINE_DET_EN	2	De-flicker horizontal line detect enable.	
	DFK_MOT_RATIO_EN_F2	1	De-flicker motion ratio enable F2.	
	DFK_EN_F2	0	De-flicker enable F2.	
40h (2F81h)	**REG2F81**	**7:0**	Default : 0x40	Access : R/W
	DFK_STD_H_THRD[7:0]	7:0	De-flicker active threshold.	
41h (2F82h)	**REG2F82**	**7:0**	Default : 0x08	Access : R/W
	DFK_ALPHA_STEP[2:0]	7:5	De-flicker alpha step.	
	-	4	Reserved.	
	DFK_STRN_GAIN_F2[3:0]	3:0	De-flicker strength F2.	
41h (2F83h)	**REG2F83**	**7:0**	Default : 0x08	Access : R/W
	-	7:4	Reserved.	
	DFK_STRN_GAIN_F1[3:0]	3:0	De-flicker strength F1.	
48h (2F90h)	**REG2F90**	**7:0**	Default : 0x10	Access : R/W
	DFK_TABLE_01[7:0]	7:0	De-flicker LUT_01.	
48h (2F91h)	**REG2F91**	**7:0**	Default : 0x32	Access : R/W
	DFK_TABLE_23[7:0]	7:0	De-flicker LUT_23.	
49h (2F92h)	**REG2F92**	**7:0**	Default : 0x54	Access : R/W
	DFK_TABLE_45[7:0]	7:0	De-flicker LUT_45.	
49h (2F93h)	**REG2F93**	**7:0**	Default : 0x76	Access : R/W
	DFK_TABLE_67[7:0]	7:0	De-flicker LUT_67.	
4Ah (2F94h)	**REG2F94**	**7:0**	Default : 0x98	Access : R/W
	DFK_TABLE_89[7:0]	7:0	De-flicker LUT_89.	
4Ah (2F95h)	**REG2F95**	**7:0**	Default : 0xBA	Access : R/W
	DFK_TABLE_AB[7:0]	7:0	De-flicker LUT_AB.	
4Bh (2F96h)	**REG2F96**	**7:0**	Default : 0xDC	Access : R/W
	DFK_TABLE_CD[7:0]	7:0	De-flicker LUT_CD.	
4Bh (2F97h)	**REG2F97**	**7:0**	Default : 0xFE	Access : R/W
	DFK_TABLE_EF[7:0]	7:0	De-flicker LUT_EF.	
4Ch (2F98h)	**REG2F98**	**7:0**	Default : 0x10	Access : R/W
	MOTION_TABLE_01[7:0]	7:0	De-flicker motion ratio LUT_01.	
4Ch (2F99h)	**REG2F99**	**7:0**	Default : 0x32	Access : R/W
	MOTION_TABLE_23[7:0]	7:0	De-flicker motion ratio LUT_23.	
4Dh	**REG2F9A**	**7:0**	Default : 0x54	Access : R/W

SNR Register (Bank = 2F, Sub-Bank = 0C)

Index (Absolute)	Mnemonic	Bit	Description	
(2F9Ah)	MOTION_TABLE_45[7:0]	7:0	De-flicker motion ratio LUT_45.	
4Dh (2F9Bh)	**REG2F9B**	**7:0**	**Default : 0x76**	**Access : R/W**
	MOTION_TABLE_67[7:0]	7:0	De-flicker motion ratio LUT_67.	
4Eh (2F9Ch)	**REG2F9C**	**7:0**	**Default : 0x98**	**Access : R/W**
	MOTION_TABLE_89[7:0]	7:0	De-flicker motion ratio LUT_89.	
4Eh (2F9Dh)	**REG2F9D**	**7:0**	**Default : 0xBA**	**Access : R/W**
	MOTION_TABLE_AB[7:0]	7:0	De-flicker motion ratio LUT_AB.	
4Fh (2F9Eh)	**REG2F9E**	**7:0**	**Default : 0xDC**	**Access : R/W**
	MOTION_TABLE_CD[7:0]	7:0	De-flicker motion ratio LUT_CD.	
4Fh (2F9Fh)	**REG2F9F**	**7:0**	**Default : 0xFE**	**Access : R/W**
	MOTION_TABLE_EF[7:0]	7:0	De-flicker motion ratio LUT_EF.	

S_VOP Register (Bank = 2F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description	
01h (2F02h)	**REG2F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_BORDER_EN	7	Sub window (F1) border enable.	
	-	6:0	Reserved.	
01h (2F03h)	**REG2F03**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
02h (2F04h)	**REG2F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDLO[3:0]	7:4	Sub window border outside height of left side.	
	BDLI[3:0]	3:0	Sub window border inside height of left side.	
02h (2F05h)	**REG2F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDLO_BO[3:0]	7:4	Main window border outside height of left side.	
	BDLI_BO[3:0]	3:0	Main window inside height of left side.	
03h (2F06h)	**REG2F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDRO[3:0]	7:4	Sub window border outside height of right side.	
	BDRI[3:0]	3:0	Sub window border inside height of right side.	
03h (2F07h)	**REG2F07**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDRO_BO[3:0]	7:4	Main window border outside height of right side.	

S_VOP Register (Bank = 2F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description	
	BDRI_BO[3:0]	3:0	Main window border inside height of right side.	
04h (2F08h)	REG2F08	7:0	Default : 0x00	Access : R/W
	BDUO[3:0]	7:4	Sub window border outside width of upper side.	
	BDUI[3:0]	3:0	Sub window border inside width of upper side.	
04h (2F09h)	REG2F09	7:0	Default : 0x00	Access : R/W
	BDUO_BO[3:0]	7:4	Main window border outside width of upper side.	
	BDUI_BO[3:0]	3:0	Main window border inside width of upper side.	
05h (2F0Ah)	REG2F0A	7:0	Default : 0x00	Access : R/W
	BDDO[3:0]	7:4	Sub window border outside width of down side.	
	BDDI[3:0]	3:0	Sub window border inside width of down side.	
05h (2F0Bh)	REG2F0B	7:0	Default : 0x00	Access : R/W
	BDDO_BO[3:0]	7:4	Main window border outside width of down side.	
	BDDI_BO[3:0]	3:0	Main window border inside width of down side.	
06h (2F0Ch)	REG2F0C	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	4WINEN	6	4th window enable. 0: Disable. 1: Enable.	
	3WINEN	5	3rd window enable. 0: Disable. 1: Enable.	
	2WINEN	4	2nd window enable. 0: Disable. 1: Enable.	
	-	3:2	Reserved.	
	181FWINSEL[1:0]	1:0	18h~1Fh display window select. 00: 1st window. 01: 2nd window. 10: 3rd window. 11: 4th window.	
06h (2F0Dh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
07h (2F0Eh)	REG2F0E	7:0	Default : 0x00	Access : R/W
	S_HDEST[7:0]	7:0	Sub window horizontal start.	
07h	REG2F0F	7:0	Default : 0x00	Access : R/W

S_VOP Register (Bank = 2F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description	
(2F0Fh)	-	7:4	Reserved.	
	S_HDEST[11:8]	3:0	Please see description of '2F0Eh'.	
08h (2F10h)	REG2F10	7:0	Default : 0x00	Access : R/W
	S_HDEEND[7:0]	7:0	Sub window horizontal end.	
08h (2F11h)	REG2F11	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	S_HDEEND[11:8]	3:0	Please see description of '2F10h'.	
09h (2F12h)	REG2F12	7:0	Default : 0x00	Access : R/W
	S_VDEST[7:0]	7:0	Sub window vertical start.	
09h (2F13h)	REG2F13	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	S_VDEST[11:8]	3:0	Please see description of '2F12h'.	
0Ah (2F14h)	REG2F14	7:0	Default : 0x00	Access : R/W
	S_VDEEND[7:0]	7:0	Sub window vertical end.	
0Ah (2F15h)	REG2F15	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	S_VDEEND[11:8]	3:0	Please see description of '2F14h'.	
0Bh (2F16h)	REG2F16	7:0	Default : 0x00	Access : R/W
	S_HDEST_2ND[7:0]	7:0	2nd sub window horizontal start for MWE.	
0Bh (2F17h)	REG2F17	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	S_HDEST_2ND[11:8]	3:0	Please see description of '2F16h'.	
0Ch (2F18h)	REG2F18	7:0	Default : 0x00	Access : R/W
	S_HDEEND_2ND[7:0]	7:0	2nd sub window horizontal end for MWE.	
0Ch (2F19h)	REG2F19	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	S_HDEEND_2ND[11:8]	3:0	Please see description of '2F18h'.	
0Dh (2F1Ah)	REG2F1A	7:0	Default : 0x00	Access : R/W
	S_VDEST_2ND[7:0]	7:0	2nd sub window vertical start for MWE.	
0Dh (2F1Bh)	REG2F1B	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	S_VDEST_2ND[11:8]	3:0	Please see description of '2F1Ah'.	
0Eh	REG2F1C	7:0	Default : 0x00	Access : R/W

S_VOP Register (Bank = 2F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description	
(2F1Ch)	S_VDEEND_2ND[7:0]	7:0	2nd sub window vertical end for MWE.	
0Eh (2F1Dh)	REG2F1D	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	S_VDEEND_2ND[11:8]	3:0	Please see description of '2F1Ch'.	
0Fh (2F1Eh)	REG2F1E	7:0	Default : 0x00	Access : R/W
	S_HDEST_3RD[7:0]	7:0	3rd sub window horizontal start for MWE.	
0Fh (2F1Fh)	REG2F1F	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	S_HDEST_3RD[11:8]	3:0	Please see description of '2F1Eh'.	
10h (2F20h)	REG2F20	7:0	Default : 0x00	Access : R/W
	S_HDEEND_3RD[7:0]	7:0	3rd sub window horizontal end for MWE.	
10h (2F21h)	REG2F21	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	S_HDEEND_3RD[11:8]	3:0	Please see description of '2F20h'.	
11h (2F22h)	REG2F22	7:0	Default : 0x00	Access : R/W
	S_VDEST_3RD[7:0]	7:0	3rd sub window vertical start for MWE.	
11h (2F23h)	REG2F23	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	S_VDEST_3RD[11:8]	3:0	Please see description of '2F22h'.	
12h (2F24h)	REG2F24	7:0	Default : 0x00	Access : R/W
	S_VDEEND_3RD[7:0]	7:0	3rd sub window Vertical End for MWE.	
12h (2F25h)	REG2F25	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	S_VDEEND_3RD[11:8]	3:0	Please see description of '2F24h'.	
13h (2F26h)	REG2F26	7:0	Default : 0x00	Access : R/W
	S_HDEST_4TH[7:0]	7:0	4th sub window horizontal start for MWE.	
13h (2F27h)	REG2F27	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	S_HDEST_4TH[11:8]	3:0	Please see description of '2F26h'.	
14h (2F28h)	REG2F28	7:0	Default : 0x00	Access : R/W
	S_HDEEND_4TH[7:0]	7:0	4th sub window horizontal end for MWE.	
14h (2F29h)	REG2F29	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	

S_VOP Register (Bank = 2F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description	
	S_HDEEND_4TH[11:8]	3:0	Please see description of '2F28h'.	
15h (2F2Ah)	REG2F2A	7:0	Default : 0x00	Access : R/W
	S_VDEST_4TH[7:0]	7:0	4th sub window vertical start for MWE.	
15h (2F2Bh)	REG2F2B	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	S_VDEST_4TH[11:8]	3:0	Please see description of '2F2Ah'.	
16h (2F2Ch)	REG2F2C	7:0	Default : 0x00	Access : R/W
	S_VDEEND_4TH[7:0]	7:0	4th sub window vertical end for MWE.	
16h (2F2Dh)	REG2F2D	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	S_VDEEND_4TH[11:8]	3:0	Please see description of '2F2Ch'.	
17h (2F2Eh)	REG2F2E	7:0	Default : 0x00	Access : R/W
	SWBCOL[7:0]	7:0	Sub window border color.	
17h (2F2Fh)	REG2F2F	7:0	Default : 0x00	Access : R/W
	SWNS_COL[7:0]	7:0	Sub window no signal color.	
18h (2F30h)	REG2F30	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	SGCR	4	Sub window Gamma correction rounding function. 0: Disable. 1: Enable.	
	-	3:1	Reserved.	
	SGCB	0	Sub window Gamma correction function control. 0: Bypass gamma correction function. 1: Enable gamma correction function.	
18h (2F31h)	REG2F31	7:0	Default : 0x00	Access : R/W
	S_HBC_GAIN[3:0]	7:4	HBC gain for sub window.	
	S_HBC_EN	3	HBC function enable for sub window.	
	S_HBC_ROUNDING	2	HBC rounding enable for sub window.	
	-	1	Reserved.	
	BRC	0	Brightness function 0: Off. 1: On.	
19h ~ 1Ah (2F32h ~	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	

S_VOP Register (Bank = 2F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description	
2F35h)				
1Bh (2F36h)	REG2F36	7:0	Default : 0x00	Access : R/W
	KST_HOFFS[7:0]	7:0	Keystone horizontal position offset.	
1Bh (2F37h)	REG2F37	7:0	Default : 0x00	Access : R/W
	KST_HOFFSSN	7	Keystone horizontal position initial offset sign. 0: Positive value. 1: Negative value.	
	KST_HOFFS[14:8]	6:0	Please see description of '2F36h'.	
1Ch (2F38h)	REG2F38	7:0	Default : 0x00	Access : R/W
	KSTPD[7:0]	7:0	Keystone Horizontal position Delta per line.	
1Ch (2F39h)	REG2F39	7:0	Default : 0x00	Access : R/W
	KSTPD[15:8]	7:0	Please see description of '2F38h'.	
1Dh (2F3Ah)	REG2F3A	7:0	Default : 0x00	Access : R/W
	CM11[7:0]	7:0	Color matrix coefficient 11.	
1Dh (2F3Bh)	REG2F3B	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CM11[12:8]	4:0	Please see description of '2F3Ah'.	
1Eh (2F3Ch)	REG2F3C	7:0	Default : 0x00	Access : R/W
	CM12[7:0]	7:0	Color matrix coefficient 12.	
1Eh (2F3Dh)	REG2F3D	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CM12[12:8]	4:0	Please see description of '2F3Ch'.	
1Fh (2F3Eh)	REG2F3E	7:0	Default : 0x00	Access : R/W
	CM13[7:0]	7:0	Color matrix coefficient 13.	
1Fh (2F3Fh)	REG2F3F	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CM13[12:8]	4:0	Please see description of '2F3Eh'.	
20h (2F40h)	REG2F40	7:0	Default : 0x00	Access : R/W
	CM21[7:0]	7:0	Color matrix coefficient 21.	
20h (2F41h)	REG2F41	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CM21[12:8]	4:0	Please see description of '2F40h'.	
21h	REG2F42	7:0	Default : 0x00	Access : R/W

S_VOP Register (Bank = 2F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description	
(2F42h)	CM22[7:0]	7:0	Color matrix coefficient 22.	
21h (2F43h)	REG2F43	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CM22[12:8]	4:0	Please see description of '2F42h'.	
22h (2F44h)	REG2F44	7:0	Default : 0x00	Access : R/W
	CM23[7:0]	7:0	Color matrix coefficient 23.	
22h (2F45h)	REG2F45	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CM23[12:8]	4:0	Please see description of '2F44h'.	
23h (2F46h)	REG2F46	7:0	Default : 0x00	Access : R/W
	CM31[7:0]	7:0	Color matrix coefficient 31.	
23h (2F47h)	REG2F47	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CM31[12:8]	4:0	Please see description of '2F46h'.	
24h (2F48h)	REG2F48	7:0	Default : 0x00	Access : R/W
	CM32[7:0]	7:0	Color matrix coefficient 32.	
24h (2F49h)	REG2F49	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CM32[12:8]	4:0	Please see description of '2F48h'.	
25h (2F4Ah)	REG2F4A	7:0	Default : 0x00	Access : R/W
	CM33[7:0]	7:0	Color matrix coefficient 33.	
25h (2F4Bh)	REG2F4B	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CM33[12:8]	4:0	Please see description of '2F4Ah'.	
26h (2F4Ch)	REG2F4C	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	CMRND	5	Color matrix rounding control. 0: Disable. 1: Enable.	
	CMC	4	Color matrix control. 0: Disable. 1: Enable.	
	-	3	Reserved.	
	RRAN	2	Red range.	

S_VOP Register (Bank = 2F, Sub-Bank = 0F)					
Index (Absolute)	**Mnemonic**	**Bit**	**Description**		
			0: 0~255. 1: -128~127.		
	GRAN	1	Green range. 0: 0~255. 1: -128~127.		
	BRAN	0	Blue range. 0: 0~255. 1: -128~127.		
26h (2F4Dh)	REG2F4D	7:0	Default : 0x00	Access : R/W	
	SMEN	7	SVM main window enable.		
	SMTE	6	SVM main window tap enable.		
	SMFT[1:0]	5:4	SVM main window filter tap. 00: 2 tap. 01: 3 tap. 10: 4 tap. 11: 5 tap.		
	SSWEN	3	SVM sub window enable.		
	SSWETE	2	SVM sub window tap enable.		
	SSWFT[1:0]	1:0	SVM sub window filter Tap. 00: 2 tap. 01: 3 tap. 10: 4 tap. 11: 5 tap.		
27h (2F4Eh)	REG2F4E	7:0	Default : 0x00	Access : R/W	
	OSDY	7	OSD color space. 0: OSD color space. 1: OSD is YUV color space.		
	SINV	6	SMV polarity invert. 0: Normal. 1: Invert.		
	SVMBYS[1:0]	5:4	SVM bypass Y select. 0x: SMV data. 10: Original Y data. 11: Y with tap filter.		
	SCOR[3:0]	3:0	SVM coring.		
27h (2F4Fh)	REG2F4F	7:0	Default : 0x00	Access : R/W	
	SVMLMT[7:0]	7:0	SVM limit.		

S_VOP Register (Bank = 2F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description	
28h (2F50h)	REG2F50	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	SMSTP[2:0]	6:4	SVM main window step.	
	SMGAIN[3:0]	3:0	SVM main window gain.	
28h (2F51h)	REG2F51	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	SSWSTP[2:0]	6:4	SVM sub window step.	
	SWGAIN[3:0]	3:0	SVM sub window gain.	
29h (2F52h)	REG2F52	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	SPAJ[1:0]	6:5	SVM pipe adjust.	
	SDLYAJ[4:0]	4:0	SVM delay adjust.	
29h (2F53h)	REG2F53	7:0	Default : 0x00	Access : RO, R/W
	SVM_SEP_DLY	7	SVM separate delay enable.	
	OVERLAP_SEL[1:0]	6:5	Overlap select. 00: Average. 01: No action. 10: Keep slow down result. 11: Keep speed up result.	
	SVM_SD_DLY[4:0]	4:0	SVM slow down delay.	
2Ah (2F54h)	REG2F54	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	SBPMC	6	Scaler bypass mode control. 0: Disable. 1: Enable.	
	IPFI	5	To pad field invert enable.	
	-	4	Reserved.	
	IRDEN	3	Random 10 bit DAC enable.	
	IHSRE	2	HSYNC shift control. 0: Shift left. 1: Shift right.	
	IOFI	1	Interlace output field invert.	
	IOEN	0	Interlace output enable.	
2Bh	-	7:0	Default : -	Access : -

S_VOP Register (Bank = 2F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description	
(2F56h)	-	7:0	Reserved.	
2Bh (2F57h)	**REG2F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP_FINV	7	IP field inverse.	
	IP_ITLC	6	IP interlace.	
	-	5:4	Reserved.	
	BES[1:0]	3:2	Border extend for SVM.	
	OES[1:0]	1:0	OSD extend for SVM.	
2Ch (2F58h)	**REG2F58**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSOFFS[7:0]	7:0	HYSNC shift offset.	
2Ch (2F59h)	**REG2F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	OP1INTERLACE_OUT	7	OP1 output is interlace out mode.	
	-	6:4	Reserved.	
	HSOFFS[11:8]	3:0	Please see description of '2F58h'.	
30h (2F60h)	**REG2F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	R_BRI_OFFSET[7:0]	7:0	Offset for R data (after gamma).	
30h (2F61h)	**REG2F61**	**7:0**	**Default : 0x00**	**Access : R/W**
	BRI_EN	7	Brightness enable (after gamma).	
	CON_EN	6	Contrast enable (after gamma).	
	NOISE_ROUND_EN	5	Noise rounding enable for contrast brightness function.	
	-	4:3	Reserved.	
	R_BRI_OFFSET[10:8]	2:0	Please see description of '2F60h'.	
31h (2F62h)	**REG2F62**	**7:0**	**Default : 0x00**	**Access : R/W**
	G_BRI_OFFSET[7:0]	7:0	Offset for G data (after gamma).	
31h (2F63h)	**REG2F63**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	G_BRI_OFFSET[10:8]	2:0	Please see description of '2F62h'.	
32h (2F64h)	**REG2F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	B_BRI_OFFSET[7:0]	7:0	Offset for B data (after gamma).	
32h (2F65h)	**REG2F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	B_BRI_OFFSET[10:8]	2:0	Please see description of '2F64h'.	
33h (2F66h)	**REG2F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	R_CON_GAIN[7:0]	7:0	Contrast gain for R data.	

S_VOP Register (Bank = 2F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description	
33h (2F67h)	REG2F67	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	R_CON_GAIN[11:8]	3:0	Please see description of '2F66h'.	
34h (2F68h)	REG2F68	7:0	Default : 0x00	Access : R/W
	G_CON_GAIN[7:0]	7:0	Contrast gain for G data.	
34h (2F69h)	REG2F69	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	G_CON_GAIN[11:8]	3:0	Please see description of '2F68h'.	
35h (2F6Ah)	REG2F6A	7:0	Default : 0x00	Access : R/W
	B_CON_GAIN[7:0]	7:0	Contrast gain for B data.	
35h (2F6Bh)	REG2F6B	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	B_CON_GAIN[11:8]	3:0	Please see description of '2F6Ah'.	
36h (2F6Ch)	REG2F6C	7:0	Default : 0x00	Access : R/W
	M_BRI_R[7:0]	7:0	Brightness offset (before gamma) for main window R.	
36h (2F6Dh)	REG2F6D	7:0	Default : 0x00	Access : R/W
	SS_MD	7	Brightness offset (before gamma) range control. 0: From -1024 ~ 1023; output = input + (offset[10:0] − 1024). 1: From -512 ~ 511; output = input + (offset[9:0] − 512).	
	-	6:3	Reserved.	
	M_BRI_R[10:8]	2:0	Please see description of '2F6Ch'.	
37h (2F6Eh)	REG2F6E	7:0	Default : 0x00	Access : R/W
	M_BRI_G[7:0]	7:0	Brightness offset (before gamma) for main window G.	
37h (2F6Fh)	REG2F6F	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	M_BRI_G[10:8]	2:0	Please see description of '2F6Eh'.	
38h (2F70h)	REG2F70	7:0	Default : 0x00	Access : R/W
	M_BRI_B[7:0]	7:0	Brightness offset (before gamma) for main window B.	
38h (2F71h)	REG2F71	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	M_BRI_B[10:8]	2:0	Please see description of '2F70h'.	
39h	REG2F72	7:0	Default : 0x00	Access : R/W

S_VOP Register (Bank = 2F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description	
(2F72h)	S_BRI_R[7:0]	7:0	Brightness offset (before gamma) for sub window R.	
39h (2F73h)	REG2F73	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	S_BRI_R[10:8]	2:0	Please see description of '2F72h'.	
3Ah (2F74h)	REG2F74	7:0	Default : 0x00	Access : R/W
	S_BRI_G[7:0]	7:0	Brightness offset (before gamma) for sub window G.	
3Ah (2F75h)	REG2F75	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	S_BRI_G[10:8]	2:0	Please see description of '2F74h'.	
3Bh (2F76h)	REG2F76	7:0	Default : 0x00	Access : R/W
	S_BRI_B[7:0]	7:0	Brightness offset (before gamma) for sub window B.	
3Bh (2F77h)	REG2F77	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	S_BRI_B[10:8]	2:0	Please see description of '2F76h'.	

VOP Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
01h (2F02h)	REG2F02	7:0	Default : 0x00	Access : R/W
	HSEND0[7:0]	7:0	20h: Recommended value (power on default value is 0).	
02h (2F04h)	REG2F04	7:0	Default : 0x00	Access : R/W
	VSST[7:0]	7:0	Output VSYNC start (only useful when AOVS=1) 302h: Recommended value for XGA output (power on default value is 3 402h: Recommended value for SXGA output.	
02h (2F05h)	REG2F05	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	VSRU	3	VSYNC register usage. 0: Registers 20h _ 23h are used to define output VSYNC. 1: Registers 20h and 21h are used to define No signal VSYNC. Registers 22h and 23h are used to define minimum H total.	

VOP Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
	VSST[10:8]	2:0	Please see description of '2F04h'.	
03h (2F06h)	**REG2F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSEND[7:0]	7:0	Output VSYNC END (only useful when AOVS=1) 304h: Recommended value for XGA output (power on default value is 6). 404h: Recommended value for SXGA output.	
03h (2F07h)	**REG2F07**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	VSEND[10:8]	2:0	Please see description of '2F06h'.	
04h (2F08h)	**REG2F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEHST[7:0]	7:0	External VD using sync. 0: Sync is generated from data internally. 1: Sync from external source.	
04h (2F09h)	**REG2F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DEHST[11:8]	3:0	Please see description of '2F08h'.	
05h (2F0Ah)	**REG2F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEHEND[7:0]	7:0	Output DE horizontal end. 447h: Recommended value for XGA output (power on default value is 0). 547h: Recommended value for SXGA output.	
05h (2F0Bh)	**REG2F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DEHEND[11:8]	3:0	Please see description of '2F0Ah'.	
06h (2F0Ch)	**REG2F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEVST[7:0]	7:0	Output DE vertical start. 00: Default value.	
06h (2F0Dh)	**REG2F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSTSEL	7	Vertical start select. 0: DEVST[10:0] is output DE vertical start. 1: DEVST[10:0] is scaling image window vertical start.	
	-	6:4	Reserved.	
	DEVST[11:8]	3:0	Please see description of '2F0Ch'.	
07h (2F0Eh)	**REG2F0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEVEND[7:0]	7:0	Output DE vertical end.	

VOP Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
			2FFh: Recommended value for XGA output (power on default value is 6). 3FFh: Recommended value for SXGA output	
07h (2F0Fh)	REG2F0F	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	DEVEND[11:8]	3:0	Please see description of '2F0Eh'.	
08h (2F10h)	REG2F10	7:0	Default : 0x00	Access : R/W
	SIHST[7:0]	7:0	Scaling image window horizontal start. 48h: Recommended value (power on default is 0)	
08h (2F11h)	REG2F11	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	SIHST[11:8]	3:0	Please see description of '2F10h'.	
09h (2F12h)	REG2F12	7:0	Default : 0x00	Access : R/W
	SIHEND[7:0]	7:0	447h: Recommended value for XGA output (power on default is 0). 547h: Recommended value for SXGA output.	
09h (2F13h)	REG2F13	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	SIHEND[11:8]	3:0	Please see description of '2F12h'.	
0Ah (2F14h)	REG2F14	7:0	Default : 0x00	Access : R/W
	SIVST[7:0]	7:0	Scaling image window vertical start.	
0Ah (2F15h)	REG2F15	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	SIVST[11:8]	3:0	Please see description of '2F14h'.	
0Bh (2F16h)	REG2F16	7:0	Default : 0x00	Access : R/W
	SIVEND[7:0]	7:0	Scaling image window vertical end. 2FFh: Recommended value for XGA output (power on default value is 6). 3FFh: Recommended value for SXGA output.	
0Bh (2F17h)	REG2F17	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	SIVEND[11:8]	3:0	Please see description of '2F16h'.	
0Ch (2F18h)	REG2F18	7:0	Default : 0x00	Access : R/W
	HDTOT[7:0]	7:0	Output horizontal total.	

VOP Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
			53fh: Recommended value for XGA output (power on default value is 3). 697h: Recommended value for SXGA output.	
0Ch (2F19h)	REG2F19	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	HDTOT[11:8]	3:0	Please see description of '2F18h'.	
0Dh (2F1Ah)	REG2F1A	7:0	Default : 0x00	Access : R/W
	VDTOT[7:0]	7:0	Output vertical total. 326h: Recommended value for XGA output (power on default value is 3). 42Ah: Recommended value for SXGA output	
0Dh (2F1Bh)	REG2F1B	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	VDTOT[11:8]	3:0	Please see description of '2F1Ah'.	
10h (2F20h)	REG2F20	7:0	Default : 0x00	Access : R/W
	HSEND[7:0]	7:0	20h: Recommended value (power on default value is 0).	
10h (2F21h)	REG2F21	7:0	Default : 0x4C	Access : R/W
	AOVS	7	Auto output VSYNC. 0: OVSYNC is defined automatically. 1: OVSYNC is defined manually (register 0x20 _ 0x23).	
	OUTM	6	Output mode. 0: Mode 0. 1: Mode 1.	
	-	5:4	Reserved.	
	EHTT	3	Even H total. 0: Enable, output H total always be even pixels. 1: Disable, output H total always be odd pixels.	
	MOD2	2	Mode 2. 0: Disable. 1: Enable.	
	AHRT	1	Auto H total and read start tuning enable. 0: Disable. 1: Enable.	
	CTRL	0	ATCTRL function enable. 0: Disable. 1: Enable.	

VOP Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
11h (2F22h)	REG2F22	7:0	Default : 0x00	Access : R/W
	FPLLMD0	7	Frame PLL Mode 0.	
	SL_TUNE_EN	6	Short line tune enable.	
	-	5:2	Reserved.	
	SSC_SHIFT	1	SSC shift. 0: Enable. 1: Disable.	
	CLKDIV2_POINT_SEL	0	CLKDIV2 point select. 0: Original. 1: New.	
12h (2F24h)	REG2F24	7:0	Default : 0x20	Access : R/W
	LCK_TH[7:0]	7:0	Frame PLL lock threshold.	
12h (2F25h)	REG2F25	7:0	Default : 0x08	Access : R/W
	LCK_TH[15:8]	7:0	Please see description of '2F24h'.	
13h (2F26h)	REG2F26	7:0	Default : 0x10	Access : R/W
	FTNF[7:0]	7:0	Frame tune number of frame.	
13h (2F27h)	REG2F27	7:0	Default : 0x10	Access : R/W
	FTNS[3:0]	7:4	Tune frame number of short-line tune.	
	-	3	Reserved.	
	PIP_REG_EN	2	PIP register enable.	
	FPLL_REP_EN	1	Frame PLL report enable.	
	NOISY_GEN	0	Noise generator.	
14h (2F28h)	REG2F28	7:0	Default : 0x00	Access : R/W
	PFLL_LMT1[7:0]	7:0	Frame PLL limit.	
14h (2F29h)	REG2F29	7:0	Default : 0x00	Access : R/W
	PFLL_LMT0[7:0]	7:0	Frame PLL limit.	
15h (2F2Ah)	REG2F2A	7:0	Default : 0x00	Access : R/W
	PFLL_LMT[7:0]	7:0	Frame PLL limit.	
15h (2F2Bh)	REG2F2B	7:0	Default : 0x00	Access : R/W
	FPLL_LMT_OFST0[7:0]	7:0	Frame PLL limit offset low byte.	
16h (2F2Ch)	REG2F2C	7:0	Default : 0x00	Access : R/W
	FPLL_LMT_OFST1[7:0]	7:0	Frame PLL limit offset high byte.	
16h (2F2Dh)	REG2F2D	7:0	Default : 0xF0	Access : R/W
	M_HBC_GAIN[3:0]	7:4	Main window high brightness gain.	

VOP Register (Bank = 2F, Sub-Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	M_HBC_EN	3	Main window high brightness enable.	
	M_HBC_ROUNDING	2	Main window high brightness enable.	
	-	1	Reserved.	
	BRC	0	Brightness function. 0: Off. 1: On.	
19h **(2F32h)**	**REG2F32**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADEAD_EN	7	Ahead mode enable.	
	SWBLBK	6	Sub window blue screen color. 0: Black color. 1: Blue color.	
	SWBLUE	5	Sub window blue screen control. 0: Off. 1: On.	
	S_FMCLR_EN	4	Sub window frame color enable.	
	-	3	Reserved.	
	MBD_EN	2	Main window border enable.	
	MBLK	1	Main window black screen control. 0: Off. 1: On.	
	NOSC_EN	0	No signal color enable.	
19h **(2F33h)**	**REG2F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCL_R[7:0]	7:0	Frame color red.	
1Ah **(2F34h)**	**REG2F34**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCL_G[7:0]	7:0	Frame color green. Green	
1Ah **(2F35h)**	**REG2F35**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCL_B[7:0]	7:0	Frame color blue.	
1Bh **(2F36h)**	**REG2F36**	**7:0**	**Default : 0x02**	**Access : R/W**
	DITHG[1:0]	7:6	Dither coefficient for G channel.	
	DITHB[1:0]	5:4	Dither coefficient for B channel.	
	SROT	3	Spatial coefficient rotate. 0: Disable. 1: Enable.	
	TROT	2	Temporal coefficient rotate.	

VOP Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
			0: Disable. 1: Enable.	
	OBN	1	Output bits number (used for 8/10-bit gamma). 0: 8-bit output. 1: 6-bit output (power on default value).	
	DITH	0	Dither function. 0: Off. 1: On.	
1Bh (2F37h)	REG2F37	7:0	Default : 0x2D	Access : R/W
	TL[1:0]	7:6	Top left dither coefficient.	
	TR[1:0]	5:4	Top right dither coefficient.	
	BL[1:0]	3:2	Bottom left dither coefficient.	
	BR[1:0]	1:0	Bottom right dither coefficient.	
1Ch (2F38h)	REG2F38	7:0	Default : 0x00	Access : R/W
	RST_E_4_FRAME	7	Reset noise generator by frames enable.	
	NDMD	6	Noise dithering method.	
	DATP	5	Dither based on auto phase threshold. 0: Disable. 1: Enable.	
	DRT	4	Dither rotate type. 0: EOR. 1: Rotate.	
	DT3	3	Dither type 2 control. 0: Disable dither type 2. 1: Enable dither type 2.	
	DT2	2	Dither type 2. 0: Output data bits 1 and 0 according to input pixel value. 1: Output data bits 2, 1 and 0 according to input pixel value.	
	DT1	1	Dither type 1. 0: Normal.1: Output data bits 1 and 0 are always 00.	
	TDFNC	0	Tempo-dither frame number control. 0: Tempo-dither every frame. 1: Tempo-dither every 2 frames.	
1Ch	REG2F39	7:0	Default : 0x00	Access : R/W

VOP Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
(2F39h)	-	7	Reserved.	
	SHORT_1LINE_DISABLE	6	Short 1 line. 1: Disable. 0: Enable.	
	-	5	Reserved.	
	EGWT	4	Encode Gamma write.	
	HTOTAL	3	H total end 11.	
	HDE_END	2	HDE end 11.	
	HFDE_END	1	HFDE end 11.	
	OUTFRR_EN0	0	Output free-run enable.	
1Dh (2F3Ah)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
1Dh (2F3Bh)	REG2F3B	7:0	Default : 0x07	Access : R/W
	TUNE_FLD_IP	7	Select insert point of one field for VOP_DISP inset signal.	
	-	6:0	Reserved.	
1Eh (2F3Ch)	REG2F3C	7:0	Default : 0x00	Access : R/W
	LMT_ADD_NMB[7:0]	7:0	Limit adjust number in ACC_FPLL mode.	
1Eh (2F3Dh)	REG2F3D	7:0	Default : 0x00	Access : R/W
	FPLL_MD1	7	FPLL mode 1.	
	FPLL_DIS	6	FPLL stop.	
	-	5:3	Reserved.	
	ADD_LINE_SEL	2	Select add line into frame or pixel into line.	
	CON_BRI_SWITCH	1	Select CON_BRI function stage. 0: Before OSD. 1: After OSD.	
	-	0	Reserved.	
1Fh (2F3Eh)	REG2F3E	7:0	Default : 0x00	Access : R/W
	IVS_PRD_NUM[7:0]	7:0	Count number per input v.s.	
1Fh (2F3Fh)	REG2F3F	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	IVS_PRD_NUM[11:8]	3:0	Please see description of '2F3Eh'.	
21h (2F42h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
21h	REG2F43	7:0	Default : 0x00	Access : R/W

VOP Register (Bank = 2F, Sub-Bank = 10)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
(2F43h)	-	7	Reserved.
	DOT	6	Differential output type. 0: Normal LVDS/RSDS operation. 1: Reduced-swing LVDS/increased-swing RSDS.
	WHTS	5	White screen (including main window and sub window). 0: Disable. 1: Enable.
	BLSK	4	Black screen (including main window and sub window). 0: Disable. 1: Enable.
	REVERSE	3	Reverse luminosity. 0: Off. 1: On.
	-	2:1	Reserved.
	DUAL_PIXEL_OUTPUT	0	Dual pixel output. 0: Single pixel. 1: Dual pixel.
22h (2F44h)	**REG2F44**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:0	Reserved.
22h (2F45h)	**REG2F45**	**7:0**	**Default : 0x00**	**Access : R/W**
	FBLALL_SET	7	Tune on/off short line.
	-	6:0	Reserved.
23h (2F46h)	**REG2F46**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSDCHBLEND	7	OSD character blending mode.
	-	6	Reserved.
	NBM	5	New blending level. 0: Original blending level (BLENDL = 000 means 0% transparency). 1: New blending level (BLENDL = 000 means 12.5% transparency).
	-	4	Reserved.
	GATP	3	Gamma automatically on/off based on auto phase value. 0: Disable. 1: Enable.
	BLENDL[2:0]	2:0	OSD alpha blending level. 000: 12.5% transparency.

VOP Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
			001: 25.0% transparency.	
			010: 37.5% transparency.	
			011: 50.0%% transparency.	
			100: 62.5% transparency	
			101: 75.0% transparency.	
			110: 87.5% transparency.	
			111: 100% transparency.	
23h (2F47h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
24h (2F48h)	REG2F48	7:0	Default : 0x00	Access : R/W
	MNS_COL[7:0]	7:0	Main window no signal color.	
24h (2F49h)	REG2F49	7:0	Default : 0x00	Access : R/W
	MBCOL[7:0]	7:0	Main window border color.	
25h (2F4Ah)	REG2F4A	7:0	Default : 0x00	Access : R/W
	FPLL_NEW_EN	7	Select FPLL output lock point.	
	-	6:0	Reserved.	
25h (2F4Bh)	REG2F4B	7:0	Default : 0x00	Access : R/W
	GATED_LVL[1:0]	7:6	ODCLK gated level.	
	FLCK_DL_LN[2:0]	5:3	Delay line number in flock mode.	
	FLCK_AH_LN[2:0]	2:0	Ahead line in flock mode.	
26h (2F4Ch)	REG2F4C	7:0	Default : 0x00	Access : R/W
	CM11[7:0]	7:0	Color matrix coefficient 11.	
26h (2F4Dh)	REG2F4D	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CM11[12:8]	4:0	Please see description of '2F4Ch'.	
27h (2F4Eh)	REG2F4E	7:0	Default : 0x00	Access : R/W
	CM12[7:0]	7:0	Color matrix coefficient 12.	
27h (2F4Fh)	REG2F4F	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CM12[12:8]	4:0	Please see description of '2F4Eh'.	
28h (2F50h)	REG2F50	7:0	Default : 0x00	Access : R/W
	CM13[7:0]	7:0	Color matrix coefficient 13.	
28h (2F51h)	REG2F51	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	

VOP Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
	CM13[12:8]	4:0	Please see description of '2F50h'.	
29h (2F52h)	REG2F52	7:0	Default : 0x00	Access : R/W
	CM21[7:0]	7:0	Color matrix coefficient 21.	
29h (2F53h)	REG2F53	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CM21[12:8]	4:0	Please see description of '2F52h'.	
2Ah (2F54h)	REG2F54	7:0	Default : 0x00	Access : R/W
	CM22[7:0]	7:0	Color matrix coefficient 22.	
2Ah (2F55h)	REG2F55	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CM22[12:8]	4:0	Please see description of '2F54h'.	
2Bh (2F56h)	REG2F56	7:0	Default : 0x00	Access : R/W
	CM23[7:0]	7:0	Color matrix coefficient 23.	
2Bh (2F57h)	REG2F57	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CM23[12:8]	4:0	Please see description of '2F56h'.	
2Ch (2F58h)	REG2F58	7:0	Default : 0x00	Access : R/W
	CM31[7:0]	7:0	Color matrix coefficient 31.	
2Ch (2F59h)	REG2F59	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CM31[12:8]	4:0	Please see description of '2F58h'.	
2Dh (2F5Ah)	REG2F5A	7:0	Default : 0x00	Access : R/W
	CM32[7:0]	7:0	Color matrix coefficient 32.	
2Dh (2F5Bh)	REG2F5B	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CM32[12:8]	4:0	Please see description of '2F5Ah'.	
2Eh (2F5Ch)	REG2F5C	7:0	Default : 0x00	Access : R/W
	CM33[7:0]	7:0	Color matrix coefficient 33.	
2Eh (2F5Dh)	REG2F5D	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CM33[12:8]	4:0	Please see description of '2F5Ch'.	
2Fh (2F5Eh)	REG2F5E	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	

VOP Register (Bank = 2F, Sub-Bank = 10)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	FTPS	6	Front-TPSCR. 0: Disable. 1: Enable.
	CMRND	5	Color matrix rounding control. 0: Disable. 1: Enable.
	CMC	4	Color matrix control. 0: Disable. 1: Enable.
	-	3	Reserved.
	RRAN	2	Red range. 0: 0~255. 1: -128~127.
	GRAN	1	Green range. 0: 0~255. 1: -128~127.
	BRAN	0	Blue range. 0: 0~255. 1: -128~127.
2Fh (2F5Fh)	REG2F5F	7:0	Default : 0x00 Access : R/W
	SSFD	7	Sub window shift field. 0: Shift even field. 1: Shift odd field.
	SSLN[1:0]	6:5	Sub window shift line numbers. 00: Shift 0 line between odd and even field. 01: Shift 1 line between odd and even field. 10: Shift 2 lines between odd and even field. 11: Shift 3 lines between odd and even field.
	ILIM	4	Insert line when interlace mode. 0: Do not insert. 1: Insert.
	MSFD	3	Main window shift field. 0: Shift even field. 1: Shift odd field.
	MSLN[2:0]	2:0	Main window shift line numbers. 000: Shift 0 line between odd and even field. 001: Shift 1 lines between odd and even field. 010: Shift 2 lines between odd and even field.

VOP Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
			011: Shift 3 lines between odd and even field.	
			1xx: Shift 4 lines between odd and even field.	
30h (2F60h)	REG2F60	7:0	Default : -	Access : RO
	IFVP[7:0]	7:0	Insert fraction vertical position.	
30h (2F61h)	REG2F61	7:0	Default : -	Access : RO
	IFVP[15:8]	7:0	Please see description of '2F60h'.	
31h (2F62h)	REG2F62	7:0	Default : -	Access : RO
	IFRACTW[7:0]	7:0	Insert fraction width PD down value.	
31h (2F63h)	REG2F63	7:0	Default : -	Access : RO
	IFRACTW[15:8]	7:0	Please see description of '2F62h'.	
32h (2F64h)	REG2F64	7:0	Default : -	Access : RO
	OVSSTAT[7:0]	7:0	Output vertical total status; lock status, equal to 1 when phase error less than 29h/2Ah.	
32h (2F65h)	REG2F65	7:0	Default : -	Access : RO
	-	7	Reserved.	
	OVERDESTAT	6	Output vertical DE status.	
	-	5:3	Reserved.	
	OVSSTAT[10:8]	2:0	Please see description of '2F64h'.	
33h (2F66h)	REG2F66	7:0	Default : 0x00	Access : R/W
	OHTSTAT0[7:0]	7:0	OHSTAT initial value.	
34h (2F68h)	REG2F68	7:0	Default : -	Access : RO
	OHTSTAT1[7:0]	7:0	Output H total status.	
35h (2F6Ah)	REG2F6A	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	OHTSTAT2[3:0]	3:0	OHSTAT initial value.	
36h (2F6Ch)	REG2F6C	7:0	Default : -	Access : RO
	-	7:4	Reserved.	
	OHTSTAT3[3:0]	3:0	OHSTAT initial value.	
37h (2F6Eh)	REG2F6E	7:0	Default : 0x00	Access : R/W
	FRACST0[7:0]	7:0	Fraction initial value.	
38h (2F70h)	REG2F70	7:0	Default : -	Access : RO
	FRACST1[7:0]	7:0	Fraction status	
39h	REG2F72	7:0	Default : 0x00	Access : R/W

VOP Register (Bank = 2F, Sub-Bank = 10)				
Index (Absolute)	Mnemonic	Bit	Description	
(2F72h)	-	7:3	Reserved.	
	FRACST2[2:0]	2:0	Fraction status.	
3Ah (2F74h)	REG2F74	7:0	Default : -	Access : RO
	-	7:3	Reserved.	
	FRACST3[2:0]	2:0	Fraction status.	
3Bh (2F76h)	REG2F76	7:0	Default : 0x00	Access : R/W
	HTTMGN[7:0]	7:0	H total margin	
3Bh (2F77h)	REG2F77	7:0	Default : 0x00	Access : R/W
	SSCMGN[7:0]	7:0	SSC margin.	
3Ch (2F78h)	REG2F78	7:0	Default : 0x00	Access : R/W
	RSTVALUE0[7:0]	7:0	Read start initial value.	
3Dh (2F7Ah)	REG2F7A	7:0	Default : -	Access : RO
	RSTVALUE1[7:0]	7:0	Read start value.	
3Eh (2F7Ch)	REG2F7C	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	RSTVALUE2[4:0]	4:0	Read start initial value.	
3Fh (2F7Eh)	REG2F7E	7:0	Default : -	Access : RO
	-	7:5	Reserved.	
	RSTVALUE3[4:0]	4:0	Read start value.	
40h (2F80h)	REG2F80	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	FRONT_BACK	5	Set front back mode.	
	-	4:0	Reserved.	
41h (2F81h)	REG2F81	7:0	Default : 0x00	Access : R/W
	INP8	7	Enable G replace R and B for gamma mapping with ONE_DRV3.	
	ONE_DRV3	6	Gamma use G replacing R and B for gamma mapping.	
	GABYP	5	Bypass gamma function.	
	-	4:3	Reserved.	
	TUN_FPLL_DL_LN[2:0]	2:0	Delay line numbers of FPLL mode.	
41h (2F82h)	REG2F82	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	TUNE_SLOW_REG_EN	3	FPLL tune slow register enable.	

VOP Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
	FRAME_LPLL_MCU_EN	2	Frame PLL MCU mode.	
	VCR_MD	1	VSYNC follow mode.	
	-	0	Reserved.	
42h (2F83h)	**REG2F83**	**7:0**	**Default : 0x00**	**Access : R/W**
	LFCOEF1[2:0]	7:5	Loop filter coef. 1.	
	LFCOEF2[4:0]	4:0	Loop filter coef. 2.	
42h (2F84h)	-	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
43h (2F85h)	**REG2F85**	**7:0**	**Default : 0x00**	**Access : R/W**
	TFRACN[7:0]	7:0	Target fraction number; frame PLL limit RK[7:0].	
43h (2F86h)	-	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
44h (2F87h ~ 2F88h)	-	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
45h (2F8Ah)	**REG2F8A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	FX_PROT	4	Frame change protect.	
	-	3:0	Reserved.	
45h (2F8Bh)	**REG2F8B**	**7:0**	**Default : 0x40**	**Access : R/W**
	TSTMD_REG_EN	7	Test mode register enable. 0: Disable. 1: Enable.	
	EOCK	6	Use external clock (pin #) as output dot clock. 0: Disable (use internal dot clock). 1: Enable (use external dot clock)	
	SEE_DEBUG_SEL[2:0]	5:3	See debug bus output byte enable, bit0=DI[7:0], bit1=DI[15:8], bit2=DI[23:16].	
	-	2:0	Reserved.	
46h (2F8Ch)	-	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
46h (2F8Dh)	REG2F8D	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	BOUND_PATENT	3	Register set for bound patent.	

VOP Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
	-	2:0	Reserved.	
47h ~ 48h (2F8Eh ~ 2F90h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
48h (2F91h)	**REG2F91**	7:0	**Default : 0x00**	**Access : R/W**
	TEST_CLK_MD	7	Test Clock Mode. 0: Disable. 1: Enable.	
	PLL_DIV2	6	0: Normal. 1: Test clock output divided by 2.	
	DDR_TEST	5	1: Select DDR 29est bus.	
	TEST_MD_D	4	1: Enable 24-bit test bus output.	
	TEST_MD[3:0]	3:0	Reserved.	
49h ~ 4Ah (2F92h ~ 2F95h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
4Bh (2F96h)	**REG2F96**	7:0	**Default : 0x44**	**Access : R/W**
	LP_SET0[7:0]	7:0	Output PLL set.	
4Bh (2F97h)	**REG2F97**	7:0	**Default : 0x55**	**Access : R/W**
	LP_SET0[15:8]	7:0	Please see description of '2F96h'.	
4Ch (2F98h)	**REG2F98**	7:0	**Default : 0x00**	**Access : R/W**
	LP_SET1[7:0]	7:0	Output PLL set.	
4Ch (2F99h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
50h (2FA0h)	**REG2FA0**	7:0	**Default : 0x00**	**Access : R/W**
	OBN10	7	10-bit bus enable. 0: Disable. 1: Enable.	
	DITHER_MINUS	6	Dither minus. 0: Disable. 1: Enable.	
	-	5	Reserved.	
	M_GRG	4	Main window gamma rounding.	
	-	3:1	Reserved.	
	GCFE	0	Gamma correction function enable.	

VOP Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
			0: Off. 1: On.	
50h ~ 55h (2FA1h ~ 2FABh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
56h (2FACh)	REG2FAC	7:0	Default : 0x00	Access : R/W
	LIM_HS	7	Limit H-total by PWM counter enable.	
	NEW_FLD_SEL	6	Select field created method. 0: Created by VSYNC and HSYNC.	
	SEL_OSD_AL	5	Select OSD down count index. 0: VFDE end. 1: VSYNC end.	
	-	4:0	Reserved.	
57h (2FAEh)	REG2FAE	7:0	Default : -	Access : RO
	REM[7:0]	7:0	H-total remainder value.	
57h (2FAFh)	REG2FAF	7:0	Default : -	Access : RO
	-	7:4	Reserved.	
	REM[11:8]	3:0	Please see description of '2FAEh'.	
58h (2FB0h)	REG2FB0	7:0	Default : 0x00	Access : R/W
	PWM5DIV[7:0]	7:0	PWM5 clock div. factor.	
58h (2FB1h)	REG2FB1	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	PWM5DIV[8]	0	Please see description of '2FB0h'.	
59h (2FB2h)	REG2FB2	7:0	Default : 0x00	Access : R/W
	PWM5DUTY[7:0]	7:0	PWM5 period.	
5Ah (2FB4h)	REG2FB4	7:0	Default : 0x00	Access : R/W
	TRACE_PHASE_HTOTAL[7:0]	7:0	New HTOTAL for fast phase offset reduce, only active when REG_TRACE_PHASE_EN set to 1.	
5Ah (2FB5h)	REG2FB5	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	NEW_HBC_CLAMP	6	Clamp function for HBC gain.	
	NEW_HBC_GAIN	5	HBC gain mode. 0: 0.4. 1: 0.04.	

VOP Register (Bank = 2F, Sub-Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TRACE_PHASE_EN	4	Enable modify HTOTAL for fast phase offset reduce.	
	TRACE_PHASE_HTOTAL[11:8]	3:0	Please see description of '2FB4h'.	
65h (2FCAh)	**REG2FCA**	**7:0**	**Default : 0x00**	**Access : R/W**
	FREEZE_VCNT_VALUE[7:0]	7:0	Freeze v counter position.	
65h (2FCBh)	**REG2FCB**	**7:0**	**Default : 0x00**	**Access : R/W**
	FREEZE_VCNT_VALUE[10:8]	2:0	Please see description of '2FCA'.	
66h (2FCC)	**REG2FCC**	**7:0**	**Default : 0x00**	**Access : R/W**
	LOCK_VCNT_VALUE[7:0]	7:0	New OVS reference position.	
66h (2FCD)	**REG2FCD**	**7:0**	**Default : 0x00**	**Access : R/W**
	LOCK_VCNT_VALUE[10:8]	2:0	Please see description of 'REG2FCC'.	
67h (2FCE)	**REG2FCE**	**7:0**	**Default : 0x00**	**Access : R/W**
	OUTPUT_FIELD_SEL	5	OVS reference field select.	
	OUTPUT_FIELD_INV	4	OVS reference field invert.	
	SW_RESET_VCNT_FREEZ	3	Software clear VCNT freeze region.	
	IVS_SEL	2	IVS reference signal select.	
	NEW_LOCK_POINT	1	Enable new OVS reference signal.	
	INPUT_FREEZ	0	Enable V counter freeze function.	
67h (2FCF)	**REG2FCF**	**7:0**	**Default : 0x00**	**Access : R/W**
	IVS_CNT	1:0	Input frame for IVS reference generate.	
6Ah (2FD4h)	**REG2FD4**	**7:0**	**Default : 0x00**	**Access : R/W**
	HIFRC_SROT	7	Enable HIFRC spatial rotation.	
	RAN[1:0]	6:5	Enable HIFRC random noise latch for rotation.	
	F2_EN	4	Enable noise repeats 2 frames.	
	NEW_DITH_M	3	New dither method select.	
	-	2	Reserved.	
	PSEUDO_EN_T	1	Enable dither pattern rotation line by line.	
	PSEUDO_EN_S	0	Enable dither pattern rotation frame by frame.	
6Ah (2FD5h)	**REG2FD5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	OSD_HDE_SEL	6	Select OSD_HDE with VFDE signal. 0: OSD_HDE = HFDE. 1: OSD_HDE = HFDE & VFDE.	
	PSE_RST_NUM[1:0]	5:4	Frame period for dither pseudo noise reset.	

**VOP Register (Bank = 2F, Sub-Bank = 10)**
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	H_RAN_EN	3	H direction using random noise enable for HIFRC.	
	NEW_ACBD	2	Swap HIFRC probability sequence.	
	OLD_HIFRC	1	Select old HIFRC dither method.	
	RAN_DIR_EN	0	Enable noise as rotate direction.	
6Ch (2FD8h)	REG2FD8	7:0	Default : 0x00	Access : R/W
	LUT_RAM_ADDRESS[7:0]	7:0	LUT table r/w address.	
6Dh (2FDAh)	REG2FDA	7:0	Default : 0x00	Access : R/W
	LUT_W_FLAG2	7	LUT table blue write command.	
	LUT_W_FLAG1	6	LUT table green write command.	
	LUT_W_FLAG0	5	LUT table red write command.	
	-	4:0	Reserved.	
6Dh (2FDBh)	REG2FDB	7:0	Default : 0x00	Access : R/W
	LUT_R_FLAG2	7	LUT table blue read command.	
	LUT_R_FLAG1	6	LUT table green read command.	
	LUT_R_FLAG0	5	LUT table red read command.	
	-	4:0	Reserved.	
6Eh (2FDCh)	REG2FDC	7:0	Default : 0x00	Access : R/W
	WR_R[7:0]	7:0	Data write to R LUT SRAM.	
6Eh (2FDDh)	REG2FDD	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	WR_R[11:8]	3:0	Please see description of '2FDCh'.	
6Fh (2FDEh)	REG2FDE	7:0	Default : 0x00	Access : R/W
	WR_G[7:0]	7:0	Data write to G LUT SRAM.	
6Fh (2FDFh)	REG2FDF	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	WR_G[11:8]	3:0	Please see description of '2FDEh'.	
70h (2FE0h)	REG2FE0	7:0	Default : 0x00	Access : R/W
	WR_B[7:0]	7:0	Data write to B LUT SRAM.	
70h (2FE1h)	REG2FE1	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	WR_B[11:8]	3:0	Please see description of '2FE0h'.	
71h (2FE2h)	REG2FE2	7:0	Default : -	Access : RO
	RD_R[7:0]	7:0	Data read from R LUT SRAM.	

VOP Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
71h (2FE3h)	REG2FE3	7:0	Default : -	Access : RO
	-	7:4	Reserved.	
	RD_R[11:8]	3:0	Please see description of '2FE2h'.	
72h (2FE4h)	REG2FE4	7:0	Default : -	Access : RO
	RD_G[7:0]	7:0	Data read from G LUT SRAM.	
72h (2FE5h)	REG2FE5	7:0	Default : -	Access : RO
	-	7:4	Reserved.	
	RD_G[11:8]	3:0	Please see description of '2FE4h'.	
73h (2FE6h)	REG2FE6	7:0	Default : -	Access : RO
	RD_B[7:0]	7:0	Data read from B LUT SRAM.	
73h (2FE7h)	REG2FE7	7:0	Default : -	Access : RO
	-	7:4	Reserved.	
	RD_B[11:8]	3:0	Please see description of '2FE6h'.	
74h (2FE8h)	REG2FE8	7:0	Default : 0x00	Access : RO, R/W
	-	7:4	Reserved.	
	CLR_MLOAD_TOO_SLOW	3	Clear auto MLOAD gamma too slow flag.	
	MLOAD_TOO_SLOW	2	Auto MLOAD gamma too slow flag.	
	AUTO_MLOAD_SWITCH	1	Enable auto-MLOAD gamma switch gamma table by frame.	
	AUTO_MLOAD_GAMMA	0	Enable auto-MLOAD gamma function.	
75h (2FEAh)	REG2FEA	7:0	Default : 0x00	Access : R/W
	MLOAD_GAMMA_BASE0[7:0]	7:0	Gamma table base address 0.	
75h (2FEBh)	REG2FEB	7:0	Default : 0x00	Access : R/W
	MLOAD_GAMMA_BASE0[15:8]	7:0	Please see description of '2FEAh'.	
76h (2FECh)	REG2FEC	7:0	Default : 0x00	Access : R/W
	MLOAD_GAMMA_BASE0[23:16]	7:0	Please see description of '2FEAh'.	
77h (2FEEh)	REG2FEE	7:0	Default : 0x00	Access : R/W
	MLOAD_GAMMA_BASE1[7:0]	7:0	Gamma table base address 1.	
77h (2FEFh)	REG2FEF	7:0	Default : 0x00	Access : R/W
	MLOAD_GAMMA_BASE1[15:8]	7:0	Please see description of '2FEEh'.	
78h (2FF0h)	REG2FF0	7:0	Default : 0x00	Access : R/W
	MLOAD_GAMMA_BASE1[23:16]	7:0	Please see description of '2FEEh'.	
79h	REG2FF2	7:0	Default : 0x00	Access : R/W

VOP Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
(2FF2h)	MLOAD_CNT[7:0]	7:0	Load gamma table from DRAM number.	
7Ah (2FF4h)	REG2FF4	7:0	Default : 0x00	Access : R/W
	R_MAX_BASE0[7:0]	7:0	Max value for R channel gamma table 0.	
7Ah (2FF5h)	REG2FF5	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	R_MAX_BASE0[11:8]	3:0	Please see description of '2FF4h'.	
7Bh (2FF6h)	REG2FF6	7:0	Default : 0x00	Access : R/W
	R_MAX_BASE1[7:0]	7:0	Max value for R channel gamma table 1.	
7Bh (2FF7h)	REG2FF7	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	R_MAX_BASE1[11:8]	3:0	Please see description of '2FF6h'.	
7Ch (2FF8h)	REG2FF8	7:0	Default : 0x00	Access : R/W
	G_MAX_BASE0[7:0]	7:0	Max value for G channel gamma table 0.	
7Ch (2FF9h)	REG2FF9	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	G_MAX_BASE0[11:8]	3:0	Please see description of '2FF8h'.	
7Dh (2FFAh)	REG2FFA	7:0	Default : 0x00	Access : R/W
	G_MAX_BASE1[7:0]	7:0	Max value for G channel gamma table 1.	
7Dh (2FFBh)	REG2FFB	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	G_MAX_BASE1[11:8]	3:0	Please see description of '2FFAh'.	
7Eh (2FFCh)	REG2FFC	7:0	Default : 0x00	Access : R/W
	B_MAX_BASE0[7:0]	7:0	Max value for B channel gamma table 0.	
7Eh (2FFDh)	REG2FFD	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	B_MAX_BASE0[11:8]	3:0	Please see description of '2FFCh'.	
7Fh (2FFEh)	REG2FFE	7:0	Default : 0x00	Access : R/W
	B_MAX_BASE1[7:0]	7:0	Max value for B channel gamma table 1.	
7Fh (2FFFh)	REG2FFF	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	B_MAX_BASE1[11:8]	3:0	Please see description of '2FFEh'.	

ACE Register (Bank = 2F, Sub-Bank = 18)

Index (Absolute)	Mnemonic	Bit	Description	
00h (2F00h)	REG2F00	7:0	Default : 0x00	Access : R/W
	MODULE_REGBANK[7:0]	7:0	Register bank select. 00: Register of OSD/Interrupt. 01: Register of IP1 Main Window. 02: Register of IP2 Main Window. 03: Register of IP1 Sub Window. 04: Register of IP2 Sub Window. 05: Register of OPM. 06: Register of DNR. 07: Register of OP1. 08: Register of OP1PIP. 09: Register of OP1AH. 0A: Register of OP1ZZ. 0B: Register of ELA. 0C: Register of SNR. 0F: Register of S_VOP. 10: Register of VOP. 14: Register of ESB. 15: Register of GNR. 16: Register of OD. 18: Register of ACE. 19: Register of Peaking. 1A: Register of DLC. Default: Reserved.	
	MAIN_FCC_7T_EN	6	Main window FCC region 7 enable.	
	MAIN_FCC_6T_EN	5	Main window FCC region 6 enable.	
	MAIN_FCC_5T_EN	4	Main window FCC region 5 enable.	
	MAIN_FCC_4T_EN	3	Main window FCC region 4 enable.	
	MAIN_FCC_3T_EN	2	Main window FCC region 3 enable.	
	MAIN_FCC_2T_EN	1	Main window FCC region 2 enable.	
	MAIN_FCC_1T_EN	0	Main window FCC region 1 enable.	
10h (2F21h)	REG2F21	7:0	Default : 0x00	Access : R/W
	WIN1_DARK_MD_EN	7	Region 1 dark mode enable.	
	-	6:1	Reserved.	
	MAIN_FCC_9T_EN	0	Main window FCC window 9 enable.	
11h	REG2F22	7:0	Default : 0x00	Access : R/W

ACE Register (Bank = 2F, Sub-Bank = 18)

Index (Absolute)	Mnemonic	Bit	Description	
(2F22h)	SUB_FCC_8T_EN	7	Sub window FCC region 8 enable.	
	SUB_FCC_7T_EN	6	Sub window FCC region 7 enable.	
	SUB_FCC_6T_EN	5	Sub window FCC region 6 enable.	
	SUB_FCC_5T_EN	4	Sub window FCC region 5 enable.	
	SUB_FCC_4T_EN	3	Sub window FCC region 4 enable.	
	SUB_FCC_3T_EN	2	Sub window FCC region 3 enable.	
	SUB_FCC_2T_EN	1	Sub window FCC region 2 enable.	
	SUB_FCC_1T_EN	0	Sub window FCC region 1 enable.	
11h (2F23h)	REG2F23	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	SUB_FCC_9T_EN	0	Sub window FCC region 9 enable.	
13h (2F26h)	REG2F26	7:0	Default : 0x00	Access : R/W
	CB_T1_Y_10[7:0]	7:0	FCC region 1 Cb target, when Y=10.	
13h (2F27h)	REG2F27	7:0	Default : 0x00	Access : R/W
	CR_T1_Y_10[7:0]	7:0	FCC region 1 Cr target, when Y=10.	
14h (2F28h)	REG2F28	7:0	Default : 0x00	Access : R/W
	CB_T1_Y_20[7:0]	7:0	FCC region 1 Cb target, when Y=20.	
14h (2F29h)	REG2F29	7:0	Default : 0x00	Access : R/W
	CR_T1_Y_20[7:0]	7:0	FCC region 1 Cr target, when Y=20.	
15h (2F2Ah)	REG2F2A	7:0	Default : 0x00	Access : R/W
	CB_T1_Y_30[7:0]	7:0	FCC region 1 Cb target, when Y=30.	
15h (2F2Bh)	REG2F2B	7:0	Default : 0x00	Access : R/W
	CR_T1_Y_30[7:0]	7:0	FCC region 1 Cr target, when Y=30.	
16h (2F2Ch)	REG2F2C	7:0	Default : 0x00	Access : R/W
	CB_T1_Y_40[7:0]	7:0	FCC region 1 Cb target, when Y=40.	
16h (2F2Dh)	REG2F2D	7:0	Default : 0x00	Access : R/W
	CR_T1_Y_40[7:0]	7:0	FCC region 1 Cr target, when Y=40.	
17h (2F2Eh)	REG2F2E	7:0	Default : 0x00	Access : R/W
	CB_T1_Y_50[7:0]	7:0	FCC region 1 Cb target, when Y=50.	
17h (2F2Fh)	REG2F2F	7:0	Default : 0x00	Access : R/W
	CR_T1_Y_50[7:0]	7:0	FCC region 1 Cr target, when Y=50.	
18h (2F30h)	REG2F30	7:0	Default : 0x00	Access : R/W
	CB_T1[7:0]	7:0	FCC region 1 Cb target.	

ACE Register (Bank = 2F, Sub-Bank = 18)

Index (Absolute)	Mnemonic	Bit	Description	
18h (2F31h)	REG2F31	7:0	Default : 0x00	Access : R/W
	CR_T1[7:0]	7:0	FCC region 1 Cr target.	
19h (2F32h)	REG2F32	7:0	Default : 0x00	Access : R/W
	CB_T2[7:0]	7:0	FCC region 2 Cb target.	
19h (2F33h)	REG2F33	7:0	Default : 0x00	Access : R/W
	CR_T2[7:0]	7:0	FCC region 2 Cr target.	
1Ah (2F34h)	REG2F34	7:0	Default : 0x00	Access : R/W
	CB_T3[7:0]	7:0	FCC region 3 Cb target.	
1Ah (2F35h)	REG2F35	7:0	Default : 0x00	Access : R/W
	CR_T3[7:0]	7:0	FCC region 3 Cr target.	
1Bh (2F36h)	REG2F36	7:0	Default : 0x00	Access : R/W
	CB_T4[7:0]	7:0	FCC region 4 Cb target.	
1Bh (2F37h)	REG2F37	7:0	Default : 0x00	Access : R/W
	CR_T4[7:0]	7:0	FCC region 4 Cr target.	
1Ch (2F38h)	REG2F38	7:0	Default : 0x00	Access : R/W
	CB_T5[7:0]	7:0	FCC region 5 Cb target.	
1Ch (2F39h)	REG2F39	7:0	Default : 0x00	Access : R/W
	CR_T5[7:0]	7:0	FCC region 5 Cr target.	
1Dh (2F3Ah)	REG2F3A	7:0	Default : 0x00	Access : R/W
	CB_T6[7:0]	7:0	FCC region 6 Cb target.	
1Dh (2F3Bh)	REG2F3B	7:0	Default : 0x00	Access : R/W
	CR_T6[7:0]	7:0	FCC region 6 Cr target.	
1Eh (2F3Ch)	REG2F3C	7:0	Default : 0x00	Access : R/W
	CB_T7[7:0]	7:0	FCC region 7 Cb target.	
1Eh (2F3Dh)	REG2F3D	7:0	Default : 0x00	Access : R/W
	CR_T7[7:0]	7:0	FCC region 7 Cr target.	
1Fh (2F3Eh)	REG2F3E	7:0	Default : 0x00	Access : R/W
	CB_T8[7:0]	7:0	FCC region 8 Cb target.	
1Fh (2F3Fh)	REG2F3F	7:0	Default : 0x00	Access : R/W
	CR_T8[7:0]	7:0	FCC region 8 Cr target.	
20h (2F40h)	REG2F40	7:0	Default : 0xFF	Access : R/W
	FCC_K_2T[3:0]	7:4	FCC region 2 strength.	
	FCC_K_1T[3:0]	3:0	FCC region 1 strength.	

ACE Register (Bank = 2F, Sub-Bank = 18)

Index (Absolute)	Mnemonic	Bit	Description	
20h (2F41h)	REG2F41	7:0	Default : 0xFF	Access : R/W
	FCC_K_4T[3:0]	7:4	FCC region 4 strength.	
	FCC_K_3T[3:0]	3:0	FCC region 3 strength.	
21h (2F42h)	REG2F42	7:0	Default : 0xFF	Access : R/W
	FCC_K_6T[3:0]	7:4	FCC region 6 strength.	
	FCC_K_5T[3:0]	3:0	FCC region 5 strength.	
21h (2F43h)	REG2F43	7:0	Default : 0xFF	Access : R/W
	FCC_K_8T[3:0]	7:4	FCC region 8 strength.	
	FCC_K_7T[3:0]	3:0	FCC region 7 strength.	
22h (2F44h)	REG2F44	7:0	Default : 0x0F	Access : R/W
	-	7:4	Reserved.	
	FCC_K_9T[3:0]	3:0	FCC region 9 strength.	
24h (2F48h)	REG2F48	7:0	Default : 0x00	Access : R/W
	FCC_WIN1_CB_UP[1:0]	7:6	FCC region 1 target Cb up distance.	
	FCC_WIN1_CB_DOWN[1:0]	5:4	FCC region 1 target Cb down distance.	
	FCC_WIN1_CR_UP[1:0]	3:2	FCC region 1 target Cr up distance.	
	FCC_WIN1_CR_DOWN[1:0]	1:0	FCC region 1 target Cr down distance.	
24h (2F49h)	REG2F49	7:0	Default : 0x00	Access : R/W
	FCC_WIN2_CB_UP[1:0]	7:6	FCC region 2 target Cb up distance.	
	FCC_WIN2_CB_DOWN[1:0]	5:4	FCC region 2 target Cb down distance.	
	FCC_WIN2_CR_UP[1:0]	3:2	FCC region 2 target Cr up distance.	
	FCC_WIN2_CR_DOWN[1:0]	1:0	FCC region 2 target Cr down distance.	
25h (2F4Ah)	REG2F4A	7:0	Default : 0x00	Access : R/W
	FCC_WIN3_CB_UP[1:0]	7:6	FCC region 3 target Cb up distance.	
	FCC_WIN3_CB_DOWN[1:0]	5:4	FCC region 3 target Cb down distance.	
	FCC_WIN3_CR_UP[1:0]	3:2	FCC region 3 target Cr up distance.	
	FCC_WIN3_CR_DOWN[1:0]	1:0	FCC region 3 target Cr down distance.	
25h (2F4Bh)	REG2F4B	7:0	Default : 0x00	Access : R/W
	FCC_WIN4_CB_UP[1:0]	7:6	FCC region 4 target Cb up distance.	
	FCC_WIN4_CB_DOWN[1:0]	5:4	FCC region 4 target Cb down distance.	
	FCC_WIN4_CR_UP[1:0]	3:2	FCC region 4 target Cr up distance.	
	FCC_WIN4_CR_DOWN[1:0]	1:0	FCC region 4 target Cr down distance.	
26h	REG2F4C	7:0	Default : 0x00	Access : R/W

ACE Register (Bank = 2F, Sub-Bank = 18)

Index (Absolute)	Mnemonic	Bit	Description	
(2F4Ch)	FCC_WIN5_CB_UP[1:0]	7:6	FCC region 5 target Cb up distance.	
	FCC_WIN5_CB_DOWN[1:0]	5:4	FCC region 5 target Cb down distance.	
	FCC_WIN5_CR_UP[1:0]	3:2	FCC region 5 target Cr up distance.	
	FCC_WIN5_CR_DOWN[1:0]	1:0	FCC region 5 target Cr down distance.	
26h (2F4Dh)	REG2F4D	7:0	Default : 0x00	Access : R/W
	FCC_WIN6_CB_UP[1:0]	7:6	FCC region 6 target Cb up distance.	
	FCC_WIN6_CB_DOWN[1:0]	5:4	FCC region 6 target Cb down distance.	
	FCC_WIN6_CR_UP[1:0]	3:2	FCC region 6 target Cr up distance.	
	FCC_WIN6_CR_DOWN[1:0]	1:0	FCC region 6 target Cr down distance.	
27h (2F4Eh)	REG2F4E	7:0	Default : 0x00	Access : R/W
	FCC_WIN7_CB_UP[1:0]	7:6	FCC region 7 target Cb up distance.	
	FCC_WIN7_CB_DOWN[1:0]	5:4	FCC region 7 target Cb down distance.	
	FCC_WIN7_CR_UP[1:0]	3:2	FCC region 7 target Cr up distance.	
	FCC_WIN7_CR_DOWN[1:0]	1:0	FCC region 7 target Cr down distance.	
27h (2F4Fh)	REG2F4F	7:0	Default : 0x00	Access : R/W
	FCC_WIN8_CB_UP[1:0]	7:6	FCC region 8 target Cb up distance.	
	FCC_WIN8_CB_DOWN[1:0]	5:4	FCC region 8 target Cb down distance.	
	FCC_WIN8_CR_UP[1:0]	3:2	FCC region 8 target Cr up distance.	
	FCC_WIN8_CR_DOWN[1:0]	1:0	FCC region 8 target Cr down distance.	
28h (2F50h)	REG2F50	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	FCC_WIN9_CB[2:0]	5:3	FCC region 9 target Cb distance.	
	FCC_WIN9_CR[2:0]	2:0	FCC region 9 target Cr distance.	
28h (2F51h)	REG2F51	7:0	Default : 0x00	Access : R/W
	FCC_TEST_MD[7:0]	7:0	FCC test mode enable.	
30h (2F60h)	REG2F60	7:0	Default : 0x00	Access : R/W
	MAIN_CBCR_TO_UV	7	Main window CbCr to UV enable.	
	MAIN_ICC_EN	6	Main window ICC enable.	
	-	5:4	Reserved.	
	SUB_CBCR_TO_UV	3	Sub window CbCr to UV enable.	
	SUB_ICC_EN	2	Sub window ICC enable.	
	-	1:0	Reserved.	
31h	REG2F62	7:0	Default : 0x00	Access : R/W

ACE Register (Bank = 2F, Sub-Bank = 18)

Index (Absolute)	Mnemonic	Bit	Description	
(2F62h)	SUB_SA_USER_R[3:0]	7:4	Sub window ICC saturation adjustment of R.	
	MAIN_SA_USER_R[3:0]	3:0	Main window ICC saturation adjustment of R.	
31h (2F63h)	REG2F63	7:0	Default : 0x00	Access : R/W
	SUB_SA_USER_G[3:0]	7:4	Sub window ICC saturation adjustment of G.	
	MAIN_SA_USER_G[3:0]	3:0	Main window ICC saturation adjustment of G.	
32h (2F64h)	REG2F64	7:0	Default : 0x00	Access : R/W
	SUB_SA_USER_B[3:0]	7:4	Sub window ICC saturation adjustment of B.	
	MAIN_SA_USER_B[3:0]	3:0	Main window ICC saturation adjustment of B.	
32h (2F65h)	REG2F65	7:0	Default : 0x00	Access : R/W
	SUB_SA_USER_C[3:0]	7:4	Sub window ICC saturation adjustment of C.	
	MAIN_SA_USER_C[3:0]	3:0	Main window ICC saturation adjustment of C.	
33h (2F66h)	REG2F66	7:0	Default : 0x00	Access : R/W
	SUB_SA_USER_M[3:0]	7:4	Sub window ICC saturation adjustment of M.	
	MAIN_SA_USER_M[3:0]	3:0	Main window ICC saturation adjustment of M.	
33h (2F67h)	REG2F67	7:0	Default : 0x00	Access : R/W
	SUB_SA_USER_Y[3:0]	7:4	Sub window ICC saturation adjustment of Y.	
	MAIN_SA_USER_Y[3:0]	3:0	Main window ICC saturation adjustment of Y.	
34h (2F68h)	REG2F68	7:0	Default : 0x00	Access : R/W
	SUB_SA_USER_F[3:0]	7:4	Sub window ICC saturation adjustment of F.	
	MAIN_SA_USER_F[3:0]	3:0	Main window ICC saturation adjustment of F.	
35h (2F6Ah)	REG2F6A	7:0	Default : 0x00	Access : R/W
	MAIN_SIGN_SA_USER[7:0]	7:0	Main window ICC decrease saturation.	
35h (2F6Bh)	REG2F6B	7:0	Default : 0x00	Access : R/W
	SUB_SIGN_SA_USER[7:0]	7:0	Sub window ICC decrease saturation.	
36h (2F6Ch)	REG2F6C	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	COMMON_MINUS_GAIN[4:0]	4:0	ICC decrease saturation common gain.	
36h (2F6Dh)	REG2F6D	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	SA_MIN[6:0]	6:0	ICC decrease saturation minimum threshold.	
38h (2F70h)	REG2F70	7:0	Default : 0x00	Access : R/W
	MAIN_Y_SWITCH_EN	7	Main window Y switch enable.	
	MAIN_ACK_EN	6	Main window ACK enable.	

ACE Register (Bank = 2F, Sub-Bank = 18)

Index (Absolute)	Mnemonic	Bit	Description	
	-	5:4	Reserved.	
	SUB_Y_SWITCH_EN	3	Sub window Y switch enable.	
	SUB_ACK_EN	2	Sub window ACK enable.	
	BW_DITHER_EN	1	UV compensate dither enable.	
	-	0	Reserved.	
39h (2F72h)	REG2F72	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	U_SWITCH_COEF[5:0]	5:0	U coefficient for Y switch.	
39h (2F73h)	REG2F73	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	V_SWITCH_COEF[5:0]	5:0	V coefficient for Y switch.	
3Ah (2F74h)	REG2F74	7:0	Default : 0x00	Access : R/W
	ACK_OFFSET[3:0]	7:4	ACK offset.	
	ACK_Y_THRD[3:0]	3:0	ACK Y threshold.	
3Ah (2F75h)	REG2F75	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	ACK_Y_SLOP[4:0]	4:0	ACK Y slop.	
3Bh (2F76h)	REG2F76	7:0	Default : 0x00	Access : R/W
	ACK_C_COMP_EN	7	ACK chroma compensate enable.	
	ACK_LMT[6:0]	6:0	ACK limit.	
3Bh (2F77h)	REG2F77	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	ACK_C_RANGE[1:0]	6:5	ACK chroma range.	
	-	4	Reserved.	
	ACK_C_THRD[3:0]	3:0	ACK chroma threshold.	
3Ch (2F78h)	REG2F78	7:0	Default : 0xFF	Access : R/W
	WHITE_PEAK_LMT_THRD[7:0]	7:0	White peak limit threshold.	
40h (2F80h)	REG2F80	7:0	Default : 0x00	Access : R/W
	MAIN_IBC_EN	7	Main window IBC enable.	
	SUB_IBC_EN	6	Sub window IBC enable.	
	IBC_Y_ADJUST_LPF_EN	5	IBC Y adjust LPF enable.	
	-	4	Reserved.	
	IBC_CORING_THRD[3:0]	3:0	IBC coring threshold.	

ACE Register (Bank = 2F, Sub-Bank = 18)

Index (Absolute)	Mnemonic	Bit	Description	
41h (2F82h)	REG2F82	7:0	Default : 0x20	Access : R/W
	-	7:6	Reserved.	
	MAIN_YR_ADJ[5:0]	5:0	Main window IBC Y adjustment of R.	
41h (2F83h)	REG2F83	7:0	Default : 0x20	Access : R/W
	-	7:6	Reserved.	
	MAIN_YG_ADJ[5:0]	5:0	Main window IBC Y adjustment of G.	
42h (2F84h)	REG2F84	7:0	Default : 0x20	Access : R/W
	-	7:6	Reserved.	
	MAIN_YB_ADJ[5:0]	5:0	Main window IBC Y adjustment of B.	
42h (2F85h)	REG2F85	7:0	Default : 0x20	Access : R/W
	-	7:6	Reserved.	
	MAIN_YC_ADJ[5:0]	5:0	Main window IBC Y adjustment of C.	
43h (2F86h)	REG2F86	7:0	Default : 0x20	Access : R/W
	-	7:6	Reserved.	
	MAIN_YM_ADJ[5:0]	5:0	Main window IBC Y adjustment of M.	
43h (2F87h)	REG2F87	7:0	Default : 0x20	Access : R/W
	-	7:6	Reserved.	
	MAIN_YY_ADJ[5:0]	5:0	Main window IBC Y adjustment of Y.	
44h (2F88h)	REG2F88	7:0	Default : 0x20	Access : R/W
	-	7:6	Reserved.	
	MAIN_YF_ADJ[5:0]	5:0	Main window IBC Y adjustment of F.	
45h (2F8Ah)	REG2F8A	7:0	Default : 0x20	Access : R/W
	-	7:6	Reserved.	
	SUB_YR_ADJ[5:0]	5:0	Subwindow IBC Y adjustment of R.	
45h (2F8Bh)	REG2F8B	7:0	Default : 0x20	Access : R/W
	-	7:6	Reserved.	
	SUB_YG_ADJ[5:0]	5:0	Sub window IBC Y adjustment of G.	
46h (2F8Ch)	REG2F8C	7:0	Default : 0x20	Access : R/W
	-	7:6	Reserved.	
	SUB_YB_ADJ[5:0]	5:0	Sub window IBC Y adjustment of B.	
46h (2F8Dh)	REG2F8D	7:0	Default : 0x20	Access : R/W
	-	7:6	Reserved.	
	SUB_YC_ADJ[5:0]	5:0	Sub window IBC Y adjustment of C.	

ACE Register (Bank = 2F, Sub-Bank = 18)

Index (Absolute)	Mnemonic	Bit	Description	
47h (2F8Eh)	REG2F8E	7:0	Default : 0x20	Access : R/W
	-	7:6	Reserved.	
	SUB_YM_ADJ[5:0]	5:0	Sub window IBC Y adjustment of M.	
47h (2F8Fh)	REG2F8F	7:0	Default : 0x20	Access : R/W
	-	7:6	Reserved.	
	SUB_YY_ADJ[5:0]	5:0	Sub window IBC Y adjustment of Y.	
48h (2F90h)	REG2F90	7:0	Default : 0x20	Access : R/W
	-	7:6	Reserved.	
	SUB_YF_ADJ[5:0]	5:0	Sub window IBC Y adjustment of F.	
48h (2F91h)	REG2F91	7:0	Default : 0x00	Access : R/W
	WEIGHT_Y_MIN_LMT[3:0]	7:4	IBC y weight min limit.	
	WEIGHT_C_MIN_LMT[3:0]	3:0	IBC c weight min limit.	
50h (2FA0h)	REG2FA0	7:0	Default : 0x00	Access : R/W
	MAIN_Y_HIGH_PASS_EN	7	Main window Y H_coring as high pass filter.	
	MAIN_Y_TABLE_STEP[2:0]	6:4	Main window Y H_coring LUT step.	
	MAIN_PC_MD	3	Main window PC mode.	
	-	2	Reserved.	
	MAIN_Y_BAND2_H_CORING_EN	1	Main window Y band2 H_coring enable.	
	MAIN_Y_BAND1_H_CORING_EN	0	Main window Y band1 H_coring enable.	
50h (2FA1h)	REG2FA1	7:0	Default : 0x00	Access : R/W
	MAIN_C_HIGH_PASS_EN	7	Main window C H_coring as high pass filter.	
	MAIN_C_TABLE_STEP[2:0]	6:4	Main window C H_coring LUT step.	
	MAIN_WHITE_PEAK_LMT_EN	3	Main window white peak limit enable.	
	-	2	Reserved.	
	MAIN_C_BAND2_H_CORING_EN	1	Main window C band2 H_coring enable.	
	MAIN_C_BAND1_H_CORING_EN	0	Main window C band1 H_coring enable.	
51h (2FA2h)	REG2FA2	7:0	Default : 0x00	Access : R/W
	MAIN_Y_GAIN_TABLE1[7:0]	7:0	Main window Y gain table 1.	
51h (2FA3h)	REG2FA3	7:0	Default : 0x00	Access : R/W
	MAIN_Y_GAIN_TABLE2[7:0]	7:0	Main window Y gain table 2.	
52h (2FA4h)	REG2FA4	7:0	Default : 0x00	Access : R/W
	MAIN_Y_GAIN_TABLE3[7:0]	7:0	Main window Y gain table 3.	
52h	REG2FA5	7:0	Default : 0x00	Access : R/W

ACE Register (Bank = 2F, Sub-Bank = 18)

Index (Absolute)	Mnemonic	Bit	Description	
(2FA5h)	MAIN_Y_GAIN_TABLE4[7:0]	7:0	Main window Y gain table 4.	
53h (2FA6h)	**REG2FA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_C_GAIN_TABLE1[7:0]	7:0	Main window C gain table 1.	
53h (2FA7h)	**REG2FA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_C_GAIN_TABLE2[7:0]	7:0	Main window C gain table 2.	
54h (2FA8h)	**REG2FA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_C_GAIN_TABLE3[7:0]	7:0	Main window C gain table 3.	
54h (2FA9h)	**REG2FA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_C_GAIN_TABLE4[7:0]	7:0	Main window C gain table 4.	
55h (2FAAh)	**REG2FAA**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_Y_NOISE_MSKING_EN	7	Main window horizontal Y noise-masking enable.	
	MAIN_Y_DITHER_EN	6	Main and sub window horizontal Y noise-masking dither enable.	
	MAIN_Y_CF_NOISE_MSKING_EN	5	Main window horizontal Y noise-masking flesh color adaptive enable.	
	MAIN_Y_NOISE_MSK_GAIN[4:0]	4:0	Main window horizontal Y noise-masking gain.	
55h (2FABh)	**REG2FAB**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_C_NOISE_MSKING_EN	7	Main window horizontal C noise-masking enable.	
	MAIN_C_DITHER_EN	6	Main and sub window horizontal C noise-masking dither enable.	
	MAIN_C_CF_NOISE_MSKING_EN	5	Main window horizontal C noise-masking flesh color adaptive enable.	
	MAIN_C_NOISE_MSK_GAIN[4:0]	4:0	Main window horizontal C noise-masking gain.	
58h (2FB0h)	**REG2FB0**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_Y_HIGH_PASS_EN	7	Sub window Y H_coring as high pass filter.	
	SUB_Y_TABLE_STEP[2:0]	6:4	Sub window Y H_coring LUT step.	
	SUB_PC_MD	3	Sub window PC mode.	
	-	2	Reserved.	
	SUB_Y_BAND2_H_CORING_EN	1	Sub window Y band2 H_coring enable.	
	SUB_Y_BAND1_H_CORING_EN	0	Sub window Y band1 H_coring enable.	
58h (2FB1h)	**REG2FB1**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_C_HIGH_PASS_EN	7	Sub window C H_coring as high pass filter.	
	SUB_C_TABLE_STEP[2:0]	6:4	Sub window C H_coring LUT step.	
	SUB_WHITE_PEAK_LMT_EN	3	Sub window white peak limit enable.	

ACE Register (Bank = 2F, Sub-Bank = 18)

Index (Absolute)	Mnemonic	Bit	Description	
	-	2	Reserved.	
	SUB_C_BAND2_H_CORING_EN	1	Sub window C band2 H_coring enable.	
	SUB_C_BAND1_H_CORING_EN	0	Sub window C band1 H_coring enable.	
59h (2FB2h)	REG2FB2	7:0	Default : 0x00	Access : R/W
	SUB_Y_GAIN_TABLE1[7:0]	7:0	Sub window Y gain table 1.	
59h (2FB3h)	REG2FB3	7:0	Default : 0x00	Access : R/W
	SUB_Y_GAIN_TABLE2[7:0]	7:0	Sub window Y gain table 2.	
5Ah (2FB4h)	REG2FB4	7:0	Default : 0x00	Access : R/W
	SUB_Y_GAIN_TABLE3[7:0]	7:0	Sub window Y gain table 3.	
5Ah (2FB5h)	REG2FB5	7:0	Default : 0x00	Access : R/W
	SUB_Y_GAIN_TABLE4[7:0]	7:0	Sub window Y gain table 4.	
5Bh (2FB6h)	REG2FB6	7:0	Default : 0x00	Access : R/W
	SUB_C_CORE_TABLE1[7:0]	7:0	Sub window C gain table 1.	
5Bh (2FB7h)	REG2FB7	7:0	Default : 0x00	Access : R/W
	SUB_C_CORE_TABLE2[7:0]	7:0	Sub window C gain table 2.	
5Ch (2FB8h)	REG2FB8	7:0	Default : 0x00	Access : R/W
	SUB_C_CORE_TABLE3[7:0]	7:0	Sub window C gain table 3.	
5Ch (2FB9h)	REG2FB9	7:0	Default : 0x00	Access : R/W
	SUB_C_CORE_TABLE4[7:0]	7:0	Sub window C gain table 4.	
5Dh (2FBAh)	REG2FBA	7:0	Default : 0x00	Access : R/W
	SUB_Y_NOISE_MSK_EN	7	Sub window horizontal Y noise-masking enable.	
	HDE_REF_PANEL_DE_EN	6	As PANEL_DE less than HDE for 1920 PIP.	
	SUB_Y_CF_NOISE_MSK_EN	5	Sub window horizontal Y noise-masking flesh color adaptive enable.	
	SUB_Y_NOISE_MSK_GAIN[4:0]	4:0	Sub window horizontal Y noise-masking gain.	
5Dh (2FBBh)	REG2FBB	7:0	Default : 0x00	Access : R/W
	SUB_C_NOISE_MSK_EN	7	Sub window horizontal C noise-masking enable.	
	-	6	Reserved.	
	SUB_C_CF_NOISE_MSK_EN	5	Sub window horizontal C noise-masking flesh color adaptive enable.	
	SUB_C_NOISE_MSK_GAIN[4:0]	4:0	Sub window horizontal C noise-masking gain.	
60h (2FC0h)	REG2FC0	7:0	Default : 0x00	Access : R/W
	MAIN_IHC_EN	7	Main window IHC enable.	

ACE Register (Bank = 2F, Sub-Bank = 18)

Index (Absolute)	Mnemonic	Bit	Description	
	SUB_IHC_EN	6	Sub window IHC enable.	
	-	5:0	Reserved.	
61h (2FC2h)	REG2FC2	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	MAIN_HUE_USER_R[6:0]	6:0	Main window IHC hue adjustment of R.	
61h (2FC3h)	REG2FC3	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	MAIN_HUE_USER_G[6:0]	6:0	Main window IHC hue adjustment of G.	
62h (2FC4h)	REG2FC4	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	MAIN_HUE_USER_B[6:0]	6:0	Main window IHC hue adjustment of B.	
62h (2FC5h)	REG2FC5	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	MAIN_HUE_USER_C[6:0]	6:0	Main window IHC hue adjustment of C.	
63h (2FC6h)	REG2FC6	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	MAIN_HUE_USER_M[6:0]	6:0	Main window IHC hue adjustment of M.	
63h (2FC7h)	REG2FC7	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	MAIN_HUE_USER_Y[6:0]	6:0	Main window IHC hue adjustment of Y.	
64h (2FC8h)	REG2FC8	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	MAIN_HUE_USER_F[6:0]	6:0	Main window IHC hue adjustment of F.	
65h (2FCAh)	REG2FCA	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	SUB_HUE_USER_R[6:0]	6:0	Sub window IHC hue adjustment of R.	
65h (2FCBh)	REG2FCB	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	SUB_HUE_USER_G[6:0]	6:0	Sub window IHC hue adjustment of G.	
66h (2FCCh)	REG2FCC	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	SUB_HUE_USER_B[6:0]	6:0	Sub window IHC hue adjustment of B.	
66h	REG2FCD	7:0	Default : 0x00	Access : R/W

ACE Register (Bank = 2F, Sub-Bank = 18)

Index (Absolute)	Mnemonic	Bit	Description	
(2FCDh)	-	7	Reserved.	
	SUB_HUE_USER_C[6:0]	6:0	Sub window IHC hue adjustment of C.	
67h (2FCEh)	REG2FCE	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	SUB_HUE_USER_M[6:0]	6:0	Sub window IHC hue adjustment of M.	
67h (2FCFh)	REG2FCF	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	SUB_HUE_USER_Y[6:0]	6:0	Sub window IHC hue adjustment of Y.	
68h (2FD0h)	REG2FD0	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	SUB_HUE_USER_F[6:0]	6:0	Sub window IHC hue adjustment of F.	

Peaking Register (Bank = 2F, Sub-Bank = 19)

Index (Absolute)	Mnemonic	Bit	Description	
10h (2F20h)	REG2F20	7:0	Default : 0x00	Access : R/W
	VPS_SRAM_ACT	7	2D peaking line-buffer SRAM active.	
	MAIN_Y_LPF_COEF[2:0]	6:4	Main window horizontal Y low pass filter coefficient.	
	SUB_IS_MWE_EN	3	Sub window is MWE.	
	-	2:1	Reserved.	
	MAIN_POST_PEAK_EN	0	Main window 2D peaking enable.	
10h (2F21h)	REG2F21	7:0	Default : 0x00	Access : R/W
	MAIN_BAND8_PEAK_EN	7	Main window band8 peaking enable.	
	MAIN_BAND7_PEAK_EN	6	Main window band7 peaking enable.	
	MAIN_BAND6_PEAK_EN	5	Main window band6 peaking enable.	
	MAIN_BAND5_PEAK_EN	4	Main window band5 peaking enable.	
	MAIN_BAND4_PEAK_EN	3	Main window band4 peaking enable.	
	MAIN_BAND3_PEAK_EN	2	Main window band3 peaking enable.	
	MAIN_BAND2_PEAK_EN	1	Main window band2 peaking enable.	
	MAIN_BAND1_PEAK_EN	0	Main window band1 peaking enable.	
11h (2F22h)	REG2F22	7:0	Default : 0x00	Access : R/W
	MAIN_BAND4_COEF_STEP[1:0]	7:6	Main window band4 coefficient step.	
	MAIN_BAND3_COEF_STEP[1:0]	5:4	Main window band3 coefficient step.	
	MAIN_BAND2_COEF_STEP[1:0]	3:2	Main window band2 coefficient step.	
	MAIN_BAND1_COEF_STEP[1:0]	1:0	Main window band1 coefficient step.	
11h (2F23h)	REG2F23	7:0	Default : 0x00	Access : R/W
	MAIN_BAND8_COEF_STEP[1:0]	7:6	Main window band8 coefficient step.	
	MAIN_BAND7_COEF_STEP[1:0]	5:4	Main window band7 coefficient step.	
	MAIN_BAND6_COEF_STEP[1:0]	3:2	Main window band6 coefficient step.	
	MAIN_BAND5_COEF_STEP[1:0]	1:0	Main window band5 coefficient step.	
12h (2F24h)	REG2F24	7:0	Default : -	Access : -
	-	7:0	Reserved.	
12h (2F25h)	REG2F25	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	MAIN_V_LPF_COEF_2[2:0]	6:4	Main window vertical central pixel Y LPF coefficient.	
	-	3	Reserved.	

Peaking Register (Bank = 2F, Sub-Bank = 19)

Index (Absolute)	Mnemonic	Bit	Description	
	MAIN_V_LPF_COEF_1[2:0]	2:0	Main window vertical up-down pixel Y LPF coefficient.	
13h (2F26h)	REG2F26	7:0	Default : 0x00	Access : R/W
	MAIN_COR_THRD_2[3:0]	7:4	Main window coring threshold 2.	
	MAIN_COR_THRD_1[3:0]	3:0	Main window coring threshold 1.	
13h (2F27h)	REG2F27	7:0	Default : 0x10	Access : R/W
	-	7:6	Reserved.	
	MAIN_OSD_SHARP_CTRL[5:0]	5:0	Main window user sharpness adjust.	
14h (2F28h)	REG2F28	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	MAIN_SUB_EXCH_EN	3	Main/Sub window swap enable.	
	-	2	Reserved.	
	SUB_POST_PEAK_EN	0	Sub window 2D peaking enable.	
14h (2F29h)	REG2F29	7:0	Default : 0x00	Access : R/W
	SUB_BAND8_PEAK_EN	7	Sub window band8 peaking enable.	
	SUB_BAND7_PEAK_EN	6	Sub window band7 peaking enable.	
	SUB_BAND6_PEAK_EN	5	Sub window band6 peaking enable.	
	SUB_BAND5_PEAK_EN	4	Sub window band5 peaking enable.	
	SUB_BAND4_PEAK_EN	3	Sub window band4 peaking enable.	
	SUB_BAND3_PEAK_EN	2	Sub window band3 peaking enable.	
	SUB_BAND2_PEAK_EN	1	Sub window band2 peaking enable.	
	SUB_BAND1_PEAK_EN	0	Sub window band1 peaking enable.	
15h (2F2Ah)	REG2F2A	7:0	Default : 0x00	Access : R/W
	SUB_BAND4_COEF_STEP[1:0]	7:6	Sub window band4 coefficient step.	
	SUB_BAND3_COEF_STEP[1:0]	5:4	Sub window band3 coefficient step.	
	SUB_BAND2_COEF_STEP[1:0]	3:2	Sub window band2 coefficient step.	
	SUB_BAND1_COEF_STEP[1:0]	1:0	Sub window band1 coefficient step.	
15h (2F2Bh)	REG2F2B	7:0	Default : 0x00	Access : R/W
	SUB_BAND8_COEF_STEP[1:0]	7:6	Sub window band8 coefficient step.	
	SUB_BAND7_COEF_STEP[1:0]	5:4	Sub window band7 coefficient step.	
	SUB_BAND6_COEF_STEP[1:0]	3:2	Sub window band6 coefficient step.	
	SUB_BAND5_COEF_STEP[1:0]	1:0	Sub window band5 coefficient step.	
16h (2F2Ch)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	

Peaking Register (Bank = 2F, Sub-Bank = 19)

Index (Absolute)	Mnemonic	Bit	Description	
16h (2F2Dh)	REG2F2D	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	SUB_V_LPF_COEF_2[2:0]	6:4	Sub window vertical central pixel Y LPF coefficient.	
	-	3	Reserved.	
	SUB_V_LPF_COEF_1[2:0]	2:0	Sub window vertical up-down pixel Y LPF coefficient.	
17h (2F2Eh)	REG2F2E	7:0	Default : 0x00	Access : R/W
	SUB_COR_THRD_2[3:0]	7:4	Sub window coring threshold 2.	
	SUB_COR_THRD_1[3:0]	3:0	Sub window coring threshold 1.	
17h (2F2Fh)	REG2F2F	7:0	Default : 0x10	Access : R/W
	-	7:6	Reserved.	
	SUB_OSD_SHARPNESS_CTRL[5:0]	5:0	Sub window user sharpness adjust.	
14h ~ 17h (2F29h ~ 2F2Fh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
18h (2F30h)	REG2F30	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	MAIN_BAND1_COEF[5:0]	5:0	Main window band1 coefficient.	
18h (2F31h)	REG2F31	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	MAIN_BAND2_COEF[5:0]	5:0	Main window band2 coefficient.	
19h (2F32h)	REG2F32	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	MAIN_BAND3_COEF[5:0]	5:0	Main window band3 coefficient.	
19h (2F33h)	REG2F33	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	MAIN_BAND4_COEF[5:0]	5:0	Main window band4 coefficient.	
1Ah (2F34h)	REG2F34	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	MAIN_BAND5_COEF[5:0]	5:0	Main window band5 coefficient.	
1Ah (2F35h)	REG2F35	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	MAIN_BAND6_COEF[5:0]	5:0	Main window band6 coefficient.	

Peaking Register (Bank = 2F, Sub-Bank = 19)

Index (Absolute)	Mnemonic	Bit	Description	
1Bh (2F36h)	REG2F36	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	MAIN_BAND7_COEF[5:0]	5:0	Main window band7 coefficient.	
1Bh (2F37h)	REG2F37	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	MAIN_BAND8_COEF[5:0]	5:0	Main window band8 coefficient.	
1Ch ~ 27h (2F38h ~ 2F4Fh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
28h (2F50h)	REG2F50	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	SUB_BAND1_COEF[5:0]	5:0	Sub window band1 coefficient.	
28h (2F51h)	REG2F51	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	SUB_BAND2_COEF[5:0]	5:0	Sub window band2 coefficient.	
29h (2F52h)	REG2F52	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	SUB_BAND3_COEF[5:0]	5:0	Sub window band3 coefficient.	
29h (2F53h)	REG2F53	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	SUB_BAND4_COEF[5:0]	5:0	Sub window band4 coefficient.	
2Ah (2F54h)	REG2F54	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	SUB_BAND5_COEF[5:0]	5:0	Sub window band5 coefficient.	
2Ah (2F55h)	REG2F55	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	SUB_BAND6_COEF[5:0]	5:0	Sub window band6 coefficient.	
2Bh (2F56h)	REG2F56	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	SUB_BAND7_COEF[5:0]	5:0	Sub window band7 coefficient.	
2Bh (2F57h)	REG2F57	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	SUB_BAND8_COEF[5:0]	5:0	Sub window band8 coefficient.	

Peaking Register (Bank = 2F, Sub-Bank = 19)

Index (Absolute)	Mnemonic	Bit	Description	
2Ch ~ 30h (2F58h ~ 2F60h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
30h (2F61h)	REG2F61	7:0	Default : 0x33	Access : R/W
	-	7:6	Reserved.	
	MAIN_COR_THRD_STEP	5:4	Main window coring step.	
	-	3:2	Reserved.	
	SUB_COR_THRD_STEP	1:0	Sub window coring step.	
31h ~ 32h (2F62h ~ 2F65h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
33h (2F66h)	REG2F66	7:0	Default : 0x00	Access : R/W
	MAIN_BAND2_COR_THRD[3:0]	7:4	Main window band2 coring threshold.	
	MAIN_BAND1_COR_THRD[3:0]	3:0	Main window band1 coring threshold.	
33h (2F67h)	REG2F67	7:0	Default : 0x00	Access : R/W
	MAIN_BAND4_COR_THRD[3:0]	7:4	Main window band4 coring threshold.	
	MAIN_BAND3_COR_THRD[3:0]	3:0	Main window band3 coring threshold.	
34h (2F68h)	REG2F68	7:0	Default : 0x00	Access : R/W
	MAIN_BAND6_COR_THRD[3:0]	7:4	Main window band6 coring threshold.	
	MAIN_BAND5_COR_THRD[3:0]	3:0	Main window band5 coring threshold.	
34h (2F69h)	REG2F69	7:0	Default : 0x00	Access : R/W
	MAIN_BAND8_COR_THRD[3:0]	7:4	Main window band8 coring threshold.	
	MAIN_BAND7_COR_THRD[3:0]	3:0	Main window band7 coring threshold.	
35h (2F6Ah)	REG2F6A	7:0	Default : 0x00	Access : R/W
	SUB_BAND2_COR_THRD[3:0]	7:4	Sub window band2 coring threshold.	
	SUB_BAND1_COR_THRD[3:0]	3:0	Sub window band1 coring threshold.	
35h (2F6Bh)	REG2F6B	7:0	Default : 0x00	Access : R/W
	SUB_BAND4_COR_THRD[3:0]	7:4	Sub window band4 coring threshold.	
	SUB_BAND3_COR_THRD[3:0]	3:0	Sub window band3 coring threshold.	
36h (2F6Ch)	REG2F6C	7:0	Default : 0x00	Access : R/W
	SUB_BAND6_COR_THRD[3:0]	7:4	Sub window band6 coring threshold.	
	SUB_BAND5_COR_THRD[3:0]	3:0	Sub window band5 coring threshold.	
36h (2F6Dh)	REG2F6D	7:0	Default : 0x00	Access : R/W
	SUB_BAND8_COR_THRD[3:0]	7:4	Sub window band8 coring threshold.	

Peaking Register (Bank = 2F, Sub-Bank = 19)

Index (Absolute)	Mnemonic	Bit	Description	
	SUB_BAND7_COR_THRD[3:0]	3:0	Sub window band7 coring threshold.	
37h ~ 5Fh (2F6Eh ~ 2FBFh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
60h (2FC0h)	REG2FC0	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	MAIN_GAUSS_LUT_STEP[1:0]	5:4	Main window Gaussian SNR LUT step.	
	-	3:1	Reserved.	
	MAIN_GAUSS_NR_EN	0	Main window Gaussian SNR enable.	
60h (2FC1h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
61h (2FC2h)	REG2FC2	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	SUB_GAUSS_LUT_STEP[1:0]	5:4	Sub window Gaussian SNR LUT step.	
	-	3:0	Reserved.	
61h (2FC3h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
64h (2FC8h)	REG2FC8	7:0	Default : 0x00	Access : R/W
	SNR_LUT_0[7:0]	7:0	Gaussian SNR Table 0.	
64h (2FC9h)	REG2FC9	7:0	Default : 0x00	Access : R/W
	SNR_LUT_1[7:0]	7:0	Gaussian SNR Table 1.	
65h (2FCAh)	REG2FCA	7:0	Default : 0x00	Access : R/W
	SNR_LUT_2[7:0]	7:0	Gaussian SNR Table 2.	
65h (2FCBh)	REG2FCB	7:0	Default : 0x00	Access : R/W
	SNR_LUT_3[7:0]	7:0	Gaussian SNR Table 3.	
66h (2FCCh)	REG2FCC	7:0	Default : 0x00	Access : R/W
	SNR_LUT_4[7:0]	7:0	Gaussian SNR Table 4.	
66h (2FCDh)	REG2FCD	7:0	Default : 0x00	Access : R/W
	SNR_LUT_5[7:0]	7:0	Gaussian SNR Table 5.	
67h (2FCEh)	REG2FCE	7:0	Default : 0x00	Access : R/W
	SNR_LUT_6[7:0]	7:0	Gaussian SNR Table 6.	
67h (2FCFh)	REG2FCF	7:0	Default : 0x00	Access : R/W
	SNR_LUT_7[7:0]	7:0	Gaussian SNR Table 7.	

DLC Register (Bank = 2F, Sub-Bank = 1A)

Index (Absolute)	Mnemonic	Bit	Description	
01h (2F02h)	**REG2F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_STAT_V_START[7:0]	7:0	Main window histogram vertical start.	
01h (2F03h)	**REG2F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_STAT_V_END[7:0]	7:0	Main window histogram vertical end.	
03h (2F06h)	**REG2F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_STAT_V_START[7:0]	7:0	Sub window histogram vertical start.	
03h (2F07h)	**REG2F07**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_STAT_V_END[7:0]	7:0	Sub window histogram vertical end.	
04h (2F08h)	**REG2F08**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	MAIN_CRV_FIT_EN	7	Main window luma curve enable.	
	SUB_CRV_FIT_EN	6	Sub window luma curve enable.	
	YCV_DITH_EN	5	Y curve fit dither enable.	
	HIST_MD	4	0: 3 section. 1: 8 section.	
	STAT_ACK	3	Histogram acknowledged.	
	STAT_REQ	2	Histogram request.	
	MAIN_STAT_EN	1	Main window statistic enable.	
	SUB_STAT_EN	0	Sub window statistic enable.	
04h (2F09h)	**REG2F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	STAT_LOCATE[1:0]	7:6	Statistic locate. 00: Original location, after Y adjust. 01: Before Y adjust. 10: After color engine.	
	-	5:1	Reserved.	
	VARIABLE_RANGE_EN	0	Variable 8 section of histogram enable.	
05h (2F0Ah)	**REG2F0A**	**7:0**	**Default : 0x44**	**Access : R/W**
	DARK_LVL[7:0]	7:0	Dark level for 3 section histogram.	
05h (2F0Bh)	**REG2F0B**	**7:0**	**Default : 0xAA**	**Access : R/W**
	LIGHT_LVL[7:0]	7:0	Light level for 3 section histogram.	
06h (2F0Ch)	**REG2F0C**	**7:0**	**Default : -**	**Access : RO**
	TOTAL_PIX_WT[7:0]	7:0	Histogram report sum of total Y.	
06h	**REG2F0D**	**7:0**	**Default : -**	**Access : RO**

DLC Register (Bank = 2F, Sub-Bank = 1A)

Index (Absolute)	Mnemonic	Bit	Description	
(2F0Dh)	TOTAL_PIX_WT[15:8]	7:0	Please see description of '2F0Ch'.	
07h (2F0Eh)	REG2F0E	7:0	Default : -	Access : RO
	TOTAL_PIX_CNT[7:0]	7:0	Histogram report sum of pixel number.	
07h (2F0Fh)	REG2F0F	7:0	Default : -	Access : RO
	TOTAL_PIX_CNT[15:8]	7:0	Please see description of '2F0Eh'.	
08h (2F10h)	REG2F10	7:0	Default : 0x00	Access : R/W
	MAIN_RANGE_EN	7	Main window histogram range enable.	
	MAIN_BLE_EN	6	Firmware main window black level extension enable.	
	MAIN_WLE_EN	5	Firmware main window white level extension enable.	
	-	4	Reserved.	
	SUB_RANGE_EN	3	Sub window histogram range enable.	
	SUB	2	Firmware sub window black level extension enable.	
	SUB_WLE_EN	1	Firmware sub window white level extension enable.	
	-	0	Reserved.	
09h (2F12h)	REG2F12	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	BLE_UPR_BOUND[5:0]	5:0	Firmware black level extension upper bound.	
09h (2F13h)	REG2F13	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	BLE_LOW_BOUND[5:0]	5:0	Firmware black level extension lower bound.	
0Ah (2F14h)	REG2F14	7:0	Default : 0x3F	Access : R/W
	-	7:6	Reserved.	
	WLE_UPR_BOUND[5:0]	5:0	Firmware white level extension upper bound.	
0Ah (2F15h)	REG2F15	7:0	Default : 0x3F	Access : R/W
	-	7:6	Reserved.	
	WLE_LOW_BOUND[5:0]	5:0	Firmware white level extension lower bound.	
0Bh (2F16h)	REG2F16	7:0	Default : -	Access : RO
	MAIN_MAX_PIX[7:0]	7:0	Main window minimum pixel.	
0Bh (2F17h)	REG2F17	7:0	Default : -	Access : RO
	MAIN_MIN_PIX[7:0]	7:0	Main window maximum pixel.	
0Ch (2F18h)	REG2F18	7:0	Default : -	Access : RO
	SUB_MAX_PIX[7:0]	7:0	Sub window minimum pixel.	
0Ch	REG2F19	7:0	Default : -	Access : RO

DLC Register (Bank = 2F, Sub-Bank = 1A)

Index (Absolute)	Mnemonic	Bit	Description	
(2F19h)	SUB_MIN_PIXEL[7:0]	7:0	Sub window maximum pixel.	
0Dh (2F1Ah)	REG2F1A	7:0	Default : -	Access : RO
	TOTAL_LUMA_LVL[7:0]	7:0	Number of picture luma lvel appear.	
0Eh (2F1Ch)	REG2F1C	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	MAIN_BRI_ADJUST_LSB[1:0]	1:0	Main window Y adjust low bit.	
0Eh (2F1Dh)	REG2F1D	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SUB_BRI_ADJ_LSB[1:0]	1:0	Sub window Y adjust low bit.	
0Fh (2F1Eh)	REG2F1E	7:0	Default : 0x00	Access : R/W
	MAIN_BRI_ADJ[7:0]	7:0	Main window Y adjust.	
0Fh (2F1Fh)	REG2F1F	7:0	Default : 0x00	Access : R/W
	SUB_BRI_ADJ[7:0]	7:0	Sub window Y adjust.	
10h (2F20h)	REG2F20	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	MAIN_BLACK_START[6:0]	6:0	Main window black start.	
10h (2F21h)	REG2F21	7:0	Default : 0x80	Access : R/W
	MAIN_BLACK_SLOP[7:0]	7:0	Main window black slope.	
11h (2F22h)	REG2F22	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	MAIN_WHITE_START[6:0]	6:0	Main window white start.	
11h (2F23h)	REG2F23	7:0	Default : 0x80	Access : R/W
	MAIN_WHITE_SLOP[7:0]	7:0	Main window white slope.	
12h (2F24h)	REG2F24	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	SUB_BLACK_START[6:0]	6:0	Sub window black start.	
12h (2F25h)	REG2F25	7:0	Default : 0x80	Access : R/W
	SUB_BLACK_SLOP[7:0]	7:0	Sub window black slope.	
13h (2F26h)	REG2F26	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	SUB_WHITE_START[6:0]	6:0	Sub window white start.	
13h (2F27h)	REG2F27	7:0	Default : 0x80	Access : R/W
	SUB_WHITE_SLOP[7:0]	7:0	Sub window white slope.	

DLC Register (Bank = 2F, Sub-Bank = 1A)

Index (Absolute)	Mnemonic	Bit	Description	
14h (2F28h)	REG2F28	7:0	Default : 0x40	Access : R/W
	MAIN_Y_GAIN[7:0]	7:0	Main window Y gain.	
14h (2F29h)	REG2F29	7:0	Default : 0x40	Access : R/W
	MAIN_C_GAIN[7:0]	7:0	Main window C gain.	
15h (2F2Ah)	REG2F2A	7:0	Default : 0x40	Access : R/W
	SUB_Y_GAIN[7:0]	7:0	Sub window Y gain.	
15h (2F2Bh)	REG2F2B	7:0	Default : 0x40	Access : R/W
	SUB_C_GAIN[7:0]	7:0	Sub window C gain.	
1Ch (2F38h)	REG2F38	7:0	Default : 0x20	Access : R/W
	HIST_RANGE1[7:0]	7:0	Variable 8 section of histogram range 1.	
1Ch (2F39h)	REG2F39	7:0	Default : 0x40	Access : R/W
	HIST_RANGE2[7:0]	7:0	Variable 8 section of histogram range 2.	
1Dh (2F3Ah)	REG2F3A	7:0	Default : 0x60	Access : R/W
	HIST_RANGE3[7:0]	7:0	Variable 8 section of histogram range 3.	
1Dh (2F3Bh)	REG2F3B	7:0	Default : 0x80	Access : R/W
	HIST_RANGE4[7:0]	7:0	Variable 8 section of histogram range 4.	
1Eh (2F3Ch)	REG2F3C	7:0	Default : 0xA0	Access : R/W
	HIST_RANGE5[7:0]	7:0	Variable 8 section of histogram range 5.	
1Eh (2F3Dh)	REG2F3D	7:0	Default : 0xC0	Access : R/W
	HIST_RANGE6[7:0]	7:0	Variable 8 section of histogram range 6.	
1Fh (2F3Eh)	REG2F3E	7:0	Default : 0xE0	Access : R/W
	HIST_RANGE7[7:0]	7:0	Variable 8 section of histogram range 7.	
20h (2F40h)	REG2F40	7:0	Default : 0x00	Access : R/W
	GPR_REG_0[7:0]	7:0	DLC general purpose register 0.	
20h (2F41h)	REG2F41	7:0	Default : 0x00	Access : R/W
	GPR_REG_0[15:8]	7:0	Please see description of '2F40h'.	
21h (2F42h)	REG2F42	7:0	Default : 0x00	Access : R/W
	GPR_REG_1[7:0]	7:0	DLC general purpose register 1.	
21h (2F43h)	REG2F43	7:0	Default : 0x00	Access : R/W
	GPR_REG_1[15:8]	7:0	Please see description of '2F42h'.	
22h (2F44h)	REG2F44	7:0	Default : 0x00	Access : R/W
	GPR_REG_2[7:0]	7:0	DLC general purpose register 2.	
22h	REG2F45	7:0	Default : 0x00	Access : R/W

DLC Register (Bank = 2F, Sub-Bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F45h)	GPR_REG_2[15:8]	7:0	Please see description of '2F44h'.	
23h (2F46h)	**REG2F46**	**7:0**	**Default : 0x00**	Access : R/W
	GPR_REG_3[7:0]	7:0	DLC general purpose register 3.	
23h (2F47h)	**REG2F47**	**7:0**	**Default : 0x00**	Access : R/W
	GPR_REG_3[15:8]	7:0	Please see description of '2F46h'.	
24h (2F48h)	**REG2F48**	**7:0**	**Default : 0x11**	Access : R/W
	GPR_REG_4[7:0]	7:0	DLC general purpose register 4.	
24h (2F49h)	**REG2F49**	**7:0**	**Default : 0x11**	Access : R/W
	GPR_REG_4[15:8]	7:0	Please see description of '2F48h'.	
25h (2F4Ah)	**REG2F4A**	**7:0**	**Default : 0x11**	Access : R/W
	GPR_REG_5[7:0]	7:0	DLC general purpose register 5.	
25h (2F4Bh)	**REG2F4B**	**7:0**	**Default : 0x11**	Access : R/W
	GPR_REG_5[15:8]	7:0	Please see description of '2F4Ah'.	
26h (2F4Ch)	**REG2F4C**	**7:0**	**Default : 0x11**	Access : R/W
	GPR_REG_6[7:0]	7:0	DLC general purpose register 6.	
26h (2F4Dh)	**REG2F4D**	**7:0**	**Default : 0x11**	Access : R/W
	GPR_REG_6[15:8]	7:0	Please see description of '2F4Ch'.	
27h (2F4Eh)	**REG2F4E**	**7:0**	**Default : 0x11**	Access : R/W
	GPR_REG_7[7:0]	7:0	DLC general purpose register 7.	
27h (2F4Fh)	**REG2F4F**	**7:0**	**Default : 0x11**	Access : R/W
	GPR_REG_7[15:8]	7:0	Please see description of '2F4Eh'.	
28h (2F50h)	**REG2F50**	**7:0**	**Default : -**	Access : RO
	TOTAL_1F_00[7:0]	7:0	Histogram report section1.	
28h (2F51h)	**REG2F51**	**7:0**	**Default : -**	Access : RO
	TOTAL_1F_00[15:8]	7:0	Please see description of '2F50h'.	
29h (2F52h)	**REG2F52**	**7:0**	**Default : -**	Access : RO
	TOTAL_3F_20[7:0]	7:0	Histogram report section2.	
29h (2F53h)	**REG2F53**	**7:0**	**Default : -**	Access : RO
	TOTAL_3F_20[15:8]	7:0	Please see description of '2F52h'.	
2Ah (2F54h)	**REG2F54**	**7:0**	**Default : -**	Access : RO
	TOTAL_5F_40[7:0]	7:0	Histogram report section3.	
2Ah (2F55h)	**REG2F55**	**7:0**	**Default : -**	Access : RO
	TOTAL_5F_40[15:8]	7:0	Please see description of '2F54h'.	

DLC Register (Bank = 2F, Sub-Bank = 1A)

Index (Absolute)	Mnemonic	Bit	Description	
2Bh (2F56h)	REG2F56	7:0	Default : -	Access : RO
	TOTAL_7F_60[7:0]	7:0	Histogram report section4.	
2Bh (2F57h)	REG2F57	7:0	Default : -	Access : RO
	TOTAL_7F_60[15:8]	7:0	Please see description of '2F56h'.	
2Ch (2F58h)	REG2F58	7:0	Default : -	Access : RO
	TOTAL_9F_80[7:0]	7:0	Histogram report section5.	
2Ch (2F59h)	REG2F59	7:0	Default : -	Access : RO
	TOTAL_9F_80[15:8]	7:0	Please see description of '2F58h'.	
2Dh (2F5Ah)	REG2F5A	7:0	Default : -	Access : RO
	TOTAL_BF_A0[7:0]	7:0	Histogram report section6.	
2Dh (2F5Bh)	REG2F5B	7:0	Default : -	Access : RO
	TOTAL_BF_A0[15:8]	7:0	Please see description of '2F5Ah'.	
2Eh (2F5Ch)	REG2F5C	7:0	Default : -	Access : RO
	TOTAL_DF_C0[7:0]	7:0	Histogram report section7.	
2Eh (2F5Dh)	REG2F5D	7:0	Default : -	Access : RO
	TOTAL_DF_C0[15:8]	7:0	Please see description of '2F5Ch'.	
2Fh (2F5Eh)	REG2F5E	7:0	Default : -	Access : RO
	TOTAL_FF_E0[7:0]	7:0	Histogram report section8.	
2Fh (2F5Fh)	REG2F5F	7:0	Default : -	Access : RO
	TOTAL_FF_E0[15:8]	7:0	Please see description of '2F5Eh'.	
30h (2F60h)	REG2F60	7:0	Default : 0x08	Access : R/W
	MAIN_CURVE_FIT_TABLE_0[7:0]	7:0	Main window curve table 0.	
30h (2F61h)	REG2F61	7:0	Default : 0x18	Access : R/W
	MAIN_CURVE_FIT_TABLE_1[7:0]	7:0	Main window curve table 1.	
31h (2F62h)	REG2F62	7:0	Default : 0x28	Access : R/W
	MAIN_CURVE_FIT_TABLE_2[7:0]	7:0	Main window curve table 2.	
31h (2F63h)	REG2F63	7:0	Default : 0x38	Access : R/W
	MAIN_CURVE_FIT_TABLE_3[7:0]	7:0	Main window curve table 3.	
32h (2F64h)	REG2F64	7:0	Default : 0x48	Access : R/W
	MAIN_CURVE_FIT_TABLE_4[7:0]	7:0	Main window curve table 4.	
32h (2F65h)	REG2F65	7:0	Default : 0x58	Access : R/W
	MAIN_CURVE_FIT_TABLE_5[7:0]	7:0	Main window curve table 5.	
33h	REG2F66	7:0	Default : 0x68	Access : R/W

DLC Register (Bank = 2F, Sub-Bank = 1A)

Index (Absolute)	Mnemonic	Bit	Description	
(2F66h)	MAIN_CURVE_FIT_TABLE_6[7:0]	7:0	Main window curve table 6.	
33h (2F67h)	REG2F67	7:0	Default : 0x78	Access : R/W
	MAIN_CURVE_FIT_TABLE_7[7:0]	7:0	Main window curve table 7.	
34h (2F68h)	REG2F68	7:0	Default : 0x88	Access : R/W
	MAIN_CURVE_FIT_TABLE_8[7:0]	7:0	Main window curve table 8.	
34h (2F69h)	REG2F69	7:0	Default : 0x98	Access : R/W
	MAIN_CURVE_FIT_TABLE_9[7:0]	7:0	Main window curve table 9.	
35h (2F6Ah)	REG2F6A	7:0	Default : 0xA8	Access : R/W
	MAIN_CURVE_FIT_TABLE_10[7:0]	7:0	Main window curve table 10.	
35h (2F6Bh)	REG2F6B	7:0	Default : 0x00	Access : R/W
	MAIN_CURVE_FIT_TABLE_11[7:0]	7:0	Main window curve table 11.	
36h (2F6Ch)	REG2F6C	7:0	Default : 0xC8	Access : R/W
	MAIN_CURVE_FIT_TABLE_12[7:0]	7:0	Main window curve table 12.	
36h (2F6Dh)	REG2F6D	7:0	Default : 0xD8	Access : R/W
	MAIN_CURVE_FIT_TABLE_13[7:0]	7:0	Main window curve table 13.	
37h (2F6Eh)	REG2F6E	7:0	Default : 0xE8	Access : R/W
	MAIN_CURVE_FIT_TABLE_14[7:0]	7:0	Main window curve table 14.	
37h (2F6Fh)	REG2F6F	7:0	Default : 0xF8	Access : R/W
	MAIN_CURVE_FIT_TABLE_15[7:0]	7:0	Main window curve table 15.	
38h (2F70h)	REG2F70	7:0	Default : 0x08	Access : R/W
	SUB_CURVE_FIT_TABLE_0[7:0]	7:0	Sub window curve table 0.	
38h (2F71h)	REG2F71	7:0	Default : 0x18	Access : R/W
	SUB_CURVE_FIT_TABLE_1[7:0]	7:0	Sub window curve table 1.	
39h (2F72h)	REG2F72	7:0	Default : 0x28	Access : R/W
	SUB_CURVE_FIT_TABLE_2[7:0]	7:0	Sub window curve table 2.	
39h (2F73h)	REG2F73	7:0	Default : 0x38	Access : R/W
	SUB_CURVE_FIT_TABLE_3[7:0]	7:0	Sub window curve table 3.	
3Ah	REG2F74	7:0	Default : 0x48	Access : R/W

DLC Register (Bank = 2F, Sub-Bank = 1A)

Index (Absolute)	Mnemonic	Bit	Description	
(2F74h)	SUB_CURVE_FIT_TABLE_4[7:0]	7:0	Sub window curve table 4.	
3Ah (2F75h)	REG2F75	7:0	Default : 0x58	Access : R/W
	SUB_CURVE_FIT_TABLE_5[7:0]	7:0	Sub window curve table 5.	
3Bh (2F76h)	REG2F76	7:0	Default : 0x68	Access : R/W
	SUB_CURVE_FIT_TABLE_6[7:0]	7:0	Sub window curve table 6.	
3Bh (2F77h)	REG2F77	7:0	Default : 0x78	Access : R/W
	SUB_CURVE_FIT_TABLE_7[7:0]	7:0	Sub window curve table 7.	
3Ch (2F78h)	REG2F78	7:0	Default : 0x88	Access : R/W
	SUB_CURVE_FIT_TABLE_8[7:0]	7:0	Sub window curve table 8.	
3Ch (2F79h)	REG2F79	7:0	Default : 0x98	Access : R/W
	SUB_CURVE_FIT_TABLE_9[7:0]	7:0	Sub wndow curve table 9.	
3Dh (2F7Ah)	REG2F7A	7:0	Default : 0xA8	Access : R/W
	SUB_CURVE_FIT_TABLE_10[7:0]	7:0	Sub window curve table 10.	
3Dh (2F7Bh)	REG2F7B	7:0	Default : 0x00	Access : R/W
	SUB_CURVE_FIT_TABLE_11[7:0]	7:0	Sub window curve table 11.	
3Eh (2F7Ch)	REG2F7C	7:0	Default : 0xC8	Access : R/W
	SUB_CURVE_FIT_TABLE_12[7:0]	7:0	Sub window curve table 12.	
3Eh (2F7Dh)	REG2F7D	7:0	Default : 0xD8	Access : R/W
	SUB_CURVE_FIT_TABLE_13[7:0]	7:0	Sub window curve table 13.	
3Fh (2F7Eh)	REG2F7E	7:0	Default : 0xE8	Access : R/W
	SUB_CURVE_FIT_TABLE_14[7:0]	7:0	Sub window curve table 14.	
3Fh (2F7Fh)	REG2F7F	7:0	Default : 0xF8	Access : R/W
	SUB_CURVE_FIT_TABLE_15[7:0]	7:0	Sub window curve table 15.	
40h (2F80h)	REG2F80	7:0	Default : -	Access : RO
	TOTAL_32_0[7:0]	7:0	Histogram report section 32_0.	
40h (2F81h)	REG2F81	7:0	Default : -	Access : RO
	TOTAL_32_0[15:8]	7:0	Please see description of '2F80h'.	
41h (2F82h)	REG2F82	7:0	Default : -	Access : RO
	TOTAL_32_1[7:0]	7:0	Histogram report section 32_1.	
41h (2F83h)	REG2F83	7:0	Default : -	Access : RO
	TOTAL_32_1[15:8]	7:0	Please see description of '2F82h'.	
42h (2F84h)	REG2F84	7:0	Default : -	Access : RO
	TOTAL_32_2[7:0]	7:0	Histogram report section 32_2.	

DLC Register (Bank = 2F, Sub-Bank = 1A)

Index (Absolute)	Mnemonic	Bit	Description	
42h (2F85h)	REG2F85	7:0	Default : -	Access : RO
	TOTAL_32_2[15:8]	7:0	Please see description of '2F84h'.	
43h (2F86h)	REG2F86	7:0	Default : -	Access : RO
	TOTAL_32_3[7:0]	7:0	Histogram report section 32_3.	
43h (2F87h)	REG2F87	7:0	Default : -	Access : RO
	TOTAL_32_3[15:8]	7:0	Please see description of '2F86h'.	
44h (2F88h)	REG2F88	7:0	Default : -	Access : RO
	TOTAL_32_4[7:0]	7:0	Histogram report section 32_4.	
44h (2F89h)	REG2F89	7:0	Default : -	Access : RO
	TOTAL_32_4[15:8]	7:0	Please see description of '2F88h'.	
45h (2F8Ah)	REG2F8A	7:0	Default : -	Access : RO
	TOTAL_32_5[7:0]	7:0	Histogram report section 32_5.	
45h (2F8Bh)	REG2F8B	7:0	Default : -	Access : RO
	TOTAL_32_5[15:8]	7:0	Please see description of '2F8Ah'.	
46h (2F8Ch)	REG2F8C	7:0	Default : -	Access : RO
	TOTAL_32_6[7:0]	7:0	Histogram report section 32_6.	
46h (2F8Dh)	REG2F8D	7:0	Default : -	Access : RO
	TOTAL_32_6[15:8]	7:0	Please see description of '2F8Ch'.	
47h (2F8Eh)	REG2F8E	7:0	Default : -	Access : RO
	TOTAL_32_7[7:0]	7:0	Histogram report section 32_7.	
47h (2F8Fh)	REG2F8F	7:0	Default : -	Access : RO
	TOTAL_32_7[15:8]	7:0	Please see description of '2F8Eh'.	
48h (2F90h)	REG2F90	7:0	Default : -	Access : RO
	TOTAL_32_8[7:0]	7:0	Histogram report section 32_8.	
48h (2F91h)	REG2F91	7:0	Default : -	Access : RO
	TOTAL_32_8[15:8]	7:0	Please see description of '2F90h'.	
49h (2F92h)	REG2F92	7:0	Default : -	Access : RO
	TOTAL_32_9[7:0]	7:0	Histogram report section 32_9.	
49h (2F93h)	REG2F93	7:0	Default : -	Access : RO
	TOTAL_32_9[15:8]	7:0	Please see description of '2F92h'.	
4Ah (2F94h)	REG2F94	7:0	Default : -	Access : RO
	TOTAL_32_10[7:0]	7:0	Histogram report section 32_10.	
4Ah	REG2F95	7:0	Default : -	Access : RO

DLC Register (Bank = 2F, Sub-Bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F95h)	TOTAL_32_10[15:8]	7:0	Please see description of '2F94h'.	
4Bh (2F96h)	REG2F96	7:0	Default : -	Access : RO
	TOTAL_32_11[7:0]	7:0	Histogram report section 32_11.	
4Bh (2F97h)	REG2F97	7:0	Default : -	Access : RO
	TOTAL_32_11[15:8]	7:0	Please see description of '2F96h'.	
4Ch (2F98h)	REG2F98	7:0	Default : -	Access : RO
	TOTAL_32_12[7:0]	7:0	Histogram report section 32_12.	
4Ch (2F99h)	REG2F99	7:0	Default : -	Access : RO
	TOTAL_32_12[15:8]	7:0	Please see description of '2F98h'.	
4Dh (2F9Ah)	REG2F9A	7:0	Default : -	Access : RO
	TOTAL_32_13[7:0]	7:0	Histogram report section 32_13.	
4Dh (2F9Bh)	REG2F9B	7:0	Default : -	Access : RO
	TOTAL_32_13[15:8]	7:0	Please see description of '2F9Ah'.	
4Eh (2F9Ch)	REG2F9C	7:0	Default : -	Access : RO
	TOTAL_32_14[7:0]	7:0	Histogram report section 32_14.	
4Eh (2F9Dh)	REG2F9D	7:0	Default : -	Access : RO
	TOTAL_32_14[15:8]	7:0	Please see description of '2F9Ch'.	
4Fh (2F9Eh)	REG2F9E	7:0	Default : -	Access : RO
	TOTAL_32_15[7:0]	7:0	Histogram report section 32_15.	
4Fh (2F9Fh)	REG2F9F	7:0	Default : -	Access : RO
	TOTAL_32_15[15:8]	7:0	Please see description of '2F9Eh'.	
50h (2FA0h)	REG2FA0	7:0	Default : -	Access : RO
	TOTAL_32_16[7:0]	7:0	Histogram report section 32_16.	
50h (2FA1h)	REG2FA1	7:0	Default : -	Access : RO
	TOTAL_32_16[15:8]	7:0	Please see description of '2FA0h'.	
51h (2FA2h)	REG2FA2	7:0	Default : -	Access : RO
	TOTAL_32_17[7:0]	7:0	Histogram report section 32_17.	
51h (2FA3h)	REG2FA3	7:0	Default : -	Access : RO
	TOTAL_32_17[15:8]	7:0	Please see description of '2FA2h'.	
52h (2FA4h)	REG2FA4	7:0	Default : -	Access : RO
	TOTAL_32_18[7:0]	7:0	Histogram report section 32_18.	
52h (2FA5h)	REG2FA5	7:0	Default : -	Access : RO
	TOTAL_32_18[15:8]	7:0	Please see description of '2FA4h'.	

DLC Register (Bank = 2F, Sub-Bank = 1A)

Index (Absolute)	Mnemonic	Bit	Description	
53h (2FA6h)	REG2FA6	7:0	Default : -	Access : RO
	TOTAL_32_19[7:0]	7:0	Histogram report section 32_19.	
53h (2FA7h)	REG2FA7	7:0	Default : -	Access : RO
	TOTAL_32_19[15:8]	7:0	Please see description of '2FA6h'.	
54h (2FA8h)	REG2FA8	7:0	Default : -	Access : RO
	TOTAL_32_20[7:0]	7:0	Histogram report section 32_20.	
54h (2FA9h)	REG2FA9	7:0	Default : -	Access : RO
	TOTAL_32_20[15:8]	7:0	Please see description of '2FA8h'.	
55h (2FAAh)	REG2FAA	7:0	Default : -	Access : RO
	TOTAL_32_21[7:0]	7:0	Histogram report section 32_21.	
55h (2FABh)	REG2FAB	7:0	Default : -	Access : RO
	TOTAL_32_21[15:8]	7:0	Please see description of '2FAAh'.	
56h (2FACh)	REG2FAC	7:0	Default : -	Access : RO
	TOTAL_32_22[7:0]	7:0	Histogram report section 32_22.	
56h (2FADh)	REG2FAD	7:0	Default : -	Access : RO
	TOTAL_32_22[15:8]	7:0	Please see description of '2FACh'.	
57h (2FAEh)	REG2FAE	7:0	Default : -	Access : RO
	TOTAL_32_23[7:0]	7:0	Histogram report section 32_23.	
57h (2FAFh)	REG2FAF	7:0	Default : -	Access : RO
	TOTAL_32_23[15:8]	7:0	Please see description of '2FAEh'.	
58h (2FB0h)	REG2FB0	7:0	Default : -	Access : RO
	TOTAL_32_24[7:0]	7:0	Histogram report section 32_24.	
58h (2FB1h)	REG2FB1	7:0	Default : -	Access : RO
	TOTAL_32_24[15:8]	7:0	Please see description of '2FB0h'.	
59h (2FB2h)	REG2FB2	7:0	Default : -	Access : RO
	TOTAL_32_25[7:0]	7:0	Histogram report section 32_25.	
59h (2FB3h)	REG2FB3	7:0	Default : -	Access : RO
	TOTAL_32_25[15:8]	7:0	Please see description of '2FB2h'.	
5Ah (2FB4h)	REG2FB4	7:0	Default : -	Access : RO
	TOTAL_32_26[7:0]	7:0	Histogram report section 32_26.	
5Ah (2FB5h)	REG2FB5	7:0	Default : -	Access : RO
	TOTAL_32_26[15:8]	7:0	Please see description of '2FB4h'.	
5Bh	REG2FB6	7:0	Default : -	Access : RO

DLC Register (Bank = 2F, Sub-Bank = 1A)

Index (Absolute)	Mnemonic	Bit	Description	
(2FB6h)	TOTAL_32_27[7:0]	7:0	Histogram report section 32_27.	
5Bh (2FB7h)	REG2FB7	7:0	Default : -	Access : RO
	TOTAL_32_27[15:8]	7:0	Please see description of '2FB6h'.	
5Ch (2FB8h)	REG2FB8	7:0	Default : -	Access : RO
	TOTAL_32_28[7:0]	7:0	Histogram report section 32_28.	
5Ch (2FB9h)	REG2FB9	7:0	Default : -	Access : RO
	TOTAL_32_28[15:8]	7:0	Please see description of '2FB8h'.	
5Dh (2FBAh)	REG2FBA	7:0	Default : -	Access : RO
	TOTAL_32_29[7:0]	7:0	Histogram report section 32_29.	
5Dh (2FBBh)	REG2FBB	7:0	Default : -	Access : RO
	TOTAL_32_29[15:8]	7:0	Please see description of '2FBAh'.	
5Eh (2FBCh)	REG2FBC	7:0	Default : -	Access : RO
	TOTAL_32_30[7:0]	7:0	Histogram report section 32_30.	
5Eh (2FBDh)	REG2FBD	7:0	Default : -	Access : RO
	TOTAL_32_30[15:8]	7:0	Please see description of '2FBCh'.	
5Fh (2FBEh)	REG2FBE	7:0	Default : -	Access : RO
	TOTAL_32_31[7:0]	7:0	Histogram report section 32_31.	
5Fh (2FBFh)	REG2FBF	7:0	Default : -	Access : RO
	TOTAL_32_31[15:8]	7:0	Please see description of '2FBEh'.	

OP1PIP_EXT Register (Bank = 2F, Sub-Bank = 1B)

Index (Absolute)	Mnemonic	Bit	Description	
OP1PIP_EXT Register (Bank = 2F, Sub-Bank = 1B)				
01h (2F02h)	REG2F02	7:0	Default : 0x00	Access : R/W
	ATP_FLAG	7	PIP auto tune flag for reg_01[6] usage.	
	SUB2VBLK_EN	6	Sub window data pre-fetch in V blanking enable.	
	-	5:0	Reserved.	
10h (2F20h)	REG2F20	7:0	Default : 0x00	Access : R/W
	UBOUND2_M_NUM_F2[3:0]	7:4	Main window ELA upper boundary control #2 manual line number.	
	UBOUND2_M_NUM_F1[3:0]	3:0	Sub window ELA upper boundary control #2 manual line number.	

OP1PIP_EXT Register (Bank = 2F, Sub-Bank = 1B)

Index (Absolute)	Mnemonic	Bit	Description	
10h (2F21h)	REG2F21	7:0	Default : 0x00	Access : R/W
	UBOUND2_EN_F2	7	Main window ELA upper boundary control #2 enable.	
	UBOUND2_M_EN_F2	6	Main window ELA upper boundary control #2 manual enable.	
	UBOUND2_M_ODD_P1_F2	5	Main window ELA upper boundary control #2 odd field plus 1 line.	
	-	4	Reserved.	
	UBOUND2_EN_F1	3	Sub window ELA upper boundary control #2 enable.	
	UBOUND2_M_EN_F1	2	Sub window ELA upper boundary control #2 manual enable.	
	UBOUND2_M_ODD_P1_F1	1	Sub window ELA upper boundary control #2 odd field plus 1 line.	
	-	0	Reserved.	
13h (2F26h)	REG2F26	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	F2A_TO_F2AA	5	F2A to F2AA for case3 PIP.	
	-	4:3	Reserved.	
	SYNC_MIU_OP1_F2_EN	2	Sync MIU_F2_EN and OP1_F2_EN, for deinterlace.	
	SYNC_MIU_OP1_F1_EN	1	Sync MIU_F1_EN and OP1_F1_EN, for deinterlace.	
	-	0	Reserved.	
13h (2F27h)	REG2F27	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	AB2F_CTRL	3	PIP A, B sections merge control 1.	
	MASK_B_CTRL	2	PIP A, B sections merge control 2.	
	-	1:0	Reserved.	
18h (2F31h)	REG2F31	7:0	Default : 0x00	Access : R/W
	ELA_UBOUND_EN_MAIN	7	Main window ELA upper boundary control enable.	
	ELA_UBOUND_MAN_MAIN	6	Main window ELA upper boundary manual control enable.	
	ELA_UBOUND_MAN_SEL_MAIN[1:0]	5:4	Main window ELA upper boundary manual selection.	
	ELA_UBOUND_EN_SUB	3	Sub window ELA upper boundary control enable.	
	ELA_UBOUND_MAN_SUB	2	Sub window ELA upper boundary manual control enable.	
	ELA_UBOUND_MAN_SEL_SUB[1:0]	1:0	Sub window ELA upper boundary manual selection.	

OP1PIP_EXT Register (Bank = 2F, Sub-Bank = 1B)

Index (Absolute)	Mnemonic	Bit	Description	
1Ah (2F35h)	REG2F35	7:0	Default : 0x00	Access : R/W
	TUNE_MASK_SLOWDOWN	7	Mask slowdown when PIP auto tune.	
	TUNE_MASK_AUTOAHEAD	6	Mask auto-ahead when PIP auto tune.	
	-	5:0	Reserved.	
1Ch (2F38h)	REG2F38	7:0	Default : 0x00	Access : R/W
	AH_SUB_END_MSB[2:0]	7:5	MSB 3 part of sub end ahead value.	
	AH_SUB_END_LSB	4	LSB part of sub end ahead value.	
	AH_SUB_ST_MSB[2:0]	3:1	MSB 3 part of sub start ahead value.	
	AH_SUB_ST_LSB	0	LSB part of sub start ahead value.	
1Ch (2F39h)	REG2F39	7:0	Default : 0x00	Access : R/W
	AH_MAIN_END_MSB[2:0]	7:5	MSB 3 part of main end ahead value.	
	AH_MAIN_END_LSB	4	LSB part of main end ahead value.	
	AH_MAIN_ST_MSB[2:0]	3:1	MSB 3 part of main start ahead value.	
	AH_MAIN_ST_LSB	0	LSB part of main start ahead value.	
20h (2F40h)	REG2F40	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	EXRQ_FETCH_NUM_SEL[2:0]	6:4	Extra Request fetch num select. 000: 8 pixels. 001: 16 pixels. 010: 24 pixels. 011: 32 pixels. 100: 64 pixels. 101:128 pixels. 110: 256 pixels. 111: Sub window width.	
	-	3:1	Reserved.	
	EXRQ_EN	0	Extra request enable.	
21h (2F42h)	REG2F42	7:0	Default : 0x00	Access : R/W
	EXRQ_PARA1[7:0]	7:0	Extra request parameter 1.	
21h (2F43h)	REG2F43	7:0	Default : 0x00	Access : R/W
	PREFETCH_CNTR_SELECT	7	Pre-fetch counter select.	
	EXRQ_PARA1[14:8]	6:0	See description of '2F42h'.	
22h (2F44h)	REG2F44	7:0	Default : 0x00	Access : R/W
	EXRQ_PARA2[7:0]	7:0	Extra request parameter 2.	

OP1PIP_EXT Register (Bank = 2F, Sub-Bank = 1B)

Index (Absolute)	Mnemonic	Bit	Description	
22h (2F45h)	REG2F45	7:0	Default : 0x00	Access : R/W
	EXRQ_PARA2[15:8]	7:0	See description of '2F44h'.	
23h (2F46h)	REG2F46	7:0	Default : 0x00	Access : R/W
	EXRQ_PARA3[7:0]	7:0	Extra request parameter 3.	
23h (2F47h)	REG2F47	7:0	Default : 0x00	Access : R/W
	EXRQ_PARA3[15:8]	7:0	See description of '2F46h'.	

DISP_TC Register (Bank = 30)

DISP_TC Register (Bank = 30)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
00h (3000h)	REG3000	7:0	Default : 0x00	Access : R/W
	TCH0END_ODD[7:0]	7:0	H-end value of odd frame for TCON GPO0.
00h (3001h)	REG3001	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.
	LG_MD_0	6	LG mode enable for TCON GPO0.
	HEAD_PROC_EN_0	5	Head protect enable for TCON GPO0.
	HEAD_MD_0	4	Head mode enable for TCON GPO0.
	TCH0END_ODD[11:8]	3:0	Please see description of '3000h'.
01h (3002h)	REG3002	7:0	Default : 0x00	Access : R/W
	TCH1END_ODD[7:0]	7:0	H-end value of odd frame for TCON GPO1.
01h (3003h)	REG3003	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.
	LG_MD_1	6	LG mode enable for TCON GPO1.
	HEAD_PROC_EN_1	5	Head protect enable for TCON GPO1.
	HEAD_MD_1	4	Head mode enable for TCON GPO1.
	TCH1END_ODD[11:8]	3:0	Please see description of '3002h'.
02h (3004h)	REG3004	7:0	Default : 0x00	Access : R/W
	TCH2END_ODD[7:0]	7:0	H-end value of odd frame for TCON GPO2.
02h (3005h)	REG3005	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.
	LG_MD_2	6	LG mode enable for TCON GPO2.
	HEAD_PROC_EN_2	5	Head protect enable for TCON GPO2.
	HEAD_MD_2	4	Head mode enable for TCON GPO2.
	TCH2END_ODD[11:8]	3:0	Please see description of '3004h'.
03h (3006h)	REG3006	7:0	Default : 0x00	Access : R/W
	TCH3END_ODD[7:0]	7:0	H-end value of odd frame for TCON GPO3.
03h (3007h)	REG3007	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.
	LG_MD_3	6	LG mode enable for TCON GPO3.
	HEAD_PROC_EN_3	5	Head protect enable for TCON GPO3.
	HEAD_MD_3	4	Head mode enable for TCON GPO3.

DISP_TC Register (Bank = 30)

Index (Absolute)	Mnemonic	Bit	Description	
	TCH3END_ODD[11:8]	3:0	Please see description of '3006h'.	
04h (3008h)	REG3008	7:0	Default : 0x00	Access : R/W
	TCH4END_ODD[7:0]	7:0	H-end value of odd frame for TCON GPO4.	
04h (3009h)	REG3009	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	LG_MD_4	6	LG mode enable for TCON GPO4.	
	HEAD_PROC_EN_4	5	Head protect enable for TCON GPO4.	
	HEAD_MD_4	4	Head mode enable for TCON GPO4.	
	TCH4END_ODD[11:8]	3:0	Please see description of '3008h'.	
05h (300Ah)	REG300A	7:0	Default : 0x00	Access : R/W
	TCH5END_ODD[7:0]	7:0	H-end value of odd frame for TCON GPO5.	
05h (300Bh)	REG300B	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	LG_MD_5	6	LG mode enable for TCON GPO5.	
	HEAD_PROC_EN_5	5	Head protect enable for TCON GPO5.	
	HEAD_MD_5	4	Head mode enable for TCON GPO5.	
	TCH5END_ODD[11:8]	3:0	Please see description of '300Ah'.	
06h (300Ch)	REG300C	7:0	Default : 0x00	Access : R/W
	TCH6END_ODD[7:0]	7:0	H-end value of odd frame for TCON GPO6.	
06h (300Dh)	REG300D	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	LG_MD_6	6	LG mode enable for TCON GPO6.	
	HEAD_PROC_EN_6	5	Head protect enable for TCON GPO6.	
	HEAD_MD_6	4	Head mode enable for TCON GPO6.	
	TCH6END_ODD[11:8]	3:0	Please see description of '300Ch'.	
07h (300Eh)	REG300E	7:0	Default : 0x00	Access : R/W
	TCH7END_ODD[7:0]	7:0	H-end value of odd frame for TCON GPO7.	
07h (300Fh)	REG300F	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	LG_MD_7	6	LG mode enable for TCON GPO7.	
	HEAD_PROC_EN_7	5	Head protect enable for TCON GPO7.	
	HEAD_MD_7	4	Head mode enable for TCON GPO7.	
	TCH7END_ODD[11:8]	3:0	Please see description of '300Eh'.	

DISP_TC Register (Bank = 30)

Index (Absolute)	Mnemonic	Bit	Description	
08h (3010h)	REG3010	7:0	Default : 0x00	Access : R/W
	TCH8END_ODD[7:0]	7:0	H-end value of odd frame for TCON GPO8.	
08h (3011h)	REG3011	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	LG_MD_8	6	LG mode enable for TCON GPO8.	
	HEAD_PROC_EN_8	5	Head protect enable for TCON GPO8.	
	HEAD_MD_8	4	Head mode enable for TCON GPO8.	
	TCH8END_ODD[11:8]	3:0	Please see description of '3010h'.	
09h (3012h)	REG3012	7:0	Default : 0x00	Access : R/W
	TCH9END_ODD[7:0]	7:0	H-end value of odd frame for TCON GPO9.	
09h (3013h)	REG3013	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	LG_MD_9	6	LG mode enable for TCON GPO9.	
	HEAD_PROC_EN_9	5	Head protect enable for TCON GPO9.	
	HEAD_MD_9	4	Head mode enable for TCON GPO9.	
	TCH9END_ODD[11:8]	3:0	Please see description of '3012h'.	
0Ah (3014h)	REG3014	7:0	Default : 0x00	Access : R/W
	TCHAEND_ODD[7:0]	7:0	H-end value of odd frame for TCON GPOA.	
0Ah (3015h)	REG3015	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	LG_MD_A	6	LG mode enable for TCON GPOA.	
	HEAD_PROC_EN_A	5	Head protect enable for TCON GPOA.	
	HEAD_MD_A	4	Head mode enable for TCON GPOA.	
	TCHAEND_ODD[11:8]	3:0	Please see description of '3014h'.	
0Bh (3016h)	REG3016	7:0	Default : 0x00	Access : R/W
	TC_GPO_PUA_7	7	Register set PUA value for TCON GPO7.	
	TC_GPO_PUA_6	6	Register set PUA value for TCON GPO6.	
	TC_GPO_PUA_5	5	Register set PUA value for TCON GPO5.	
	TC_GPO_PUA_4	4	Register set PUA value for TCON GPO4.	
	TC_GPO_PUA_3	3	Register set PUA value for TCON GPO3.	
	TC_GPO_PUA_2	2	Register set PUA value for TCON GPO2.	
	TC_GPO_PUA_1	1	Register set PUA value for TCON GPO1.	
	TC_GPO_PUA_0	0	Register set PUA value for TCON GPO0.	

DISP_TC Register (Bank = 30)

Index (Absolute)	Mnemonic	Bit	Description	
0Bh (3017h)	REG3017	7:0	Default : 0x00	Access : R/W
	TC_GPO_PUA_SEL	7	TCON GPO PUA select. 0: (REG_PUA & TCON) for all GPO. 1: Register setting value for each TCON GPO.	
	-	6:3	Reserved.	
	TC_GPO_PUA_A	2	Register set PUA value for TCON GPOA.	
	TC_GPO_PUA_9	1	Register set PUA value for TCON GPO9.	
	TC_GPO_PUA_8	0	Register set PUA value for TCON GPO8.	
0Ch (3018h)	REG3018	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	ONE_FRAME_TOGGLE	4	Toggle per frame.	
	GATE_DE	3	Gate data enable.	
	TCON	2	TCON enable.	
	G0AT	1	Select GPO0 for mini-LVDS mode.	
	PUA	0	Power-up Active (TCON feature only). 0: Outputs inactive. 1: Outputs active	
0Dh (301Ah)	REG301A	7:0	Default : 0x00	Access : R/W
	TC_V0ST[7:0]	7:0	Line number where GPO0 start.	
0Dh (301Bh)	REG301B	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	TC_V0ST[10:8]	2:0	Please see description of '301Ah'.	
0Eh (301Ch)	REG301C	7:0	Default : 0x00	Access : R/W
	TC_V0END[7:0]	7:0	Line number where GPO0 end.	
0Eh (301Dh)	REG301D	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	TC_V0END[10:8]	2:0	Please see description of '301Ch'.	
0Fh (301Eh)	REG301E	7:0	Default : 0x00	Access : R/W
	TC_H0ST[7:0]	7:0	Pixel number where GPO0 start.	
0Fh (301Fh)	REG301F	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	TC_H0ST[10:8]	2:0	Please see description of '301Eh'.	
10h (3020h)	REG3020	7:0	Default : 0x00	Access : R/W
	TC_H0END[7:0]	7:0	Pixel number where GPO0 end.	

DISP_TC Register (Bank = 30)

Index (Absolute)	Mnemonic	Bit	Description	
10h (3021h)	REG3021	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	TC_H0END[11:8]	3:0	Please see description of '3020h'.	
11h (3022h)	REG3022	7:0	Default : 0x00	Access : R/W
	TC_V1ST[7:0]	7:0	Line number where GPO1 start.	
11h (3023h)	REG3023	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	TC_V1ST[10:8]	2:0	Please see description of '3022h'.	
12h (3024h)	REG3024	7:0	Default : 0x00	Access : R/W
	TC_V1END[7:0]	7:0	Line number where GPO1 end.	
12h (3025h)	REG3025	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	TC_V1END[10:8]	2:0	Please see description of '3024h'.	
13h (3026h)	REG3026	7:0	Default : 0x00	Access : R/W
	TC_H1ST[7:0]	7:0	Pixel number where GPO1 start.	
13h (3027h)	REG3027	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	TC_H1ST[10:8]	2:0	Please see description of '3026h'.	
14h (3028h)	REG3028	7:0	Default : 0x00	Access : R/W
	TC_H1END[7:0]	7:0	Pixel number where GPO1 end.	
14h (3029h)	REG3029	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	TC_H1END[11:8]	3:0	Please see description of '3028h'.	
15h (302Ah)	REG302A	7:0	Default : 0x00	Access : R/W
	TC_V2ST[7:0]	7:0	Line number where GPO2 start.	
15h (302Bh)	REG302B	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	TC_V2ST[10:8]	2:0	Please see description of '302Ah'.	
16h (302Ch)	REG302C	7:0	Default : 0x00	Access : R/W
	TC_V2END[7:0]	7:0	Line number where GPO2 end.	
16h (302Dh)	REG302D	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	TC_V2END[10:8]	2:0	Please see description of '302Ch'.	

DISP_TC Register (Bank = 30)

Index (Absolute)	Mnemonic	Bit	Description	
17h (302Eh)	REG302E	7:0	Default : 0x00	Access : R/W
	TC_H2ST[7:0]	7:0	Pixel number where GPO2 start.	
17h (302Fh)	REG302F	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	TC_H2ST[10:8]	2:0	Please see description of '302Eh'.	
18h (3030h)	REG3030	7:0	Default : 0x00	Access : R/W
	TC_H2END[7:0]	7:0	Pixel number where GPO2 end.	
18h (3031h)	REG3031	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	TC_H2END[11:8]	3:0	Please see description of '3030h'.	
19h (3032h)	REG3032	7:0	Default : 0x00	Access : R/W
	TC_V3ST[7:0]	7:0	Line number where GPO3 start.	
19h (3033h)	REG3033	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	TC_V3ST[10:8]	2:0	Please see description of '3032h'.	
1Ah (3034h)	REG3034	7:0	Default : 0x00	Access : R/W
	TC_V3END[7:0]	7:0	Line number where GPO3 end.	
1Ah (3035h)	REG3035	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	TC_V3END[10:8]	2:0	Please see description of '3034h'.	
1Bh (3036h)	REG3036	7:0	Default : 0x00	Access : R/W
	TC_H3ST[7:0]	7:0	Pixel number where GPO3 start.	
1Bh (3037h)	REG3037	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	TC_H3ST[10:8]	2:0	Please see description of '3036h'.	
1Ch (3038h)	REG3038	7:0	Default : 0x00	Access : R/W
	TC_H3END[7:0]	7:0	Pixel number where GPO3 end.	
1Ch (3039h)	REG3039	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	TC_H3END[11:8]	3:0	Please see description of '3038h'.	
1Dh (303Ah)	REG303A	7:0	Default : 0x00	Access : R/W
	TC_V4ST[7:0]	7:0	Line number where GPO4 start.	
1Dh	REG303B	7:0	Default : 0x00	Access : R/W

DISP_TC Register (Bank = 30)

Index (Absolute)	Mnemonic	Bit	Description	
(303Bh)	-	7:3	Reserved.	
	TC_V4ST[10:8]	2:0	Please see description of '303Ah'.	
1Eh (303Ch)	REG303C	7:0	Default : 0x00	Access : R/W
	TC_V4END[7:0]	7:0	Line number where GPO4 end.	
1Eh (303Dh)	REG303D	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	TC_V4END[10:8]	2:0	Please see description of '303Ch'.	
1Fh (303Eh)	REG303E	7:0	Default : 0x00	Access : R/W
	TC_H4ST[7:0]	7:0	Pixel number where GPO4 start.	
1Fh (303Fh)	REG303F	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	TC_H4ST[10:8]	2:0	Please see description of '303Eh'.	
20h (3040h)	REG3040	7:0	Default : 0x00	Access : R/W
	TC_H4END[7:0]	7:0	Pixel number where GPO4 end.	
20h (3041h)	REG3041	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	TC_H4END[11:8]	3:0	Please see description of '3040h'.	
21h (3042h)	REG3042	7:0	Default : 0x00	Access : R/W
	TC_V5ST[7:0]	7:0	Line number where GPO5 start.	
21h (3043h)	REG3043	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	TC_V5ST[10:8]	2:0	Please see description of '3042h'.	
22h (3044h)	REG3044	7:0	Default : 0x00	Access : R/W
	TC_V5END[7:0]	7:0	Line number where GPO5 end.	
22h (3045h)	REG3045	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	TC_V5END[10:8]	2:0	Please see description of '3044h'.	
23h (3046h)	REG3046	7:0	Default : 0x00	Access : R/W
	TC_H5ST[7:0]	7:0	Pixel number where GPO5 start.	
23h (3047h)	REG3047	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	TC_H5ST[10:8]	2:0	Please see description of '3046h'.	
24h	REG3048	7:0	Default : 0x00	Access : R/W

DISP_TC Register (Bank = 30)

Index (Absolute)	Mnemonic	Bit	Description	
(3048h)	TC_H5END[7:0]	7:0	Pixel number where GPO5 end.	
24h (3049h)	REG3049	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	TC_H5END[11:8]	3:0	Please see description of '3048h'.	
25h (304Ah)	REG304A	7:0	Default : 0x00	Access : R/W
	TC_V6ST[7:0]	7:0	Line number where GPO6 start.	
25h (304Bh)	REG304B	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	TC_V6ST[10:8]	2:0	Please see description of '304Ah'.	
26h (304Ch)	REG304C	7:0	Default : 0x00	Access : R/W
	TC_V6END[7:0]	7:0	Line number where GPO6 end.	
26h (304Dh)	REG304D	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	TC_V6END[10:8]	2:0	Please see description of '304Ch'.	
27h (304Eh)	REG304E	7:0	Default : 0x00	Access : R/W
	TC_H6ST[7:0]	7:0	Pixel number where GPO6 start.	
27h (304Fh)	REG304F	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	TC_H6ST[10:8]	2:0	Please see description of '304Eh'.	
28h (3050h)	REG3050	7:0	Default : 0x00	Access : R/W
	TC_H6END[7:0]	7:0	Pixel number where GPO6 end.	
28h (3051h)	REG3051	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	TC_H6END[11:8]	3:0	Please see description of '3050h'.	
29h (3052h)	REG3052	7:0	Default : 0x00	Access : R/W
	TC_V7ST[7:0]	7:0	Line number where GPO7 start.	
29h (3053h)	REG3053	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	TC_V7ST[10:8]	2:0	Please see description of '3052h'.	
2Ah (3054h)	REG3054	7:0	Default : 0x00	Access : R/W
	TC_V7END[7:0]	7:0	Line number where GPO7 end.	
2Ah (3055h)	REG3055	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	

DISP_TC Register (Bank = 30)

Index (Absolute)	Mnemonic	Bit	Description	
	TC_V7END[10:8]	2:0	Please see description of '3054h'.	
2Bh (3056h)	REG3056	7:0	Default : 0x00	Access : R/W
	TC_H7ST[7:0]	7:0	Pixel number where GPO7 start.	
2Bh (3057h)	REG3057	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	TC_H7ST[10:8]	2:0	Please see description of '3056h'.	
2Ch (3058h)	REG3058	7:0	Default : 0x00	Access : R/W
	TC_H7END[7:0]	7:0	Pixel number where GPO7 end.	
2Ch (3059h)	REG3059	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	TC_H7END[11:8]	3:0	Please see description of '3058h'.	
2Dh (305Ah)	REG305A	7:0	Default : 0x00	Access : R/W
	TC_V8ST[7:0]	7:0	Line number where GPO8 start.	
2Dh (305Bh)	REG305B	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	TC_V8ST[10:8]	2:0	Please see description of '305Ah'.	
2Eh (305Ch)	REG305C	7:0	Default : 0x00	Access : R/W
	TC_V8END[7:0]	7:0	Line number where GPO8 end.	
2Eh (305Dh)	REG305D	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	TC_V8END[10:8]	2:0	Please see description of '305Ch'.	
2Fh (305Eh)	REG305E	7:0	Default : 0x00	Access : R/W
	TC_H8ST[7:0]	7:0	Pixel number where GPO8 start.	
2Fh (305Fh)	REG305F	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	TC_H8ST[10:8]	2:0	Please see description of '305Eh'.	
30h (3060h)	REG3060	7:0	Default : 0x00	Access : R/W
	TC_H8END[7:0]	7:0	Pixel number where GPO8 end.	
30h (3061h)	REG3061	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	TC_H8END[11:8]	3:0	Please see description of '3060h'.	
31h (3062h)	REG3062	7:0	Default : 0x00	Access : R/W
	TC_V9ST[7:0]	7:0	Line number where GPO9 start.	

DISP_TC Register (Bank = 30)

Index (Absolute)	Mnemonic	Bit	Description	
31h (3063h)	REG3063	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	TC_V9ST[10:8]	2:0	Please see description of '3062h'.	
32h (3064h)	REG3064	7:0	Default : 0x00	Access : R/W
	TC_V9END[7:0]	7:0	Line number where GPO9 end.	
32h (3065h)	REG3065	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	TC_V9END[10:8]	2:0	Please see description of '3064h'.	
33h (3066h)	REG3066	7:0	Default : 0x00	Access : R/W
	TC_H9ST[7:0]	7:0	Pixel number where GPO9 start.	
33h (3067h)	REG3067	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	TC_H9ST[10:8]	2:0	Please see description of '3066h'.	
34h (3068h)	REG3068	7:0	Default : 0x00	Access : R/W
	TC_H9END[7:0]	7:0	Pixel number where GPO9 end.	
34h (3069h)	REG3069	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	TC_H9END[11:8]	3:0	Please see description of '3068h'.	
35h (306Ah)	REG306A	7:0	Default : 0x00	Access : R/W
	TC_VAST[7:0]	7:0	Line number where GPOA start.	
35h (306Bh)	REG306B	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	TC_VAST[10:8]	2:0	Please see description of '306Ah'.	
36h (306Ch)	REG306C	7:0	Default : 0x00	Access : R/W
	TC_VAEND[7:0]	7:0	Line number where GPOA end.	
36h (306Dh)	REG306D	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	TC_VAEND[10:8]	2:0	Please see description of '306Ch'.	
37h (306Eh)	REG306E	7:0	Default : 0x00	Access : R/W
	TC_HAST[7:0]	7:0	Pixel number where GPOA start.	
37h (306Fh)	REG306F	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	TC_HAST[10:8]	2:0	Please see description of '306Eh'.	

DISP_TC Register (Bank = 30)

Index (Absolute)	Mnemonic	Bit	Description	
38h (3070h)	REG3070	7:0	Default : 0x00	Access : R/W
	TC_HAEND[7:0]	7:0	Pixel number where GPOA end.	
38h (3071h)	REG3071	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	TC_HAEND[11:8]	3:0	Please see description of '3070h'.	
39h (3072h)	REG3072	7:0	Default : 0x00	Access : R/W
	G0OP	7	Output polarity for GPO0.	
	G0TC	6	Toggle circuit for GPO0.	
	G0ES	5	Early start function for GPO0.	
	G0TS[1:0]	4:3	Type select for GPO0.	
	G0CS[2:0]	2:0	Combination select for GPO0.	
39h (3073h)	REG3073	7:0	Default : 0x00	Access : R/W
	G1OP	7	Output polarity for GPO1.	
	G1TC	6	Toggle circuit for GPO1.	
	G1ES	5	Early start function for GPO1.	
	G1TS[1:0]	4:3	Type select for GPO1.	
	G1CS[2:0]	2:0	Combination select for GPO1.	
3Ah (3074h)	REG3074	7:0	Default : 0x00	Access : R/W
	G2OP	7	Output polarity for GPO2.	
	G2TC	6	Toggle circuit for GPO2.	
	G2ES	5	Early start function for GPO2.	
	G2TS[1:0]	4:3	Type select for GPO2.	
	G2CS[2:0]	2:0	Combination select for GPO2.	
3Ah (3075h)	REG3075	7:0	Default : 0x00	Access : R/W
	G3OP	7	Output polarity for GPO3.	
	G3TC	6	Toggle circuit for GPO3.	
	G3ES	5	Early start function for GPO3.	
	G3TS[1:0]	4:3	Type select for GPO3.	
	G3CS[2:0]	2:0	Combination select for GPO3.	
3Bh (3076h)	REG3076	7:0	Default : 0x00	Access : R/W
	G4OP	7	Output polarity for GPO4.	
	G4TC	6	Toggle circuit for GPO4.	
	G4ES	5	Early start function for GPO4.	

DISP_TC Register (Bank = 30)

Index (Absolute)	Mnemonic	Bit	Description	
	G4TS[1:0]	4:3	Type select for GPO4.	
	G4CS[2:0]	2:0	Combination select for GPO4.	
3Bh (3077h)	REG3077	7:0	Default : 0x00	Access : R/W
	G5OP	7	Output polarity for GPO5.	
	G5TC	6	Toggle circuit for GPO5.	
	G5ES	5	Early start function for GPO5.	
	G5TS[1:0]	4:3	Type select for GPO5.	
	G5CS[2:0]	2:0	Combination select for GPO5.	
3Ch (3078h)	REG3078	7:0	Default : 0x00	Access : R/W
	G6OP	7	Output polarity for GPO6.	
	G6TC	6	Toggle circuit for GPO6.	
	G6ES	5	Early start function for GPO6.	
	G6TS[1:0]	4:3	Type select for GPO6.	
	G6CS[2:0]	2:0	Combination select for GPO6.	
3Ch (3079h)	REG3079	7:0	Default : 0x00	Access : R/W
	G7OP	7	Output polarity for GPO7.	
	G7TC	6	Toggle circuit for GPO7.	
	G7ES	5	Early start function for GPO7.	
	G7TS[1:0]	4:3	Type select for GPO7.	
	G7CS[2:0]	2:0	Combination select for GPO7.	
3Dh (307Ah)	REG307A	7:0	Default : 0x00	Access : R/W
	G8OP	7	Output polarity for GPO8.	
	G8TC	6	Toggle circuit for GPO8.	
	G8ES	5	Early start function for GPO8.	
	G8TS[1:0]	4:3	Type select for GPO8.	
	G8CS[2:0]	2:0	Combination select for GPO8.	
3Dh (307Bh)	REG307B	7:0	Default : 0x00	Access : R/W
	G9OP	7	Output polarity for GPO9.	
	G9TC	6	Toggle circuit for GPO9.	
	G9ES	5	Early start function for GPO9.	
	G9TS[1:0]	4:3	Type select for GPO9.	
	G9CS[2:0]	2:0	Combination select for GPO9.	
3Eh	REG307C	7:0	Default : 0x00	Access : R/W

DISP_TC Register (Bank = 30)

Index (Absolute)	Mnemonic	Bit	Description	
(307Ch)	GAOP	7	Output polarity for GPOA.	
	GATC	6	Toggle circuit for GPOA.	
	GAES	5	Early start function for GPOA.	
	GATS[1:0]	4:3	Type select for GPOA.	
	GACS[2:0]	2:0	Combination select for GPOA.	
3Eh (307Dh)	REG307D	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	MINIGPO_SEL[3:0]	6:3	GPO select for mini-LVDS.	
	MINITP1_PIPE[2:0]	2:0	Pipe for minitp1.	
3Fh (307Eh)	REG307E	7:0	Default : 0x00	Access : R/W
	GPO5_EN	7	GPO5 output enable.	
	GPO4_EN	6	GPO4 output enable.	
	GPO3_EN	5	GPO3 output enable.	
	GPO2_EN	4	GPO2 output enable.	
	GPO1_EN	3	GPO1 output enable.	
	GPO0_EN	2	GPO0 output enable.	
	GPOA_N_1_SEL	1	GPOA_N_1 signal select 0: Set GPOA_N_1 to 0. 1: Select GPO9 as GPOA_N_1.	
	TG_SEL	0	Select new TG_VSYNC for TCON GPO_7,GPO_9, and GPO_A.	
3Fh (307Fh)	REG307F	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	GPOA_EN	4	GPOA output enable.	
	GPO9_EN	3	GPO9 output enable.	
	GPO8_EN	2	GPO8 output enable.	
	GPO7_EN	1	GPO7 output enable.	
	GPO6_EN	0	GPO6 output enable.	
40h (3080h)	REG3080	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	EARLY_END	6	TCON GPO early end function enable.	
	-	5:0	Reserved.	
42h (3084h)	REG3084	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	

DISP_TC Register (Bank = 30)

Index (Absolute)	Mnemonic	Bit	Description	
	OE_POL	2	Select GPO4 output polarity. 0: Normal. 1: Invert.	
	-	1:0	Reserved.	
42h (3085h)	REG3085	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	SEL_FIELD	4	VOP output field select. 0: Vop2 output field. 1: FBL mode output field.	
	SYNC_FIELD	3	TG_VSYNC signal select for GPO9. 0: Sync with VSYNC signal. 1: Sync with VOP output field.	
	INTERLACE_VTOT	2	Interlace output mode. 0: Non-interlace output. 1: Interlace output.	
	-	1:0	Reserved.	
43h (3086h)	REG3086	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	DLY_FRAME[2:0]	2:0	GPO4 power active up delay frame number.	
43h (3087h)	REG3087	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	GATE_HS	4	HSYNC gate enable.	
	-	3	Reserved.	
	POLB	2	OPOL/EPOL signal select. 0: OPOL = GPO0_FF & PUA_0. EPOL = GPO0_FF & PUA_1 1: OPOL = GPO0_FF & GPOA_FF & PUA_0. EPOL = GPO0_FF & GPOA_FF & PUA_1	
	-	1:0	Reserved.	
47h (308Fh)	REG308F	7:0	Default : 0x33	Access : R/W
	-	7:6	Reserved.	
	SEQ_MD	5	TCON SEQ_MD output value 0: Simultaneous mode. 1: SEQ mode.	
	TCCLK_MOD	4	TCCLK source select 0: 3 phase clk.	

DISP_TC Register (Bank = 30)

Index (Absolute)	Mnemonic	Bit	Description	
			1: Register set value.	
	-	3:2	Reserved.	
	L_R	1	TCON L_R output value.	
	U_D	0	TCON U_D output value.	
48h (3090h)	**REG3090**	**7:0**	**Default : 0x80**	**Access : R/W**
	TCCLK23_SETHL	7	Tcclk2, tcclk33 register set value, this register is valid with REG_TCCLK_MOD is high.	
	-	6:0	Reserved.	
58h (30B1h)	**REG30B1**	**7:0**	**Default : 0x00**	**Access : R/W**
	IDCLK_GAT	7	IDCLK gate enable.	
	BYPASSMD	6	ODCLK generator force to mode 0 (bypass) enable.	
	ADC_TESTMD	5	ODCLK generator force to mode 0 (bypass) enable.	
	DSUB_TESTMD	4	ODCLK generator force to mode 0 (bypass) enable.	
	BP	3	ODCLK generator force to mode 0 (bypass) enable.	
	TESTCLK_MD	2	ODCLK generator force to mode 2 (normal) enable.	
	EOCK	1	ODCLK generator force to mode 3 (DFT) enable.	
	TESTFUNC	0	ODCLK generator force to mode 3 (DFT) enable.	
59h (30B2h)	**REG30B2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	ODCLK_DIV3	0	ODCLK divide 3 mode enable.	
60h (30C0h)	**REG30C0**	**7:0**	**Default : 0x00**	**Access : R/W**
	LG_REG24[7:0]	7:0	Frame number to generate PVDD_ODD.	
60h (30C1h)	**REG30C1**	**7:0**	**Default : 0x00**	**Access : R/W**
	LG_REG25[7:0]	7:0	Pixel number to sample PVDD_ODD to PVDD_EVEN.	
61h (30C2h)	**REG30C2**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPO7_FF_OEN	7	GPO7_FF output enable.	
	GPO6_FF_OEN	6	GPO6_FF output enable.	
	GPO5_FF_OEN	5	GPO5_FF output enable.	
	GPO4_FF_OEN	4	GPO4_FF output enable.	
	GPO3_FF_OEN	3	GPO3_FF output enable.	
	GPO2_FF_OEN	2	GPO2_FF output enable.	
	GPO1_FF_OEN	1	GPO1_FF output enable.	
	GPO0_FF_OEN	0	GPO0_FF output enable.	

DISP_TC Register (Bank = 30)

Index (Absolute)	Mnemonic	Bit	Description	
61h (30C3h)	REG30C3	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	GPOA_FF_OEN	2	GPOA_FF output enable.	
	GPO9_FF_OEN	1	GPO9_FF output enable.	
	GPO8_FF_OEN	0	GPO8_FF output enable.	

LPLL Register (Bank = 31)

LPLL Register (Bank = 31)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
00h (3100h)	REG3100	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.
	LPLL_INPUT_DIV_FIRST[1:0]	1:0	Input divider ratio control. 00: /1. 01: /2. 10: /4. 11: /8.
00h (3101h)	REG3101	7:0	Default : 0x00	Access : R/W
	LPLL_INPUT_DIV_SECOND[7:0]	7:0	Input divider ratio control: divide ratio = (1/N). 0: Divide 1. 1: Divide 1. 2: Divide 2. 3: Divide 3. 4: Divide 4...
01h (3102h)	REG3102	7:0	Default : 0x03	Access : R/W
	-	7:2	Reserved.
	LPLL_LOOP_DIV_FIRST[1:0]	1:0	Loop divider ration control.
01h (3103h)	REG3103	7:0	Default : 0x01	Access : R/W
	LPLL_LOOP_DIV_SECOND[7:0]	7:0	Loop divider ratio control: divide ratio = (1/N); Default ratio = 8. 0: Divide 1. 1: Divide 1. 2: Divide 2. 3: Divide 3. 4: Divide 4...
02h (3104h)	REG3104	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.
	LPLL_EN_DCCM	2	Enable duty cycle correction for divider M, high active.
	LPLL_EN_DCCN	1	Enable duty cycle correction for divider N, high active.
	LPLL_EN_MINILVDS	0	Enable mini-LVDS control, high active.
02h (3105h)	REG3105	7:0	Default : 0x22	Access : R/W
	LPLL_DIVM_S[3:0]	7:4	Divider M ratio control 0010: Div1. 0011: Div1p5. 0100: Div2.

LPLL Register (Bank = 31)			

Index (Absolute)	Mnemonic	Bit	Description
			0101: Div2p5. 0110: Div3. 0111: Div3p5. 1000: Div4. 1001: Div4p5. 1010: Div5. 1100: Div6. Others: Power down.
	LPLL_DIVN_S[3:0]	3:0	Divider N ratio control 0010: Div1. 0011: Div1p5. 0100: Div2. 0101: Div2p5. 0110: Div3. 0111: Div3p5. 1000: Div4. 1001: Div4p5. 1010: Div5. 1100: Div6. Others: Power down.
03h (3106h)	**REG3106**	7:0	**Default : 0x23**	**Access : R/W**
	LPLL_MODE	7	LPLL mode. 0: Single mode. 1: Dual mode.
	LPLL_TYPE	6	LPLL type. 0: LVDS mode. 1: RSDS mode.
	LPLL_PD	5	Power down control to PLL; active high.
	LPLL_RESET	4	Reset digital circuit in LPLL.
	LPLL_VCO_OFFSET	3	Enable VCO free running; active low.
	LPLL_ICTRL[2:0]	2:0	Charge-pump current control.
03h (3107h)	**REG3107**	7:0	**Default : 0x00**	**Access : R/W**
	LPLL_TEST[7:0]	7:0	Test mode configuration.
04h (3108h)	**REG3108**	7:0	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.
	HIGH_FLAG	1	Output flag for VCO supply voltage too high (need monitor for mass production).

LPLL Register (Bank = 31)

Index (Absolute)	Mnemonic	Bit	Description	
	LOCK	0	PLL lock flag.	
04h (3109h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
05h (310Ah)	REG310A	7:0	Default : 0x00	Access : R/W
	RK_HOLD_GAIN[7:0]	7:0	RK gain holds line number.	
05h (310Bh)	REG310B	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	RK_HOLD_GAIN[11:8]	3:0	Please see description of '310Ah'.	
06h (310Ch)	REG310C	7:0	Default : 0x00	Access : R/W
	LIMIT_D5D6D7[7:0]	7:0	Limit for clock freq. correction modification.	
06h (310Dh)	REG310D	7:0	Default : 0x00	Access : R/W
	LIMIT_D5D6D7[15:8]	7:0	Please see description of '310Ch'.	
07h (310Eh)	REG310E	7:0	Default : 0x00	Access : R/W
	LIMIT_D5D6D7[23:16]	7:0	Please see description of '310Ch'.	
08h (3110h)	REG3110	7:0	Default : 0x00	Access : R/W
	LIMIT_D5D6D7_RK[7:0]	7:0	Limit for phase correction modification.	
08h (3111h)	REG3111	7:0	Default : 0x00	Access : R/W
	LIMIT_D5D6D7_RK[15:8]	7:0	Please see description of '3110h'.	
09h (3112h)	REG3112	7:0	Default : 0x00	Access : R/W
	LIMIT_D5D6D7_RK[23:16]	7:0	Please see description of '3110h'.	
0Ah (3114h)	REG3114	7:0	Default : 0x00	Access : R/W
	LIMIT_LPLL_OFFSET[7:0]	7:0	Limit for LPLL phase offset.	
0Ah (3115h)	REG3115	7:0	Default : 0x00	Access : R/W
	LIMIT_LPLL_OFFSET[15:8]	7:0	Please see description of '3114h'.	
0Bh (3116h)	REG3116	7:0	Default : 0x10	Access : R/W
	FRAME_TUN_FRAM_NO[7:0]	7:0	Frame tune number setting.	
0Bh (3117h)	REG3117	7:0	Default : 0x05	Access : R/W
	CTUNE_COEF_RK[3:0]	7:4	Coarse TUNE_COEF (for phase).	
	CTUNE_COEF[3:0]	3:0	Coarse TUNE_COEF (for frequency).	
0Ch (3118h)	REG3118	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	FRAME_LPLL_EN	3	Frame LPLL enable. 0: Disable.	

LPLL Register (Bank = 31)

Index (Absolute)	Mnemonic	Bit	Description	
			1: Enable.	
	-	2:1	Reserved.	
	FRAME_LPLL_FBL_EN	0	Frame LPLL FBL enable. 0: Disable. 1: Enable.	
0Dh (311Ah)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
0Dh (311Bh)	REG311B	7:0	Default : 0xB3	Access : R/W
	-	7:4	Reserved.	
	SSC_EN	3	SSC enable. 0: Disable. 1: Enable.	
	-	2:0	Reserved.	
0Fh (311Eh)	REG311E	7:0	Default : 0x44	Access : R/W
	LPLL_SET[7:0]	7:0	PLL initial setting value.	
0Fh (311Fh)	REG311F	7:0	Default : 0x55	Access : R/W
	LPLL_SET[15:8]	7:0	Please see description of '311Eh'.	
10h (3120h)	REG3120	7:0	Default : 0x22	Access : R/W
	LPLL_SET[23:16]	7:0	Please see description of '311Eh'.	
11h (3122h)	REG3122	7:0	Default : 0x00	Access : RO
	LPLL_UP_OFS[7:0]	7:0	LPLL log phase offset.	
11h (3123h)	REG3123	7:0	Default : 0x00	Access : RO
	LPLL_UP_OFS[15:8]	7:0	Please see description of '3122h'.	
12h (3124h)	REG3124	7:0	Default : 0x00	Access : RO
	-	7:4	Reserved.	
	LPLL_UP_OFS[19:16]	3:0	Please see description of '3122h'.	
13h (3126h)	REG3126	7:0	Default : 0x00	Access : RO
	LPLL_DN_OFF[7:0]	7:0	LPLL leading phase offset.	
13h (3127h)	REG3127	7:0	Default : 0x00	Access : RO
	LPLL_DN_OFF[15:8]	7:0	Please see description of '3126h'.	
14h (3128h)	REG3128	7:0	Default : 0x00	Access : RO
	-	7:4	Reserved.	
	LPLL_DN_OFF[19:16]	3:0	Please see description of '3126h'.	
16h	-	7:0	Default : -	Access : -

LPLL Register (Bank = 31)

Index (Absolute)	Mnemonic	Bit	Description	
(312Ch ~ 312Dh)	-	7:0	Reserved.	
17h (312Eh)	REG312E	7:0	Default : 0x20	Access : R/W
	LPLL_STEP[7:0]	7:0	Output PLL spread spectrum step.	
17h (312Fh)	REG312F	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	LPLL_STEP[9:8]	1:0	Please see description of '312Eh'.	
18h (3130h)	REG3130	7:0	Default : 0x00	Access : R/W
	LPLL_SPAN[7:0]	7:0	Output PLL spread spectrum span.	
18h (3131h)	REG3131	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	LPLL_SPAN[13:8]	5:0	Please see description of '3130h'.	
19h (3132h ~ 3133h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
1Ah (3134h)	REG3134	7:0	Default : 0x00	Access : R/W
	ADD_LINE_SEL	7	Add one line enable.	
	-	6:0	Reserved.	
1Ah (3135h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
1Bh (3136h)	REG3136	7:0	Default : 0x00	Access : R/W
	PWMDIV[7:0]	7:0	PWM divider.	
1Bh (3137h)	REG3137	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	PWMDIV[8]	0	Please see description of '3136h'.	
1Ch (3138h)	REG3138	7:0	Default : 0x00	Access : R/W
	LOCK_THRD_VA[7:0]	7:0	Lock threshold value.	
1Ch (3139h)	REG3139	7:0	Default : 0x00	Access : R/W
	REG_FAST_FPLL_EN	7	Fast FPLL enable. 0: Disable. 1: Enable.	
	-	6:2	Reserved.	
	LOCK_THRESH_VA[9:8]	1:0	Please see description of '3138h'.	
1Dh	REG313A	7:0	Default : 0x00	Access : R/W

LPLL Register (Bank = 31)

Index (Absolute)	Mnemonic	Bit	Description	
(313Ah)	FTUNE_COEF_RK[3:0]	7:4	Fine tune COEF_RK.	
	FTUNE_COEF_C[3:0]	3:0	Fine tune COEF_C.	
1Eh (313Ch)	REG313C	7:0	Default : 0x00	Access : R/W
	BIUCLK_DIV[3:0]	7:4	Reference clock for frame PLL counter divider.	
	-	3:2	Reserved.	
	VCNT_REST_PULSE	1	Select VCNT_REST as pulse or level signal.	
	SEL_VMDE_START	0	Select start or end pulse of VMDE as output reference.	
21h (3142h)	REG3142	7:0	Default : 0x00	Access : RO
	IVS_PRD[7:0]	7:0	IVS reference signal period.	
21h (3143h)	REG3143	7:0	Default : 0x00	Access : RO
	IVS_PRD[15:8]	7:0	Please see description of '3142h'.	
22h (3144h)	REG3144	7:0	Default : 0x00	Access : RO
	-	7:4	Reserved.	
	IVS_PRD[19:16]	3:0	Please see description of '3142h'.	
23h (3146h)	REG3146	7:0	Default : 0x00	Access : RO
	OVDE_PRD[7:0]	7:0	OVDE reference signal period.	
23h (3147h)	REG3147	7:0	Default : 0x00	Access : RO
	OVDE_PRD[15:8]	7:0	Please see description of '3146h'.	
24h (3148h)	REG3148	7:0	Default : 0x00	Access : RO
	-	7:4	Reserved.	
	OVDE_PRD[19:16]	3:0	Please see description of '3146h'.	
25h (314Ah)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
26h (314Ch)	REG314C	7:0	Default : 0x00	Access : RO
	LPLL_SET_MUX[7:0]	7:0	LPLL_SET value used for DISP_LPLL.	
26h (314Dh)	REG314D	7:0	Default : 0x00	Access : RO
	LPLL_SET_MUX[15:8]	7:0	Please see description of '314Ch'.	
27h (314Eh)	REG314E	7:0	Default : 0x00	Access : RO
	LPLL_SET_MUX[23:16]	7:0	Please see description of '314Ch'.	

DISP MISC Register (Bank = 32)

DISP_MISC Register (Bank = 32)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (3200h)	REG3200	7:0	Default : 0x00	Access : R/W
	EN_CVBS_DAC	7	CVBS DAC enable.	
	ED0	6	ED0 signal.	
	ED1	5	ED1 signal.	
	EN	4	Bandgap bias enable.	
	ENB	3	B DAC enable.	
	ENG	2	G DAC enable.	
	ENR	1	R DAC enable.	
	ENX	0	SVM DAC enable.	
00h (3201h)	REG3201	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	DAGAIN[4:0]	5:1	Gain control for all DACs.	
	BGT	0	BGT signal.	
01h (3202h)	REG3202	7:0	Default : 0x00	Access : R/W
	SVM_CLK_DLY[3:0]	7:4	Delay setting of SVM clock.	
	-	3:1	Reserved.	
	SVM_CLK_INV	0	Invert SVM clock.	
01h (3203h)	REG3203	7:0	Default : 0x00	Access : R/W
	DAT_CLK_DLY[3:0]	7:4	Delay setting of DAT clock.	
	-	3:1	Reserved.	
	DAT_CLK_INV	0	Invert DAT clock.	
02h (3204h)	REG3204	7:0	Default : 0x00	Access : R/W
	SVM_HALF_STEL	7	SVM half step.	
	CLK_INVERT	6	Invert SVM clock.	
	DAC_RAMP_MD[1:0]	5:4	Ramp mode of DAC pattern gen. 00: Force DAC to minimum value (10 & apos; b0). 01: Force DAC to maximum value (10 & apos; h3ff). 1x : Output ramp pattern to DAC (pat = pat + 1)	
	DAC_TEST_SEL[1:0]	3:2	Test input select of DAC. 00: ADCDVIPLL test bus. 01: External test vector from pads. 10: VD test bus. 11: Internal BIST pattern.	

DISP_MISC Register (Bank = 32)

Index (Absolute)	Mnemonic	Bit	Description	
	DAC_OUT_SEL[1:0]	1:0	Source of DAC output. 00: CRT output. 01: VE output.	
03h (3206h ~ 3207h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
04h (3208h)	REG3208	7:0	Default : 0x00	Access : R/W
	BVCOM_DC[7:0]	7:0	DC of BVCOM.	
04h (3209h)	REG3209	7:0	Default : 0x00	Access : R/W
	TST_IVCOM[3:0]	7:4	Test I VCOM.	
	-	3	Reserved.	
	TST_VCOMBGO	2	Test VCOM B/G output.	
	PWDN_VCOM	1	Power down for VCOM.	
	BVCOM_DC[8]	0	Please see description of '3208h'.	
05h (320Ah)	REG320A	7:0	Default : 0x00	Access : R/W
	BVCOM_OUT[7:0]	7:0	BVCOM output.	
10h (3220h)	REG3220	7:0	Default : 0x00	Access : R/W
	HD_OFFSET_EN	7	HD offset enable.	
	PBPR_SYNC_EN	6	PbPr sync. enable.	
	PHASE3_EN	5	3: Phase enable.	
	HD_EN	4	HDTV signal enable. 0: Disable. 1: Enable.	
	P3_INIT_V1	3	Initial value of set1 of 3 phases.	
	P3_INIT_V0	2	Initial value of set0 of 3 phases.	
	INIT_V1	1	Initial value of set1.	
	INIT_V0	0	Initial value of set0.	
10h (3221h)	REG3221	7:0	Default : 0x00	Access : R/W
	TP_EN1[3:0]	7:4	Transition point enable set 1.	
	TP_EN0[3:0]	3:0	Transition point enable set 0.	
11h (3222h)	REG3222	7:0	Default : 0x00	Access : R/W
	FIELD_INV_HD	7	HD field inverse.	
	-	6:4	Reserved.	
	P3_TP_EN1[1:0]	3:2	Transition point enable set 1 of 3 phases.	

DISP_MISC Register (Bank = 32)

Index (Absolute)	Mnemonic	Bit	Description	
	P3_TP_EN0[1:0]	1:0	Transition point enable set 0 of 3 phases.	
11h (3223h)	REG3223	7:0	Default : 0x3F	Access : R/W
	HSYNC_PWIDTH[7:0]	7:0	HSYNC pulse width number; unit: ODCLK.	
12h (3224h)	REG3224	7:0	Default : 0xC0	Access : R/W
	SET_WAVE0[7:0]	7:0	Set wave of set0 by half line cycle[23:0].	
12h (3225h)	REG3225	7:0	Default : 0x0F	Access : R/W
	SET_WAVE0[15:8]	7:0	Please see description of '3224h'.	
13h (3226h)	REG3226	7:0	Default : 0x00	Access : R/W
	SET_WAVE0[23:16]	7:0	Please see description of '3224h'.	
13h (3227h)	REG3227	7:0	Default : 0x80	Access : R/W
	SET_WAVE1_B0[7:0]	7:0	Set wave of set1 by half line cycle[7:0].	
14h (3228h)	REG3228	7:0	Default : 0x80	Access : R/W
	SET_WAVE1_B2B1[7:0]	7:0	Set wave of set1 by half line cycle[23:8].	
14h (3229h)	REG3229	7:0	Default : 0x1F	Access : R/W
	SET_WAVE1_B2B1[15:8]	7:0	Please see description of '3228h'.	
15h (322Ah)	REG322A	7:0	Default : 0x08	Access : R/W
	CSYN_LENGTH0[7:0]	7:0	C sync. length of set0.	
15h (322Bh)	REG322B	7:0	Default : 0x08	Access : R/W
	CSYN_LENGTH1[7:0]	7:0	C sync. Length of set1.	
16h (322Ch)	REG322C	7:0	Default : 0x00	Access : R/W
	CS_ST0[7:0]	7:0	C sync. Start line of set0.	
16h (322Dh)	REG322D	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	CS_ST0[10:8]	2:0	Please see description of '322Ch'.	
17h (322Eh)	REG322E	7:0	Default : 0x01	Access : R/W
	CS_ST1[7:0]	7:0	C sync. Start line of set1.	
17h (322Fh)	REG322F	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	CS_ST1[10:8]	2:0	Please see description of '322Eh'.	
18h (3230h)	REG3230	7:0	Default : 0x20	Access : R/W
	TP00[7:0]	7:0	Transition point0 of set0.	
18h (3231h)	REG3231	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	

DISP_MISC Register (Bank = 32)

Index (Absolute)	Mnemonic	Bit	Description	
	TP00[9:8]	1:0	Please see description of '3230h'.	
19h (3232h)	REG3232	7:0	Default : 0xFF	Access : R/W
	TP01[7:0]	7:0	Transition point1 of set0.	
19h (3233h)	REG3233	7:0	Default : 0x03	Access : R/W
	-	7:2	Reserved.	
	TP01[9:8]	1:0	Please see description of '3232h'.	
1Ah (3234h)	REG3234	7:0	Default : 0xFF	Access : R/W
	TP02[7:0]	7:0	Transition point2 of set0.	
1Ah (3235h)	REG3235	7:0	Default : 0x03	Access : R/W
	-	7:2	Reserved.	
	TP02[9:8]	1:0	Please see description of '3234h'.	
1Bh (3236h)	REG3236	7:0	Default : 0xFF	Access : R/W
	TP03[7:0]	7:0	Transition point3 of set0.	
1Bh (3237h)	REG3237	7:0	Default : 0x03	Access : R/W
	-	7:2	Reserved.	
	TP03[9:8]	1:0	Please see description of '3236h'.	
1Ch (3238h)	REG3238	7:0	Default : 0x6E	Access : R/W
	TP10[7:0]	7:0	Transition point0 of set1.	
1Ch (3239h)	REG3239	7:0	Default : 0x01	Access : R/W
	-	7:2	Reserved.	
	TP10[9:8]	1:0	Please see description of '3238h'.	
1Dh (323Ah)	REG323A	7:0	Default : 0xFF	Access : R/W
	TP11[7:0]	7:0	Transition point1 of set1.	
1Dh (323Bh)	REG323B	7:0	Default : 0x03	Access : R/W
	-	7:2	Reserved.	
	TP11[9:8]	1:0	Please see description of '323Ah'.	
1Eh (323Ch)	REG323C	7:0	Default : 0xFF	Access : R/W
	TP12[7:0]	7:0	Transition point2 of set1.	
1Eh (323Dh)	REG323D	7:0	Default : 0x03	Access : R/W
	-	7:2	Reserved.	
	TP12[9:8]	1:0	Please see description of '323Ch'.	
1Fh (323Eh)	REG323E	7:0	Default : 0xFF	Access : R/W
	TP13[7:0]	7:0	Transition point3 of set1.	

DISP_MISC Register (Bank = 32)

Index (Absolute)	Mnemonic	Bit	Description	
1Fh (323Fh)	REG323F	7:0	Default : 0x03	Access : R/W
	-	7:2	Reserved.	
	TP13[9:8]	1:0	Please see description of '323Eh'.	
20h (3240h)	REG3240	7:0	Default : 0x2C	Access : R/W
	P3_TP00[7:0]	7:0	Transition point0 of set0 of 3 phases.	
20h (3241h)	REG3241	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	P3_TP00[9:8]	1:0	Please see description of '3240h'.	
21h (3242h)	REG3242	7:0	Default : 0x58	Access : R/W
	P3_TP01[7:0]	7:0	Transition point1 of set0 of 3 phases.	
21h (3243h)	REG3243	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	P3_TP01[9:8]	1:0	Please see description of '3242h'.	
22h (3244h)	REG3244	7:0	Default : 0x2C	Access : R/W
	P3_TP10[7:0]	7:0	Transition point0 of set1 of 3 phases.	
22h (3245h)	REG3245	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	P3_TP10[9:8]	1:0	Please see description of '3244h'.	
23h (3246h)	REG3246	7:0	Default : 0x58	Access : R/W
	P3_TP11[7:0]	7:0	Transition point1 of set1 of 3 phases.	
23h (3247h)	REG3247	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	P3_TP11[9:8]	1:0	Please see description of '3246h'.	
24h (3248h)	REG3248	7:0	Default : 0x14	Access : R/W
	Y_BOT[7:0]	7:0	HDTV signal Y's bottom value.	
24h (3249h)	REG3249	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	Y_BOT[9:8]	1:0	Please see description of '3248h'.	
25h (324Ah)	REG324A	7:0	Default : 0x41	Access : R/W
	Y_BLK[7:0]	7:0	HDTV signal Y's blanking value.	
25h (324Bh)	REG324B	7:0	Default : 0x01	Access : R/W
	-	7:2	Reserved.	
	Y_BLK[9:8]	1:0	Please see description of '324Ah'.	

DISP_MISC Register (Bank = 32)

Index (Absolute)	Mnemonic	Bit	Description	
26h (324Ch)	REG324C	7:0	Default : 0x6F	Access : R/W
	Y_PHASE3_VAL[7:0]	7:0	HDTV signal Y's phase3 value.	
26h (324Dh)	REG324D	7:0	Default : 0x02	Access : R/W
	-	7:2	Reserved.	
	Y_PHASE3_VAL[9:8]	1:0	Please see description of '324Ch'.	
27h (324Eh)	REG324E	7:0	Default : 0x67	Access : R/W
	PBPR_BOT[7:0]	7:0	HDTV signal PbPr's bottom value.	
27h (324Fh)	REG324F	7:0	Default : 0x01	Access : R/W
	-	7:2	Reserved.	
	PBPR_BOT[9:8]	1:0	Please see description of '324Eh'.	
28h (3250h)	REG3250	7:0	Default : 0x9A	Access : R/W
	PBPR_BLK[7:0]	7:0	HDTV signal PbPr's blanking value.	
28h (3251h)	REG3251	7:0	Default : 0x02	Access : R/W
	-	7:2	Reserved.	
	PBPR_BLK[9:8]	1:0	Please see description of '3250h'.	
29h (3252h)	REG3252	7:0	Default : 0xCD	Access : R/W
	PBPR_PHASE3_VAL[7:0]	7:0	HDTV signal PbPr's phase3 value.	
29h (3253h)	REG3253	7:0	Default : 0x03	Access : R/W
	-	7:2	Reserved.	
	PBPR_PHASE3_VAL[9:8]	1:0	Please see description of '3252h'.	
2Ah (3254h)	REG3254	7:0	Default : 0x41	Access : R/W
	Y_OFFSET[7:0]	7:0	HDTV signal Y's offset value.	
2Ah (3255h)	REG3255	7:0	Default : 0x01	Access : R/W
	-	7:2	Reserved.	
	Y_OFFSET[9:8]	1:0	Please see description of '3254h'.	
2Bh (3256h)	REG3256	7:0	Default : 0x35	Access : R/W
	PBPR_OFFSET[7:0]	7:0	HDTV signal PbPr's offset value.	
2Bh (3257h)	REG3257	7:0	Default : 0x01	Access : R/W
	-	7:2	Reserved.	
	PBPR_OFFSET[9:8]	1:0	Please see description of '3256h'.	
2Ch ~ 3Fh (3257h ~ 327Fh)	-	7:0	Default : -	Access : -
	-	7:2	Reserved.	

DISP_MISC Register (Bank = 32)

Index (Absolute)	Mnemonic	Bit	Description	
40h (3280h)	REG3280	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	CH_SWAP	6	Channel swap.	
	CH_POLARITY	5	Channel polarity.	
	LVDS_PLASMA	4	Set LVDS or plasma.	
	PDP_10BIT	3	PDP output 10-bit.	
	LVDS_TI	2	LVDS TI mode select.	
	RSCLK_TESTMD	1	LVDS output clock test mode.	
	CLKB	0	GPOA gate clock enable. 0: Disable. 1: Enable.	
40h (3281h)	REG3281	7:0	Default : 0x00	Access : R/W
	ECLKDLYSEL[3:0]	7:4	TTL output de-delay select.	
	CLKDLYSEL[3:0]	3:0	TTL output clock delay select.	
41h (3282h)	REG3282	7:0	Default : 0x00	Access : R/W
	TESTER_PIX[7:0]	7:0	LVDS data output test value.	
41h (3283h)	REG3283	7:0	Default : 0x00	Access : R/W
	PDP_MSK_EN	7	PDP mask enable.	
	PDP_MSK_SET	6	PDP mask set.	
	PDP_CH3_EN	5	PDP channel 3 enable.	
	PDP_CH3_SET	4	PDP channel 3 set.	
	PDP_CH4_EN	3	PDP channel 4 enable.	
	PDP_CH4_SET	2	PDP channel 4 set.	
	SKEW[1:0]	1:0	Clock skew select.	
42h (3284h)	REG3284	7:0	Default : 0x00	Access : R/W
	TESTMOD_REG[7:0]	7:0	Test mode select.	
42h (3285h)	REG3285	7:0	Default : 0x90	Access : R/W
	-	7:5	Reserved.	
	SW_RST	4	Software reset; active low.	
	SELGPO_TG_REG[3:0]	3:0	Select GPO to TG.	
43h (3286h)	REG3286	7:0	Default : 0x00	Access : R/W
	SELGPO_REG[7:0]	7:0	GPO mode select.	
43h	REG3287	7:0	Default : 0x00	Access : R/W

DISP_MISC Register (Bank = 32)

Index (Absolute)	Mnemonic	Bit	Description	
(3287h)	-	7:6	Reserved.	
	SELGPO_REG[13:8]	5:0	Please see description of '3286h'.	
44h (3288h)	**REG3288**	**7:0**	**Default : 0x00**	**Access : R/W**
	SELTTL_REG[7:0]	7:0	TTL mode select.	
44h (3289h)	**REG3289**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SELTTL_REG[13]	5	Select LDE (GPIOE[2]), LCK (GPIOE[3]) as TTL output.	
	SELTTL_REG[12]	4	Select LVSYNC (GPIOE[0]), HSYNC (GPIOE[1]) as TTL output.	
	SELTTL_REG[11:8]	3:0	Please see description of '3288h'.	
45h (328Ah)	**REG328A**	**7:0**	**Default : 0x3F**	**Access : R/W**
	-	7:6	Reserved.	
	LVDS_LA_OEZ	5	Enable LVDS A port output; for LVDS output, must set as "1".	
	LVDS_LB_OEZ	4	Enable LVDS B port output; for LVDS output, must set as "1".	
	CK_OEZ	3	CLK output enable. 0: Disable. 1: Enable.	
	DE_OEZ	2	Data valid output enable. 0: Disable. 1: Enable.	
	HS_OEZ	1	HSYNC output enable. 0: Disable. 1: Enable.	
	VS_OEZ	0	VSYNC output enable. 0: Disable. 1: Enable.	
45h (328Bh)	**REG328B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	DHC_OUT_EN	2	Output data in HDE blanking period. DHC_DDR_G0: HSYNC DHC_DDR_G1: TO_PAD_FIELD	
	-	1:0	Reserved.	
46h	**REG328C**	**7:0**	**Default : 0x00**	**Access : R/W**

DISP_MISC Register (Bank = 32)

Index (Absolute)	Mnemonic	Bit	Description	
(328Ch)	EXT_DATA_EN[7:4]	7:4	Enable external data output by TTL pad.	
	EXT_DATA_EN[3]	3	Enable LCK (GPIOE[3]) as GPIO or external data, when GPO_SEL[3] = 1, as GPIO pad; GPO_SEL[3] = 0, as external data output. This bit is effective when SELTTL_REG[13] is high.	
	EXT_DATA_EN[2]	2	Enable LDE (GPIOE[2]) as GPIO or external data, when GPO_SEL[2] = 1, as GPIO pad; GPO_SEL[2] = 0, as external data output. This bit is effective when SELTTL_REG[13] is high.	
	EXT_DATA_EN[1]	1	Enable LHSYNC (GPIOE[1]) as GPIO or external data, when GPO_SEL[1] = 1, as GPIO pad; GPO_SEL[1] = 0, as external data output. This bit is effective when SELTTL_REG[12] is high.	
	EXT_DATA_EN[0]	0	Enable PAD_LVSYNC (GPIOE[0]) as GPIO or external data, when GPO_SEL[0] = 1, as GPIO pad; GPO_SEL[0] = 0, as external data output. This bit is effective when SELTTL_REG[12] is high.	
46h (328Dh)	REG328D	7:0	Default : 0x00	Access : R/W
	EXT_DATA_EN[15:8]	7:0	Please see description of '328Ch'.	
47h (328Eh)	REG328E	7:0	Default : 0x00	Access : R/W
	EXT_DATA_EN[23:16]	7:0	Please see description of '328Ch'.	
47h (328Fh)	REG328F	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	EXT_DATA_EN[27:24]	3:0	Please see description of '328Ch'.	
48h (3290h)	REG3290	7:0	Default : 0x00	Access : R/W
	DRV_HS	7	Over drive for HSYNC.	
	DRV_DE	6	Over drive for data valid.	
	DRV_CLK	5	Over drive for clock.	
	EN2IB	4	Enable double current.	
	EN_ETLRG	3	Enable even channel TLRG.	
	EN_OTLRG	2	Enable odd channel TLRG.	
	EN_TG	1	Enable TG output.	
	MOD_PDN	0	Mod power down.	

DISP_MISC Register (Bank = 32)

Index (Absolute)	Mnemonic	Bit	Description	
48h (3291h)	REG3291	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	DRV_VS	0	Over drive for VSYNC.	
49h (3292h)	REG3292	7:0	Default : 0x00	Access : R/W
	MLX_METHOD[1:0]	7:6	MSB LSB swap method.	
	ERGX	5	Even channel R, G data swap.	
	EGBX	4	Even channel G, B data swap.	
	ORGX	3	Odd channel R, G data swap.	
	OGBX	2	Odd channel G, B data swap.	
	FRONT_BACK	1	Front back select.	
	INTERLACE_OUT	0	Interlace out select.	
49h (3293h)	REG3293	7:0	Default : 0x00	Access : R/W
	GATE_DE	7	Date data valid.	
	EMLX	6	MSB LSB inverse for even channel.	
	ERBX	5	Even channel R B data swap.	
	OMLX	4	MSB LSB inverse for odd channel.	
	ORBX	3	Odd channel R B data swap.	
	OBN	2	Output is 6-bit select.	
	WDG	1	Set output pixel to white during blanking period.	
	REVL	0	Invert output pixel.	
4Ah (3294h)	REG3294	7:0	Default : 0x00	Access : R/W
	SVM_HALF_STEP	7	SVM half step.	
	TTL_LVDS	6	TTL LVDS select.	
	CLKB_TC_REG	5	Output TTL clock gate with GPOA enable.	
	CLK_INVERT	4	Clock invert.	
	VS_INVERT	3	VSYNC invert.	
	DE_INVERT	2	Data valid invert.	
	DUALMD	1	Dual model select.	
	ABSWITCH	0	A B port swap (only used when dual mode is enabled).	
4Ah (3295h)	REG3295	7:0	Default : 0x00	Access : R/W
	AUTOVS_EARLY	7	Enable auto v.s. early function.	
	INTER_HS	6	TTL mode interlace out HSYNC signal enable.	
	INTERLACE_HS_GATE	5	Gate for interlace HSYNC.	

DISP_MISC Register (Bank = 32)

Index (Absolute)	Mnemonic	Bit	Description	
	HS_INVERT	4	HSYNC invert.	
	HS_REMO	3	TTL mode HSYNC gate with GPOA_FF enable.	
	OCP	2	OCLK polarity. 0: Normal. 1: Invert.	
	ECP	1	ECLK polarity. 0: Normal. 1: Invert.	
	PUA	0	TTL VSYNC and clock output enable.	
4Bh (3296h)	REG3296	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	MASK_TTL_DUAL	2	Mask TTL dual mode.	
	SEL_TCLK	1	Select TCLK.	
	RSDS_SWAP_B	0	Swap RSDS_B.	
4Ch (3297h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
4Ch (3298h)	REG3298	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	CRC_EN	3	Enable CRC function.	
	CHANNEL_SEL[2:0]	2:0	Channel select for CRC check. 0: Odd channel data R. 1: Odd channel data G. 2: Odd channel data B. 3: Odd channel data B. 4: Even channel data R. 5: Even channel data G. 6: Even channel data B. 7: Even channel data B.	
4Dh (329Ah)	REG329A	7:0	Default : 0x00	Access : R/W
	GPO_SEL[7:4]	7:4	Select pad as GPIO.	
	GPO_SEL[3]	3	Set LCK (GPIOE[3]) as GPIO, this bit is effective when EXT_DATA_EN[3] and SELTTL_REG[13] are high.	
	GPO_SEL[2]	2	Set LDE (GPIOE[2]) as GPIO, this bit is effective when EXT_DATA_EN[2] and SELTTL_REG[13] are high.	
	GPO_SEL[1]	1	Set LHSYNC (GPIOE[1]) as GPIO, this bit is effective when EXT_DATA_EN[1] and SELTTL_REG[12] are high.	

DISP_MISC Register (Bank = 32)

Index (Absolute)	Mnemonic	Bit	Description	
	GPO_SEL[0]	0	Set LVSYNC (GPIOE[0]) as GPIO, this bit is effective when EXT_DATA_EN[0] and SELTTL_REG[12] are high.	
4Dh (329Bh)	**REG329B**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPO_SEL[15:8]	7:0	Please see description of '329Ah'.	
4Eh (329Ch)	**REG329C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPO_SEL[23:16]	7:0	Please see description of '329Ah'.	
4Eh (329Dh)	**REG329D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GPO_SEL[27:24]	3:0	Please see description of '329Ah'.	
4Fh (329Eh)	**REG329E**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPO_DATAIN[7:4]	7:4	Data for GPIO output.	
	GPO_DATAIN[3]	3	Data for LCK (GPIOE[3]) output.	
	GPO_DATAIN[2]	2	Data for LDE (GPIOE[2]) output.	
	GPO_DATAIN[1]	1	Data for LHSYNC (GPIOE[1]) output.	
	GPO_DATAIN[0]	0	Data for LVSYNC (GPIOE[0]) output.	
4Fh (329Fh)	**REG329F**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPO_DATAIN[15:8]	7:0	Please see description of '329Eh'.	
50h (32A0h)	**REG32A0**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPO_DATAIN[23:16]	7:0	Please see description of '329Eh'.	
50h (32A1h)	**REG32A1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GPO_DATAIN[27:24]	3:0	Please see description of '329Eh'.	
51h (32A2h)	**REG32A2**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPO_OEZ[7:4]	7:4	GPIO output enable.	
	GPO_OEZ[3]	3	Output enable for LCK (GPIOE[3]). 0: Output, data is set in GPO_DATAIN[3]. 1: Input, input data is in MOD_GPI[3].	
	GPO_OEZ[2]	2	Output enable for PAD_LDE (GPIOE[2]). 0: Output, data is set in GPO_DATAIN[2]. 1: Input , input data is in MOD_GPI[2].	
	GPO_OEZ[1]	1	Output enable for Data for PAD_LHSYNC (GPIOE[1]). 0: Output, data is set in GPO_DATAIN[1]. 1: Input, input data is in MOD_GPI[1].	

DISP_MISC Register (Bank = 32)

Index (Absolute)	Mnemonic	Bit	Description	
	GPO_OEZ[0]	0	Output enable for Data for PAD_LVSYNC (GPIOE[0]). 0: Output, data is set in GPO_DATAIN[0]. 1: Input, input data is in MOD_GPI[0].	
51h (32A3h)	**REG32A3**	**7:0**	Default : 0x00	Access : R/W
	GPO_OEZ[15:8]	7:0	Please see description of '32A2h'.	
52h (32A4h)	**REG32A4**	**7:0**	Default : 0x00	Access : R/W
	GPO_OEZ[23:16]	7:0	Please see description of '32A2h'.	
52h (32A5h)	**REG32A5**	**7:0**	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	GPO_OEZ[27:24]	3:0	Please see description of '32A2h'.	
54h (32A8h)	**REG32A8**	**7:0**	Default : -	Access : RO
	CRC_OUT[7:0]	7:0	CRC check result.	
54h (32A9h)	**REG32A9**	**7:0**	Default : -	Access : RO
	CRC_OUT[15:8]	7:0	Please see description of '32A8h'.	
55h (32AAh)	**REG32AA**	**7:0**	Default : -	Access : RO
	MOD_GPI[7:4]	7:4	GPIO input data.	
	MOD_GPI[3]	3	LCK (GPIOE[3]) input data.	
	MOD_GPI[2]	2	LDE (GPIOE[2]) input data.	
	MOD_GPI[1]	1	LHSYNC (GPIOE[1]) input data.	
	MOD_GPI[0]	0	LVSYNC (GPIOE[0]) input data.	
55h (32ABh)	**REG32AB**	**7:0**	Default : -	Access : RO
	MOD_GPI[15:8]	7:0	Please see description of '32AAh'.	
56h (32ACh)	**REG32AC**	**7:0**	Default : -	Access : RO
	MOD_GPI[23:16]	7:0	Please see description of '32AAh'.	
56h (32ADh)	**REG32AD**	**7:0**	Default : -	Access : RO
	-	7:4	Reserved.	
	MOD_GPI[27:24]	3:0	Please see description of '32AAh'.	
57h (32AEh)	**REG32AE**	**7:0**	Default : 0x00	Access : R/W
	ATCON_OEN[7:0]	7:0	ATCON output enable.	
57h (32AFh)	**REG32AF**	**7:0**	Default : 0x00	Access : R/W
	-	7	Reserved.	
	ATCON_OEN[14:8]	6:0	Please see description of '32AEh'.	
58h	**REG32B0**	**7:0**	Default : 0x00	

DISP_MISC Register (Bank = 32)

Index (Absolute)	Mnemonic	Bit	Description	
(32B0h)	DTCON_OEN[7:0]	7:0	DTCON output enable.	
58h (32B1h)	**REG32B1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	DTCON_OEN[9:8]	1:0	Please see description of '32B0h'.	
59h (32B2h)	**REG32B2**	**7:0**	**Default : 0x00**	**Access : R/W**
	ATCON_SEL[3:0]	7:4	Select ATCON output.	
	DTCON_SEL[3:0]	3:0	Select DTCON output.	
59h (32B3h)	**REG32B3**	**7:0**	**Default : 0x00**	**Access : R/W**
	DHC_MD_0	7:6	DHC mode select bit 0.	
	DHC_MD_1	5:4	DHC mode select bit 1. 00: TTL output mode. 01: DDR output mode. 10: Audio test in mode. 11: Audio test out mode.	
	PWM_SEL[3:0]	3:0	Select PWM output.	
5Ah (32B4h)	**REG32B4**	**7:0**	**Default : 0x30**	**Access : R/W**
	SWAP_CHANNEL_R	7	0: Not for RLV. 1: Swap channel.	
	SWAP_CHANNEL_L	6	0: Not for LLV. 1: Swap channel.	
	SWAP_PN_R	5	0: Not for RLV. 1: Swap PN.	
	SWAP_PN_L	4	0: Not for LLV. 1: Swap PN.	
	SWAP_ML_R	3	0: Not for RLV. 1: Swap ML.	
	SWAP_ML_L	2	0: Not for LLV. 1: Swap ML.	
	SWAP_LPL6B5L_R	1	1: LPL6B5L special swap in R channel.	
	SWAP_LPL6B5L_L	0	1: LPL6B5L special swap in L channel.	
5Ah (32B5h)	**REG32B5**	**7:0**	**Default : 0x03**	**Access : R/W**
	VIEW_FIFOCLKDIV4	7	1: View FIFOCLKDIV4.	
	MINICLK_INV	6	1: Inverse MINICLK.	
	MINI_TST	5	1: Mini LVDS test mode.	
	SWAP_RL	4	1: Swap R&L channel.	

DISP_MISC Register (Bank = 32)

Index (Absolute)	Mnemonic	Bit	Description	
	ENDDATA	3	0: End data = 1'b0. 1: End data = 1'b1.	
	TP_MOD	2	0: Detect DE out edge for reset. 1: Detect TP1 edge for reset.	
	MINOCLK_DIV2_INV	1	1: MINICLK_DIV2 inverse.	
	SOFT_RSTZ	0	0: Software reset. 1: Normal operation.	
5Bh (32B6h)	REG32B6	7:0	Default : 0x00	Access : R/W
	SWAP_ORDER_L[5:0]	7:2	0: Not for LLV. 1: Swap order.	
	SWAP_4PAIR_R	1	1: Swap 4 pairs in R channel.	
	SWAP_4PAIR_L	0	1: Swap 4 pairs in L channel.	
5Bh (32B7h)	REG32B7	7:0	Default : 0x00	Access : R/W
	SWAP_ORDER_R[5:0]	7:2	0: Not for RLV. 1: Swap order.	
	SWAP2_LPL6B5L_R	1	1: LPL6B5L special swap2 in R channel.	
	SWAP2_LPL6B5L_L	0	1: LPL6B5L special swap2 in L channel.	
5Ch (32B8h)	REG32B8	7:0	Default : 0x00	Access : R/W
	MINITP1_PIPE[2:0]	7:5	TP1 to MINI_INST pipe select (0_7).	
	CKDATA_ASSIGN[2:0]	4:2	CK data channel assignment.	
	-	1:0	Reserved.	
5Ch (32B9h)	REG32B9	7:0	Default : 0x1C	Access : R/W
	MOD[2:0]	7:5	000: MOD0. 001: MOD1. 010: MOD2. 011: MOD3. 100: MOD4. 101: MOD5. 110: MOD6. 111: MOD7.	
	DELAY_PROG[2:0]	4:2	Program delay of DE out negative edge detect for designer.	
	-	1:0	Reserved.	
5Dh (32BAh)	REG32BA	7:0	Default : 0x00	Access : R/W
	LVD1_CHASSIGN[2:0]	7:5	LVD1 data channel assignment.	

DISP_MISC Register (Bank = 32)

Index (Absolute)	Mnemonic	Bit	Description	
	LVD2_CHASSIGN[2:0]	4:2	LVD2 data channel assignment.	
	-	1:0	Reserved.	
5Dh (32BBh)	REG32BB	7:0	Default : 0x18	Access : R/W
	-	7	Reserved.	
	MINOGPO_SEL[3:0]	6:3	GPO select for TP1 (0-10).	
	LVD0_CHASSIGN[2:0]	2:0	LVD0 data channel assignment.	
5Eh (32BCh)	REG32BC	7:0	Default : 0x00	Access : R/W
	LVD4_CHASSIGN[2:0]	7:5	LVD4 data channel assignment.	
	LVD5_CHASSIGN[2:0]	4:2	LVD5 data channel assignment.	
	DELAY_EN_INV	1	1: Inverse DELY_EN.	
	6BIT_MSB	0	1: Catch 6 bits MSB of 8 bits RGB.	
5Eh (32BDh)	REG32BD	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	LVD3_CHASSIGN[2:0]	2:0	LVD3 data channel assignment.	
5Fh (32BEh)	REG32BE	7:0	Default : 0x18	Access : R/W
	TP1RISE_CNT[7:0]	7:0	Program the TP1 delay time for the inner counter.	
60h (32C0h)	REG32C0	7:0	Default : 0x22	Access : R/W
	DIVN_S[3:0]	7:4	0010/0011/0100/0101/0110/0111/1000/1001/1010/1100: DIV 2/3/4/5/6/7/8/9/10/12 (LOOP-DIVIDER).	
	DIVM_S[3:0]	3:0	0010/0011/0100/0101/0110/0111/1000/1001/1010/1100: DIV 1/1.5/2/2.5/3/3.5/4/4.5/5/6 (POST-DIVIDER).	
61h (32C2h)	REG32C2	7:0	Default : 0x00	Access : R/W
	MINICLK_EN[7:0]	7:0	M-LVDS clock channel enabled for RLV & LLV.	
61h (32C3h)	REG32C3	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	MINICLK_EN[13:8]	5:0	Please see description of '32C2h'.	
62h (32C4h)	REG32C4	7:0	Default : 0x00	Access : R/W
	PE_CUR_DA[1:0]	7:6	Pre-emphasis drive level control for data channel.	
	PE_CUR_CK[1:0]	5:4	Pre-emphasis drive level control for clock channel.	
	PE_EN_DA	3	Enable pre-emphasis for data channel. 0: Disable. 1: Enable.	

DISP_MISC Register (Bank = 32)

Index (Absolute)	Mnemonic	Bit	Description	
	PE_EN_CK	2	Enable pre-emphasis for clock channel. 0: Disable. 1: Enable.	
	PE_SET	1	Set for pre-emphasis of M-LVDS. 0: Disable. 1: Enable.	
	PE_RST	0	Reset for pre-emphasis of M-LVDS. 0: Disable. 1: Enable.	
62h (32C5h)	REG32C5	7:0	Default : 0x00	Access : R/W
	ENDCCN	7	Enable divider N (LOOP-DIVIDER) duty-cycle correction.	
	ENDCCM	6	Enable divider M (POST-DIVIDER) duty-cycle correction.	
	EN_MINILVDS	5	Enable mini-LVDS mode.	
	MINILCK_SET	4	Set for clock channel of M-LVDS. 0: Disable. 1: Enable.	
	MINILCK_RST	3	Reset for clock channel of M-LVDS. 0: Disable. 1: Enable.	
	MINILCKL_POL	2	Polarity control for LLV clock channel.	
	MINILCKR_POL	1	Polarity control for RLV clock channel.	
	SELVCM	0	LVDS/RSDS/M-LVDS common mode voltage adjustment. 0: VDDP*0.375. 1: VDDP*0.286.	
63h (32C6h)	REG32C6	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	USE_HFDE	6	Using 0x65 to define half length of HFDE.	
	P1440	5	Using 1440 to define half length of HFDE.	
	RSDS_LB_EN	4	Enable mini-LVDS line buffer.	
	-	3:0	Reserved.	
64h (32C8h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
65h (32CAh)	REG32CA	7:0	Default : 0x00	Access : R/W
	HFDE_BY2[7:0]	7:0	Define mini-LVDS half length value of horizontal DE.	
65h	REG32CB	7:0	Default : 0x00	Access : R/W

DISP_MISC Register (Bank = 32)

Index (Absolute)	Mnemonic	Bit	Description		
(32CBh)	-	7:2	Reserved.		
	HFDE_BY2[9:8]	1:0	Please see description of '32CAh'.		
66h (32CCh)	REG32CC	7:0	Default : 0x00	Access : R/W	
	EDEST[7:0]	7:0	Reserved.		
66h (32CDh)	REG32CD	7:0	Default : 0x00	Access : R/W	
	-	7:3	Reserved.		
	EDEST[10:8]	2:0	Please see description of '32CCh'.		
67h (32CEh)	-	7:0	Default : -	Access : -	
	-	7:0	Reserved.		
67h (32CFh)	REG32CF	7:0	Default : 0x00	Access : R/W	
	-	7:3	Reserved.		
	EDEEND[10:8]	2:0	Please see description of '32CEh'.		
68h (32D0h)	REG32D0	7:0	Default : 0x00	Access : R/W	
	-	7:0	Reserved.		
68h (32D1h)	REG32D1	7:0	Default : 0x00	Access : R/W	
	-	7:3	Reserved.		
	SYNCST[10:8]	2:0	Please see description of '32D0h'.		
69h (32D2h)	-	7:0	Default : -	Access : -	
	-	7:0	Reserved.		
69h (32D3h)	REG32D3	7:0	Default : 0x00	Access : R/W	
	-	7:3	Reserved.		
	SYNCEND[10:8]	2:0	Please see description of '32D2h'.		
6Ah ~ 6Bh (32D4h ~ 32D7h)	-	7:0	Default : -	Access : -	
	-	7:0	Reserved.		

IIC Register (Bank = 34)

IIC Register (Bank = 34)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (3420h)	REG3420	7:0	Default : 0x10	Access : R/W
	MENABLE	7	Master I2C enable.	
	SBIT	6	Start bit assert.	
	PBIT	5	Stop bit assert.	
	MACKO	4	ACK output.	
	MACKI	3	ACK input.	
	-	2	Reserved.	
	CLR_NEW_DATA	1	Clear new data flag.	
	RESERVED0	0	Reserved.	
10h (3421h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
11h (3422h)	REG3422	7:0	Default : 0x10	Access : R/W
	MCLK_SEL[7:0]	7:0	Master IIC0 clock select. 1: CLK/4. 2: CLK/8. 3: CLK/16. 4: CLK/32. 5: CLK/ 64. 6: CLK/128. 7: CLK/256. 8: CLK/512. 9: CLK/1024. OTHERS: CLK/2.	
11h (3423h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
12h (3424h)	REG3424	7:0	Default : 0x10	Access : R/W
	WMBUF[7:0]	7:0	Write data.	
12h (3425h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
13h (3426h)	REG3426	7:0	Default : -	Access : RO
	RMBUF[7:0]	7:0	Read data.	
13h (3427h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	

IIC Register (Bank = 34)

Index (Absolute)	Mnemonic	Bit	Description	
14h (3428h)	REG3428	7:0	Default : 0x10	Access : RO, R/W, WO
	-	7:4	Reserved.	
	MIIC_RST	3	Set 1 to reset MIIC circuit.	
	RD_START	2	Set 1 to start byte reading.	
	INT_CLR	1	Set 1 to clear IIC0 interrupt status.	
	INT_STATUS	0	Used for software polling, the bit is set if byte write or byte read is finished. The interrupt status can be cleared by writing INT_CLR bit.	
14h (3429h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	

PWM Register (Bank = 34)

PWM Register (Bank = 34)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
30h (3460h)	REG3460	7:0	Default : 0x30	Access : R/W
	PWM_DBEN	7	PWM0 and PWM1 double buffer enable. 0: Disable. 1: Enable.	
	PWM_RESET_EN1	6	PWM1 reset every frame enable. 0: Disable. 1: Enable.	
	PWM_RESET_EN0	5	PWM0 reset every frame enable. 0: Disable. 1: Enable.	
	NEW_POLARITY1	4	PWM1 polarity when enhanced PWM1 enable.	
	NEW_PWM_METHOD1	3	Enhance PWM1 enable. 0: Disable. 1: Enable.	
	NEW_POLARITY0	2	PWM0 polarity when enhanced PWM0 enable.	
	NEW_PWM_METHOD0	1	Enhance PWM0 enable. 0: Disable. 1: Enable.	
	PWM_CLK_SEL	0	PWM 0 and PWM1 base clock select. 0: Crystal clock. 1: Crystal clock/4.	
30h (3461h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
31h (3462h)	REG3462	7:0	Default : 0x30	Access : R/W
	PWM_PERIOD0[7:0]	7:0	Enhanced PWM0 period.	
31h (3463h)	REG3463	7:0	Default : 0x30	Access : R/W
	PWM_PERIOD0[15:8]	7:0	Please see description of '3462h'.	
32h (3464h)	REG3464	7:0	Default : 0x30	Access : R/W
	PWM_PERIOD1[7:0]	7:0	Enhanced PWM1 period.	
32h (3465h)	REG3465	7:0	Default : 0x30	Access : R/W
	PWM_PERIOD1[15:8]	7:0	Please see description of '3464h'.	
33h (3466h)	REG3466	7:0	Default : 0x00	Access : R/W
	PWM0_CTUN[7:0]	7:0	PWM0 coarse adjustment.	
33h	REG3467	7:0	Default : 0x00	Access : R/W

PWM Register (Bank = 34)

Index (Absolute)	Mnemonic	Bit	Description	
(3467h)	PWM1_CTUN[7:0]	7:0	PWM1 coarse adjustment.	
34h (3468h)	REG3468	7:0	Default : 0x30	Access : R/W
	PWM2_DBEN	7	PWM2 and PWM3 double buffer enable. 0: Disable. 1: Enable.	
	PWM2_RESET_EN1	6	PWM3 reset every frame enable. 0: Disable. 1: Enable.	
	PWM2_RESET_EN0	5	PWM2 reset every frame enable. 0: Disable. 1: Enable.	
	NEW2_POLARITY1	4	PWM3 polarity when enhanced PWM3 enable.	
	NEW2_PWM_METHOD1	3	Enhance PWM3 enable. 0: Disable. 1: Enable.	
	NEW2_POLARITY0	2	PWM2 polarity when enhanced PWM2 enable.	
	NEW2_PWM_METHOD0	1	Enhance PWM2 enable. 0: Disable. 1: Enable.	
	PWM2_CLK_SEL	0	PWM 2 and PWM3 base clock select. 0: Crystal clock. 1: Crystal clock/4.	
34h (3469h)	REG3469	7:0	Default : 0x00	Access : R/W
	VS_RST_EN[3:0]	7:4	Counter reset enable (PWM3~PWM0) for every VSYNC.	
	-	3:1	Reserved.	
	PWM20_CTUN[7]	0	Bit [7] of PWM2 coarse adjustment.	
35h (346Ah)	REG346A	7:0	Default : 0x30	Access : R/W
	PWM2_PERIOD0[7:0]	7:0	Enhanced PWM2 period.	
35h (346Bh)	REG346B	7:0	Default : 0x30	Access : R/W
	PWM2_PERIOD0[15:8]	7:0	Please see description of '346Ah'.	
36h (346Ch)	REG346C	7:0	Default : 0x30	Access : R/W
	PWM2_PERIOD1[7:0]	7:0	Enhanced PWM3 period.	
36h (346Dh)	REG346D	7:0	Default : 0x30	Access : R/W
	PWM2_PERIOD1[15:8]	7:0	Please see description of '346Ch'.	
37h	REG346E	7:0	Default : 0x00	Access : R/W

PWM Register (Bank = 34)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(346Eh)	PWM20_ALT_EN	7	Alternate PWM2 enable. 0: Disable. 1: Enable.	
	PWM20_CTUN[6:0]	6:0	Bit [6:0] of PWM2 coarse adjustment.	
37h (346Fh)	**REG346F**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM21_CTUN[7:0]	7:0	PWM3 coarse adjustment.	
38h (3470h)	**REG3470**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM3_RST_SEL	7	PWM3 reset select. 0: VSYNC. 1: HSYNC or VSYNC.	
	PWM2_RST_SEL	6	PWM2 reset select. 0: VSYNC. 1: HSYNC or VSYNC.	
	PWM1_RST_SEL	5	PWM1 reset select. 0: VSYNC. 1: HSYNC or VSYNC.	
	PWM0_RST_SEL	4	PWM0 reset select. 0: VSYNC. 1: HSYNC or VSYNC.	
	HSYNC_CNT[3:0]	3:0	HSYNC count threshold to reset PWM.	
38h (3471h)	**REG3471**	**7:0**	**Default : 0x30**	**Access : R/W**
	-	7:5	Reserved.	
	PWM5_TRIG[12:8]	4:0	Please see description of '3470h'.	
39h (3472h)	**REG3472**	**7:0**	**Default : 0x30**	**Access : R/W**
	PWM6_TRIG[7:0]	7:0	PWM6 period.	
39h (3473h)	**REG3473**	**7:0**	**Default : 0x30**	**Access : R/W**
	-	7:5	Reserved.	
	PWM6_TRIG[12:8]	4:0	Please see description of '3472h'.	

RTC Register (Bank = 34)

RTC Register (Bank = 34)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
40h (3480h)	REG3480	7:0	Default : 0x21	Access : R/W
	C_INT_CLEAR	7	Clear RTC interrupt.	
	C_INT_FORCE	6	Force RTC interrupt to be 1.	
	C_INT_MASK	5	Mask RTC interrupt.	
	C_READ_EN	4	Read enable for reading value from RTC counter (write and generate one-shot signal for latching RTC_CNT).	
	C_LOAD_EN	3	Load enable for loading value into RTC counter (write and generate one-shot enable signal).	
	C_WRAP_EN	2	Wrap RTC counter when C_MATCH_VAL is reached.	
	C_CNT_EN	1	Enable RTC counter.	
	C_SOFT_RSTZ	0	RTC software reset (low active).	
41h (3482h)	REG3482	7:0	Default : 0xFF	Access : R/W
	C_FREQ_CW[7:0]	7:0	Frequency control word of RTC counter. Clock frequency of RTC counter = XTAL_FREQUENCY/CONTROL_WORD	
41h (3483h)	REG3483	7:0	Default : 0x7F	Access : R/W
	C_FREQ_CW[15:8]	7:0	Please see description of '3422h'.	
42h (3484h)	REG3484	7:0	Default : 0x00	Access : R/W
	C_FREQ_CW[23:16]	7:0	Please see description of '3422h'.	
42h (3485h)	REG3485	7:0	Default : 0x00	Access : R/W
	C_FREQ_CW[31:24]	7:0	Please see description of '3422h'.	
43h (3486h)	REG3486	7:0	Default : 0x00	Access : R/W
	C_LOAD_VAL[7:0]	7:0	Value to load into RTC counter.	
43h (3487h)	REG3487	7:0	Default : 0x00	Access : R/W
	C_LOAD_VAL[15:8]	7:0	Please see description of '3426h'.	
44h (3488h)	REG3488	7:0	Default : 0x00	Access : R/W
	C_LOAD_VAL[23:16]	7:0	Please see description of '3426h'.	
44h (3489h)	REG3489	7:0	Default : 0x00	Access : R/W
	C_LOAD_VAL[31:24]	7:0	Please see description of '3426h'.	
45h (348Ah)	REG348A	7:0	Default : 0xFF	Access : R/W
	C_MATCH_VAL[7:0]	7:0	Counter match value.	
45h	REG348B	7:0	Default : 0xFF	Access : R/W

RTC Register (Bank = 34)

Index (Absolute)	Mnemonic	Bit	Description	
(348Bh)	C_MATCH_VAL[15:8]	7:0	Please see description of '342Ah'.	
46h (348Ch)	**REG348C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	C_MATCH_VAL[23:16]	7:0	Please see description of '342Ah'.	
46h (348Dh)	**REG348D**	**7:0**	**Default : 0xFF**	**Access : R/W**
	C_MATCH_VAL[31:24]	7:0	Please see description of '342Ah'.	
47h (348Eh)	**REG348E**	**7:0**	**Default : -**	**Access : RO**
	-	7:2	Reserved.	
	RTC_INT	1	RTC interrupt status.	
	RTC_RAW_INT	0	Raw interrupt status.	
48h (3490h)	**REG3490**	**7:0**	**Default : -**	**Access : RO**
	RTC_CNT[7:0]	7:0	RTC counter value.	
48h (3491h)	**REG3491**	**7:0**	**Default : -**	**Access : RO**
	RTC_CNT[15:8]	7:0	Please see description of '3490h'.	
49h (3492h)	**REG3492**	**7:0**	**Default : -**	**Access : RO**
	RTC_CNT[23:16]	7:0	Please see description of '3490h'.	
49h (3493h)	**REG3493**	**7:0**	**Default : -**	**Access : RO**
	RTC_CNT[31:24]	7:0	Please see description of '3490h'.	
4Ah (3494h)	**REG3494**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIO_ACT_LEVEL[7:0]	7:0	GPIO pads active level for wakeup. 0: Active low. 1: Active high.	
4Ah (3495h)	**REG3495**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIO_SEL[7:0]	7:0	GPIO pads enable for wakeup 0: Disable. 1: Enable.	
4Bh (3496h)	**REG3496**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	CLR_VEC	7	Set 1 to clear wakeup source vector.	
	-	6	Reserved.	
	WAKEUP_VEC[5:0]	5:0	Wakeup source vector. [5]: PAD_INT interrupt. [4]: GPIO interrupt. [3]: IR interrupt. [2]: SAR ACT interrupt. [1]: RTC interrupt. [0]: CRC error.	

RTC Register (Bank = 34)

Index (Absolute)	Mnemonic	Bit	Description	
4Ch (3498h)	REG3498	7:0	Default : 0x00	Access : R/W
	PD_KEY[7:0]	7:0	Power down key; the system power down is enable if REG_PD_KEY[15:0] is set to 0x55AA.	
4Ch (3499h)	REG3499	7:0	Default : 0x00	Access : R/W
	PD_KEY[15:8]	7:0	Please see description of '3418h'.	
4Dh (349Ah)	REG349A	7:0	Default : 0x00	Access : R/W
	CRC_SAVE	7	Set 1 to start calculating golden CRC value of RTC.	
	-	6	Reserved.	
	HDMI_GATE	5	HDMI gate. 0: Enable HDMI signal. 1: Disable HDMI signal.	
	HDMI_WK_EN	4	HDMI wakeup enable. 0: Disable. 1: Enable.	
	EINT_WK_EN	3	PAD_INT wakeup enable. 0: Disable. 1: Enable.	
	EINT_ACT_LEVEL	2	PAD_INT active level for wakeup. 0: Active low. 1: Active high.	
	GPIO_WK_INT_EN	1	GPIO wakeup enable. 0: Disable. 1: Enable.	
	-	0	Reserved.	
4Dh (349Bh)	REG349B	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	MCU_PD_CLR	0	Set "1" to clear MCU power down signal.	

ECC Register (Bank = 34)

ECC Register (Bank = 34)					
Index (Absolute)	**Mnemonic**	**Bit**	**Description**		
70h (34E0h)	REG34E0	7:0	Default : 0x8F		Access : R/W
	DMAWR_SAFEMD	7	DMA write safe mode.		
	-	6:5	Reserved.		
	RST_ECC	4	Reset ECC kernel engine.		
	CAC_BYPASS	3	Cache bypass mode.		
	ORCRD_BYPASS	2	Open-risc read bypass mode enable.		
	MCURD_BYPASS	1	8051 read bypass mode enable.		
	DMAWR_BYPASS	0	DMAWR bypass mode enable.		
70h (34E1h)	REG34E1	7:0	Default : 0x02		Access : R/W
	RERD_NUM[3:0]	7:4	Re-read number. 0: Off. 1: Re-read once if error2 occurs.		
	CAC_RST	3	Cache reset flag (toggles when RST_D1T != RST_D2T).		
	CAC_FR_MD	2	Cache toggle mode (fast response in miss pre-fetch status).		
	CAC_WAYSEL	1	Cache 4Way/2Way select. 0: 2-way. 1: 4-way.		
	CAC_PREFETCH	0	Cache pre-fetch mode enable.		
71h (34E2h)	REG34E2	7:0	Default : 0x00		Access : R/W
	RESERVE01_A	7	Reserved.		
	ORC_BRDEN	6	Open-risc burst read enable (Re-read not supported).		
	MCU_BRDEN	5	MCU read burst read enable (Re-read not supported).		
	MEMRD_STRST	4	Memory read status reset.		
	DERR_RST_EN	3	Double error RST enable.		
	DERR_INT_EN	2	ECC double error interrupt enable.		
	DERR_RST	1	ECC double error reset.		
	SERR_RST	0	ECC single error reset.		
71h (34E3h)	REG34E3	7:0	Default : -		Access : -
	-	7:0	Reserved.		
72h (34E4h)	REG34E4	7:0	Default : 0x00		Access : R/W
	DMA_BASEADR[7:0]	7:0	DMA base address.		

ECC Register (Bank = 34)

Index (Absolute)	Mnemonic	Bit	Description	
72h (34E5h)	REG34E5	7:0	Default : 0x00	Access : R/W
	DMA_BASEADR[15:8]	7:0	Please see description of '34E4h'.	
73h (34E6h)	REG34E6	7:0	Default : 0x00	Access : R/W
	DMA_BASEADR[23:16]	7:0	Please see description of '34E4h'.	
74h (34E8h)	REG34E8	7:0	Default : 0x00	Access : R/W
	DMA_ECC_ENDADR[7:0]	7:0	DMA ECC end address.	
74h (34E9h)	REG34E9	7:0	Default : 0x00	Access : R/W
	DMA_ECC_ENDADR[15:8]	7:0	Please see description of '34E8h'.	
75h (34EAh)	REG34EA	7:0	Default : 0x00	Access : R/W
	DMA_ECC_ENDADR[23:16]	7:0	Please see description of '34E8h'.	
75h (34EBh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
76h (34ECh)	REG34EC	7:0	Default : 0x00	Access : R/W
	MCU_BASEADR[7:0]	7:0	8051 base address.	
76h (34EDh)	REG34ED	7:0	Default : 0x00	Access : R/W
	MCU_BASEADR[15:8]	7:0	Please see description of '34ECh'.	
77h (34EEh)	REG34EE	7:0	Default : 0x00	Access : R/W
	MCU_BASEADR[23:16]	7:0	Please see description of '34ECh'.	
77h (34EFh)	REG34EF	7:0	Default : 0x00	Access : R/W
	RESERVE07_A[7:0]	7:0	Reserved.	
78h (34F0h)	REG34F0	7:0	Default : 0x00	Access : R/W
	MCU_ECC_ENDADR[7:0]	7:0	8051 ECC end address.	
78h (34F1h)	REG34F1	7:0	Default : 0x00	Access : R/W
	MCU_ECC_ENDADR[15:8]	7:0	Please see description of '34F0h'.	
79h (34F2h)	REG34F2	7:0	Default : 0x00	Access : R/W
	MCU_ECC_ENDADR[23:16]	7:0	Please see description of '34F0h'.	
79h (34F3h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
7Ah (34F4h)	REG34F4	7:0	Default : 0x00	Access : R/W
	ORC_BASEADR[7:0]	7:0	Open-risc base address.	
7Ah (34F5h)	REG34F5	7:0	Default : 0x00	Access : R/W
	ORC_BASEADR[15:8]	7:0	Please see description of '34F4h'.	
7Bh	REG34F6	7:0	Default : 0x00	Access : R/W

ECC Register (Bank = 34)

Index (Absolute)	Mnemonic	Bit	Description	
(34F6h)	ORC_BASEADR[23:16]	7:0	Please see description of '34F4h'.	
7Bh (34F7h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
7Ch (34F8h)	REG34F8	7:0	Default : 0x00	Access : R/W
	ORC_ECC_ENDADR[7:0]	7:0	Open-risc ECC end address.	
7Ch (34F9h)	REG34F9	7:0	Default : 0x00	Access : R/W
	ORC_ECC_ENDADR[15:8]	7:0	Please see description of '34F8h'.	
7Dh (34FAh)	REG34FA	7:0	Default : 0x00	Access : R/W
	ORC_ECC_ENDADR[23:16]	7:0	Please see description of '34F8h'.	
7Dh ~ 7Fh (34FBh ~ 34FFh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	

AFEC Register (Bank = 35)

AFEC Register (Bank = 35)				
Index	**Mnemonic**	**Bit**	**Description**	
01h ~ 19h	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
1Ah	REG1A	7:0	Default : 0x40	Access : R/W
	SVIDEO_EN	7	0: Chroma source from CVBS-channel input. 1: Chroma source from C-channel input.	
	ADC_C_ALWAYS_ON	6	Chroma ADC 16fsc-to-4fsc down-sampling is enabled.	
	-	5:0	Reserved.	
1Bh ~ 6Eh	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
6Fh	REG6F	7:0	Default : 0x00	Access : R/W
	LINE_START_VF_SEL[1:0]	7:6	Line start V half line.	
	LINE_MIDDLE_VF_SEL[1:0]	5:4	Line middle V half line.	
	DPL_DPLDB	3	DPL_DE double mode enable.	
	DPL_DBDE	2	Double DE enable.	
	DPL_HSEN	1	DPL_HS mode enable.	
	DPL_DEEN	0	DPL _DE bypass mode enable.	
70h ~ 75h	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
76h	REG76	7:0	Default : 0x02	Access : R/W
	-	7:3	Reserved.	
	656_BLANK_MD	2	656 blank mode.	
	656_EN	1	656 enable. 0: Disable. 1: Enable.	
	-	0	Reserved.	
77h	REG77	7:0	Default : 0x02	Access : R/W
	656_BLANK_MAX[7:0]	7:0	Maximum of 656 blank region.	
78h	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
79h	REG79	7:0	Default : 0x18	Access : R/W
	656_HDES_O_9_2[7:0]	7:0	BT.656 SAV position. For VCR, 656_HDES = 656_HDES_O - 656_HDES_VCR_OFST * 4. Otherwise, 656_HDES = 656_HDES_O.	

AFEC Register (Bank = 35)

Index	Mnemonic	Bit	Description	
7Ah	**REG7A**	**7:0**	**Default : 0x20**	Access : R/W
	656_HDES_O_1_0[1:0]	7:6	656 H DE start.	
	-	5:2	Reserved.	
	656_INV_F	1	656 field inverse.	
	SELMIX	0	Mixed data out select.	
7Bh	**REG7B**	**7:0**	**Default : 0xB3**	Access : R/W
	656_HDEW[7:0]	7:0	BT.656 active data width (*4+4).	
7Ch ~ 7Fh	-	**7:0**	**Default : -**	Access : -
	-	7:0	Reserved.	
8Ch	**REG8C**	**7:0**	**Default : 0x4A**	Access : R/W
	TEST_Y[7:0]	7:0	Pattern generation Y.	
8Dh	**REG8D**	**7:0**	**Default : 0xAD**	Access : R/W
	TEST_CB[7:0]	7:0	Pattern generation Cb.	
8Eh	**REG8E**	**7:0**	**Default : 0x27**	Access : R/W
	TEST_CR[7:0]	7:0	Pattern generation Cr.	
8Fh	**REG8F**	**7:0**	**Default : 0x00**	Access : R/W
	-	7:4	Reserved.	
	FSC_TABLE_3_2[1:0]	3:2	Frequency synthesizer base. 0: 160MHz. 1: 15*14.31818MHz. 2: 216Mhz. 3: 15*14.31818MHz; only valid for REG_FSC_TABLE[4] = 1.	
	FSC_TABLE_1_0[1:0]	1:0	Frequency synthesizer output. 0: 4*fsc. 1: 8*fsc. 2: 16*fsc. 3: 16*fsc.	
92h ~ 95h	-	**7:0**	**Default : -**	Access : -
	-	7:0	Reserved.	
96h	**REG96**	**7:0**	**Default : 0xA0**	Access : R/W
	NOISE_DC_SEL[1:0]	7:6	Noise magnitude estimation DC level selection. 0: IIR_8. 1: IIR_8. 2: CCTRAP_13. 3: CCTRAP.	

AFEC Register (Bank = 35)

Index	Mnemonic	Bit	Description	
	EDGES_NOISY[5:0]	5:0	Threshold of the average number of sliced edges per line to determine noisy mode (/ 4).	
97h	**REG97**	**7:0**	Default : 0x05	Access : R/W
	SYNC_INMUX_3_2[1:0]	7:6	Slicer input pre-filter selection. Enable when SYNC_INMUX[0] = 0. 0: CCTRAP. 1: CCTRAP_13. 2: IIR_8. 3: IIR_16.	
	SYNC_INMUX_1	5	Slicer auxiliary pre-filter selection. 0: IIR_8. 1: IIR_16.	
	SYNC_INMUX_0	4	Slicer input pre-filter selection extend bit. 0: See SYNC_INMUX[3:2]. 1: IIR_4.	
	-	3:0	Reserved.	
98h ~ 9Ch	-	**7:0**	Default : -	Access : -
	-	7:0	Reserved.	
9Dh	**REG9D**	**7:0**	Default : 0x6C	Access : R/W
	DPL_NSPL_10_3[7:0]	7:0	PI-type display PLL number of samples per line (MSB). Typically 864.	
9Eh	**REG9E**	**7:0**	Default : 0x00	Access : R/W
	DPL_NSPL_2_0[2:0]	7:5	PI-type display PLL number of samples per line (LSB). Typically 864.	
	-	4:0	Reserved.	
9Fh ~ BDh	-	**7:0**	Default : -	Access : -
	-	7:6	Reserved.	
BEh	**REGBE**	**7:0**	Default : 0x6C	Access : R/W
	DPL_NSPL_656_10_3[7:0]	7:0	PI-type display PLL number of samples per line for BT.656 output (MSB). Typically 864.	
BFh	**REGBF**	**7:0**	Default : 0x00	Access : R/W
	DPL_NSPL_656_2_0[2:0]	7:5	PI-type display PLL number of samples per line for BT.656 output (LSB). Typically 864.	
	-	4:1	Reserved.	
	STD_656_EN	0	Enable standard 656 output.	
E3h ~	-	**7:0**	Default : -	Access : -

AFEC Register (Bank = 35)

Index	Mnemonic	Bit	Description
FFh	-	7:0	Reserved.

COMB Register (Bank = 36)

COMB Register (Bank = 36)				
Index	Mnemonic	Bit	Description	
10h	REG10	7:0	Default : 0x17	Access : R/W
	SVDOIN	7	S-video input.	
	SVDOCBP	6	Band pass filter for S-video C channel.	
	DIRADCIN	5	Direct use ADC input (bypass AFEC).	
	NEW_COMB_EN	4	New Comb enable.	
	MANUCOMB	3	0: Auto select working mode. 1: Manual select working mode.	
	WORKMD[2:0]	2:0	Working mode. 0/1: 1D. 2: 2D. 3: 3D. Other: Enhanced 3D.	
11h	REG11	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	CRMAOFF	1	Chroma off.	
	BSTOFF	0	Burst off.	
12h	REG12	7:0	Default : 0x18	Access : R/W
	FREESYNC	7	H/V sync free-run.	
	FREECNTMD	6	Free run counter mode. 0: NTSC. 1: PAL.	
	SNOWTYPE[1:0]	5:4	Snow type. 0: Never. 1: Auto. 2: Force.	
	VWINPOS[3:0]	3:0	Vertical window position.	
13h	REG13	7:0	Default : 0x05	Access : R/W
	-	7:6	Reserved.	
	DEMO3DMD[1:0]	5:4	2D/3D demo mode. 0x: Off. 10: 2D/3D. 11: 3D/2D.	
	-	3:2	Reserved.	
	PKTMD[1:0]	1:0	Packet mode. 00: 64 pixels per packet.	

COMB Register (Bank = 36)

Index	Mnemonic	Bit	Description	
			01: 128 pixels per packet.	
			10: 256 pixels per packet.	
			11: Reserved.	
14h	**REG14**	**7:0**	**Default : 0x88**	**Access : R/W**
	HSTRATIO[2:0]	7:5	History ratio.	
	NRLEVEL[4:0]	4:0	Noise reduction strength.	
15h	**REG15**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
16h	**REG16**	**7:0**	**Default : 0x70**	**Access : R/W**
	BNDOF2D3D[7:0]	7:0	Boundary of 2D/3D demo mode.	
17h	**REG17**	**7:0**	**Default : 0xC0**	**Access : R/W**
	HORSTPOS[7:0]	7:0	3D window horizontal starting position. 0..255 -> -128..127.	
18h	**REG18**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
19h	**REG19**	**7:0**	**Default : 0x8D**	**Access : R/W**
	FREEHTOT_LOW[7:0]	7:0	Free-run HSYNC total (L).	
1Ah	**REG1A**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:4	Reserved.	
	FREEHTOT_HIGH[3:0]	3:0	Free run HSYNC total (H).	
1Bh	**REG1B**	**7:0**	**Default : 0x83**	**Access : R/W**
	PHSDETEN	7	Line-lock phase detection enable.	
	PHSDETINV	6	Output inverse.	
	NEWLLEN	5	New line lock enable (for no burst).	
	SCLR_DO_DEM	4	New comb do DEM disable.	
	PAL_CMP_INV	3	New comb pal CMP up inverse bit.	
	PHSDETSFT[2:0]	2:0	Shift-right bit number.	
1Ch	**REG1C**	**7:0**	**Default : 0xEC**	**Access : R/W**
	HSFRAFEC	7	H sync from AFEC.	
	VSFRAFEC	6	V sync from AFEC.	
	BLKFRAFEC	5	Black level from AFEC (MCU).	
	-	4	Reserved.	
	LNFRMCU	3	525/625 line information from MCU.	
	FREQFRMCU	2	3.58/4.43 MHz information from MCU.	

COMB Register (Bank = 36)

Index	Mnemonic	Bit	Description	
	STDSEL[1:0]	1:0	NTSC/PAL decision. 00: From MCU. 01: Force NTSC. 10: Force PAL. 11: From AFEC.	
1Dh ~ 1Fh	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
20h	**REG20**	7:0	Default : 0x67	Access : R/W
	-	7	Reserved.	
	YNCHMD[2:0]	6:4	Notch mode of Y.	
	-	3	Reserved.	
	CNCHMD[2:0]	2:0	Notch mode of C.	
21h	**REG21**	7:0	Default : 0x81	Access : R/W
	-	7:4	Reserved.	
	CRMAFLTMD[1:0]	3:2	Chroma filter mode. 00: Off. 01: Band pass. 10: Median type A. 11: Median type B.	
	CDEMCHK[1:0]	1:0	Chroma vertical check (DEM). 00: Off. 01: PAL only. 1x: Always do.	
22h	**REG22**	7:0	Default : 0x86	Access : R/W
	-	7:4	Reserved.	
	NEWMOTYSEL	3	New motion Y selection.	
	NEWMOTYDIFFSEL	2	New motion Y difference selection.	
	STLMD_ECO[1:0]	1:0	Still mode selection.	
23h	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
24h	**REG24**	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	3DMOTDET5F	1	3D motion detection uses 5 frames.	
	MOTYC_STILECO	0	Still image motion detection add MOTYC.	
25h ~ 2Dh	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	

COMB Register (Bank = 36)

Index	Mnemonic	Bit	Description	
2Eh	**REG2E**	**7:0**	**Default : 0x0C**	**Access : R/W**
	THDEM[7:0]	7:0	Threshold for 2D comb filter, check separated chroma complement with up/down line or not.	
2Fh	**REG2F**	**7:0**	**Default : 0xF8**	**Access : R/W**
	NEWMOTYTH[3:0]	7:4	New motion Y threshold.	
	DEMOFFSET[3:0]	3:0	Threshold for 2D comb filter, check separated chroma complement with up/down line or not.	
30h	**REG30**	**7:0**	**Default : 0xA7**	**Access : R/W**
	MOTXEN	7	Extra reference of motion detection.	
	MOTXSEL	6	Extra motion mode.	
	MOTZEN	5	Ultra reference of motion detection.	
	LONG3D	4	Using 5 frame do Y/C separate.	
	MOTMD[1:0]	3:2	Motion different mode select.	
	DYNTHMD[1:0]	1:0	Dynamic threshold mode.	
31h	**REG31**	**7:0**	**Default : 0x20**	**Access : R/W**
	MOTYTHU[7:0]	7:0	Upper bound motion Y threshold.	
32h	**REG32**	**7:0**	**Default : 0x10**	**Access : R/W**
	MOTYTHL[7:0]	7:0	Lower bound motion Y threshold.	
33h	**REG33**	**7:0**	**Default : 0x20**	**Access : R/W**
	MOTCTHU[7:0]	7:0	Upper bound motion C threshold.	
34h	**REG34**	**7:0**	**Default : 0x10**	**Access : R/W**
	MOTCTHL[7:0]	7:0	Lower bound motion C threshold.	
35h	**REG35**	**7:0**	**Default : 0x20**	**Access : R/W**
	MOTTHX[7:0]	7:0	Extra motion threshold.	
36h	**REG36**	**7:0**	**Default : 0x30**	**Access : R/W**
	MOTTHZ[7:0]	7:0	Z-extra motion threshold.	
37h	**REG37**	**7:0**	**Default : 0x8C**	**Access : R/W**
	STLDET	7	Still image detection enable. 0: Disable. 1: Enable.	
	STLTH[6:0]	6:0	Still threshold.	
38h	**REG38**	**7:0**	**Default : 0x04**	**Access : R/W**
	MFMD[1:0]	7:6	Motion factor mode (MAX/AVG/MOTY/MOTC).	
	PAL3D_FLT_SEL	5	Use (DIFF+LPF) or (DIFF+MAX) in special domain.	

COMB Register (Bank = 36)

Index	Mnemonic	Bit	Description	
	PAL3D_DIFF_SEL	4	Use (DIFF) or (DIFF+MAX) in time domain.	
	COMB_3DETPC_SEL	3	Use chroma diff for 3D entropy calculation.	
	STDTRSP[2:0]	2:0	Still image detect response time. 000: 1 field. 001: 2 field. 010~110: Reserved. 111: 128 field.	
39h	**REG39**	**7:0**	Default : 0x02	Access : R/W
	STLBK[7:0]	7:0	Motion level go back when find motion once.	
3Ah	**REG3A**	**7:0**	Default : 0x30	Access : R/W
	DYNTH[7:0]	7:0	Dynamic motion threshold.	
3Bh	**REG3B**	**7:0**	Default : 0x00	Access : R/W
	NOISELVL[7:0]	7:0	Noise level for dynamic motion detection.	
3Ch	**REG3C**	**7:0**	Default : 0x2F	Access : R/W
	NEWMOTYEN	7	New motion Y enable.	
	NEWMOTCEN	6	New motion C enable.	
	NEWMOTCGAIN[1:0]	5:4	New motion C gain.	
	NEWMOTCTH[3:0]	3:0	New motion C threshold.	
3Dh	**REG3D**	**7:0**	Default : 0x00	Access : R/W
	MEMBASEADRH[7:0]	7:0	Base address of DRAM request (H).	
3Eh	**REG3E**	**7:0**	Default : 0x00	Access : R/W
	MEMBASEADRM[7:0]	7:0	Base address of DRAM request (M).	
3Fh	**REG3F**	**7:0**	Default : 0x00	Access : R/W
	MEMBASEADRL[7:0]	7:0	Base address of DRAM request (L).	
40h	**REG40**	**7:0**	Default : 0x9C	Access : R/W
	-	7:3	Reserved.	
	BLNKDETMD	2	Blank level detect mode. 0: Either 240 or 252. 1: 230~262 is possible.	
	VDETMD[1:0]	1:0	Vertical timing detect mode. 0x: Auto. 10: Force 525 line. 11: Force 625 line.	
41h	**REG41**	**7:0**	Default : 0x08	Access : R/W
	SENSSIGDET[7:0]	7:0	Sensitivity of signal detect.	

COMB Register (Bank = 36)

Index	Mnemonic	Bit	Description	
42h	**REG42**	**7:0**	**Default : 0xFF**	Access : R/W
	SYNCLVLTLRN[7:0]	7:0	Sync level tolerance.	
43h	**REG43**	**7:0**	**Default : 0x60**	Access : R/W
	VCRCOASTLEN[7:0]	7:0	VCR coast length.	
44h	**REG44**	**7:0**	**Default : 0x80**	Access : R/W
	HBIDLY[7:0]	7:0	Horizontal blanking region position.	
45h ~ 47h	-	**7:0**	**Default : -**	Access : -
	-	7:0	Reserved.	
48h	**REG48**	**7:0**	**Default : 0x20**	Access : R/W
	YCPIPE[1:0]	7:6	Y/C pipe delay.	
	DEGPIPE[1:0]	5:4	Degree pipe delay.	
	-	3:2	Reserved.	
	-	1:0	Reserved.	
49h	**REG3692**	**7:0**	**Default : 0x00**	Access : R/W
	FORCERATIO_SEL[7:0]	7:0	Force ratio selection.	
4Ah ~ 4Bh	-	**7:0**	**Default : -**	Access : -
	-	7:0	Reserved.	
4Ch	**REG4C**	**7:0**	**Default : 0x00**	Access : R/W
	-	7:6	Reserved.	
	DBGMD32	5	Debug mode for 32 bit bus test.	
	DBGMD3D	4	Debug mode for 3D. 0: Normal. 1: Use motion factor as Y.	
	-	3:0	Reserved.	
4Dh	**REG4D**	**7:0**	**Default : 0x00**	Access : R/W
	DBGPATTERN[7:0]	7:0	Debug pattern for 32-bit bus test.	
4Eh	**REG4E**	**7:0**	**Default : 0x00**	Access : R/W
	-	7:6	Reserved.	
	PIPDBGHST[1:0]	5:4	Motion factor pipeline control.	
	PIPCHKHST[3:0]	3:0	Motion history pipeline control.	
4Fh	**REG4F**	**7:0**	**Default : 0x00**	Access : R/W
	-	7:5	Reserved.	
	3DBLUR_GAIN[4:0]	4:0	3D blur gain (1~1/16).	
50h	**REG50**	**7:0**	**Default : 0x07**	Access : R/W

COMB Register (Bank = 36)

Index	Mnemonic	Bit	Description	
	DBG_2DCOMB_YCETP_SEL[1:0]	7:6	Selection of (ENTROPYH/EH4/EH2) / (ENTROPYV/EV2/EV1) / (ENTROPYV-H/SW_GAIN/CDET_SWGAIN) with d[5:4] = 2'd1/2'd2/2'd3.	
	DBG_2DCOMB_ENTROPY[1:0]	5:4	00: Normal. 01: Entropy H. 10: Entropy V. 11: Entropy V - Entropy H.	
	AUTOSTOPSYNC	3	Automatic stop H/V sync when no input.	
	LNFREEMD[2:0]	2:0	Line buffer free run mode. 000: Off (always synchronize). 001: 909 return. 010: 910 return. 011: 917 return. 100: 1127 return. 101: 1135 return. 110: Decided by register. 111: Automatic.	
51h	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
52h	**REG52**	7:0	Default : 0x8E	Access : R/W
	HRETPOS[7:0]	7:0	Horizontal return position in line buffer free run mode.	
53h	**REG53**	7:0	Default : 0x03	Access : R/W
	-	7:3	Reserved.	
	HRETPOS[10:8]	2:0	Please see description of 52h.	
54h	**REG54**	7:0	Default : 0x02	Access : R/W
	TILTTLRN[7:0]	7:0	Line position tilt tolerance.	
55h	**REG55**	7:0	Default : 0x04	Access : R/W
	JITTLRN3D[7:0]	7:0	3D timing detection tolerance.	
56h	**REG56**	7:0	Default : 0x40	Access : R/W
	LCKSTEP[7:0]	7:0	3D lock counter go back distance when sync unstable.	
57h	**REG57**	7:0	Default : 0x68	Access : R/W
	LCK3DTHU[7:0]	7:0	3D timing detection threshold.	
58h	**REG58**	7:0	Default : 0x40	Access : R/W
	LCK3DTHL[7:0]	7:0	3D timing detection threshold.	
59h	**REG59**	7:0	Default : 0x08	Access : R/W

COMB Register (Bank = 36)

Index	Mnemonic	Bit	Description	
	JITTLRN1[7:0]	7:0	Tolerance of HSYNC jitter.	
5Ah	REG5A	7:0	Default : 0x20	Access : R/W
	JITTLRN2[7:0]	7:0	Tolerance of HSYNC jitter.	
5Bh	REG5B	7:0	Default : 0x10	Access : R/W
	HSLCKTHU[7:0]	7:0	Upper bound threshold of hysteresis HSYNC lock counter.	
5Ch	REG5C	7:0	Default : 0x08	Access : R/W
	HSLCKTHL[7:0]	7:0	Lower bound threshold of hysteresis HSYNC lock counter.	
5Dh	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
5Eh	REG5E	7:0	Default : 0x14	Access : R/W
	SYNCDLY[7:0]	7:0	HSYNC (from decoder to scaler) pipe delay.	
5Fh	REG5F	7:0	Default : 0x80	Access : R/W
	HSLDCNTMD[1:0]	7:6	H-sync lead counter mode.	
	CNTSTEPMD[1:0]	5:4	Counter step mode.	
	-	3:0	Reserved.	
60h	REG60	7:0	Default : 0x00	Access : R/W
	IFMD[1:0]	7:6	IF compensation mode.	
	IFCOEF[5:0]	5:0	IF compensation coefficient, 2-bit integer, 4-bit frac.	
61h ~ 63h	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
64h	REG64	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	SAWCMP2D_EN	0	SAW compensation 2D enable.	
65h ~ 6Bh	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
6Ch	REG6C	7:0	Default : 0x00	Access : R/W
	ACC_MD	7	ACC mode selection.	
	-	6:4	Reserved.	
	CBINV	3	Cb inverse for S-video.	
	CRINV	2	Cr inverse for S-video.	
	-	1:0	Reserved.	
6Dh ~	-	7:0	Default : -	Access : -

COMB Register (Bank = 36)

Index	Mnemonic	Bit	Description	
6Fh	-	7:0	Reserved.	
70h	**REG70**	**7:0**	**Default : 0xF0**	**Access : R/W**
	-	7:6	Reserved.	
	CGMD[1:0]	5:4	Auto chroma gain mode. 00: Off. 01: Auto. 10: Manu. 11: MCU control.	
	BRSTFRAFEC	3	Burst height from AFEC.	
	-	2	Reserved.	
	DBG_GAIN_SEL[1:0]	1:0	Debug gain selection.	
71h	**REG71**	**7:0**	**Default : 0x0A**	**Access : R/W**
	SAWCMPDETEN	7	SAW compensation detection enable.	
	-	6:0	Reserved.	
72h	**REG72**	**7:0**	**Default : 0x00**	**Access : R/W**
	BSTHGHT[7:0]	7:0	Burst height for auto chroma gain. 0: Auto, 112 for NTSC and 117 for PAL. Other: Use REGBSTHGHT/DETBSTHGHT as C gain.	
73h	**REG73**	**7:0**	**Default : 0x80**	**Access : R/W**
	CTST[7:0]	7:0	Contrast adjustment coefficient.	
74h	**REG74**	**7:0**	**Default : 0x80**	**Access : R/W**
	BRHT[7:0]	7:0	Brightness adjustment coefficient.	
75h	**REG75**	**7:0**	**Default : 0x80**	**Access : R/W**
	SAT[7:0]	7:0	Saturation adjustment coefficient.	
76h ~ 77h	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
78h	**REG78**	**7:0**	**Default : 0x80**	**Access : R/W**
	CRMAGAIN[7:0]	7:0	Chroma gain value for manual chroma gain.	
79h	**REG79**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CRMAGAIN[13:8]	5:0	Please see description of 79h.	
7Ah ~ 7Ch	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
7Dh	**REG7D**	**7:0**	**Default : 0x80**	**Access : R/W**
	SNOWDLY[7:0]	7:0	Latency of snow output after signal missing.	

COMB Register (Bank = 36)

Index	Mnemonic	Bit	Description	
7Eh	**REG7E**	**7:0**	**Default : 0x00**	**Access : R/W**
	ACC_CRMAGAIN_INC[2:0]	7:5	Chroma gain step of ACC.	
	ACCUPONLY	4	ACC up only.	
	ACCDLY[3:0]	3:0	ACC latency.	
7Fh	**REG7F**	**7:0**	**Default : 0xFF**	**Access : R/W**
	ACCMAXGAIN[7:0]	7:0	ACC maximum gain.	
80h	**REG80**	**7:0**	**Default : 0xC8**	**Access : R/W**
	YGAIN[7:0]	7:0	Luma gain for U/V demodulation.	
81h	**REG81**	**7:0**	**Default : 0x96**	**Access : R/W**
	CBGAIN[7:0]	7:0	Cb gain for U/V demodulation.	
82h	**REG82**	**7:0**	**Default : 0x6A**	**Access : R/W**
	CRGAIN[7:0]	7:0	Cr gain for U/V demodulation.	
83h	**REG83**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:6	Reserved.	
	CTIMD[1:0]	5:4	CTI mode. 00: Off. 01: Weak. 10: Normal. 11: Strong.	
	-	3:2	Reserved.	
	CBCRLPMD[1:0]	1:0	Cb/Cr low pass mode. 00: Off. 01: Weak. 10: Normal. 11: Strong.	
84h	**REG84**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CTSTDITHEN	6	Dithering when contrast adjustment.	
	CTSTDITHPOS[1:0]	5:4	Dithering position (offset) of contrast.	
	-	3	Reserved.	
	SATDITHEN	2	Dithering when saturation adjustment.	
	SATDITHPOS[1:0]	1:0	Dithering position (offset) of saturation.	
85h	**REG85**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	YDEMDITHEN	6	Dithering when demodulation Y gain.	

COMB Register (Bank = 36)

Index	Mnemonic	Bit	Description	
	YDEMDITHPOS[1:0]	5:4	Dithering position (offset) of Y gain.	
	-	3	Reserved.	
	CDEMDITHEN	2	Dithering when demodulation C gain.	
	CDEMDITHPOS[1:0]	1:0	Dithering position (offset) of C gain.	
86h ~ 8Ch	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
8Dh	**REG8D**	**7:0**	**Default : 0x00**	**Access : R/W**
	COMBCTRL[7:0]	7:0	Some control signals for FPGA.	
8Eh	**REG8E**	**7:0**	**Default : 0xE0**	**Access : R/W**
	FPGACTRL[7:0]	7:0	Some control signals for FPGA.	
8Fh	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
90h	**REG90**	**7:0**	**Default : 0x13**	**Access : R/W**
	-	7:6	Reserved.	
	YDETV_PATCH_EN	3	YDET patch V enable.	
	MBS_V_HDIFF_EN	2	Jeff H MBS-C enable. 0: 1,0,2,0,1. 1: 2,0,0,0,-2.	
	MIN_YDETH_EN	1	Minimum YDETH mode enable. 0: Normal. 1: Min (2tap,3tap).	
	NEW_YDET_EN	0	CVBS low pass YDET enable.	
91h	**REG91**	**7:0**	**Default : 0x12**	**Access : R/W**
	YDIFFV1_LUMA_ENG_GAIN[1:0]	7:6	YDET V Luma gain (div 1/2/4/8).	
	YDIFFV1_CRMA_ENG_GAIN[1:0]	5:4	YDET V Chroma gain (div 1/2/4/8).	
	YDIFFH2_LUMA_ENG_GAIN[1:0]	3:2	YDET H Luma gain (div 1/2/4/8).	
	YDIFFH2_CRMA_ENG_GAIN[1:0]	1:0	YDET H Chroma gain (div 1/2/4/8).	
92h	**REG92**	**7:0**	**Default : 0x51**	**Access : R/W**
	DET_FILTER_MD_H_B[1:0]	7:6	PAL H DET filter mode B. 00: LPF[1,2,-1]. 01~10: Reserved. 11: BPF[1,-1].	
	-	5	Reserved.	
	PAL_MBS_TAP_MD_H_B	4	PAL H multi-burst tap B. 0: 2 tap.	

COMB Register (Bank = 36)

Index	Mnemonic	Bit	Description	
			1: 3 tap. Note: If we set [0], DET_FILTER_MD MUST set [11].	
	-	3	Reserved.	
	DET_FILTER_MD_H_A[1:0]	2:1	PAL H DET filter mode A. 00: LPF[1,2,-1]. 01~10: Reserved. 11: BPF[1,-1].	
	PAL_MBS_TAP_MD_H_A	0	PAL H multi-burst tap A. 0: 2 tap. 1: 3 tap. Note: If we set [0], DET_FILTER_MD must set as "11".	
93h	**REG93**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	DET_FILTER_MD_V[1:0]	2:1	PAL V DET filter mode. 0: 2 tap mode: 2,0,-2/0,2,-2. 1: 3 tap mode: 1,1,-2/0,2,-2.	
	PAL_MBS_TAP_MD_V	0	PAL V multi-burst tap. 0: 2 tap. 1: 3 tap.	
94h	**REG94**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB_GAIN_H[3:0]	7:4	YDET patch H multi-burst gain (multiply 1~16).	
	C_GAIN_H[1:0]	3:2	YDET patch H Chroma gain (divide 2, 4, 8, 16).	
	ENG_SCALE[1:0]	1:0	YDET patch multi-burst-Chroma energy scale (multiply 4/8/16/32).	
95h	**REG95**	**7:0**	**Default : 0xCC**	**Access : R/W**
	CDET_V_LUMA_ENG_GAIN[1:0]	7:6	CDET V Luma gain (multiply 1/2/4/8).	
	CDET_V_CRMA_ENG_GAIN[1:0]	5:4	CDET V Chroma gain (multiply 1/2/4/8).	
	CDET_H_LUMA_ENG_GAIN[1:0]	3:2	CDET H Luma gain (multiply 1/2/4/8).	
	CDET_H_CRMA_ENG_GAIN[1:0]	1:0	CDET H Chroma gain (multiply 1/2/4/8).	
96h	**REG96**	**7:0**	**Default : 0x00**	**Access : R/W**
	CDET_SWITCH_THR[7:0]	7:0	CDET switch threshold.	
97h	**REG97**	**7:0**	**Default : 0x00**	**Access : R/W**
	CDET_SWITCH_STEP[1:0]	7:6	CDET switch step (multiply 1/2/4/8).	
	-	5:0	Reserved.	
98h	**REG98**	**7:0**	**Default : 0x2A**	**Access : R/W**

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Index	Mnemonic	Bit	Description	
	PAL_2DCNCH_MD[1:0]	7:6	PAL Chroma 2D 9x5 mode. 00: V12221. 01:14641. 1x: 01210.	
	PAL_DIFFV2_SEL	5	CVDiff V2 select for PAL. 0: Blend (max2, DiffUD). 1: Max (max2, DiffUD).	
	LPF_FACTOR[4:0]	4:0	CVBS low pass blending factor.	
99h	**REG99**	**7:0**	**Default : 0x01**	**Access : R/W**
	CVH2PATCH_EN	7	SC's diagonal patch enable (NTSC443 only).	
	CVDIFF_H2_GAIN[2:0]	6:4	SC's diagonal patch gain (multiply 1/0.5/0.25/0.125//0.0625/0.03125/2/4).	
	PAL_DIFFV1_SEL	3	PAL CVDIFF v1 select. 0: Ian v1. 1: Jeff v1.	
	PAL_CVDIFF_V2_GAIN[2:0]	2:0	CVDIFF v2 gain for PAL (multiply 0/1/2/4/8/0.5/0.25/0.125).	
9Ah	**REG9A**	**7:0**	**Default : 0x03**	**Access : R/W**
	AMPV1_GAIN[3:0]	7:4	AMP_YDIFF_V1 gain (div 8/16/24/32/40/48/56/64/80/96/112/128/160/192/224/256).	
	AMPH2_GAIN[3:0]	3:0	AMP_YDIFF_H2 gain (div 8/16/24/32/40/48/56/64/80/96/112/128/160/192/224/256).	
9Bh	**REG9B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CHROMA_ADPBLD_SEL	4	Chroma fix select for adaptive Chroma blending. 0: Original. 1: 12221Fix.	
	YDETHBND_TH[2:0]	3:1	YDET H bound TH by Reg.	
	YDETHBND_EN	0	YDET H bound enable by Reg.	
9Ch	**REG9C**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7	Reserved..	
	V5DBG_EN	6	Entropy V5 debug mode enable (use V2).	
	V5FLT_SEL	5	Entropy V5 filter select. 0: Max. 1: LP12221.	

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Index	Mnemonic	Bit	Description
	PALETPV_SEL	4	PAL entropy V select. 0: Original. 1: Entropy V5.
	ETP_H2GAIN[1:0]	3:2	Entropy H2 gain (multiply 1/2/4/8).
	PALV1_EN	1	Disable PAL V1 calculation in PAL (for PAL use only).
	H2V1_EN	0	H2 v1 enable. 0: Disable. 1: Enable.
9Dh	REG9D	7:0	Default : 0x08	Access : R/W
	EV2_PROCFLT_SEL[1:0]	7:6	Entropy V2 proc filter select. 00: Original. 01: LP121 (NTSC only). 10: M_MAXMIN. 11: LP12221 M_CVDIFFV2.
	-	5	Reserved.
	EH4_PROCFLT_SEL	4	Entropy H4 proc filter select. 0: Original. 1: LP12221.
	EV1_POSTFLT_SEL	3	Entropy V1 post filter select. 0: Original. 1: LP121.
	EV1_PROCFLT_SEL	2	Entropy V1 proc filter select. 0: Original. 1: Min/Max.
	EH2_POSTFLT_SEL	1	Entropy H2 post filter select. 0: Max. 1: LP12221.
	EH2_PROCFLT_SEL	0	Entropy H2 proc filter select. 0: Original. 1: Min/Max.
9Eh	REG9E	7:0	Default : 0xC1	Access : R/W
	IAN_MAXEH4_GAIN[1:0]	7:6	T-cross patch H4 gain (1/2/4/8).
	IAN_MAXEH2_GAIN[1:0]	5:4	T-cross patch H2 gain (1/2/4/8).
	-	3:1	Reserved.
	IAN_EV_EN	0	T-cross patch V enable.
9Fh	REG9F	7:0	Default : 0x01	Access : R/W
	-	7:5	Reserved.

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Index	Mnemonic	Bit	Description	
	SAWBLENDDIV[4:0]	4:0	SAW blend division.	
A0h	REGA0	7:0	Default : 0x48	Access : R/W
	ADP9X5_CSWEN	7	Adaptive 9X5 use CDET switch gain enable.	
	ADPGAIN_SCUP_EN	6	Adaptive 9x5 scale up enable.	
	REFER_3X3LRDIFF_EN	5	Adaptive 9x5 reference adaptive 3x3 difference enable (for LR Diff).	
	REFER_H4_EN	4	Adaptive 3x3 reference adaptive 9x5 difference enable (for LR Diff).	
	ADPCRMA_SEL	3	Adaptive Chroma select. 0: 14641. 1: 12221).	
	ADPLUMA_SEL	2	Adaptive Luma select. 0: 14641. 1: 12221.	
	ADP2DSEL[1:0]	1:0	Adaptive mode (9x5/9x3/3x5/3x3).	
A1h	REGA1	7:0	Default : 0x00	Access : R/W
	ADPGAINLR1P[3:0]	7:4	Adp3x3 gain lookup LR table.	
	ADPGAINLR0P[3:0]	3:0	Adp3x3 gain lookup LR table.	
A2h	REGA2	7:0	Default : 0x21	Access : R/W
	ADPGAINLR3P[3:0]	7:4	Adp3x3 gain lookup LR table.	
	ADPGAINLR2P[3:0]	3:0	Adp3x3 gain lookup LR table.	
A3h	REGA3	7:0	Default : 0x84	Access : R/W
	ADPGAINLR5P[3:0]	7:4	Adp3x3 gain lookup LR table.	
	ADPGAINLR4P[3:0]	3:0	Adp3x3 gain lookup LR table.	
A4h	REGA4	7:0	Default : 0xEC	Access : R/W
	ADPGAINLR7P[3:0]	7:4	Adp3x3 gain lookup LR table.	
	ADPGAINLR6P[3:0]	3:0	Adp3x3 gain lookup LR table.	
A5h	REGA5	7:0	Default : 0x0F	Access : R/W
	ADPGAINLR9P[3:0]	7:4	Adp3x3 gain lookup LR table.	
	ADPGAINLR8P[3:0]	3:0	Adp3x3 gain lookup LR table.	
A6h	REGA6	7:0	Default : 0x60	Access : R/W
	-	7	Reserved.	
	ADPGAINLR8TOAP[2:0]	6:4	Adp3x3 gain lookup LR table (Sign Bit), 8~AP[4].	
	ADPGAINLRAP[3:0]	3:0	Adp3x3 gain lookup LR table.	
A7h	REGA7	7:0	Default : 0x00	Access : R/W

COMB Register (Bank = 36)

Index	Mnemonic	Bit	Description	
	ADPGAINLR0TO7P[7:0]	7:0	Adp3x3 gain lookup LR table (Sign Bit), 0~7P[4].	
A8h	**REGA8**	**7:0**	**Default : 0x00**	Access : R/W
	ADPGAINUD1P[3:0]	7:4	Adp3x3 gain lookup UD table.	
	ADPGAINUD0P[3:0]	3:0	Adp3x3 gain lookup UD table.	
A9h	**REGA9**	**7:0**	**Default : 0x21**	Access : R/W
	ADPGAINUD3P[3:0]	7:4	Adp3x3 gain lookup UD table.	
	ADPGAINUD2P[3:0]	3:0	Adp3x3 gain lookup UD table.	
AAh	**REGAA**	**7:0**	**Default : 0x84**	Access : R/W
	ADPGAINUD5P[3:0]	7:4	Adp3x3 gain lookup UD table.	
	ADPGAINUD4P[3:0]	3:0	Adp3x3 gain lookup UD table.	
ABh	**REGAB**	**7:0**	**Default : 0xEC**	Access : R/W
	ADPGAINUD7P[3:0]	7:4	Adp3x3 gain lookup UD table.	
	ADPGAINUD6P[3:0]	3:0	Adp3x3 gain lookup UD table.	
ACh	**REGAC**	**7:0**	**Default : 0x0F**	Access : R/W
	ADPGAINUD9P[3:0]	7:4	Adp3x3 gain lookup UD table.	
	ADPGAINUD8P[3:0]	3:0	Adp3x3 gain lookup UD table.	
ADh	**REGAD**	**7:0**	**Default : 0x00**	Access : R/W
	-	7	Reserved.	
	ADPGAINUD8TOAP[2:0]	6:4	Adp3x3 gain lookup UD table (sign bit), 8~AP[4].	
	ADPGAINUDAP[3:0]	3:0	Adp3x3 gain lookup UD table.	
AEh	**REGAE**	**7:0**	**Default : 0x00**	Access : R/W
	ADPGAINUD0TO7P[7:0]	7:0	Adp3x3 gain lookup UD table (sign bit), 0~7P[4].	
B0h	**REGB0**	**7:0**	**Default : 0x00**	Access : R/W
	-	7:3	Reserved.	
	ADP9X5_DBGSEL[2:0]	2:0	Adaptive 9x5 debug output select.	
B1h	**REGB1**	**7:0**	**Default : 0x00**	Access : R/W
	-	7:6	Reserved.	
	ADP9X5GAIN0[5:0]	5:0	Adp9x5 gain lookup table (0~32) <=> (-16~16).	
B2h	**REGB2**	**7:0**	**Default : 0x00**	Access : R/W
	-	7:6	Reserved.	
	ADP9X5GAIN1[5:0]	5:0	Adp9x5 gain lookup table (0~32) <=> (-16~16).	
B3h	**REGB3**	**7:0**	**Default : 0x00**	Access : R/W
	-	7:6	Reserved.	
	ADP9X5GAIN2[5:0]	5:0	Adp9x5 gain lookup table (0~32) <=> (-16~16).	

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Index	Mnemonic	Bit	Description	
B4h	**REGB4**	**7:0**	**Default : 0x0C**	**Access : R/W**
	-	7:6	Reserved.	
	ADP9X5GAIN3[5:0]	5:0	Adp9x5 gain lookup table (0~32) <=> (-16~16).	
B5h	**REGB5**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:6	Reserved.	
	ADP9X5GAIN4[5:0]	5:0	Adp9x5 gain lookup table (0~32) <=> (-16~16).	
B6h	**REGB6**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	ADP9X5GAIN5[5:0]	5:0	Adp9x5 gain lookup table (0~32) <=> (-16~16).	
B7h	**REGB7**	**7:0**	**Default : 0x11**	**Access : R/W**
	-	7:6	Reserved.	
	ADP9X5GAIN6[5:0]	5:0	Adp9x5 gain lookup table (0~32) <=> (-16~16).	
B8h	**REGB8**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:6	Reserved.	
	ADP9X5GAIN7[5:0]	5:0	Adp9x5 gain lookup table (0~32) <=> (-16~16).	
B9h	**REGB9**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	ADP9X5GAIN8[5:0]	5:0	Adp9x5 gain lookup table (0~32) <=> (-16~16).	
BAh	**REGBA**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	ADP9X5GAIN9[5:0]	5:0	Adp9x5 gain lookup table (0~32) <=> (-16~16).	
BBh	**REGBB**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	ADP9X5GAINA[5:0]	5:0	Adp9x5 gain lookup table (0~32) <=> (-16~16).	
C0h	**REGC0**	**7:0**	**Default : 0xA0**	**Access : R/W**
	CRMA2D_SEL[1:0]	7:6	Chroma 2D Select (5x5/5x5/ADP/DEMBLD).	
	LUMA2D_SEL[1:0]	5:4	Luma 2D Select (5x5/5x5/ADP/adaptive).	
	CRMAOUT_MD[1:0]	3:2	Chroma output mode. 00: Normal. 01: 1DH. 10: 1DV. 11: 2D.	
	LUMAOUT_MD[1:0]	1:0	Luma output mode. 00: Normal. 01: 1DH.	

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Index	Mnemonic	Bit	Description	
			10: 1DV.	
			11: 2D.	
C1h	REGC1	7:0	Default : 0x33	Access : R/W
	YETPV_GAIN[3:0]	7:4	Luma Entropy gain V for lookup table (multiply (1~16)/4).	
	YETPH_GAIN[3:0]	3:0	Luma Entropy gain H for lookup table (multiply (1~16)/4).	
C2h	REGC2	7:0	Default : 0x33	Access : R/W
	CETPV_GAIN[3:0]	7:4	Chroma entropy gain V for lookup table (multiply (1~16)/4).	
	CETPH_GAIN[3:0]	3:0	Chroma Entropy gain H for lookup table (multiply (1~16)/4).	
C3h	REGC3	7:0	Default : 0x1F	Access : R/W
	-	7:5	Reserved.	
	AUTO2D_EN	4	When it is unknown TV system, force 2D output enable.	
	CETP_SCDN_EN	3	Chroma entropy scaled down enable.	
	CETP_SCUP_EN	2	Chroma entropy scaled up enable.	
	YETP_SCDN_EN	1	Luma entropy scaled down enable.	
	YETP_SCUP_EN	0	Luma entropy scaled up enable.	
C4h (3688h)	REG3688	7:0	Default : 0x00	Access : R/W
	YBLD_FORCE_SW_GAIN[3:0]	7:4	Luma blending forced switch gain (0~128).	
	-	3:1	Reserved.	
	YBLD_FORCE_SW	0	Luma blending forced switch enable.	
C5h	REGC5	7:0	Default : 0x00	Access : R/W
	CROSSPT_EN	7	Cross point patch enable.	
	-	6	Reserved.	
	CROSSPT_DEBUG[1:0]	5:4	Cross point patch debug mode.	
	CROSSPOINT_CSHIFT[1:0]	3:2	Cross point C shift.	
	CMBRATIO_A[1:0]	1:0	Cross point patch, Chroma multi-burst ratio A.	
C6h	REGC6	7:0	Default : 0x20	Access : R/W
	YGAINYH1P[3:0]	7:4	Luma gain lookup table YH.	
	YGAINYH0P[3:0]	3:0	Luma gain lookup table YH.	
C7h	REGC7	7:0	Default : 0x85	Access : R/W
	YGAINYH3P[3:0]	7:4	Luma gain lookup table YH.	

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Index	Mnemonic	Bit	Description	
	YGAINYH2P[3:0]	3:0	Luma gain lookup table YH.	
C8h	REGC8	7:0	Default : 0x88	Access : R/W
	YGAINYH5P[3:0]	7:4	Luma gain lookup table YH.	
	YGAINYH4P[3:0]	3:0	Luma gain lookup table YH.	
C9h	REGC9	7:0	Default : 0x88	Access : R/W
	YGAINYH7P[3:0]	7:4	Luma gain lookup table YH.	
	YGAINYH6P[3:0]	3:0	Luma gain lookup table YH.	
CAh	REGCA	7:0	Default : 0x20	Access : R/W
	YGAINYV1P[3:0]	7:4	Luma gain lookup table YV.	
	YGAINYV0P[3:0]	3:0	Luma gain lookup table YV.	
CBh	REGCB	7:0	Default : 0x85	Access : R/W
	YGAINYV3P[3:0]	7:4	Luma gain lookup table YV.	
	YGAINYV2P[3:0]	3:0	Luma gain lookup table YV.	
CCh	REGCC	7:0	Default : 0x88	Access : R/W
	YGAINYV5P[3:0]	7:4	Luma gain lookup table YV.	
	YGAINYV4P[3:0]	3:0	Luma gain lookup table YV.	
CDh	REGCD	7:0	Default : 0x88	Access : R/W
	YGAINYV7P[3:0]	7:4	Luma gain lookup table YV.	
	YGAINYV6P[3:0]	3:0	Luma gain lookup table YV.	
CEh	REGCE	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	CMPSEL[3:0]	3:0	CMP selection.	
CFh	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
D0h	REGD0	7:0	Default : 0xB9	Access : R/W
	PEAKING_PALCMP_INV	7	Peaking PALCMP inverse.	
	IAN_ENH_CLIP[2:0]	6:4	Clipping TH (0/16/32/64/96/128/160/192).	
	IAN_ENH_CORING[1:0]	3:2	Coring TH (0/4/8/16).	
	NTSC_PEAKING_SEL	1	NTSC peaking method select. 0: Ian mode. 1: X mode.	
	IAN_ENH_PEAKING_EN	0	Ian enhanced peaking enable.	
D1h	REGD1	7:0	Default : 0x40	Access : R/W
	IAN_ENH_Y1GAIN[7:0]	7:0	Y1 gain (div(16~128) >>3).	

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Index	Mnemonic	Bit	Description	
D2h	REGD2	7:0	Default : 0x40	Access : R/W
	IAN_ENH_Y2GAIN[7:0]	7:0	Y2 gain (div(16~128) >>3).	
D3h	REGD3	7:0	Default : 0x60	Access : R/W
	IAN_ENH_Y3GAIN[7:0]	7:0	Y3 gain (div(16~128) >>3).	
D4h	REGD4	7:0	Default : 0x20	Access : R/W
	IAN_MIN_CDIFFH[7:0]	7:0	Peaking minimum C difference horizontal.	
D5h	REGD5	7:0	Default : 0x08	Access : R/W
	IAN_MIN_CDIFFV[7:0]	7:0	Peaking minimum C difference vertical.	
D6h	REGD6	7:0	Default : 0x0A	Access : R/W
	-	7:4	Reserved.	
	IAN_CDIFFV_RANGE[1:0]	3:2	Peaking C difference vertical range (16/32/64/128).	
	IAN_CDIFFH_RANGE[1:0]	1:0	Peaking C difference horizontal range (16/32/64/128).	
DAh	REGDA	7:0	Default : 0x01	Access : R/W
	DBG_FP_MD[3:0]	7:4	Final patch debug mode. [3]: Debug enable (1). [2:1]: VDiff(0)/HDiff(1)/Gain(2). [0]: Up(0)/Down(1).	
	-	3:1	Reserved.	
	FINALPATCH_EN	0	Ian final patch enable.	
DBh	REGDB	7:0	Default : 0x42	Access : R/W
	-	7	Reserved.	
	IAN_PLHDIFF_SC[2:0]	6:4	Ian pure Luma H-diff scale select (multiply 0/0.125/0.25/0.5/1/2/4/8).	
	-	3	Reserved.	
	IAN_PLHDIFF_TH[2:0]	2:0	Ian pure Luma H-diff threshold select (32/64/128/256).	
DCh	REGDC	7:0	Default : 0x00	Access : R/W
	IAN_DIFF_SHIFTD[1:0]	7:6	Ian pure Luma D diff shift (div 4/8/16/32) after TH (8~=32 inC).	
	IAN_DIFF_SHIFTU[1:0]	5:4	Ian pure Luma U diff shift (div 4/8/16/32) after TH (8~=32 inC).	
	IAN_DIFF_MSHTD[1:0]	3:2	Ian pure Luma D diff shift (div 1/2/4/8) before TH.	
	IAN_DIFF_MSHTU[1:0]	1:0	Ian pure Luma U diff shift (div 1/2/4/8) before TH.	
DDh	REGDD	7:0	Default : 0x00	Access : R/W
	IAN_TH_VER[7:0]	7:0	Ian pure Luma TH_VER (25): U/D diff threshold for	

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Index	Mnemonic	Bit	Description	
			detection.	
DEh	REGDE	7:0	Default : 0x05	Access : R/W
	PLHDIFF_TH[7:0]	7:0	Pure Luma H difference threshold.	
E0h	REGE0	7:0	Default : -	Access : RO
	HSLOCK	7	HSYNC lock happen.	
	LOCK3D	6	Good timing happen.	
	MEMRDBWEVN	5	Memory read bandwidth not enough.	
	MEMWRBWEVN	4	Memory write bandwidth not enough.	
	NOTHSLOCK	3	HSYNC unlock happen.	
	NOTLOCK3D	2	Good timing disappear.	
	HSCHG	1	HSYNC counter change.	
	MEMBWEVN	0	DRAM bandwidth not enough.	
E1h	REGE1	7:0	Default : -	Access : RO
	STLIMG	7	Still image happen.	
	NOTSTLIMG	6	Still image disappear.	
	CCHNLACT	5	C-channel active (maybe S-video input).	
	NOTCCHNLACT	4	C-channel quiet (maybe CVBS input).	
	-	3	Reserved.	
	FLDCNTCHG	2	Field counter change.	
	-	1:0	Reserved.	
E2h	REGE2	7:0	Default : -	Access : RO
	LN525	7	525 line system.	
	LN625	6	625 line system.	
	F358	5	3.58 MHz system.	
	F443	4	4.43 MHz system.	
	NOINPUT	3	No input.	
	VDOMD[2:0]	2:0	Video mode.	
			0: NTSC_M.	
			1: NTSC_443.	
			2: PAL_M.	
			3: PAL_BDGHIN.	
			4: PAL_NC.	
			5: PAL_60.	
			6: Input without burst.	
			7: Unknown.	

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Index	Mnemonic	Bit	Description	
E3h	**REGE3**	**7:0**	**Default : -**	**Access : RO**
	IRQ_FINAL_STS[1:0]	7:6	Raw IRQ status.	
	IRQ_RAW_STS[1:0]	5:4	Final IRQ status.	
	-	3:1	Reserved.	
	INTERLACE	0	Interlace input.	
E4h	**REGE4**	**7:0**	**Default : -**	**Access : RO**
	DETBLANK[7:0]	7:0	Detected blank level.	
E5h	**REGE5**	**7:0**	**Default : -**	**Access : RO**
	CURBLANK[7:0]	7:0	Current used blank level.	
E6h	**REGE6**	**7:0**	**Default : -**	**Access : RO**
	SYNCLVL[7:0]	7:0	Detected sync level.	
E7h	**REGE7**	**7:0**	**Default : -**	**Access : RO**
	SYNCHGHT[7:0]	7:0	Detected sync height.	
E8h	**REGE8**	**7:0**	**Default : -**	**Access : RO**
	BURSTHGHT[7:0]	7:0	Detected burst height.	
E9h	**REGE9**	**7:0**	**Default : -**	**Access : RO**
	DETHORTOTAL[7:0]	7:0	Detected horizontal total.	
EAh	**REGEA**	**7:0**	**Default : -**	**Access : RO**
	DETHORTOTAL[15:8]	7:0	Please see description of '36D2h'.	
EBh	**REGEB**	**7:0**	**Default : -**	**Access : RO**
	RPTCOVFH[7:0]	7:0	Reported chroma overflow count per line.	
ECh	**REGEC**	**7:0**	**Default : -**	**Access : RO**
	RPTCOVFV[7:0]	7:0	Reported chroma overflow count per field.	
EDh ~ FFh	-	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	

VBI Register (Bank = 37)

VBI Register (Bank = 37)				
Index	**Mnemonic**	**Bit**	**Description**	
40h	REG40	7:0	Default : 0x21	Access : R/W
	CRIAMPTHDL_9_8	7:6	Closed caption clock run-in amplitude L (upper 2 bits).	
	CCLNSTR1_4_3	5:4	Closed caption line start 1 (upper 2 bits).	
	CRIDETENNUM_10_8	3:1	Closed caption clock run-in detection enable number (upper 3 bits).	
	SLCTHDMD	0	Closed caption slicer threshold mode.	
41h	REG41	7:0	Default : 0x52	Access : R/W
	CCLNSTR1_2_0	7:5	Closed caption line start 1 (lower 3 bits).	
	CCLNEND1	4:0	Closed caption line end 1.	
42h	REG42	7:0	Default : 0x1C	Access : R/W
	CCINTTYPE	7	Closed caption interrupt type. 0: Assert 8T after CC line in even field if CC is found. 1: According to CCREQ.	
	-	6:0	Reserved.	
43h	REG43	7:0	Default : 0xA8	Access : R/W
	CRIDETENNUM_7_0	7:0	Closed caption clock run-un detection enable number (lower 8 bits).	
44h	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
45h	REG45	7:0	Default : 0xA0	Access : R/W
	CRIAMPTHDL_7_0	7:0	Closed caption clock run-in amplitude L (lower 8 bits).	
46h	REG46	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	CCFRAMTRIGNUM_4_0	5:1	Closed caption frame trigger number. This controls CCFRAMTRIG (VBI_IRQ_STS[3]). When CCFRAMCNT == CCFRAMTRIGNUM, CCFRAMTRIG would be asserted.	
	CCEN	0	Closed caption enable.	
47h ~ 4Eh	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
4Fh	REG4F	7:0	Default : 0xF8	Access : R/W
	CRIAMPTHDH_7_0	7:0	Closed caption clock run-in amplitude upper threshold (lower 8 bits).	
50h	REG50	7:0	Default : 0x72	Access : R/W

VBI Register (Bank = 37)

Index	Mnemonic	Bit	Description	
	CRIAMPTHDH_9_8	7:6	Closed caption clock run-in amplitude upper threshold (upper 2 bits).	
	CCCRIZCTYPE	5	Closed caption CRI zero crossing type. 1: positive edge ; 0: negative edge.	
	CCLNSTR2	4:0	Closed caption line start 2.	
51h	**REG51**	**7:0**	**Default : 0xB2**	**Access : R/W**
	-	7:5	Reserved.	
	CCLNEND2	4:0	Closed caption line end 2.	
52h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
53h	**REG53**	**7:0**	**Default : 0x90**	**Access : R/W**
	CCSCWINLEN	7:0	Closed caption start code checking window length.	
54h	**REG54**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:6	Reserved.	
	CCSTRCODEMSK	5:3	Closed caption start code mask. 1: mask(ignore) ; 0: normal.	
	CCSTRCODE	2:0	Closed caption start code.	
55h	**REG55**	**7:0**	**Default : -**	**Access : RO**
	-	7:2	Reserved.	
	CCBYTEERRH	1	Closed caption byte error (upper part).	
	CCBYTEERRL	0	Closed caption byte error (lower part).	
56h	**REG56**	**7:0**	**Default : -**	**Access : RO**
	CCODDFOUND	7	Closed caption odd byte found indication.	
	CCEVEFOUND	6	Closed cation even byte found indication.	
	-	5	Reserved.	
	CCFRAMCNT	4:0	Closed caption frame counter.	
57h	**REG57**	**7:0**	**Default : -**	**Access : RO**
	CCBYTES_7_0	7:0	Closed caption bytes (lower 8 bits).	
58h	**REG58**	**7:0**	**Default : -**	**Access : RO**
	CCBYTES_15_8	7:0	Closed caption bytes (upper 8 bits).	
5Bh	**REG5B**	**7:0**	**Default : -**	**Access : RO**
	CC_PACKET_COUNTER	7:0	Closed caption packet counter.	
5Ch	REG5C	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7	Reserved.	

VBI Register (Bank = 37)

Index	Mnemonic	Bit	Description	
	CCBUFLEN	6:0	Closed caption buffer length.	
5Dh	REG5D	7:0	Default : 0xFF	Access : R/W
	CCBASEADDR_23_16	7:0	Closed caption base address (upper 8 bits).	
5Eh	REG5E	7:0	Default : 0xFF	Access : R/W
	CCBASEADDR_15_8	7:0	Closed caption base address (middle 8 bits).	
5Fh	REG5F	7:0	Default : 0xFF	Access : R/W
	CCBASEADDR_7_0	7:0	Closed caption base address (lower 8 bits).	
68h ~	-	7:0	Default : -	Access : -
FFh	-	7:0	-	

SECAM Register (Bank = 38)

SECAM Register (Bank = 38)				
Index	**Mnemonic**	**Bit**	**Description**	
01h	REG01	7:0	Default : 0x00	Access : R/W
	SCM_RST	7	SECAM software reset. 0: Normal operation. 1: Reset.	
	MIXC_EN	6	Chroma mixing enable. 0: Disable. 1: Enable according to settings of WFUNC_ISO and YDEV_THRSD.	
	WFUNC_ISO	5	Chroma weighting function isolation. 0: Normal. 1: Isolate asymmetric weighting.	
	SCM_RES_OP	4	SCM_RESULT report option. 0: Immediate. 1: During VBI.	
	-	3	Reserved.	
	ID_MD	2	Identification mode selection. Set to 1 only if using frame ID for SECAM detection in line 7~15 and line 320~328.	
	SCMID_OP	1	SECAM identification option. 0: Identification is on when VD state is stable. 1: Ignore VD state stable condition.	
	SCMID_EN	0	SECAM identification forced enable.	
02h	REG02	7:0	Default : 0x98	Access : R/W
	SAMPLE_ST0_7_0	7:0	Start of sample point (lower 8 bits) for 4.43 MHz.	
03h	REG03	7:0	Default : 0xA4	Access : R/W
	SAMPLE_END0_7_0	7:0	End of sample point (lower 8 bits) for 4.43 MHz.	
04h	REG04	7:0	Default : 0x1B	Access : R/W
	LINE_STA	7:0	Start of line number of odd field.	
05h	REG05	7:0	Default : 0x54	Access : R/W
	LINE_STB_7_0	7:0	Start of line number of even field.	
06h	REG06	7:0	Default : 0x01	Access : R/W
	SAMPLE_ST0_10_8	7:5	Start of sample point (upper 3 bits) for 4.43MHz.	
	SAMPLE_END0_10_8	4:2	End of sample point (upper 3 bits) for 4.43MHz.	
	LINE_STB_9_8	1:0	Start of line number of even field (upper 2 bits).	
07h	REG07	7:0	Default : 0xF0	Access : R/W

SECAM Register (Bank = 38)

Index	Mnemonic	Bit	Description	
	LINE_LEN0	7:0	Length of observation line for 4.43MHz.	
08h	REG08	7:0	Default : 0x01	Access : R/W
	SCM_Y2Y601_BP	7	SECAM Y (Luma) to BT601 operation bypassing option.	
	MAG_MD	6:5	00: Original value. 01: MAG_INT/2. 10: MAG_INT/8. 11: MAG/32.	
	ID_CTR_MD	4:3	SECAM identification criterion mode. 00: Depend on magnitude difference. 01: Depend on magnitude and sign difference. 10: Depend on magnitude difference and sign flipping. 11: Depend on magnitude difference, sign difference, and sign flipping.	
	ID_ACT_FIELD	2:0	Active field number of SECAM identification.	
09h	REG09	7:0	Default : 0x60	Access : R/W
	MAG_THRSD44_7_0	7:0	Magnitude threshold for Fsc 4.43MHz (lower 8 bits).	
0Ah	REG0A	7:0	Default : 0x21	Access : R/W
	MAG_THRSD44_15_8	7:0	Magnitude threshold for Fsc 4.43MHz (middle 8 bits).	
0Bh	REG0B	7:0	Default : 0x40	Access : R/W
	-	7	Reserved.	
	LINE_PIXNUM_10_8	6:4	Pixel number of line buffer (upper 3 bits).	
	MAG_THRSD44_19_16	3:0	Magnitude threshold for Fsc 4.43MHz (upper 4 bits).	
0Ch	REG0C	7:0	Default : 0x48	Access : R/W
	LINE_PIXNUM_7_0	7:0	Pixel number of line buffer (if the number is 1097, program 11'h448).	
0Dh	REG0D	7:0	Default : 0x06	Access : R/W
	ID_THRSD	7:0	Threshold for SECAM identification.	
0Eh	REG0E	7:0	Default : 0x88	Access : R/W
	NONSCM_THRSD	7:4	Non-SECAM decision threshold.	
	SCM_THRSD	3:0	SECAM decision threshold.	
0Fh	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
10h	REG10	7:0	Default : 0x00	Access : R/W
	MAG_THRSD42_7_0	7:0	Magnitude threshold for Fsc 4.285MHz (lower 8 bits).	

SECAM Register (Bank = 38)

Index	Mnemonic	Bit	Description	
11h	**REG11**	7:0	Default : 0x20	Access : R/W
	MAG_THRSD42_15_8	7:0	Magnitude threshold for Fsc 4.285MHz (middle 8 bits).	
12h	**REG12**	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	MAG_THRSD42_19_16	3:0	Magnitude threshold for Fsc 4.285MHz (upper 4 bits).	
13h	**REG13**	7:0	Default : 0x08	Access : R/W
	MAG_DEV_THRSD_7_0	7:0	Magnitude deviation threshold for SECAM color-off detection (unsigned lower 8 bits).	
14h	**REG14**	7:0	Default : 0x00	Access : R/W
	MAG_DEV_THRSD_15_8	7:0	Magnitude deviation threshold for SECAM color-off detection (unsigned upper 8 bits).	
15h	**REG15**	7:0	Default : 0xFF	Access : R/W
	HW_SCM_COFF_EN	7	Hardware SECAM color-off enable. 0: Disable ; 1: Enable.	
	SCM_COFF_THRSD	6:0	Hardware SECAM color-off threshold (2 lines / unit).	
16h ~ 18h	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
19h	**REG19**	7:0	Default : 0x03	Access : R/W
	SCM_BPYN	7	Bypass Y (Luma) notch filter option. 0: Normal mode. 1: Bypass mode.	
	OBV_MD	6	Observation mode. 0: Field base. 1: Within one field.	
	-	5:4	Reserved.	
	SCMGCLK_OP	3	SECAM clock gating option. 0: Gate SECAM clock when operating at 3.58MHZ(or not stable VD state). 1: No clock gating.	
	CMBGCLK_OP	2	Comb clock gating option. 0: No clock gating. 1: Gate comb filter clock when SECAM decoder is operating.	

SECAM Register (Bank = 38)

Index	Mnemonic	Bit	Description	
	CLPMD[1:0]	1:0	Chroma LPF mode. 00: Bypass. 01: 1.5 MHz. 10: 1.25 MHz. 11: 1 MHz.	
1Ah ~ 1Dh	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
1Eh	**REG1E**	7:0	Default : 0x04	Access : R/W
	SCM_YSEP_FLTMD	7:6	Y separation filter selection. 00: Normal. 01: Medium. 10: Strong. 11: Reserved.	
	-	5	Reserved.	
	SCM_CBCRLPON	4	SECAM Cb/Cr LPF switch. 0: Off. 1: On.	
	LUMAFIXMD	3	Luma Fix Mode. 0: Normal. 1: Luma is controlled by SDBK level.	
	SCM_YDLYMD	2:0	SECAN Luma(Y) delay mode. 0: advance 4 ; 1: advance 3 ; 2: advance 2 ; 3: advance 1 ; 4: normal ; 5: delay 1 ; 6: delay 2 ; 7: delay 3.	
1Fh	**REG1F**	7:0	Default : 0x30	Access : RO, R/W
	SCM_IRQ_FORCE	7:6	SECAM Interrupt force bits.	
	SCM_IRQ_MSK	5:4	SECAM Interrupt mask bits.	
	SCM_IRQ_CLR	3:2	SECAM Interrupt clear bits.	
	SCM_IRQ_STS	1:0	SECAM Interrupt status bits.	
20h	**REG20**	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	SCMINTTYPE	3	SECAM interrupt type. 0: Issue when SECAM ID result changes. 1: Issue when detection related data updates.	
	-	2:0	Reserved.	
21h ~ 24h	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
25h	**REG25**	7:0	Default : 0x00	Access : R/W

SECAM Register (Bank = 38)

Index	Mnemonic	Bit	Description	
	-	7	Reserved.	
	SCM_IFMD	6:4	SECAM IF Compensation Filter Mode.	
	-	3:0	Reserved.	
26h	**REG26**	**7:0**	**Default : 0xFC**	**Access : R/W**
	SDBKLEVEL_7_0	7:0	Static de-blanking level (lower 8 bits).	
27h	**REG27**	**7:0**	**Default : 0x04**	**Access : R/W**
	SCMBLANKSTR	7:0	Start point of blank period.	
28h	**REG28**	**7:0**	**Default : 0x6C**	**Access : R/W**
	SCMBLANKEND	7:0	End point of blank period.	
29h	**REG29**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	SIGN_FLIP_THRSD_11_8	3:0	Frequency deviation sign flipping threshold for detection (upper 4 bits).	
2Ah	**REG2A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SIGN_FLIP_THRSD_7_0	7:0	Frequency deviation sign flipping threshold for detection (lower 8 bits).	
2Bh	**REG2B**	**7:0**	**Default : 0x5F**	**Access : R/W**
	VDE_SCTL_11_8	7:4	Saturation bound value control after de-emphasis filter (upper 4 bits).	
	DCAL_SCTL_11_8	3:0	Saturation bound value control before de-emphasis filter (upper 4 bits).	
2Ch	**REG2C**	**7:0**	**Default : 0x3A**	**Access : R/W**
	DCAL_SCTL_7_0	7:0	Saturation bound value control before de-emphasis filter (lower 8 bits).	
2Dh	**REG2D**	**7:0**	**Default : 0x54**	**Access : R/W**
	VDE_SCTL_7_0	7:0	Saturation bound value control after de-emphasis filter (lower 8 bits).	
2Eh	**REG2E**	**7:0**	**Default : 0x06**	**Access : R/W**
	TRIG_LINE_NUM_7_0	7:0	Trigger line number for generating interrupt (lower 8 bits).	
2Fh	**REG2F**	**7:0**	**Default : 0x80**	**Access : R/W**
	SCM_CGAINMD	7	SECAM chroma gain register mode. 0: Controlled by DSP. 1: Controlled by 2Fh[6:5].	

SECAM Register (Bank = 38)

Index	Mnemonic	Bit	Description	
	SCM_CGAINREG	6:5	SECAM chroma gain. 01: x2. 10: x4. Others: x1.	
	-	4:2	Reserved.	
	TRIG_LINE_NUM_9_8	1:0	Trigger line number for generating interrupt (upper 2 bits).	
30h	**REG30**	**7:0**	**Default : -**	**Access : RO**
	SCMID_DONE	7	SECAM identification done indication.	
	SCMID_YES	6	SECAM signal found bit.	
	DR_LINE	5	Dr line indication.	
	DB_LINE	4	Db line indication.	
	INTB	3	Line type indication.	
	SCMID_STS	2:0	SECAM ID status. 000: Idle. 001/010/011: ID progress. 110: SECAM. 111: No SECAM signal discovery.	
31h ~ 35h	-	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
36h	**REG36**	**7:0**	**Default : -**	**Access : RO**
	-	7:5	Reserved.	
	HW_SCM_COFF	4	Hardware SECAM color-off indication.	
	-	3:2	Reserved.	
	SCM_FSC	1:0	Fsc status from AFEC_TOP. 00: NTSC 3.58MHz. 01: PAL 4.43MHz. 10: SECAM 4.285156MHz. 11: Reserved.	
38h ~ 3Bh	-	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	

SAR Register (Bank = 3A)

SAR Register (Bank = 3A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (3A00h)	**REG3A00**	**7:0**	**Default : 0x00**	**Access : R/W**
	SAR_START	7	SAR start.	
	SAR_PD	6	1: Power down SAR ADC.	
	SAR_MODE	5	Select SAR ADC operation mode. 0: One-shot. 1: Free-run.	
	SINGLE	4	1: Enable single channel mode.	
	-	3	Reserved.	
	KEYPAD_LEVEL	2	Keypad level.	
	SAR_SINGLE_CH[1:0]	1:0	Select channel for single channel mode.	
01h (3A02h)	**REG3A02**	**7:0**	**Default : 0x00**	**Access : R/W**
	CKSAMP_PRD[7:0]	7:0	Sampling period.	
04h (3A08h)	**REG3A08**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SAR_CH1_UPB[5:0]	5:0	The upper limit of keypad wake-up for CH1 SAR ADC.	
05h (3A0Ah)	**REG3A0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SAR_CH1_LOB[5:0]	5:0	The lower limit of keypad wake-up for CH1 SAR ADC.	
06h (3A0Ch)	**REG3A0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SAR_CH2_UPB[5:0]	5:0	The upper limit of keypad wake-up for CH2 SAR ADC.	
07h (3A0Eh)	**REG3A0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SAR_CH2_LOB[5:0]	5:0	The lower limit of keypad wake-up for CH2 SAR ADC.	
08h (3A10h)	**REG3A10**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SAR_CH3_UPB[5:0]	5:0	The upper limit of keypad wake-up for CH3 SAR ADC.	
09h (3A12h)	**REG3A12**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SAR_CH3_LOB[5:0]	5:0	The lower limit of keypad wake-up for CH3 SAR ADC.	
0Ah (3A14h)	**REG3A14**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	

SAR Register (Bank = 3A)

Index (Absolute)	Mnemonic	Bit	Description	
	SAR_CH4_UPB[5:0]	5:0	The upper limit of keypad wake-up for CH4 SAR ADC.	
0Bh (3A16h)	REG3A16	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	SAR_CH4_LOB[5:0]	5:0	The lower limit of keypad wake-up for CH4 SAR ADC.	
0Ch (3A18h)	REG3A18	7:0	Default : -	Access : RO
	SAR_RDY	7	SAR ADC data ready in one-shot mode.	
	-	6	Reserved.	
	SAR_ADC_CH1_DATA[5:0]	5:0	Digital data output of CH1 SAR ADC.	
0Dh (3A1Ah)	REG3A1A	7:0	Default : -	Access : RO
	-	7:6	Reserved.	
	SAR_ADC_CH2_DATA[5:0]	5:0	Digital data output of CH2 SAR ADC.	
0Eh (3A1Ch)	REG3A1C	7:0	Default : -	Access : RO
	-	7:6	Reserved.	
	SAR_ADC_CH3_DATA[5:0]	5:0	Digital data output of CH3 SAR ADC.	
0Fh (3A1Eh)	REG3A1E	7:0	Default : -	Access : RO
	-	7:6	Reserved.	
	SAR_ADC_CH4_DATA[5:0]	5:0	Digital data output of CH4 SAR ADC.	
10h (3A20h)	REG3A20	7:0	Default : 0xFF	Access : R/W
	OEN_SAR_GPIO[3:0]	7:4	Output enable for GPIO pad. 0: Enable. 1: Disable.	
	SAR_AISEL[3:0]	3:0	Pad GPIO/AIN switch. 1: Analog input. 0: GPIO.	
10h (3A21h)	REG3A21	7:0	Default : 0x00	Access : R/W
	SAR_FREERUN	7	Setup SAR ADC to free-run. 0: Controlled by digital (default). 1: Free-run.	
	SARADC_PD	6	SAR ADC power down. 1: Power down. 0: Enable SAR ADC.	

SAR Register (Bank = 3A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SAR_CHSEL[1:0]	5:4	SAR ADC channel select. 00: Channel 0. 01: Channel 1. 10: Channel 2. 11: Channel 3.	
	I_SAR_GPIO[3:0]	3:0	Output data for GPIO pad.	
11h (3A22h)	**REG3A22**	**7:0**	**Default : 0x00**	**Access : R/W**
	SAR_TEST[7:0]	7:0	SAR ADC test mode control.	
11h (3A23h)	**REG3A23**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SAR_TEST[9:8]	1:0	Please see description of '3A22h'.	
12h (3A24h)	**REG3A24**	**7:0**	**Default : -**	**Access : RO**
	-	7:4	Reserved.	
	C_SAR_GPIO[3:0]	3:0	Input data for GPIO pad.	
13h (3A26h)	**REG3A26**	**7:0**	**Default : 0x01**	**Access : RO, R/W**
	-	7:4	Reserved.	
	SAR_INT_STATUS	3	Status of SAR_INT.	
	SAR_INT_FORCE	2	Force interrupt for SAR_INT.	
	SAR_INT_CLR	1	Interrupt clear for SAR_INT.	
	SAR_INT_MASK	0	Interrupt mask for SAR_INT. 0: Enable. 1: Disable.	

PIU_MISC Register (Bank = 3C)

PIU_MISC Register (Bank = 3C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h ~ 0Fh (3C00h ~ 3C1Fh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
10h (3C20h)	REG3C20	7:0	Default : 0x00	Access : RO, R/W
	CRC_DUM_10[4:0]	7:3	Bit 0 is used as DST_SEL_VDMCU.	
	DMA_BUSY	2	DMA Busy (RO).	
	DMA_DONE	1	DMA Done (RO).	
	CRC_DUM_10_BIT0	0	CRC_DUM_10_BIT0	
10h (3C21h)	REG3C21	7:0	Default : -	Access : RO
	DMA_STATE[7:0]	7:0	DMA_STATE[7:0]	
11h ~ 1Fh (3C22h ~ 3C3Fh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
20h (3C40h)	REG3C40	7:0	Default : 0x11	Access : R/W
	CSZ_SETUP[3:0]	7:4	Number of cycles between SPI_CSZ falling to first SPI_SCK.	
	CSZ_HOLD[3:0]	3:0	Number of cycles between last SPI_SCK to SPI_CSZ rise.	
20h (3C41h)	REG3C41	7:0	Default : 0x01	Access : R/W
	FAST	7	Fast mode.	
	DUAL	6	Winbond dual mode (not supported yet).	
	QUAD	5	Winbond quad mode (not supported yet).	
	-	4	Reserved.	
	CSZ_HIGH[3:0]	3:0	Number of cycles when SPI_CSZ=high.	
21h (3C42h)	REG3C42	7:0	Default : -	Access : RO
	SPI_1ST_ADDR[7:0]	7:0	Debug: 1st request address.	
21h (3C43h)	REG3C43	7:0	Default : -	Access : RO
	SPI_1ST_ADDR[15:8]	7:0	Please see description of '3C42h'.	
22h (3C44h)	REG3C44	7:0	Default : -	Access : RO
	SPI_1ST_ADDR[23:16]	7:0	Please see description of '3C42h'.	
22h (3C45h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
23h	REG3C46	7:0	Default : -	Access : RO

PIU_MISC Register (Bank = 3C)

Index (Absolute)	Mnemonic	Bit	Description	
(3C46h)	SPI_2ND_ADDR[7:0]	7:0	Debug: 2nd request address.	
23h (3C47h)	**REG3C47**	**7:0**	**Default : -**	**Access : RO**
	SPI_2ND_ADDR[15:8]	7:0	Please see description of '3C46h'.	
24h (3C48h)	**REG3C48**	**7:0**	**Default : -**	**Access : RO**
	SPI_2ND_ADDR[23:16]	7:0	Please see description of '3C46h'.	
24h (3C49h)	-	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
25h (3C4Ah)	**REG3C4A**	**7:0**	**Default : -**	**Access : RO**
	-	7:2	Reserved.	
	SPI_ADDR_CHANGE	1	Debug: request again when SPI is in busy mode.	
	SPI_OVERRUN	0	Debug: consecutive request with no ACK.	
25h ~ 2Fh (3C4Bh~ 3C5Fh)	-	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
30h (3C60h)	**REG3C60**	**7:0**	**Default : 0xAA**	**Access : R/W**
	WDT_KEY[7:0]	7:0	Enable: WDT_KEY != 0xAA55.	
30h (3C61h)	**REG3C61**	**7:0**	**Default : 0x55**	**Access : R/W**
	WDT_KEY[15:8]	7:0	Please see description of '3C60h'.	
31h (3C62h)	**REG3C62**	**7:0**	**Default : 0x00**	**Access : R/W**
	WDT_SEL[7:0]	7:0	WatchDog interval 65536*(65536-wdt_sel) cycles.	
31h (3C63h)	**REG3C63**	**7:0**	**Default : 0xFC**	**Access : R/W**
	WDT_SEL[15:8]	7:0	Please see description of '3C62h'.	
32h (3C64h)	**REG3C64**	**7:0**	**Default : 0x00**	**Access : R/W**
	WDT_INT_SEL[7:0]	7:0	When WDT_CNT[31:16] > WDT_INT_SEL, WatchDog interrupt occurs.	
32h (3C65h)	**REG3C65**	**7:0**	**Default : 0xFF**	**Access : R/W**
	WDT_INT_SEL[15:8]	7:0	Please see description of '3C64h'.	
33h (3C66h)	**REG3C66**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	-	7:2	Reserved.	
	WDT_CLR_MCU	1	Clear watchdog.	
	WDT_RST	0	Watchdog reset occurs.	
33h ~ 3Fh (3C67h ~ 3C7Fh)	-	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	

PIU_MISC Register (Bank = 3C)

Index (Absolute)	Mnemonic	Bit	Description	
40h (3C80h)	REG3C80	7:0	Default : 0x00	Access : R/W
	TIMER_MAX_0[7:0]	7:0	When internal counter == TIMER_MAX, interrupt occurs.	
40h (3C81h)	REG3C81	7:0	Default : 0x00	Access : R/W
	TIMER_MAX_0[15:8]	7:0	Please see description of '3C80h'.	
41h (3C82h)	REG3C82	7:0	Default : 0x00	Access : R/W
	TIMER_MAX_0[23:16]	7:0	Please see description of '3C80h'.	
41h (3C83h)	REG3C83	7:0	Default : 0x00	Access : R/W
	TIMER_MAX_0[31:24]	7:0	Please see description of '3C80h'.	
42h (3C84h)	REG3C84	7:0	Default : -	Access : RO
	TIMER_CNT_CAP_0[7:0]	7:0	Captured counter.	
42h (3C85h)	REG3C85	7:0	Default : -	Access : RO
	TIMER_CNT_CAP_0[15:8]	7:0	Please see description of '3C84h'.	
43h (3C86h)	REG3C86	7:0	Default : -	Access : RO
	TIMER_CNT_CAP_0[23:16]	7:0	Please see description of '3C84h'.	
43h (3C87h)	REG3C87	7:0	Default : -	Access : RO
	TIMER_CNT_CAP_0[31:24]	7:0	Please see description of '3C84h'.	
44h (3C88h)	REG3C88	7:0	Default : 0x00	Access : WO
	-	7:2	Reserved.	
	CLR_0	1	Clear internal counter.	
	CAPTURE_0	0	Capture internal counter.	
44h (3C89h)	REG3C89	7:0	Default : 0x00	Access : R/W
	TIMER_CTRL_0[7:0]	7:0	0: Disable. 3: Enable.	
45h ~ 4Fh (3C8Ah ~ 3C9Fh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
50h (3CA0h)	REG3CA0	7:0	Default : 0x00	Access : R/W
	TIMER_MAX_1[7:0]	7:0	When internal counter == TIMER_MAX, interrupt occurs.	
50h (3CA1h)	REG3CA1	7:0	Default : 0x00	Access : R/W
	TIMER_MAX_1[15:8]	7:0	Please see description of '3CA0h'.	
51h (3CA2h)	REG3CA2	7:0	Default : 0x00	Access : R/W
	TIMER_MAX_1[23:16]	7:0	Please see description of '3CA0h'.	

PIU_MISC Register (Bank = 3C)

Index (Absolute)	Mnemonic	Bit	Description	
51h (3CA3h)	REG3CA3	7:0	Default : 0x00	Access : R/W
	TIMER_MAX_1[31:24]	7:0	Please see description of '3CA0h'.	
52h (3CA4h)	REG3CA4	7:0	Default : -	Access : RO
	TIMER_CNT_CAP_1[7:0]	7:0	Captured counter.	
52h (3CA5h)	REG3CA5	7:0	Default : -	Access : RO
	TIMER_CNT_CAP_1[15:8]	7:0	Please see description of '3CA4h'.	
53h (3CA6h)	REG3CA6	7:0	Default : -	Access : RO
	TIMER_CNT_CAP_1[23:16]	7:0	Please see description of '3CA4h'.	
53h (3CA7h)	REG3CA7	7:0	Default : -	Access : RO
	TIMER_CNT_CAP_1[31:24]	7:0	Please see description of '3CA4h'.	
54h (3CA8h)	REG3CA8	7:0	Default : 0x00	Access : WO
	-	7:2	Reserved.	
	CLR_1	1	Clear internal counter.	
	CAPTURE_1	0	Capture internal counter.	
54h (3CA9h)	REG3CA9	7:0	Default : 0x00	Access : R/W
	TIMER_CTRL_1[7:0]	7:0	0: Disable. 3: Enable.	
55h ~ 5Fh (3CAAh ~ 3CBFh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
60h (3CC0h)	REG3CC0	7:0	Default : 0x92	Access : R/W
	ISP_ID[7:0]	7:0	ISP_ID[7:0]	
60h (3CC1h)	REG3CC1	7:0	Default : 0x4D	Access : R/W
	ISP_PWD1[7:0]	7:0	ISP_PWD1[7:0]	
61h (3CC2h)	REG3CC2	7:0	Default : 0x53	Access : R/W
	ISP_PWD2[7:0]	7:0	ISP_PWD2[7:0]	
61h (3CC3h)	REG3CC3	7:0	Default : 0x54	Access : R/W
	ISP_PWD3[7:0]	7:0	ISP_PWD3[7:0]	
62h (3CC4h)	REG3CC4	7:0	Default : 0x41	Access : R/W
	ISP_PWD4[7:0]	7:0	ISP_PWD4[7:0]	
62h (3CC5h)	REG3CC5	7:0	Default : 0x52	Access : R/W
	ISP_PWD5[7:0]	7:0	ISP_PWD5[7:0]	
63h	REG3CC6	7:0	Default : 0x00	Access : R/W

PIU_MISC Register (Bank = 3C)

Index (Absolute)	Mnemonic	Bit	Description	
(3CC6h)	ISP_CTRL0[7:0]	7:0	ISP_CTRL0[7:0]	
63h ~ 6Fh (3CC7h ~ 3CDFh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
70h (3CE0h)	REG3CE0	7:0	Default : 0x00	Access : R/W
	DMA_SRC_ADR_0[7:0]	7:0	DMA_SRC_ADR_0[7:0]	
70h (3CE1h)	REG3CE1	7:0	Default : 0x00	Access : R/W
	DMA_SRC_ADR_0[15:8]	7:0	Please see description of '3CE0h'.	
71h (3CE2h)	REG3CE2	7:0	Default : 0x00	Access : R/W
	DMA_SRC_ADR_1[7:0]	7:0	DMA_SRC_ADR_1[7:0]	
71h (3CE3h)	REG3CE3	7:0	Default : 0x00	Access : R/W
	DMA_SRC_ADR_1[15:8]	7:0	Please see description of '3CE2h'.	
72h (3CE4h)	REG3CE4	7:0	Default : 0x00	Access : R/W
	DMA_DST_ADR_0[7:0]	7:0	DMA_DST_ADR_0[7:0]	
72h (3CE5h)	REG3CE5	7:0	Default : 0x00	Access : R/W
	DMA_DST_ADR_0[15:8]	7:0	Please see description of '3CE4h'.	
73h (3CE6h)	REG3CE6	7:0	Default : 0x00	Access : R/W
	DMA_DST_ADR_1[7:0]	7:0	DMA_DST_ADR_1[7:0]	
73h (3CE7h)	REG3CE7	7:0	Default : 0x00	Access : R/W
	DMA_DST_ADR_1[15:8]	7:0	Please see description of '3CE6h'.	
74h (3CE8h)	REG3CE8	7:0	Default : 0x00	Access : R/W
	DMA_SIZE_0[7:0]	7:0	DMA_SIZE_0[7:0]	
74h (3CE9h)	REG3CE9	7:0	Default : 0x00	Access : R/W
	DMA_SIZE_0[15:8]	7:0	Please see description of '3CE8h'.	
75h (3CEAh)	REG3CEA	7:0	Default : 0x00	Access : R/W
	DMA_SIZE_1[7:0]	7:0	DMA_SIZE_1[7:0]	
75h (3CEBh)	REG3CEB	7:0	Default : 0x00	Access : R/W
	DMA_SIZE_1[15:8]	7:0	Please see description of '3CEAh'.	
76h (3CECh)	REG3CEC	7:0	Default : 0x00	Access : R/W, WO
	DMA_ADDR_INC	7	DMA_ADDR_INC	
	DMA_RIU_MD	6	DMA_RIU_MD	
	DMA_BIG_ENDIAN	5	DMA_BIG_ENDIAN	
	DMA_RIU_NO_DLY	4	DMA_RIU_NO_DLY	

PIU_MISC Register (Bank = 3C)

Index (Absolute)	Mnemonic	Bit	Description	
	DMA_DST_SEL	3	DMA_DST_SEL	
	-	2:1	Reserved.	
	DMA_TRIG	0	DMA trigger (WO).	
76h ~ 7Fh (3CEDh ~ 3CFEh)	REG3CFE	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	TEST_SEL[2:0]	2:0		

DDC/IR Register (Bank = 3D)

Index (Absolute)	Mnemonic	Bit	Description	
00h (3D00h)	REG3D00	7:0	Default : -	Access : RO
	D2B_WBUF_RPORT_A0[7:0]	7:0	DDC2Bi master write buffer, MCU read point of A0.	
00h (3D01h)	REG3D01	7:0	Default : 0x00	Access : R/W
	D2B_RBUF_WPORT_A0[7:0]	7:0	DDC2Bi master read buffer, MCU write point of A0.	
02h (3D04h)	REG3D04	7:0	Default : -	Access : RO
	D2B_WBUF_RPORT_D0[7:0]	7:0	DDC2Bi master write buffer, MCU read point of D0.	
02h (3D05h)	REG3D05	7:0	Default : 0x00	Access : R/W
	D2B_RBUF_WPORT_D0[7:0]	7:0	DDC2Bi master read buffer, MCU write point of D0.	
03h (3D06h)	REG3D06	7:0	Default : -	Access : RO
	D2B_WBUF_RPORT_D1[7:0]	7:0	DDC2Bi master read buffer, MCU write point of D1.	
03h (3D07h)	REG3D07	7:0	Default : 0x00	Access : R/W
	D2B_RBUF_WPORT_D1[7:0]	7:0	DDC2Bi master read buffer, MCU write point of D1.	
04h (3D08h)	REG3D08	7:0	Default : 0x00	Access : WO
	D2B_RBUF_WPORT_PULSE_A0	7	MCU write pulse generate for D2B RBUF_A0.	
	-	6	Reserved.	
	D2B_RBUF_WPORT_PULSE_D0	5	MCU write pulse generate for D2B RBUF_D0.	
	D2B_RBUF_WPORT_PULSE_D1	4	MCU write pulse generate for D2B RBUF_D1.	
	-	3:0	Reserved.	
04h (3D09h)	REG3D09	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	EN_NO_ACK	1	DDC2Bi does not send ACK if data buffer has not been	

DDC/IR Register (Bank = 3D)

Index (Absolute)	Mnemonic	Bit	Description	
			read by CPU. 0: Disable. 1: Enable.	
	-	0	Reserved.	
05h (3D0Ah)	REG3D0A	7:0	Default : 0x00	Access : R/W
	D2B_ID_A0[7]	7	DDC2Bi enable for A0.	
	D2B_ID_A0[6:0]	6:0	DDCBi ID[7:1] for A0.	
06h (3D0Ch)	REG3D0C	7:0	Default : 0x00	Access : R/W
	D2B_ID_D0[7]	7	DDC2Bi Enable for D0.	
	D2B_ID_D0[6:0]	6:0	DDCBi ID[7:1] for D0.	
06h (3D0Dh)	REG3D0D	7:0	Default : 0x00	Access : R/W
	D2B_ID_D1[7]	7	DDC2Bi Enable for D1.	
	D2B_ID_D1[6:0]	6:0	DDCBi ID[7:1] for D1.	
07h (3D0Eh)	REG3D0E	7:0	Default : -	Access : RO
	C_LAT_SRAM_DATA_A0[7:0]	7:0	DDC data read port for ADC SRAM; CPU reads ADC SRAM data.	
07h (3D0Fh)	REG3D0F	7:0	Default : -	Access : RO
	C_LAT_SRAM_DATA_D0[7:0]	7:0	DDC data read port for DVI SRAM; CPU read DVI SRAM data.	
08h (3D10h)	REG3D10	7:0	Default : -	Access : RO
	-	7	Reserved.	
	D2B_INT_FINAL_STS_A0[6]	6	DDC2Bi start interrupt flag.	
	D2B_INT_FINAL_STS_A0[5]	5	DDC2Bi stop interrupt flag.	
	D2B_INT_FINAL_STS_A0[4]	4	DDC2Bi data read interrupt flag (write data into RBUF to clear).	
	D2B_INT_FINAL_STS_A0[3]	3	DDC2Bi data write interrupt flag (read data from WBUF to clear).	
	D2B_INT_FINAL_STS_A0[2]	2	The 8th bit of the ID, interrupt flag. 0: Write. 1: Read (RO, update automatically).	
	D2B_INT_FINAL_STS_A0[1]	1	WADR interrupt flag. 1: The data in WBUF is the 2nd byte (WADR). 0: The data in WBUF is not the 2nd byte (Not WADR).	
	D2B_INT_FINAL_STS_A0[0]	0	DDC2Bi ID interrupt flag.	
09h	REG3D12	7:0	Default : -	Access : RO

DDC/IR Register (Bank = 3D)

Index (Absolute)	Mnemonic	Bit	Description	
(3D12h)	-	7	Reserved.	
	D2B_INT_FINAL_STS_D0[6]	6	DDC2Bi start interrupt flag.	
	D2B_INT_FINAL_STS_D0[5]	5	DDC2Bi stop interrupt flag.	
	D2B_INT_FINAL_STS_D0[4]	4	DDC2Bi data read interrupt flag (write data into RBUF to clear).	
	D2B_INT_FINAL_STS_D0[3]	3	DDC2Bi data write interrupt flag (read data from WBUF to clear).	
	D2B_INT_FINAL_STS_D0[2]	2	The 8th bit of the ID, interrupt flag. 0: Write. 1: Read (RO, update automatically).	
	D2B_INT_FINAL_STS_D0[1]	1	WADR interrupt flag. 1: The data in WBUF is the 2nd byte (WADR). 0: The data in WBUF is not the 2nd byte (not WADR).	
	D2B_INT_FINAL_STS_D0[0]	0	DDC2Bi ID interrupt flag.	
09h (3D13h)	REG3D13	7:0	Default : -	Access : RO
	-	7	Reserved.	
	D2B_INT_FINAL_STS_D1[6]	6	DDC2Bi start interrupt flag.	
	D2B_INT_FINAL_STS_D1[5]	5	DDC2Bi stop interrupt flag.	
	D2B_INT_FINAL_STS_D1[4]	4	DDC2Bi data read interrupt flag (write data into RBUF to clear).	
	D2B_INT_FINAL_STS_D1[3]	3	DDC2Bi data write interrupt flag (read data from WBUF to clear).	
	D2B_INT_FINAL_STS_D1[2]	2	The 8th bit of the ID, interrupt flag. 0: Write. 1: Read (RO, update automatically).	
	D2B_INT_FINAL_STS_D1[1]	1	WADR interrupt flag. 0: The data in WBUF is not the 2nd byte (not WADR). 1: The data in WBUF is the 2nd byte (WADR).	
	D2B_INT_FINAL_STS_D1[0]	0	DDC2Bi ID interrupt flag.	
0Ah (3D14h)	REG3D14	7:0	Default : 0x06	Access : R/W
	-	7	Reserved.	
	D2B_INT_MSK_A0[6]	6	DDC2Bi start interrupt mask.	
	D2B_INT_MSK_A0[5]	5	DDC2Bi stop interrupt mask.	
	D2B_INT_MSK_A0[4]	4	DDC2Bi data read interrupt mask (write data into RBUF to clear).	

DDC/IR Register (Bank = 3D)

Index (Absolute)	Mnemonic	Bit	Description	
	D2B_INT_MSK_A0[3]	3	DDC2Bi data write interrupt mask (read data from WBUF to clear).	
	D2B_INT_MSK_A0[2]	2	The 8th bit of the ID, interrupt mask. 0: Write. 1: Read (RO, update automatically).	
	D2B_INT_MSK_A0[1]	1	WADR interrupt mask. 0: The data in WBUF is not the 2nd byte (not WADR). 1: The data in WBUF is the 2nd byte (WADR).	
	D2B_INT_MSK_A0[0]	0	DDC2Bi ID interrupt flag.	
0Bh (3D16h)	**REG3D16**	7:0	**Default : 0x06**	**Access : R/W**
	-	7	Reserved.	
	D2B_INT_MSK_D0[6]	6:0	DDC2Bi start interrupt flag. [2] The 8th bit of the ID, interrupt mask 0: Write. 1: Read (RO, update automatically). [1] WADR interrupt mask 0: The data in WBUF is not the 2nd byte(Not WADR). 1: The data in WBUF is the 2nd byte.(WADR). [0] DDC2Bi ID interrupt flag.	
	D2B_INT_MSK_D0[5]	5	DDC2Bi stop interrupt flag.	
	D2B_INT_MSK_D0[4]	4	DDC2Bi data read interrupt mask (write data into RBUF to clear).	
	D2B_INT_MSK_D0[3]	3	DDC2Bi data write interrupt flag (read data from WBUF to clear).	
	D2B_INT_MSK_D0[2]	2	The 8th bit of the ID, interrupt flag. 0: Write. 1: Read (RO, update automatically).	
	D2B_INT_MSK_D0[1]	1	WADR interrupt flag. 1: The data in WBUF is the 2nd byte (WADR). 0: The data in WBUF is not the 2nd byte (not WADR).	
	D2B_INT_MSK_D0[0]	0	DDC2Bi ID interrupt flag.	
0Bh (3D17h)	**REG3D17**	7:0	**Default : 0x06**	**Access : R/W**
	-	7	Reserved.	
	D2B_INT_MSK_D1[6]	6	DDC2Bi start interrupt flag.	
	D2B_INT_MSK_D1[5]	5	DDC2Bi stop interrupt flag.	
	D2B_INT_MSK_D1[4]	4	DDC2Bi data read interrupt flag (write data into RBUF	

DDC/IR Register (Bank = 3D)

Index (Absolute)	Mnemonic	Bit	Description	
			to clear).	
	D2B_INT_MSK_D1[3]	3	DDC2Bi data write interrupt flag (read data from WBUF to clear).	
	D2B_INT_MSK_D1[2]	2	The 8th bit of the ID, interrupt mask. 0: Write. 1: Read (RO, update automatically).	
	D2B_INT_MSK_D1[1]	1	WADR interrupt mask. 0: The data in WBUF is not the 2nd byte (not WADR). 1: The data in WBUF is the 2nd byte (WADR).	
	D2B_INT_MSK_D1[0]	0	DDC2Bi ID interrupt flag.	
0Ch (3D18h)	REG3D18	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	D2B_INT_FORCE_A0[6:0]	6:0	Force the D2B_INT_FINAL_STS_A0 to 1 by setting each of the related bit to 1.	
0Dh (3D1Ah)	REG3D1A	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	D2B_INT_FORCE_D0[6:0]	6:0	Force the D2B_INT_FINAL_STS_D0 to 1 by setting each of the related bit to 1	
0Dh (3D1Bh)	REG3D1B	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	D2B_INT_FORCE_D1[6:0]	6:0	Force the D2B_INT_FINAL_STS_D1 to 1 by setting each of the related bit to 1.	
0Eh (3D1Ch)	REG3D1C	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	D2B_INT_CLR_A0[6:0]	6:0	Clear the D2B_INT_FINAL_STS_A0 to 0 by setting each of the related bit to 1.	
0Fh (3D1Eh)	REG3D1E	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	D2B_INT_CLR_D0[6:0]	6:0	Clear the D2B_INT_FINAL_STS_D0 to 0 by setting each of the related bit to 1.	
0Fh (3D1Fh)	REG3D1F	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	D2B_INT_CLR_D1[6:0]	6:0	Clear the D2B_INT_FINAL_STS_D1 to 0 by setting each of the related bit to 1.	
21h	REG3D42	7:0	Default : 0x00	Access : WO

DDC/IR Register (Bank = 3D)

Index (Absolute)	Mnemonic	Bit	Description	
(3D42h)	D0_CLR_DIRTY	7	Clear dirty bit for DVI_0 (clear pulse generate). 0: Not clear. 1: Clear.	
	A0_CLR_DIRTY	6	Clear dirty bit for ADC_0 (clear pulse generate). 0: Not clear. 1: Clear.	
	D1_CLR_DIRTY	5	Clear dirty bit for DVI_1 (clear pulse generate). 0: Not clear. 1: Clear.	
	-	4:0	Reserved.	
21h (3D43h)	REG3D43	7:0	Default : 0x00	Access : R/W, WO
	EN_WDATA_CLK_D0	7	DVI SRAM write data pulse gen when CPU write. 0: Not gen pulse. 1: Gen pulse.	
	CPURRQ_ST_0_D0	6	DVI SRAM read pulse gen when CPU read. 0: Not gen pulse. 1: Gen pulse.	
	EN_WDATA_CLK_A0	5	ADC SRAM write data pulse gen when CPU write. 0: Not gen pulse. 1: Gen pulse.	
	CPURRQ_ST_0_A0	4	ADC SRAM read pulse gen when CPU read. 0: Not gen pulse. 1: Gen pulse.	
	-	3:2	Reserved.	
	D0_EN_READ	1	DDC SRAM read/write enable for DVI SRAM. 0: Write. 1: Read.	
	-	0	Reserved.	
22h (3D44h)	REG3D44	7:0	Default : 0x00	Access : RO, R/W, WO
	CHK_SUM_OK	7	DDC check Sum.(256Bytes) (Read Only). 0: Not OK. 1: OK.	
	CHK1ST_SUM_OK	6	DDC check sum1 (128Bytes) (Read Only). 0: Not OK. 1: OK.	
	MASTER_FINISH	5	DDC master function finish (Read Only). 0: Not finish.	

DDC/IR Register (Bank = 3D)

Index (Absolute)	Mnemonic	Bit	Description	
			1: Finish.	
	MASTER_OK	4	Master OK (write 128 bytes with acknowledgement received) (Read Only). 0: Not OK. 1: OK.	
	F128_DVI	3	First 128 bytes send to DVI (second 128 send to ADC). 0: Is DVI. 1: Is ADC.	
	SEL_256	2	Master moves from EEPROM. 0: 128 bytes. 1: 256 bytes.	
	MASTER_EN	1	Master disable/enable. 0: Disable. 1: Enable.	
	MASTER_START	0	Soft master stop/start trigger. 0: Stop. 1: Start.	
22h (3D45h)	**REG3D45**	7:0	**Default : 0x00**	**Access : RO, R/W**
	D0_DDC_EN	7	DDC function enable for DVI_0. 0: Disable. 1: Enable.	
	FILTER_ON	6	DDC filter. 0: Disable. 1: Enable.	
	D0_DDCW_PROTECT	5	DDC I2C bus write protect for DVI_0 port. 0: Not protected. 1: Protected.	
	BYPASS_DDC	4	Bypass DDC. 0: Disable. 1: Enable.	
	BYPASS_SEL_DVI	3	Bypass select DVI 0: ADC. 1: DVI.	
	D0_DDC_BUSY	2	DDC busy for DVI_0 (Read Only). 0: Not busy. 1: Busy.	
	D0_LAST_RW	1	DDC last read/write STS for DVI_0 (Read Only).	

DDC/IR Register (Bank = 3D)

Index (Absolute)	Mnemonic	Bit	Description	
			0: Write. 1: Read.	
	D0_DIRTY_BIT	0	DDC SRAM dirty STS for DVI_0 (Read Only). 0: Not dirty. 1: Dirty.	
23h (3D46h)	**REG3D46**	7:0	**Default : 0x00**	**Access : RO, R/W**
	FILTER_MSB	7	DDC filter MSB.	
	D0_LAST_ADR[6:0]	6:0	DDC last R/W address for DVI_0.	
23h (3D47h)	**REG3D47**	7:0	**Default : 0x00**	**Access : R/W**
	D0_CPU_ADR[7:0]	7:0	DDC address port for CPU read/write for DVI_0.	
24h (3D48h)	**REG3D48**	7:0	**Default : 0x00**	**Access : R/W**
	D0_CPU_WDATA[7:0]	7:0	DDC data port for CPU write for DVI_0.	
24h (3D49h)	**REG3D49**	7:0	**Default : 0x00**	**Access : RO, R/W**
	A0_DDC_EN	7	DDC function enable for ADC_0. 0: Disable. 1: Enable.	
	-	6	Reserved.	
	A0_DDCW_PROTECT	5	DDC I2C bus write protect for ADC_0 port. 0: Not protected. 1: Protected.	
	SLEW_SEL[1:0]	4:3	Slew rate control. 00: Bypass. 01: Drive 1 cycle. 10: Drive 2 cycles. 11: Drive 3 cycles.	
	A0_DDC_BUSY	2	DDC busy for ADC_0 (Read Only). 0: Not busy. 1: Busy.	
	A0_LAST_RW	1	DDC last read/write STS for ADC_0 (Read Only). 0: Write. 1: Read.	
	A0_DIRTY_BIT	0	DDC SRAM dirty STS for ADC_0 (Read Only). 0: Not dirty. 1: Dirty.	
25h (3D4Ah)	REG3D4A	7:0	**Default : 0x80**	**Access : RO, R/W**
	-	7	Reserved.	

DDC/IR Register (Bank = 3D)

Index (Absolute)	Mnemonic	Bit	Description	
	A0_LAST_ADR[6:0]	6:0	DDC last R/W address for ADC_0 (Read Only).	
25h (3D4Bh)	**REG3D4B**	**7:0**	**Default : 0x00**	**Access : R/W**
	A0_EN_READ	7	DDC SRAM read/write enable for ADC SRAM. 0: Write. 1: Read.	
	A0_CPU_ADR[6:0]	6:0	DDC address port for CPU read/write for ADC_0.	
26h (3D4Ch)	**REG3D4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	A0_CPU_WDATA[7:0]	7:0	DDC data port for CPU write for ADC_0.	
26h (3D4Dh)	**REG3D4D**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	D1_DDC_EN	7	DDC function enable for DVI_1. 0: Disable. 1: Enable.	
	-	6	Reserved.	
	D1_DDCW_PROTECT	5	DDC I2C bus write protect for DVI_1 port. 0: Not protected. 1: Protected.	
	-	4:3	Reserved.	
	D1_DDC_BUSY	2	DDC busy STS for DVI_1 (Read Only). 0: Not busy. 1: Busy.	
	D1_LAST_RW	1	DDC last read/write STS for DVI_1 (Read Only). 0: Write. 1: Read.	
	D1_DIRTY_BIT	0	DDC SRAM dirty STS for DVI_1 (Read Only). 0: Not dirty. 1: Dirty.	
27h (3D4Eh)	**REG3D4E**	**7:0**	**Default : -**	**Access : RO**
	-	7	Reserved.	
	D1_LAST_ADR[6:0]	6:0	DDC last R/W address for DVI_1 (Read Only).	
30h (3D60h)	**REG3D60**	**7:0**	**Default : 0x80**	**Access : R/W**
	HDMI_256_EN	7	HDMI SRAM 256 enable (allow DVI SRAM256x8 instead of SRAM128x8).	
	BYPASS_SEL_0	6	DDC bypass source port selection. If BYP_SEL_DVI==1, 0: Choose D1. 1: Choose D0.	

DDC/IR Register (Bank = 3D)

Index (Absolute)	Mnemonic	Bit	Description	
	-	5:0	Reserved.	
3Ah (3D74h)	REG3D74	7:0	Default : 0x22	Access : RO, R/W
	-	7:6	Reserved.	
	HDCP_EN	5	HDCP enable for DDC. 0: Disable. 1: Enable.	
	-	4:3	Reserved.	
	HDCP_MA_FINISH	2	HDCP master finish (Read Only).	
	ENWRITE_HDCP	1	Enable CPU write (for HDCP SRAM/74reg). 0: Disable. 1: Enable.	
	HDCP_SRAM_ACCESS	0	HDCP SRAM access enable (1 for CPU; 0 for 74reg access). 0: Access HDCP 74reg. 1: Access HDCP SRAM.	
3Bh (3D76h)	REG3D76	7:0	Default : 0x00	Access : R/W
	CPU_ADR_REG[7:0]	7:0	CPU R/W address (for HDCP_KEY_SRAM/74reg).	
3Bh (3D77h)	REG3D77	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	CPU_ADR_REG[9:8]	1:0	Please see description of '3D76h'.	
3Ch (3D78h)	REG3D78	7:0	Default : 0x00	Access : R/W
	CPU_WDATA_REG[7:0]	7:0	CPU write data port (for HDCP_KEY_SRAM/74reg).	
3Ch (3D79h)	REG3D79	7:0	Default : -	Access : RO
	HDCP_DATA_PORT_RD[7:0]	7:0	HDCP read data port (for HDCP_KEY_SRAM/74reg).	
3Dh (3D7Ah)	REG3D7A	7:0	Default : 0x00	Access : WO
	-	7:3	Reserved.	
	LOAD_ADR_P	2	HDCP address load pulse generate. 0: Not gen pulse. 1: Gen pulse.	
	HDCP_DATA_WR_P	1	HDCP data write port pulse generate. 0: Not gen pulse. 1: Gen pulse.	
	HDCP_DATA_RD_P	0	HDCP data read port pulse generate. 0: Not gen pulse. 1: Gen pulse.	

DDC/IR Register (Bank = 3D)

Index (Absolute)	Mnemonic	Bit	Description	
3Dh (3D7Bh)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
3Eh (3D7Ch)	REG3D7C	7:0	Default : 0x80	Access : R/W
	RSTZ_SW_DDC	7	Software resets for DDC (low active).	
	-	6:0	Reserved.	
3Eh ~ 3Fh (3D7Dh ~ 3D7F)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
40h (3D80h)	REG3D80	7:0	Default : 0x00	Access : R/W
	IR_INV	7	Invert the polarity for input IR signal.	
	IR_INT_MSK	6	IR interrupt request mask for MCU.	
	IR_RPCODE_EN	5	IR repeat code check enable.	
	IR_LG01H_CHK_EN	4	IR logic 0/1 high level edge check enable.	
	IR_DCODE_PCHK_EN	3	IR data code parity check enable.	
	IR_CCODE_CHK_EN	2	IR customer code check enable.	
	IR_LDCCHK_EN	1	IR leader code (header + off code) check enable.	
	IR_EN	0	IR decode enable for full/raw mode.	
40h (3D81h)	REG3D81	7:0	Default : 0x00	Access : R/W
	IR_INT_CRC_MSK	7	Interrupt mask for IR CRC check.	
	RAW_RPT_INT_MSK	6	Interrupt mask for repeat code in RAW mode.	
	-	5:3	Reserved.	
	IR_CODE_BIT_LSB_EN	2	Enable for IR code bit count method. 1: IR engine count code bit by bit count. 0: IR engine count code bit by byte count.	
	IR_SEPR_EN	1	IR separator code check enable.	
	IR_TIMEOUT_CHK_EN	0	IR time-out check enable.	
41h (3D82h)	REG3D82	7:0	Default : 0x00	Access : R/W
	IR_HDC_UPB[7:0]	7:0	The counter upper bound for header code.	
41h (3D83h)	REG3D83	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	IR_HDC_UPB[13:8]	5:0	Please see description of '3D82h'.	
42h (3D84h)	REG3D84	7:0	Default : 0x00	Access : R/W
	IR_HDC_LOB[7:0]	7:0	The counter lower bound for header code.	
42h	REG3D85	7:0	Default : 0x00	Access : R/W

DDC/IR Register (Bank = 3D)

Index (Absolute)	Mnemonic	Bit	Description	
(3D85h)	-	7:6	Reserved.	
	IR_HDC_LOB[13:8]	5:0	Please see description of '3D84h'.	
43h (3D86h)	REG3D86	7:0	Default : 0x00	Access : R/W
	IR_OFC_UPB[7:0]	7:0	The counter upper bound for off code.	
43h (3D87h)	REG3D87	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	IR_OFC_UPB[12:8]	4:0	Please see description of '3D86h'.	
44h (3D88h)	REG3D88	7:0	Default : 0x00	Access : R/W
	IR_OFC_LOB[7:0]	7:0	The counter lower bound for off code.	
44h (3D89h)	REG3D89	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	IR_OFC_LOB[12:8]	4:0	Please see description of '3D88h'.	
45h (3D8Ah)	REG3D8A	7:0	Default : 0x00	Access : R/W
	IR_OFC_RP_UPB[7:0]	7:0	The counter upper bound for repeat off code.	
45h (3D8Bh)	REG3D8B	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	IR_OFC_RP_UPB[11:8]	3:0	Please see description of '3D8Ah'.	
46h (3D8Ch)	REG3D8C	7:0	Default : 0x00	Access : R/W
	IR_OFC_RP_LOB[7:0]	7:0	The counter lower bound for repeat off code.	
46h (3D8Dh)	REG3D8D	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	IR_OFC_RP_LOB[11:8]	3:0	Please see description of '3D8Ch'.	
47h (3D8Eh)	REG3D8E	7:0	Default : 0x00	Access : R/W
	IR_LG01H_UPB[7:0]	7:0	The counter upper bound for logic 0/1 high level width.	
47h (3D8Fh)	REG3D8F	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	IR_LG01H_UPB[9:8]	1:0	Please see description of '3D8Eh'.	
48h (3D90h)	REG3D90	7:0	Default : 0x00	Access : R/W
	IR_LG01H_LOB[7:0]	7:0	The counter lower bound for logic 0/1 high level width.	
48h (3D91h)	REG3D91	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	IR_LG01H_LOB[9:8]	1:0	Please see description of '3D90h'.	
49h	REG3D92	7:0	Default : 0x00	Access : R/W

DDC/IR Register (Bank = 3D)

Index (Absolute)	Mnemonic	Bit	Description	
(3D92h)	IR_LG0_UPB[7:0]	7:0	The counter upper bound for logic 0 width.	
49h (3D93h)	REG3D93	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	IR_LG0_UPB[10:8]	2:0	Please see description of '3D92h'.	
4Ah (3D94h)	REG3D94	7:0	Default : 0x00	Access : R/W
	IR_LG0_LOB[7:0]	7:0	The counter lower bound for logic 0 width.	
4Ah (3D95h)	REG3D95	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	IR_LG0_LOB[10:8]	2:0	Please see description of '3D94h'.	
4Bh (3D96h)	REG3D96	7:0	Default : 0x00	Access : R/W
	IR_LG1_UPB[7:0]	7:0	The counter upper bound for logic 1 width.	
4Bh (3D97h)	REG3D97	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	IR_LG1_UPB[11:8]	3:0	Please see description of '3D96h'.	
4Ch (3D98h)	REG3D98	7:0	Default : 0x00	Access : R/W
	IR_LG1_LOB[7:0]	7:0	The counter lower bound for logic 1 width.	
4Ch (3D99h)	REG3D99	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	IR_LG1_LOB[11:8]	3:0	Please see description of '3D98h'.	
4Dh (3D9Ah)	REG3D9A	7:0	Default : 0x00	Access : R/W
	IR_SEPR_UPB[7:0]	7:0	The counter upper bound for separator code width.	
4Dh (3D9Bh)	REG3D9B	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	IR_SEPR_UPB[11:8]	3:0	Please see description of '3D9Ah'.	
4Eh (3D9Ch)	REG3D9C	7:0	Default : 0x00	Access : R/W
	IR_SEPR_LOB[7:0]	7:0	The counter lower bound for separator code width.	
4Eh (3D9Dh)	REG3D9D	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	IR_SEPR_LOB[11:8]	3:0	Please see description of '3D9Ch'.	
4Fh (3D9Eh)	REG3D9E	7:0	Default : 0x00	Access : R/W
	IR_TIMEOUT_CYC[7:0]	7:0	The counter value for IR timeout cycles. Timeout check will start when 1. IR_TIMEOUT_CHK_EN=1.	

DDC/IR Register (Bank = 3D)

Index (Absolute)	Mnemonic	Bit	Description	
			2. Counter value > IR_TIMEOUT_CYC.	
4Fh (3D9Fh)	REG3D9F	7:0	Default : 0x00	Access : R/W
	IR_TIMEOUT_CYC[15:8]	7:0	Please see description of '3D9Eh'.	
50h (3DA0h)	REG3DA0	7:0	Default : 0x30	Access : R/W
	IR_TIMEOUT_CLR_SW	7	IR timeout clear by software. 1: Enable. 0: Disable.	
	IR_TIMEOUT_CLR_SET[2:0]	6:4	IR timeout clear set. 000: Timeout be clear at HDC check pass. 001: Timeout be clear at OFC check pass & decode 0 state. 010: Timeout be clear at customer code check pass. 011: Timeout be clear at key data code check pass. 100: S/W clear, need also to set TIMEOUT_CLR_SW = 1. Recommend: Set 011 for NEC-like format.	
	-	3	Reserved.	
	IR_TIMEOUT_CYC[18:16]	2:0	Please see description of '3D9Eh'.	
50h (3DA1h)	REG3DA1	7:0	Default : 0x00	Access : R/W
	IR_CODE_BIT_LSB[2:0]	7:5	IR code bit LSB setting. If _IR_CODE_BIT_LSB_EN==1_ (reg_71h[2]) was set, then we can set these 3 bits to specify the number of code bits. Ex: If IR code bits = 36, then we can set register as following 1. Set IR_CODE_BIT_LSB_EN=1 (reg_71h[2]). 2. Set IR_CODE_BYTE= 4_b0100 (reg_91h[3:0]). 3. Set IR_CODE_BIT_LSB= 3_b100 (reg_91h[7:5]).	
	IR_CCODE_BYTE	4	IR customer code byte setting (full mode use only). 0: 1 byte customer code. 1: 2 bytes customer code. Default: 1_b1 (for NEC format).	
	IR_CODE_BYTE[3:0]	3:0	IR code bytes setting (CUSTOMER_CODE+ DATA_CODE+... for full mode and raw mode use). 1: 1 byte. 2: 2 bytes. ... F: 15 bytes.	

DDC/IR Register (Bank = 3D)

Index (Absolute)	Mnemonic	Bit	Description	
			Default: 4_b0100 (for NEC format).	
51h (3DA2h)	REG3DA2	7:0	Default : 0x00	Access : R/W, WO
	RPT_FLAG_CLR_RAW	7	Interrupt flag clear for IR repeat code flag in RAW mode. 1: Clear interrupt flag. 0: Not clear interrupt flag.	
	-	6	Reserved.	
	IR_SEPR_BIT[5:0]	5:0	IR separator bits setting (only used for Mitsubishi format in full mode). The code data bit decode after this bit will into separator state when (REG_IR_SEPR_EN==1).	
51h (3DA3h)	REG3DA3	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	IR_SHOT_SEL[1:0]	5:4	The PSHOT/NSHOT selection for internal counter (only used in S/W mode). 2_b01: Only PSHOT edge detect for counter. 2_b10: Only NSHOT edge detect for counter. 2_b00/11: Both PSHOT and NSHOT edge detect for counter.	
	IR_FIFO_FULL_EN	3	IR FIFO full enable (used in full/raw mode). 0: Disable FIOF full (data can be written over when FIFO is full). 1: Enable FIFO full (data will be discarded when FIFO is full).	
	IR_FIFO_DEPTH[2:0]	2:0	FIFO depth (for decoded IR code data or IR raw data, not for S/W mode counter data).	
52h (3DA4h)	REG3DA4	7:0	Default : 0x00	Access : R/W
	IR_CCODE[7:0]	7:0	IR customer code.	
52h (3DA5h)	REG3DA5	7:0	Default : 0x00	Access : R/W
	IR_CCODE[15:8]	7:0	Please see description of '3DA4h'.	
53h (3DA6h)	REG3DA6	7:0	Default : 0x00	Access : R/W
	IR_GLHRM_NUM[7:0]	7:0	Glitch removal number for crystal based counter. The glitches will be removed whenever their cycle width below the GLHRM_NUM cycle.	
53h (3DA7h)	REG3DA7	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	

DDC/IR Register (Bank = 3D)

Index (Absolute)	Mnemonic	Bit	Description	
	IR_DECOMD[1:0]	5:4	IR decode mode selection 00/11: Full decode mode (NEC and NEC-like format). 01: S/W mode (shot mode, output edge count value). 10: Raw mode (header decode only, output raw data).	
	IR_GLHRM_EN	3	Glitch removal enable.	
	IR_GLHRM_NUM[10:8]	2:0	Please see description of '3DA6h'.	
54h (3DA8h)	REG3DA8	7:0	Default : 0x00	Access : R/W
	IR_CKDIV_NUM[7:0]	7:0	The divided number for input crystal clock, the divided clock is for internal counter use. 8_h00: Divided by 1 8_h01: Divided by 2 .. 8_hFF: Divided by 256 Default: 8_h0E for XTAL clock=14.318MHz 8_hFF for XTAL clock=25.00MHz	
54h (3DA9h)	REG3DA9	7:0	Default : -	Access : RO
	IR_KEY_DATA[7:0]	7:0	IR key data output (for full/raw mode data).	
55h (3DAAh)	REG3DAA	7:0	Default : -	Access : RO
	IR_SHOT_CNT[7:0]	7:0	IR shot count value output in S/W mode, the type of shot is select from IR_SHOT_SEL.	
55h (3DABh)	REG3DAB	7:0	Default : -	Access : RO
	IR_SHOT_CNT[15:8]	7:0	Please see description of '3DAAh'.	
56h (3DACh)	REG3DAC	7:0	Default : -	Access : RO
	-	7:5	Reserved.	
	IR_SHOT_P	4	IR shot type (PSHOT/NSHOT) in S/W mode. 0: NSHOT occurs. 1: PSHOT occurs.	
	-	3	Reserved.	
	IR_SHOT_CNT[18:16]	2:0	Please see description of '3DAAh'.	
56h (3DADh)	REG3DAD	7:0	Default : -	Access : RO
	-	7:6	Reserved.	
	IR_INT_CRC_FLAG	5	IR CRC function interrupt flag.	
	IR_INT_FLAG	4	IR normal function interrupt flag.	
	IR_FIFO_FULL	3	IR FIFO full flag. 1: FIFO is full. 0: FIFO is not full yet.	

DDC/IR Register (Bank = 3D)

Index (Absolute)	Mnemonic	Bit	Description	
	IR_TIMEOUT_FLAG	2	IR timeout flag. 1: Timeout occurs. 0: Not timeout yet.	
	IR_FIFO_EMPTY	1	IR FIFO empty flag for full/raw mode.	
	IR_RPT_FLAG	0	IR FIFO data repeat flag for full mode.	
57h (3DAEh)	**REG3DAE**	7:0	**Default : 0x00**	**Access : R/W**
	IR_CRC_GOLDEN[7:0]	7:0	IR CRC golden value, calculated before power down (CRC check IR register range: 0x3D40 - 0x3D53).	
57h (3DAFh)	**REG3DAF**	7:0	**Default : 0x00**	**Access : R/W**
	IR_CRC_GOLDEN[15:8]	7:0	Please see description of '3DAEh'.	
58h (3DB0h)	**REG3DB0**	7:0	**Default : 0x00**	**Access : WO**
	-	7:3	Reserved.	
	IR_FLAG_CLR	2	IR interrupt flag clear. 1: Clear pulse generate. 0: No operation.	
	IR_CRC_FLAG_CLR	1	IR CRC interrupt flag clear. 1: Clear pulse generate. 0: No operation.	
	IR_FIFO_RD_PULSE	0	IR FIFO read pulse. 1: Read. 0: Not read. Note: need to set this bit to 1 after s/w read "IR_KEY_DATA" (to let FIFO read point go to the next one).	

REGISTER TABLE REVISION HISTORY

Date	Bank	Register
07/10/07		Created first version.
11/06/07	11	1100, 1101, 1104, 1105, 1107, 1118, 1110-1113, 1119, 111E, 111F, 1141, 1154-1159, 11E0-11F5
	12	1200, 1201, 1204, 1205, 1207, 1210-1213, 121E, 1220, 1222-1225, 1228, 1229, 1234, 1238, 1239, 123E, 123F, 1241, 12E1-12FE
12/27/07		Updated for clarification
01/23/08	14	1419, 141A, 1421, 14A4~14AB, 14AE~14C7
	15	1502, 1520
	16	1600
	1C	1C4A, 1CE6
	1E	1E02, 1E03, 1E06, 1E0F, 1E24, 1E25, 1E2A, 1E34, 1E35, 1E59, 1E6E, 1E7A, 1E84, 1E8A, 1EE4, 1EE6
	25	255A, 255B, 2573, 257B, 25C1
	27	27D6
	2C	2CE6, 2CE7, 2CE9, 2CEB, 2CEF
	2F05	2F3E, 2F60, 2F61
	2F07	2F02, 2F03, 2F08~2F0B
	2F0A	2F0A
	2F10	2F1E, 1FCA~2FCF
	2F16	2F37, 2F41, 2F4B, 2F5C, 2F5F
	2F1B	Added
	36	0x21, 0x40, 0x4C, 0x5F, 0x88~0x8A
	37	0x10, 0x88~0x8A
	38	0x2B~0x2D
02/14/08	2C	2CE6~2CE9, 2CEB~2CEF
	32	3289, 328C, 329A, 329E, 32A2, 32AA
02/29/08	2C	2C2A
03/05/08	34	3466, 3467, 3469, 346E, 346F, 3470
04/25/08	14 15	14A9 1544~1547
	2D	2D6C
	2F07	2FA5
	3436	34700x24

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