Yang (Adrian) Liu

(+86)181-0552-1590 | adrianliu00@gmail.com | ◊Homepage
220 Handan Road, Shanghai, China

Education

Fudan University Shanghai, China
Master of Science in Electronics Science and Technology *Sep. 2022 – Present*

- **GPA: 3.85/4.00** **Rank: 1st** (out of 45) **Core Courses GPA: 4.00/4.00**
- **Major Courses:** Advanced Digital Integrated Circuits Design, Parallel Computing, Discrete Mathematics & Optimal Decision, System-Level FPGA Design, Digital Signal Processing VLSI Design

Cornell University Ithaca, USA
Visiting: Graduate Intern in Electrical and Computer Engineering Department *June 2024 – Jan. 2025*

- **Projects:** Programming Model for Composable Accelerator Design, Tile-based Programming Interface

Fudan University Shanghai, China
Bachelor of Engineering in Microelectronic Science and Engineering *Sep. 2018 – June 2022*

- **GPA: 3.80/4.00** **Rank: 3rd** (out of 147) Graduated with Highest Distinction
- **Thesis:** A Software-Hardware Co-design Acceleration of Squeeze-and-excite Network on SOC Platform

Research Experience

Research Intern, Computer Systems Laboratory *Advisor:* Prof. Zhiru Zhang
Cornell University, Ithaca, USA *June 2024 – Jan. 2025*

- **Research Field:** Domain Specific Compiler, Programming Language

Research Assistant, State Key Laboratory of ASIC and System *Advisor:* Prof. Jun Yu, Kun Wang
Fudan University, Shanghai, China *Feb. 2022 – Present*

- **Research Field:** Computer-Aided Design, Integrated Circuit and System Design

Research Intern, Intelligence Computing Lab *Advisor:* Prof. Jun Yu, Jicheng Lu
Shanghai Fudan Microelectronics Group Co., Ltd, Shanghai, China *July 2021 – Feb. 2023*

- **Research Field:** Hardware Accelerator, Artificial Intelligence Application

Publication

[1] **TransLib: An Extensible Graph-Aware Library Framework for Automated Generation of Transformer Operators on FPGA**
Yang Liu, Tianchen Wang, Yuxuan Dong, Zexu Zhang, Shun Li, Jun Yu, Kun Wang
43rd ACM/IEEE International Conference on Computer-Aided Design (ICCAD), 2024

[2] **DIF-LUT: A Simple Yet Scalable Approximation for Non-linear Activation Function on FPGA**
Yang Liu, Xiaoming He, Jun Yu, Kun Wang
33rd International Conference on Field Programmable Logic and Applications (FPL), 2023

[3] **ATE-GCN: An FPGA-based Graph Convolutional Network Accelerator with Asymmetrical Ternary Quantization**
Ruiqi Chen, Jiayu Liu, Shidi Tang, **Yang Liu**, Yanxiang Zhu, Ming Ling and Bruno da Silva
28th Design, Automation and Test in Europe Conference (DATE), 2025

[4] **Deploying Diffusion Models with Latency-Oriented Scheduling and Memory Overflow Prevention Based on Graph Optimization**
Hao Zhou, **Yang Liu**, Hongji Wang, Enhao Tang, Shun Li, Yifan Zhang, Guohao Dai *et al.*
30th Asia and South Pacific Design Automation Conference (ASP-DAC), 2025

[5] **Fitop-Trans: Maximizing Transformer Pipeline Efficiency through Fixed-Length Token Pruning on FPGA**
Kejia Shi*, Manting Zhang*, Keqing Zhao, Xiaoxing Wu, **Yang Liu**, Jun Yu, Kun Wang
34th International Conference on Field-Programmable Logic and Applications (FPL), 2024

[6] **SDAcc: A Stable Diffusion Accelerator on FPGA via Software-Hardware Co-Design**
Hao Zhou, **Yang Liu**, Hongji Wang, Enhao Tang, Shun Li, Yifan Zhang, Kun Wang
32nd IEEE International Symposium On Field-Programmable Custom Computing Machines (FCCM), 2024

[7] **CSTrans-OPU: An FPGA-based Overlay Processor with Full Compilation for Transformer Networks via Sparsity Exploration**
Yueyin Bai*, Keqing Zhao*, **Yang Liu**, Hongji Wang, Hao Zhou, Xiaoxing Wu, Jun Yu, Kun Wang
61st ACM/IEEE Design Automation Conference (DAC), 2024

(***Papers Under Review***)

[8] **DIF-LUT Pro: An Automated Tool for Simple yet Scalable Approximation of Nonlinear Activation on FPGA**
Yang Liu, Shuyang Li, Yu Li, Ruiqi Chen, Shun Li, Jun Yu, Kun Wang
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)

Awards and Honors

- **National Scholarship** *Nov. 2024*
- **Fudan University Outstanding Student (Graduate)** *Oct. 2024*
- **Fudan University Outstanding Administrative Assistant** *June 2024*
- **Fudan University Graduate Student Excellence Scholarship First Prize** *Dec. 2023*
- **Shanghai Outstanding Graduates (Undergraduate)** *June 2022*
- **Fudan University Undergraduate Student Excellence Scholarship First Prize** *May 2022*
- **Fudan University Outstanding Student (Undergraduate)** *Oct. 2021*
- **Shanghai Municipal Scholarship** *Dec. 2020*
- **Fudan University Outstanding Internet Culture Work: Second Prize** *Dec. 2019*
  Co-founded a student mental health social media page, achieving 2k+ followers and nearly 30k views in one semester

Competitions

2024 CAD Contest at ICCAD *May 2024 – Sep. 2024*
- **Outcomes: Honorable Mention**, Participation Mode: Team
- Contest Problem: Power and Timing Optimization Using Multibit Flip-Flop
- Implemented a comprehensive cost model for metrics such as area and delay
- Developed a visualization interface for layout placement results

2021AIWIN Fall – ECG Diagnosis Track *Oct. 2021 – Feb. 2022*
- **Outcomes: Fifth Place**, Participation Mode: Team
- Proposed post-process algorithms for feature correlation analysis
- Implemented mathematical feature extraction as a prior
- Employed existing Python libraries to make further adjustments to the network's prediction

2021 Shanghai Digital Transformation Intelligent Algorithm Competition *Aug. 2021 – Nov. 2021*
- **Outcomes: Grand Prize**, Participation Mode: Team (leader)
- Designed a multi-DNN application scheme for posture recognition in urban scenarios
- Proposed and integrated filter algorithms in the object detection phase
- Collected and transformed appropriate dataset for the urban scenarios

Selected Projects

Allo-DF | *Python, C++, HLS, MLIR; Vitis, Pytest, CI* *July 2024 – Present*

- Explore the potential of agile design for programmable architecture with advanced programming model
- Develop tile-based programming interface and relevant features for dataflow architecture

TransLib | *Python, Verilog HDL, C++, Shell; PyTorch, ONNX, Docker, Vivado* *June 2023 – May 2024*

- Proposed an automated and extensible framework for the accelerator generation of transformer networks
- Proposed an innovative graph analysis and matching algorithms, ideal for large-scale networks
- Designed a configurable template library of various operations to explore the design space

DIF-LUT | *Python, Verilog HDL, Shell; Vivado* *Feb. 2023 – Sep. 2024*

- Proposes a simple yet scalable and effective approximation for Non-linear function
- Designed an automation toolchain for table generation and precision evaluation
- Integrated as an computing unit in FPGA-based accelerator for DNN and Nerf

SEResnet Accelerator on SOC | *Verilog HDL, C++, Python, Shell; Vivado, VStudio* *Feb. 2022 – Dec. 2022*

- Organized the acceleration flow of hardware and software co-design with the compiler
- Deployed specific operations on programmable logic resource of SOC
- Programmed and registered C++ operations on host CPU for simulation

The Straggler - A Vertically Scrolling Shooting Game | *C++; VStudio* *Feb. 2021 – June 2021*

- Pay homage to the classic shooting game – Raiden, based on a C++ pixel engine
- Developed various game mechanics including skill upgrades, level progression, and boss battles
- Incorporated numerous game features, including pause-and-save, background music, and sound effects

Academic and Educational Engagement

43rd ACM/IEEE International Conference on Computer-Aided Design (ICCAD)
Newark, New Jersey, USA *Oct. 2024*
Oral TransLib: An Extensible Graph-Aware Library Framework for Automated Generation of Transformer Operators on FPGA

61st ACM/IEEE Design Automation Conference (DAC)
Moscone West, San Francisco, USA *June 2024*
Oral TrafficHD: Efficient Hyperdimensional Computing for Real-Time Network Traffic Analytics

33rd International Conference on Field Programmable Logic and Applications (FPL)
Chalmers University of Technology, Gothenburg, Sweden *Sep. 2023*
Poster DIF-LUT: A Simple Yet Scalable Approximation for Non-linear Activation Function on FPGA

Teaching Assistant: Methodology of Integrated Circuit Design
Fudan University, Shanghai, China *Spring 2023*

Teaching Assistant: Psychological Training of Success Qualities
Fudan University, Shanghai, China *Fall 2019*

Other Work Experience

Administrative Assistant, Mental Health Center of Fudan University
Fudan University, Shanghai, China *Feb. 2024 – June 2024*

Middle Manager, Work-Study Program Entity of Fudan University
Student Book Kiosk, Fudan University, Shanghai, China *Jan. 2020 – Jan. 2021*

Technical Skills

Languages: Python, C/C++, Verilog HDL, HLS, Shell, Assembly, Tcl, etc.
Developer Tools: Vivado, Vitis, Quartus, Docker, Visual Studio, PyCharm, VMWare Workstation, LaTeX, etc.
Frameworks & Libraries: MLIR, PyTorch, OpenCV, Pytest, NetworkX, Matplotlib, etc.