# Yang Adrian Liu

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## Education

**Fudan University** Shanghai, China
*Master of Engineering in Electronics Science and Technology* *Sep. 2022 – Present*

- **GPA: 3.85/4.00** **Rank: 1st** (out of 45)
- **Research Field:** Integrated Circuit and System Design, Design Automation
- **Major Courses:** Advanced Digital Integrated Circuits Design, System-Level FPGA Design, Digital Signal Processing VLSI Design, Discrete Mathematics & Optimal Decision, Parallel Computing

**Fudan University** Shanghai, China
*Bachelor of Engineering in Microelectronic Science and Engineering* *Sep. 2018 – June 2022*

- **GPA: 3.80/4.00** **Rank: 3rd** (out of 147)
- **Research Field:** Hardware Accelerator, Artificial Intelligence Application
- **Thesis:** A Hardware Acceleration Strategy of Squeeze-and-excite Network Based on the FPAI Chip and Compiler

## Research Experience

**Research Assistant, State Key Laboratory of ASIC and System**
*Fudan University, Shanghai, China* *Feb. 2022 – Present*
*Advisor:* Prof. Jun Yu, Prof. Kun Wang

**Research Intern, Intelligence Computing Lab**
*Shanghai Fudan Microelectronics Group Co., Ltd, Shanghai, China* *July 2021 – Feb. 2023*
*Advisor:* Prof. Jun Yu, Jicheng Lu

**Research Assitant, Video and Image Processing Lab**
*Fudan University, Shanghai, China* *Aug. 2020 – May 2021*
*Advisor:* Prof. Yibo Fan

## Publication

[1] **CSTrans-OPU: An FPGA-based Overlay Processor with Full Compilation for Transformer Networks via Sparsity Exploration** *(pending for camera-ready)*
Yueyin Bai, Keqing Zhao, **Yang Liu**, Hongji Wang, Hao Zhou, Xiaoxing Wu, Jun Yu, Kun Wang
*61st ACM/IEEE Design Automation Conference (DAC), 2024*

[2] **DIF-LUT: A Simple Yet Scalable Approximation for Non-linear Activation Function on FPGA**
**Yang Liu**, Xiaoming He, Jun Yu, Kun Wang
*33rd International Conference on Field Programmable Logic and Applications (FPL), 2023*

## Projects

**AutoTrans** | *Python, Verilog HDL, C++, Shell; PyTorch, ONNX, Docker, Vivado* *June 2023 – Present*

- Proposed an automated and extensible framework for the accelerator generation of transformer networks
- Proposed an innovative graph analysis and matching algorithms, ideal for large-scale networks
- Designed a configurable template library of various operations to explore the design space

**DIF-LUT** | *Python, Verilog HDL, Shell; Vivado* *Feb. 2023 – Present*

- Proposes a simple yet scalable and effective approximation for Non-linear function
- Designed an automation toolchain for table generation and precision evaluation
- Integrated as an computing unit in FPGA-based accelerator for DNN and Nerf

**SEResnet Accelerator on SOC** | *Verilog HDL, C++, Python, Shell; Vivado, VStudio* *Feb. 2022 – Dec. 2022*

- Organized the acceleration flow of hardware and software co-design with the compiler
- Deployed specific operations on programmable logic resource of SOC
- Programmed and registered C++ operations on host CPU for simulation

## Competitions

**2021AIWIN Fall – ECG Diagnosis Track** *Oct. 2021 – Feb. 2022*

- **Outcomes: Fifth Place**, Participation Mode: Team
- Proposed post-process algorithms for feature correlation analysis
- Implemented mathematical feature extraction as a prior
- Employed existing Python libraries to make further adjustments to the network's prediction

**2021 Shanghai Urban Digital Transformation Intelligent Algorithm Competition** *Aug. 2021 – Nov. 2021*

- **Outcomes: Grand Prize**, Participation Mode: Team (leader)
- Designed a multi-DNN application scheme for posture recognition in urban scenarios
- Proposed and integrated filter algorithms in the object detection phase
- Collected and transformed appropriate dataset for the urban scenarios

**Autonomous Obstacle-Avoidance Mini-Car Competition** *July 2021*

- **Outcomes: Second Place**, Participation Mode: Team (leader)
- Completed the control design and physical assembly based on embedded systems
- Programmed control behaviors using assembly language on the 51 microcontroller platform
- Soldered peripheral electrical components to the PCB board

## Awards and Honors

- **Fudan University Graduate Student Excellence Scholarship First Prize** *Dec. 2023*
- **Shanghai Outstanding Graduates (Undergraduate)** *June 2022*
- **Fudan University Undergraduate Student Excellence Scholarship First Prize** *May 2022*
- **Fudan University Outstanding Student** *Oct. 2021*
- **Shanghai Municipal Scholarship** *Dec. 2020*
- **Fudan University Outstanding Internet Culture Work: Second Prize** *Dec. 2019*

  *Co-founded a student mental health social media page, achieving 2k+ followers and nearly 30k views in one semester*

## Academic and Educational Engagement

**33rd International Conference on Field Programmable Logic and Applications (FPL)**
*Chalmers University of Technology, Gothenburg, Sweden* *Sep. 2023*
**Poster** DIF-LUT: A Simple Yet Scalable Approximation for Non-linear Activation Function on FPGA

**Teaching Assistant: Methodology of Integrated Circuit Design**
*Fudan University, Shanghai, China* *Spring 2023*

**Teaching Assistant: Psychological Training of Success Qualities**
*Fudan University, Shanghai, China* *Fall 2019*

## Other Work Experience

**Middle Manager, Work-Study Program Entity of Fudan University**
*Student Book Kiosk, Fudan University, Shanghai, China* *Jan. 2020 – Jan. 2021*

## Technical Skills

**Languages**: Verilog HDL, Python, C/C++, Shell, Assembly, Tcl, etc.
**Developer Tools**: Vivado, Quartus, Git, Docker, Visual Studio, PyCharm, VMWare Workstation, LaTeX, etc.
**Frameworks & Libraries**: PyTorch, OpenCV, NetworkX, Matplotlib, etc.