CORF: Coalescing Operand Register File for GPUs

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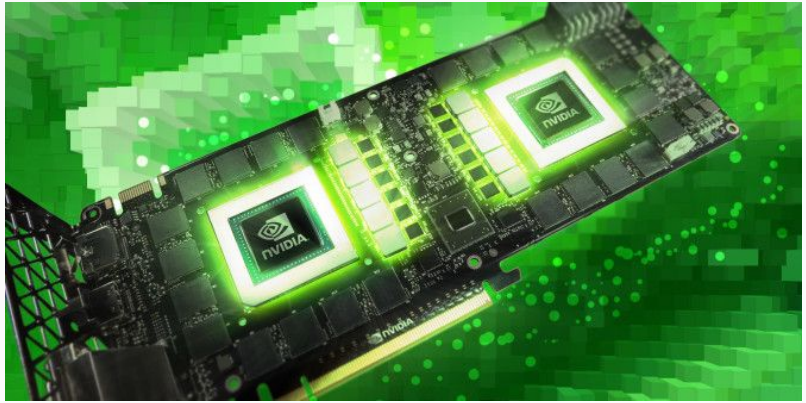
Overview

Overview

- RF substantially affects performance and energy efficiency
- How to deal with port contention on operand collectors and RF banks?
  - CORF (Coalescing Operand Register File)
  - Combine reads to multiple registers for a single instruction into a single read



Technique

Technique (CORF)

- Use the compiler to map register-pairs for the same instruction into the same physical entry
- Only if values are compatible narrow width values
    - Pack highest frequency pairs together

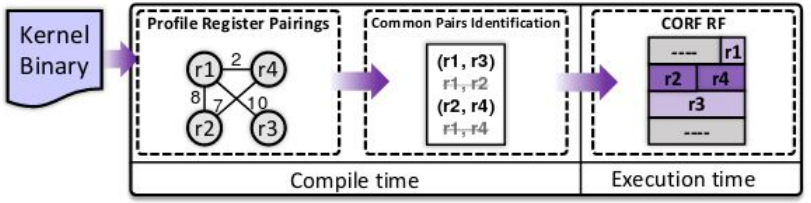


Figure 5. CORF overview. Compiler-generated register pairs guide register allocation to create coalescing opportunities

Technique (Extension -> CORF++)

- Coalesce multiple physical register entries
- Use a register affinity graph to find commonly paired operands
- Color registers such that alignment alternates between high-weight edges

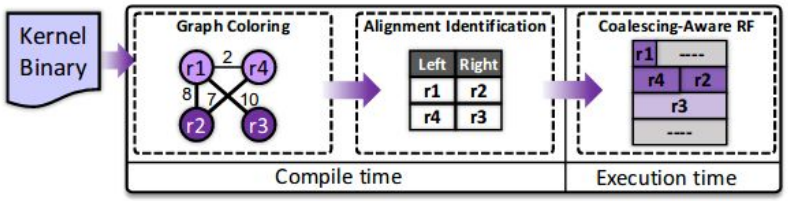


Figure 7. CORF++ overview. At compile time, we identify which registers should be left-aligning, or right-aligning through graph coloring algorithm, so that we can maximize coalescing opportunities. This information will then guide register allocation in our coalescing-aware register file.

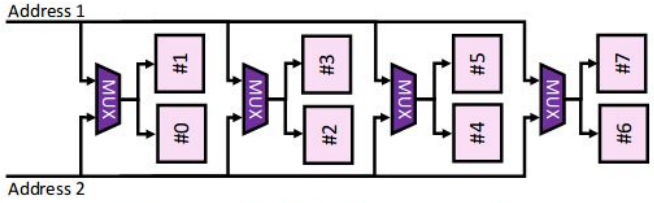


Figure 11. Dual address register file.

Example

Example

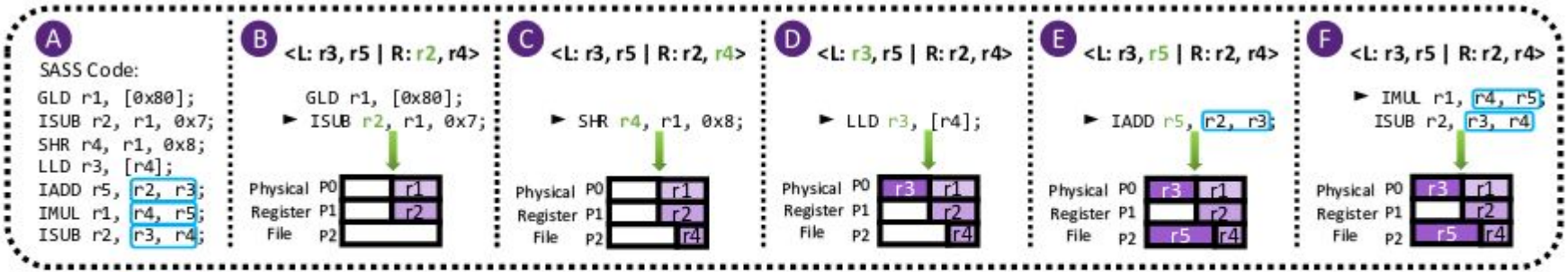


Figure 12. Illustrative Example of CORF++ register allocation (B–D) and read coalescing (E, F).

Results

Results

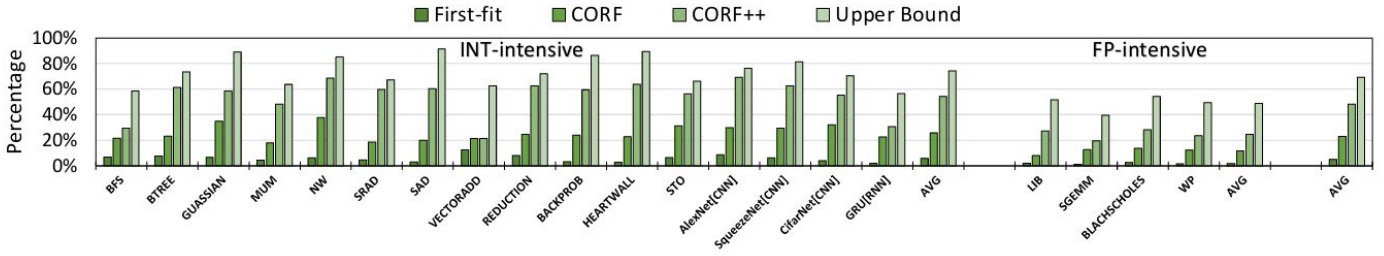


Figure 13. Coalesced instructions: CORF and CORF++ significantly increases the amount of coalescing opportunities.

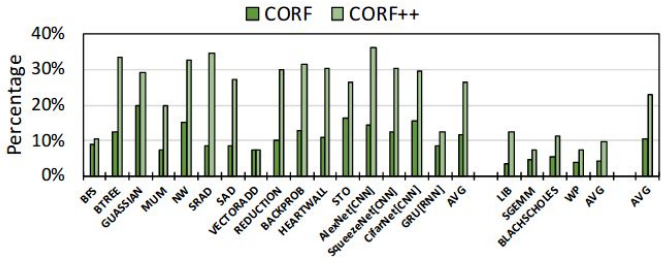


Figure 14. Reduction in number of accesses to register file.

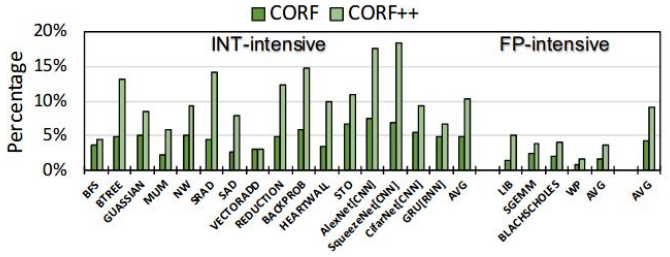


Figure 15. IPC Improvement.

Results

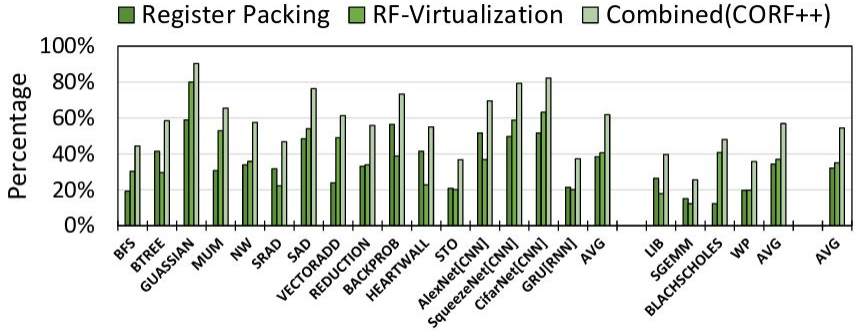


Figure 16. Reduction in allocated physical registers.

Technique	IPC	Register Reads	RF Dyn. Energy	RF Size
Register Packing	1	1	1	0.65
Register Packing + Virtualization	1	1	1	**0.43**
CORF	**1.04**	**0.9**	**0.92**	**0.43**
CORF++	**1.09**	**0.77**	**0.83**	**0.43**

Table 1. Summary of CORF, CORF++, and register packing (and register virtualization). All values normalized to the baseline GPU register file.

Conclusion

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- Complimentary ideas are good
  - Seamlessly works with RF-virtualization from 2015
- 17% if RF Dynamic Energy seems low
  - Very crowded space