Composite-ISA Cores: Enabling Multi-ISA Heterogeneity Using a Single ISA

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Presented by: Nick from CoffeeBeforeArch

Overview

Overview

- Heterogeneous architectures allow applications to migrate to the core best for them at any different moments
- Heterogeneous ISA architectures expands on this idea
- Simplify the implementation of this using a composite ISA

```
  .globl  "_*add_forty_two<Int32>:Int32"
  .align  4, 0x90
"_*add_forty_two<Int32>:Int32":
  .cfi_startproc
  pushq %rbp
Ltmp1992:
  .cfi_def_cfa_offset 16
Ltmp1993:
  .cfi_offset %rbp, -16
  movq  %rsp, %rbp
Ltmp1994:
  .cfi_def_cfa_register %rbp
  addl  $42, %edi
  movl  %edi, %eax
  popq  %rbp
  retq
  .cfi_endproc
```

Problem Definition

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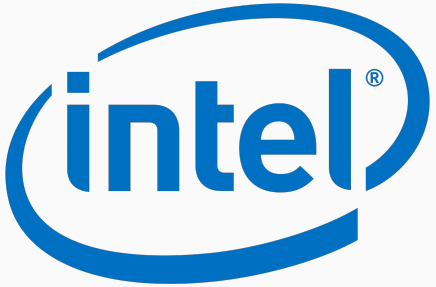
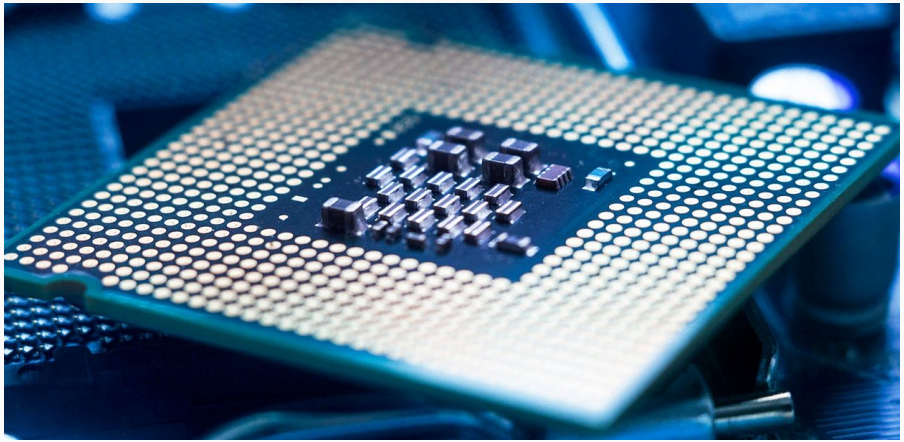
- Heterogeneous ISA architectures expand on asymmetric multi-core
  - “ISA Affinity”
- Implementing multiple ISAs is hard!
  - Benefits + Baggage
  - Legal/Licensing Cost
  - Core Migration



Parameter Exploration

Parameter Exploration

- Register Depth
- Register Width
- Instruction Complexity
- Predication
- SIMD Support



High-Level Design

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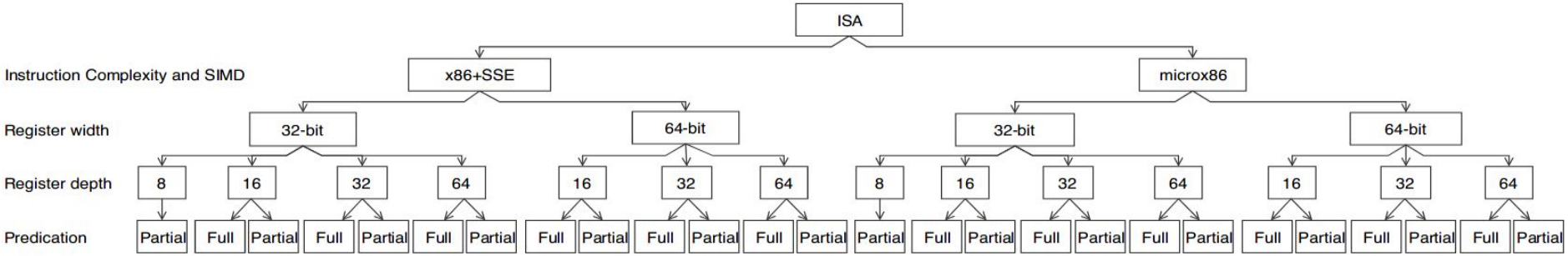


Figure 1. Derivation of Composite Feature Sets from a Superset ISA.

Major Modifications

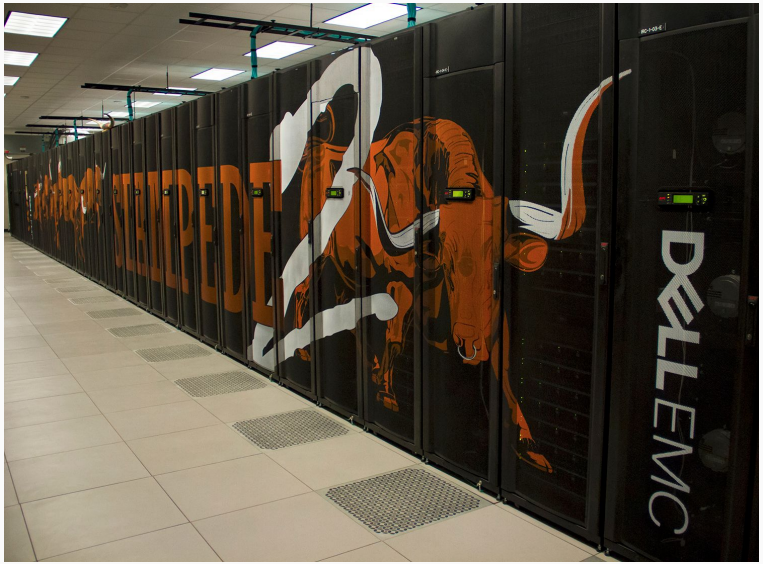
Major Modifications

- LLVM MC Infrastructure
- New encodings for instructions
- Handling downgrades and upgrades
  - Upgrades always move to a core with MORE features
  - Downgrades have a relatively simple transformation
    - Register spilling, addressing mode, etc

Methodology

Methodology

- Full RTL synthesis of decoder for area and power estimates
- 196,560 simulation runs
  - Use XSEDE Comet cluster
- Avoid simulation of obviously bad combinations



Results

Results

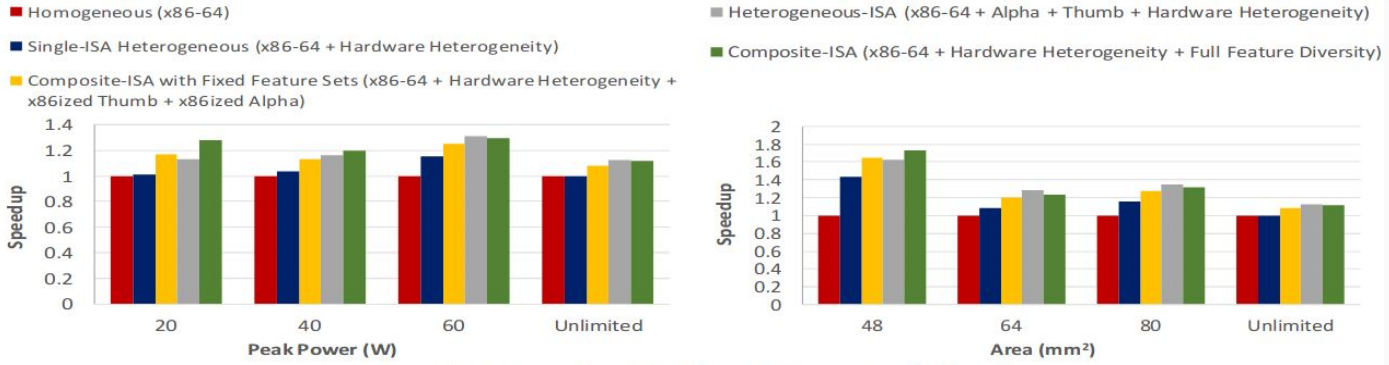


Figure 5. Multi-programmed workload throughput comparison (higher is better)

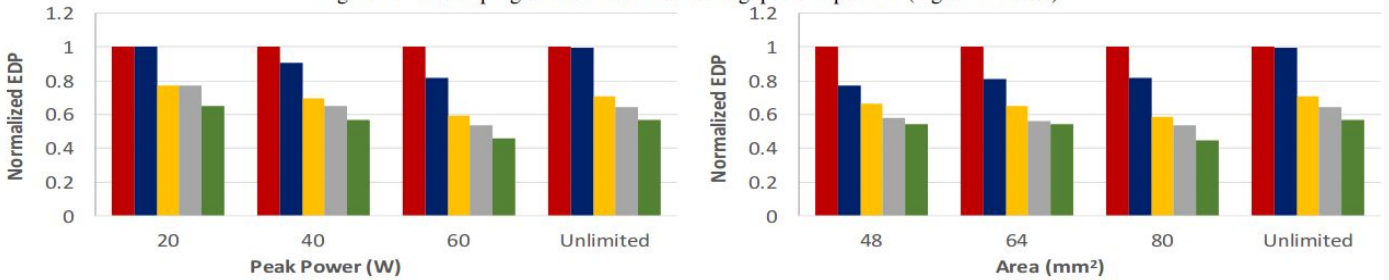


Figure 6. Multi-programmed workload EDP comparison (lower is better)

Results

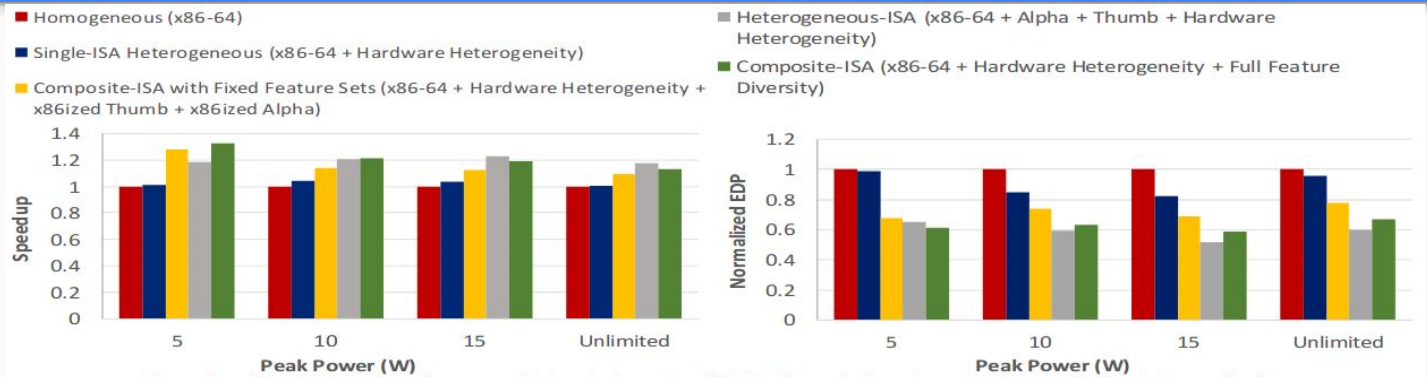


Figure 7. Single Thread Performance (higher is better) and EDP (lower is better) comparison under Peak Power Budget

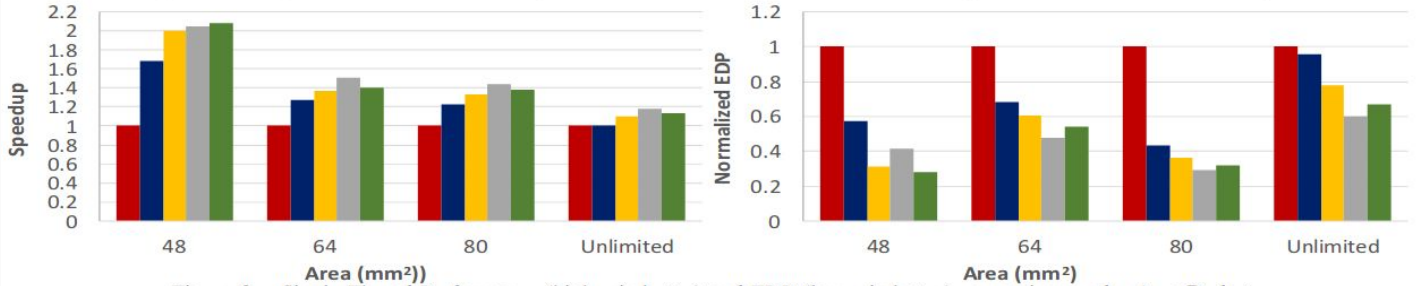


Figure 8. Single Thread Performance (higher is better) and EDP (lower is better) comparison under Area Budget

Results

- Specific areas where downgrades kill performance
  - Namely downgrade to 8 registers
- All ISA features typically included in total design
  - Cores do not usually have completely disjoint features

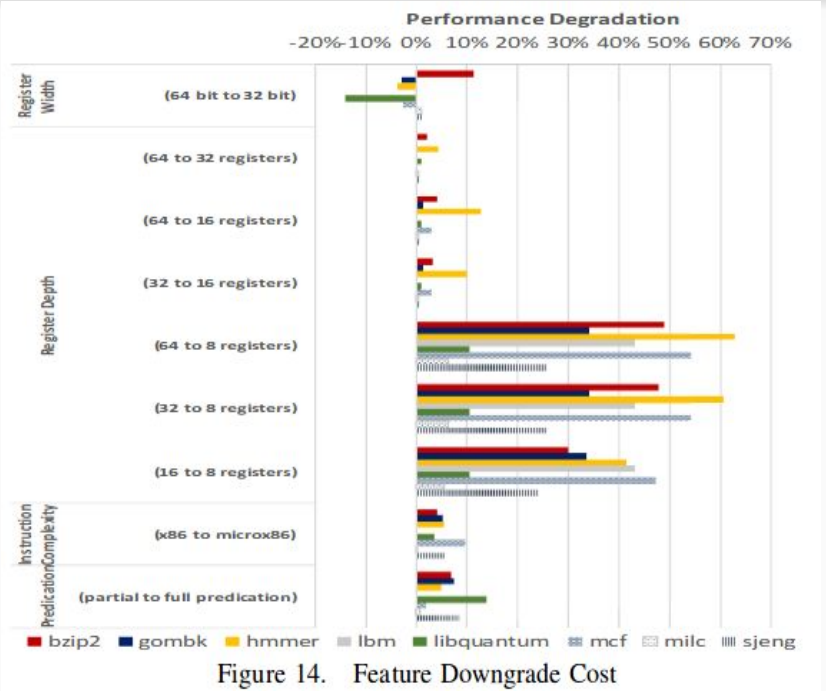


Figure 14. Feature Downgrade Cost

Results

- Overhead from downgrades are minimal!
  - Thanks to that feature diversity
- Is usually as good or better that heterogeneous ISA implementation
  - With much easier implementation!

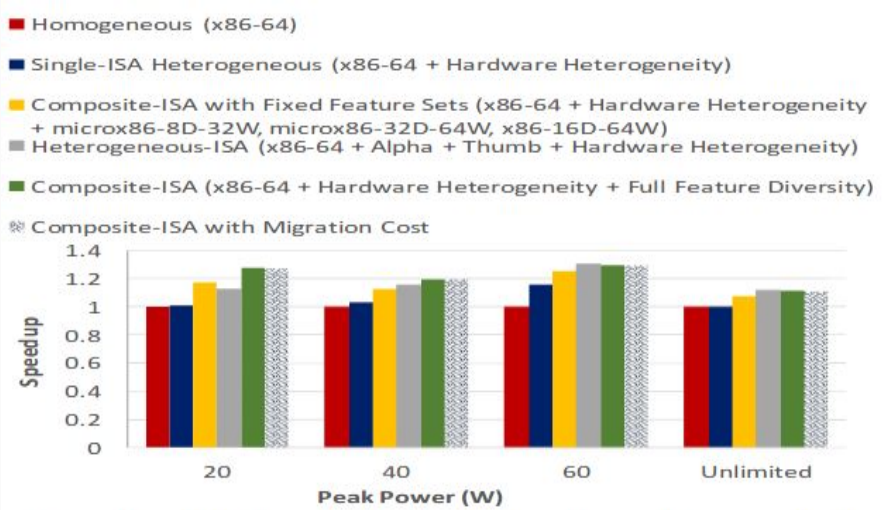


Figure 15. Multi-threaded Workload Throughput with Downgrade Cost

Conclusion

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- Get the advantages of heterogeneous ISA architectures w/o licensing/implementation struggle
  - Far better than single-ISA designs
  - As good or better than heterogeneous ISA designs
- 19% performance improvement, 30% energy savings