ECE 511 - Computer Architecture

Course Syllabus – Spring 2025

Lecture Time: Tuesday & Thursday 2:00-3:20 PM (ECEB 3015)

Instructor: Rakesh Kumar
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Course Prerequisites: ECE 411 or CS 433, C/C++ Programming, SystemVerilog for Hardware Design

Textbook: No Required Textbook.

Supplementary Textbooks:
Hill, Martonosi and Jerger. *Synthesis Lectures on Computer Architecture*, Morgan & Claypool, ISSN: 1935-3235

Dubois, Annavaram and Stenstrom. *Parallel Computer Organization and Design* (1st Ed.), Cambridge University Press, ISBN: 978-0521886758

Hennessy and Patterson. *Computer Architecture: A Quantitative Approach* (5th Ed.), The Morgan Kaufmann, ISBN: 978-0123838728

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1. Course Objectives

Advanced concepts in computer architecture: design, management, and modeling of memory hierarchies; pipelined computers; and multiple processor systems. Emphasis on hardware alternatives in detail and their relation to system performance and cost. More specifically, assuming knowledge of pipelined processors with cache memories, as studied in depth in ECE 411, we continue with advanced techniques for extracting greater levels of instruction-level parallelism and memory-level parallelism in ECE 511. The former exploits opportunities for parallel execution of instructions from an inherently serial instruction stream, while the latter attempts to overlap increasing memory access latency with other useful work. We will study the memory hierarchy as well as virtual memory and will also cover processor chips with multiple cores, where concurrency is extracted from multiple sequential threads of execution and finally look at emerging technologies. Through this course, students will learn not only

the fundamental concepts of computer architecture via the lecture materials, but also the hands-on experience of designing and evaluating architecture techniques via MPs and a course project.

2. Important Links

Campuswire (Q&A): https://campuswire.com/p/GE76EEAD4 (Join Code: 9879)
Canvas (Grades/Assignments): https://canvas.illinois.edu/courses/55131

3. Assignments and Grading

Assignments consist of paper reviews, machine problems (MPs), and a course project. Additionally, there will be a midterm and final exam.

3.1. Grading Breakdown

The table below shows the grading breakdown for this class

Percentage	Assignment	Breakdown
10%	Paper Reviews	The 2 lowest grades will be dropped
30%	Machine Problems	MP1 (10%), MP2 (10%), MP3 (10%)
15%	Midterm Exam	-
15%	Final Exam	-
30%	Final Project	Proposal (5%), Progress Report (5%) Final Presentation (6%), Final Report (14%)

The project can be done in groups, all other assignments must be done individually.

3.2. Paper Reviews

Two papers will be assigned for reading before each lecture, some of the papers will be marked as review candidates, you will choose one of the review candidates and write a brief paper review. The readings can be found on the course website, the readings must be done before lecture, while the reviews are submitted separately at a later deadline.

You must write one paper review per week, they will be due on Canvas at Friday 11:59 PM each week. The two lowest grades from the paper reviews will be dropped at the end of the semester.

The paper review has two parts:

- A paragraph summarizing the paper explaining the problem statement, main ideas and insight, experiment methodology, and key results (200-250 words)
- A paragraph critiquing the work, namely the strengths and weaknesses of the paper and suggested improvements or next steps (200-250 words).

3.3. Machine Problems

Machine problems will involve architecture simulators (Gem5) and hardware design (SystemVerilog). Please see the class webpage for details of each MP.

3.4. Exams

One midterm and one final exam will be administered. Topics will include paper readings, lecture material, and machine problems. More details to come when the dates approach.

4. Course Schedule

Date	*Event*
01/21/2025 T	*Introduction Lecture / **MP1 Released***
01/23/2025 R	Gem5 Tutorial
01/28/2025 T	Lecture
01/30/2025 R	Lecture
02/04/2025 T	Lecture / **MP1 Due** / **MP2 Released**
02/06/2025 R	Lecture
02/11/2025 T	SystemVerilog and RTL Tutorial
02/13/2025 R	Lecture
02/18/2025 T	Lecture / **MP2 Due** / **MP3 Released**
02/20/2025 R	Lecture
02/25/2025 T	Lecture
02/27/2025 R	Lecture / **Midterm Exam**
03/04/2025 T	Lecture
03/06/2025 R	Lecture
03/11/2025 T	Lecture
03/13/2025 R	Lecture / **MP3 Due** / **Final Project Start**
03/18/2025 T	*Spring Break*
03/20/2025 R	*Spring Break*
03/25/2025 T	Lecture / **Final Project Proposal Due**
03/27/2025 R	Lecture

04/01/2025 T	Lecture
04/03/2025 R	Lecture
04/08/2025 T	Lecture / **Final Exam**
04/10/2025 R	Lecture
04/15/2025 T	Lecture / **Progress Report Due**
04/17/2025 R	Lecture
04/22/2025 T	Lecture
04/24/2025 R	Lecture
04/29/2025 T	Lecture
05/01/2025 R	***Project Presentations***
05/06/2025 T	***Project Presentations / Final Report Due***