IBM PowerPC Broadway RISC Microprocessor Revision Level DD1.X

Datasheet

Version: 0.3

Preliminary

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1. General Information

The IBM PowerPC® Broadway RISC[1] Microprocessor is a 32-bit implementation of the IBM PowerPC family. This document contains pertinent physical and electrical characteristics of the IBM PowerPC Broadway RISC Microprocessor Revision DD1.X Single Chip Module (SCM). The IBM PowerPC Broadway RISC Microprocessor is also referred to as the Broadway throughout this document.

1.1 Features

This section summarizes the features of the Broadway implementation of the PowerPC Architecture™. Major features of the Broadway include the following:

- Branch processing unit
  - Fetches four instructions per clock
  - Processes one branch per cycle and can resolve two speculations
  - Executes single speculative stream during fetch of another speculative stream
  - Has 512-entry branch history table (BHT) for dynamic prediction
- Dispatch unit
  - Has full hardware detection of dependencies which are resolved in the execution units
  - Dispatches two instructions to six independent units (system, branch, load/store, fixed-point unit 1, fixed-point unit 2, or floating-point)
  - Has serialization control (predispatch, postdispatch, execution, serialization).
- Decode
  - Register file access
  - Forwarding control
  - Partial instruction decode
- Load/store unit
  - Has single-cycle load or store cache access (byte, half-word, word, double-word).
  - Has effective address generation
  - Allows hits under misses (one outstanding miss).
  - Has single-cycle misaligned access within double word boundary
  - Has alignment, zero padding, sign extend for integer register file
  - Converts floating-point internal format (using alignment, normalization, and quantization).
  - Sequences for load/store multiples and string operations.
  - Has store gathering.
  - Has cache and TLB instructions
  - Supports big and little-endian byte addressing
  - Supports misaligned little-endian in hardware.
- Fixed-point units

1. Reduced instruction set computer

- Fixed-point unit 1 (FXU1); multiply, divide, shift, rotate, arithmetic, logical
- Fixed-point unit 2 (FXU2); shift, rotate, arithmetic, logical
- Single-cycle arithmetic, shift, rotate, logical
- Multiply and divide support (multi-cycle)
- Early out multiply.

- Floating-point unit
  - Support for IEEE-754 standard single- and double-precision floating-point arithmetic
  - 3-cycle latency, 1-cycle throughput, single-precision multiply-add
  - 3-cycle latency, 1-cycle throughput, double-precision add
  - 4-cycle latency, 2-cycle throughput, double-precision multiply-add
  - Hardware support for divide
  - Hardware support for denormalized numbers
  - Time deterministic non-IEEE mode
  - Support for paired single floating point arithmetic
  - Data quantization support.
- System unit
  - Executes CR logical instructions and miscellaneous system instructions
  - Has special register transfer instructions.
- Level 1 (L1) cache structure
  - 32K, 32-byte line, 8-way set associative instruction cache.
  - 32K, 32-byte line, 8-way set associative data cache.
  - Instruction cache line lock.
  - Optional local memory partition.
  - Single-cycle cache access.
  - Pseudo-LRU replacement.
  - Copy-back or write-through data cache (on a page per page basis).
  - Supports PowerPC memory coherency modes.
  - Non-blocking instruction and data cache (supports hits under one outstanding miss).
  - No snooping of instruction cache.
- Memory management unit
  - 128 entry, 2-way set associative instruction TLB.
  - 128 entry, 2-way set associative data TLB.
  - Hardware reload for TLB's.
  - 4 instruction BAT's and 4 data BATs (8 each in enhanced mode).
  - Virtual memory support for up to 4 exabytes (2^{52}) virtual memory.
  - Real memory support for up to 4 gigabytes (2^{32}) of physical memory.

- Level 2 (L2) cache
  - 256KB, 64-byte line, 2-way set associative on-chip cache memory
  - Internal L2 cache controller with 2K-entry tag array.
  - Copy-back or write-through data cache (on a page basis, or for all L2).
  - 64-byte cache line organized as two 32-byte sectors.
  - L2 frequency at core speed.
  - Load miss causes 32B fetch from memory (64B or 128B fetch selectable in enhanced mode).
  - Error correction code (ECC) protection on cache array.
- Bus interface
  - Is compatible with 60X processor interface
  - Has a 32-bit address bus
  - Has a 64-bit data bus (also supports 32-bit data bus mode)
  - Supports bus-to-core frequency multipliers of 2x, 2.5x, 3x, 3.5x, 4x, 4.5x, 5x, 5.5x, 6x, 6.5x, 7x, 7.5x, 8x, 8.5x, 9x, 9.5x, 10x, 11x, 12x, 13x, 14x, 15x, 16x, 17x, 18x, 19x and 20x
  - Has DMA support for local memory load/store.
  - Supports up to two outstanding transactions on the bus (four in enhanced mode).
- Write Gather Pipe
  - 128 byte circular queue
  - 32 byte transfers
  - Independent read and write ports
- Testability
  - LSSD scan design
  - JTAG interface.

1.2 Processor Version Register

The IBM PowerPC Broadway RISC Microprocessor has the following processor version register (PVR) values for the respective design revision levels.

Table 1-1. Broadway Processor Version Register (PVR)

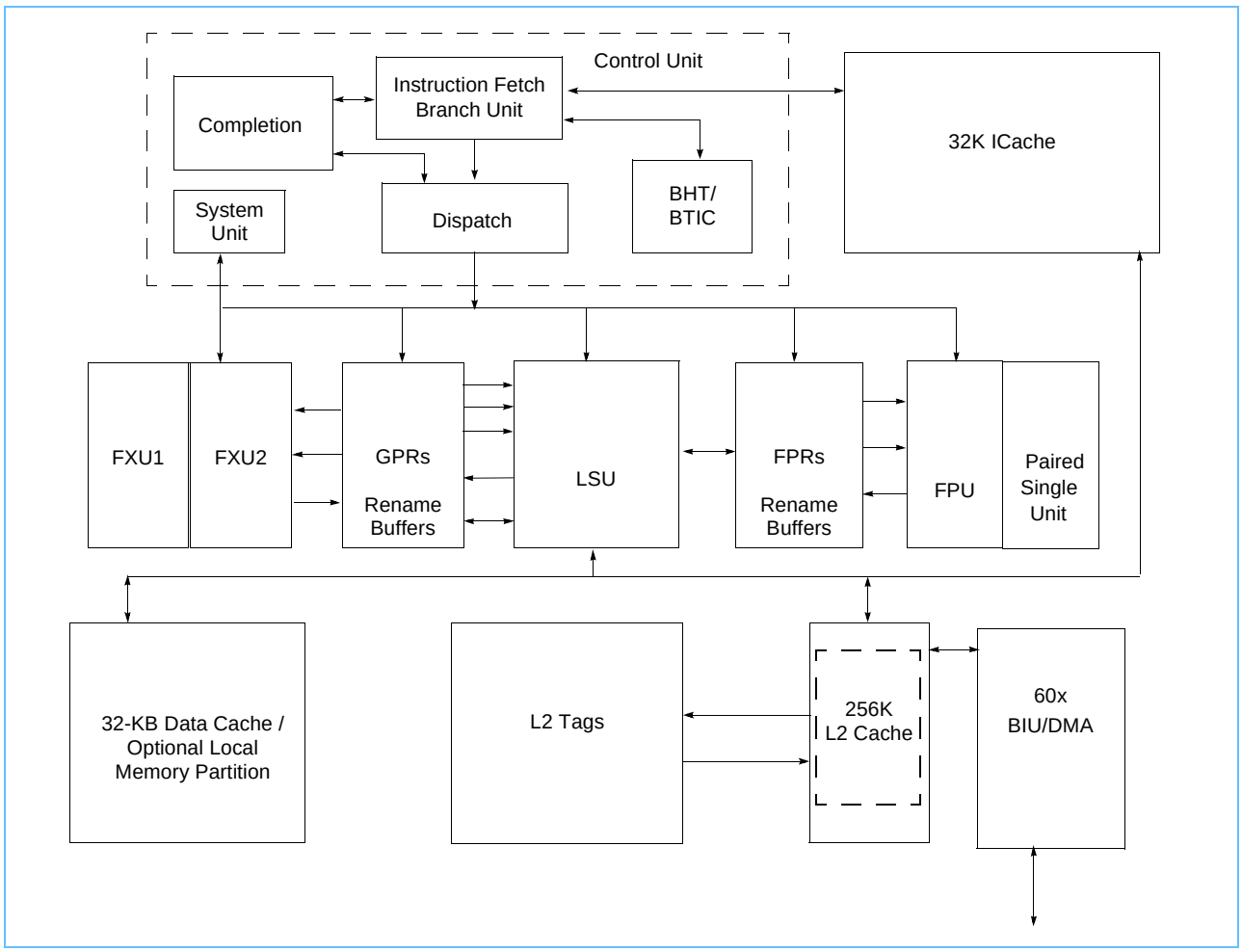
Broadway Design Revision Level	Broadway PVR
DD1.0	0x000871r0
Note: r = reserved nibble; reserved bits can be either '0' or '1', and should be masked in application software.	

2. Overview

The IBM PowerPC Broadway RISC Microprocessor, also called the Broadway, is targeted for high-performance, low-power systems using a 60× bus. The Broadway also includes an internal 256kB L2 cache with on-board error correction circuitry (ECC).

2.1 Block Diagram

Figure 2-1. IBM PowerPC Broadway RISC Microprocessor Block Diagram



2.2 General Parameters

Table 2-1. Broadway General Parameters

Item	Description	Notes
Technology	90nm copper silicon-on-insulator (SOI) technology Low-K dialectric 8 layer metal wirings	
Die Size	15.21 sq. mm (3.9x3.9mm)	
Logic design	Fully static	
Package	292-pin plastic ball grid array (FC-PBGA) 21 × 21 mm (1.0-mm pitch) 0.8-mm ball size	
Core power supply	1.15V ± 5%	
I/O power supply	1.20 V ±120 mV	

3. Electrical and Thermal Characteristics

This section provides AC and DC electrical specifications and thermal characteristics for the Broadway.

3.1 DC Electrical Characteristics

The tables in this section describe the DC electrical characteristics for the Broadway.

Table 3-1. Recommended Operating Conditions

Characteristic	Symbol	Value	Unit	Notes
Core supply voltage (729 MHz)	V_{DD}	1.15 +/- 5%	V	
60X bus I/O supply voltage	OV_{DD}	1.20 +/- 120mV	V	
PLL supply voltage[2]	AV_{DD}	1.20 +/- 120mV	V	
Input voltage	V_{IN}	GND to OV_{DD}	V	
Die-junction temperature	T_J	0 to 95	°C	
Case temperature	T_c	90	°C	3

Notes:
1. ESD Specifications:
   Human body model +/- 500V (Nintendo Specs)
   Machine model +/- 200V (Nintendo Specs)
   CDM = 800V (Nintendo's specs)
2. AVDD power supply AC noise should be less than 20mV for 0 to 500MHz and 3mV for 500MHz and higher.
3. T_c corresponds to max. junction temperature of 95C with a max. power dissipation of 5.5W.

Table 3-2. Package Thermal Characteristics

Characteristic	Symbol	Value	Unit
FC-PBGA package thermal resistance, junction-to-case thermal resistance (typical)	θ_{JC}	TBD	°C/W
FC-PBGA package thermal resistance, junction-to-lead thermal resistance (typical)	θ_{JB}	TBD	°C/W
Note: θ_{JC} is the internal resistance from the junction to the back of the die. A heat sink customized to the end user application and ambient operating environment is required to ensure the die junction temperature is maintained within the limits defined in *Table 3-1* on page 14.			

Table 3-3. DC Electrical Specifications
See *Table 3-1* on page 14 for recommended operating conditions.

Characteristic	Symbol	Voltage		Unit	Notes
		Min.	Max.		
Input high voltage	$V_{IH\ (1.20\ V)}$	0.75	—	V	
Input low voltage	$V_{IL\ (1.20\ V)}$	—	0.40	V	
Input leakage current, V_{IN} = applies to all OV_{DD} levels	I_{IN}	—	TBD	µA	
Hi-Z (off state) leakage current, V_{IN} = applies to all OV_{DD} levels	I_{TSI}	—	TBD	µA	
Output high voltage, I_{OH} = -4 mA	$V_{OH\ (1.20\ V)}$	0.90	—	V	
Output low voltage, I_{OL} = 4 mA	$V_{OL\ (1.20\ V)}$	—	0.30	V	
Capacitance, V_{IN} = 0 V, f = 1 MHz	C_{IN}	—	5	pF	

Table 3-4. Power Consumption
See *Table 3-1* on page 14 for recommended operating conditions.

Mode	T_j	T_c	Processor Frequency	Unit	Notes
			729 MHz		
Maximum Power[1]	95°C	90°C	5.5	W	
Maximum Power[1]	90°C	TBD	5.2	W	
Maximum Power[1]	85°C	TBD	4.8	W	

Note:
1. Maximum power is an estimate of DC and AC power for worst case instruction mix and process parameters at Vdd=1.2V, OVdd=1.2V, 729Mhz, and different T_j and T_c conditions (i.e. junction and case temperature, respectively).

3.2 AC Electrical Characteristics

This section provides the AC electrical characteristics for the Broadway. After fabrication, parts are sorted by maximum processor core frequency as shown in *Section 3.3, Clock AC Specifications,* on page 16, and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL configuration (PLL_CFG[0-4]) signals.

3.3 Clock AC Specifications

Table 3-5 provides the clock AC timing specifications as defined in *Figure 3-1*.

Table 3-5. Clock AC Timing Specifications
See *Table 3-1* on page 14 for recommended operating conditions.[1, 3, 5]

Figure 3-1 Timing Reference	Characteristic	Value		Unit	Notes
		Min.	Max.		
	Processor frequency	486	729	MHz	
	SYSCLK frequency	162	243	MHz	
1	SYSCLK cycle time	4.11	6.17	ns	
2, 3	SYSCLK slew rate	2.50	10.0	V/ns	2

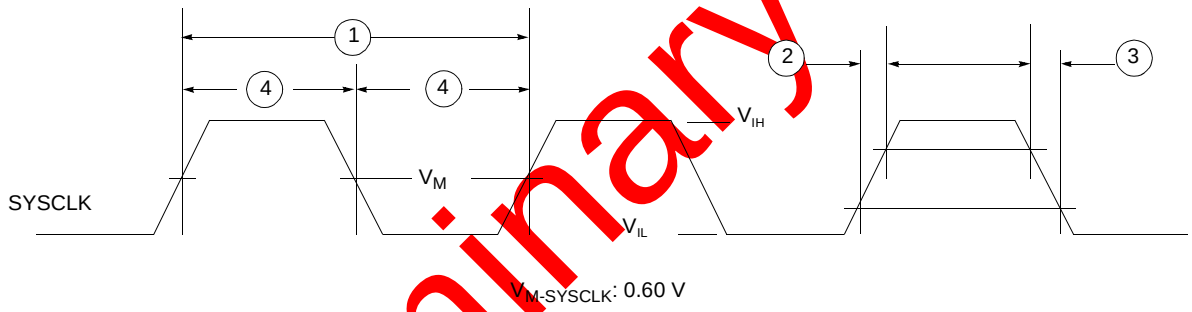
Notes:
1. **Caution:** The SYSCLK frequency and the PLL_CFG[0:4] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:4] signal description in *Table 5-1, Broadway Microprocessor PLL Configuration,* on page 35 for valid PLL_CFG[0:4] settings.
2. Slew rate for the SYSCLK inputs is measured from 0.4 to 0.75 V.
3. Timing is guaranteed by design and characterization, and is not tested.
4. Relock timing is guaranteed by design and characterization, and is not tested. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that hard reset ($\overline{\text{HRESET}}$) must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.
5. During power-up or if the frequency of SYSCLK is changed during hardware reset ($\overline{\text{HRESET}}$), then the PLL must be reset to lock onto the new frequency. The PLL is reset with the $\overline{\text{SRESET}}$ pin. Internal PLL reset time is the minimum time that $\overline{\text{SRESET}}$ must be asserted once SYSCLK and applied voltage are stable.

Table 3-5. Clock AC Timing Specifications
See *Table 3-1* on page 14 for recommended operating conditions.[1, 3, 5]

Figure 3-1 Timing Reference	Characteristic	Value		Unit	Notes
		Min.	Max.		
4	SYSCLK duty cycle measured at 0.60 V	25	75	%	
	SYSCLK cycle-to-cycle jitter	—	TBD	ps	4
	Internal PLL relock time	—	100	µs	4
	Internal PLL reset time	10	—	µs	5

Notes:
1. **Caution:** The SYSCLK frequency and the PLL_CFG[0:4] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:4] signal description in *Table 5-1, Broadway Microprocessor PLL Configuration,* on page 35 for valid PLL_CFG[0:4] settings.
2. Slew rate for the SYSCLK inputs is measured from 0.4 to 0.75 V.
3. Timing is guaranteed by design and characterization, and is not tested.
4. Relock timing is guaranteed by design and characterization, and is not tested. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that hard reset (HRESET) must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.
5. During power-up or if the frequency of SYSCLK is changed during hardware reset (HRESET), then the PLL must be reset to lock onto the new frequency. The PLL is reset with the SRESET pin. Internal PLL reset time is the minimum time that SRESET must be asserted once SYSCLK and applied voltage are stable.

Figure 3-1. SYSCLK Input Timing Diagram



3.4 60x Bus Input AC Specifications

Table 3-6 provides the 60x bus AC timing specifications defined in *Figure 3-3* and *Figure 3-4* on page 20.

Table 3-6. 60x Bus Input AC Timing Specifications
See *Table 3-1* on page 14 for operating conditions.[1, 5, 6]

Figure 3-3 and 3-4 Timing Reference	Characteristic	Min.	Max.	Unit	Notes
10a	Input setup: SYSCLK to all inputs valid	TBD	—	ns	
10c	Mode select input setup to HRESET, (TLBISYNC), QACK, and DRTRY	8	—	t_{SYSCLK}	2, 3, 4
11a	Input hold: SYSCLK to inputs invalid	TBD	—	ns	
11c	HRESET to mode select input hold (TLBISYNC)., QACK, and DRTRY	0	—	ns	2, 4
V_M	Measurement reference voltage for inputs			—	
V_{IL-AC}	AC timing reference levels	—	TBD	V	7
V_{IH-AC}		TBD	—		
Slew Rate	Reference input slew rate	TBD	—	V/ns	

Notes:
1. Input specifications are measured from the midpoint voltage (V_M) of the signal in question to the V_M of the rising edge of the input SYSCLK. Timings are measured at the pin (see *Figure 3-3* on page 19).
2. The setup and hold time is with respect to the rising edge of HRESET (see *Figure 3-4* on page 20).
3. t_{SYSCLK} is the period of the external clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
4. This specification is for configuration mode select only. Also note that the HRESET must be held asserted for a *minimum of 255 bus clocks* after the PLL relock time during the power-on reset sequence.
5. All values are guaranteed by design, and are not tested.
6. Refer to *Section 3.4.1* on page 18 and *Figure 3-2* on page 19 for input setup timing definitions.
7. Input reference signal levels used to establish the timings defined in this table.

3.4.1 Input Setup Timing

The information in this subsection is provided to clarify the criteria used to establish the timings in *Table 3-6*. The DC Electrical Specifications shown in *Table 3-3* on page 15 are not altered by this clarification. The valid input signal levels remain V_{IH} and V_{IL}.

The input setup times shown as 10a in *Table 3-6* specify the required time from the input signal crossing V_M to the rising edge of SYSCLK crossing V_M.

For the timings in *Table 3-6* to be valid, the falling edge of the input signal shown in *Table 3-6* is assumed to transition through V_M and cross V_{IL-AC} at the slew rate specified in *Table 3-6*. Input signals that do not reach the V_{IL-AC} boundary, or slew from V_M to V_{IL-AC} more slowly than specified, will result in longer input setup times.

In the same way, on the rising edge, the input signal must continue past V_M and cross the V_{IH-AC} boundary within the specified minimum slew rate. Input signals that do not reach the V_{IH-AC} boundary within the slew rate specified will result in longer input setup times.

Figure 3-3 provides the input timing diagram for the Broadway.

Figure 3-2. Input Timing Definition

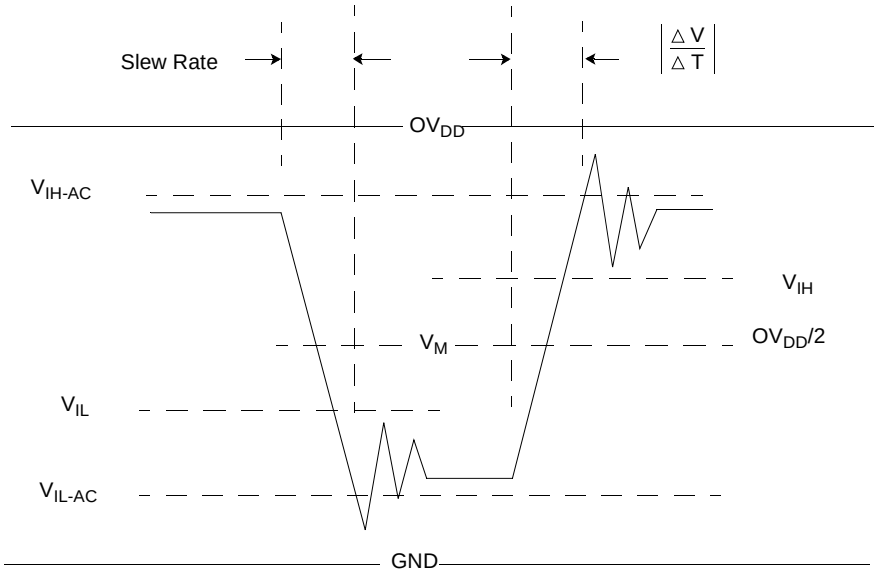


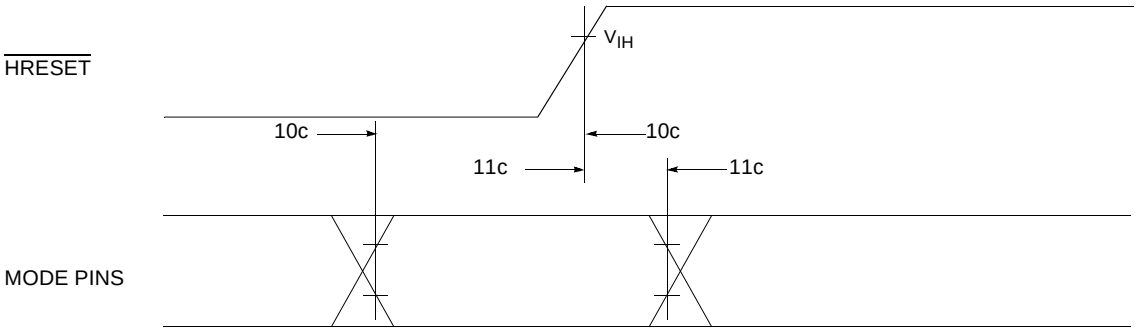
Figure 3-3. Input Timing Diagram

V_M = Midpoint Voltage (OV_{DD}/2)

Note: The minimum slew rate specified in *Table 3-6* on page 18 is required to achieve the input timings specified. See *Section 3.4.1, Input Setup Timing,* on page 18 and *Figure 3-2* for additional information.

Figure 3-4 provides the mode select input timing diagram for the Broadway.

Figure 3-4. Mode Select Input Timing Diagram



3.5 60x Bus Output AC Specifications

Table 3-7 provides the 60× bus output AC timing specifications for the Broadway as defined in *Figure 3-6* on page 23.

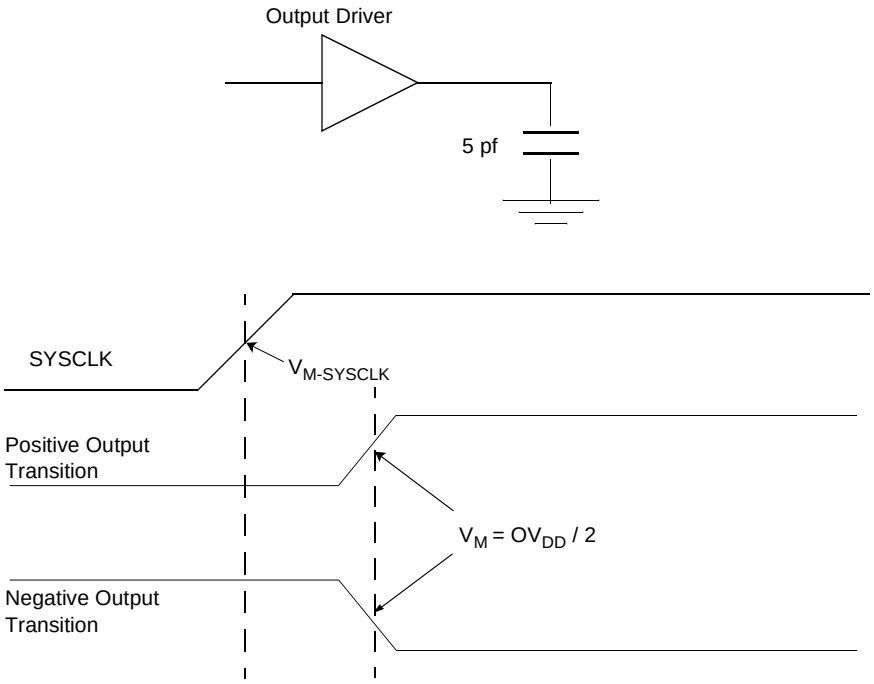
Table 3-7. 60x Bus Output AC Timing Specifications
See *Table 3-1* on page 14 for operating conditions.[1, 4, 6]

Figure 3-6 Timing Reference	Characteristic	Min.	Max.	Unit	Notes
12	SYSCLK to Output Driven (Output Enable Time)	TBD	—	ns	
13	SYSCLK to Output Valid	—	TBD	ns	5
14	SYSCLK to Output Invalid (Output Hold)	TBD	–	ns	
15	SYSCLK to Output High Impedance (all signals except address retry [$\overline{\text{ARTRY}}$], address bus busy [$\overline{\text{ABB}}$], and data bus busy [$\overline{\text{DBB}}$])	—	TBD	ns	
16	SYSCLK to $\overline{\text{ABB}}$ and $\overline{\text{DBB}}$ high impedance after pre-charge	—	1.0	t_{SYSCLK}	2
17	SYSCLK to $\overline{\text{ARTRY}}$ high impedance before precharge	—	TBD	ns	
18	SYSCLK to $\overline{\text{ARTRY}}$ precharge enable	TBD	—	ns	3
19	Maximum delay to $\overline{\text{ARTRY}}$ precharge	—	1.0	t_{SYSCLK}	2, 3
20	SYSCLK to $\overline{\text{ARTRY}}$ high impedance after precharge	—	2.0	t_{SYSCLK}	2, 3

Notes:

1. All output specifications are measured from the V_M of the rising edge of SYSCLK to the midpoint of the output signal in question using a test load as shown in *Figure 3-5* on page 22. Both input and output timings are measured at the pin. Timings are determined by design.
2. t_{SYSCLK} is the period of the external bus clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration of the parameter in question.
3. Nominal precharge width for $\overline{\text{ARTRY}}$ is 1.0 t_{SYSCLK}.
4. Guaranteed by design and characterization, and not tested.
5. Output Valid timing increases as the V_{DD} is reduced. These values assume a V_{DD} minimum of TBD V.
6. See *Figure 3-5* on page 22 and *Figure 3-6* on page 23 for output loading and timing definitions.

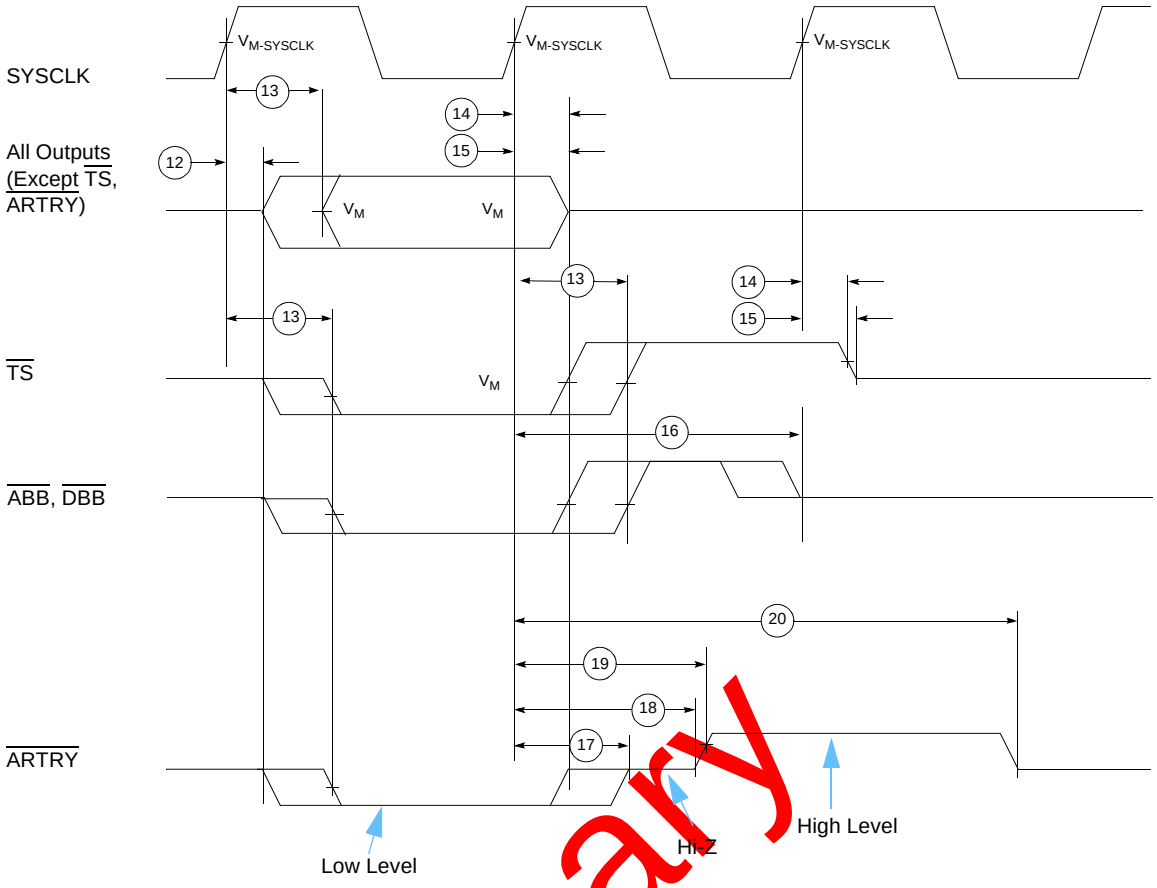
Figure 3-5. Output Valid Timing Definition



Output Transition defined between SYSCLK at V_M and the respective transition level.

Note: The timing definition is valid using the termination model shown here with timings referenced to the respective pin of the specified output driver.

Figure 3-6. Output Timing Diagram for IBM PowerPC Broadway RISC Microprocessor



Note: SYSCLK V_M as defined in *Section 3.3, Clock AC Specifications*, on page 16.
Output V_M as defined in *Figure 3-5, Output Valid Timing Definition*, on page 22.

3.5.1 IEEE 1149.1 AC Timing Specifications

Table 3-8 provides the IEEE 1149.1 (JTAG) AC timing specifications as defined in the following figures:

To find out more about...	See...
JTAG Clock Input Timing Diagram	*Figure 3-7* on page 25.
TRST Timing Diagram	*Figure 3-8* on page 25.
Boundary-Scan Timing Diagram	*Figure 3-9* on page 25.
Test Access Port Timing Diagram	*Figure 3-10* on page 26.

The five JTAG signals are: test data input (TDI), test data output (TDO), test mode select (TMS), test clock (TCK), and test reset ($\overline{\text{TRST}}$).

Table 3-8. JTAG AC Timing Specifications (Independent of SYSCLK)
See *Table 3-1* on page 14 for operating conditions.

Figures 3-7 through 3-10 Timing Reference	Characteristic	Min.	Max.	Unit	Notes
	TCK frequency of operation	TBD	TBD	MHz	
1	TCK cycle time	TBD	—	ns	
2	TCK clock pulse width measured at TBD V	TBD	—	ns	
3	TCK rise and fall times	TBD	TBD	ns	4
4	Specification obsolete, intentionally omitted	—	—	—	
5	$\overline{\text{TRST}}$ assert time	TBD	—	ns	1
6	Boundary-scan input data setup time	TBD	—	ns	2
7	Boundary-scan input data hold time	TBD	—	ns	2
8	TCK to output data valid	—	TBD	ns	3, 5
9	TCK to output high impedance	TBD	TBD	ns	3, 4
10	TMS, TDI data setup time	TBD	—	ns	
11	TMS, TDI data hold time	TBD	—	ns	
12	TCK to TDO data valid	TBD	TBD	ns	5
13	TCK to TDO high impedance	TBD	TBD	ns	4
14	TCK to output data invalid (output hold)	TBD	—	ns	

Notes:
1. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. Guaranteed by design.
2. Non-JTAG signal input timing with respect to TCK.
3. Non-JTAG signal output timing with respect to TCK.
4. Guaranteed by characterization and not tested.
5. Minimum specification guaranteed by characterization and not tested.

Figure 3-7 provides the JTAG clock input timing diagram.

Figure 3-7. JTAG Clock Input Timing Diagram

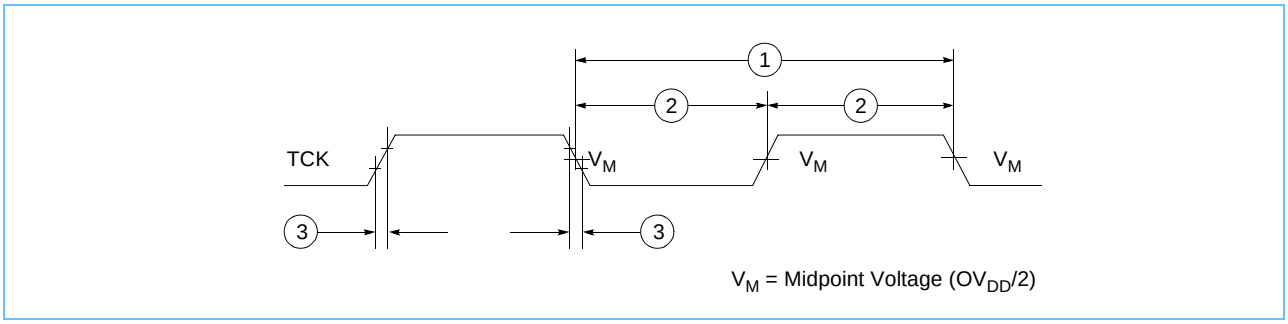


Figure 3-8 provides the $\overline{\text{TRST}}$ timing diagram.

Figure 3-8. $\overline{\text{TRST}}$ Timing Diagram

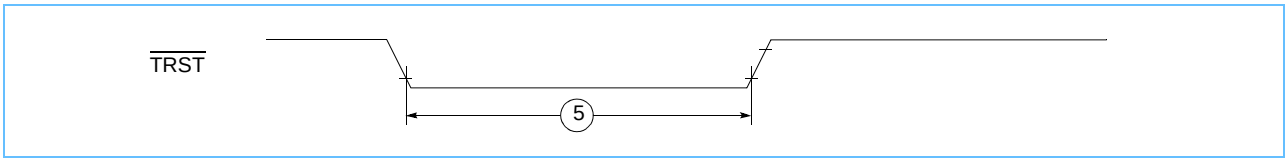


Figure 3-9 provides the boundary-scan timing diagram.

Figure 3-9. Boundary-Scan Timing Diagram

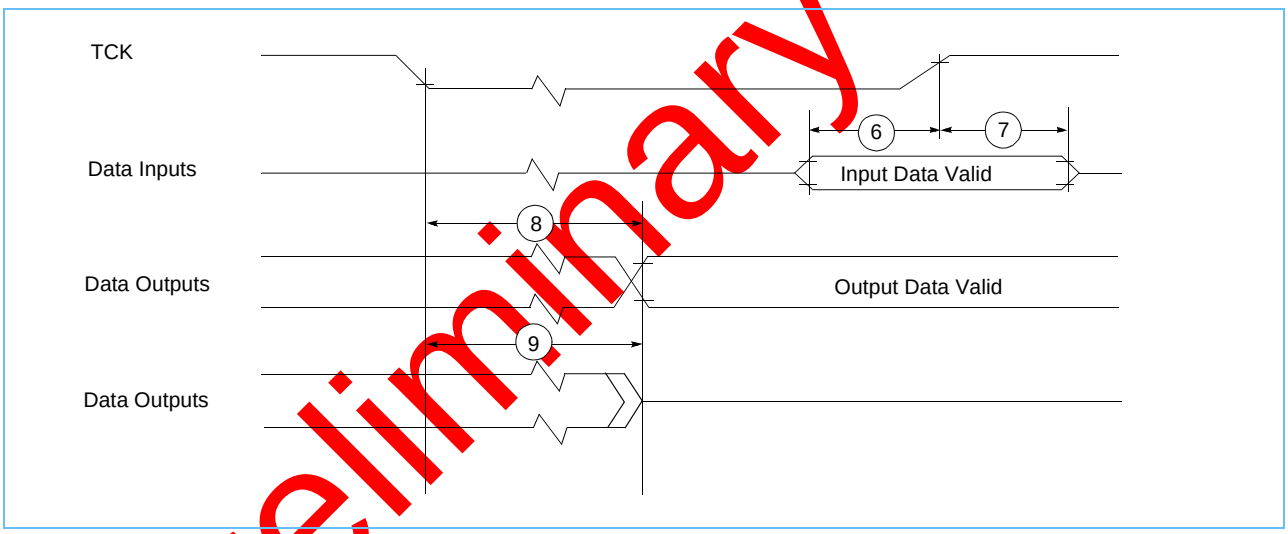
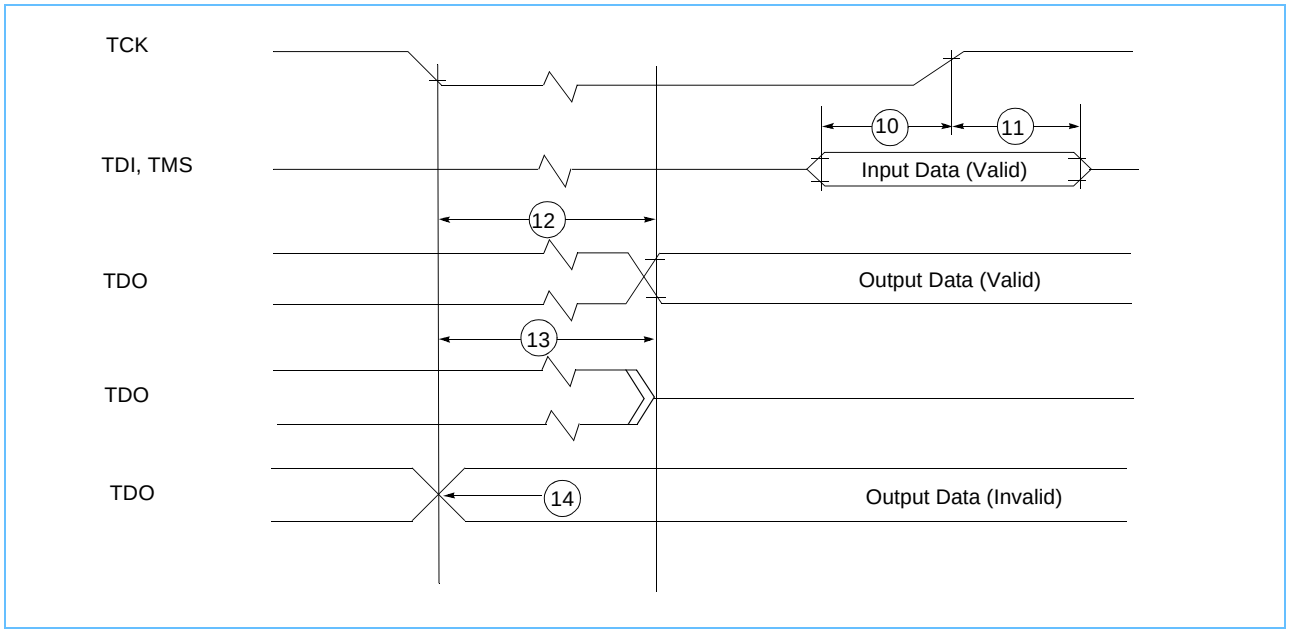


Figure 3-10 provides the test access port timing diagram.

Figure 3-10. Test Access Port Timing Diagram



4. Dimensions and Signal Assignments

IBM offers a plastic ball grid array (FC-PBGA) that supports 292 balls for the Broadway package. This is a signal and power compatible footprint to the PowerPC 750FX RISC Microprocessor module.

This section contains several views of the Broadway physical package and descriptions and listings of the signals and ball/pin locations. For more information about the physical layout of the Broadway, see *Table 4-2, Pinout Listing for the FC-PBGA Package ,,* on page 31.

Table 4-1 lists the drawings used in this section and the corresponding IBM package numbers. For the latest package information, obtain the current IBM drawings.

List of Drawings with IBM Package Numbers

Table 4-1. List of Drawings with IBM Package Numbers

For Figure...	See Page...	Package Number
Mechanical Dimensions and Bottom Surface Nomenclature of the FC-PBGA Package for DD1.0	38	TBD
Note: Use A01 corner designation for correct placement. Use the five plated dots that form a right angle (|_) to locate the A01 corner as shown in *Figure 4-3, Mechanical Dimensions and Bottom Surface Nomenclature of the FC-PBGA Package for DD1.0,* on page TBD.		

Figure 4-1. Mechanical Dimensions and Bottom Surface Nomenclature of the FC-PBGA Package for DD1.0

TBD

4.1 Package

4.1.1 Overview

FC-PBGA packages are suited for applications requiring much higher I/O counts and better electrical performance than that offered by EPBGA and HPBGA packages. They are recommended for applications having medium electrical performance and power dissipation requirements.

4.1.2 Features

- Low dielectric-constant organic build-up substrate
- Flip chip die attach; BGA second-level interconnect
- Two-layer core
- Up to eight discrete surface-mount dogbone or interdigitated decoupling capacitors (custom offering). Not all menu points support on-package capacitors.
- JEDEC-compliant packages

4.1.3 Package Cross-Section

Figure 4-2 FC-PBGA Two-Layer Core Package Cross Section and Figure 4-3 FC-PBGA Two-Layer Core Package Configuration show the predominant metal function on each layer.

Figure 4-2. FC-PBGA Two-Layer Core Package Cross Section

TBD

Figure 4-3. FC-PBGA Two-Layer Core Package Configuration

TBD

4.2 Mechanical Specifications

Figure 4-4. Mechanical Dimensions and Bottom Surface Nomenclature of the FC-PBGA Package for DD1.0

TBD

4.3 Microprocessor Ball Placement

Figure 4-5. PowerPC Broadway Microprocessor Ball Placement

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y
20	A6	A8	A3	A2	A0	DH31	DH25	DH26	NC	DH22	DH19	DH18	DH16	DH15	DH14	NC	DH9	DH10	DH4	DH2
19	A13	GND	A5	A4	A1	DH29	NC	DH28	DH23	DH24	DH21	DH20	NC	DH17	DH11	DH8	DH6	DH5	GND	DH3
18	A11	A10		**OVDD**	GND		**OVDD**	GND		VDD	VDD		GND	**OVDD**		GND	**OVDD**		DH0	PLL_CFG0
17	A12	TT1	**OVDD**		A9		DH30	DH27		GND	GND		DH12	DH13		DH1		**OVDD**	PLL_CFG1	PLL_CFG2
16	A14	A15	GND	NC	A7		GND	**OVDD**		**OVDD**	**OVDD**		**OVDD**	GND		DH7	PLL_CFG3	GND	SYSCLK	**TL**
15	TT3	TS				VDD									VDD				NC	**A1VDD**
14	TSIZ0	TT2	**OVDD**	TT0	GND		**OVDD**			GND	GND			**OVDD**		GND	NC	**OVDD**	PLL_CFG4	**AGND**
13	NC	TT4	GND	NC	VDD		GND	GND	VDD	VDD	VDD	VDD	GND	GND		VDD	LLSD_ MODE	GND	L2_TSTCLK	L1_TSTCLK
12	TA	TSIZ1				VDD		GND	GND			GND	GND		VDD				MCP	CHECKSTOP
11	TBST	TSIZ2	VDD	GND	**OVDD**	GND				VDD	VDD				GND	**OVDD**	GND	VDD	TLBI-SYNC	HRESET
10	TH	A16	VDD	GND	**OVDD**	GND				GND	GND				GND	**OVDD**	GND	VDD	TH	CKSTP
9	A18	A17				VDD		GND	VDD			VDD	GND		VDD				BVSEL	INT
8	AACK	NC	GND	A21	VDD		GND	GND	VDD	VDD	VDD	VDD	GND	GND		VDD	QREQ	GND	TH	QACK
7	A20	A19	**OVDD**	A24	GND		**OVDD**			GND	GND			**OVDD**		GND	PU	**OVDD**	ARTRY	SRESET
6	TH	A23				VDD									VDD				TEA	PU
5	A22	A26	GND	A25	A31		GND	**OVDD**		**OVDD**	**OVDD**		**OVDD**	GND		NC	WT	GND	TDO	DBG
4	A28	A27	**OVDD**		DL3		NC	DL13		GND	GND		DL23	DL26		CI		**OVDD**	BG	NC
3	A29	A30		**OVDD**	GND		**OVDD**	GND		VDD	VDD		GND	**OVDD**		GND	**OVDD**		DRTRY	BR
2	DL0	GND	DL2	DL6	DL5	DL11	DL10	DL12	DL16	DL15	DL19	DL20	DL22	DL27	DL28	TCK	DL30	TDI	GND	KVDD
1	DL1	NC	DL4	DL8	DL7	DL9	DL14	NC	DL18	DL17	DL21	NC	DL24	DL25	DL29	DL31	TRST	TMS	GBL	KGND

Note: This view is looking down from above the Broadway placed and soldered on the system board.

4.4 Pinout Listings

Table 4-2 contains the pinout listing for the Broadway FC-PBGA package.

Table 4-2. Pinout Listing for the FC-PBGA Package ,

Signal Name	Pin Number	Active	Input/Output	Notes
A[0:31]	E20, E19, D20, C20, D19, C19, A20, E16, B20, E17, B18, A18, A17, A19, A16, B16, B10, B9, A9, B7, A7, D8, A5, B6, D7, D5, B5, B4, A4, A3, B3, E5.	High	Input/Output	
$A1V_{DD}$	Y15	—	—	
$\overline{\text{AACK}}$	A8	Low	Input	
AGND	Y14	—	—	
$\overline{\text{ARTRY}}$	W7	Low	Input/Output	
$\overline{\text{BG}}$	W4	Low	Input	
$\overline{\text{BR}}$	Y3	Low	Output	
BVSEL	W9	—	Input	3
$\overline{\text{CHECKSTOP}}$	Y12	Low	Output	
$\overline{\text{CI}}$	T4	Low	Output	
$\overline{\text{CKSTP\_IN}}$	Y10	Low	Input	
$\overline{\text{DBG}}$	Y5	Low	Input	
DH[0:31]	W18, T17, Y20, Y19, W20, V19, U19, T16, T19, U20, V20, R19, N17, P17, R20, P20, N20, P19, M20, L20, M19, L19, K20, J19, K19, G20, H20, H17, H19, F19, G17, F20	High	Input/Output	
DL[0:31]	A2, A1, C2, E4, C1, E2, D2, E1, D1, F1, G2, F2, H2, H4, G1, K2, J2, K1, J1, L2, M2, L1, N2, N4, N1, P1, P4, P2, R2, R1, U2, T1	High	Input/Output	
$\overline{\text{DRTRY}}$	W3	Low	Input	
$\overline{\text{GBL}}$	W1	Low	Input/Output	
GND	B2, B19, C5, C8, C13, C16, D10, D11, E3, E7, E14, E18, F10, F11, G5, G8, G13, G16, H3, H8, H9, H12, H13, H18, J12, K4, K7, K10, K14, K17, L4, L7, L10, L14, L17, M12, N3, N8, N9, N12, N13, N18, P5, P8. P13, P16, R10, R11, T3, T7, T14, T18, U10, U11, V5, V8, V13, V16, W2, W19,	—	—	
$\overline{\text{HRESET}}$	Y11	Low	Input	
$\overline{\text{INT}}$	Y9	Low	Input	
L1_TSTCLK	Y13	High	Input	3

Notes:

1. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
2. OV_{DD} inputs supply power to the input/output drivers and V_{DD} inputs supply power to the processor core.
3. BVSEL and L1_TSTCLK select the input/output voltage mode on the 60x bus.
4. TCK must be tied high or low for normal machine operation.
5. No connect.
6. Pullup resistor to OV_{DD}.
7. Tied high to OV_{DD}.
8. Tied low to GND.
9. Kelvin V_{DD} and GND for voltage regulator sensing.

Table 4-2. Pinout Listing for the FC-PBGA Package (Continued),

Signal Name	Pin Number	Active	Input/Output	Notes
L2_TSTCLK	W13	High	Input	1
$\overline{\text{LSSD\_MODE}}$	U13	Low	Input	1
$\overline{\text{MCP}}$	W12	Low	Input	
OV_{DD}	C4, C7, C14, C17, D3, D18, E10, E11, G3, G7, G14, G18, H5, H16, K5, K16, L5, L16, N5, N16, P3, P7, P14, P18, T10, T11, U3, U18, V4, V7, V14, V17	—	—	2
PLL_CFG[0:4]	Y18, W17, Y17, U16, W14	High	Input	
$\overline{\text{QACK}}$	Y8	Low	Input	
$\overline{\text{QREQ}}$	U8	Low	Output	
$\overline{\text{SRESET}}$	Y7	Low	Input	
SYSCLK	W16	High	Input	
$\overline{\text{TA}}$	A12	Low	Input	
$\overline{\text{TBST}}$	A11	Low	Input/Output	
TCK	T2	High	Input	4
TDI	V2	High	Input	
TDO	W5	High	Output	
$\overline{\text{TEA}}$	W6	Low	Input	
$\overline{\text{TLBISYNC}}$	W11	Low	Input	
TMS	V1	High	Input	
$\overline{\text{TRST}}$	U1	Low	Input	
$\overline{\text{TS}}$	B15	Low	Input/Output	
TSIZ[0:2]	A14, B12, B11	High	Output	
TT[0:4]	D14, B17, B14, A15, B13	High	Input/Output	
V_{DD}	C10, C11, E8, E13, F6, F9, F12, F15, J8, J9, J13, K3, K8, K11, K13, K18, L3, L8, L11, L13, L18, M8, M9, M13, R6, R9, R12, R15, T8, T13, V10, V11	—	—	2
$\overline{\text{WT}}$	U5	Low	Output	
NC	W15, U14, Y4, D16, D13, A13, B8, T5, T20, N19, J20, G19, B1, G4, H1, M1	—	—	5
PU	Y6,U7	—	—	6
TH	W10, W8, A10, A6	—	—	7
TL	Y16	—	—	8

Notes:

1. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
2. OV_{DD} inputs supply power to the input/output drivers and V_{DD} inputs supply power to the processor core.
3. BVSEL and L1_TSTCLK select the input/output voltage mode on the 60x bus.
4. TCK must be tied high or low for normal machine operation.
5. No connect.
6. Pullup resistor to OV_{DD}.
7. Tied high to OV_{DD}.
8. Tied low to GND.
9. Kelvin V_{DD} and GND for voltage regulator sensing.

Table 4-2. Pinout Listing for the FC-PBGA Package (Continued),

Signal Name	Pin Number	Active	Input/Output	Notes
KGND	Y1	—	—	9
KV_{DD}	Y2	—	—	9

Notes:

1. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
2. OV_{DD} inputs supply power to the input/output drivers and V_{DD} inputs supply power to the processor core.
3. BVSEL and L1_TSTCLK select the input/output voltage mode on the 60x bus.
4. TCK must be tied high or low for normal machine operation.
5. No connect.
6. Pullup resistor to OV_{DD}.
7. Tied high to OV_{DD}.
8. Tied low to GND.
9. Kelvin V_{DD} and GND for voltage regulator sensing.

Table 4-3. Signal Listing for the FC-PBGA Package

Signal Name	Pin Count	Active	Input/Output	Notes
TBD	TBD	TBD	TBD	TBD
Notes:				

Table 4-4. Signal Locations

Signal	Ball Location	Signal	Ball Location	Signal	Ball Location	Signal	Ball Location
TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Table 4-5. Voltage and Ground Assignments

$A1V_{DD}$	$A2V_{DD}$	OV_{DD}	OV_{DD}	V_{DD}	V_{DD}	GND	GND
TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

5. System Design Information

This section provides electrical and thermal design recommendations for successful applications on the Broadway.

5.1 PLL Configuration

Table 5-1 shows the PLL configuration for the Broadway for nominal frequencies.

Table 5-1. Broadway Microprocessor PLL Configuration

PLL_CFG [0:4]		Processor to Bus Frequency Ratio (PTBFR)	Frequency Range Supported by VCO Having an Example Range of...			
			SYSCLK[1] (MHz)		Core (MHz)	
Binary	Decimal		Minimum ($SYSCLK_{MIN}$)	Maximum ($SYSCLK_{MAX}$)	Minimum ($Core\ Frequency_{MIN}$)	Maximum ($Core\ Frequency_{MAX}$)
00100	4	2×	200	243	400	486
00101	5	2.5×	160	243	400	608
00110	6	3×	133	243	400	729
00111	7	3.5×	114	229	400	800
01000	8	4×	100	200	400	800
01001	9	4.5×	89	178	400	800
01010	10	5×	80	160	400	800
01011	11	5.5×	80	145	440	800
01100	12	6×	80	133	480	800
01101	13	6.5×	80	123	520	800
01110	14	7×	80	114	560	800
01111	15	7.5×	80	107	600	800
10000	16	8×	80	100	640	800
10001	17	8.5×	80	94	680	800
10010	18	9×	80	89	720	800
10011	19	9.5×	80	84	760	800
10100	20	10×	80	80	800	800
10101	21	11×	N/A	N/A	N/A	N/A
10110	22	12×	N/A	N/A	N/A	N/A
10111	23	13×	N/A	N/A	N/A	N/A
11000	24	14×	N/A	N/A	N/A	N/A
11001	25	15×	N/A	N/A	N/A	N/A

Notes:

1. The SYSCLK frequency equals the core frequency divided by the processor-to-bus frequency ratio (PTBFR).
2. In clock-off mode, no clocking occurs inside the Broadway regardless of the SYSCLK input.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use only.
   The AC timing specifications given in the document do not apply in PLL-bypass mode.

Table 5-1. Broadway Microprocessor PLL Configuration (Continued)

PLL_CFG [0:4]		Processor to Bus Frequency Ratio (PTBFR)	Frequency Range Supported by VCO Having an Example Range of...			
			SYSCLK[1] (MHz)		Core (MHz)	
Binary	Decimal		Minimum ($SYSCLK_{MIN}$)	Maximum ($SYSCLK_{MAX}$)	Minimum ($Core\ Frequency_{MIN}$)	Maximum ($Core\ Frequency_{MAX}$)
11010	26	16×	N/A	N/A	N/A	N/A
11011	27	17×	N/A	N/A	N/A	N/A
11100	28	18×	N/A	N/A	N/A	N/A
11101	29	19×	N/A	N/A	N/A	N/A
11110	30	20×	N/A	N/A	N/A	N/A
11111	31	Off[2]	N/A	N/A	N/A	N/A

Notes:

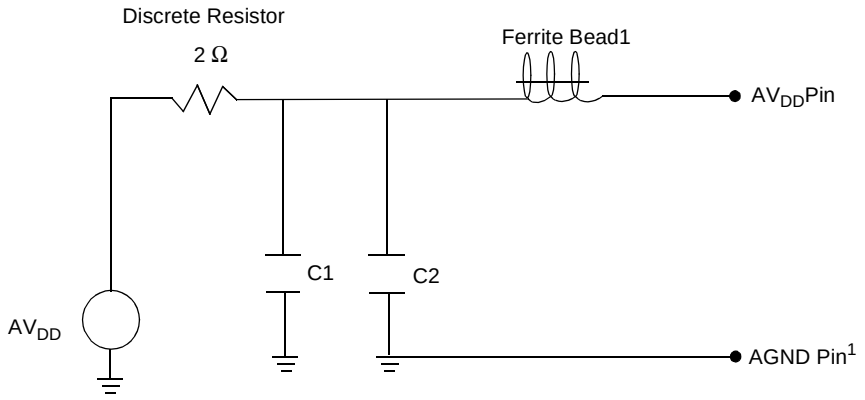
1. The SYSCLK frequency equals the core frequency divided by the processor-to-bus frequency ratio (PTBFR).
2. In clock-off mode, no clocking occurs inside the Broadway regardless of the SYSCLK input.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use only.
   The AC timing specifications given in the document do not apply in PLL-bypass mode.

5.2 PLL Power Supply Filtering

The Broadway microprocessor has an AV_{DD} signal which provides power to the clock generation PLL.

To ensure stability of the internal clock, the power supplied to the AV_{DD} input signals should be filtered using a circuit similar to the one shown in *Figure 5-1* on page 37. The circuit should be placed as close as possible to the AV_{DD} pin to ensure it filters out as much noise as possible.

Figure 5-1. PLL Power Supply Filter Circuit



Item	Description/Value
Resistor	2 Ω
C1	0.1 µF Ceramic
C2	10.0 µF Ceramic
Ferrite Bead	30 Ω (typical) - Murata BLM21P300S or similar

Notes:
1. Connected to ground without a filter.

5.3 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD}. Unused active high inputs should be connected to GND. All no-connect (NC) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, OV_{DD}, AV_{DD}, and GND pins of the Broadway.

5.4 Output Buffer DC Impedance

The Broadway 60x drivers were characterized over various process, voltage, and temperature conditions. To measure driver impedance, an external resistor is connected to the chip pad, either to OV_{DD} or GND. Then the value of such resistor is varied until the pad voltage is $OV_{DD}/2$ (see *Figure 5-2*).

The output impedance is actually the average of two resistances: the resistance of the pull-up and the resistance of pull-down devices. When Data is held high, SW1 is closed (SW2 is open), and R_N is trimmed until Pad = $OV_{DD}/2$; R_N then becomes the resistance of the pull-up devices. When Data is held low, SW2 is closed (SW1 is open), and R_P is trimmed until Pad = $OV_{DD}/2$; R_P then becomes the resistance of the pull-down devices. With a properly designed driver, R_P and R_N are close to each other in value; then driver impedance equals $(R_P + R_N)/2$.

Figure 5-2. Driver Impedance Measurement

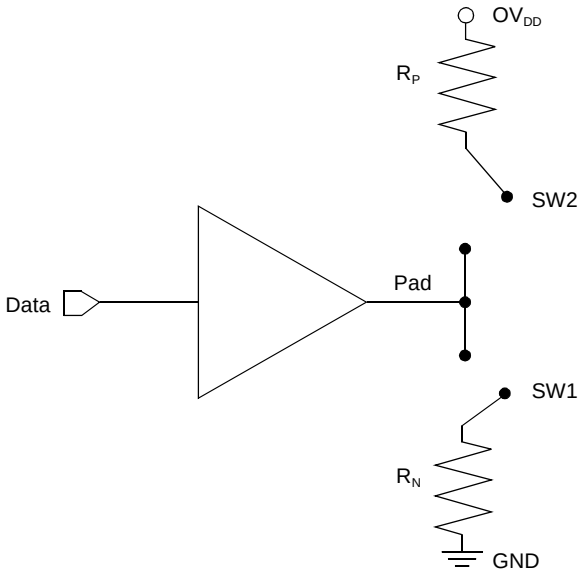


Table 5-2 summarizes the driver impedance characteristics a designer uses to design a typical process.

Table 5-2. Driver Impedance Characteristics

Process	60× Impedance (Ω)	OV_{DD} (V)
Worst	57	1.20
Typical	50	1.20
Best	46	1.20

5.4.1 Input/Output Usage

Table 5-3, Input/Output Usage, on page 40 provides details on the input/output usage of the IBM PowerPC Broadway RISC Microprocessor signals. The *Usage Group* column refers to the general functional category of the signal.

In the IBM PowerPC Broadway RISC Microprocessor, certain input/output signals have pullups and pulldowns, which may or may not be enabled. In *Table 5-3,* the “Input/Output with Internal Pullup Resistors” column defines which signals have these pullups or pulldowns and their active or inactive state. The “Level Protect” column defines which signals have the designated function added to their Input/Output cell. For more about level protection, see *Section 5.5.1* on page 41.

Caution: This section is based on preliminary information and is subject to change.

Table 5-3. Input/Output Usage

Broadway Signal Name	Active Level	Input/ Output	Usage Group	Input/Output with Internal Pullup Resistors	Level Protect	Required External Resistor	Comments	Notes
TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

5.5 Operational and Design Considerations

5.5.1 Level Protection

A level protection feature is included in the IBM PowerPC Broadway RISC Microprocessor. This feature prevents ambiguous floating reference voltages by pulling the respective signal line to the last valid or nearest valid state.

For example, if the input/output voltage level is closer to OV_{DD}, the circuit pulls the I/O level to $OV_{DD.}$ If the I/O level is closer to GND, the I/O level is pulled low. This self-latching circuitry *keeps* the floating inputs defined and avoids meta-stability. In *Table 5-3, Input/Output Usage,* on page 40, these signals are defined as “keeper” in the “Level Protect” column.

The level protect circuitry provides no additional leakage current to the signal I/O; however, some amount of current must be applied to the *keeper* node to overcome the level protection latch. This current is process dependent, but in no case is the current required over 100 µA.

This feature allows the system designer to limit the number of resistors in the design and optimize placement and reduce costs.

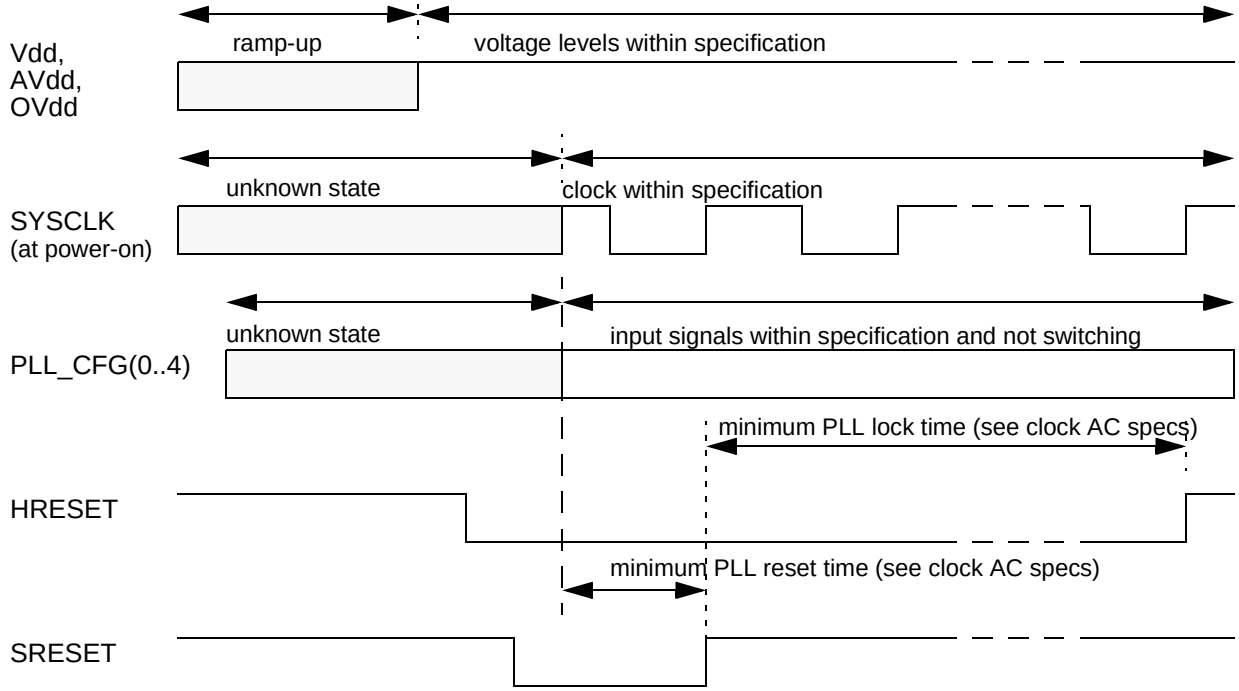
Note: Having a *keeper* on the associated signal I/O does not replace a pull-up or pull-down resistor that is needed by a separate device located on the 60x bus. The designer must supply any termination requirements for these separate devices, as defined in their specifications.

5.5.2 Adjusting the processor clock frequency

The Broadway processor generates an internal clock that is a frequency multiple of the external system clock, SYSCLK, using an internal phase-lock loop (PLL) circuit. The PLL circuit must generate a stable internal clock before executing microprocessor instructions. Consequently, any time the PLL clock frequency is changed, a proper reset sequence of the processor is required.

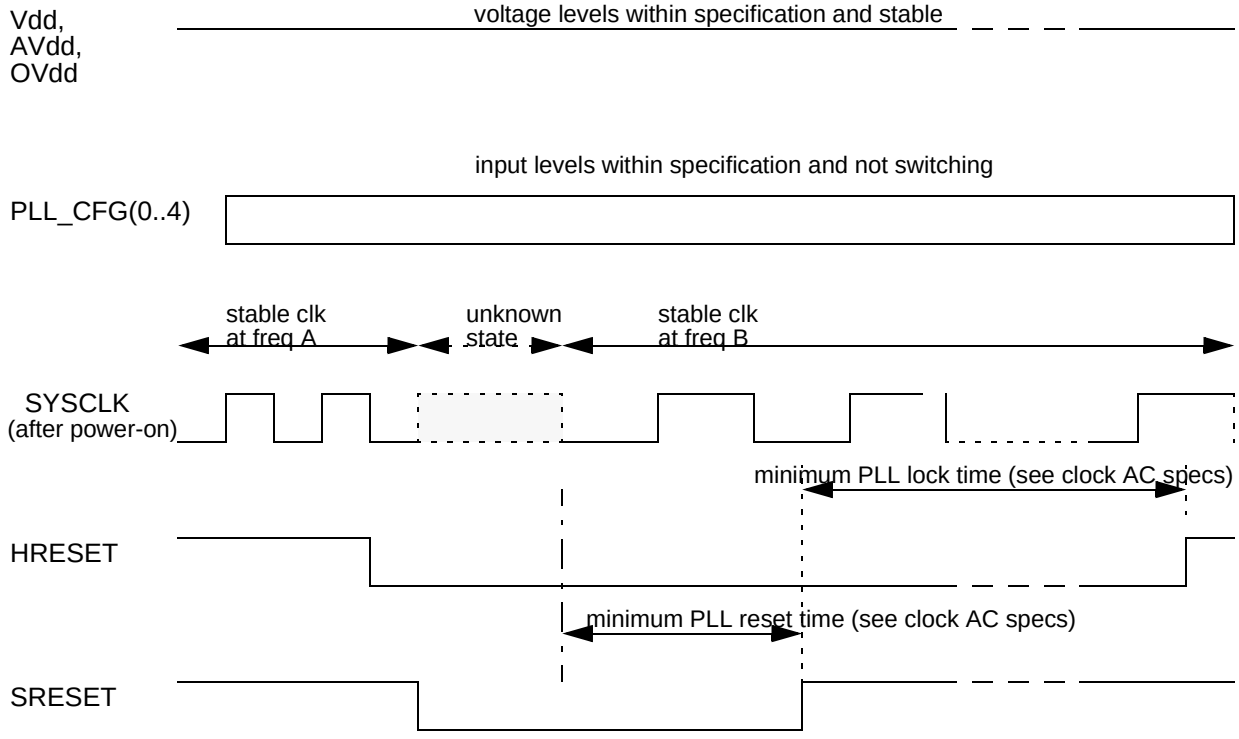
At power up, the voltage applied to the processor through the Vdd, AVdd, and OVDD pins must be within specification prior to asserting processor reset, HRESET. When HRESET is asserted, SRESET is pulsed to reset the PLL and start it syncronizing to SYSCLK with the clock multiple selected by the PLL_CFG pins. After the pulse on SRESET, HRESET is held asserted a mininum100usec to allow the PLL to stabilize. This process is illustrated in *Figure 5-3 Selection of Processor Frequency at Power-On*.

Figure 5-3. Selection of Processor Frequency at Power-On



After power-up and PLL stabilization, the PLL frequency may be changed by adjusting the frequency of the external SYSCLK. The reset procedure previously described is used, whereby the SYSCLK frequency is changed while SRESET is asserted. Once the SYSCLK frequency stabilizes, then SRESET may be de-asserted. This is illustrated in *Figure 5-4 Control Sequence for Switching Processor Clock Frequency*.

Figure 5-4. Control Sequence for Switching Processor Clock Frequency



5.5.3 Configuring the Processor During Reset

Operating modes of the processor such as data bus width, drtry mode, etc. are selected when the processor exits reset mode (i.e. when HRESET is deasserted). Specifically, selected pins are sampled when HRESET transitions to the de-asserted state and the sampled value determines the operating mode. The mode select pins and their descriptions follow.

Table 5-4. Summary of Mode Select

Mode	Broadway
32-bit mode	Sample TLBISYNC to select High = 64-bit mode Low = 32-bit mode
Data retry mode	Selects DRTRY mode. 0 at HRESET transition No DRTRY mode 1 at HRESET transition DRTRY mode
Standard/extended precharge mode	QACK in a logical high state at the transition of HRESET from asserted to negated enables standard precharge mode, the recommended default. See *Section 5.5.4.1* for details.

5.5.4 64-Bit or 32-Bit Data Bus Mode

The typical operation for the Broadway DD1.X revision level is considered to be in 64-bit data bus mode. Mode setting is determined by the state of the mode signal, TLBISYNC, at the transition of HRESET from its active to inactive state (low to high). If TLBISYNC is *high* when HRESET transitions from active to inactive, 64-bit mode is selected. If TLBISYNC is *low* when HRESET transitions from active to inactive, 32-bit mode is selected.

5.5.4.1 Precharge Duration Selection and Application

An extended precharge feature is available for the signals ABB, DBB, and ARTRY in situations where the loading and net topology of these signals requires a longer precharge duration for the signals to attain a valid level.

This feature has not been fully tested and should not be necessary in a properly designed system, even at 200 MHz. System designers should assume standard precharge as the default selection, with an option to use extended precharge.

The bus signals, ABB, DBB, and ARTRY, require a precharge to the inactive state (bus high) before going to tristate. The precharge duration in standard precharge mode is approximately one half cycle, and should be used for systems with point-to-point topologies. Extended precharge mode increases the precharge duration to one cycle. This increase may be required for bus speeds approaching 200 MHz when bus loading is high.

QACK in a logical high state at the transition of HRESET from asserted to negated enables standard pre-charge mode in the Broadway. QACK in a logical low state at the transition of HRESET from asserted to negated enables extended pre-charge mode in the Broadway.

5.6 JTAG Test Access Port (TAP) Operation

Broadway supports the IEEE 1149.1 standard, “IEEE Standard Test Access Port and Boundary-Scan Architecture”. The standard defines a five-pin interface that is used to perform functions such as continuity testing between components on boards and system debug. Data is serially shifted into the processor through the TDI pin and shifted out of the processor through the TDO pin. The scan operations can be divided into two categories: instruction scan and data scan operations. The operations or modes are selected using the TMS pin. Finally, all scanning and mode selection is performed synchronously with respect to the clock pin, TCK.

This section details the IEEE 1149.1 operations supported by the Broadway processor and also recommendations for system design to support system debug using the TAP interface. For additional details, please refer to the IEEE 1149.1 document.

5.6.1 Interface Pins

A brief description of the five dedicated pins comprising the Test Access Port (TAP) are given below. These pins do not have an associated boundary scan cell.

Table 5-5. TAP Pins

Pin	Input/Output	Weak Pullup	Mandatory TAP Pin	Function
TDI	Input	Yes	Yes	Serial Scan input pin
TDO	Output	No	Yes	Serial Scan output pin
TMS	Input	Yes	Yes	TAP controller mode pin
TCK	Input	No	Yes	Scan clock
TRST	Input	Yes	No	TAP controller reset

TRST_ is an optional pin, but it is required for Broadway to reset the TAP controller on a power-on reset (POR). The 1149.1 standard requires a weak pullup only on the TRST_ pin, but in the Broadway, weak pullups are provided to most TAP input pins such that the Broadway will function normally with the TAP pins unconnected. However, it is recommended to tie the TDI and TMS input pins high and TRST_ low when they are not in use for greater system reliability.

5.6.2 Supported IEEE 1149 JTAG Instructions and Data Registers

5.6.2.1 Instructions

Broadway supports the three required JTAG instructions; Bypass, Sample/Preload and Extest. plus the optional HIGHZ and CLAMP JTAG instructions. The 8-bit hexadecimal encoding for these instructions is shown in the table below. Hexadecimal encodings not included in the table are reserved for other functions.

JTAG instructions are scanned in serially (LSB bit first) into an 8 bit TAP controller instruction register via the TDI pin. Please consult the IEEE 1149.1 standard for details regarding loading the jtag instructions using the TAP.

Table 5-6. Instruction Encodings

Instruction	Encoding	Description
EXTEST	X'00'	JTAG extest instruction
SMPL_PLD	X'C0'	JTAG sample/preload instruction
HIGHZ	X'F0'	JTAG HIGHZ instruction
CLAMP	X'F1'	JTAG CLAMP instruction
BYPASS	X'FF'	JTAG bypass instruction

The instruction register output is forced to the Bypass instruction (all 1s) if the TAP controller is in the Test_Logic_Reset state or if TRST_ is active**.**

5.6.2.2 Data Registers

Broadway supports the Bypass and Boundary Scan data registers. When selected with the corresponding JTAG instruction (as shown in the table below), the register is inserted between the TDI and TDO TAP pins and may be scanned when the TAP controlled is in "Shift-DR" state to control or observe Broadway input and output states. Please consult the IEEE 1149.1 specification for details on manipulation of the data registers. An industry-standard boundary scan design language (i.e. BSDL) file will be created for Broadway with specific information on the boundary scan latch size and organization. This document can be used to create card level connectivity tests between components.

Table 5-7. JTAG Instructions

Data Register	Instruction	TAP State	Scan Clock	Data Register Length
Bypass register	Bypass	Shift-DR	TCK	1
Boundary scan register	Sample/preload or extest	Shift-DR	TCK	TBD

Bypass Register

The Bypass register is required by the 1149.1 standard. This is a single bit register that is used to bypass the Broadway This feature allows a shorter system data scan string when scanning an entire system board in which the Broadway boundary scan string is a part of a larger system data scan string.

Boundary Scan Register

Boundary scan register allow system board trace tests, and access to the pins where physical access is difficult. Basically a latch is placed on inputs to capture data and a latch is placed on outputs to force data. Additional latches may be needed to configure bidirectional pins as either inputs or outputs and also enable or disable tri-state outputs. All these latches, or boundary scan cells, are serially connected to comprise the boundary scan register.

Not all pins of the Broadway have an associated boundary scan cell. The 5 TAP pins and the dedicated test pins do not have a boundary scan cell.

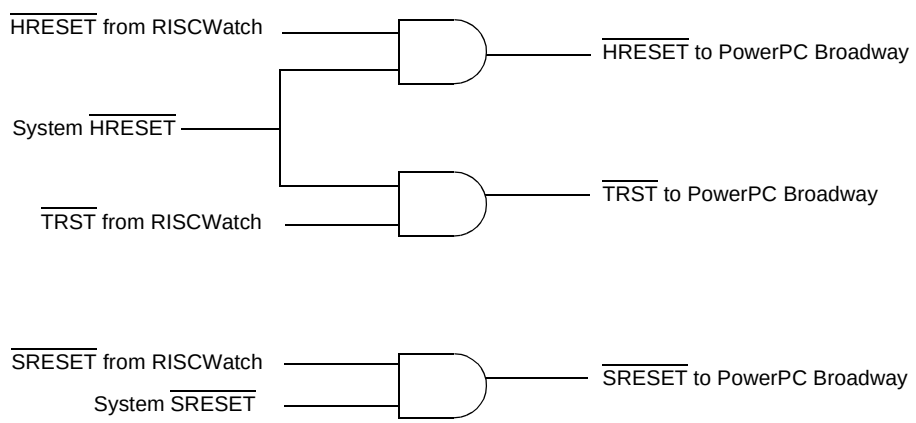
An industry-standard boundary scan design language (i.e. BSDL) file will be created for Broadway with specific information on the boundary scan register size and individual cell placement and function. This document can then be used to create card level connectivity tests between components

5.6.3 5.8.3 Recommendations to Support System Debug

The TAP interface also allows functions such as observation and control of Broadway general-purpose registers, cache contents, 60x bus cycles, etc., using the IBM RISCwatch debug tool. To simplify system debug, the following system design recommendations are offered to allow use of RISCwatch and other diagnostic tools.

HRESET_, SRESET_, and TRST_ are signals used for RISCwatch to enable proper operation of the tool. Logical 'AND' gates should be placed between these signals and the IBM Broadway RISC microprocessor as shown below.

Figure 5-5. IBM RISCWatch JTAG to $\overline{\text{HRESET}}$, $\overline{\text{TRST}}$, and $\overline{\text{SRESET}}$ Signal Connector



Note: See notes for *Table 5-3, Input/Output Usage,* on page 40.

5.6.3.1 Processor Debug System Enablement when Implementing Precharge Selection

System designers who want to use a processor debug system attached to the Broadway IEEE 1149.1 test access port (TAP) interface (such as the IBM RISCWatch debug system) should provide a method to assert QACK after the transition of HRESET. Debug systems use a "soft stop" feature to stop the processor, allow processor internal states to be read, and then restart of the processor. A soft stop requires the system to be in a quiescent state before the processor can be queried for internal state values. This is accomplished by the assertion of a quiescent request (that is, QREQ is asserted) and subsequent acknowledgement (that is, QACK is asserted). Systems that do not use the power management features; doze, nap, and sleep; and do not require the extended pre-charge feature can drive the QACK pin with an inverted version of HRESET.

Revision Log

Date	Description
January 17, 2005	Initial advance release (version 0.1).
February 16, 2005	Updated advance release (version 0.2). Changed *Table 2-1. Broadway General Parameters.* Changed *Table 3-1. Recommended Operating Conditions.* Changed *Table 3-3. DC Electrical Specifications.* Changed *Table 3-4. Power Consumption.* Changed note 2 in *Table 3-5. Clock AC Timing Specifications.* Changed *Table 3-5. Clock AC Timing Specifications.* Changed *Figure 3-1. SYSCLK Input Timing Diagram.*
February 24, 2005	Updated advance release (version 0.3). Changed *Table 3-1. Recommended Operating Conditions.* Changed *Table 3-4. Power Consumption.*