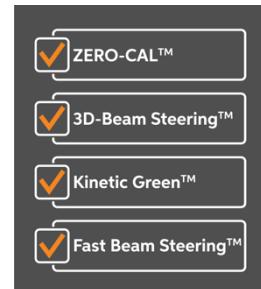
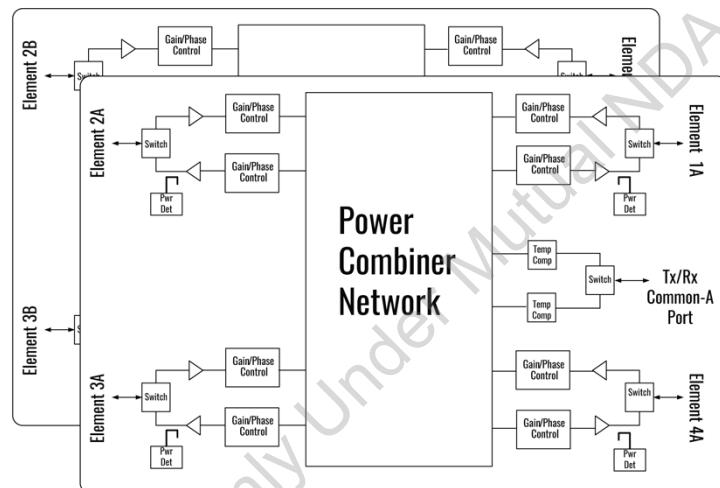


Product Features

- 37 – 40 GHz operation
- Supports 4 dual-pol radiating elements
- Tx/Rx half duplex operation
- Tx output power (VDDPA=2V):
 - +10.5 dBm @ 3% EVM
 - +18.5 dBm @ P1dB
- 21 dB Tx gain
- 30 dB Rx coherent gain*
- 3.8 dB Rx coherent NF*
- -25 dBm Rx coherent IIP3 (adjustable)
- 6-bit phase control (LSB=5.6 deg)
- 5-bit gain control (LSB=0.5 dB)
- Fast beam steering
- Telemetry reporting
- 5.2 mm x 4.0 mm WLCSP
- Single 1.8V supply operation with 2.0V PA option
- 3.1W Tx mode quiescent power dissipation
- 1.2W Rx mode power dissipation



Applications

5G communications antenna arrays

General Description

The AWMF-0159 is a highly-integrated silicon quad-core dual-pol IC intended for 5G phased array applications. The IC has eight antenna ports that can be connected to four dual-pol antenna elements to support both horizontal and vertical polarizations in a phased array. Two common ports, one for each polarization, enable simultaneous processing of both polarizations. The device includes all requisite beam steering controls for phase and gain control, and operates in half duplex fashion to enable a single antenna to support both Tx and Rx operation. The device provides 21 dB gain and +10.5 dBm linear output power during transmit mode and 30 dB coherent gain, 3.8 dB NF, and -25 dBm IIP3 during receive mode. Additional features include gain compensation over temperature, temperature reporting, Tx power telemetry, and fast beam switching using on-chip beam weight storage registers. The device features ESD protection on all pins, operates from 1.8 V supply, and is packaged in a 5.2 mm x 4.0 mm WLCSP (wafer level chip scale package) for easy flip chip installation in planar phased array antennas.



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n260 Band 5G Tx/Rx Dual-Pol Quad Core BFIC

AWMF-0159

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Table 1: Table of Contents

n260 Band 5G Tx/Rx Dual-Pol Quad Core BFIC

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Specifications

Electrical Specifications

$T_{case} = 25^\circ\text{C}$; all RF ports are single-ended and terminated in 50Ω , and 1.8V unless otherwise noted.

Parameter	Test Conditions/Comments	Min	Typ	Max	Units
General					
Frequency Range		37		40	GHz
# Channels	8 channel; Dual polarization 2T2R		4		
SPI Clock Rate				100	MHz
Beam Steering					
Phase-Shift Resolution	6-bit control		5.6		deg
RMS Phase Error			3		deg
Phase Control Range			360		deg
Gain Control Resolution	4-bit control in element and common arms		0.5		dB
Gain Control Range	See SPI Control on page 6 of this document		15		dB
RMS Gain Error			0.4		dB
TDD Switching Time	Measured from 50% timing edge to RF signal within 90%/10% of final level		250		ns
Transmit Mode					
Gain			21		dB
Output P1dB (at each channel)	VDDPA = 1.8 V		17.5		dBm
	VDDPA = 2.0 V		18.5		
Output Power at 3% EVM (at each channel)	5GNR 64QAM 100MHz; VDDPA = 1.8 V		9.5		dBm
	5GNR 64QAM 400MHz; VDDPA = 1.8V		9.5		dBm
	5GNR 64QAM 100MHz; VDDPA = 2.0 V		10.5		dBm
	5GNR 64QAM 400MHz; VDDPA = 2.0 V		10.0		dBm
ACLR at 3% EVM	5GNR 64QAM 100MHz; VDDPA = 1.8V/2.0V		-36		dBc
	5GNR 64QAM 400MHz; VDDPA = 1.8V/2.0V		-32		dBc
IC Total Power Dissipation (sum of all channels)	Quiescent (no RF input); VDDPA = 1.8V		3.1		W
	5GNR 64QAM 100MHz, 3% EVM; VDDPA = 1.8V		3.6		W
	5GNR 64QAM 400MHz, 3% EVM; VDDPA = 1.8V		3.6		W
	P1dB output; VDDPA = 1.8V		4.6		W
	Quiescent (no RF input); VDDPA = 2.0 V		3.4		W
	5GNR 64QAM 100MHz, 3% EVM; VDDPA = 2.0V		4		W
	5GNR 64QAM 400MHz, 3% EVM; VDDPA = 2.0V		4		W
	P1dB output; VDDPA = 2.0V		5.3		W
Noise Figure			19		dB

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Parameter	Test Conditions/Comments	Min	Typ	Max	Units
Receive Mode					
Coherent Gain ¹			30		dB
Coherent Noise Figure ¹			3.8		dB
Coherent IIP3 ¹			-25		dBm
IC Total Power Dissipation	Sum of all channels		1.2		W
Other					
Operating Temperature Range	Temperature at die backside	-40		+105	°C
Θ_{JC} ²	Junction-to-case thermal resistance		15		°C/W

Table 2: Electrical Specifications

¹Coherent gain (CG) is the RF gain with all Rx input ports energized and is most useful for assessing RF power handling in the beam forming network. Electronic gain (EG) is the RF gain exclusive of the 4:1 sum and is most useful for cascaded NF and gain calculation. The total gain of the antenna aperture can be calculated from EG + 10*log(n), where n is the number of antenna elements in the array. Single path gain (SPG) is the RF gain with only one input port energized. This is representative of the RF gain measured in a 2-port measurement system, such as with the Developer's Kit.
 $CG = SPG + 12 \text{ dB} = EG + 6 \text{ dB}$ for a quad IC.

Coherent Noise Figure and IIP3 is the noise figure/IIP3 obtained when all input ports are energized and coherently combined.

² Θ_{JC} assumes a heat sink is on the back of the die.

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RMS Phase and Amplitude Equations

To normalize to the 0 state, the following equation is used:

$$\varphi_0(n) = \varphi(n) - \varphi(0) \text{ (Phase)}$$

$$A_0(n) = A(n) - A(0) \text{ (Amplitude)}$$

Note: n is the nth state of the phase shifter or attenuator. For the phase shifter used in the AWMF-0159, values for n are from 0 to 63; for the attenuator used in the AWMF-0159, values for n are from 0 to 15.

To calculate the error for each state, the following equation is used:

$$\varphi_{err}(n) = \varphi_0(n) - n\Delta \text{ (Phase)}$$

$$A_{err}(n) = A_0(n) - n\Delta \text{ (Amplitude)}$$

Note: Δ is the LSB of the phase shifter or attenuator. For the phase shifter used in the AWMF-0159, the value for Δ is 5.625° ; for the attenuator used in the AWMF-0159, the value for Δ is 0.5 dB.

To calculate the Mean phase or amplitude error, the following equation is used:

$$\varphi_{errM} = \text{mean}(\varphi_{err}(n)) \text{ (Phase)}$$

$$A_{errM} = \text{mean}(A_{err}(n)) \text{ (Amplitude)}$$

To calculate the RMS error the following equation is used:

$$\varphi_{rms} = \sqrt{\text{mean}((\varphi_{err}(n) - \varphi_{errM})^2)} \text{ (Phase)}$$

$$A_{rms} = \sqrt{\text{mean}((A_{err}(n) - A_{errM})^2)} \text{ (Amplitude)}$$

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IC Control

All gain specifications are at 25°C die backside temperature and 0 dB beam weight setting. Beam weight gain control range is 7.5 dB in each element arm and 7.5 dB in the common arm for a total of 15 dB; this gain control range is not used for temperature compensation.

The AWMF-0159 features temperature compensation of gain across -40°C to 105°C die backside temperature range. Both manual and automatic temperature compensation modes are supported.

The AWMF-0159 has 4 operating modes defined by the states of the RX_EN and TX_EN input pins. Table 3 summarizes these modes.

Mode	RX_EN	Tx_EN	Description
Stand-by	0	0	RF circuits powered down. Fast switching to Tx/Rx modes.
Tx Mode	0	1	Transmit mode.
Rx Mode	1	0	Receive mode.
Sleep	1	1	RF/bias circuits powered down. Low power dissipation. Slow switching to Tx/Rx modes.

Table 3: AWMF-0159 Operating Mode

Example data for power detector output vs. transmit output power is shown below in Figure 1. The ADC value is returned by the Telemetry read and can be converted to power using this graph.

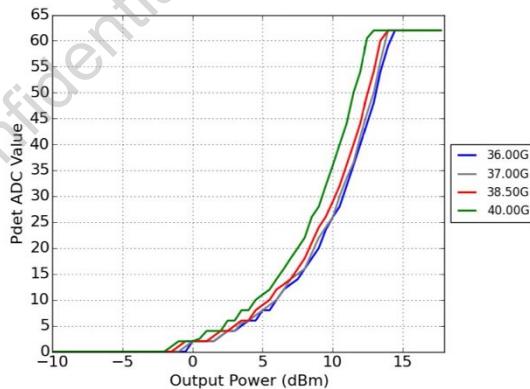


Figure 1: AWMF-0159 Power Detector Characteristics

For details of the digital control interface and features, please refer to the SPI Users Guide.

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— TDD Switching Performance

The switching time performance of the AWMF-0159 for different modes is summarized in Table 4. The timing is measured from 50% timing edge to RF signal within 90%/10% of final level. A 25ns guard period is recommended between Tx_EN and Rx_EN transitions to avoid both signals being high at the same time during switching which would inadvertently result in the IC going into sleep mode.

Start State	Finish State	Signal Level	Typ (ns)
Standby	Rx	Rx_EN r50% -> RF r90%	115
Rx	Standby	Rx_EN f50% -> RF f10%	10
Sleep	Rx	Rx_EN r50% -> RF r90%	450
Rx	Sleep	Rx_EN f50% -> RF f10%	5
Tx	Rx	Rx_EN r50% -> RF r90%	110
Standby	Tx	Tx_EN r50% -> RF r90%	180
Tx	Standby	Tx_EN f50% -> RF f10%	10
Sleep	Tx	Tx_EN r50% -> RF r90%	360
Tx	Sleep	Tx_EN f50% -> RF f10%	10
Rx	Tx	Tx_EN f50% -> RF r90%	200

Table 4: TDD Switching Performance

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Recommended Operating Conditions

Parameter	Pin-Out Symbol	Min	Typ	Max	Unit	Comment
Power Supply	VDD	1.75	1.8	1.85	V	
PA Power Supply	VDDPA_xx	1.75	2.0	2.05	V	See Note 3
SPI Input Negative Going Threshold Voltage	SPI_xx, TX_EN, RX_EN	0.3*VDD	-	0.6*VDD	V	
SPI Input Positive Going Threshold Voltage	SPI_xx, TX_EN, RX_EN	0.4*VDD	-	0.7 *VDD	V	Compliant with JESD8-7A standard
SPI Input Hysteresis Voltage		0.1*VDD	-	0.4*VDD	V	

³Note: Tx output power increases with PA Power Supply

Table 5: Recommended Operating Conditions

Power Consumption

All VDD pins connected together on PCB.

Operating Mode	Power Supply (V)		Typical Total IC Current (mA)		Typ. Total IC Power Consumption (W)
	Vdd_1P8	VDDPA	Vdd_1P8	VDDPA	
RX	1.8	1.8	664	1	1.2
TX (Quiescent)	1.8	1.8	440	1300	3.1
	1.8	2.0	440	1310	3.4
TX (at 9.5 dBm)	1.8	1.8	452	1520	3.6
Tx (at 10.5 dBm)	1.8	2.0	452	1550	4.0
Standby	1.8	1.8	18	1	0.034
Sleep	1.8	1.8	5	1	0.011

Table 6: Power Consumption

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Absolute Maximum Ratings

Parameter	Rating
VDD_1P8	2 V
VDDPA	2.2 V
Logic Level	2 V
RF Input Level – all ports	0 dBm
ESD Sensitivity, CDM	250V
ESD Sensitivity, HBM	1000V
Reflow Temperature (Maximum Peak)	260 °C
MSL Rating	1
Maximum Junction Temperature	175 °C
Storage Temperature	150 °C

Table 7: Absolute Maximum Ratings

Note: Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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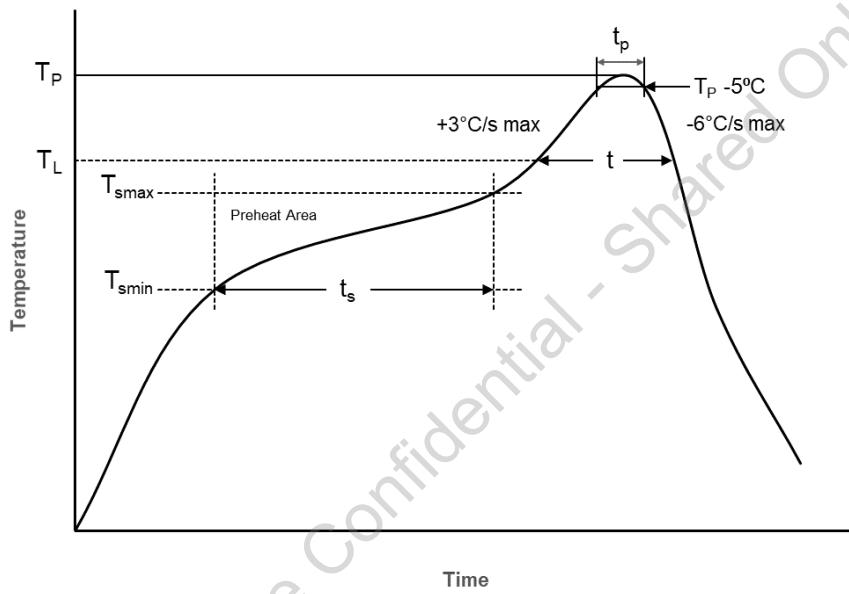
AWMF-0159

WLCSP Soldering Recommendations

Anokiwave's WLCSP product family is classified as Moisture Sensitivity Level 1 (MSL=1) with a maximum component temperature of 260°C ($T_c=260^\circ\text{C}$) per IPC/JEDEC J-STD-020E, Figure 1. The SAC405 solder balls are compatible with standard lead-free reflow profiles. Customers should consult with their SMT subcontractor or internal expert to define a solder paste, solder volume and stencil that supports both fine pitch WLCSP devices and the remaining components of their assembly.

Fine Pitch Process Considerations

A high-quality stencil and lead-free solder paste with T4 or T5 mesh size is recommended. Both no-clean and water-soluble solder pastes are acceptable. Good results have been obtained using a 0.1mm thick Nano Gold Coat stencil with a 0.216mm diameter opening and AIM NC258 T4 solder paste. Process development should include pre-reflow measurement of solder paste volume to understand stencil release and post reflow x-ray inspection to detect voids or other defects. Finally, a cross section should be used to determine the fillet shape and standoff height.



T_{smin} = min soak temperature = 150°C
 T_{smax} = max soak temperature = 200°C
 T_L = liquidous temperature = 217°C
 T_P = peak package temperature = 260°C
 t_s = preheat soak time = 20 to 120 sec
 t = time above liquidous = 60 to 150 sec
 t_p = time within 5 degrees of TP = 30 sec
Time from 25°C to TP = 8 minutes max
Package Thickness < 1.6 mm
Package Volume < 350 mm²

Figure 2: Lead Free Reflow Profile per J-STD-020E

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Pinout and Functional Description

	13	12	11	10	9	8	7	6	5	4	3	2	1	
A		GND	VDDPA_3A	RX_EN	SPI_SDO	GND	RF_COM_A	GND	SPI_CLK	TX_EN	VDDPA_2A	GND		A
B	RF3_A	GND	VDDPA_3A	GND	VDD_1P8	GND		GND	VDD_1P8	GND	VDDPA_2A	GND	RF2_A	B
C	GND	GND	VDDPA_3B		VDD_1P8	GND		GND	VDD_1P8		VDDPA_2B	GND	GND	C
D	RF3_B	GND	VDDPA_3B	GND	VDD_1P8	VDD_1P8		VDD_1P8	VDD_1P8	GND	VDDPA_2B	GND	RF2_B	D
E	GND	GND	GND	GND	GND			GND	GND	GND	GND	GND	GND	E
F	GND	GND	GND		GND			VDD_DIG_1P8	GND_DIG	GND	GND	GND	GND	F
G	RF4_B	GND	VDDPA_4B	GND	VDD_1P8	VDD_1P8		VDD_1P8	VDD_1P8	GND	VDDPA_1B	GND	RF1_B	G
H	GND	GND	VDDPA_4B		VDD_1P8	GND		GND	VDD_1P8		VDDPA_1B	GND	GND	H
J	RF4_A	GND	VDDPA_4A	GND	VDD_1P8	GND		GND	VDD_1P8	GND	VDDPA_1A	GND	RF1_A	J
K		GND	VDDPA_4A	SPI_CSB	SPI_SDI	GND	RF_COM_B	GND	SPI_PDI	SPI_LDB	VDDPA_1A	GND		K
	13	12	11	10	9	8	7	6	5	4	3	2	1	

Figure 3: AWMF-0159 WLBGA Ball Map Pinout

(Bottom View)

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Pin	Signal	Function
B5, B9, C5, C9, D5, D6, D8, D9, F5, G5, G6, G8, G9, H5, H9, J5, J9,	VDD_1P8	1.8V Power Supply
A3, A11, B3, B11, C3, C11, D3, D11, G3, G11, H3, H11, J3, J11, K3, K11	VDDPA	PA Power Supply
A2, A6, A8, A12, B2, B4, B6, B8, B10, B12, C1, C2, C6, C8, C12, C13, D2, D4, D10, D12, E1, E2, E3, E4, E5, E9, E10, E11, E12, E13, F1, F2, F3, F4, F9, F11, F12, F13, G2, G4, G10, G12, H1, H2, H6, H8, H12, H13, J2, J4, J6, J8, J10, J12, K2, K6, K8, K12	GND	Ground
G1	RF1_B	RF In/Out Antenna Port Element 1B
D1	RF2_B	RF In/Out Antenna Port Element 2B
D13	RF3_B	RF In/Out Antenna Port Element 3B
G13	RF4_B	RF In/Out Antenna Port Element 4B
K7	RF_COM_B	RF In/Out Common B
J1	RF1_A	RF In/Out Antenna Port Element 1A
B1	RF2_A	RF In/Out Antenna Port Element 2A
B13	RF3_A	RF In/Out Antenna Port Element 3A
J13	RF4_A	RF In/Out Antenna Port Element 4A
A7	RF_COM_A	RF In/Out Common A
A4	TX_EN	Tx Enable
A10	RX_EN	Rx Enable
K10	SPI_CS _B	SPI Chip Select Active Low
K9	SPI_SD _I	SPI Serial Data Input
K5	SPI_PDI	SPI Parallel Data Input
A5	SPI_CLK	SPI Clock
A9	SPI_SDO	SPI Data Output
K4	SPI_LDB	Latch SPI Data (Active Low)

Table 8: AWMF-0159 Pin-out and Pin Descriptions

n260 Band 5G Tx/Rx Dual-Pol Quad Core BFIC

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Tx Typical Performance

All measurements at Vdd = 1.8V and 25°C unless otherwise noted

— Tx Power Performance

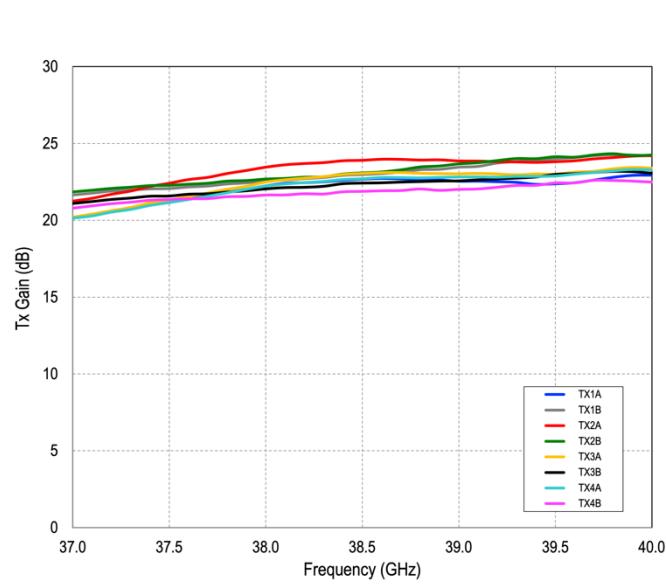


Figure 4: Tx Gain

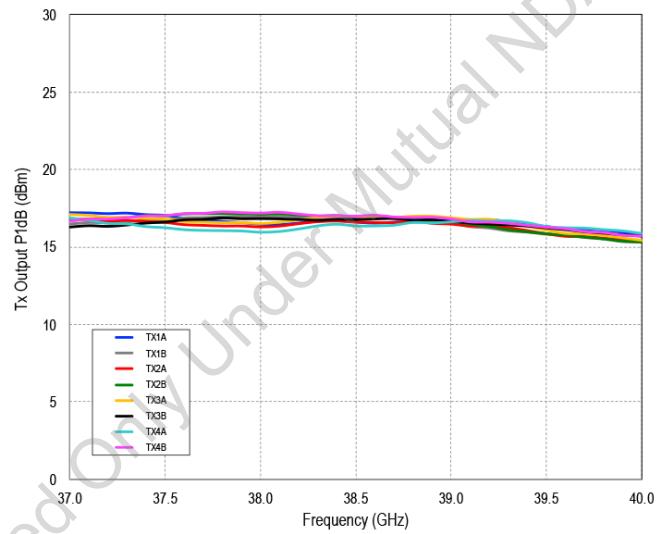


Figure 5: Tx Output P1dB

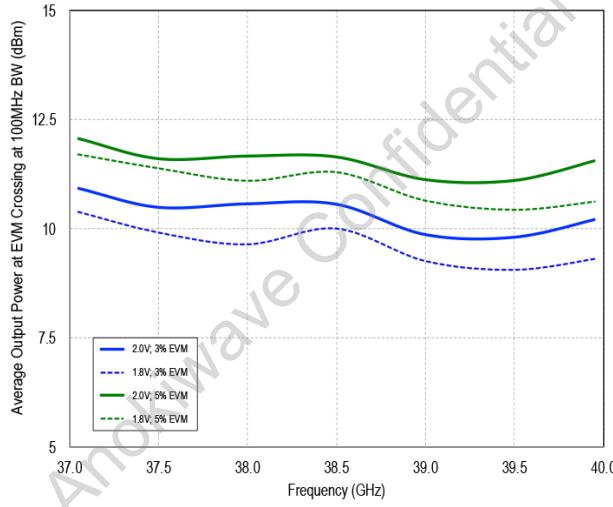


Figure 6: Tx Average Pout at EVM Crossing
5GNR 64QAM 100 MHz at VDDPA of 2.0V and 1.8V

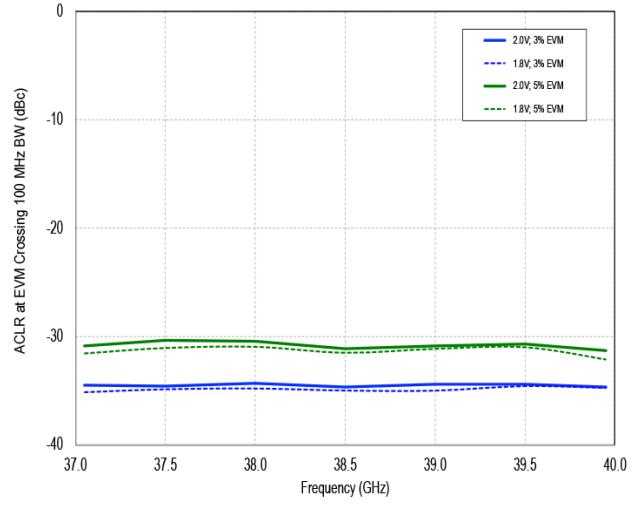


Figure 7: Tx Average ACLR at EVM Crossing
5GNR 64QAM 100 MHz at VDDPA of 2.0V and 1.8V

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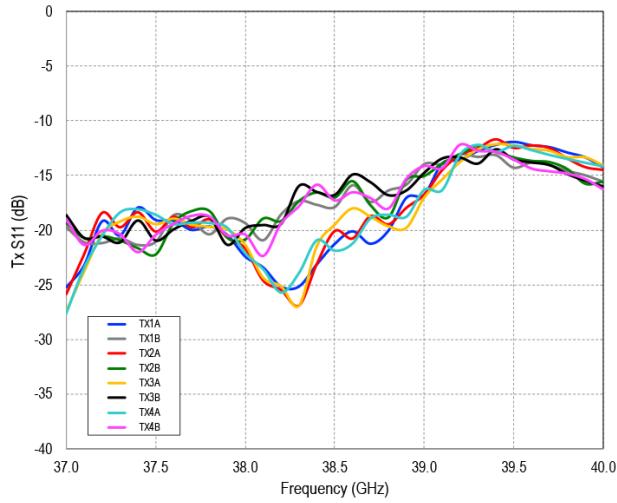


Figure 8: Tx S11

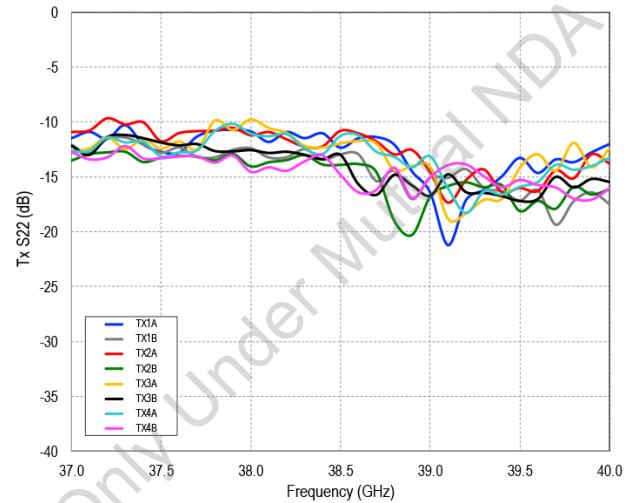


Figure 9: Tx S22

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Tx Phase Control Performance

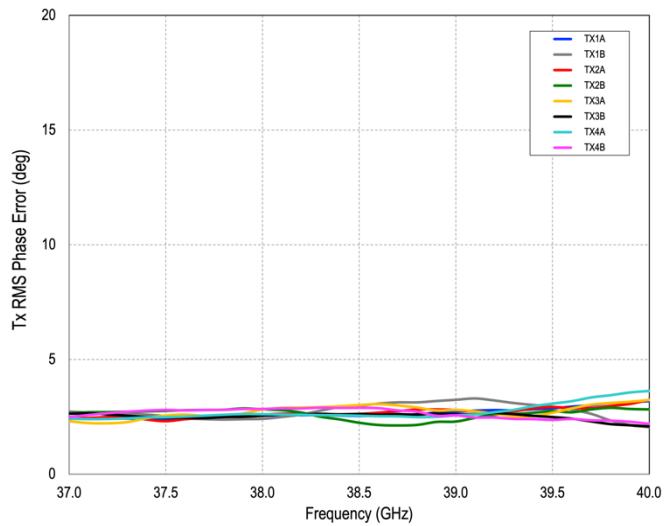


Figure 10: Tx RMS Phase Error

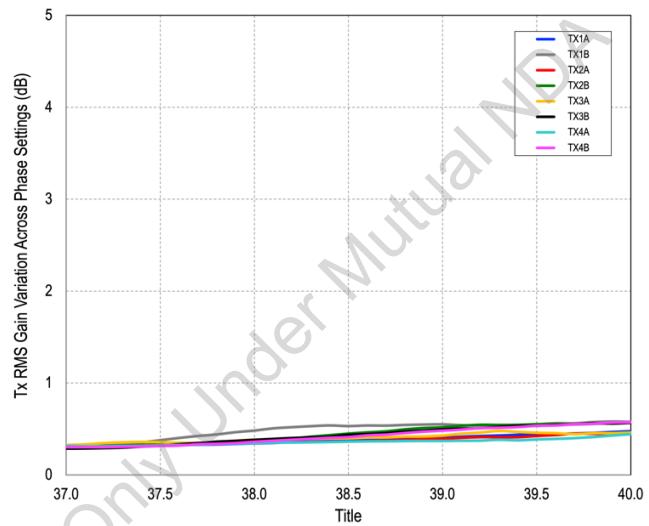


Figure 11: Tx RMS Gain Variation Across Phase Settings

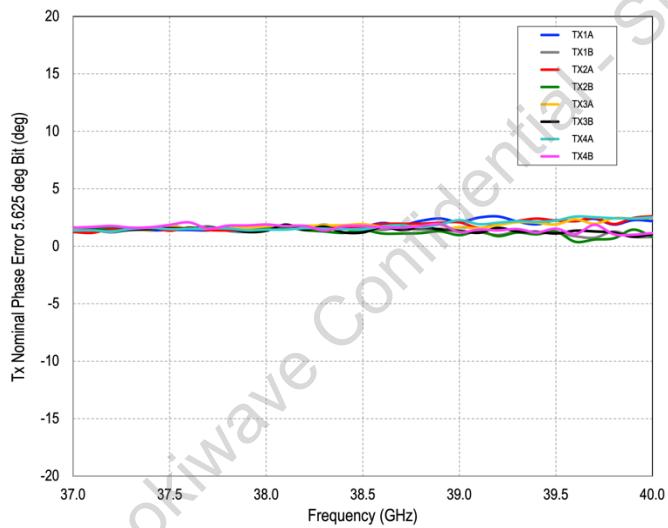


Figure 12: 5.625° Bit Tx Phase Error

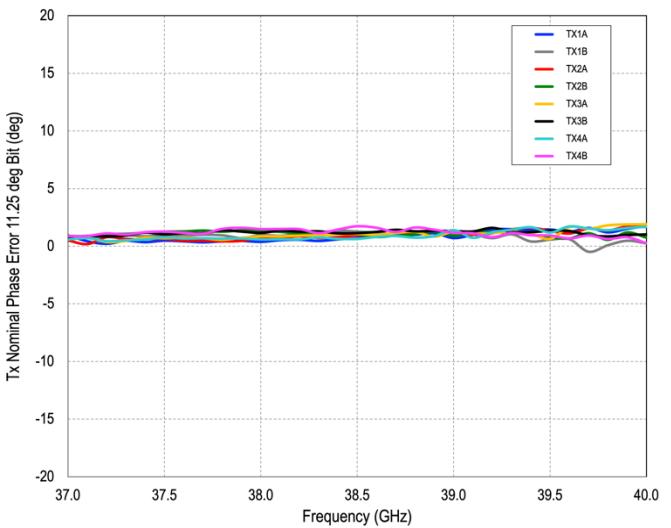


Figure 13: 11.25° Bit Tx Phase Error

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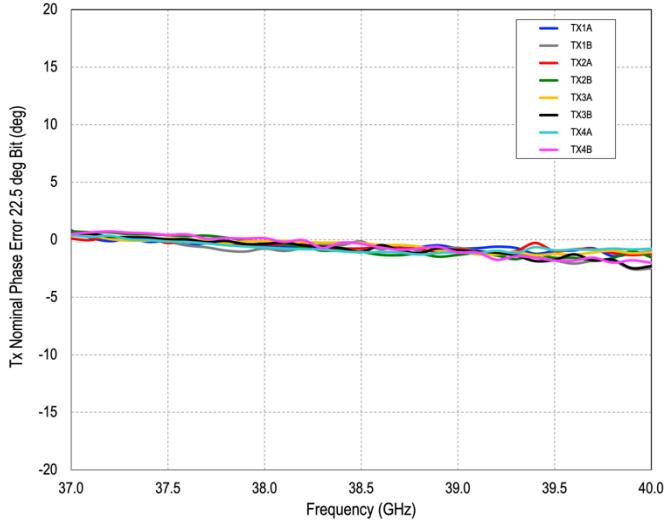


Figure 14: 22.5° Bit Tx Phase Error

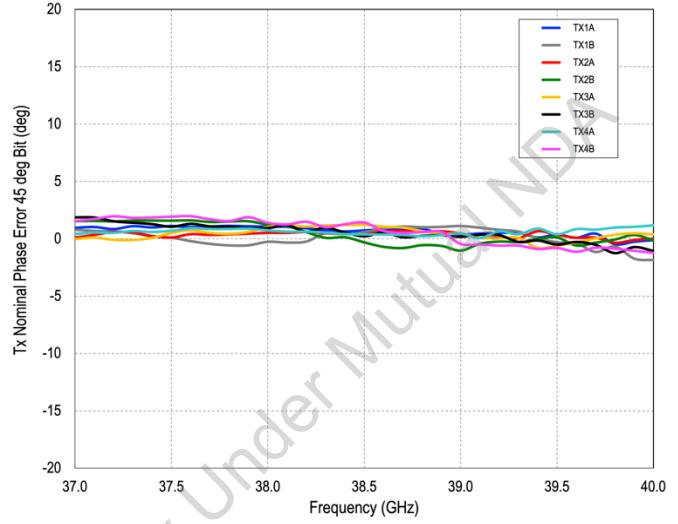


Figure 15: 45° Bit Tx Phase Error

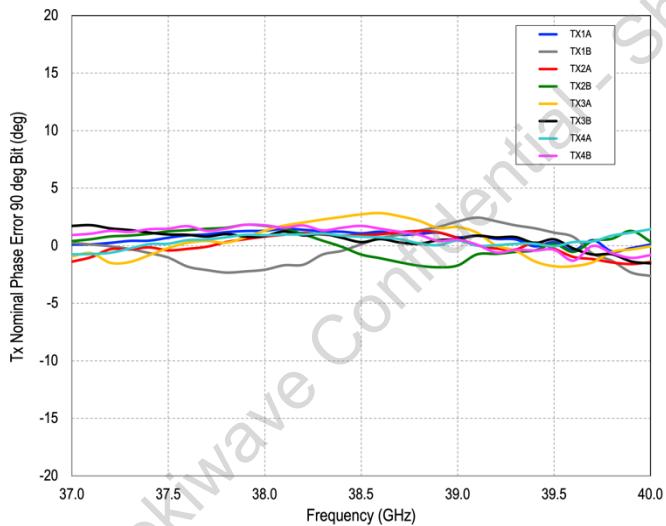


Figure 16: 90° Bit Tx Phase Error

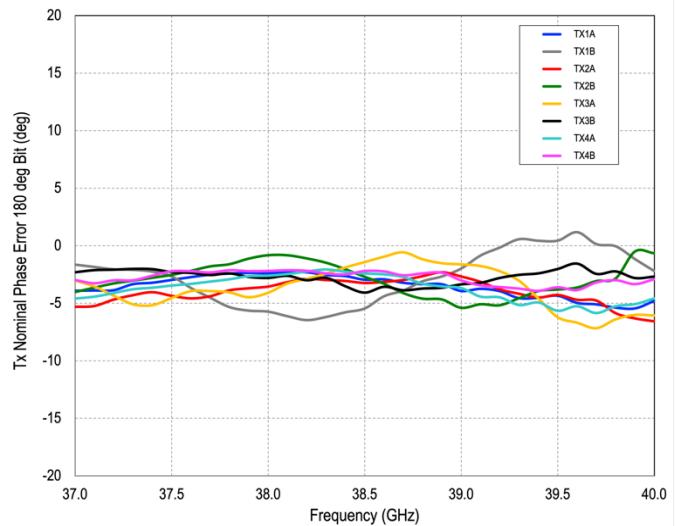


Figure 17: 180° Bit Tx Phase Error

n260 Band 5G Tx/Rx Dual-Pol Quad Core BFIC

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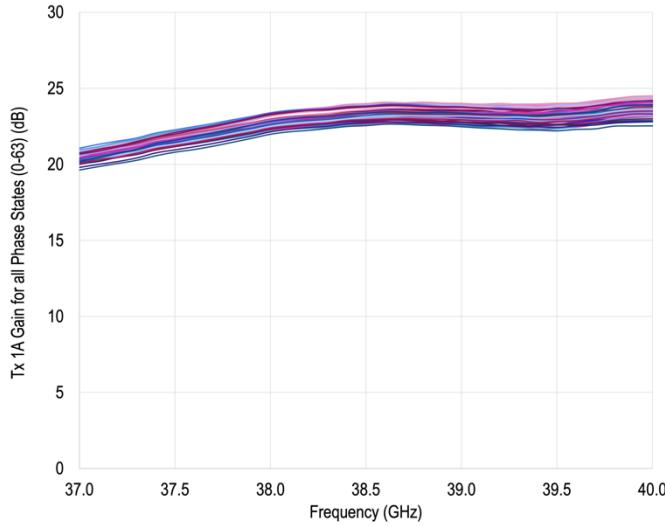


Figure 18: Tx1A Gain – all phase states

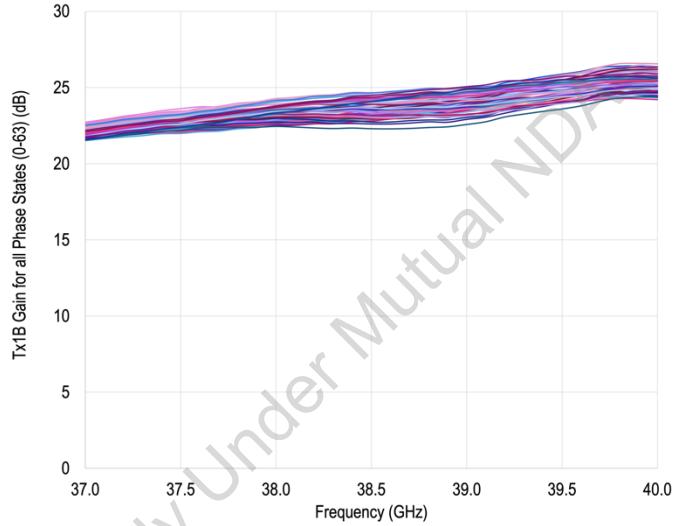


Figure 19: Tx1B Gain – all phase states

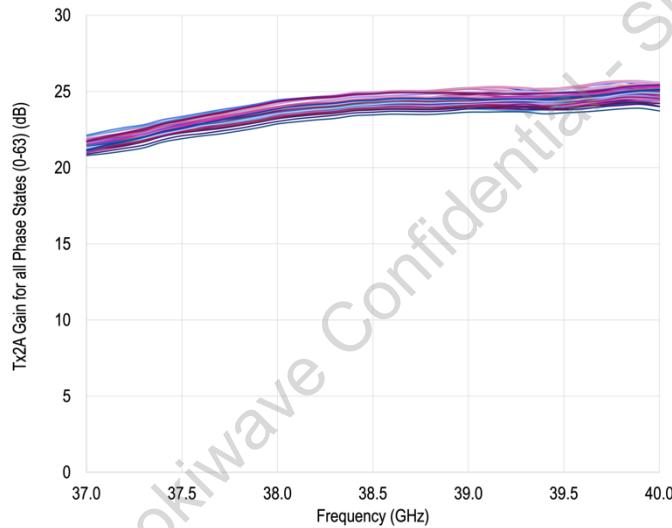


Figure 20: Tx2A Gain – all phase states

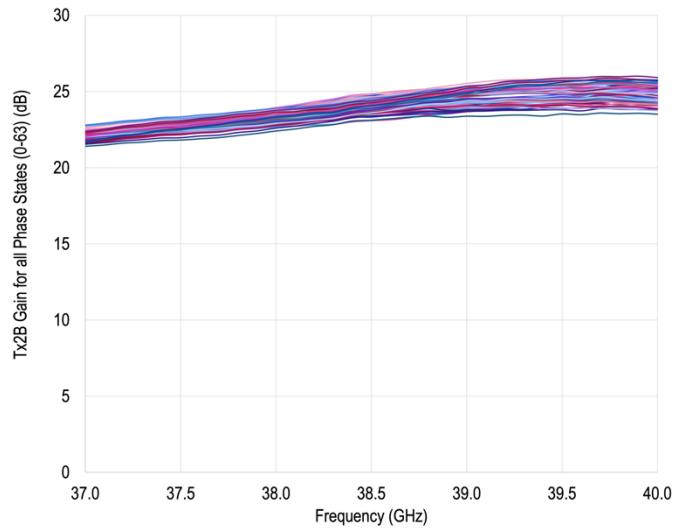


Figure 21: Tx2B Gain – all phase states

n260 Band 5G Tx/Rx Dual-Pol Quad Core BFIC

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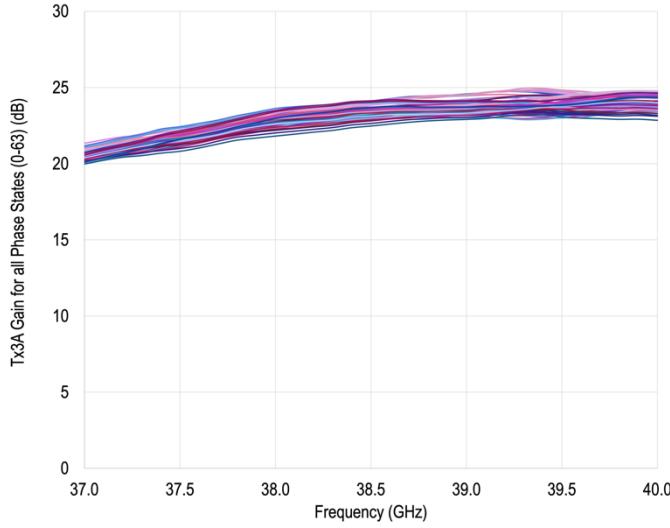


Figure 22: Tx3A Gain – all phase states

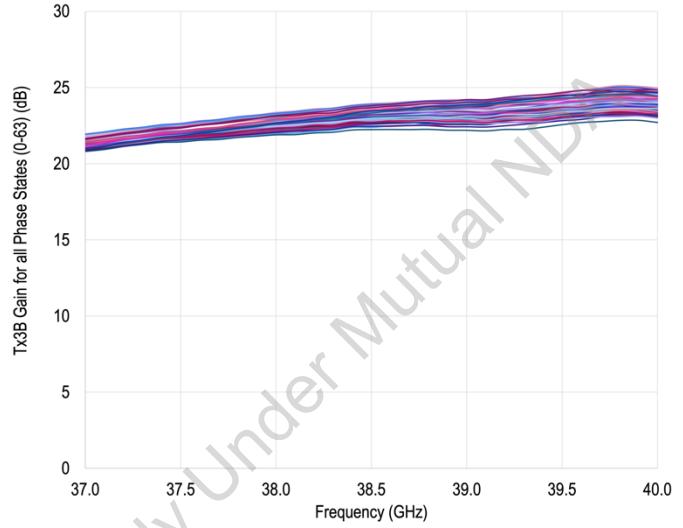


Figure 23: Tx3B Gain – all phase states

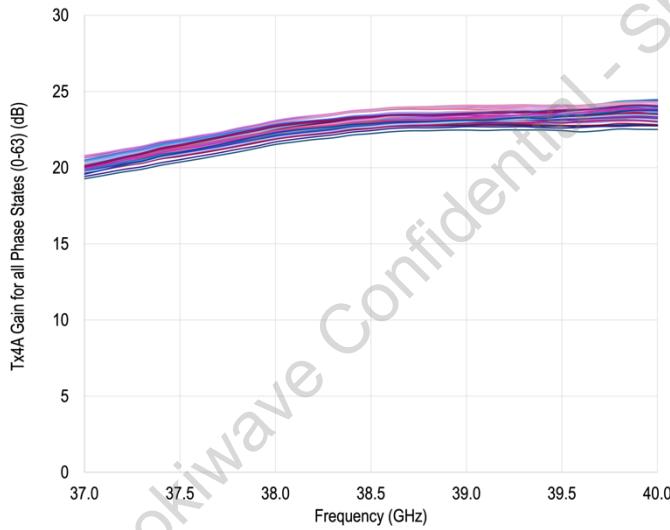


Figure 24: Tx4A Gain – all phase states

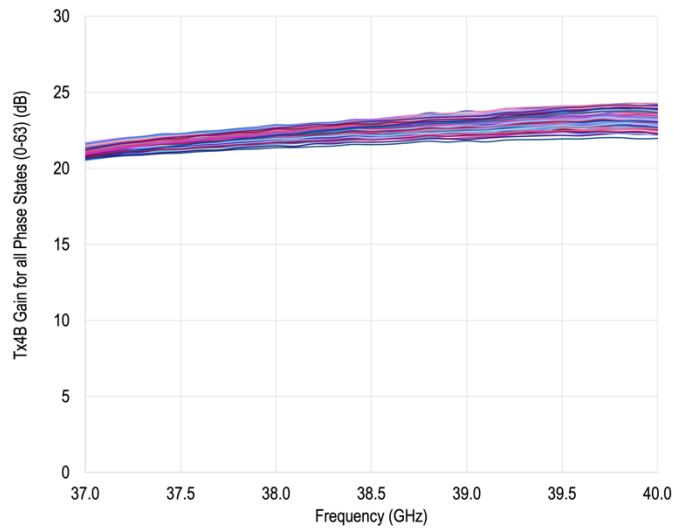


Figure 25: Tx4B Gain – all phase states

n260 Band 5G Tx/Rx Dual-Pol Quad Core BFIC

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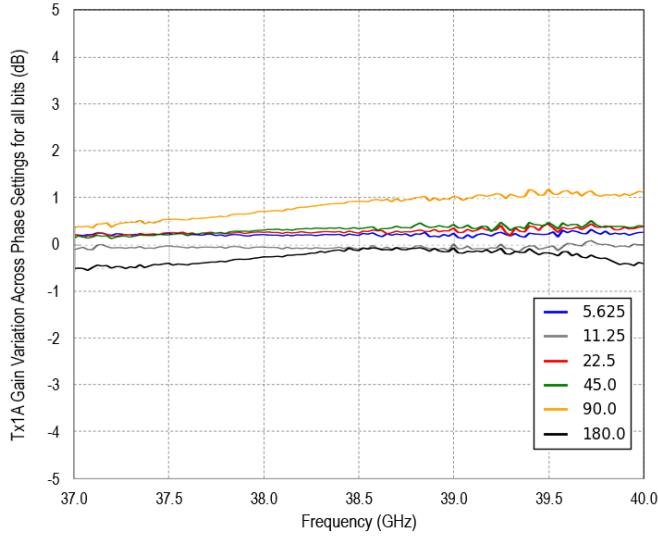


Figure 26: Tx1A Gain Variation Across Phase Settings per bit

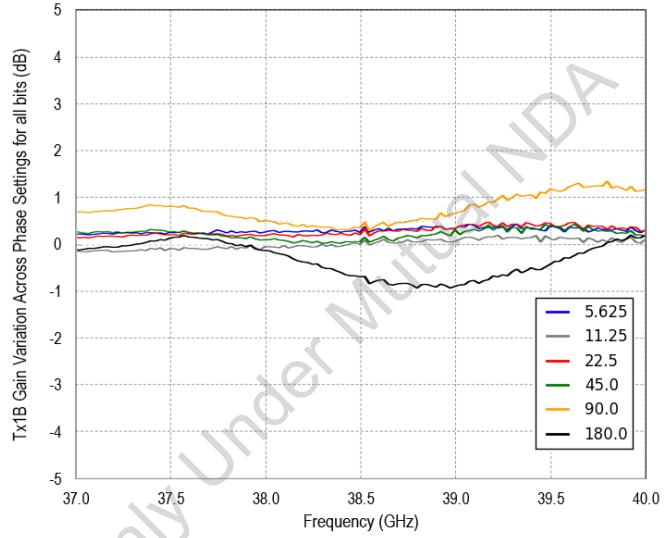


Figure 27: Tx1B Gain Variation Across Phase Settings per bit

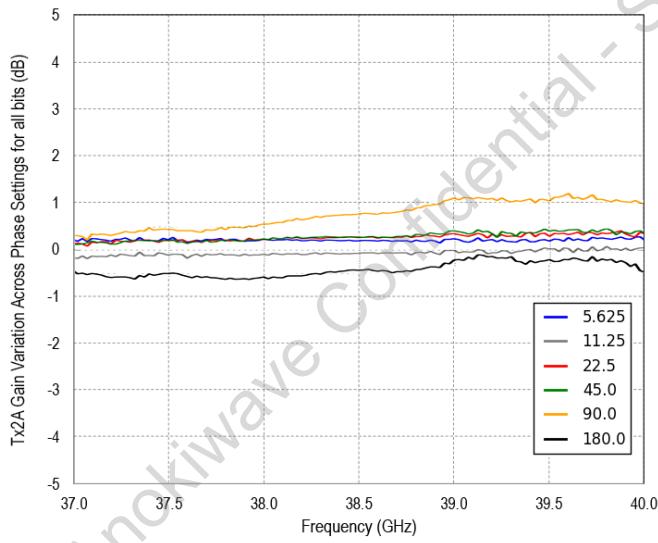


Figure 28: Tx2A Gain Variation Across Phase Settings per bit

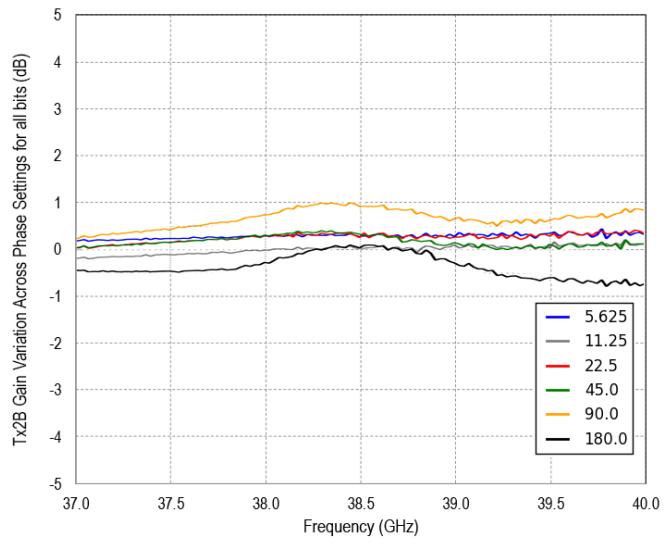


Figure 29: Tx2B Gain Variation Across Phase Settings per bit

n260 Band 5G Tx/Rx Dual-Pol Quad Core BFIC

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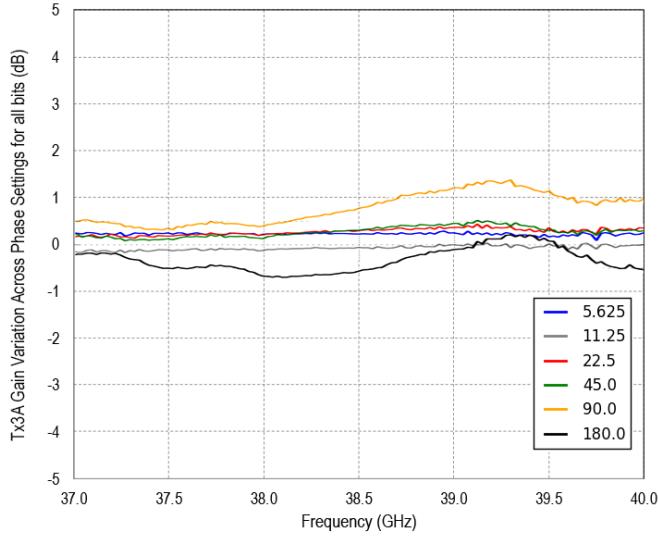


Figure 30: Tx3A Gain Variation Across Phase Settings per bit

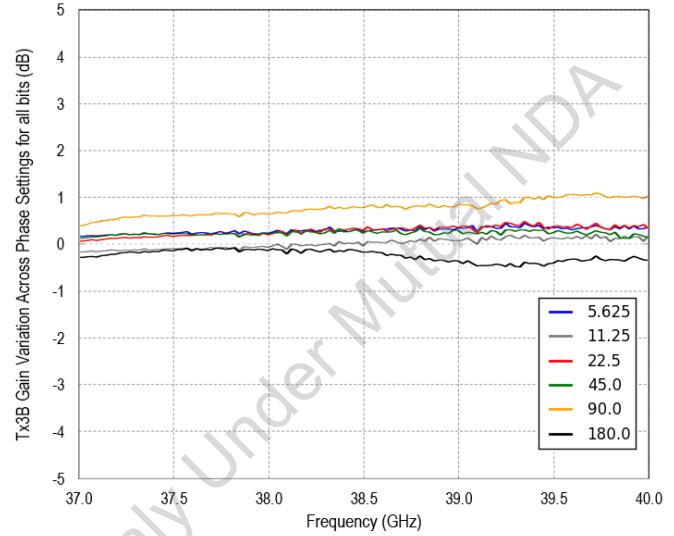


Figure 31: Tx3B Gain Variation Across Phase Settings per bit

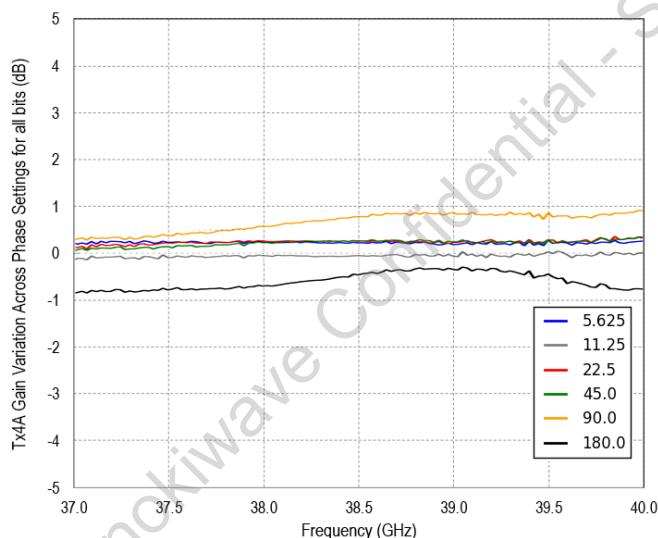


Figure 32: Tx4A Gain Variation Across Phase Settings per bit

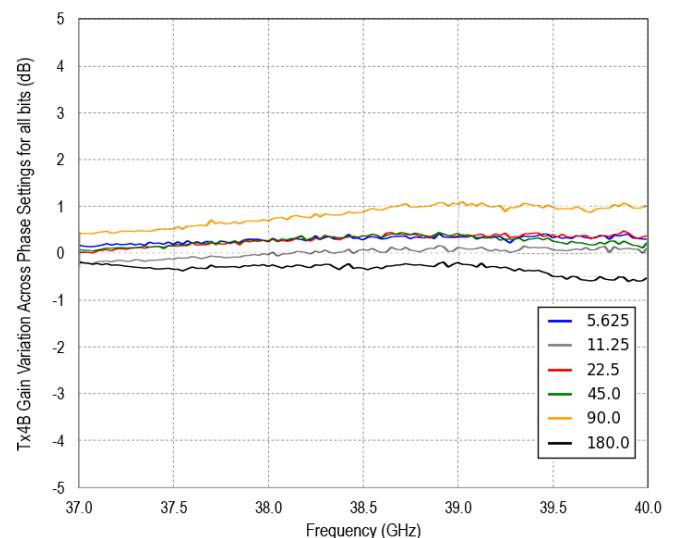


Figure 33: Tx4B Gain Variation Across Phase Settings per bit

n260 Band 5G Tx/Rx Dual-Pol Quad Core BFIC

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— Tx Gain Control Performance

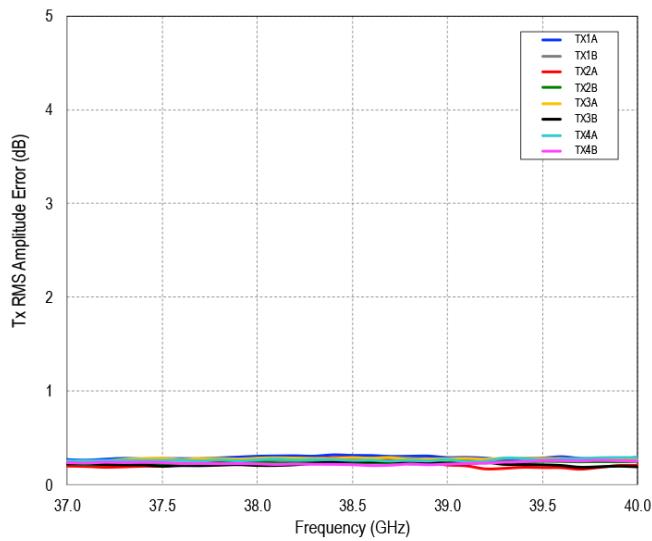


Figure 34: Tx RMS Amplitude Error

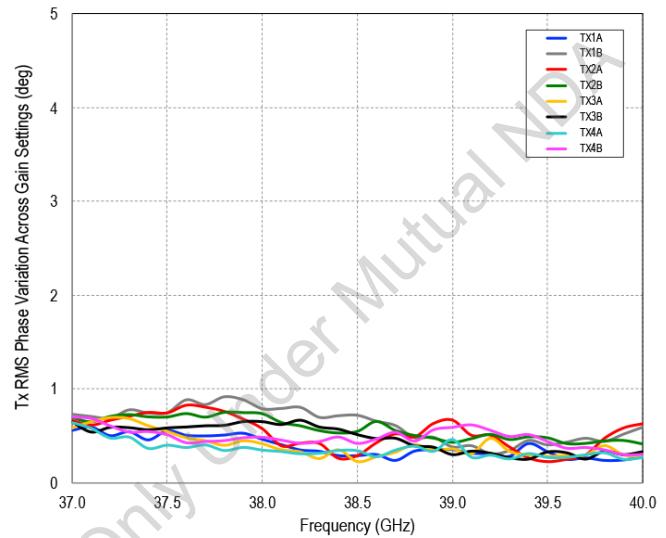


Figure 35: Tx RMS Phase Variation Across Gain Settings

n260 Band 5G Tx/Rx Dual-Pol Quad Core BFIC

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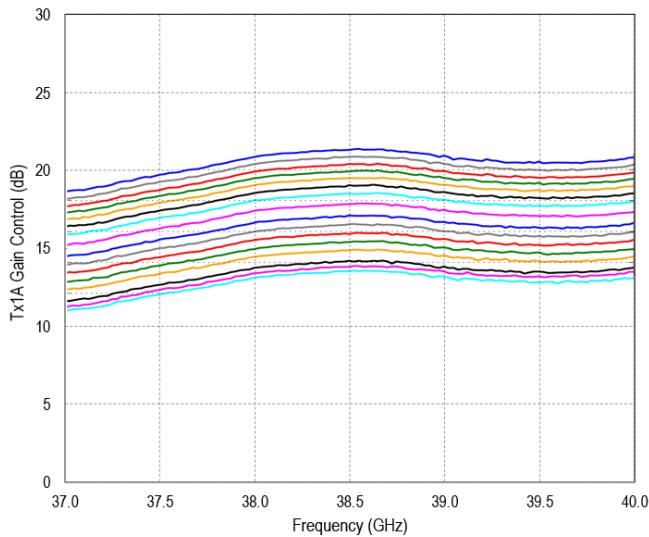


Figure 36: Tx1A Element Gain Control (0-15)

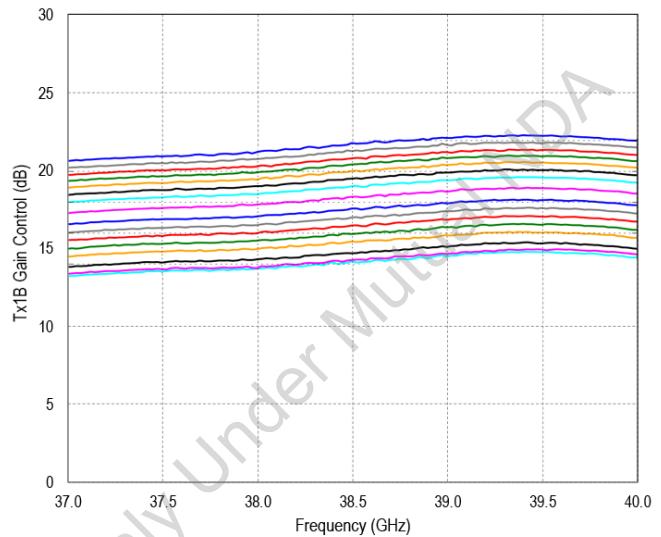


Figure 37: Tx1B Element Gain Control (0-15)

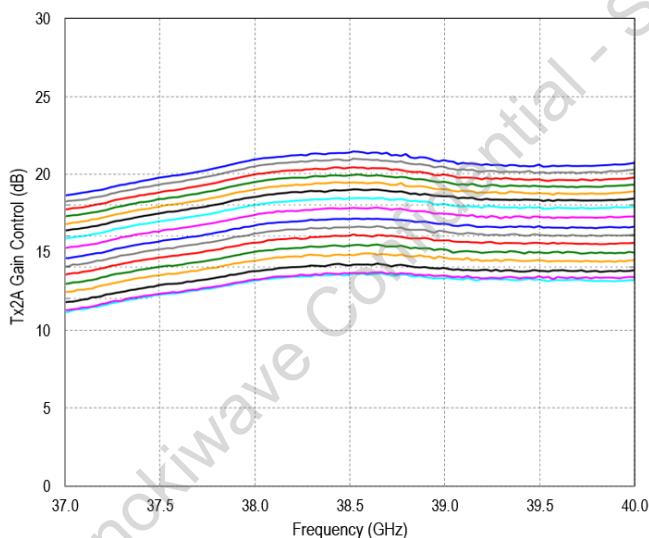


Figure 38: Tx2A Element Gain Control (0-15)

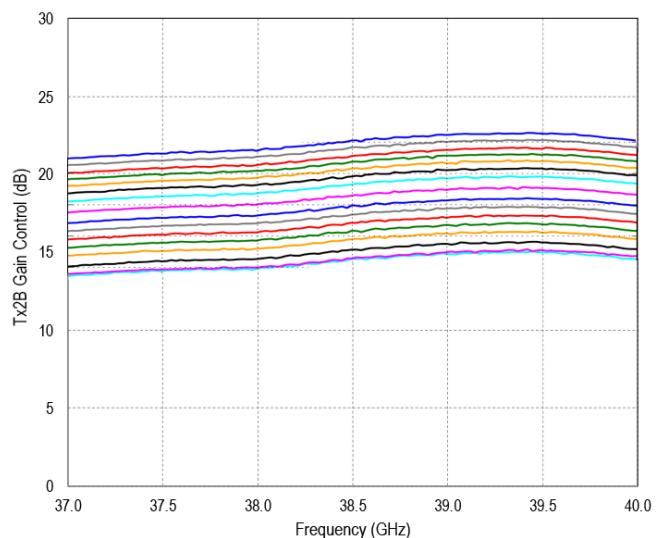


Figure 39: Tx2B Element Gain Control (0-15)

n260 Band 5G Tx/Rx Dual-Pol Quad Core BFIC

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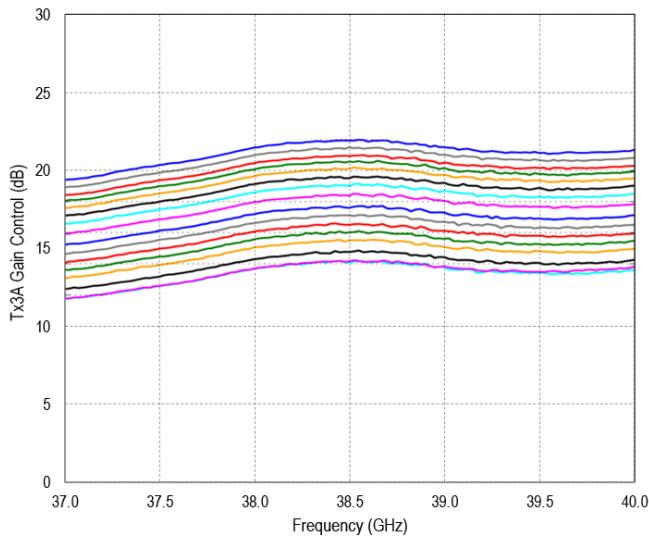


Figure 40: Tx3A Element Gain Control (0-15)

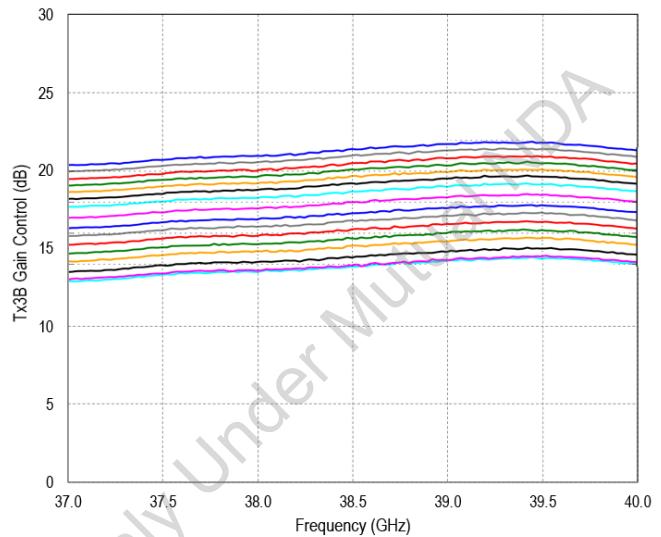


Figure 41: Tx3B Element Gain Control (0-15)

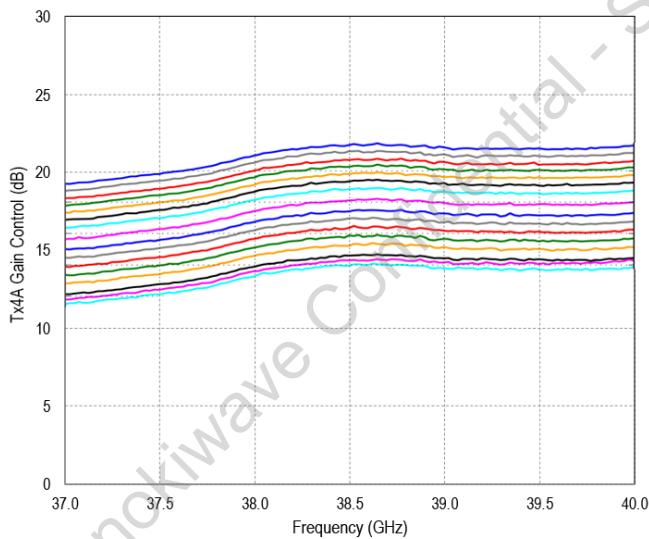


Figure 42: Tx4A Element Gain Control (0-15)

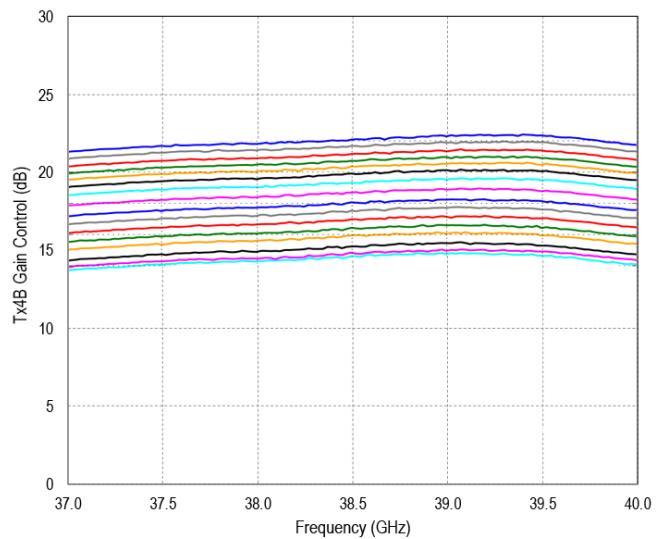


Figure 43: Tx4B Element Gain Control (0-15)

n260 Band 5G Tx/Rx Dual-Pol Quad Core BFIC

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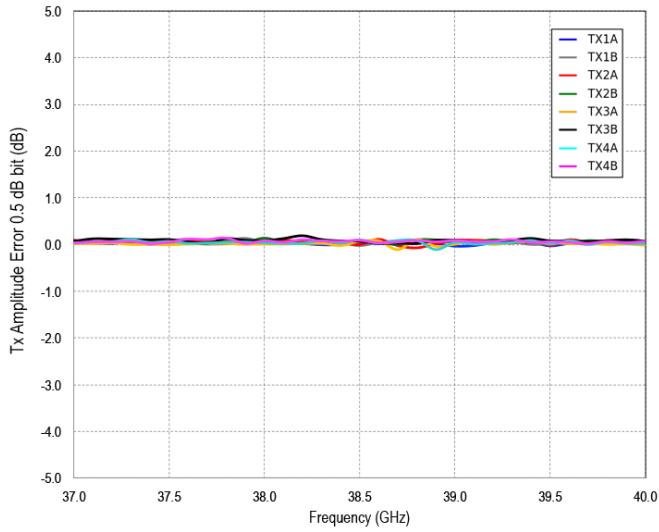


Figure 44: 0.5 dB Bit Tx Amplitude Error

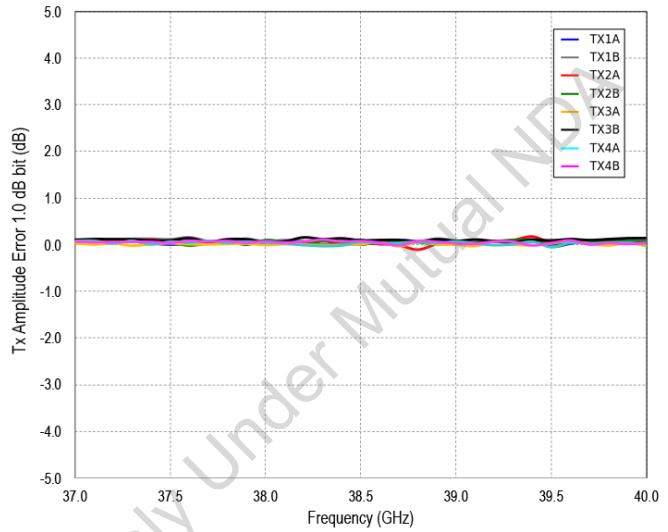


Figure 45: 1.0 dB Bit Tx Amplitude Error

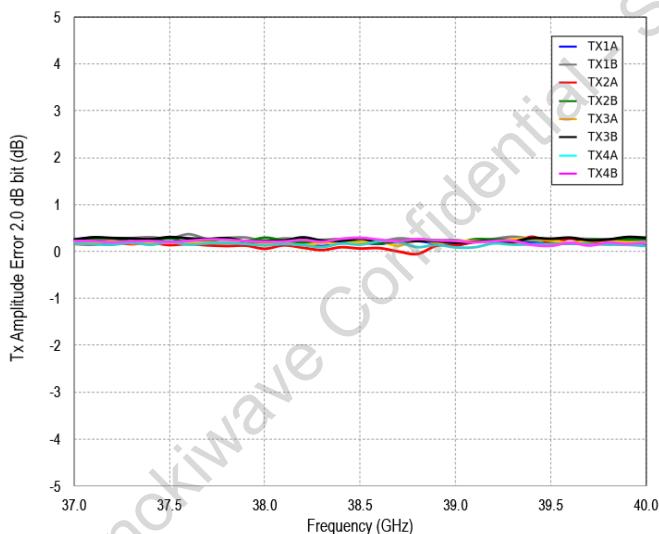


Figure 46: 2.0 dB Bit Tx Amplitude Error

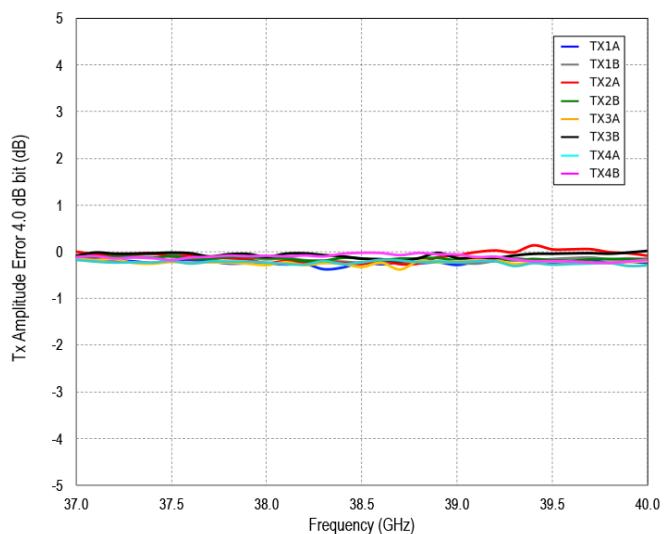


Figure 47: 4.0 dB Bit Tx Amplitude Error

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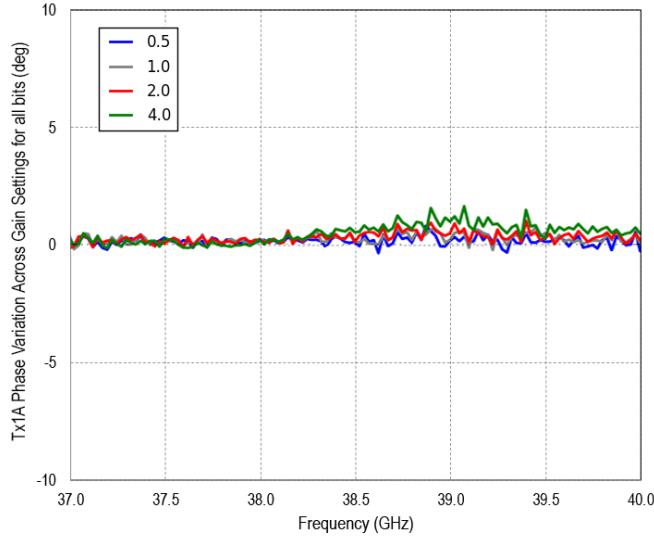


Figure 48: Tx1A Phase Variation Across Gain Settings per bit

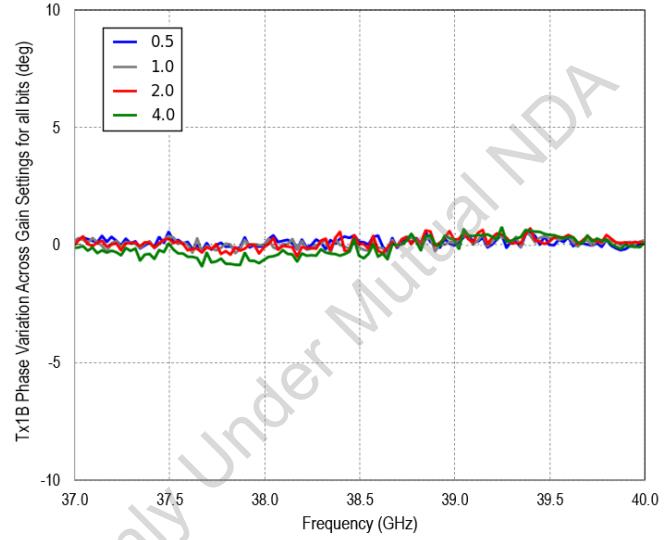


Figure 49: Tx1B Phase Variation Across Gain Settings per bit

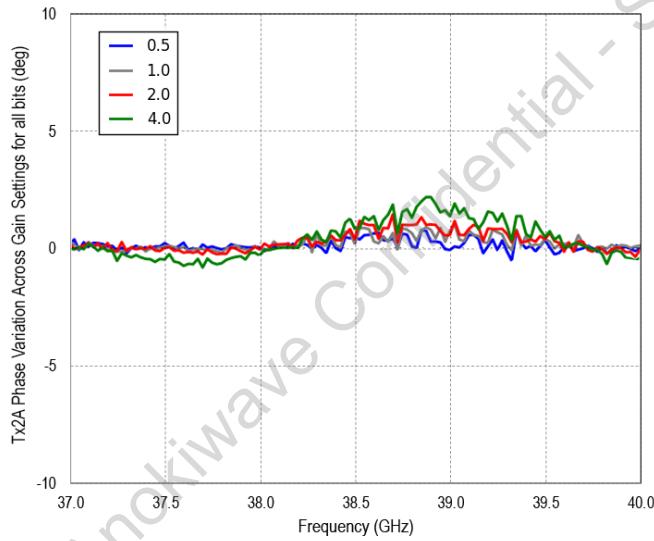


Figure 50: Tx2A Phase Variation Across Gain Settings per bit

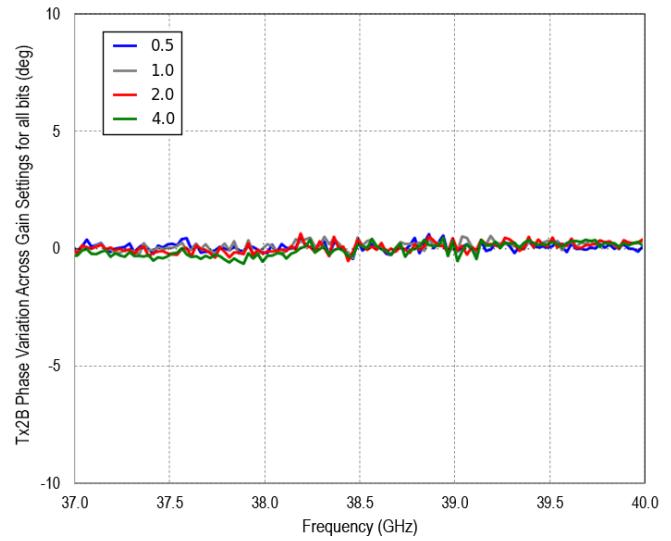


Figure 51: Tx2B Phase Variation Across Gain Settings per bit

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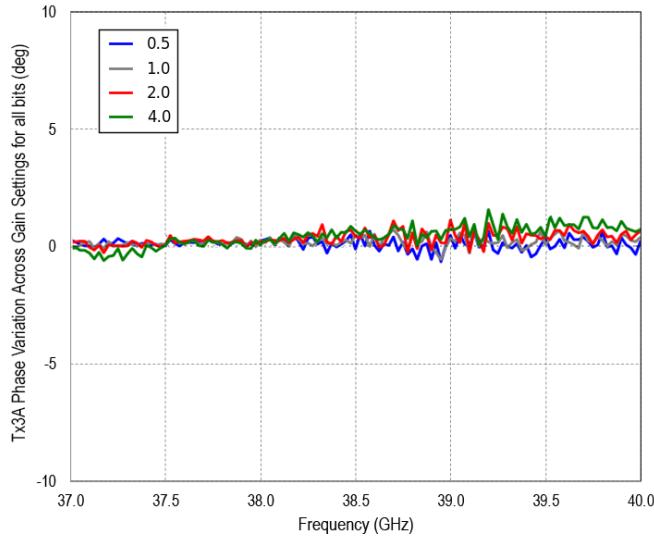


Figure 52: TX3A Phase Variation Across Gain Settings per bit

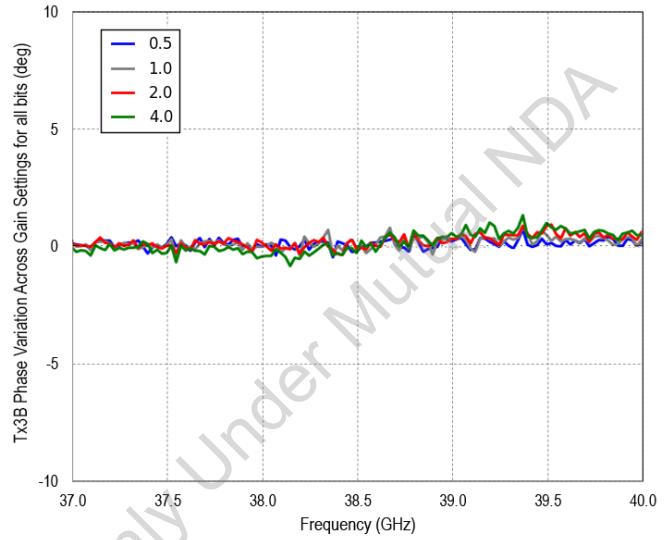


Figure 53: TX3B Phase Variation Across Gain Settings per bit

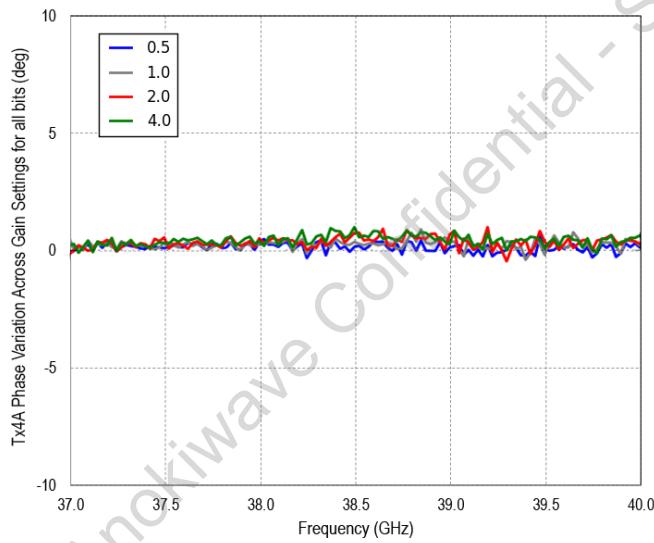


Figure 54: TX4A Phase Variation Across Gain Settings per bit

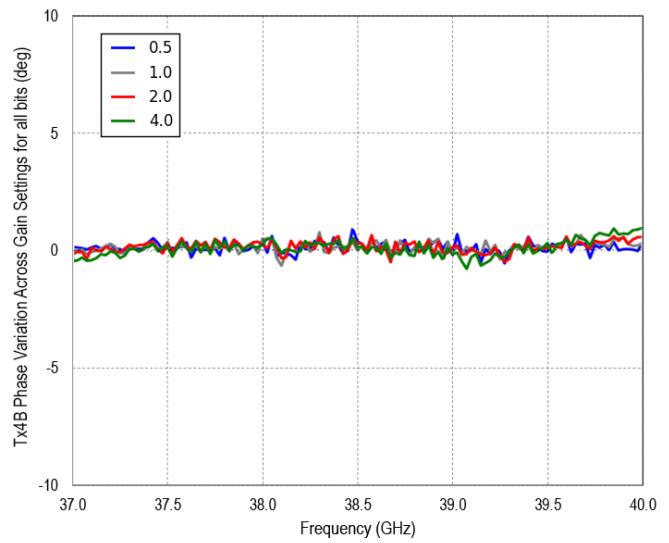


Figure 55: TX4B Phase Variation Across Gain Settings per bit

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Rx Typical Performance

All measurements at Vdd = 1.8V and 25°C unless otherwise noted.

- Rx Coherent Gain, Noise Figure, Input P1dB Performance

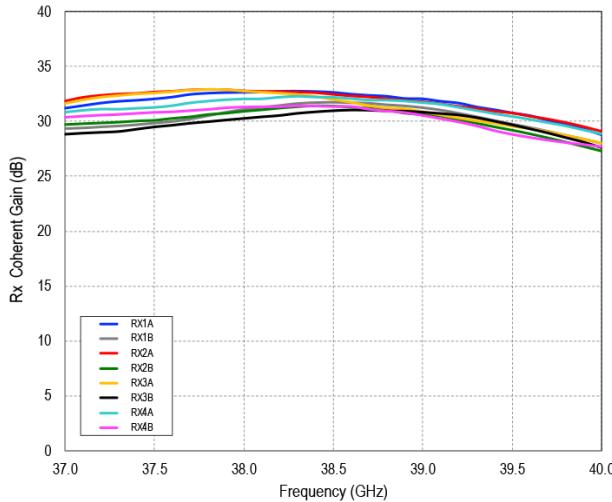


Figure 56: Rx Coherent Gain*

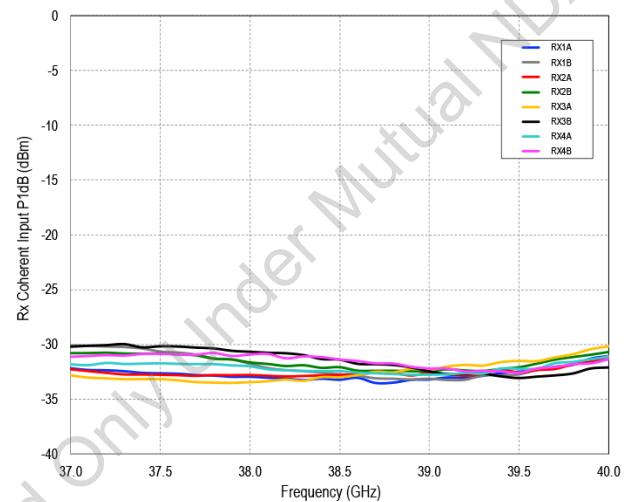


Figure 57: Rx Coherent Input P1dB*

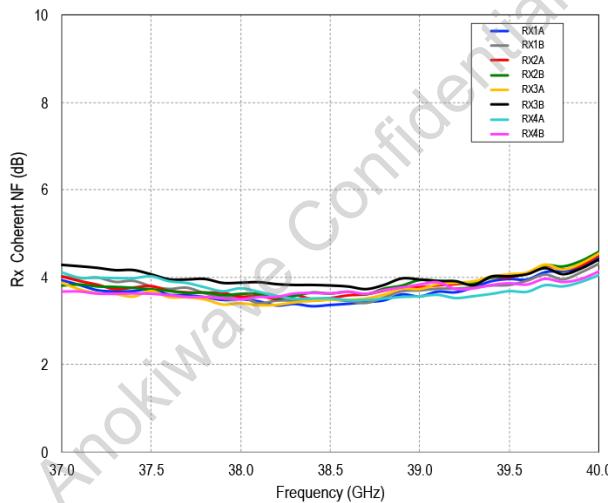


Figure 58: Rx Coherent Noise Figure*

*NOTE: Coherent gain (CG) is the RF gain with all Rx input ports energized and is most useful for assessing RF power handling in the beam forming network. Electronic gain (EG) is the RF gain exclusive of the 4:1 sum and is most useful for cascaded NF and gain calculation. The total gain of the antenna aperture can be calculated from EG + 10^{log(n)}, where n is the number of antenna elements in the array. Single path gain (SPG) is the RF gain with only one input port energized. This is representative of the RF gain measured in a 2 port measurement system, such as with the Developer's Kit. In the coherent gain plot above, 12 dB has been added to the single path gain value from each quadrant.

$$CG = SPG + 12 \text{ dB} = EG + 6 \text{ dB} \text{ for a quad IC}$$

Coherent NF and IP1dB are the noise figure/IP1dB obtained when all input ports are energized and coherently combined.

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Rx Phase Control Performance

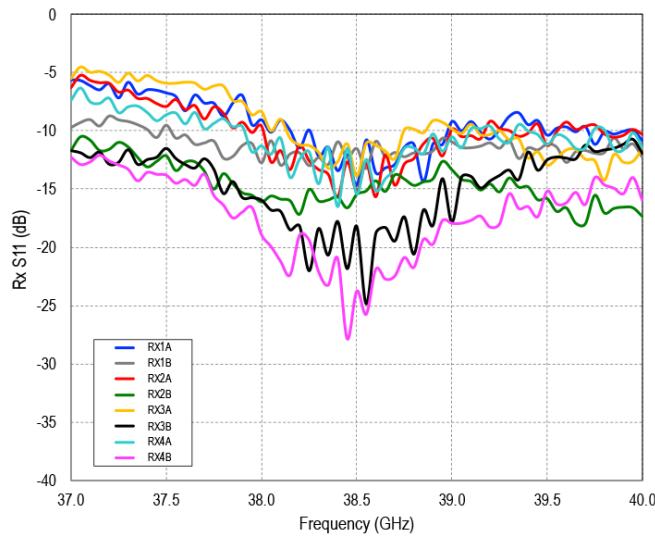


Figure 59: Rx S11

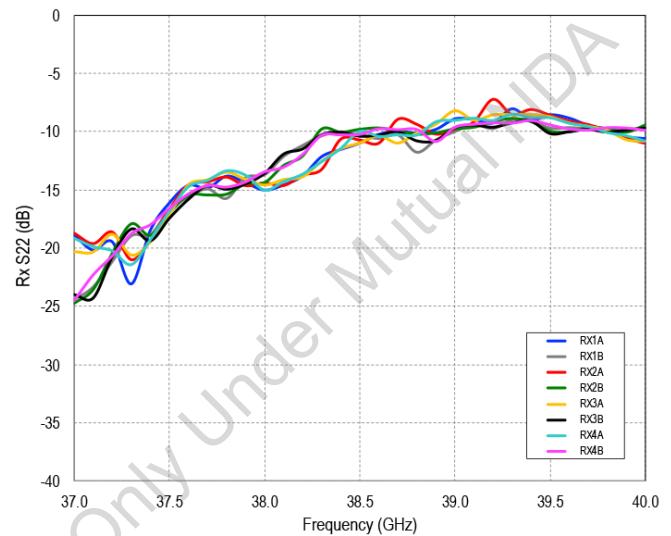


Figure 60: Rx S22

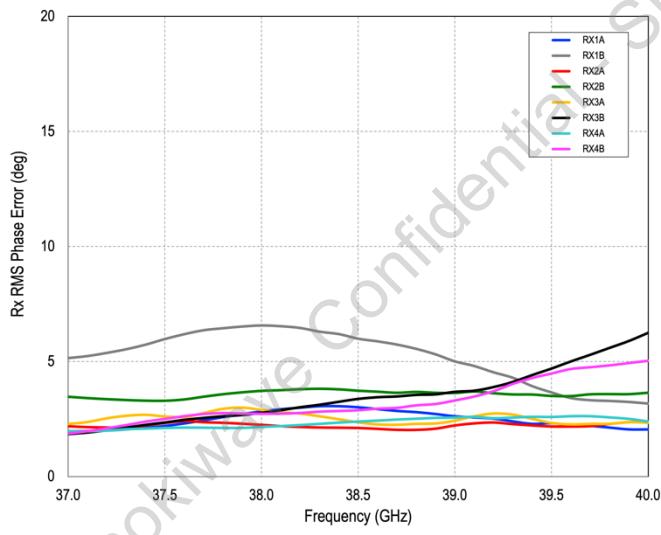


Figure 61: Rx RMS Phase Error

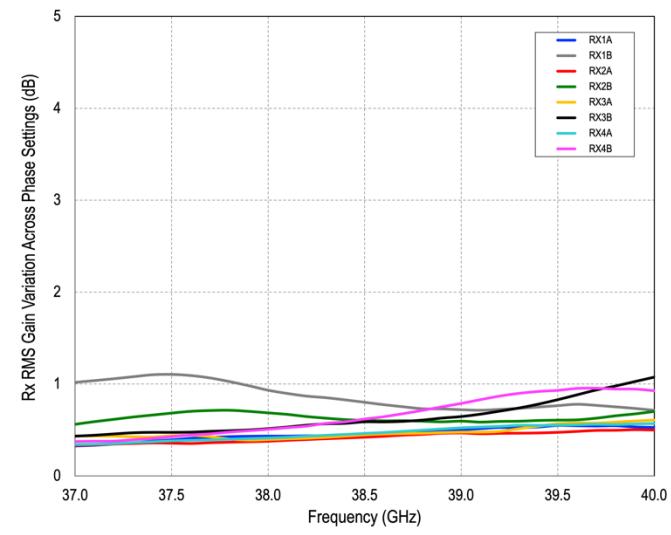


Figure 62: Rx RMS Gain Variation Across Phase Settings

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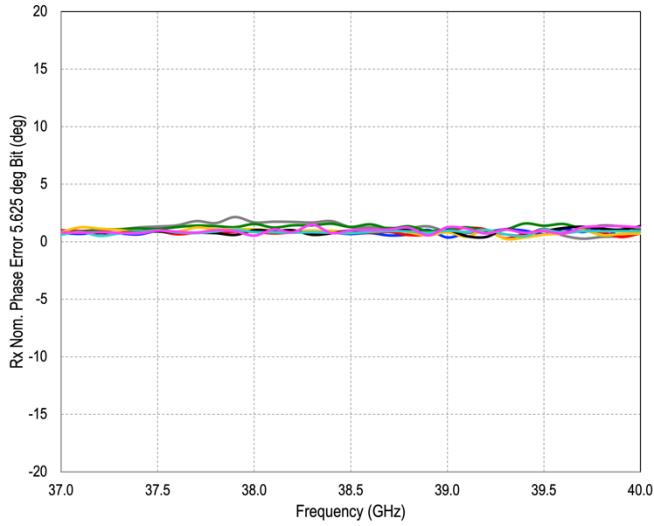


Figure 63: 5.625° Bit Rx Phase Error

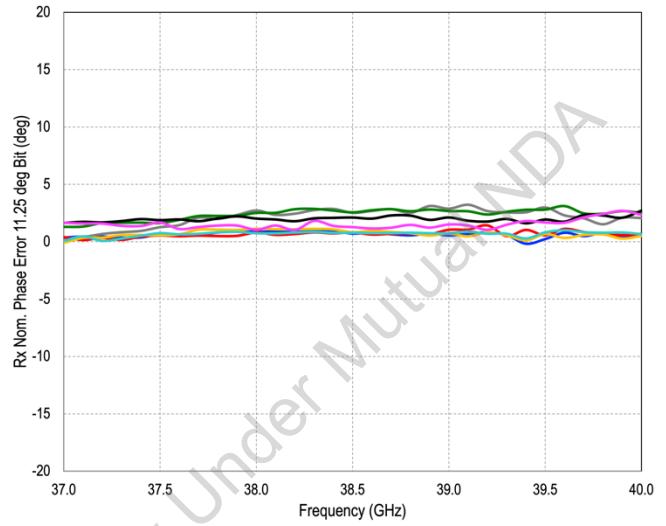


Figure 64: 11.25° Bit Rx Phase Error

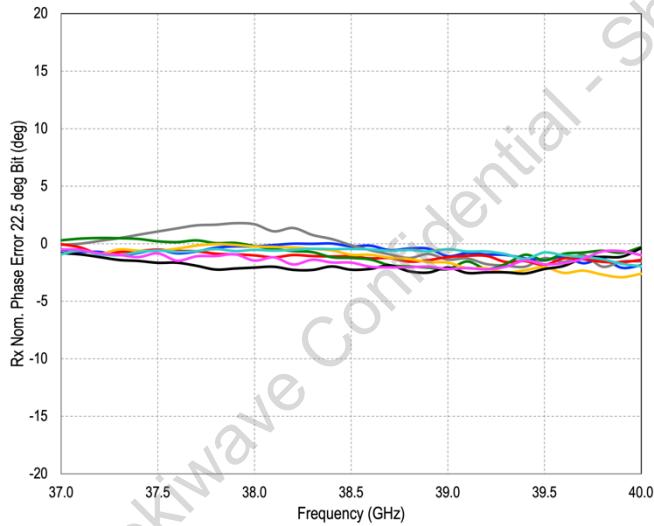


Figure 65: 22.5° Bit Rx Phase Error

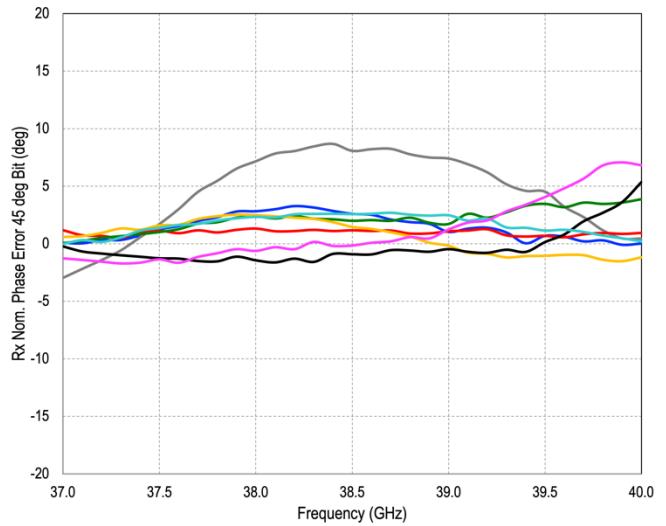


Figure 66: 45° Bit Rx Phase Error

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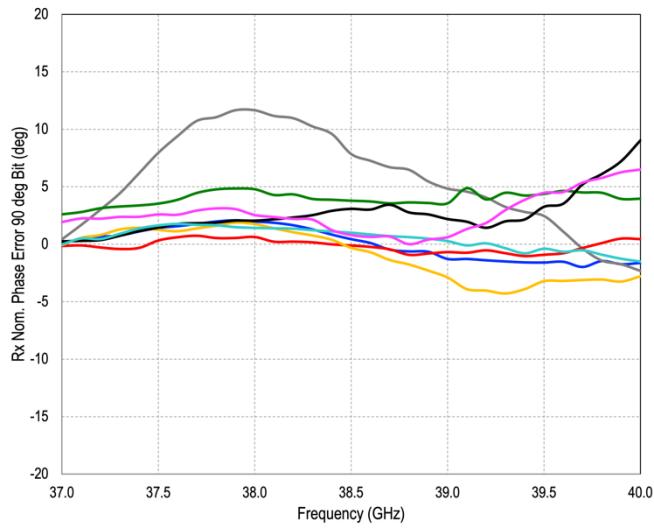


Figure 67: 90° Bit Rx Phase Error

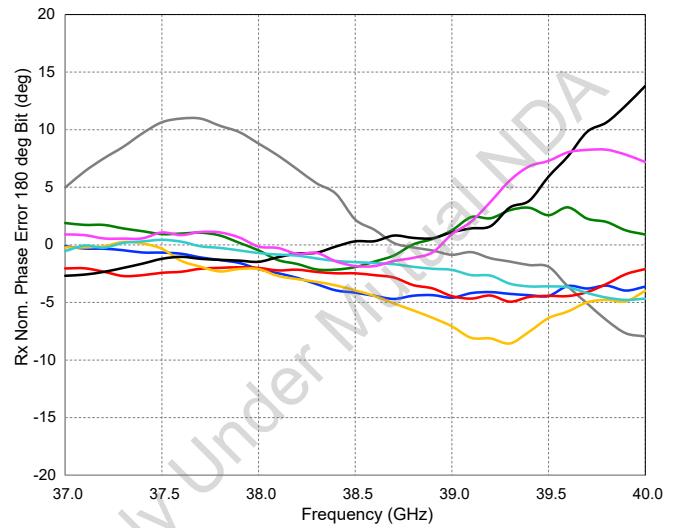


Figure 68: 180° Bit Rx Phase Error

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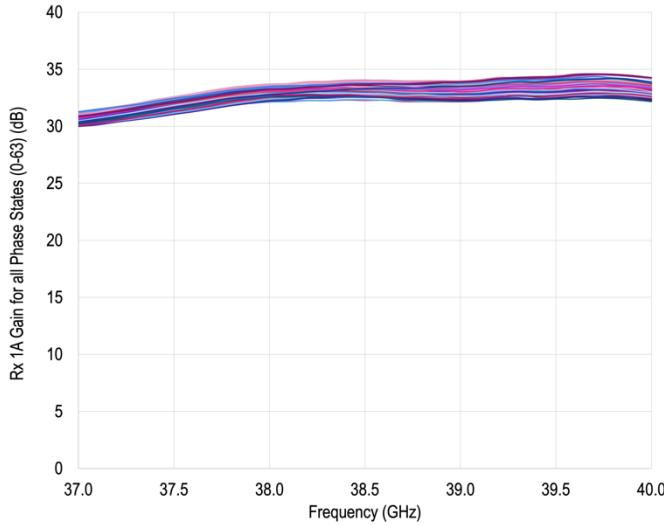


Figure 69: Rx1A Coherent Gain—all phase states

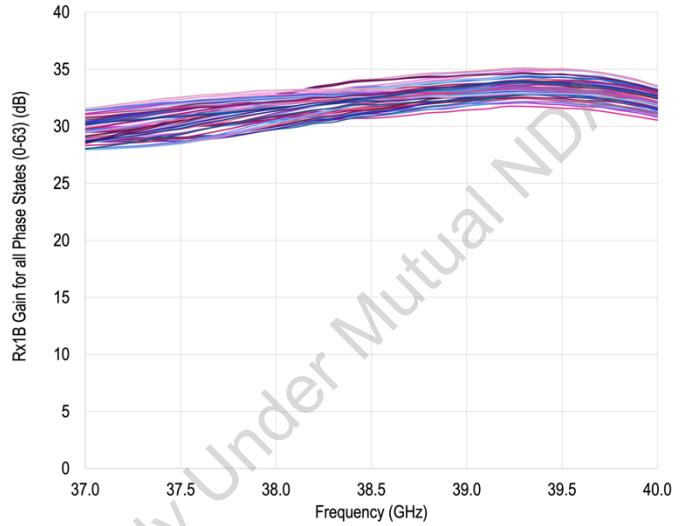


Figure 70: Rx1B Coherent Gain—all phase states

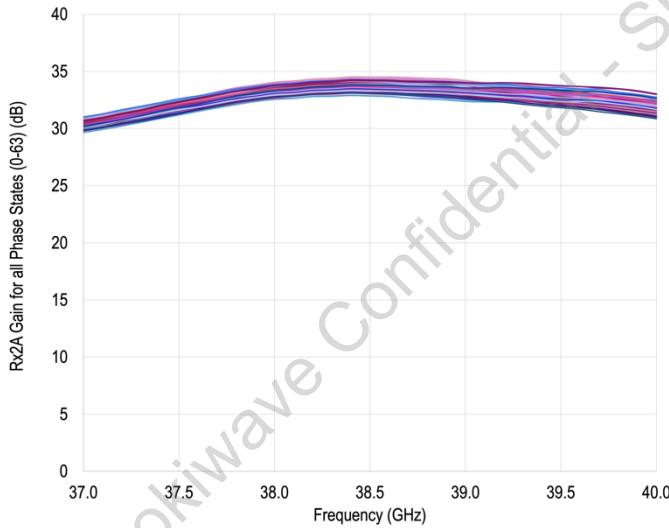


Figure 71: Rx2A Coherent Gain—all phase states

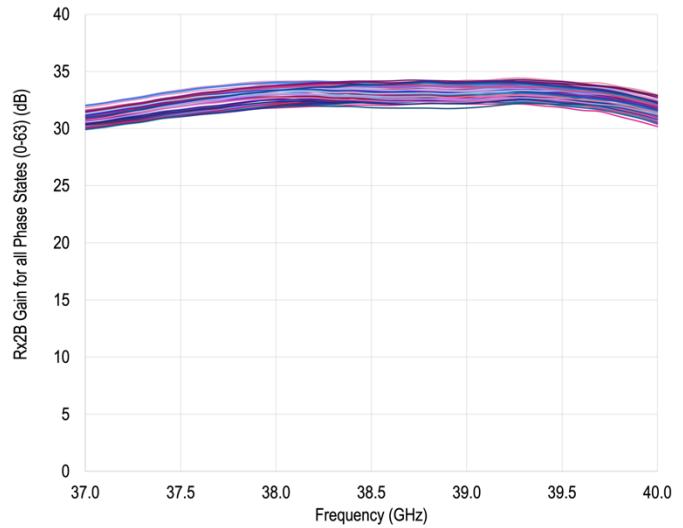


Figure 72: Rx2B Coherent Gain—all phase states

n260 Band 5G Tx/Rx Dual-Pol Quad Core BFIC

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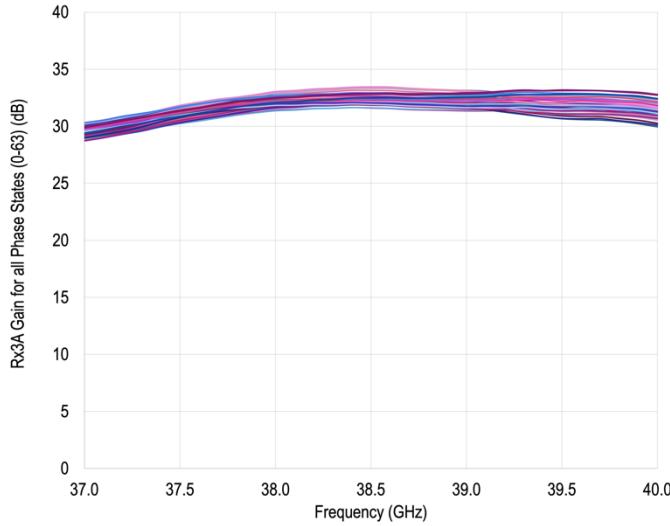


Figure 73: Rx3A Coherent Gain—all phase states

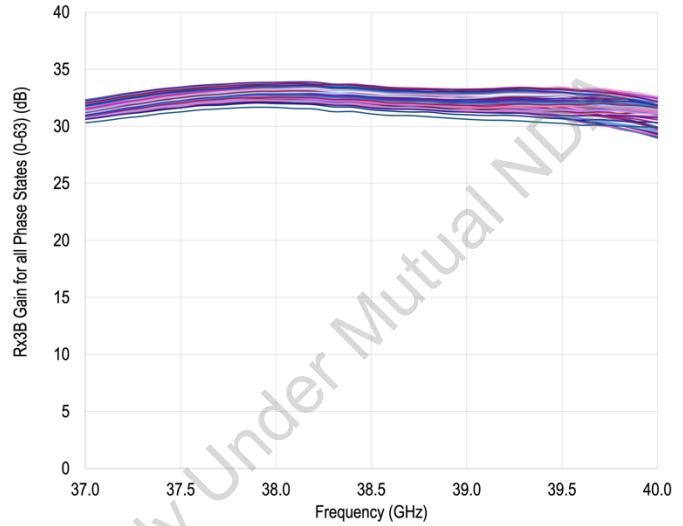


Figure 74: Rx3B Coherent Gain—all phase states

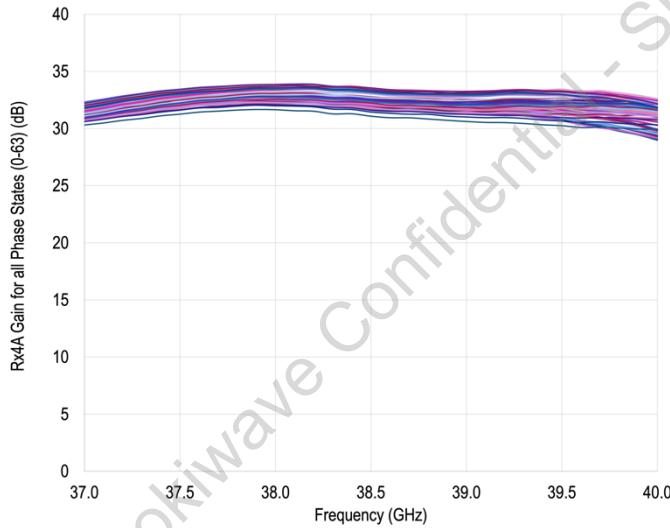


Figure 75: Rx4A Coherent Gain—all phase states

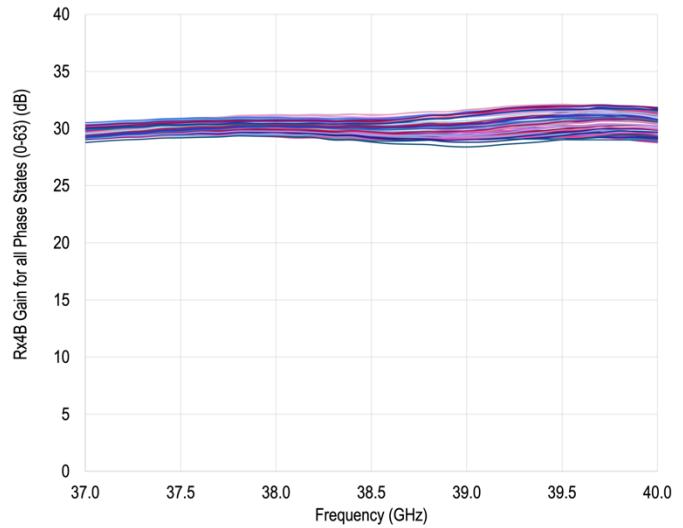
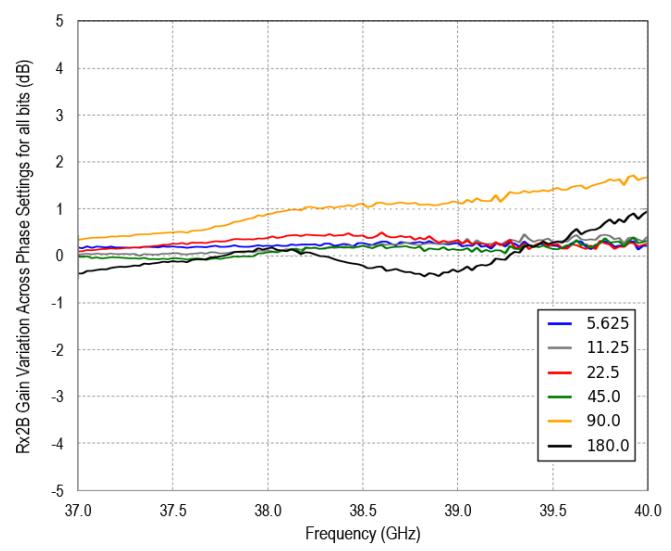
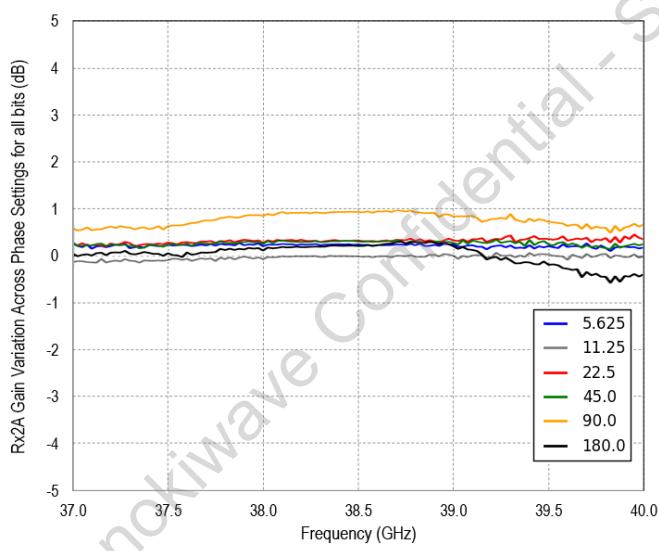
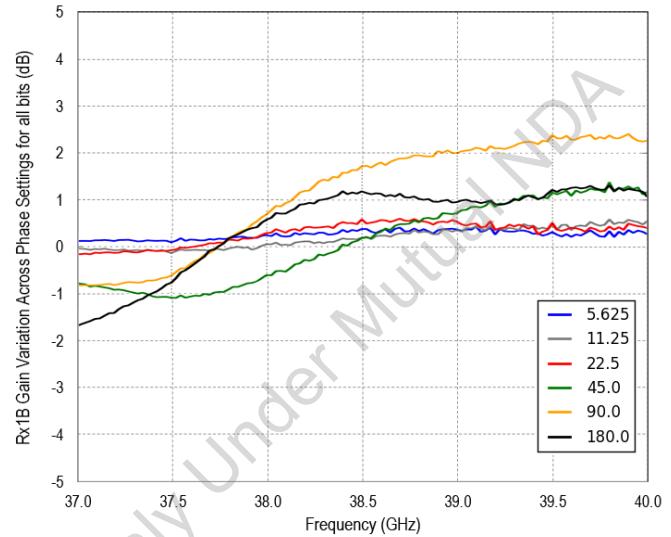
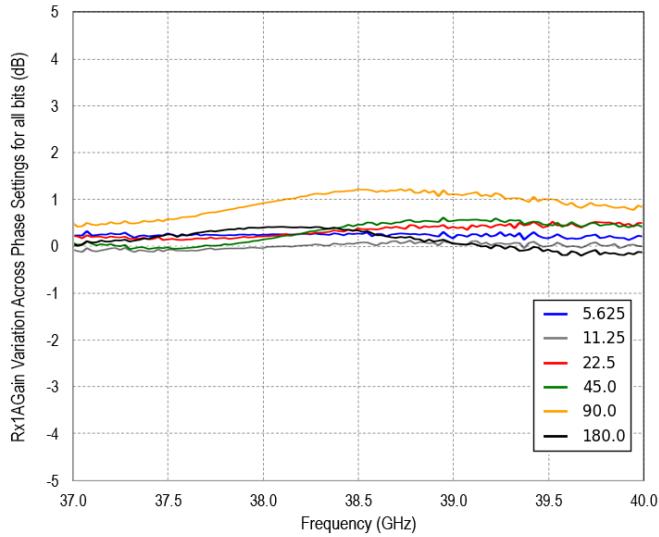


Figure 76: Rx4B Coherent Gain—all phase states

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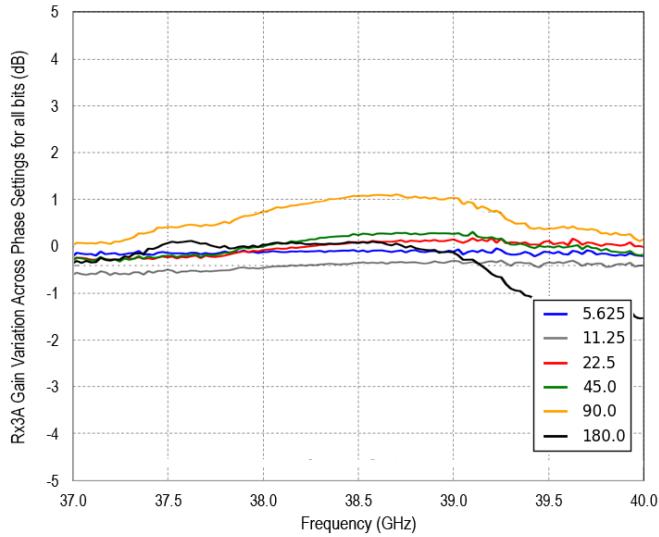


Figure 81: Rx3A Gain Variation Across Phase Settings per bit

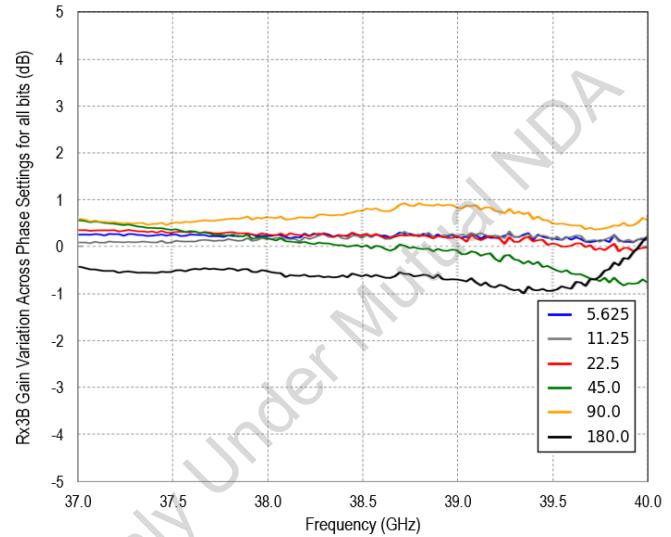


Figure 82: Rx3B Gain Variation Across Phase Settings per bit

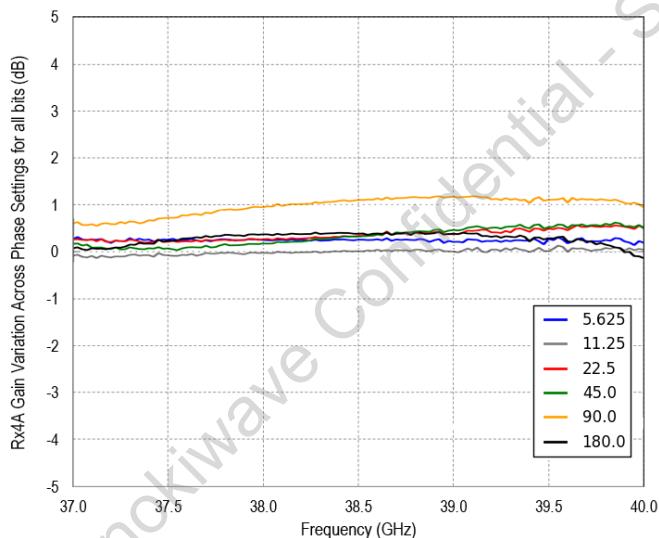


Figure 83: Rx4A Gain Variation Across Phase Settings per bit

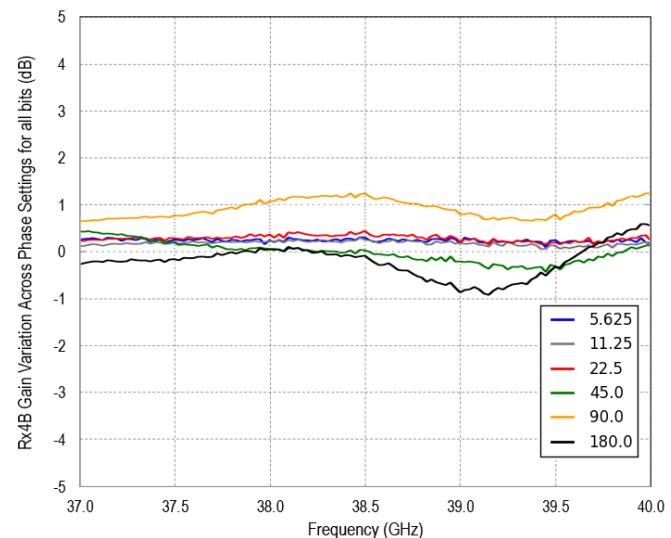


Figure 84: Rx4B Gain Variation Across Phase Settings per bit

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— Rx Gain Control Performance

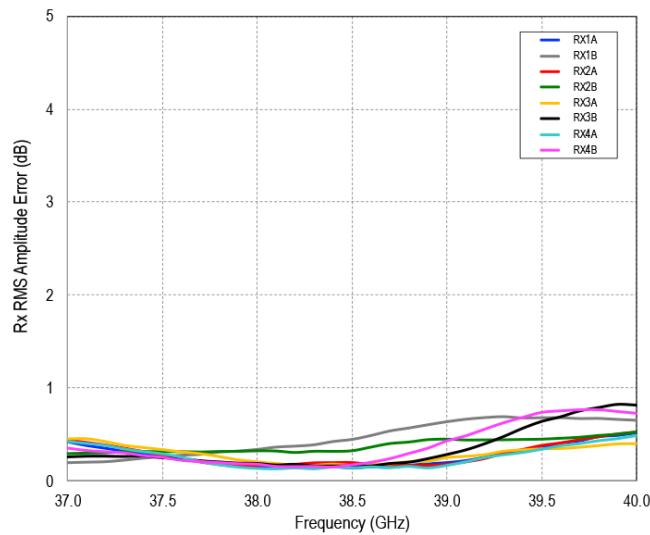


Figure 85: Rx RMS Amplitude Error

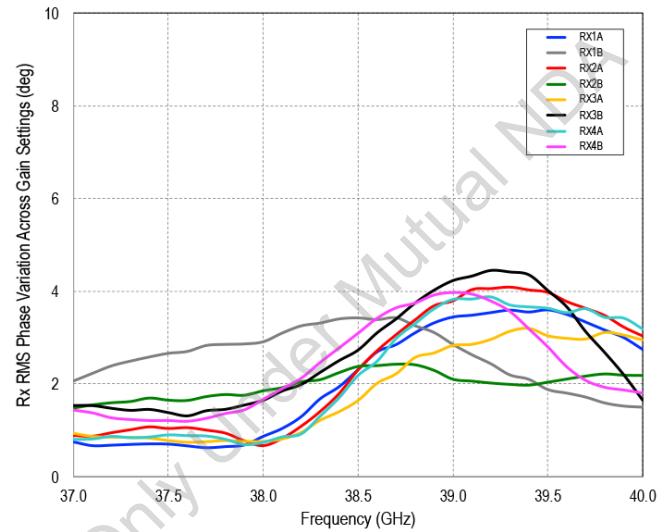


Figure 86: Rx RMS Phase Variation Across Gain Settings

n260 Band 5G Tx/Rx Dual-Pol Quad Core BFIC

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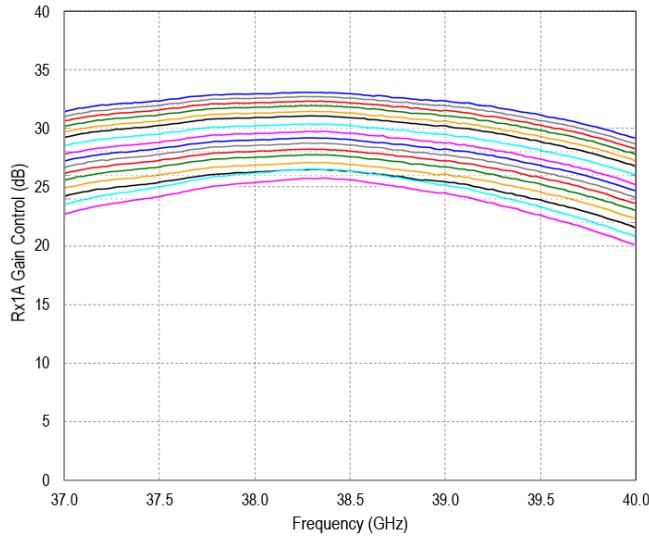


Figure 87: Rx1A Element Gain Control (0-15)

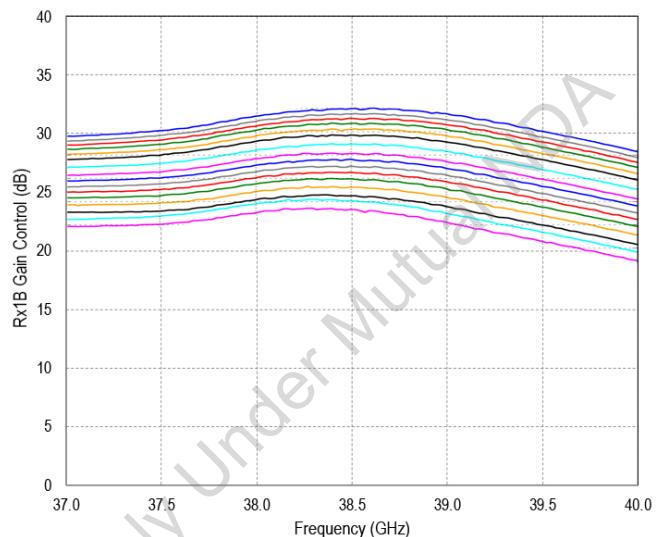


Figure 88: Rx1B Element Gain Control (0-15)

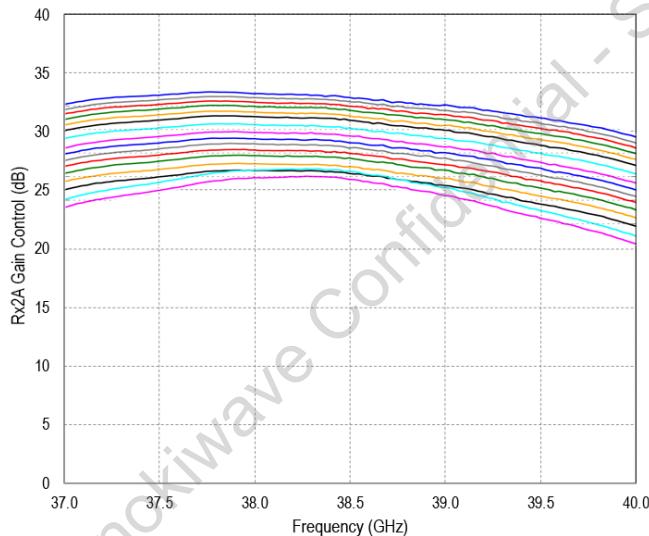


Figure 89: Rx2A Element Gain Control (0-15)

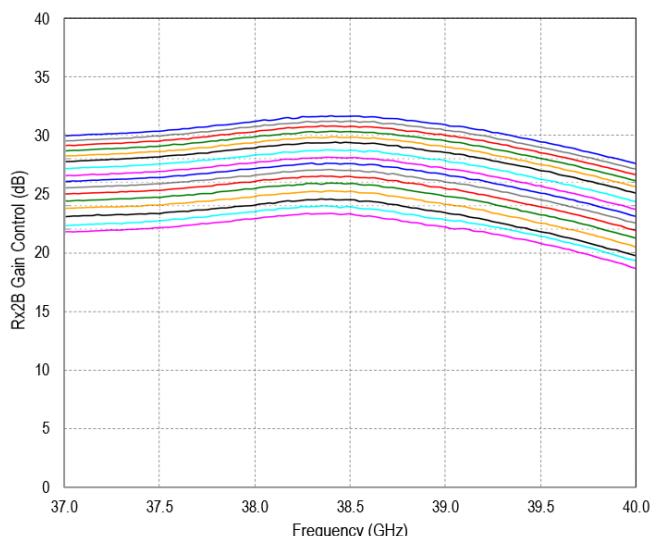


Figure 90: Rx2B Element Gain Control (0-15)

n260 Band 5G Tx/Rx Dual-Pol Quad Core BFIC

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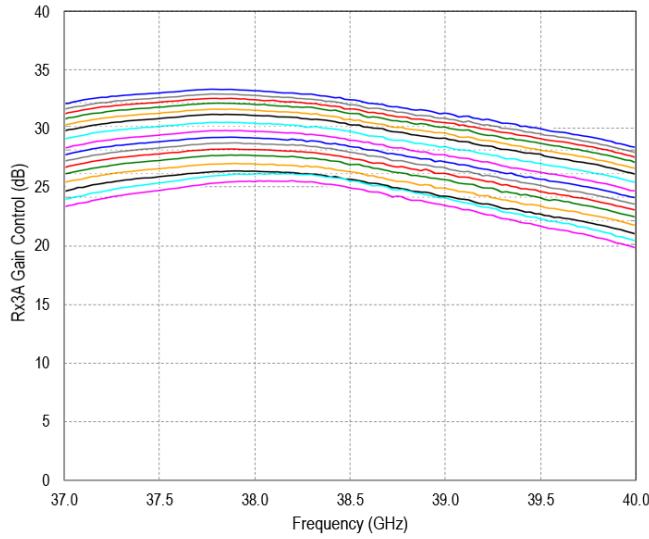


Figure 91: Rx3A Element Gain Control (0-15)

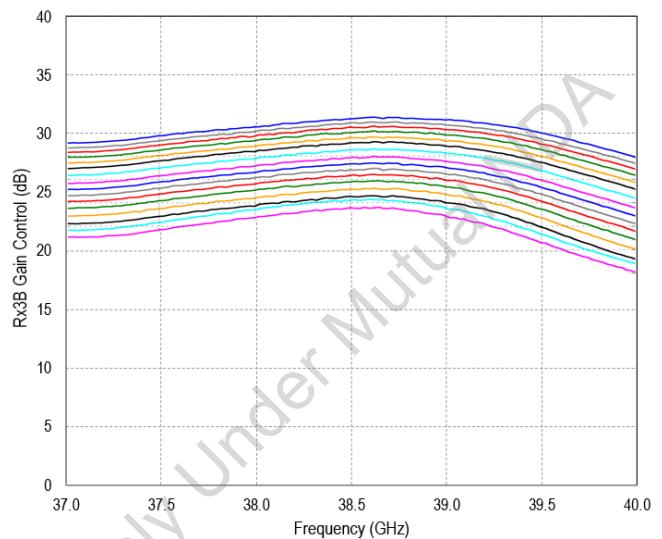


Figure 92: Rx3B Element Gain Control (0-15)

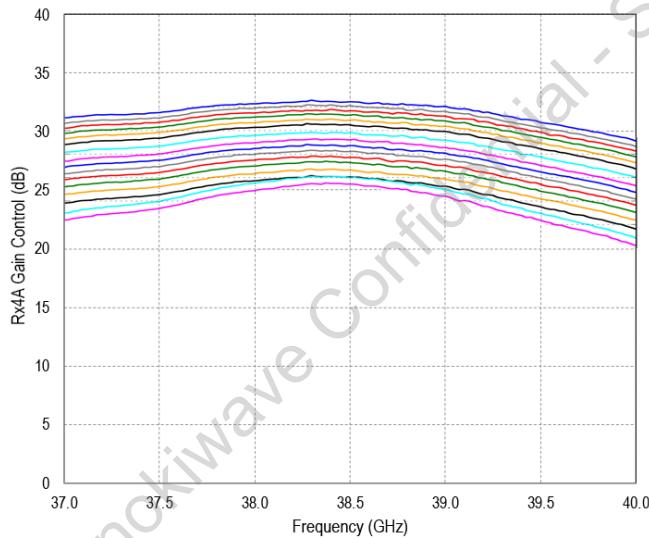


Figure 93: Rx4A Element Gain Control (0-15)

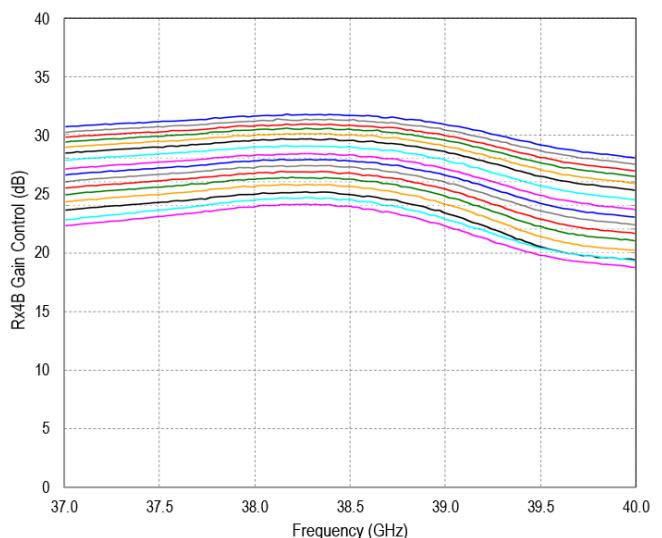


Figure 94: Rx4B Element Gain Control (0-15)

n260 Band 5G Tx/Rx Dual-Pol Quad Core BFIC

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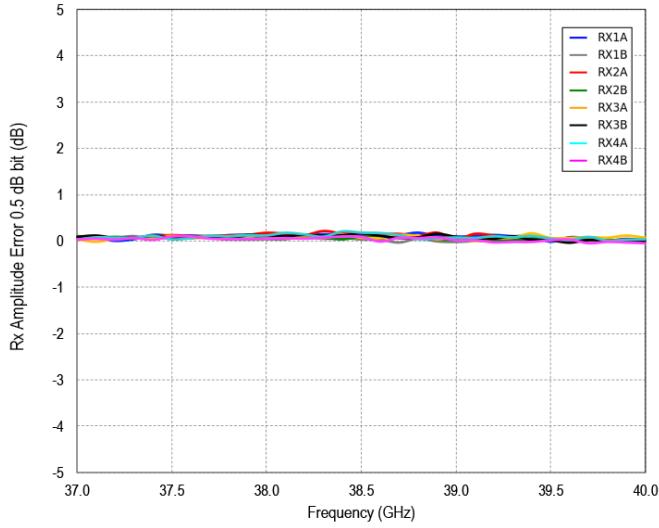


Figure 95: 0.5 dB Bit Rx Amplitude Error

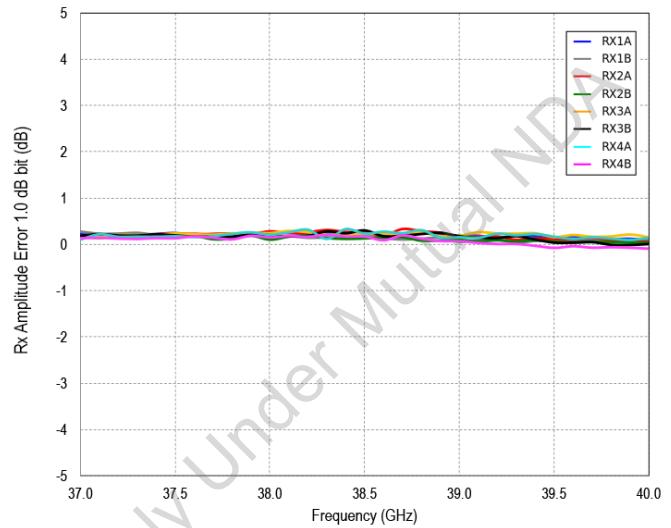


Figure 96: 1.0 dB Bit Rx Amplitude Error

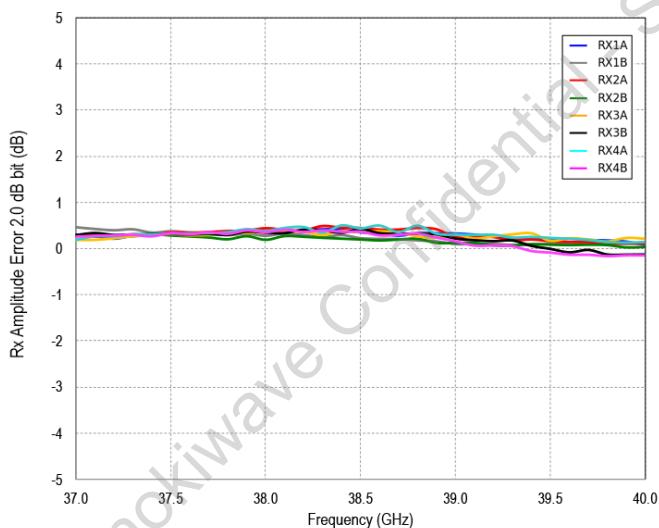


Figure 97: 2.0 dB Bit Rx Amplitude Error

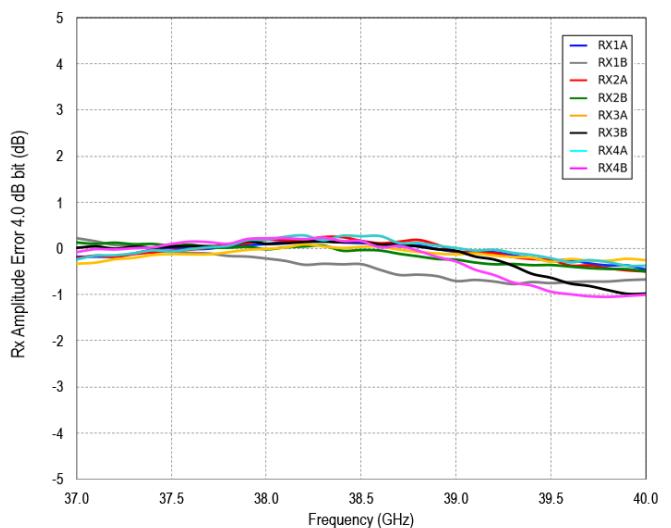


Figure 98: 4.0 dB Bit Rx Amplitude Error

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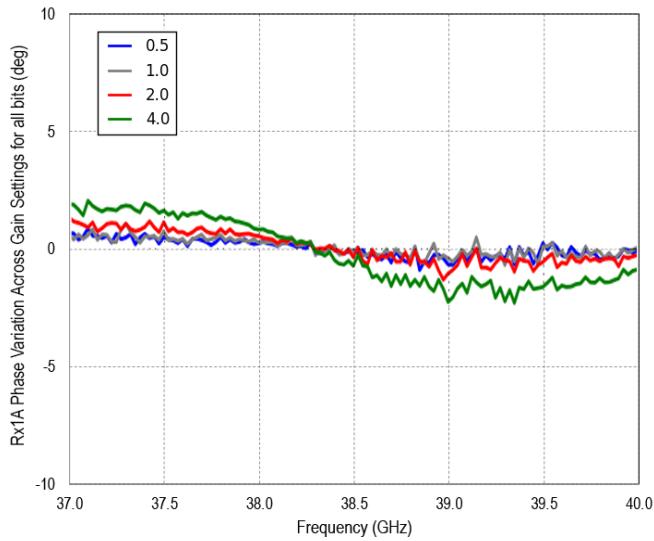


Figure 99: Rx1A Phase Variation Across Gain Settings per bit

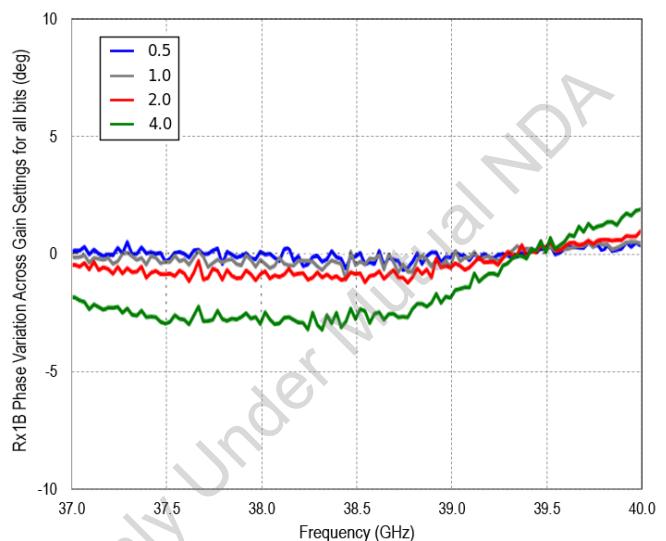


Figure 100: Rx1B Phase Variation Across Gain Settings per bit

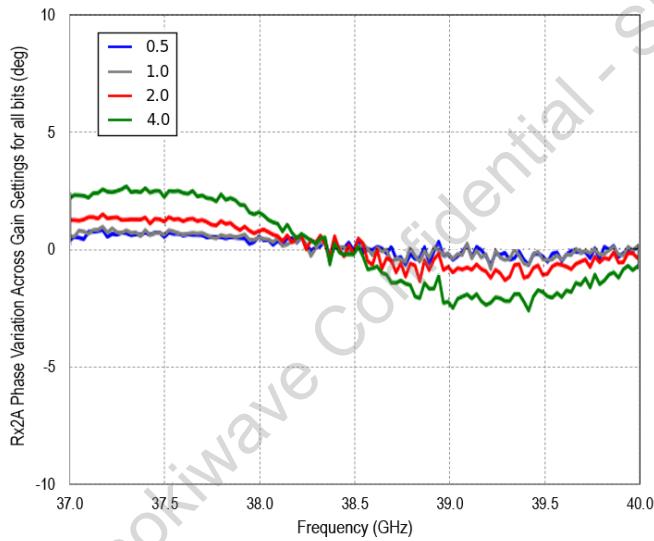


Figure 101: Rx2A Phase Variation Across Gain Settings per bit

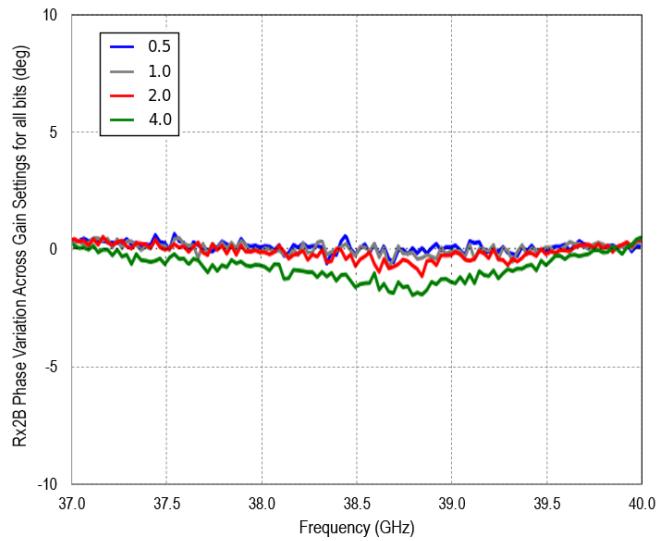


Figure 102: Rx2B Phase Variation Across Gain Settings per bit

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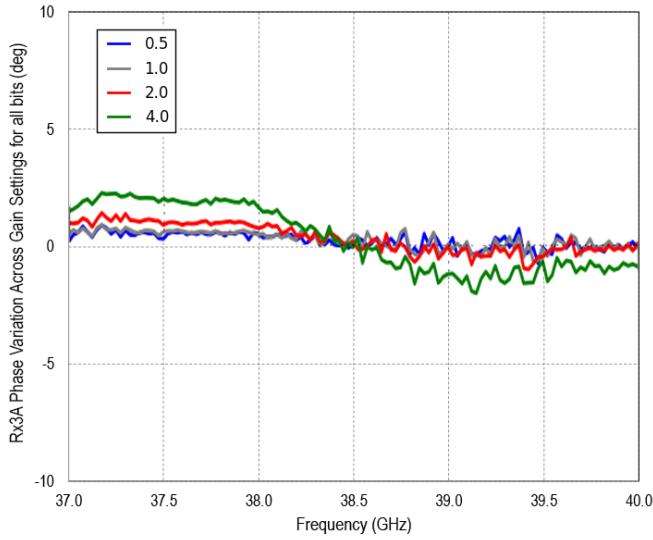


Figure 103: Rx3A Phase Variation Across Gain Settings per bit

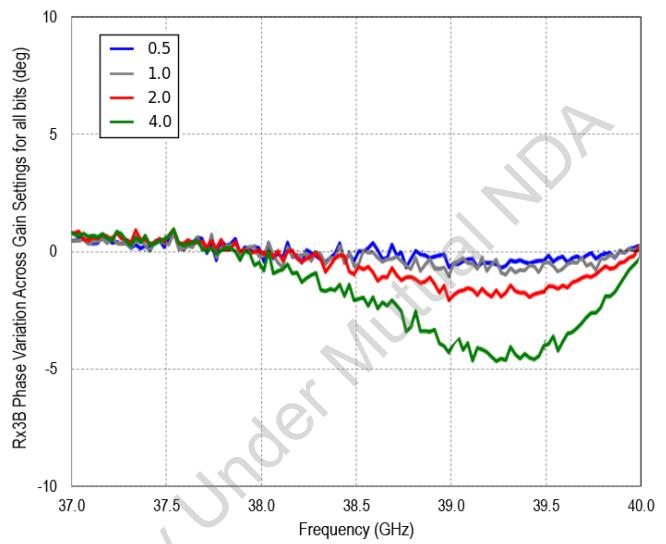


Figure 104: Rx3B Phase Variation Across Gain Settings per bit

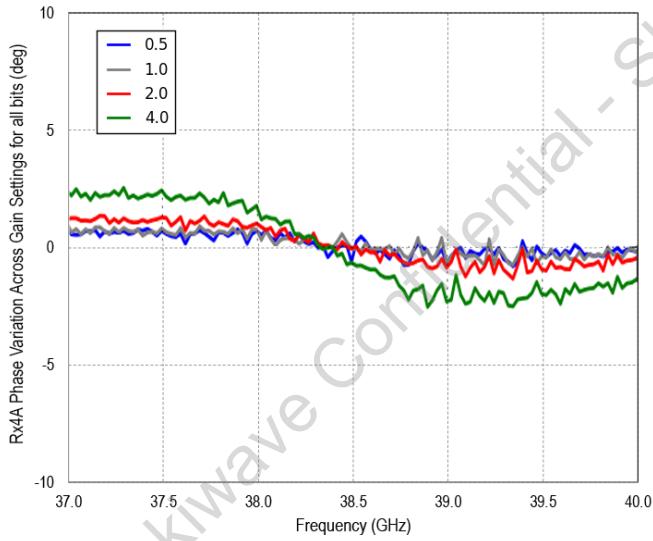


Figure 105: Rx4A Phase Variation Across Gain Settings per bit

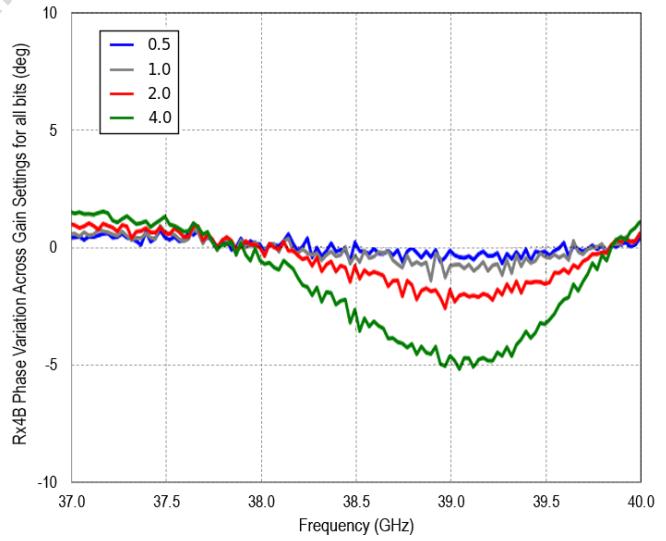


Figure 106: Rx4B Phase Variation Across Gain Settings per bit

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Applications Information

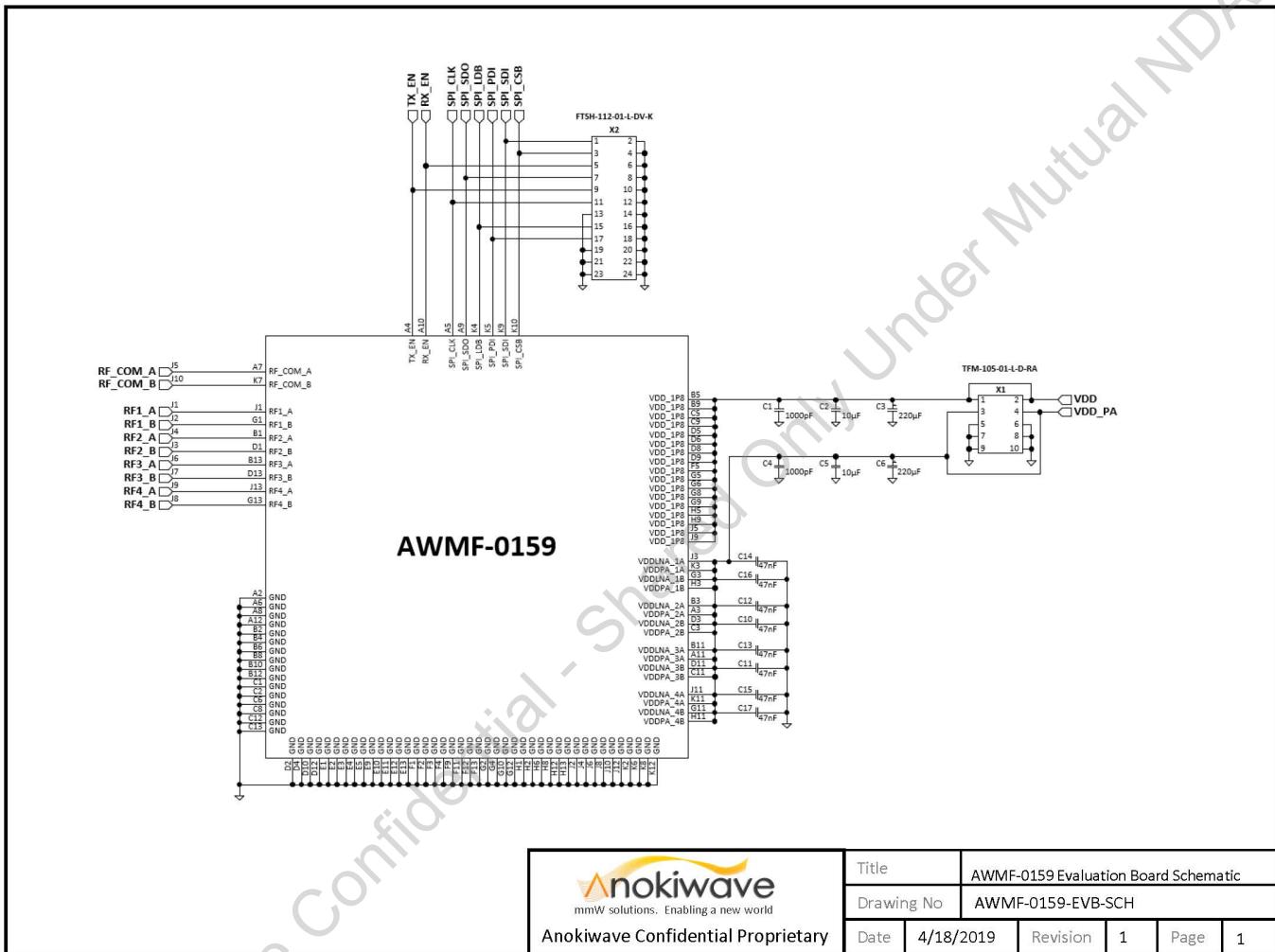


Figure 107: AWMF-0159 Evaluation Board Schematic

Document: AWMF-0159-DS

Rev. 3.1

Return to Electrical Specifications

ANOKIWAVE CONFIDENTIAL PROPRIETARY

Anokiwave reserves the right to make changes to the information contained herein without notice

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Outline Dimensions

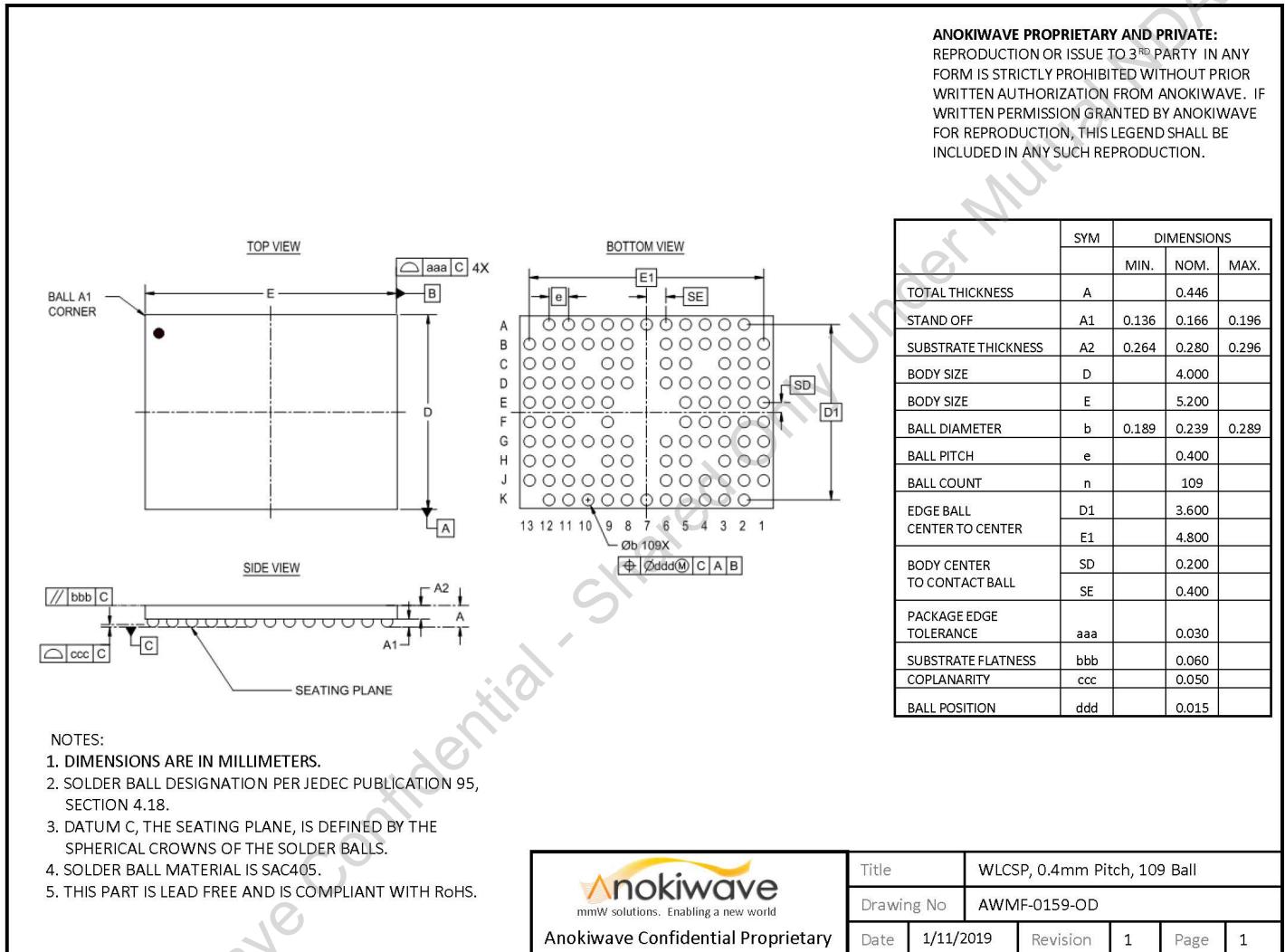


Figure 108: AWMF-0159 WLCSP Package Dimensions

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AWMF-0159 Developer Kit

The developer kits (AWMF-0159-DK, AWMF-0159-DL) include all hardware and software required to interface to the AWMF-0159. The kits enable full evaluation and RF testing of the developer kit with easily defined user interfaces. The test board has been carefully designed to easily replicate the performance of the device and to provide the necessary channel to channel isolation. Calibration data is included to enable the removal of test board line losses. The SPI control is supported through a high-speed cable, interposer board, and USB interface module. Driver software is supplied to provide control from a PC. DC power is supplied to the test board through a separate cable assembly. A full set of measured data is included to provide reference performance for each Developer Kit. Evaluation of the AWMF-0159 with the Developer Kits will significantly shorten the time to become familiar with the operation and performance of the product, thereby reducing system development time and cost.

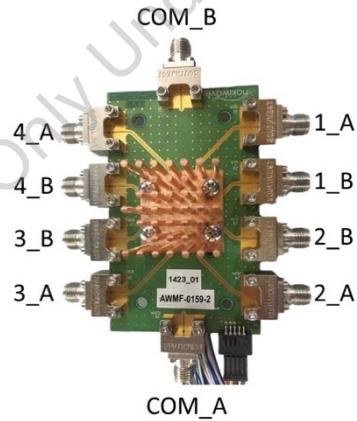


Figure 109. AWMF-0159 DK Contents and Evaluation Board

Developer Kit Contents

- 1 x Test board with 10 x RF connectors, 1 x DC connector, and 1 x SPI connector
- 1 x DC power cable assembly
- 1 x high speed SPI cable assembly
- 1 x SPI interposer board
- 1 x USB-SPI interface module
- 25 extra ICs (AWMF-0159-DK only)
- Gerber files, PCB layout support, and Anokiwave design assistance (AWMF-0159-DK only)
- SPI driver software
- Control software with User Guide, full test results, and board calibration
- 1 x Software Installation and Control Software User's Guide

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Ordering Guide

Model	Package	MSL Rating	Package Description	Package Option	Package Marking
AWMF-0159	WLCSP	1	5.2 mm x 4.0 mm WLCSP		AWMF-0159 ZZZZZZZ YYWWGHIJ KLMNOP_X
AWMF-0159-DK			Developer's Kit for evaluation (includes 25 additional ICs)		
AMSF-0159-DL			Developer's Kit Lite (without additional ICs)		