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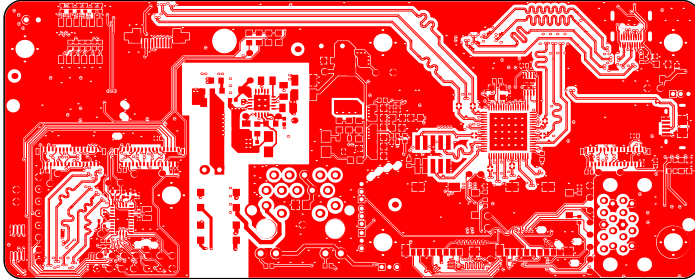
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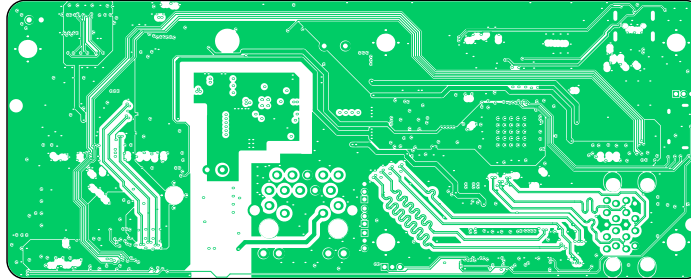
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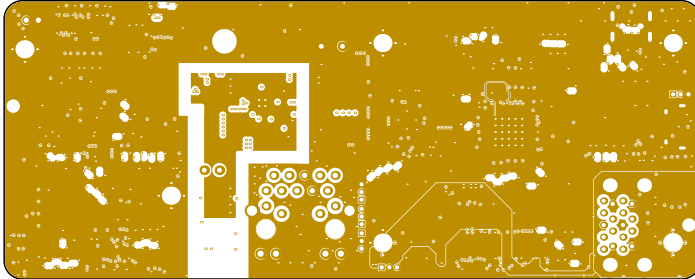
Top Copper (Scale 0.8)



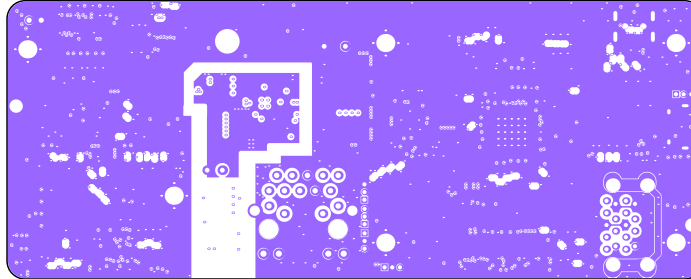
Signal Layer 1 (Scale 0.8)



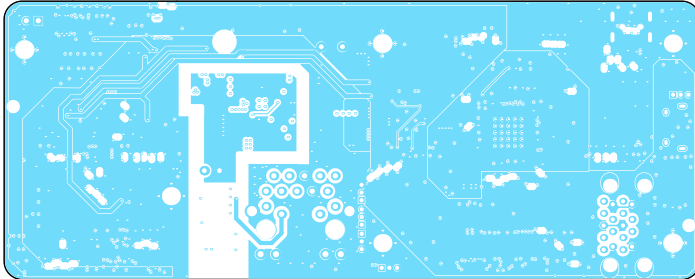
GND 1 (Scale 0.8)



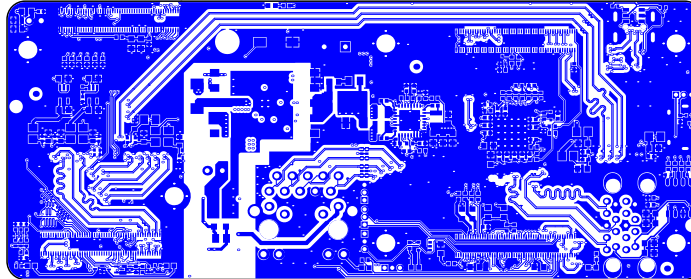
GND 2 (Scale 0.8)



PWR (Scale 0.8)



Bottom Copper (Scale 0.8)

**FABRICATION NOTES:**

Fabricate per IPC-6011 & IPC-6012 CLASS 2  
Inspect per IPC-A-600 CLASS 2  
Test per IPC-TM-650

- \* PCB has 6 copper layers
- \* Copper thicknesses are finished and include base foil plus Cu plating on plated layers.
- \* PCB thickness: Please refer to the Layer stack legend
- \* Min. trace width/clearance: 0.1mm/0.1mm
- \* Min. hole drill/ring: 8mil/16mil
- \* Soldermask gang relief is allowed for pads in same footprint, if footprint is NSMD.
- \* Silkscreen, non-conductive epoxy ink, color: white
- \* Solder mask color: black
- \* Remove slikscreen as needed to prevent ink on any exposed copper
- \* Surface finish: ENIG
- \* Hole dimensions are finished size, +/-3mil
- \* Linear board dimension tolerance: +/-10mil
- \* Bow, twist, warp not to exceed 0.75% of greatest diagonal span
- \* PCB shall be UL Recognized printed wiring board (ZPMV2), minimum flammability rating 94V-0
- \* PCB shall be marked with fabricator company or trade name, UL mark, and date code using legend ink on secondary side
- \* All PCBs shall be electrically tested for opens and shorts per gerber. Test marking shall be marked on secondard side.
- \* GM1 layer should be used as board outline

Fabricator shall panelize the PCB using mouse bites and tab routing. V-scoring not allowed.

Controlled impedance differential pairs shall be within +/-10% for 100ohm targets, and +/-10% for 90ohm targets. See Sheet 3 for transmission line details and location of 90ohm differential pairs.

Title: **DM2097**

Number: D0000200

Revision: R0M0  
E0

Date: 17/08/2021

Sheet: 1 of 3

Drawn by: David Malovrh

**LUXonjs**

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## Layer Stack Legend

Layer	Thickness	Type	Gerber	Df	Dk
Top Overlay		Legend	GTO		
Top Mask	0.59mil(0.015mm)	Solder Mask	GTS		3,8
Top Copper	1.38mil(0.035mm)	Signal	GTL		
	3.94mil(0.100mm)	Dielectric			4,05
GND 1	0.71mil(0.018mm)	Signal	G1		
	22.24mil(0.565mm)	Dielectric			4,5
PWR	0.71mil(0.018mm)	Signal	G2		
	5.00mil(0.127mm)	Dielectric			4,25
Signal Layer 1	0.71mil(0.018mm)	Signal	G3		
	22.24mil(0.565mm)	Dielectric			4,5
GND 2	0.71mil(0.018mm)	Signal	G4		
	3.94mil(0.100mm)	Dielectric			4,05
Bottom Copper	1.38mil(0.035mm)	Signal	GBL		
Bottom Mask	0.59mil(0.015mm)	Solder Mask	GBS		3,8
Bottom Overlay		Legend	GBO		
Total thickness: 64.13mil(1.629mm)					

Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
✖	25	7.87mil(0.200mm)	Plated	
✱	875	8.00mil(0.203mm)	Plated	
✴	24	10.00mil(0.254mm)	Plated	
□	2	19.69mil(0.500mm)	Plated	
◎	2	21.65mil(0.550mm)	Plated	
▽	4	25.59mil(0.650mm)	Plated	
□	33	27.56mil(0.700mm)	Plated	
☆	4	31.50mil(0.800mm)	Plated	
◇	2	31.89mil(0.810mm)	Non-Plated	
◇	2	33.86mil(0.860mm)	Plated	
✖	14	35.43mil(0.900mm)	Plated	
✱	4	40.16mil(1.020mm)	Plated	
✴	2	66.93mil(1.700mm)	Plated	
✱	2	78.74mil(2.000mm)	Non-Plated	
○	4	90.55mil(2.300mm)	Plated	
✖	2	102.36mil(2.600mm)	Plated	
⊕	6	118.11mil(3.000mm)	Plated	
⊕	2	125.98mil(3.200mm)	Plated	
	1009 Total			

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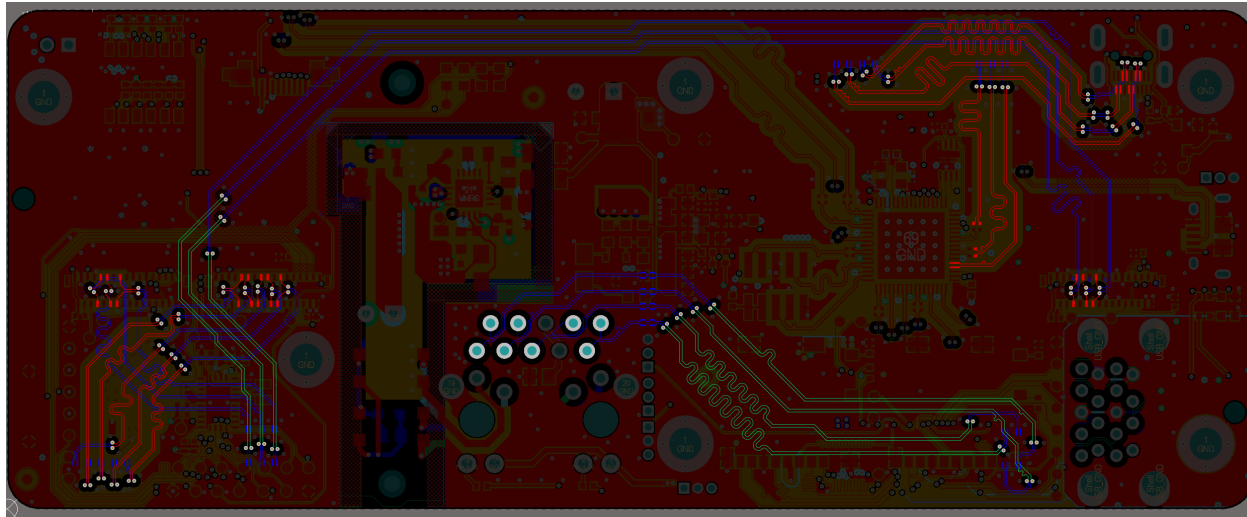
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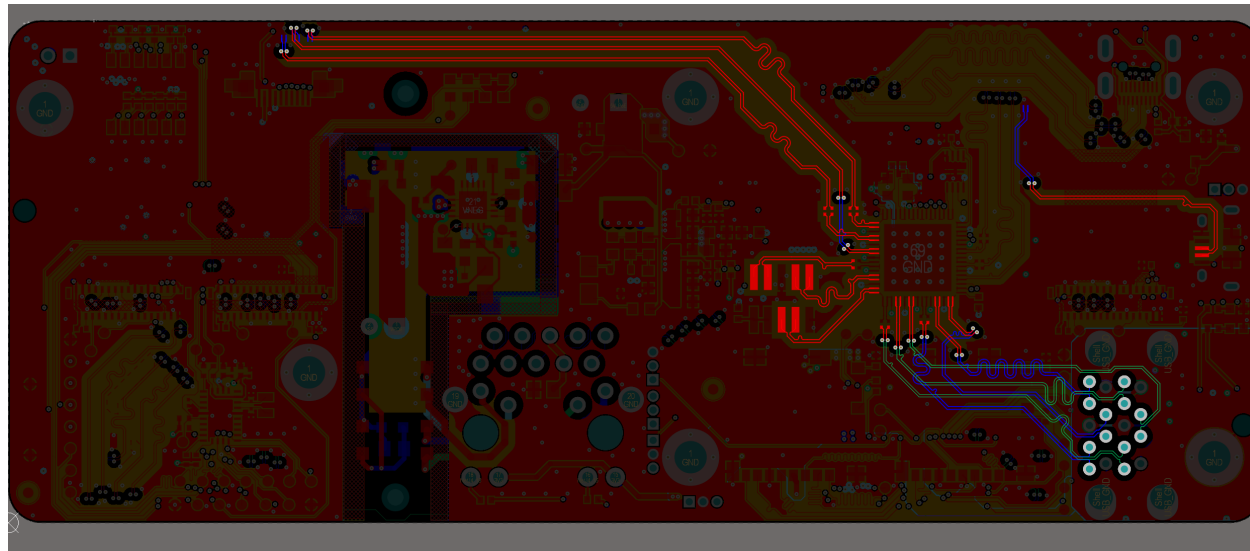
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100 OHM (+/-10%) DIFF PAIRS



90 OHM (+/-10%) DIFF PAIRS



Transmission Line Structure Table

Impedance Id	Target Impedance	Trace layer	Lower Trace Width	Upper Trace Width	Gap	Reference layers
1	100	Top Copper	4.0mil(0.101mm)	4.0mil(0.101mm)	5.0mil(0.127mm)	GND 1
2	90	Top Copper	5.5mil(0.140mm)	5.5mil(0.140mm)	5.0mil(0.127mm)	GND 1
5	100	Signal Layer 1	4.0mil(0.101mm)	4.0mil(0.101mm)	6.3mil(0.160mm)	PWR,GND 2
6	90	Signal Layer 1	4.0mil(0.102mm)	4.0mil(0.102mm)	4.1mil(0.104mm)	PWR,GND 2
7	100	Bottom Copper	4.0mil(0.101mm)	4.0mil(0.101mm)	5.0mil(0.127mm)	GND 2
8	90	Bottom Copper	5.5mil(0.140mm)	5.5mil(0.140mm)	5.0mil(0.127mm)	GND 2

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