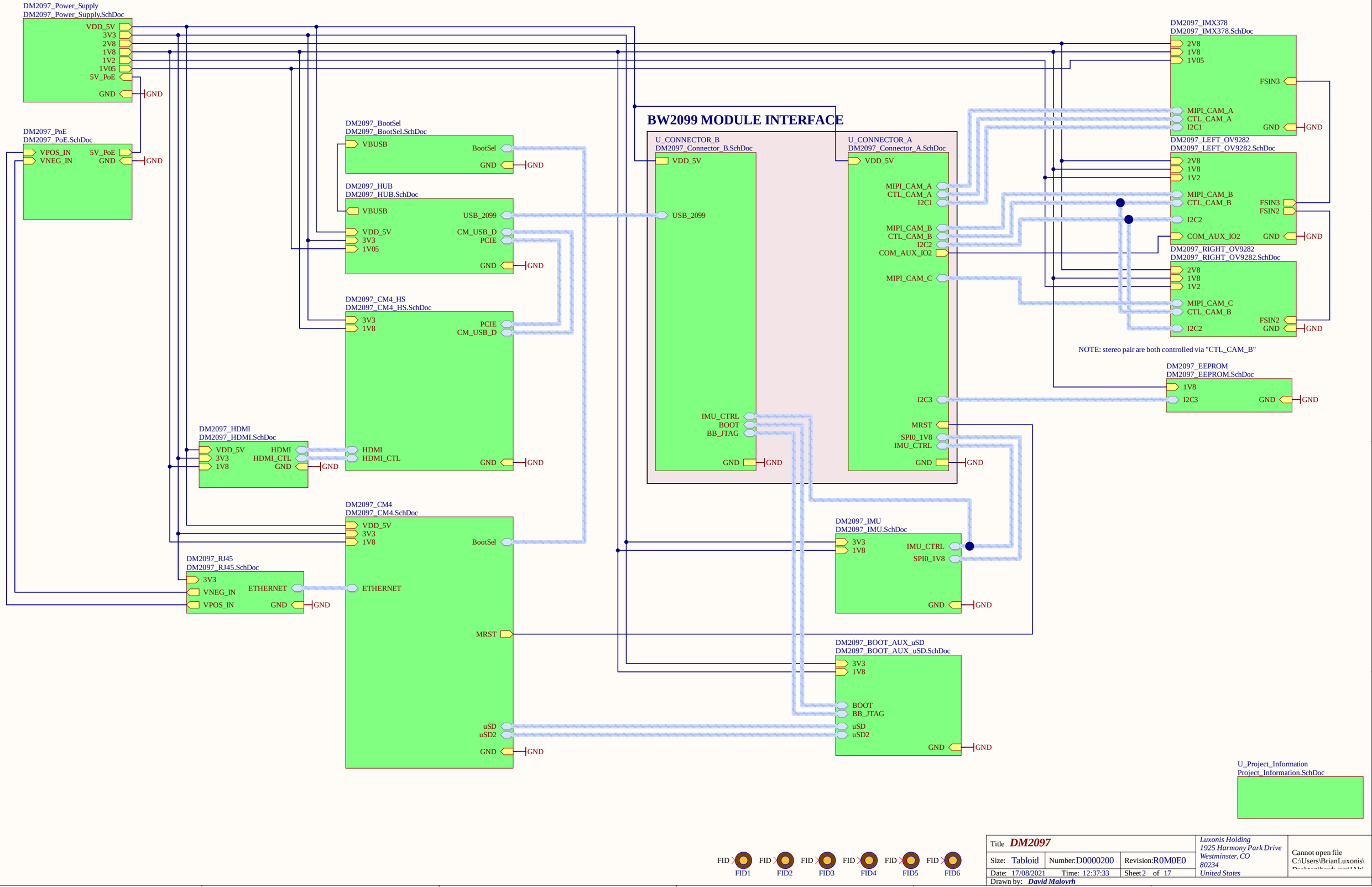
Project: DM2097
Current Revision: R0M0E0

DM2097 Revision History:

12/11/2020	R0M0E0	Initial release	
04/05/2021	R0M0E0 -> R1M1E1	1) Add PoE support so that device can be used remotely and in an eclosure 2) Design board to be easly enclosed 3) Add USB3 support for faster transfer rate betweem SoMs 4) Add IMU 5) Update all leveraged errors from previous designs	1) Imported PoE circuitry from LUX-D-PoE designs 2) Made sure that only necessary connectors are populated and used on this design 3) Added PCIe to USB3 hub 4) Implemented IMU design used on other base boards 5) Updated IMX378 footprint to 1.6mm PCB compatible, updated sync circuitry
04/05/2021	DM1097_R1M1E1 -> DM2097_R0M0E0	1) Correct the USB connection to the SoM (swapped RX and TX) add AC caps for SSTX from USB hub to SoM 2) Incorporate new Arducam FPC/connector design for CCMs 3) Add another uSD socket for mass storage 4) Add EEPROM for board info memory	1) Swapped RX and TX and added AC caps for SSTX from USB hub to SoM 2) New Arducam FPC/connector design for CCMs 3) Added another uSD socket 4) Added EEPROM

Title	***DM2097***			*Luxonis Holding* *1925 Harmony Park Drive* *Westminster, CO* *80234* *United States*
Size: Tabloid	Number: D0000200	Revision: R0M0E0		Cannot open file C:\Users\BrianLuxonis\
Date: 17/08/2021	Time: 12:37:33	Sheet 1 of 17		
Drawn by: ***David Malovrh***				



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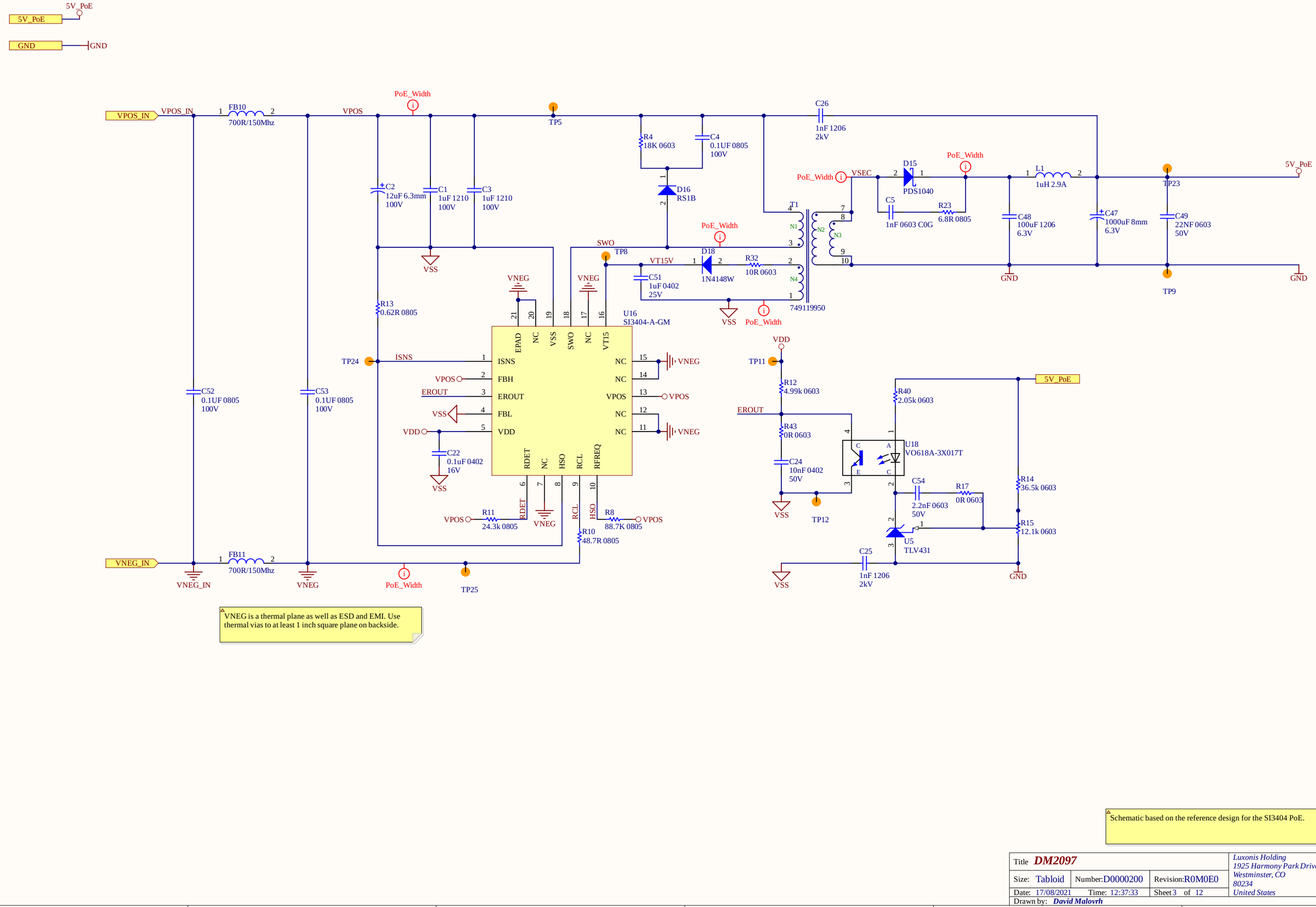
Size: Tabloid	Number: D0000200	Revision: R0M0E0	Cannot open file C:\Users\BrianLuxonis\
Date: 17/08/2021	Time: 12:37:33	Sheet 2 of 17	
Drawn by: David Malovrh			



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Size: Tabloid	Number: D0000200	Revision: R0M0E0	Cannot open file C:\Users\BrianLuxonis\
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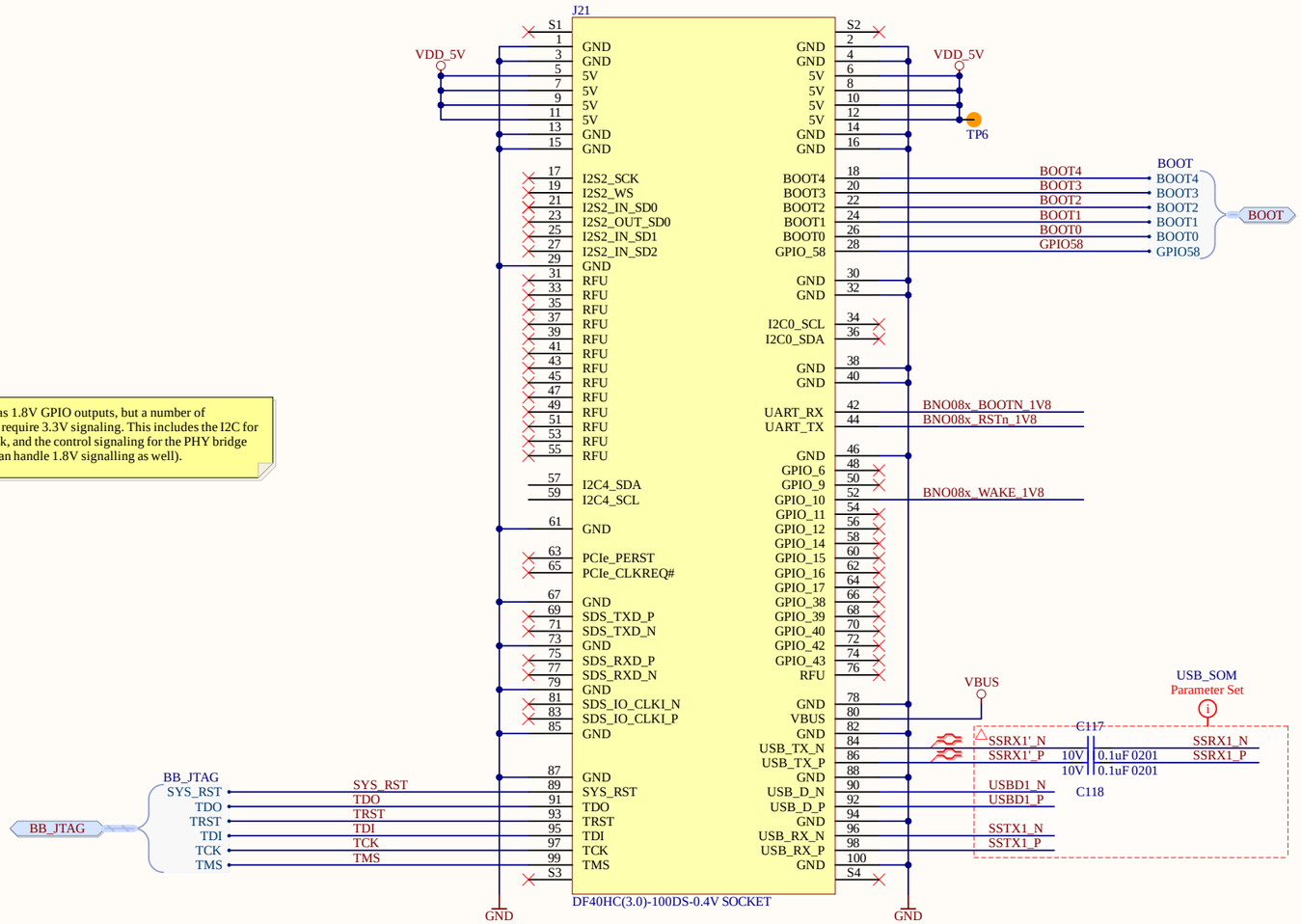
Drawn by: David Malovrh			

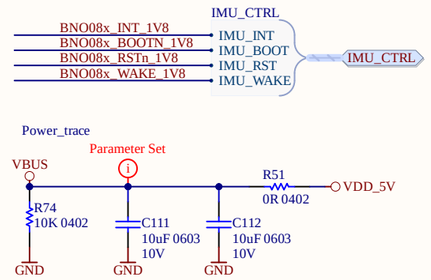
VDD_5V

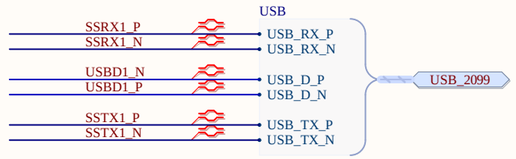
GND

BW2099 CONNECTOR B



The Myriad X (MX) has 1.8V GPIO outputs, but a number of PCIe-related functions require 3.3V signaling. This includes the I2C for the PCIe reference clock, and the control signaling for the PHY bridge (though RTL8111HS can handle 1.8V signalling as well).





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Size: Tabloid	Number: D0000200	Revision: R0M0E0	Cannot open file C:\Users\BrianLuxonis\
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Drawn by: ***David Malovrh***			

SMT mounting standoffs for module and for CM4

MTG5 MTG6 MTG7 MTG8 MTG9 MTG10

GND

MIPI Lanes:
DPHYv1.2
Max 2.1 Gbps / lane

MIPI_CAM_A

1099 only accepts 1.8V input on GPIOs. Must protect these lines for the 3.3V CM3 GPIO case.

Parameter Set

J1

DF40HC(3.0)-100DS-0.4V SOCKET
798-DF40HC30100DS451

VDD_5V

R21 1K 0402

D11 ORANGE 0603

2485_PGOOD — Q2 RE1C002UNTCL

Mark "2485_PGOOD" on PCB

MODULE_nRST is pulled to 1.8V on BW1099.

MRST — GPIO1/MRST — R18 470R 0402 — M1 RE1C002UNTCL — R75 10K 0402

R108 1K 0402

D12 ORANGE 0603

MODULE_nRST_1 — Q6 RE1C002UNTCL

Mark "nRST" on PCB

Note on silk that this button only resets the BW1099.

B1 Off-Mom, 50mA — R50 10K 0402

BW2099 PD WAKEUP

GPIO33/MRST toggled high will put the 1099 module into RST.

Default GPIO33 is low (internal PD).

MIPI_CAM_A

MIPI_RX4_C_N / MIPI_RX4_C_P
MIPI_RX4_D0_N / MIPI_RX4_D0_P
MIPI_RX4_D1_N / MIPI_RX4_D1_P
MIPI_RX5_D0_N / MIPI_RX5_D0_P
MIPI_RX5_D1_N / MIPI_RX5_D1_P

I2C1 — I2C1_SDA / I2C1_SCL

2485_PGOOD
MODULE_nRST
2485_WAKEUP

CTL_CAM_B — CAM_B_D_PWM / CAM_B_PWDN_N / CAM_B_CLK

BNO08x_INT_1V8

I2C2 — I2C2_SCL / I2C2_SDA

MIPI_CAM_B — MIPI_RX2_D1_N / MIPI_RX2_D1_P / MIPI_RX2_D0_N / MIPI_RX2_D0_P / MIPI_RX2_C_N / MIPI_RX2_C_P

Parameter Set MIPI_CAM_B

SD_HST0_CD
SD_HST0_CLK
SD_HST0_CMD

CAM_B_CLK

CAM_A_CLK
CAM_A_PWDN_N
SD_HST0_D3
SD_HST0_D2
SD_HST0_D1
SD_HST0_D0
COM_AUX_IO2

TP10

CTL_CAM_A — CAM_A_CLK / CAM_A_PWDN_N

SP0_1V8 — GPIO8/SPI0_CS_1 / SPI0_SIO0 / SPI0_SIO1 / SPI0_SIO2 / SPI0_SIO3 / SPI0_CS_0 / SPI0_SCK

I2C3 — I2C3_SCL / I2C3_SDA

MIPI_CAM_C — MIPI_RX3_D1_N / MIPI_RX3_D1_P / MIPI_RX3_D0_N / MIPI_RX3_D0_P / MIPI_RX3_C_N / MIPI_RX3_C_P

Parameter Set MIPI_CAM_C

AUX IO TESTPOINTS

MODULE_nRST TP49
2485_PGOOD TP50
2485_WAKEUP TP51
I2C3_SCL TP52
I2C3_SDA TP53
TP54
TP55

SPI
Parameter Set

SPI TESTPOINTS

SPI0_SIO0 TP1
SPI0_SIO1 TP3
SPI0_SIO2 TP14
SPI0_SIO3 TP15
SPI0_SCK TP17
SPI0_CS_0 TP18
GPIO8/SPI0_CS_1 TP19
TP20
TP21
TP22

SDIO
Parameter Set

3.3V SD TESTPOINTS

SD_HST0_D0 TP26
SD_HST0_D1 TP27
SD_HST0_D2 TP28
SD_HST0_D3 TP29
SD_HST0_CLK TP30
SD_HST0_CMD TP31
SD_HST0_CD TP32
TP33
TP46
TP47

IMU_CTRL — IMU_INT / IMU_BOOT / IMU_RST / IMU_WAKE — BNO08x_INT_1V8 / BNO08x_BOOTN_1V8 / BNO08x_RSTn_1V8 / BNO08x_WAKE_1V8

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Drawn by: David Malovrh		

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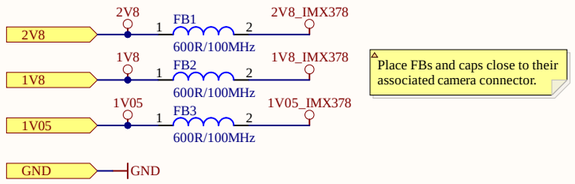
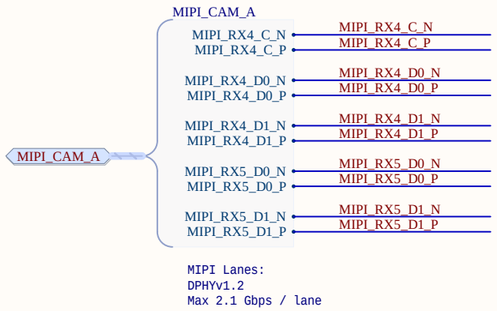


Place FBs and caps close to their associated camera connector.

On the BW1097, the IMX378 camera module is hardwired into the "Cam-A" logical position. This means the logic which used to be required to support the module being plugged into different physical connectors (and different logical positions) is no longer needed and can be removed.

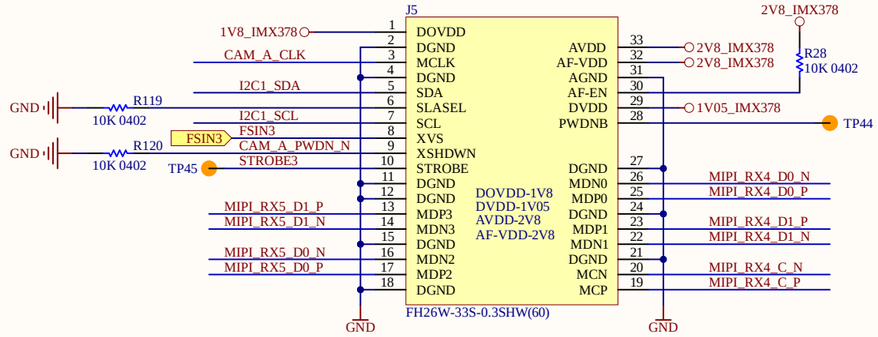
Note: It is still a limitation that the clock source for the cameras must be shared between CAMA/C and CAMB/D.

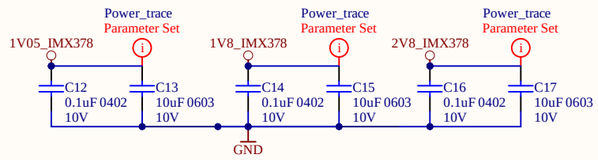


MIPI Lanes:
DPHYv1.2
Max 2.1 Gbps / lane

IMX378 MODULE CONNECTOR

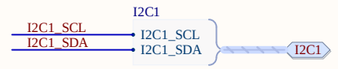
MODULE & SENSOR INFORMATION			
MODULE	A12N02A-201	I2C Clock Rate	1000 kHz Max
SENSOR	IMX378-AAQH5-C 12.3 Mega pixel CMOS 1/2.3 inch	I2C Address (8 bits)	0x34 (Sensor) 0x18 (VCM driver) 0xA0 (EEPROM driver)
MAX RESOLUTION	4056x3040	Sensor Clock Input	6 - 27 MHz

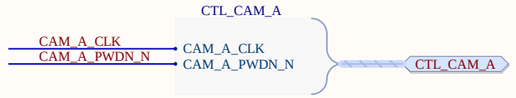




Supply Information

Supply Name		Voltage	Max Current
Module	Sensor		
AVDD	VANA	C_2.8V ± 0.1	55mA
DOVDD	VIF	C_1.8V ± 0.1	2.5mA
DVDD	VDIG	C_1.05V ± 0.1	446mA





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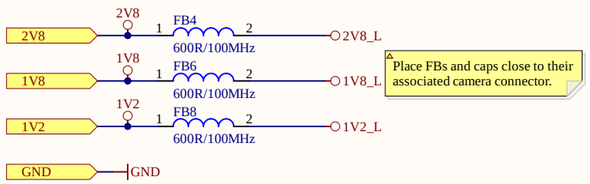
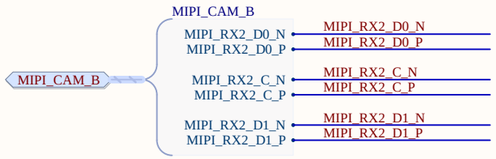
Drawn by: ***David Malovrh***			



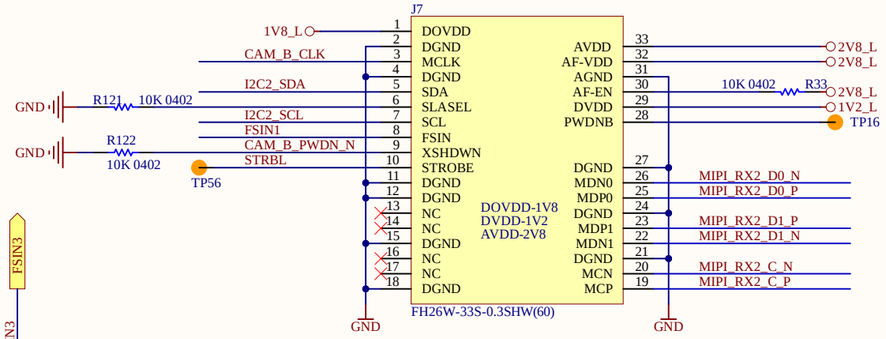
MODULE & SENSOR INFORMATION			
MODULE	TG161B-201 OR AN01V32-0JG	I2C Clock Rate	400 kHz Max
SENSOR	OV09282-GA4A B&W 1 Mega pixel CMOS 1/4 inch	I2C Address (8 bits)	0xC0(W) 0xC1(R)
MAX RESOLUTION	1280X800	Sensor Clock Input	6 - 64 MHz (24 MHz typ.)

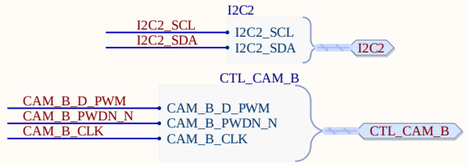
Supply Information

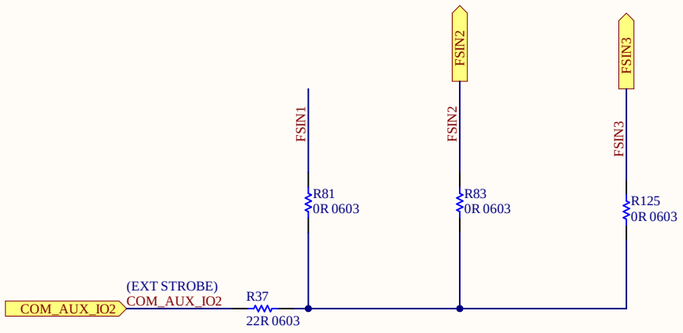
Supply Name		Voltage	Max Current
Module	Sensor		
DOVDD	VDD-IO	1.8V	2.5mA
DVDD	VDD-D	1.2V	52mA
AVDD	VDD-A	2.8V	24mA



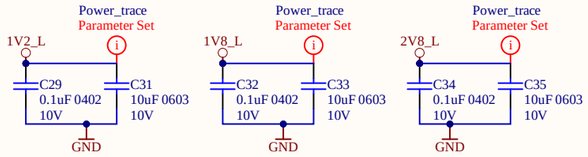
Mark "LEFT" on PCB
Place so that is the module's left camera.







Camera timing Sync Option



CAMERA CONNECTOR RESET CONNECTION TABLE

	CAMERA CONNECTOR		
	CAM_B	CAM_C	CAM_D
	CAM_PWDN	CAM_PWDN	CAM_PWDN
	CAM_PWM	CAM_AUX_IO1	CAM_AUX_IO1

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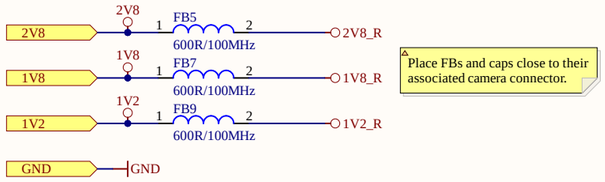
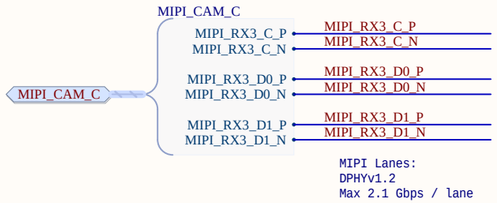


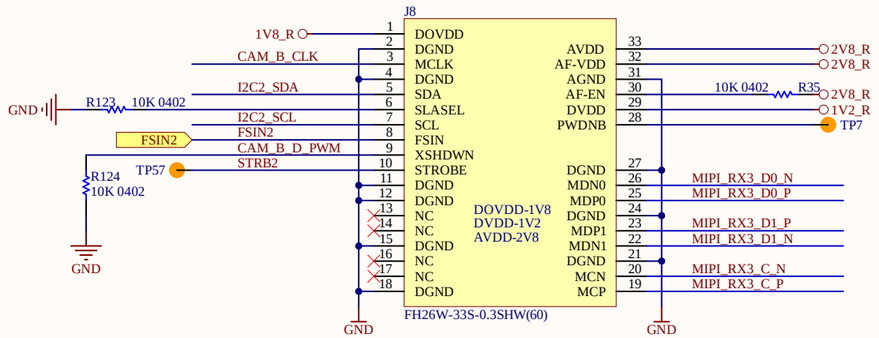
MODULE & SENSOR INFORMATION			
MODULE	TG161B-201 OR AN01V32-0JG	I2C Clock Rate	400 kHz Max
SENSOR	OV09282-GA4A B&W 1 Mega pixel CMOS 1/4 inch	I2C Address (8 bits)	0xC0(W) 0xC1(R)
MAX RESOLUTION	1280X800	Sensor Clock Input	6 - 64 MHz (24 MHz typ.)

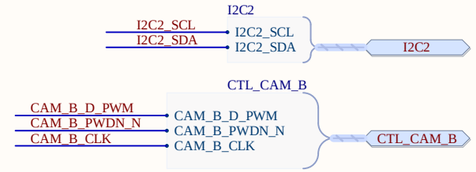
Supply Information

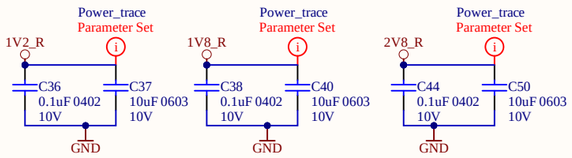
Supply Name		Voltage	Max Current
Module	Sensor		
DOVDD	VDD-IO	1.8V	2.5mA
DVDD	VDD-D	1.2V	52mA
AVDD	VDD-A	2.8V	24mA

Mark "RIGHT" on PCB
Place so that is the module's right camera.









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Drawn by: ***David Malovrh***			

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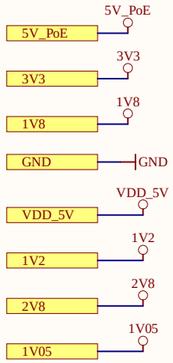
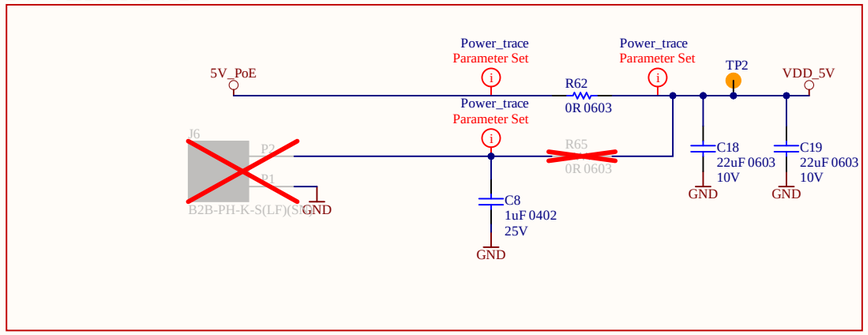
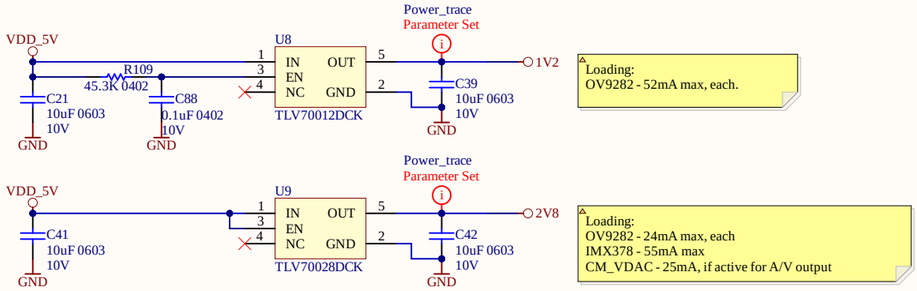
POWER INPUT





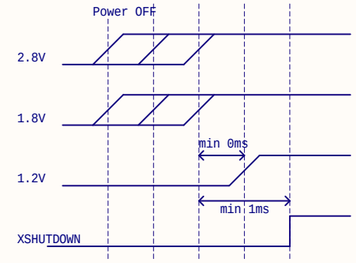


Loading:
OV9282 - 52mA max, each.

Loading:
OV9282 - 24mA max, each
IMX378 - 55mA max
CM_VDAC - 25mA, if active for A/V output

Placed RC timing circuit for EN pins in order to obtain the appropriate power supply sequencing if ncessary

OV9282 POWER REQUIREMENTS

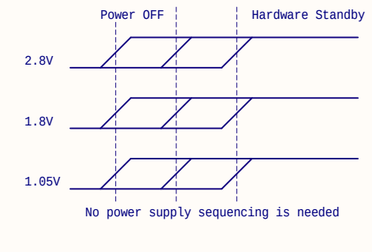


Supply Information

Supply Name		Voltage	Max Current
Module	Sensor		
DOVDD	VDD-IO	1.8V	2.5mA
DVDD	VDD-D	1.2V	52mA
AVDD	VDD-A	2.8V	24mA

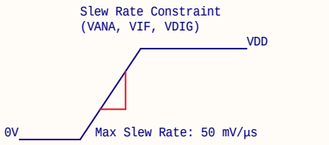
1. AVDD rising can occur before or after DOVDD rising as long as they are rising before XSHUTDOWN rising
2. XSHUTDOWN is pulled up after AVDD and DOVDD are stable
3. DVDD rises after DOVDD, but before XSHUTDOWN is pulled high

IMX378 POWER REQUIREMENTS



Supply Information

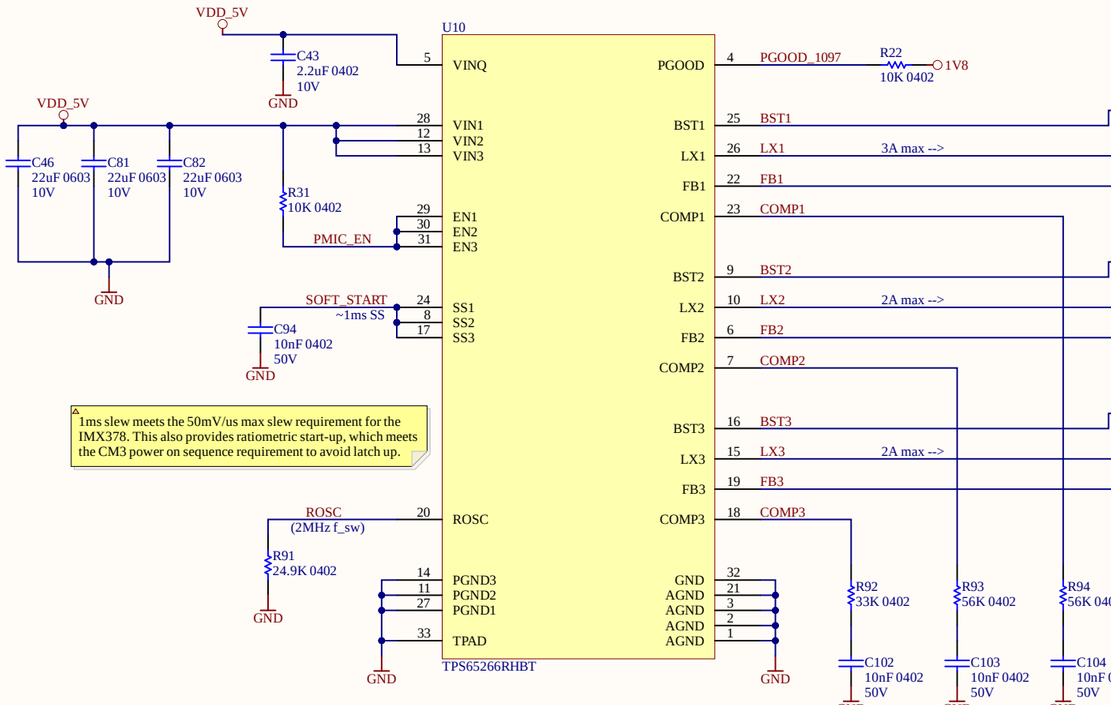
Supply Name		Voltage	Max Current
Module	Sensor		
AVDD	VANA	2.8V ± 0.1	55mA
DOVDD	VIF	1.8V ± 0.1	2.5mA
DVDD	VDIG	1.05V ± 0.1	446mA



POWER SEQUENCING REQUIREMENTS:

The BW2099 module handles it's own power sequencing on-board. (TBC)

The camera modules have their own power sequencing requirements. The OV9282 have requirements for sequencing, and the IMX378 has a max slew rate requirement. See above.



1ms slew meets the 50mV/us max slew requirement for the IMX378. This also provides ratiometric start-up, which meets the CM3 power on sequence requirement to avoid latch up.

SET POINT EQN FOR ALL REG OUTPUTS:

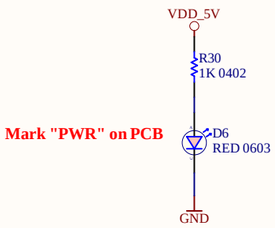
R2 = R1 x (0.6V / (Vout - 0.6V))

Compensation adjusted to set Fc 1/10th Fsw (200kHz) for all three outputs. The compensation circuitry has not been fully tuned.

Effective capacitance targets for each rail, taking into account DC bias and other effects:
3.3V C_eff = 24uF
1.8V C_eff = 26uF
1.05V C_eff = 70uF

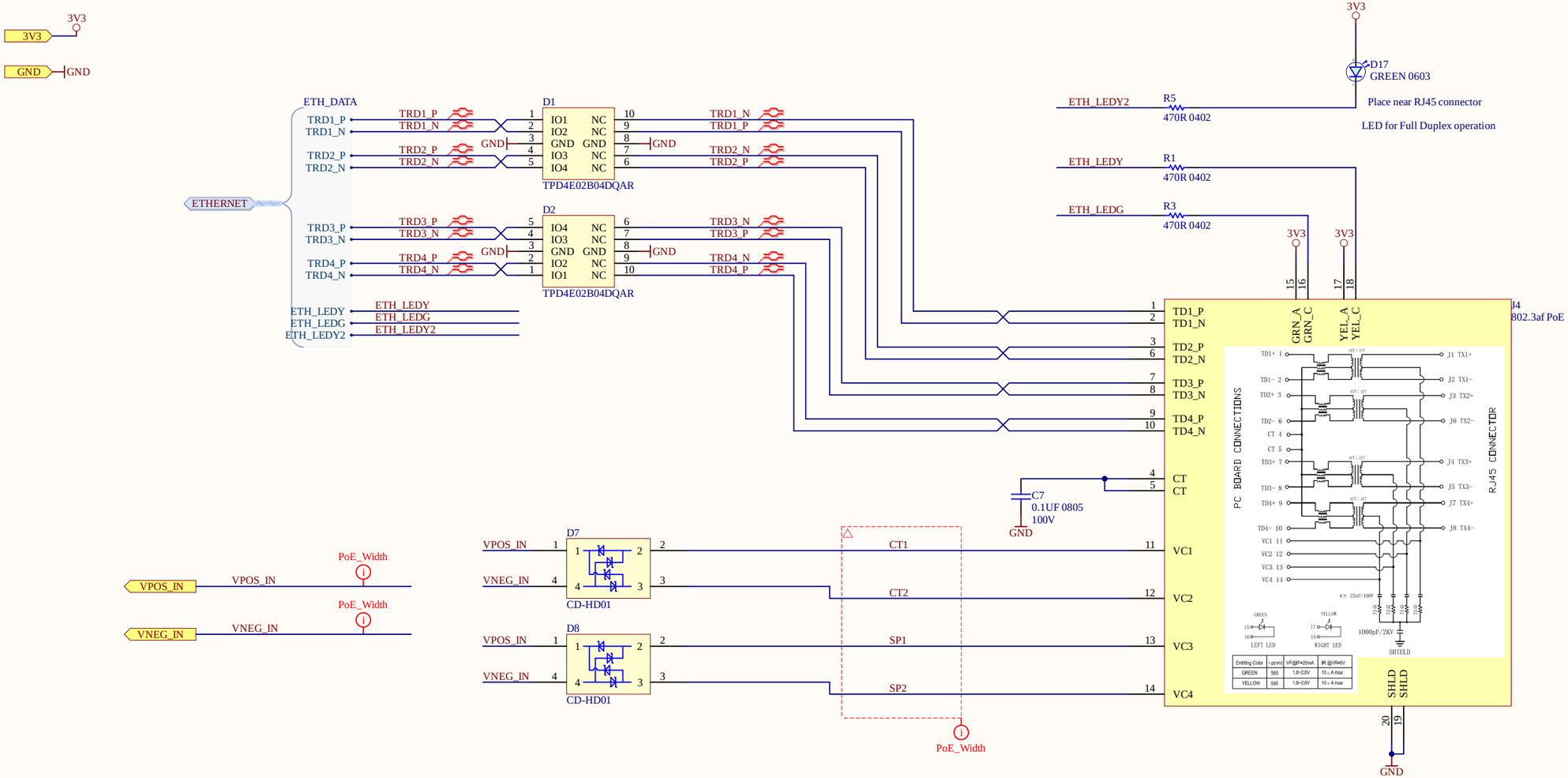
Voltage ripple and allowed voltage tolerance on all rails is +/-5%

Load step design assumptions, based on worst case rail loading:
3.3V - 2.5A step
1.8V - 1A step
1.05 - 0.5A step



Mark "PWR" on PCB

Title: DM2097			Luxonis Holding 1925 Harmony Park Drive Westminster, CO 80234 United States
Size: Tabloid	Number: D0000200	Revision: R0M0E0	Cannot open file C:\Users\BrianLuxonis\
Date: 17/08/2021 Time: 12:37:34	Sheet 7 of 17		
Drawn by: David Malovrh			



Title	**DM2097**		
Size: Tabloid	Number: D0000200	Revision: R0M0E0	
Date: 17/08/2021	Time: 12:37:34	Sheet 8 of 12	
Drawn by: ***David Malovrh***			

Luxonis Holding
1925 Harmony Park Drive
Westminster, CO
80234
United States

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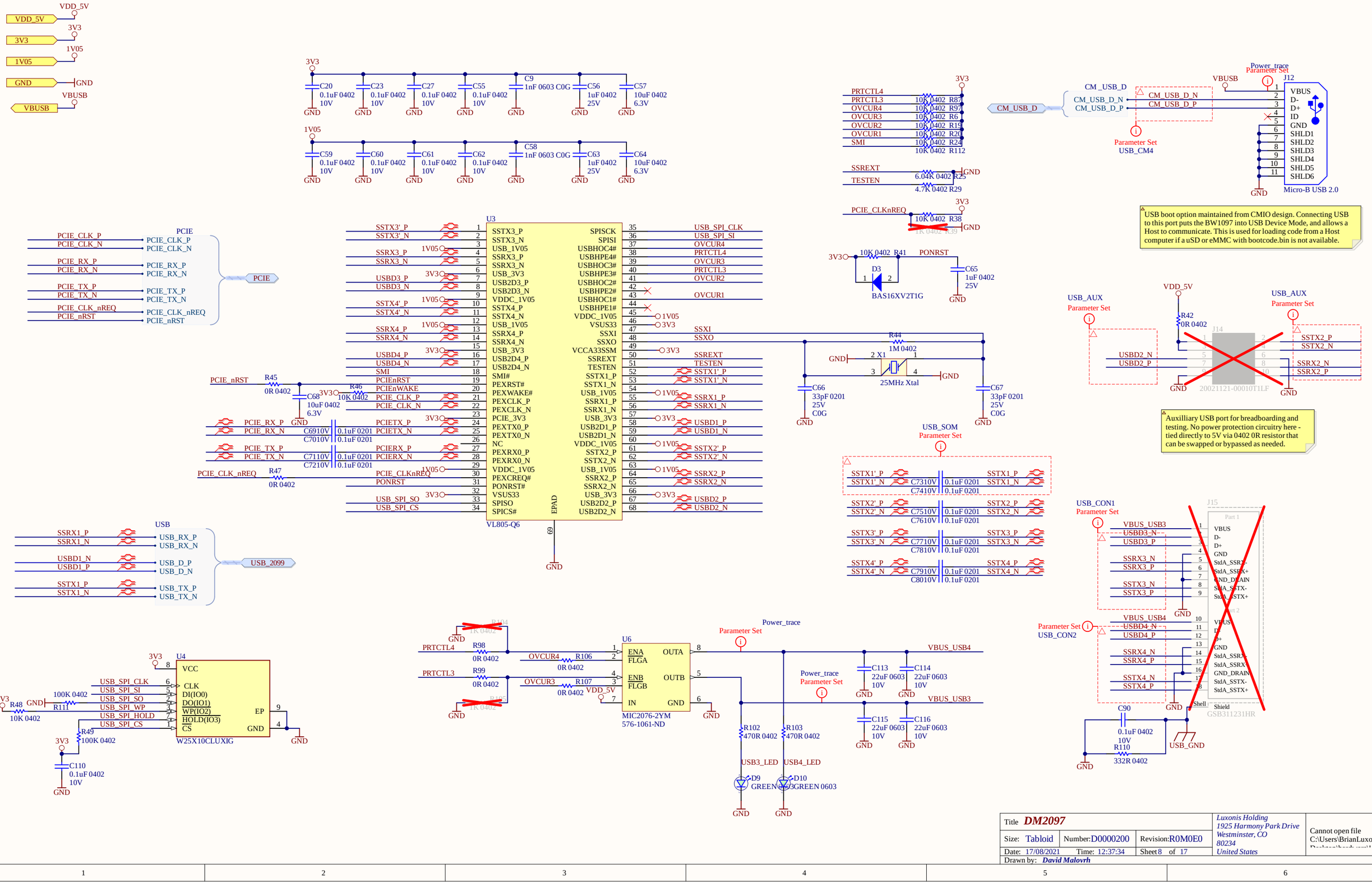
VDD_5V
3V3
1V05
GND
VBUSB
C20 0.1uF 0402 10V
C23 0.1uF 0402 10V
C27 0.1uF 0402 10V
C55 0.1uF 0402 10V
C9 1nF 0603 C0G
C56 1uF 0402 25V
C57 10uF 0402 6.3V
C59 0.1uF 0402 10V
C60 0.1uF 0402 10V
C61 0.1uF 0402 10V
C62 0.1uF 0402 10V
C58 1nF 0603 C0G
C63 1uF 0402 25V
C64 10uF 0402 6.3V
PRTCTL4
PRTCTL3
OVCUR4
OVCUR3
OVCUR2
OVCUR1
SMI
10K 0402 R87
10K 0402 R97
10K 0402 R6
10K 0402 R19
10K 0402 R20
10K 0402 R24
10K 0402 R112
SSREXT
TESTEN
6.04K 0402 R25
4.7K 0402 R29
PCIE_CLKnREQ
10K 0402 R38
1K 0402 R39
CM_USB_D
CM_USB_D_N
CM_USB_D_P
CM_USB_D_N R87
CM_USB_D_P R97
Parameter Set
USB_CM4
Power_trace
Parameter Set
VBUSB
J12
VBUS
D-
D+
ID
GND
SHLD1
SHLD2
SHLD3
SHLD4
SHLD5
SHLD6
Micro-B USB 2.0
USB boot option maintained from CMIO design. Connecting USB to this port puts the BW1097 into USB Device Mode, and allows a Host to communicate. This is used for loading code from a Host computer if a uSD or eMMC with bootcode.bin is not available.
PCIE
PCIE_CLK_P
PCIE_CLK_N
PCIE_RX_P
PCIE_RX_N
PCIE_TX_P
PCIE_TX_N
PCIE_CLK_nREQ
PCIE_nRST
U3
SSTX3'_P
SSTX3'_N
SSRX3_P
SSRX3_N
USBD3_P
USBD3_N
SSTX4'_P
SSTX4'_N
SSRX4_P
SSRX4_N
USBD4_P
USBD4_N
SMI
PCIEnRST
PCIEnWAKE
PCIE_CLK_P
PCIE_CLK_N
PCIETX_P
PCIETX_N
PCIERX_P
PCIERX_N
PCIE_CLKnREQ
PONRST
USB_SPI_SO
USB_SPI_CS
SSTX3_P
SSTX3_N
USB_1V05
SSRX3_P
SSRX3_N
USB_3V3
USB2D3_P
USB2D3_N
VDDC_1V05
SSTX4_P
SSTX4_N
USB_1V05
SSRX4_P
SSRX4_N
USB_3V3
USB2D4_P
USB2D4_N
SMI#
PEXRST#
PEXWAKE#
PEXCLK_P
PEXCLK_N
PCIE_3V3
PEXTX0_P
PEXTX0_N
NC
PEXRX0_P
PEXRX0_N
VDDC_1V05
PEXCREQ#
PONRST#
VSUS33
SPISO
SPICS#
EPAD
SPISCK
SPISI
USBHOC4#
USBHPE4#
USBHOC3#
USBHPE3#
USBHOC2#
USBHPE2#
USBHOC1#
USBHPE1#
VDDC_1V05
VSUS33
SSXI
SSXO
VCCA33SSM
SSREXT
TESTEN
SSTX1'_P
SSTX1'_N
SSTX1_P
SSTX1_N
USB_1V05
SSRX1_P
SSRX1_N
USB_3V3
USB2D1_P
USB2D1_N
VDDC_1V05
SSTX2_P
SSTX2_N
USB_1V05
SSRX2_P
SSRX2_N
USB_3V3
USB2D2_P
USB2D2_N
USB_SPI_CLK
USB_SPI_SI
USB_SPI_SO
USB_SPI_WP
USB_SPI_HOLD
USB_SPI_CS
OVCUR1
SSXI
SSXO
SSREXT
TESTEN
SSTX1'_P
SSTX1'_N
SSRX1_P
SSRX1_N
USBD1_P
USBD1_N
SSTX2'_P
SSTX2'_N
SSRX2_P
SSRX2_N
USBD2_P
USBD2_N
VL805-Q6
R44 1M 0402
2 X1
25MHz Xtal
C66 33pF 0201 25V C0G
C67 33pF 0201 25V C0G
USB_SOM
Parameter Set
SSTX1'_P
SSTX1'_N
SSTX1_P
SSTX1_N
C7310V 0.1uF 0201
C7410V 0.1uF 0201
SSTX2'_P
SSTX2'_N
SSTX2_P
SSTX2_N
C7510V 0.1uF 0201
C7610V 0.1uF 0201
SSTX3'_P
SSTX3'_N
SSTX3_P
SSTX3_N
C7710V 0.1uF 0201
C7810V 0.1uF 0201
SSTX4'_P
SSTX4'_N
SSTX4_P
SSTX4_N
C7910V 0.1uF 0201
C8010V 0.1uF 0201
USB_AUX
Parameter Set
VDD_5V
R42 0R 0402
J14
SSTX2_P
SSTX2_N
SSRX2_N
SSRX2_P
USBD2_N
USBD2_P
20021121-00010T1LF
Auxilliary USB port for breadboarding and testing. No power protection circuitry here - tied directly to 5V via 0402 0R resistor that can be swapped or bypassed as needed.
USB
SSRX1_P
SSRX1_N
USBD1_N
USBD1_P
SSTX1_P
SSTX1_N
USB_RX_P
USB_RX_N
USB_D_P
USB_D_N
USB_TX_P
USB_TX_N
USB_2099
U4
VCC
CLK
DI(IO0)
DO(IO1)
WP(IO2)
HOLD(IO3)
CS
EP
GND
W25X10CLUXIG
R48 10K 0402
R111 100K 0402
R49 100K 0402
C110 0.1uF 0402 10V
R45 0R 0402
R46 10K 0402
C68 10uF 0402 6.3V
C6910V 0.1uF 0201
C7010V 0.1uF 0201
C7110V 0.1uF 0201
C7210V 0.1uF 0201
R47 0R 0402
R104 1K 0402
R105 1K 0402
R98 0R 0402
R99 0R 0402
R106 0R 0402
R107 0R 0402
U6
ENA
FLGA
ENB
FLGB
IN
OUTA
OUTB
GND
MIC2076-2YM
576-1061-ND
Power_trace
Parameter Set
R102 470R 0402
R103 470R 0402
USB3_LED
USB4_LED
D9 GREEN 0603
D10 GREEN 0603
VBUS_USB4
VBUS_USB3
C113 22uF 0603 10V
C114 22uF 0603 10V
C115 22uF 0603 10V
C116 22uF 0603 10V
USB_CON1
Parameter Set
USB_CON2
Parameter Set
J15
Part 1
Part 2
VBUS_USB3
USBD3_N
USBD3_P
SSRX3_N
SSRX3_P
SSTX3_N
SSTX3_P
VBUS_USB4
USBD4_N
USBD4_P
SSRX4_N
SSRX4_P
SSTX4_N
SSTX4_P
VBUS
D-
D+
GND
StdA_SSRX-
StdA_SSRX+
GND_DRAIN
StdA_SSTX-
StdA_SSTX+
Shell
GSB311231HR
C90 0.1uF 0402 10V
R110 332R 0402
USB_GND
Title DM2097
Size: Tabloid
Number: D0000200
Revision: R0M0E0
Date: 17/08/2021
Time: 12:37:34
Sheet 8 of 17
Drawn by: David Malovrh
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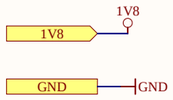

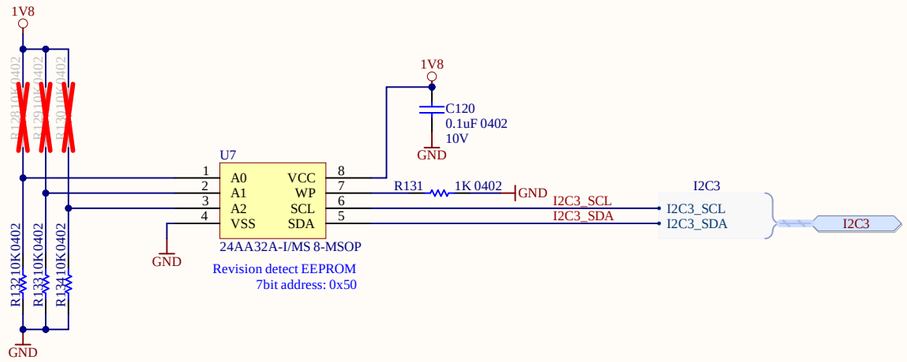

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Size: Tabloid	Number: D0000200	Revision: R0M0E0	Cannot open file C:\Users\BrianLuxonis\
Date: 17/08/2021 Time: 12:37:34		Sheet 8 of 12	
Drawn by: ***David Malovrh***			

USB_D diff pair: 90ohms +/-10%

All other diff pairs: 100ohms +/-10

R64
1K 0402

J13

CONNECTOR A

Raspberry Pi Compute Module 4

		USB_OTGID	1	USB_OTG_ID	
		CM_USB_D_N	3	USB_N	
		CM_USB_D_P	5	USB_P	
			7	GND	
		PCIE_nRST	9	PCIe_nRST	
		TVDAC	11	VDAC_COMP	
			13	GND	
		CAM1_D0_N	15	CAM1_D0_N	
		CAM1_D0_P	17	CAM1_D0_P	
			19	GND	
		CAM1_D1_N	21	CAM1_D1_N	
		CAM1_D1_P	23	CAM1_D1_P	
			25	GND	
		CAM1_CLK_N	27	CAM1_C_N	
		CAM1_CLK_P	29	CAM1_C_P	
			31	GND	
			33	CAM1_D2_N	
			35	CAM1_D2_P	
			37	GND	
			39	CAM1_D3_N	
			41	CAM1_D3_P	
			43	HDMI1_HOTPLUG	
			45	HDMI1_SDA	
			47	HDMI1_SCL	
			49	HDMI1_CEC	
		HDMI_CEC	51	HDMI0_CEC	
		HDMI_HPD_N_1V8	53	HDMI0_HOTPLUG	
			55	GND	
			57	DSI0_D0_N	
			59	DSI0_D0_P	
			61	GND	
			63	DSI0_D1_N	
			65	DSI0_D1_P	
			67	GND	
			69	DSI0_C_N	
			71	DSI0_C_P	
			73	GND	
		DSI1_D0_N	75	DSI1_D0_N	
		DSI1_D0_P	77	DSI1_D0_P	
			79	GND	
		DSI1_D1_N	81	DSI1_D1_N	
		DSI1_D1_P	83	DSI1_D1_P	
			85	GND	
		DSI1_CLK_N	87	DSI1_C_N	
		DSI1_CLK_P	89	DSI1_C_P	
			91	GND	
			93	DSI1_D2_N	
			95	DSI1_D2_P	
			97	GND	
		HDMI_SDA	99	HDMI0_SDA	

		PCIe_CLK_nREQ	2	PCIE_CLK_nREQ	
		Reserved	4		
		Reserved	6		
		GND	8		
		PCIe_CLK_P	10	PCIE_CLK_P	
		PCIe_CLK_N	12	PCIE_CLK_N	
		GND	14		
		PCIe_RX_P	16	PCIE_RX_P	
		PCIe_RX_N	18	PCIE_RX_N	
		GND	20		
		PCIe_TX_P	22	PCIE_TX_P	
		PCIe_TX_N	24	PCIE_TX_N	
		GND	26		
		CAM0_D0_N	28		
		CAM0_D0_P	30		
		GND	32		
		CAM0_D1_N	34		
		CAM0_D1_P	36		
		GND	38		
		CAM0_C_N	40		
		CAM0_C_P	42		
		GND	44		
		HDMI1_TX2_P	46		
		HDMI1_TX2_N	48		
		GND	50		
		HDMI1_TX1_P	52		
		HDMI1_TX1_N	54		
		GND	56		
		HDMI1_TX0_P	58		
		HDMI1_TX0_N	60		
		GND	62		
		HDMI1_CLK_P	64		
		HDMI1_CLK_N	66		
		GND	68		
		HDMI0_TX2_P	70	HDMI_D2_P	
		HDMI0_TX2_N	72	HDMI_D2_N	
		GND	74		
		HDMI0_TX1_P	76	HDMI_D1_P	
		HDMI0_TX1_N	78	HDMI_D1_N	
		GND	80		
		HDMI0_TX0_P	82	HDMI_D0_P	
		HDMI0_TX0_N	84	HDMI_D0_N	
		GND	86		
		HDMI0_CLK_P	88	HDMI_CLK_P	
		HDMI0_CLK_N	90	HDMI_CLK_N	
		GND	92		
		DSI1_D3_N	94		
		DSI1_D3_P	96		
		GND	98		
		HDMI0_SCL	100	HDMI_SCL	

Parameter Set
PCIe

GND

GND

PCIE

PCIE_CLK_P	PCIE_CLK_P
PCIE_CLK_N	PCIE_CLK_N
PCIE_RX_P	PCIE_RX_P
PCIE_RX_N	PCIE_RX_N
PCIE_TX_P	PCIE_TX_P
PCIE_TX_N	PCIE_TX_N
PCIE_CLK_nREQ	PCIE_CLK_nREQ
PCIE_nRST	PCIE_nRST

HDMI

HDMI_D2_P	HDMI_D2_P
HDMI_D2_N	HDMI_D2_N
HDMI_D1_P	HDMI_D1_P
HDMI_D1_N	HDMI_D1_N
HDMI_D0_P	HDMI_D0_P
HDMI_D0_N	HDMI_D0_N
HDMI_CLK_P	HDMI_CLK_P
HDMI_CLK_N	HDMI_CLK_N

HDMI_CTL

HDMI_CEC	HDMI_CEC
HDMI_SCL	HDMI_SCL
HDMI_SDA	HDMI_SDA
HDMI_HPD_N_1V8	HDMI_HPD_N_1V8

CM_USB_D

CM_USB_D_P	CM_USB_D_P
CM_USB_D_N	CM_USB_D_N

Title	DM2097		
Size: Tabloid	Number: D0000200	Revision: R0M0E0	
Date: 17/08/2021	Time: 12:37:34	Sheet 9 of 17	
Drawn by: David Malovrh			

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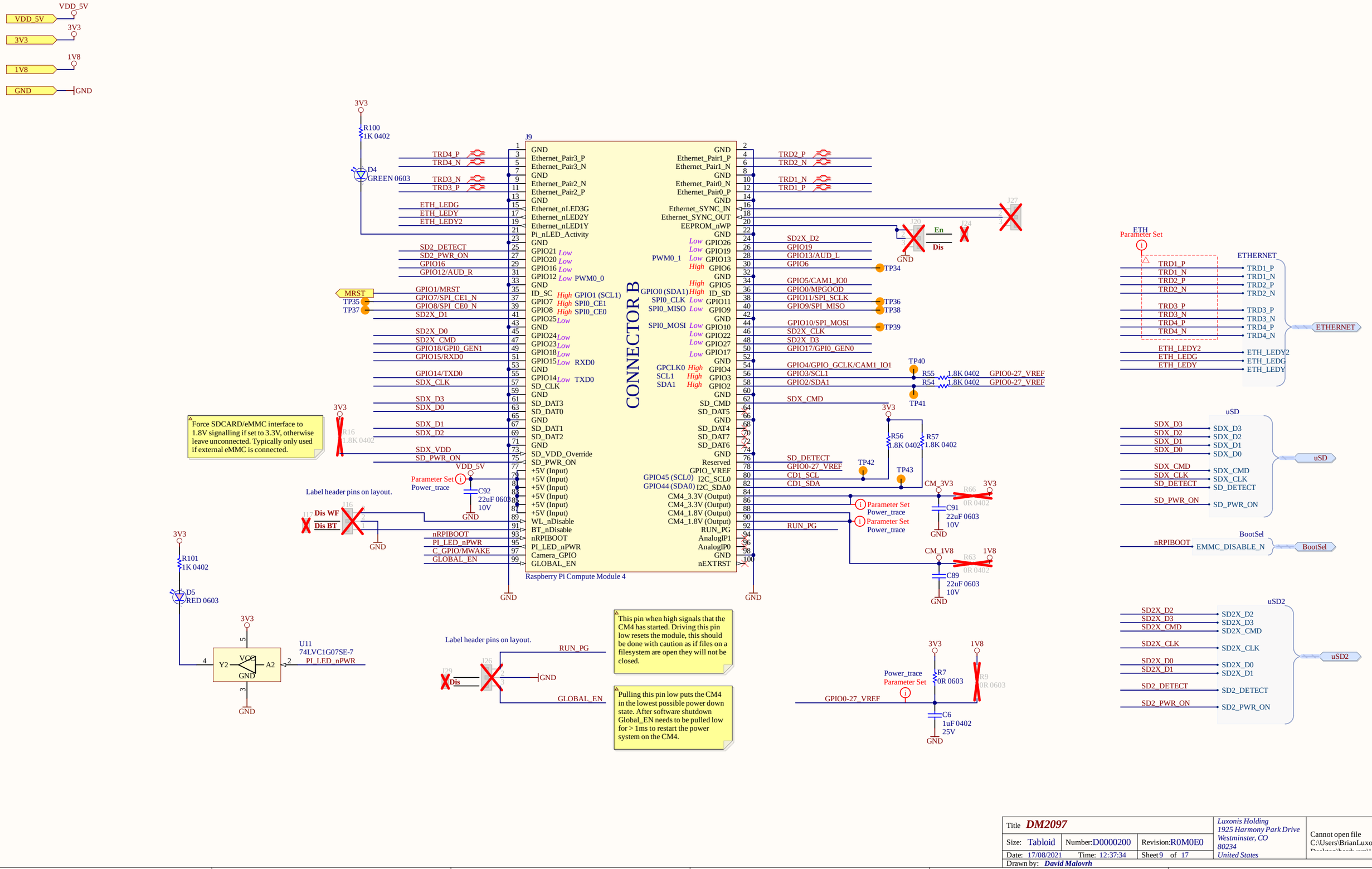

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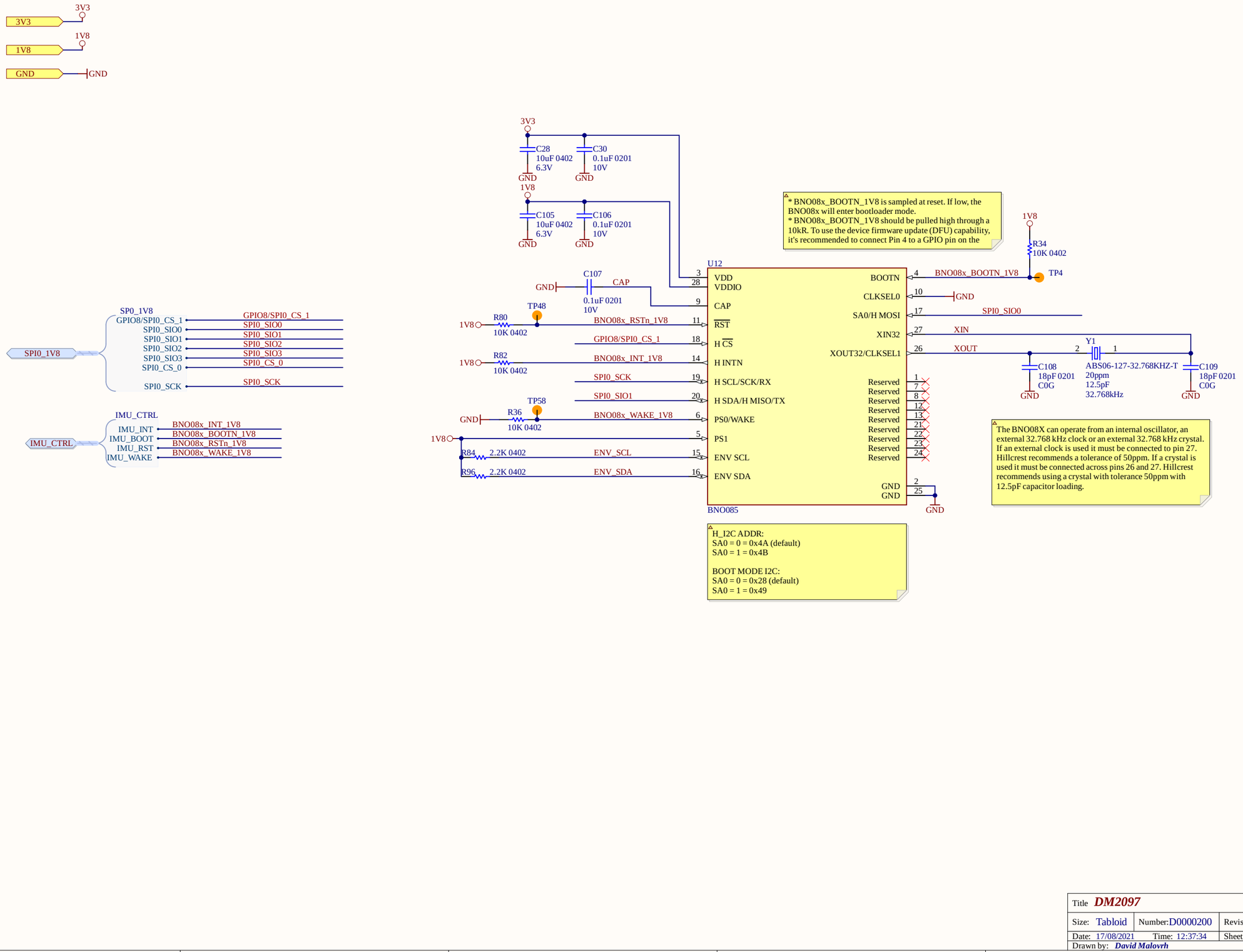
Date: 17/08/2021 Time: 12:37:34	Sheet 9 of 17		
Drawn by: ***David Malovrh***			



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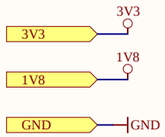
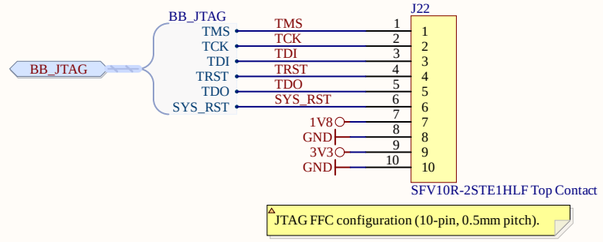
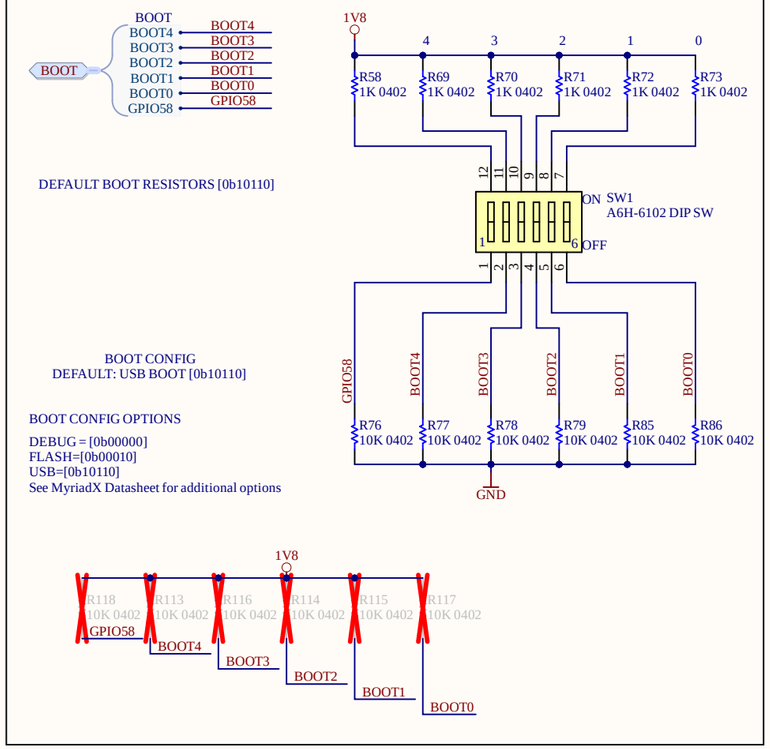


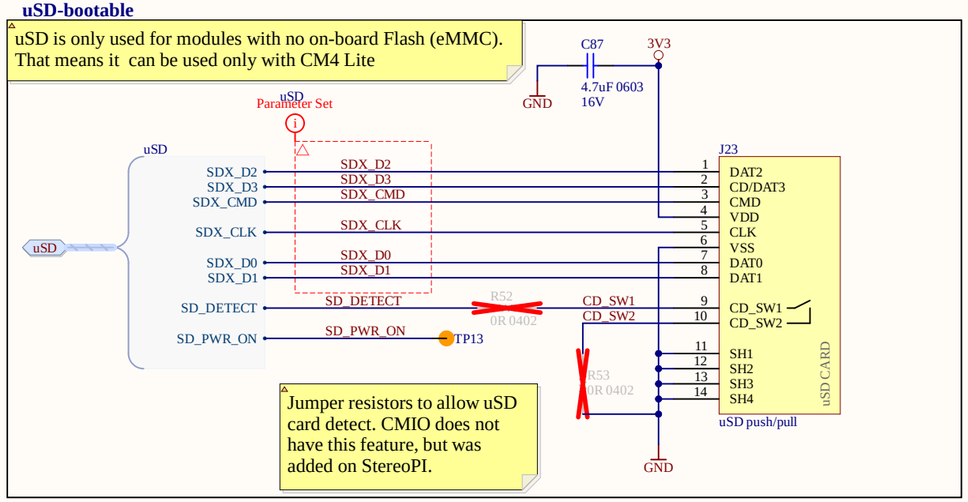
JTAG CONNECTOR



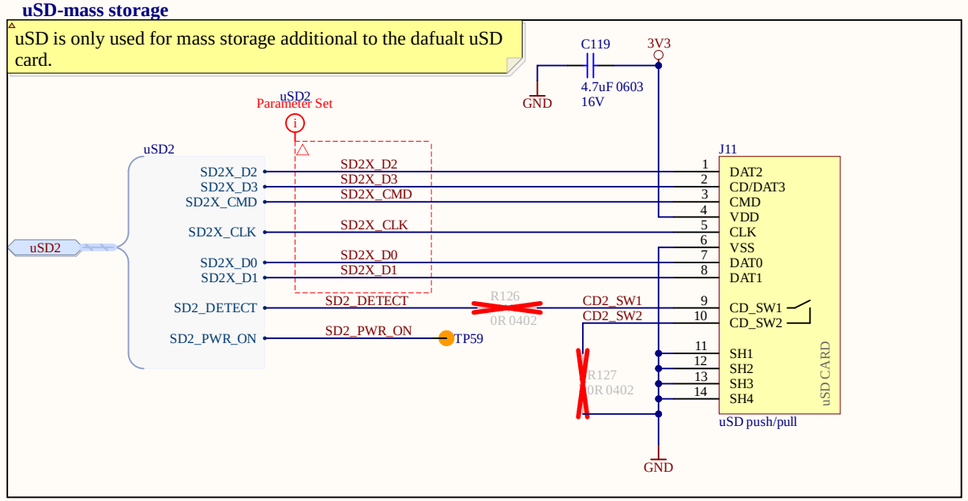
BOOT MODES



uSD-bootable



uSD-mass storage



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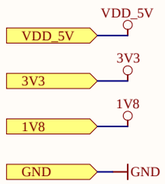
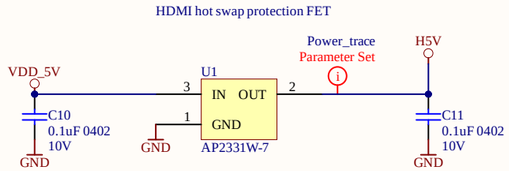
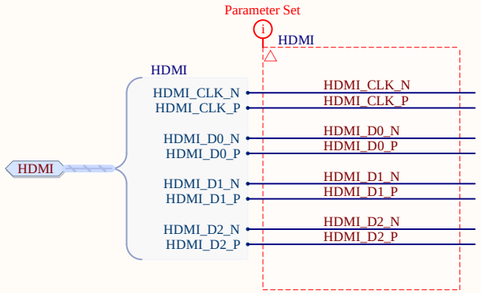
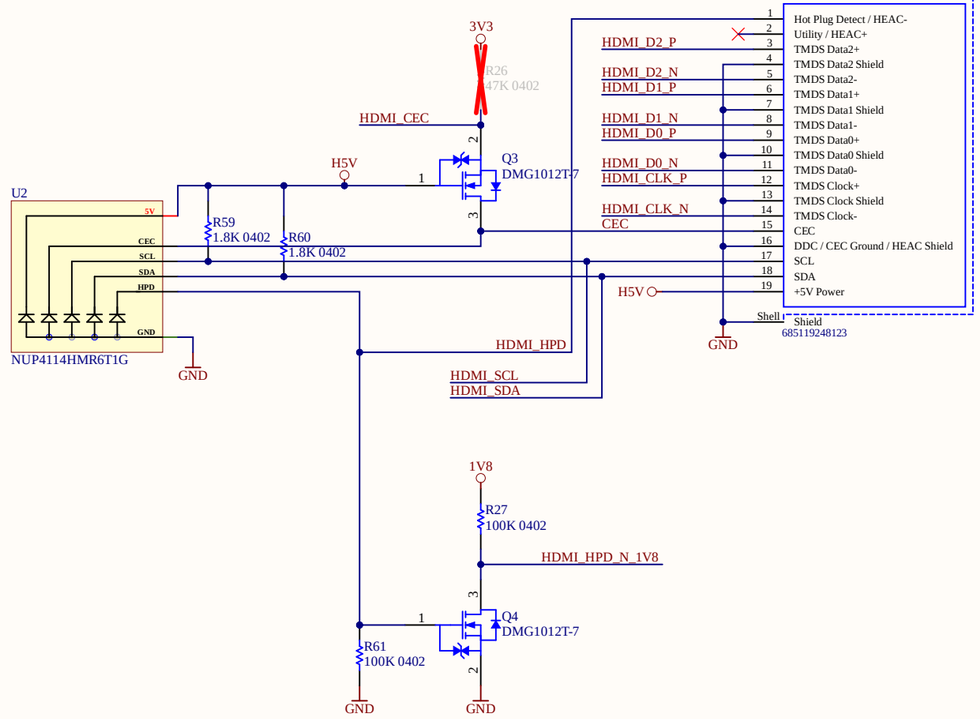


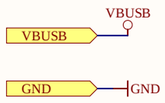


Basic onboard ESD protection is provided for the I2C EDID signals and the CEC signals, internal pullup and down resistors
are also provided.
On the {rpi4} the HDMI signals don't have any extra ESD protection , depending on the application extra
ESD protection maybe required.



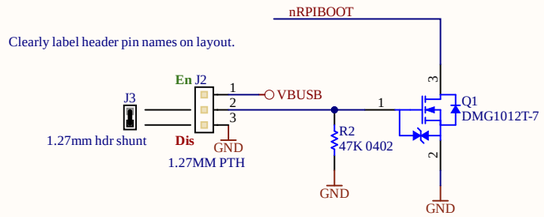


Title **DM2097**			*Luxonis Holding* *1925 Harmony Park Drive* *Westminster, CO* *80234* *United States*
Size: Tabloid	Number: D0000200	Revision: R0M0E0	Cannot open file C:\Users\BrianLuxonis\
Date: 17/08/2021	Time: 12:37:34	Sheet 12 of 17	
Drawn by: ***David Malovrh***			



MODULE BOOT OPTIONS:

Short the nRPIBOOT pin to ground to force USB boot mode. The CM4IO board has a jumper for nRPIBOOT This can be
used to enable different boot modes (e.g. network) and enable UART logging.



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Date: 17/08/2021 Time: 12:37:34		Sheet 14 of 17	
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