PixArt Imaging Inc.

PAA3905E1-Q: Optical Motion Tracking Chip

General Description

The PAA3905E1 is PixArt Imaging's optical motion tracking chip specifically designed for low light condition operation. The state of the art of architecture allows motion tracking under low light conditions as low as 5 lux. The chip supports a wide working distance of 80 mm to infinity under challenging conditions to cater for different far-field application needs and ambient conditions. It is suitable for far-field tracking applications in providing motion tracking with a stable hovering function for Drone.

Key Features

- Wide working distance from 80mm to infinity
- No focal length calibration required
- Auto-detection of challenging conditions, e.g. checkerboards, stripes, glossy surface, and yawing
- 16-bit motion data output with motion detect pin output
- Internal oscillator
- Raw Data Output through register read
- Support synchronized multi-chip operation
- Automatic switching of Operation Mode

Operation Modes

| Mode	Description	Lux (Typ)
0 @ 126 fps	Bright Mode for general motion tracking	60
1 @ 126 fps (Default)	Low Light Mode for low light motion tracking	30
2 @ 50 fps	Super Low Light Mode for super low light and low-speed motion tracking	5

Applications

- Drone or other devices that require far-field motion detection and hovering stability
- X-Y positioning in GPS denied environment

Key Parameters

Parameter	Value
Supply Voltage	VDD: 1.8 to 2.0 V VDDIO: 1.8 to 3.6 V
Working Range	80 mm to infinity
Interface	4-Wire SPI @ 2MHz
Speed	maximum 7.4 rad/s (Mode 0 &1)
Effective Viewing angle	42°
Power Consumption	3.5 mA at RUN state
Package size (L x W x H)	12-pin LGA Package with L242-ZSZ1 Lens 4.0 x 5.0 x 3.0 mm^3

Ordering Information

Part Number	Description	Package Type	Packing Type	MOQ
PAA3905E1-Q	OMT Chip	12 pins LGA	Tube	2000
L242-ZSZ1	Lens	Plastic lens	Tray	2000

RoHS compliant
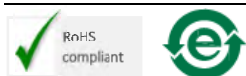
For any additional inquiries, please contact us at http://www.pixart.com

Table of Content

List of Figures

5

List of Tables

1.0 Introduction

1.1 Overview

PAA3905E1-Q contains a Picture Element Acquisition System (PEAS), a hard-coded Digital Signal Processing System (DSPS), and a four-wire serial port interface. It is based on Optical Navigation Technology to measure changes in a position where acquiring sequential picture elements for calculating the direction and magnitude of movement (delta X and delta Y).

Note: Throughout this document, the PAA3905E1-Q is referred to as the "chip".

1.2 Block Diagram
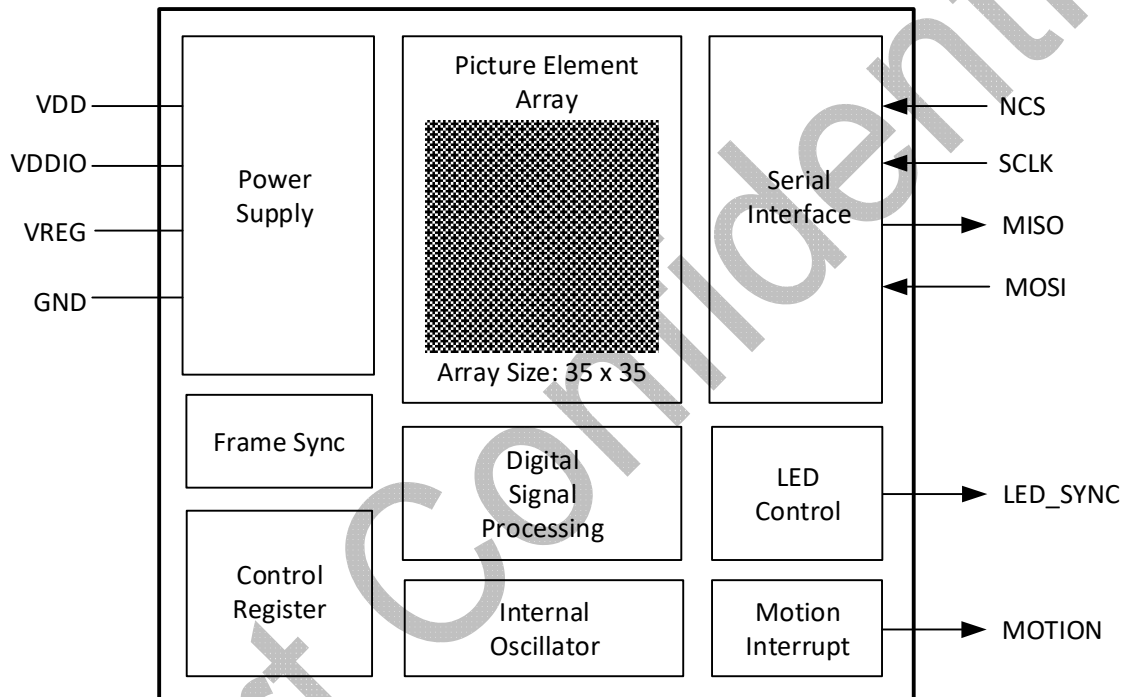
Figure 1. Block Diagram

1.3 Terminology

Term	Description
DSPS	Digital Signal Processing System
ESD	Electrostatic Discharge
LED	Light Emitting Diode
IC	Integrated Circuit
I/O	Input / Output
IR	Infrared
PCB	Printed Circuit Board
IMU	Inertial Measurement Unit
AMS	Auto Mode Switching

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1.4 Pin Assignment and Signal Description
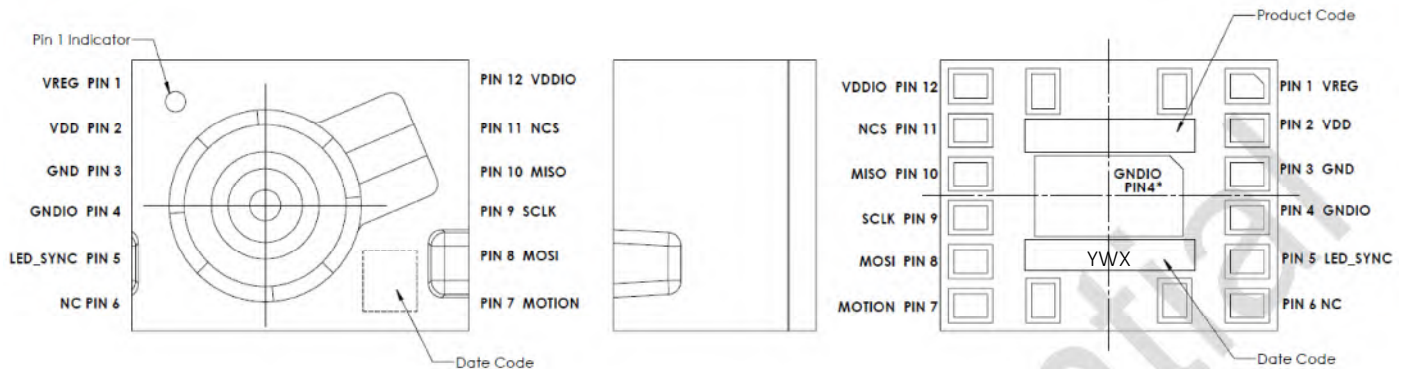
Figure 2. Pin Configuration

Table 1. Signal Pins Description

Function	Pin No.	Signal Name	Type	Description
Power Supplies	2	VDD	Power	Input power supply
	12	VDDIO	Power	I/O reference voltage
	1	VREG	Ground	Internal voltage output
	3	GND	Ground	Ground
	4	GNDIO	Ground	I/O ground
	4*	GNDIO	Ground	I/O ground pad
Control Interface	8	MOSI	Input	Serial data input
	9	SCLK	Input	Serial data clock
	10	MISO	Output	Serial data output
	11	NCS	Input	Chip select
Functional I/O	7	MOTION	Output	Motion interrupt (Active low)
	5	LED_SYNC	Output	External LED control pin (Active low).
Reserved	6	NC	NC	No Connect

2.0 Operating Specification

2.1 Absolute Maximum Rating

Table 2. Absolute Maximum Rating

Parameter	Symbol	Min.	Max.	Unit	Note
Storage Temperature	T_S	-40	85	°C	
Lead-Free Solder Temperature	T_{SOLDER}		260	°C	
Supply Voltage	VDD	-0.5	2.0	V	
	VDDIO	-0.5	3.6	V	
Input Voltage	V_{IN}	-0.5	3.6	V	All I/O pins
ESD	ESD_{HBM}		2	kV	All pins (Human Body Model)

Notes:
1. The above maximum ratings are the guaranteed parameters that the chip expects to be functional as per the intended design.
2. Exposure to these conditions or beyond those indicated may adversely affect device reliability and unexpected or premature functional failure.

2.2 Recommended Operating Condition

Table 3. Recommended Operating Condition

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Ambient Temperature	T_A	0		60	°C	
Power Supply Voltage	VDD	1.8	1.9	2.0	V	Including supply noise
	VDDIO	1.8	1.9	3.6	V	VDDIO ≥ VDD
Power Supply Rise Time	t_R	0.15		20	ms	0 to VDD min
Supply Noise	V_{NA}			100	mV	10 kHz to 75 MHz, peak to peak
Serial Port Clock Frequency	f_{SCLK}			2	MHz	50% duty cycle
Working Distance	Z	80			mm	
Effective Viewing Angle	V_A		42		°	
Minimum Illuminance[2] (@ Crimson Carpet, Grey Vinyl & Light Grey Cement surfaces)	L_{XM0}		60		lux	Mode 0: Bright Mode
	L_{XM1}		30		lux	Mode 1: Low Light Mode (Default Mode)
	L_{XM2}		5		lux	Mode 2: Super Low Light Mode
Frame Rate	F_{RM0}		126		fps	Mode 0: Bright Mode
	F_{RM1}		126		fps	Mode 1: Low Light Mode (Default Mode)
	F_{RM2}		50		fps	Mode 2: Super Low Light Mode
Speed	S			7.4	rad/s	Mode 0 & 1

Notes:
1. PixArt does not guarantee the performance of the system beyond the recommended operating condition limits.
2. In addition to visible light spectrum (lux), the chip is also sensitive to IR spectrum up to 940 nm of wavelength which aid in tracking under low light ambient condition.

2.3 DC Characteristic

Table 4. DC Electrical Specification

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Current	I_{DD_RUN}		3.5		mA	Average current. No load on MISO, MOTION.
Power Down Current	I_{PD}		12		µA	
Input Low Voltage	V_{IL}			0.3 x VDDIO	V	SCLK, MOSI, NCS
Input High Voltage	V_{IH}	0.7 x VDDIO			V	SCLK, MOSI, NCS
Input Hysteresis	V_{I_HYS}		100		mV	SCLK, MOSI, NCS
Input Leakage Current	I_{LEAK}		± 1	± 10	µA	$V_{IN} = V_{DDIO}$ or 0V, SCLK, MOSI, NCS
Output Low Voltage	V_{OL}			0.45	V	I_{OUT} = 1mA, MISO, MOTION
Output High Voltage	V_{OH}	VDDIO - 0.45			V	I_{OUT} = -1mA, MISO, MOTION
Transient Supply Current	I_{DDT}			70	mA	Max supply current during the supply ramp from 0V to VDD with min. 150 µs and max. 20 ms rise time (does not include charging currents for bypass capacitors).
	I_{DDTIO}			70	mA	Max supply current during the supply ramp from 0V to VDDIO with min. 150 µs and max. 20 ms rise time (does not include charging currents for bypass capacitors).

Note: All the parameters are tested under operating conditions: VDD = 1.9V, VDDIO = 1.9V, T_A = 25°C.

2.4 AC Characteristic

Table 5. AC Electrical Specification

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Motion Delay After Reset	$t_{MOT-RST}$	50			ms	From reset to valid motion, assuming motion is present
Shutdown	t_{STDWN}			100	ms	From Shutdown state active to low current
Wake from Shutdown	t_{WAKEUP}	300			ms	From Shutdown state inactive to valid motion.

Note: All the parameters are tested under operating conditions: VDD = 1.9V, VDDIO = 1.9V, T_A = 25°C.

2.5 SPI Specification

Table 6. SPI Timing Specification

Parameters	Symbol	Min.	Typ.	Max.	Unit	Note
MISO Rise Time	$t_{r\text{-}MISO}$		50		ns	C_L = 100pF
MISO Fall Time	$t_{f\text{-}MISO}$		50		ns	C_L = 100pF
MISO Delay After SCLK	$t_{DLY\text{-}MISO}$			120	ns	From SCLK falling edge to MISO data valid, no load conditions
MISO Hold Time	$t_{hold\text{-}MISO}$	200			ns	Data held until the next falling SCLK edge
MOSI Hold Time	$t_{hold\text{-}MOSI}$	200			ns	The amount of time data is valid after SCLK rising edge
MOSI Setup Time	$t_{setup\text{-}MOSI}$	120			ns	From data valid to SCLK rising edge
SPI Time Between Write Commands	t_{SWW}	10.5			µs	From rising SCLK for the last bit of the first data byte to rising SCLK for the last bit of the second data byte.
SPI Time Between Write And Read Commands	t_{SWR}	6			µs	From rising SCLK for the last bit of the first data byte to rising SCLK for the last bit of the second address byte.
SPI Time Between Read And Subsequent Commands	t_{SRW} t_{SRR}	1.5			µs	From rising SCLK for the last bit of the first data byte to falling SCLK for the first bit of the address byte of the next command.
SPI Read Address-Data Delay	t_{SRAD}	2			µs	From rising SCLK for the last bit of the address byte to falling SCLK for the first bit of data being read.
NCS Inactive After Motion Burst	t_{BEXIT}	500			ns	Minimum NCS inactive time after motion burst before next SPI usage
NCS To SCLK Active	$t_{NCS\text{-}SCLK}$	120			ns	From last NCS falling edge to the first SCLK rising edge
SCLK To NCS Inactive (For Read Operation)	$t_{SCLK\text{-}NCS}$	120			ns	From the last SCLK rising edge to NCS rising edge, for valid MISO data transfer
SCLK To NCS Inactive (For Write Operation)	$t_{SCLK\text{-}NCS}$	2			µs	From the last SCLK rising edge to NCS rising edge, for valid MOSI data transfer
NCS To MISO High-Z	$t_{NCS\text{-}MISO}$			500	ns	From NCS rising edge to MISO high-Z state
MOTION Rise Time	$t_{r\text{-}MOTION}$		50		ns	C_L = 100pF
MOTION Fall Time	$t_{f\text{-}MOTION}$		50		ns	C_L = 100pF
Input Capacitance	C_{in}		50		pF	SCLK, MOSI, NCS
Load Capacitance	C_L			100	pF	MISO, MOTION

Note: All the parameters are tested under operating conditions: VDD = 1.9V, VDDIO = 1.9V, T_A = 25°C.

2.6 Resolution versus Height Chart

This chart serves as a reference for resolution count with its corresponding height based on the default setting. The resolution can be changed via register *RESOLUTION* (Section 8.2.2), with a maximum of 6x of the chart below.
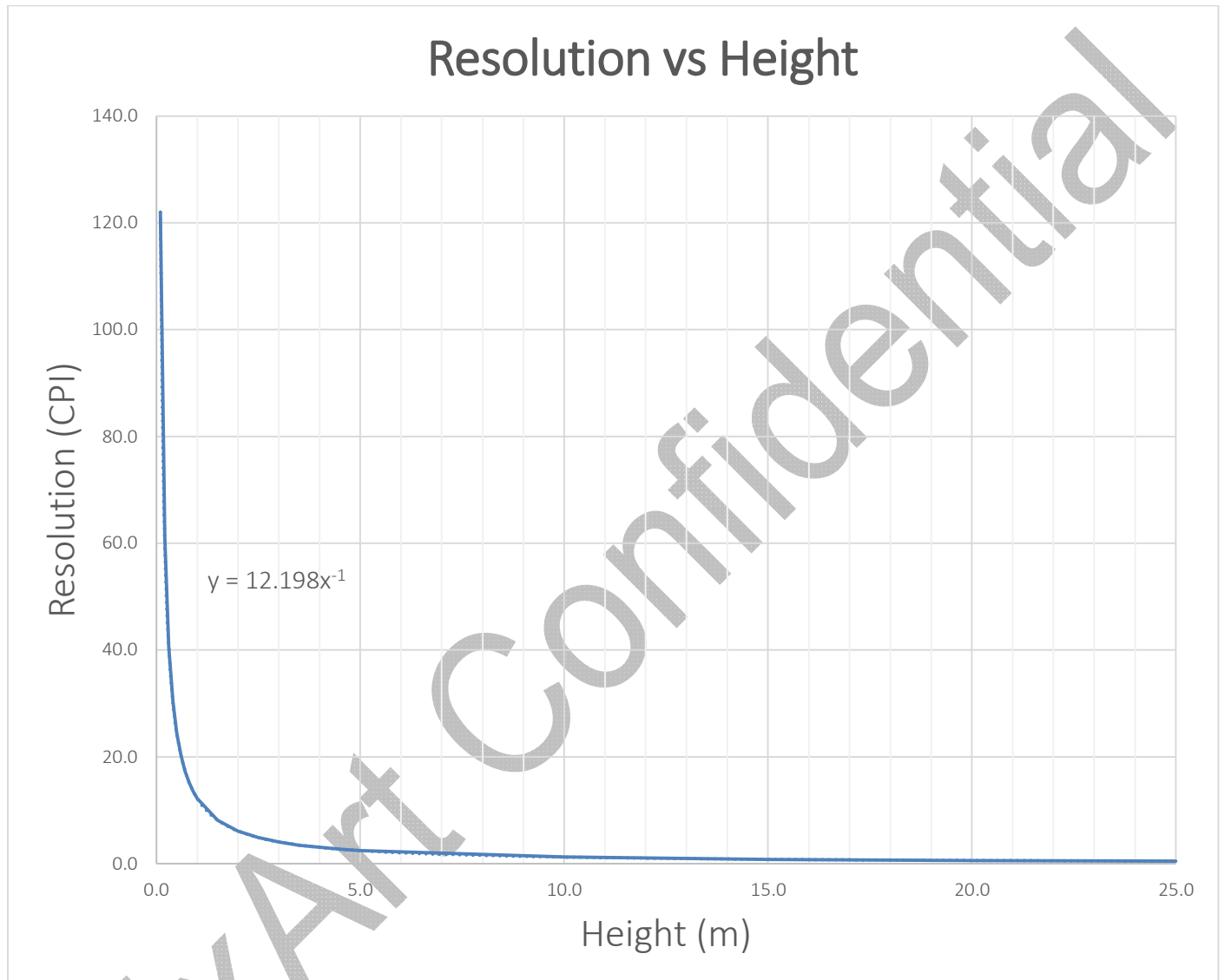
Note: Interpolation is applied to resolution count beyond 2 m.

Figure 3. Resolution versus Height Chart

2.7 Speed versus Height Chart

These charts serve as a theoretical reference of speed capability with its corresponding height for Mode 0 & 1 and Mode 2.
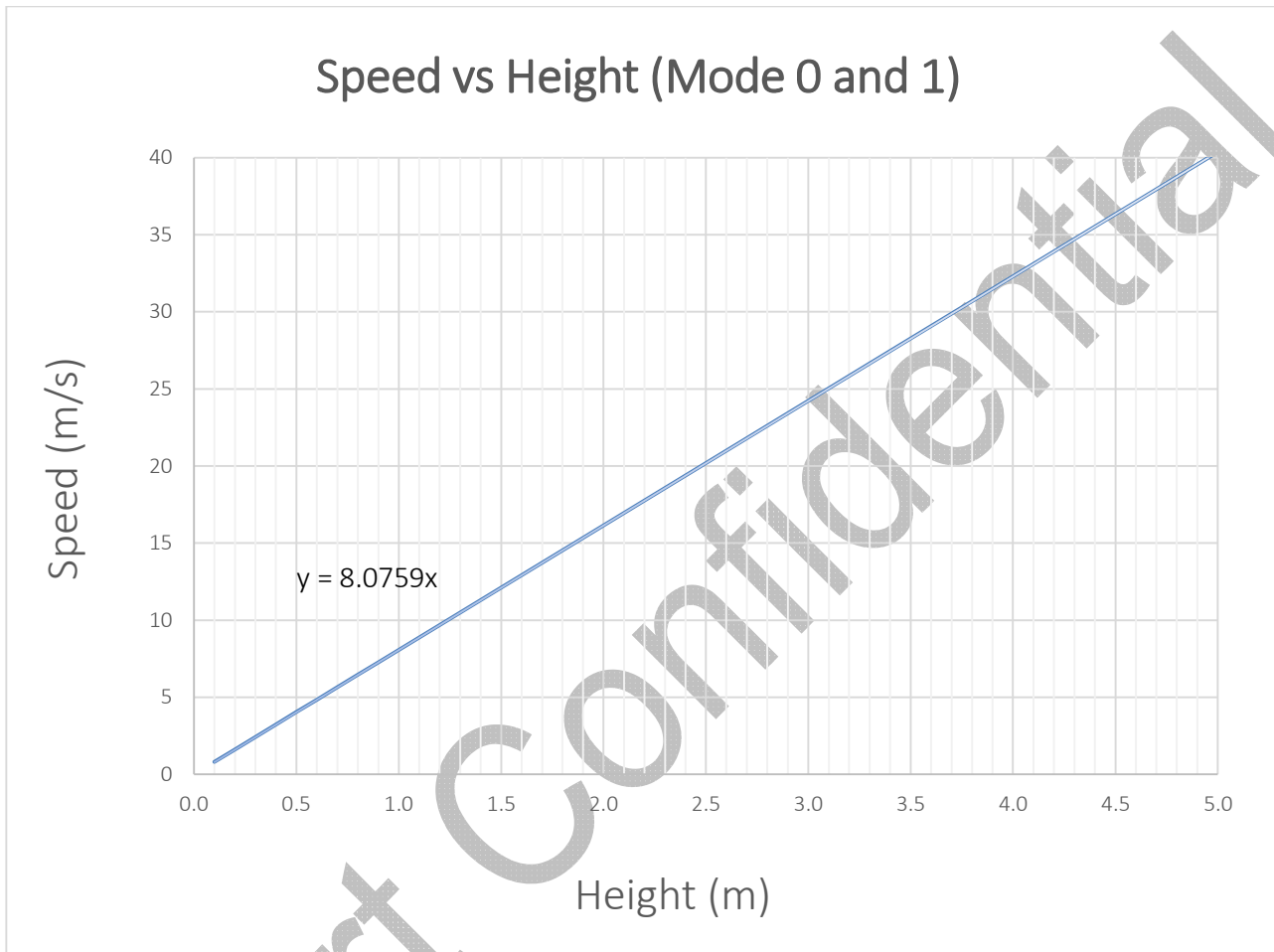
Note: Interpolation is applied beyond 0.5 m.

Figure 4. Speed versus Height Chart (Mode 0 & 1)

Speed vs Height (Mode 2)

$y = 3.2047x$
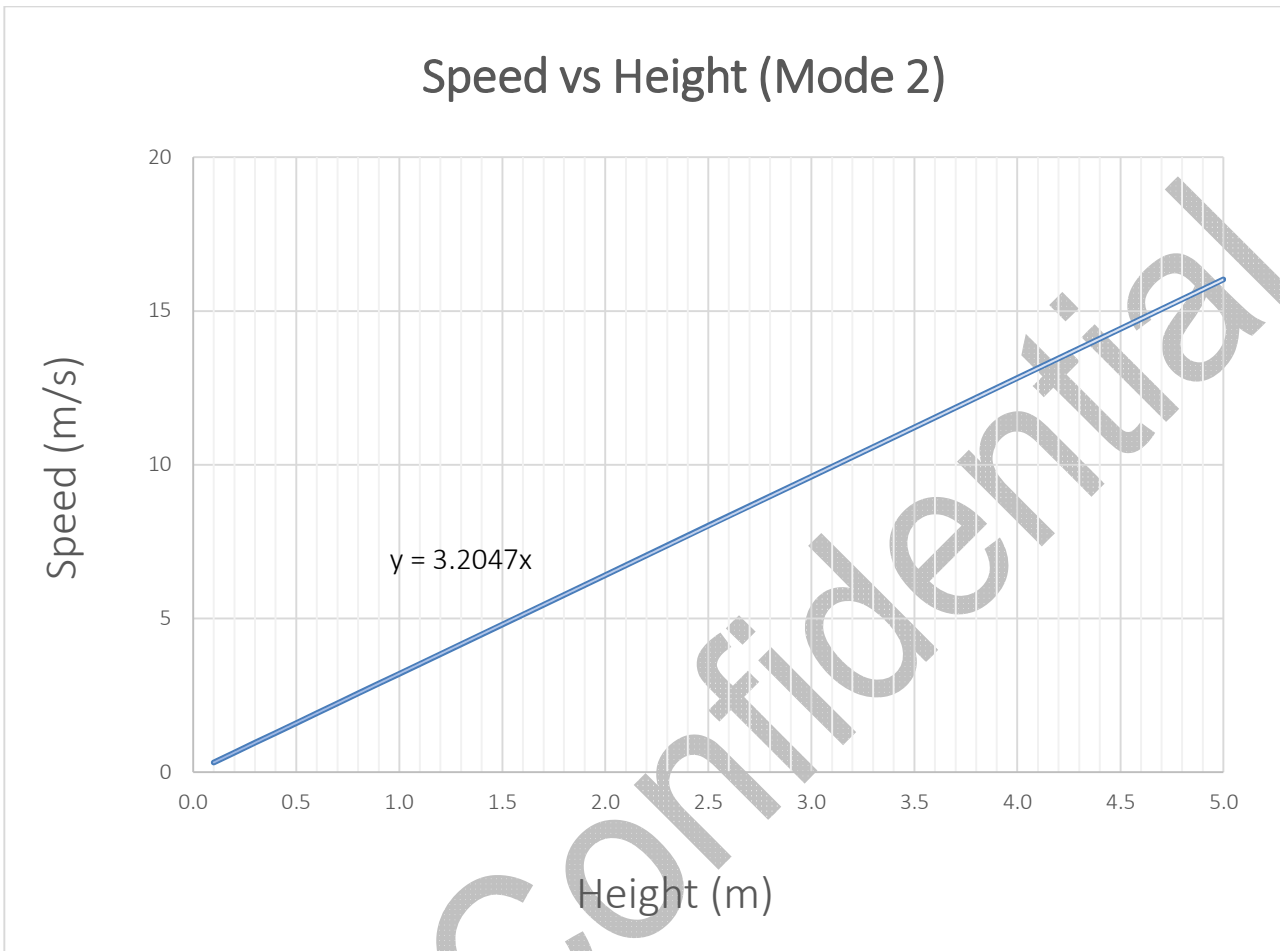
Note: Interpolation is applied beyond 0.5 m.

Figure 5. Speed versus Height Chart (Mode 2)

3.0 Mechanical Specifications

3.1 LGA Package Outline Drawing

Notes:
1. Dimensions in Milimeters [Inches]
2. Coplanarity of Pads: 0.08 mm
3. Non-cumulative pitch tolerance: ±0.10 mm
4. Maximum flash: 0.20 mm max
5. Dimensional tolerance: ±0.10 mm unless otherwise stated
6. Package referance: 12L-5X4-LGA_001
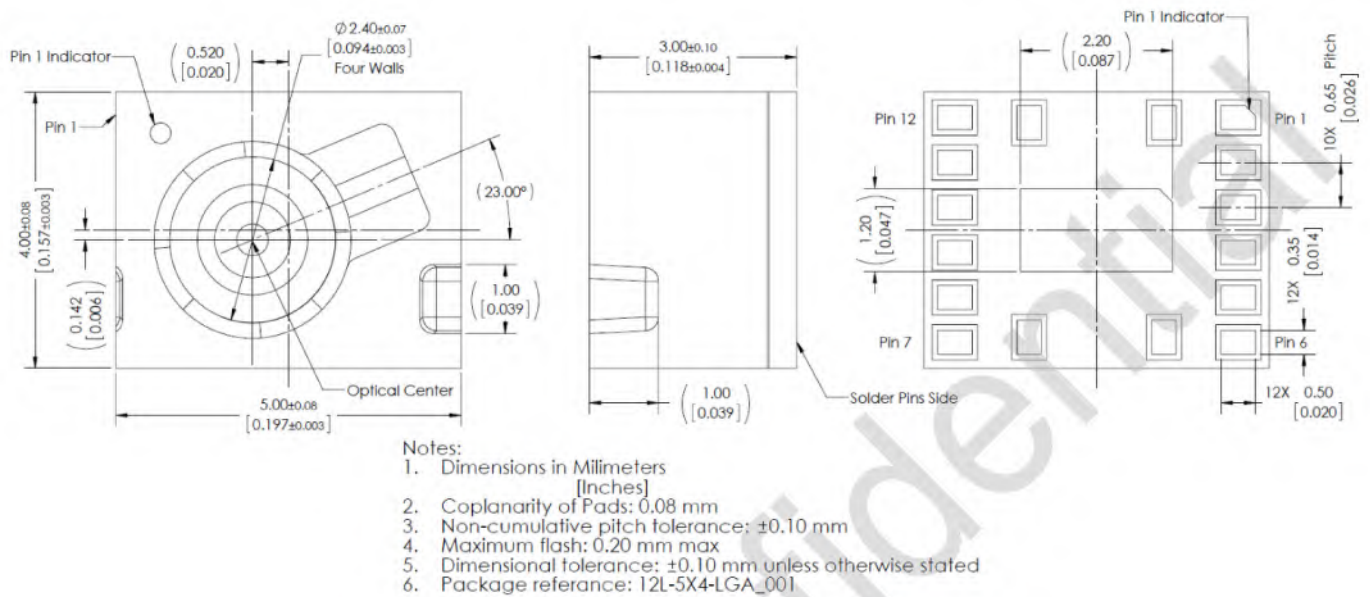
Figure 6. LGA Package Outline Drawing

3.2 Package Marking

Refer to Figure 2. Pin Configuration for the code marking the location on the device package.

Table 7. Code Identification

Code	Marking	Description
Product Number	PAA3905E1-Q	Part number label
Date Code	YWX	Date label

3.3 Packing Information

Item	Description
Product number	PAA3905E1-Q
Package type	12-pin LGA
Quantity per tube	80 pcs
Inner box quantity	2,000 pcs [25 tubes per inner box]
Shipping box quantity	24,000 pcs [12 inner boxes per shipping box]
Tube size	420 x 5.5 x 4.8 mm^3
Inner box size	89 x 540 x 58 mm^3
Shipping box size	310 x 560 x 270 mm^3
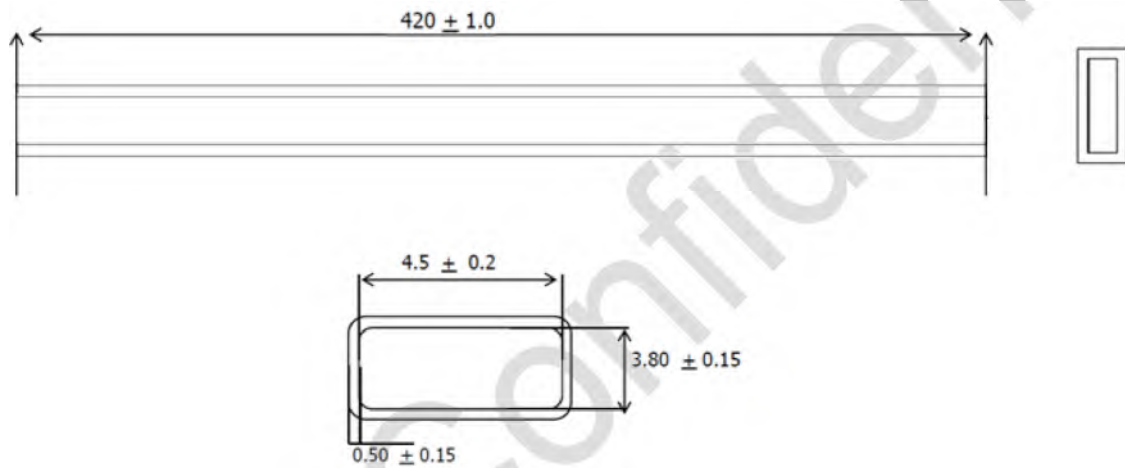
Figure 7. Tube Size (in mm)

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3.4 Package Handling Information

3.4.1 Sample of Inner Box Label

Note: This label is used on the inner box

3.4.2 Sample of Shipping Box Label

Note: This label is used on the shipping box

4.0 Design Reference

4.1 General Reference Schematic
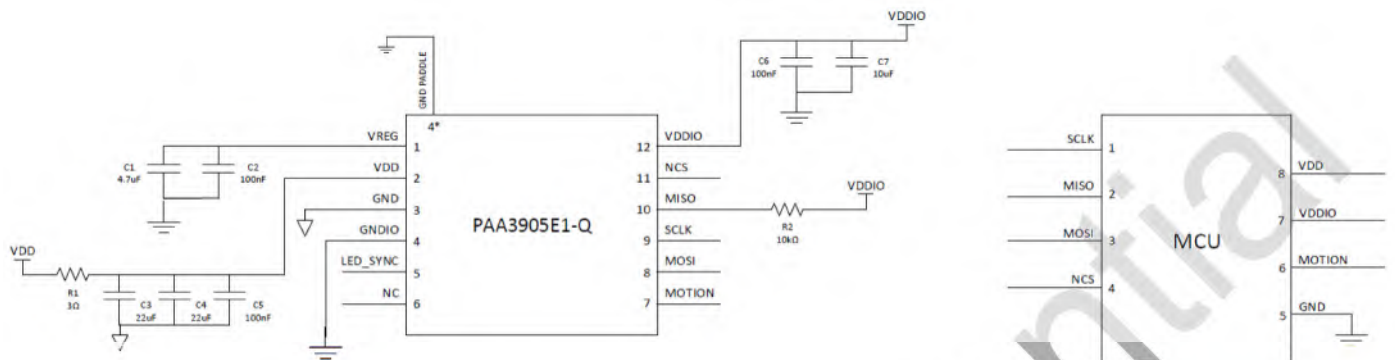
Note:
1. All capacitors must be placed as close as possible to VDD, VDDIO & VREG pins.
2. Ceramic non-polarity capacitors are recommended.

Figure 8. Reference Schematic

4.2 PCB Layout Design Guide

4.2.1 Recommended PCB Footprint
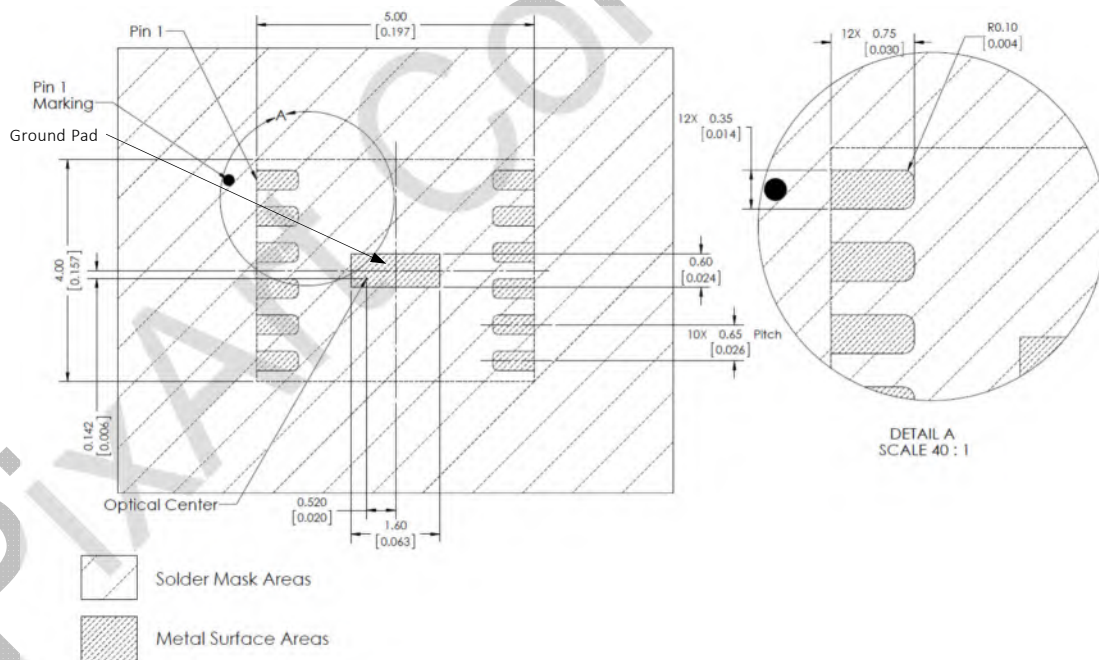
Note: The bottom ground pad of the LGA package must be connected to the circuit ground.

Figure 9. Recommended PCB Footprint

4.3   Assembly Guide

Proper grounding especially handling and assembly of the components in the PixArt manufacturing process is required to prevent the chip from being damaged prematurely or degradation of the chip performance.

4.3.1   IR Reflow Soldering Profile

- Surface mount the chip and all other electrical components onto PCB.
- Reflow the entire assembly in a no-wash solder process.

Note: It is recommended to generate a stencil profile for the reflow process.

- Remove the protective Kapton tape on top of the chip's package.

Note: Avoid contamination of the cavity surface.

- Recommend to hold the PCB assembly vertically when removing Kapton tape.
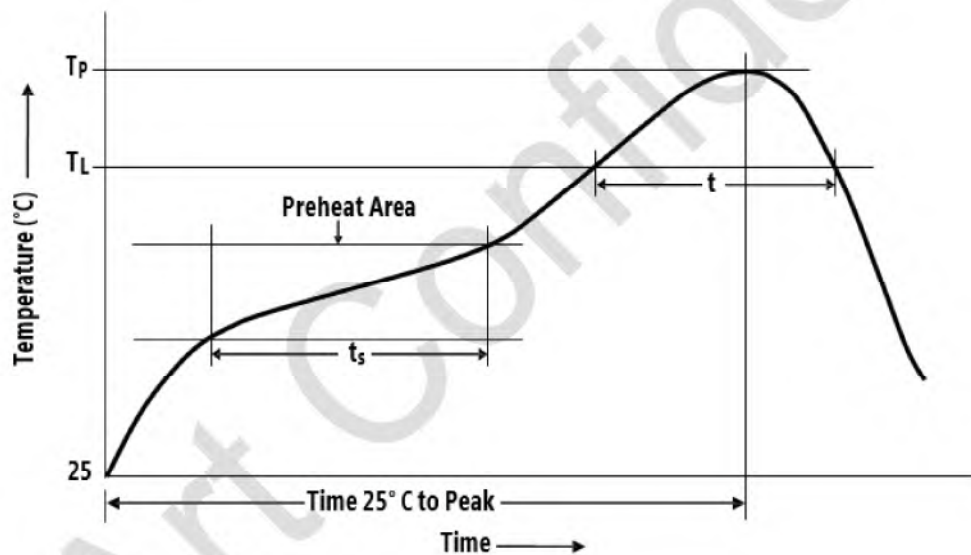
Figure 10. Solder Reflow Profile

Table 8. Reflow Profile

Specification	Value
Max rising slope	$0° - 3°C/sec$
Preheat duration ($150 - 190°C$), t_s	$60 - 120$ sec
Time above reflow ($T_L = 220°C$), t	$30 - 60$ sec
Peak temperature, T_p	$230 - 260°C$

Note: T_L is the Liquids Temperature

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4.3.2 Assembly Recommendation

1. Place the PCB assembly horizontally with the package cavity facing up. Insert the lens set with plastic or soft-tip tweezers onto the optical aperture (the chip's cavity).
2. Insert the lens set onto the chip package cavity (the hole on the chip's package).
3. Use an appropriate flat tip jig to press the lens barrel vertically onto the upper cavity of the chip's package.
4. Insert the nozzle of the glue dispenser vertically inside the gluing slots and dispense glue appropriately.
5. Remove the nozzle of the glue dispenser and let the glue cure properly.

Note:
1. No lens calibration is required.
2. Refer L242-ZSZ1 lens set datasheet for more information and detailed steps of the assembly process.
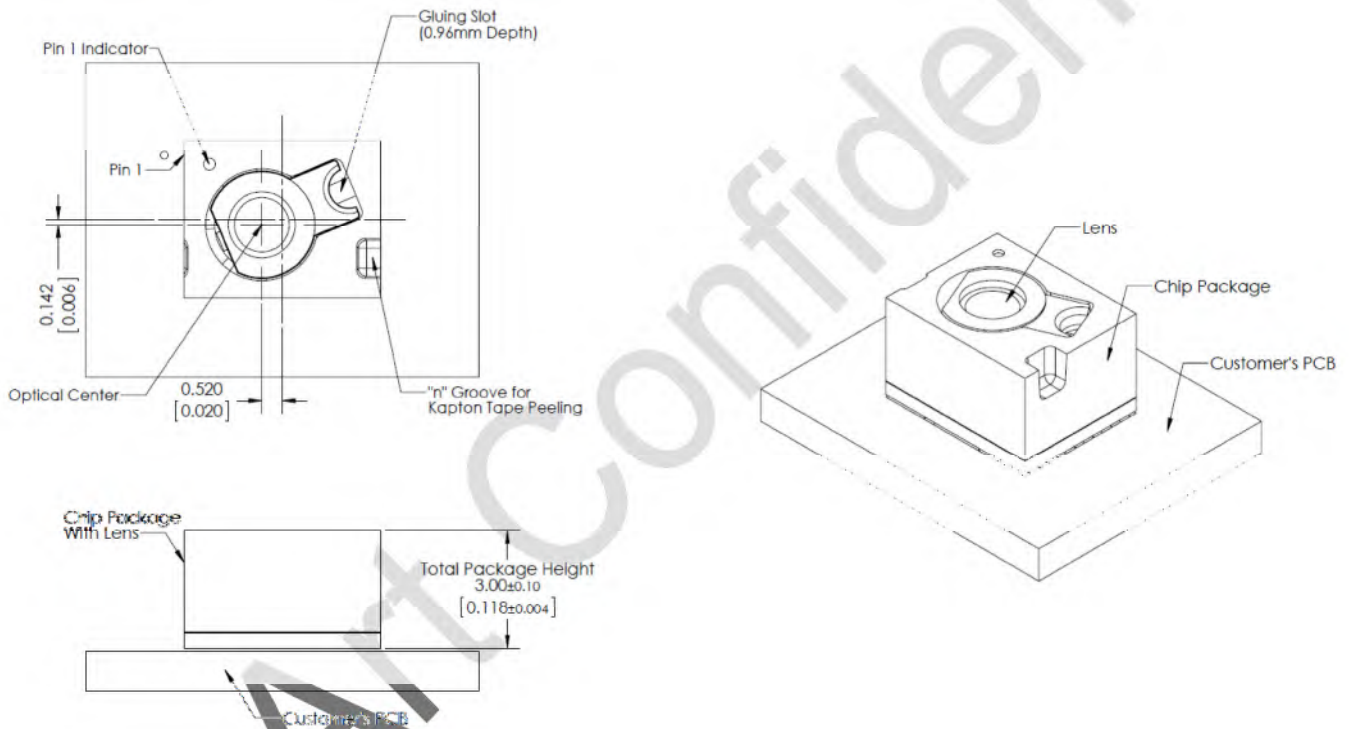
Figure 11. System Assembly View with L242-ZSZ1
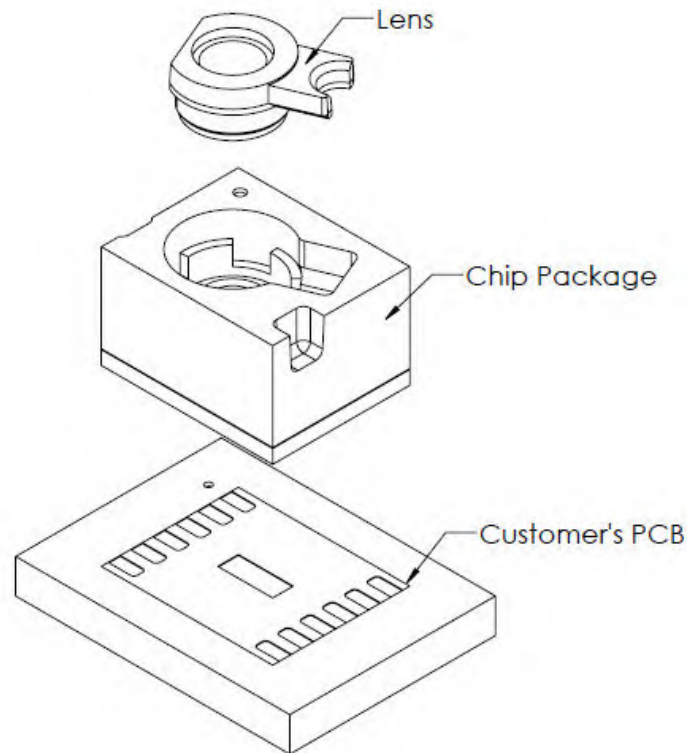
Figure 12. Exploded View of System Assembly

4.3.3 Manual rework of chip assembly

This is an optional step.

For the de-solder chip package from PCB, do disassemble the lens set first as it melts under the soldering heat.

Please note below precautions for re-work of the chip assembly.

▪ Pry up the lens set from the chip package cavity from the gluing slot using a tweezer.

Note: It is important to remove the lens set as it may melt under the soldering heat.

▪ Place Kapton tape across the top of the chip package cavity to avoid contamination

▪ Perform de-soldering & soldering activities as needed.

▪ Remove Kapton tape and insert the lens set as outlined in the above section.

5.0 Power Management

5.1 Power Supply

The chip has two power supply inputs (VDD and VDDIO). VDD is the main power supply and VDDIO is the I/O reference voltage.

5.2 Power Sequence

5.2.1 Power on Sequence Requirement

VDDIO needs to be powered up earlier than VDD, the interval time between VDD and VDDIO must be less than 100ms

Figure 13. Power-up Sequence Requirement

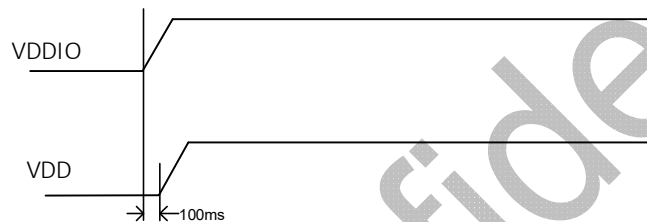### 5.2.2 Power off Sequence Requirement

It is recommended to power off both VDD and VDDIO at the same time or the VDD first, then followed by VDDIO.

5.3   Power States

5.3.1   States Description

Table 9. States Description

State	Description
OFF	No power supply and all the voltage rails and clocks are gated.
RUN	The chip enters RUN State after the regular power on and initialization.
Shutdown	The chip enters this state upon receiving the host command for power-saving purposes and all the parameter settings are still intact. The chip exits the shutdown state and transitions back to the RUN state upon receiving the host command. To exit the Shutdown state, only the power up command (write *Shutdown* register with value 0xC7) is accepted.

The table below shows the state of various pins during the shutdown.

Table 10. State of Signal Pins during Shutdown.

Pin	Status during Shutdown State
NCS	High [1]
MISO	Hi-Z [2]
SCLK	Ignore if NCS = 1 [3]
MOSI	Ignore if NCS = 1 [4]
MOTION	Output High

5.3.2   State Diagram
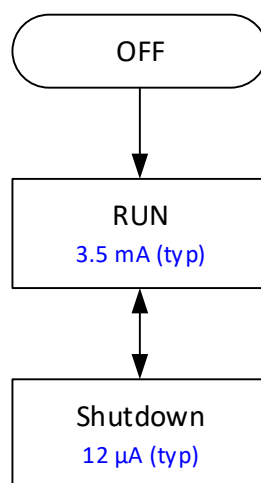
Figure 14. Power State Diagram

5.3.3 State Transition

State	Type	Description
OFF to RUN	Power-up	After the chip is powered on and initialization is completed, the chip enters the RUN state automatically.
RUN to Shutdown	Command	The host to send a command to enter the Shutdown state
Shutdown to RUN	Command	The hose to send command to exit the Shutdown state

▪ RUN to Shutdown

Write register 0x3B with value 0xB6   // Enter Shutdown state

▪ Shutdown to RUN

Step in sequence as follows:

1. Drive NCS high for 1ms, and then low   // To reset the SPI port
2. Write register 0x3B with value 0xC7   // Exit Shutdown state command
3. Wait for at least 1ms.
4. Write register 0x3B with value 0x00
5. Wait for at least 1ms.
6. Read from registers 0x02, 0x03, 0x04, 0x05 and 0x06   // read once to clear the registers

5.4   Reset

The table below shows the state of the various pins during power-up and reset.

Table 11. State of Signal Pins during Power-Up & Reset

State of Signal Pins after VDD is Valid		
Pin	**During Reset**	**After Reset**
NCS	Ignored	Functional
MISO	Undefined	Depends on NCS
SCLK	Ignored	Depends on NCS
MOSI	Ignored	Depends on NCS
MOTION	Undefined	Functional

5.4.1   Power on Reset

During power-on, the chip does not need an external reset as there is an internal circuitry that performs the power-on reset function for the chip.

5.4.2   Software Reset

Write 0x5A to the *Power_Up_Reset* register to reset the chip. All register settings will be reverted to default values, and the chip is required for re-initialization.

5.5 Related Registers

Usage	Name	Bank	Address
Power Management	*Shutdown Register*	-	0x3B
	Power_Up_Reset	-	0x3A

- Shutdown Register

Register Name	Shutdown		
Bank	-	Address	0x3B
Access	W	Default Value	-
Description	Shutdown state control register. Refer to Section 5.3.3 for the details.		

- Reset Register

Register Name	Power_Up_Reset		
Bank		Address	0x3A
Access	W	Default Value	-
Description	Write 0x5A to this register to reset the chip. All settings will revert to default values. Reset is required to restore normal operation after Raw Data Output.		

6.0 Control Interface

The chip adopts Serial Port Interface Communication (SPI) interface. The interface is configured to mode 3 (CPHA=1 and CPOL=1) for slave device communication. The maximum SCLK speed is 2MHz.

6.1 Signal Description

The 4-wire synchronous serial port interface is used to write or read registers in the chip. The host is an SPI master device where it drives SCLK, MOSI, and NCS (active low) to initiate the communication. The interface supports single or multi-chip (slaves) with NCS control.

Table 12. Signal Description

Pin	Reset Status	Description
SCLK	High	Clock input, generated by the host (master).
MOSI	High	Input data (Master Out / Slave In).
MISO	Hi-Z	Output data (Master In / Slave Out).
NCS	High	Chip select input (active low).

6.2 Chip Select Operation

The serial port is activated after NCS is asserted. If NCS is de-asserted during a transaction, the entire transaction is aborted and the serial port will be reset. After a transaction is aborted, the host needs to follow the normal address-to-data or transaction-to-transaction delay timing requirement before beginning the next transaction.

When the NCS pin is high, the SPI's inputs are ignored and the SPI's output is in tri-state. NCS can also be used to reset the serial port communication in case of an error occurred.

To improve communication reliability, all serial transactions should be framed by NCS assertion. The port should not be remained enabled when not in use to prevent misinterpretation of ESD and EFT/B events and put the chip into an unknown state.

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6.3　Protocol

The transmission protocol is a 4-wire link, the half-duplex protocol between the host and the chip. All data changes at SCLK falling edge and latched at SCLK rising edge. The host controller always initiates communication and the chip never initiates data transfers.

The transmission protocol consists of two types of operations:

- Write Operation
- Read Operation

Both the two operation modes consist of two bytes. The first byte contains the registered address (seven bits) and bit 7 as MSB to indicate data direction. The second byte contains the data.
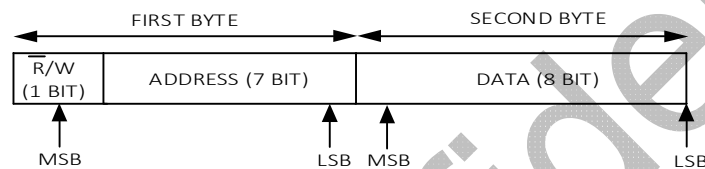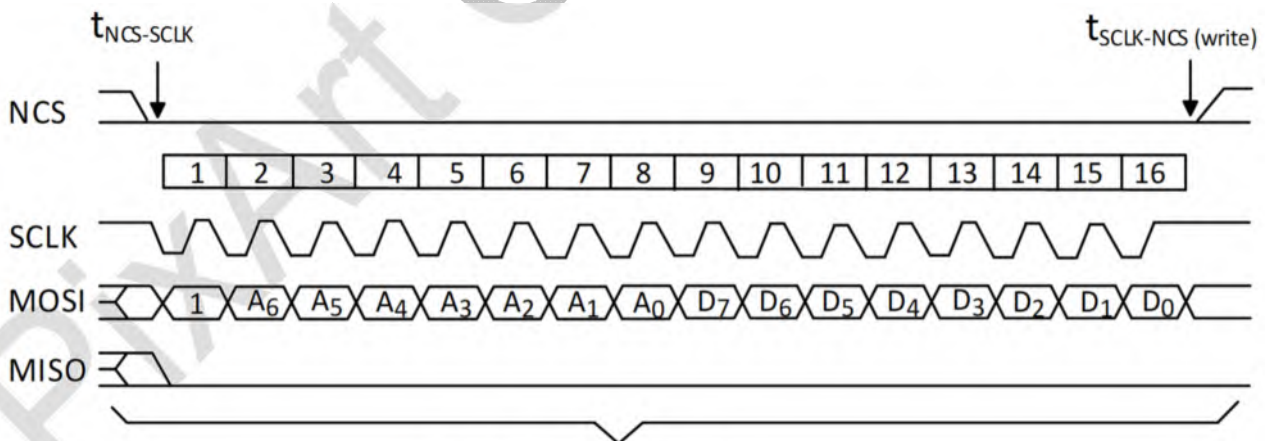

Figure 5. Transmission Protocol

6.4　Write Operation

The write operation consists of two bytes package. The first byte contains the 7-bit register address and a "1" in bit [7] indicates the data written directly from the host to the chip. The second byte contains the data to be written into the specified register. The chip latches MOSI data on rising edges of the SCLK.

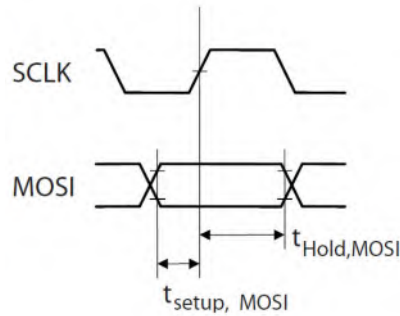Figure 15. Write Operation

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Figure 16. MOSI Set-up and Hold Time

6.5 Read Operation

The read operation consists of two bytes package. The first byte contains the 7-bit register address and a "0" in bit [7] indicates the data read directly from the chip to the host and the chip samples MOSI bits on every rising edge of SCLK. The second byte contains the data from the specified register and the chip outputs MISO bits on falling edges of SCLK.
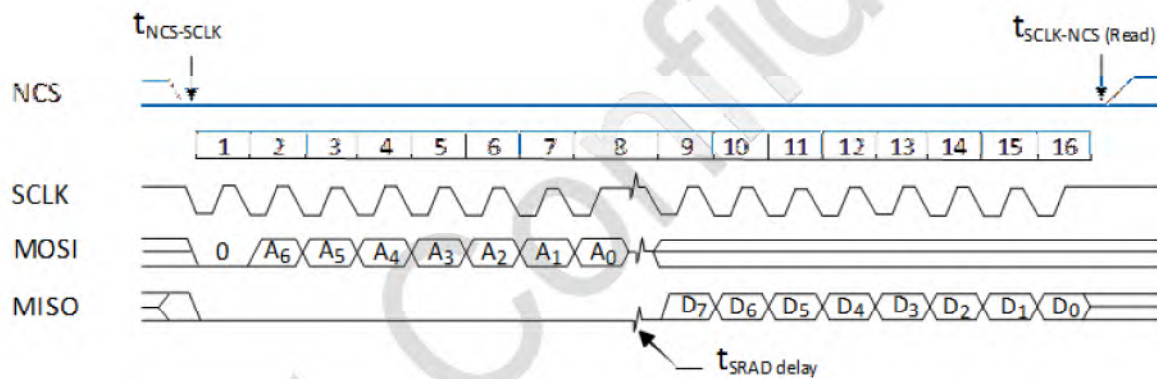

Figure 17. Read Operation

The minimum high state of SCLK is also the minimum MISO data hold time of the chip. Since the falling edge of SCLK is the start of the next read or write command, the chip will hold the state of data on MISO until the falling edge of SCLK.
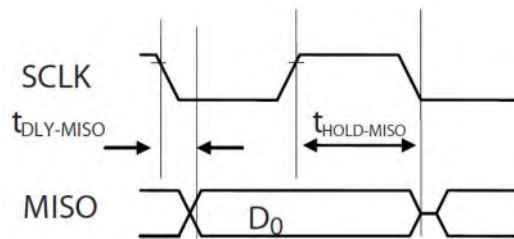

Figure 18. MISO Delay and Hold Time

6.6 Burst Read

Burst read is a special serial port interface operation mode that can be used to reduce the serial transaction time for Motion Read. The speed improvement is achieved by continuous data clocking to read multiple registers with a single dedicated address and not requiring the delay period between data bytes. Refer to Section 7.3.1 for the detail.

NCS must be de-asserted to terminate burst mode after each burst read operation transaction is completed. However, the host can terminate the Burst Read operation as needed by de-assert the NCS.

After sending the register address, the host must wait for t_{SRAD}, and then begin reading data. All data bits can be read with no delay between bytes by driving SCLK at the normal rate. The data are latched into the output buffer after the last address bit is received. After the burst transmission is completed, the host NCS is de-assert for at least t_{BEXIT} to terminate burst read operation. The serial port is not available for use until the assertion of NCS.
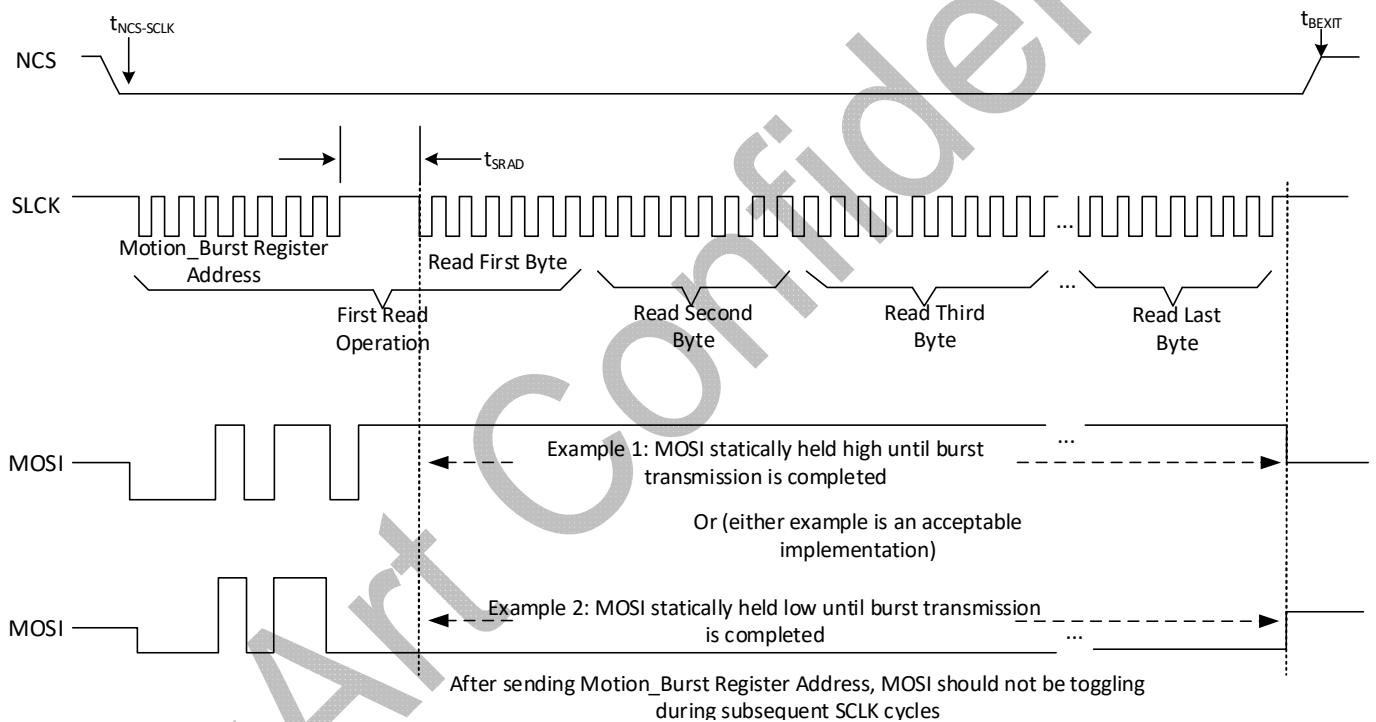

Figure 19. Burst Read Timing

6.7 Required Timing between Read and Write Commands (t$_{SXX}$)

There are minimum timing requirements between read and write commands on the serial port.

If the rising edge of the SCLK for the last data bit of the second write command occurs before the t$_{SWW}$ delay, then the first write command may not complete correctly.
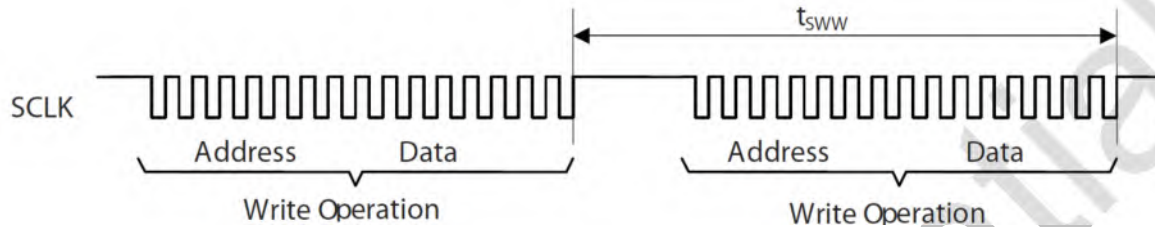

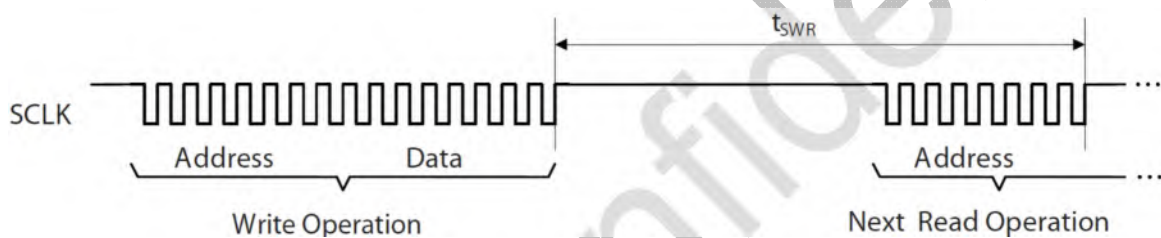Figure 20. The timing between two Write Commands

Figure 21. The timing between Write and Read commands

If the rising edge of SCLK for the last address bit of the read command occurs before the t$_{SWR}$ required delay, the write command may not complete correctly. During a read operation, SCLK should be delayed at least t$_{SRAD}$ after the last address data bit to ensure that the chip has time to prepare the requested data.

The falling edge of SCLK for the first address bit of either the read or write command must be at least t$_{SRR}$ or t$_{SRW}$ after the last SCLK rising edge of the last data bit of the previous read operation. In addition, during a read operation, SCLK should be delayed after the last address data bit to ensure that the chip has time to prepare the requested data.
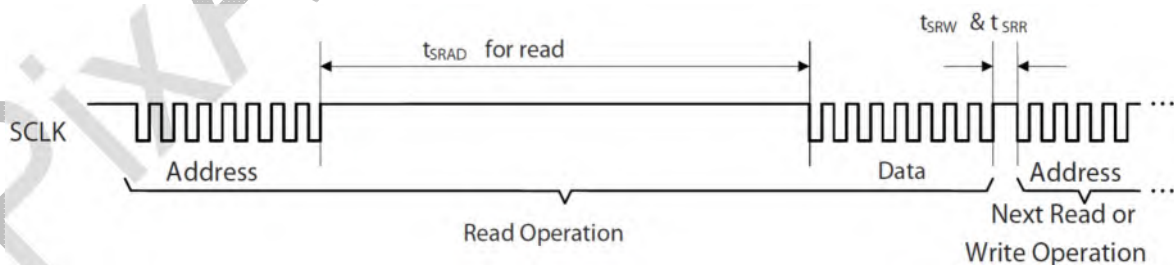

Figure 22. The timing between Read and either Write or subsequent Read commands

SEE. FEEL. TOUCH.

7.0 System Control

7.1 System Initialization

7.1.1 Initial Flow

Although the chip performs an internal self-power on reset, it is still recommended that the *Power_Up_Reset* register is written every time power is applied. The appropriate sequence is as follows:
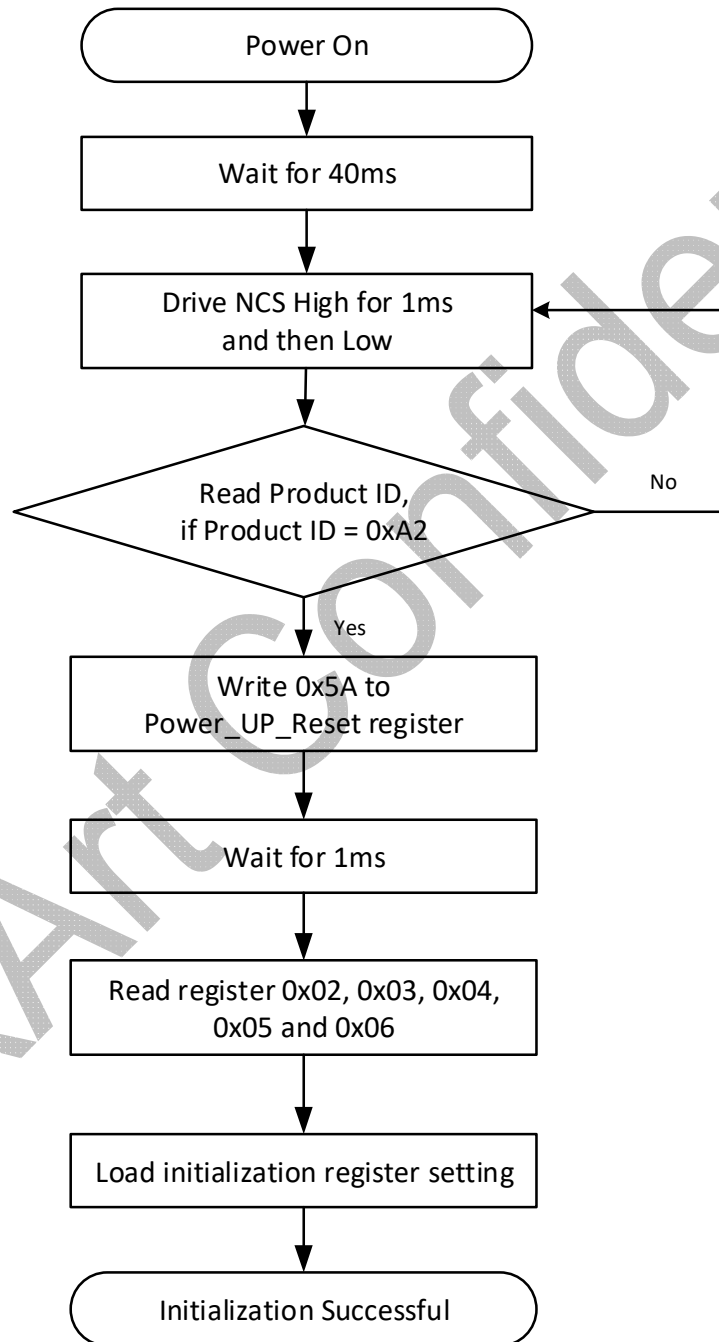

Figure 23. System Initialization Flow Chart

SEE. FEEL. TOUCH.

Note: If unable to read the correct Product ID, it is recommended to power off and power on the Module again. If the problem persists, please check the SPI interface connection and settings.

1. Apply power to VDDIO first and followed by V_{DD}, with a delay of no more than 100ms in between each supply. Ensure all supplies are stable.

2. Wait for at least 40 ms.

3. Drive NCS high for 1ms, and then low to reset the SPI port.

4. Read the *Product_ID* register to verify the PID before any other register read or write.

5. Write 0x5A to the *Power_Up_Reset* register.

6. Wait for at least 1 ms.

7. Read from registers 0x02, 0x03, 0x04, 0x05 and 0x06 one time regardless of the motion pin state to clear the motion data.

8. Refer to Section 7.1.2 to configure the needed registers to achieve optimum performance of the chip.

7.1.2 Initialization Register Setting

Upon power-up of the chip, there are a number of registers to be configured to initialize the chip. There are two types of Detection Mode Setting, Standard Detection Mode Setting, and Enhanced Detection Mode Setting.

- A standard Detection Setting is recommended for general tracking operations. In this mode, the chip can detect when it is operating over a striped, checkerboard, and glossy tile surfaces where tracking performance is compromised.

- Enhance Detection Setting has better detection sensitivity to challenging conditions. However, this setting reduces tracking performance, compared to the Standard Detection Setting, as it is more sensitive to trigger motion cut-off. Thus, it is recommended to use this setting where yaw motion detection is required, and also where more sensitive challenging condition detection is required. The recommended operating height must be greater than 15 cm to avoid false detection in challenging conditions due to an increase in sensitivity.