PAT9136E1-TXQT: Optical Tracking Chip

General Description

The PAT9136E1-TXQT is PixArt Imaging's latest optical tracking chip designed to enable navigation up to the speed of 5m/s on a wide range of surfaces. The chip is housed in a 6 x 6 x 1.35 mm^3 16-pin land-grid-array (LGA) package with an integrated laser illumination that provides X-Y motion data and consistent resolution. It is suitable for motion tracking in industrial applications.

Key Features

- Performance
  - Speed of up to 5m/s
  - Working Distance to Tracking Surface range of 5 to 50mm on glossy metal surfaces[*1]
  - Working Distance to Tracking Surface range of 10 to 27mm on glossy non-metal surfaces[*2]
  - Typical power consumption of 16.5mA
- No lens required
- Reports accurate XY motion data

Applications

- Devices that require high speed motion detection over a wide working range

Key Parameter

Parameter	Value
Supply Voltage	VDD: 1.8 to 2.1 V VDD_VCSEL: 2.8 to 3.3 V VDDIO: 1.8 to 3.3 V
Working Distance to Tracking Surface	5 to 50 mm*[1]
Frame Rate (max.)	20,000 fps
Speed (max.)	5 m/s
Acceleration	10 g; 98 m/s^2
Resolution (max.)	20,000 cpi; 7,874 count/cm
Interface	4-Wire SPI @ 4 MHz
Package Size (mm^3)	6 x 6 x 1.35

Note*[1]: Aluminum and glossy stainless steel

Note*[2]: Glossy vinyl flooring, glossy gypsum board, glossy photo paper, green ESD mat and laminated wood.

Ordering Information

Part Number	Description	Package Type	Packing Type	MOQ
PAT9136E1-TXQT	Optical Tracking Chip	16-pin LGA Package	Tube	2000

For any additional inquiries, please contact us at https://www.pixart.com

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1.0 Introduction

1.1 Overview

The PAT9136E1-TXQT is based on Optical Navigation Technology, which measures changes in position by optically acquiring sequential picture elements and mathematically determining the direction and magnitude of movement. The chip contains a Picture Element Acquisition System (PEAS), a hard-coded Digital Signal Processing System (DSPS), and an integrated VCSEL illumination source.

The chip algorithm calculates the speed, direction, magnitude of motion and stores the motion data output information in the registers. Then, the host either uses the polling method or interrupts triggering for immediate access.

Note: Throughout this document, the PAT9136E1-TXQT is referred to as the "chip".

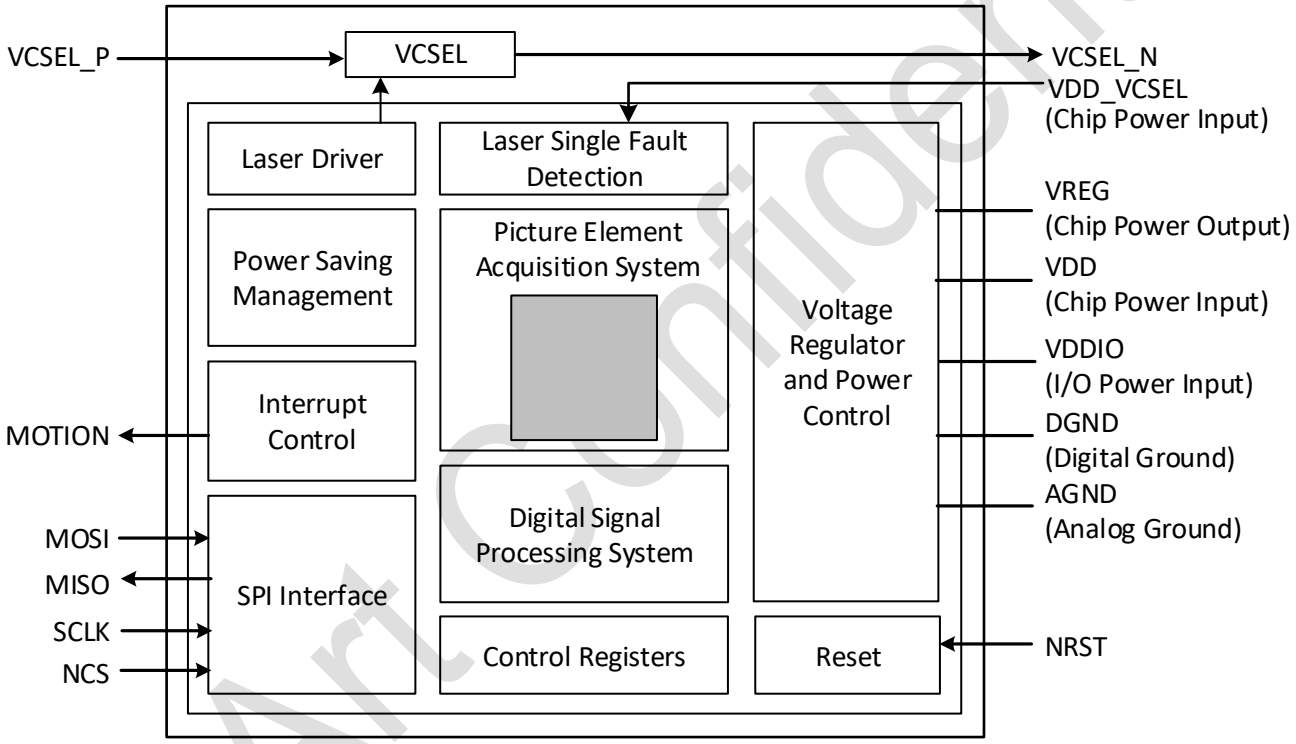
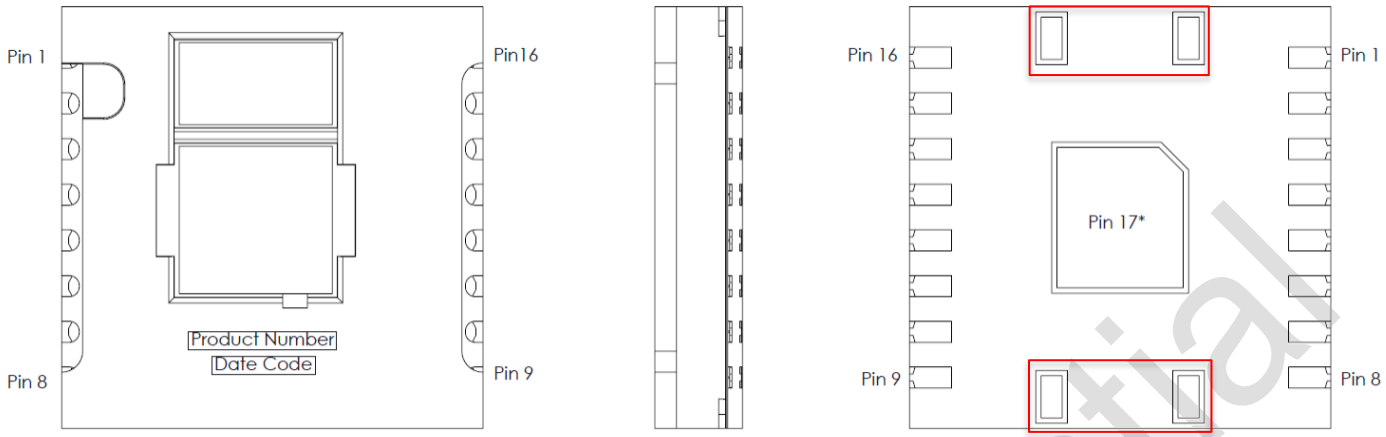


Figure 1. Block Diagram

1.2 Terminology

Term	Description
ESD	Electrostatic Discharge
I/O	Input / Output
VCSEL	Vertical Cavity Surface Emitting LASER
cpi	count per inch
fps	frame per second

1.3 Signal Description



Note: The 4 pads in Figure 2 (red boxed) must be left unconnected.

Figure 2. Pin Configuration

Table 1. Signal Pins Description

Function	Pin No.	Signal Name	Type	Description
Power Supplies	8	DGND	Ground	Digital Ground
	13	AGND	Ground	Analog Ground
	9	VDDIO	Power	I/O power input
	11	VREG	Power	Chip power output
	12	VDD	Power	Chip power input
	15	VDD_VCSEL	Power	Chip power input
Control Interface	3	NCS	Input	Chip select (Active low)
	4	MISO	Output	Serial data output
	5	MOSI	Input	Serial data input
	6	SCLK	Input	Serial data clock
Functional I/O	2	NRST	Input	Hardware reset (Active low)
	7	MOTION	Output	Motion interrupt (Active low)
Special Function Pin	1	VCSEL_P	Input	Laser Anode
	10, 14	NC	NC	No connection (floating)
	16	VCSEL_N	Output	Laser Cathode
	17*	GND PADDLE	Ground	Bottom of LGA package must be connected to circuit ground.

2.0 Operating Specifications

2.1 Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Note
Storage Temperature	T_S	-40	85	°C	
Lead-Free Solder Temperature	T_P		260	°C	
Power Supply Voltage	VDD	-0.5	2.2	V	
	VDD_VCSEL	-0.5	3.5	V	
	VDDIO	-0.5	3.5	V	
I/O pin Voltage	-	-0.5	VDDIO	V	All I/O pins
ESD	ESD_{HBM}		2	kV	All pins (Human Body Model)

Notes:

1. Maximum Ratings are the maximum parameter values that can damage the device when exceeding this limit.
2. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not recommended.

2.2 Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Operating Temperature	T_A	0		60	°C	
Power Supply Voltage	VDD	1.8	1.9	2.1	V	Including supply noise
	VDD_VCSEL	2.8	3.0	3.3	V	Including supply noise
	VDDIO	1.8	1.9	3.3	V	Including supply noise
Power Supply Rise Time	t_{RT}	0.15		20	ms	0 to VDD, VDD_VCSEL & VDDIO min
Supply Noise (Sinusoidal)	V_{NA}			100	mV	Peak to peak noise voltage. 10 kHz to 75 MHz
Serial Port Clock Frequency	f_{SCLK}			4	MHz	50% duty cycle
Resolution	R			20,000	cpi	(7874 count/cm)
Speed[3]	S		3.6	5	m/s	Glossy metal surfaces[4]
			3.6	5	m/s	Glossy non-metal surfaces[5]
			1.0	1.5	m/s	Diffuse surface - white paper
Working Distance from top of Chip to Tracking Surface[7]	Z_S	5		50	mm	Glossy metal surfaces[4]
		10		27	mm	Glossy non-metal surfaces[5]
		17		21	mm	Diffuse surface - white paper
Working Distance from top of 1.1mm cover to Tracking Surface, Z_{GAP}=0.7mm[7]	Z_C	3.2		48.2	mm	Glossy metal surfaces[4]
		8.2		25.2	mm	Glossy non-metal surfaces[5]
		15.2		19.2	mm	Diffuse surface - white paper
Frame Rate	F_R			20,000	fps	
Acceleration	a			98	m/s^2	

Notes:

1. PixArt does not guarantee the performance of the system beyond the recommended operating condition limits.
2. Chip electrical characteristics over recommended operating conditions. Typical values at VDD= 1.9V, VDD_VCSEL= 3.0V, VDDIO= 1.9V, T_A= 25°C.
3. Maximum speed can be achieved when chip moves at 45° while typical speed can be achieved when chip moves at 0° and 90°. Below is the diagram of chip orientation vs chip moving direction.

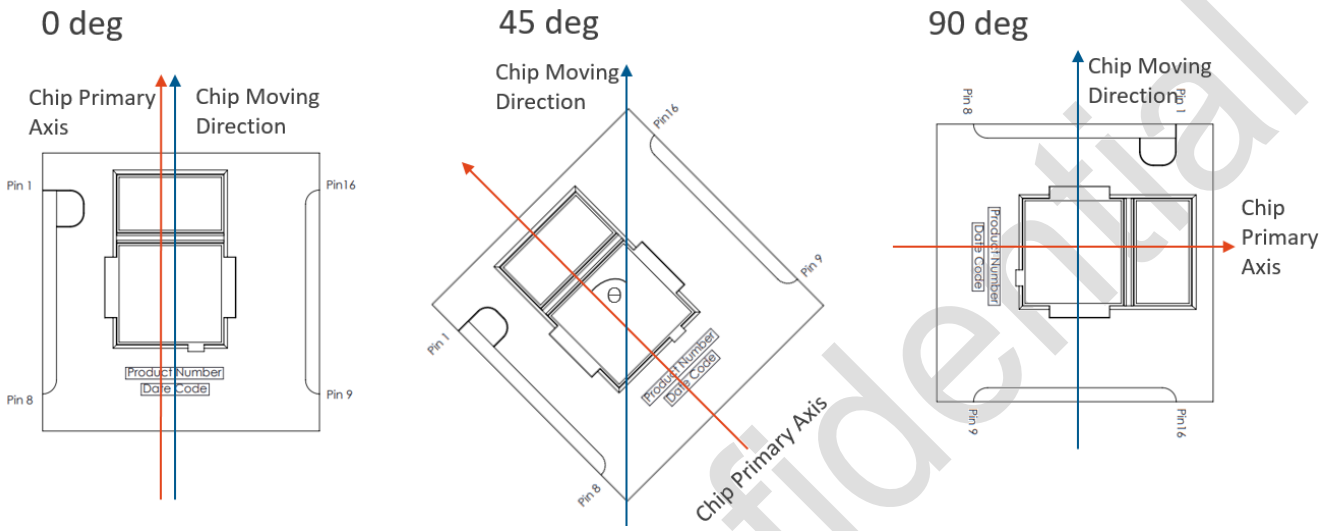


Figure 3. Chip Orientation vs Chip Moving Direction

4. Tested on Aluminum and stainless steel.
5. Tested on Glossy vinyl flooring, glossy gypsum board, glossy photo paper, green ESD mat and laminated wood.
6. For surfaces such as matte textured tiles, user may execute section 7.1.3 in order to improve the tracking performance. Please note that with the implementation of section 7.1.3, Resolution Variation RV_S% (over speed) will increase to 5%.
7. Zs, Zc and $Z_{GAP.}$ Do refer to section 4.5 for protective cover design.

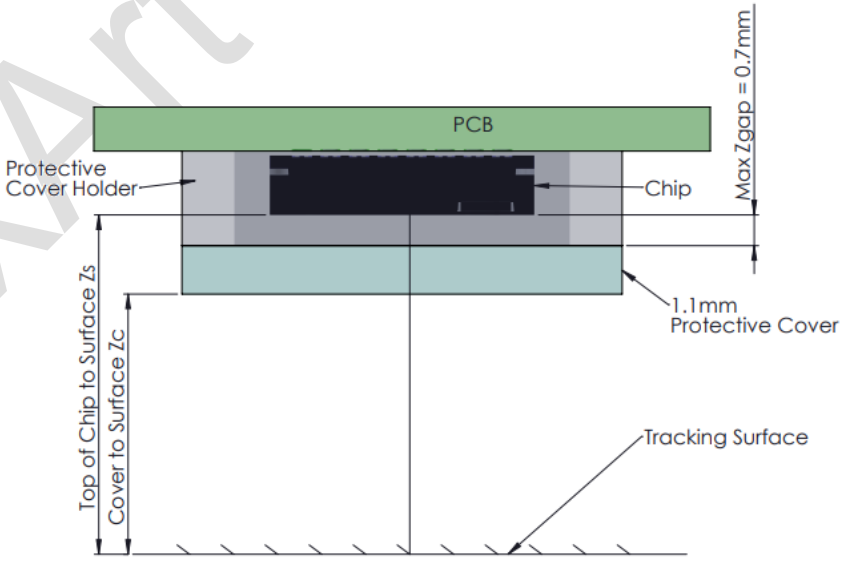


Figure 4. Cross Section View of Zs, Zc and ZGAP

2.3 DC Characteristics

Table 4. DC Electrical Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Current	I_{DD_RUN}		14.5		mA	Average current (chip only) No load on MISO, MOTION
	$I_{DD\_VCSEL\_RUN}$		2		mA	Average current with laser pulsing @ 20k fps
Shutdown state Current	I_{PD}		4		µA	
Input Low Voltage	V_{IL}			0.3 x VDDIO	V	SCLK, MOSI, NCS
Input High Voltage	V_{IH}	0.7 x VDDIO			V	SCLK, MOSI, NCS
Input Hysteresis	V_{I_HYS}		100		mV	SCLK, MOSI, NCS
Input Leakage Current	I_{LEAK}		± 1	± 10	µA	V_{in}= VDDIO or 0V, SCLK, MOSI, NCS
Output Low Voltage	V_{OL}			0.45	V	I_{OUT}= 1mA for MISO I_{OUT}= 0.1mA for MOTION
Output High Voltage	V_{OH}	VDDIO -0.45			V	I_{OUT}= -1mA for MISO I_{OUT}= -0.1mA for MOTION

Note: Electrical Characteristics are defined under recommended operating conditions. Typical values at VDD= 1.9V, VDD_VCSEL= 3.0V, VDDIO= 1.9V, T_A= 25°C.

2.4 AC Characteristics

Table 5. AC Electrical Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Motion Delay After Reset Time	$t_{MOT-RST}$	120			ms	From reset to valid motion, assuming motion is present.
Shutdown State Time	t_{STDWN}			500	ms	From Shutdown State active to low current.
Wake up from Shutdown State Time	t_{WAKEUP}	120			ms	From Shutdown State inactive to valid motion. **Note**: A RESET must be asserted after a Shutdown State. Refer to section 5.3, also note $t_{MOT-RST.}$
MISO Rise Time	t_{r-MISO}		6		ns	C_L = 20pF
MISO Fall Time	t_{f-MISO}		6		ns	C_L = 20pF
MISO Delay After SCLK	$t_{DLY-MISO}$			35	ns	From SCLK falling edge to MISO data valid. C_L = 20pF.
MISO Hold Time	$t_{hold-MISO}$	25			ns	Data held until next falling SCLK edge.
MOSI Hold Time	$t_{hold-MOSI}$	25			ns	Amount of time data is valid after SCLK rising edge.
MOSI Setup Time	$t_{setup-MOSI}$	25			ns	From data valid to SCLK rising edge.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
SPI Time Between Write Commands	t_{SWW}	5			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second data byte.
SPI Time between Write and Read Commands	t_{SWR}	5			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second address byte.
SPI Time between Read and Subsequent Commands	t_{SRW}, t_{SRR}	2			µs	From rising SCLK for last bit of the first data byte, to falling SCLK for the first bit of the address byte of the next command.
SPI Read Address-Data Delay	t_{SRAD}	2			µs	From rising SCLK for last bit of the address byte, to falling SCLK for first bit of data being read.
NCS Inactive After Motion Burst	t_{BEXIT}	500			ns	Minimum NCS inactive time after motion burst before next SPI usage
NCS To SCLK Active	$t_{NCS-SCLK}$	120			ns	From last NCS falling edge to first SCLK rising edge.
SCLK To NCS Inactive (For Read Operation)	$t_{SCLK-NCS}$	120			ns	From last SCLK rising edge to NCS rising edge, for valid MISO data transfer.
SCLK To NCS Inactive (For Write Operation)	$t_{SCLK-NCS}$	1			µs	From last SCLK rising edge to NCS rising edge, for valid MOSI data transfer.
NCS To MISO High-Z	$t_{NCS-MISO}$			500	ns	From NCS rising edge to MISO high-Z state.
MOTION Rise Time	$t_{r-MOTION}$		300		ns	C_L = 20pF
MOTION Fall Time	$t_{f-MOTION}$		300		ns	C_L = 20pF
Input Capacitance	C_{in}		10		pF	SCLK, MOSI, NCS.
Load Capacitance	C_L			20	pF	MISO, MOTION
Transient Supply Current	I_{DDT}			70	mA	Maximum supply current during the supply ramp from 0V to VDD with min. 150 µs and max. 20 ms rise time (does not include charging currents for bypass capacitors).
	I_{DDTIO}			60	mA	Maximum supply current during the supply ramp from 0V to VDDIO with min. 150 µs and max. 20 ms rise time (does not include charging currents for bypass capacitors).

Note: Electrical Characteristics are defined under recommended operating conditions. Typical values at VDD= 1.9V, VDD_VCSEL= 3.0V, VDDIO= 1.9V, T_A= 25°C.

2.5 Performance Specification

Table 6. Resolution Variation Specification

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Resolution Variation*	RV		1		%	At constant Speed and Working Distance from Tracking Surface @ 787 count/ cm.
Resolution Variation* (Over Height)	RV_H		3		%	At constant Speed, across Working Distance from Tracking Surface range @ 787 count/ cm.
Resolution Variation* (Over Speed)	RV_S		3		%	At constant Working Distance from Tracking Surface, up to max. Speed @ 787 count/ cm.

Note: *: Resolution Variation, RV = $\frac{(Rmax-Rmin)}{(Raverage)\ x\ 2}\ x\ 100\%$, chip mounted and tested at 45°.

3.0 Mechanical Specifications

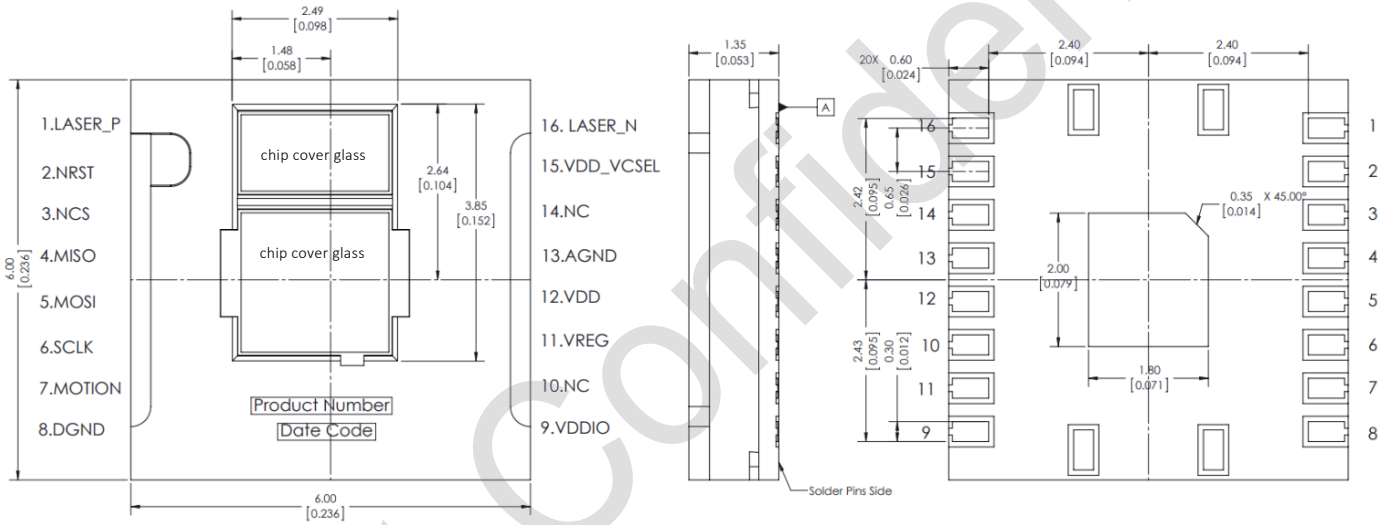
3.1 Package Marking

Refer to Figure 2. Pin Configuration for the code marking location on the device package.

Table 7. Code Identification

Label	Marking	Description
Product Number	P9136	Part number label
Date Code	YWX	Y: Year W: Week X: Reserved as PixArt reference

3.2 LGA Package Outline Drawing



Notes:

1. Dimensions in milimeter [inches]
2. Dimensional tolerance: ±0.1mm
3. Coplanarity of lead:0.1mm
4. Lead pitch tolerance: ±0.15mm

Notes:

5. Non-cumulative pitch tolerance: ±0.15mm
6. Maximum Burr:0.2mm
7. Angular tolerance: ±3°
8. Brackets () indicate reference dimension
9. Document Number:16L-6x6-LGA-G8

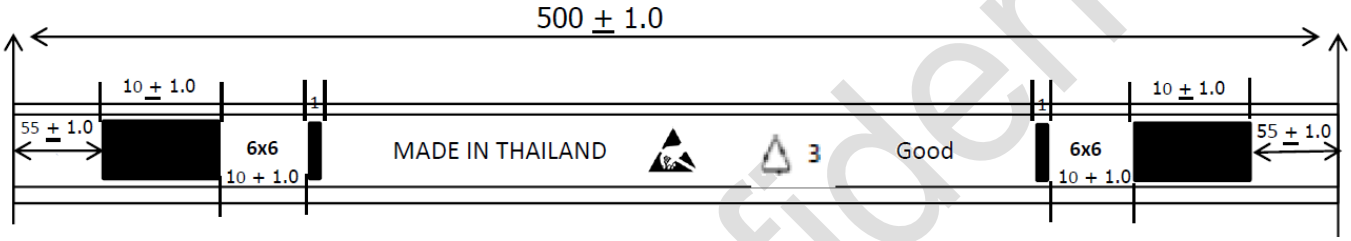
Note: It is advised that normal static discharge precautions be taken in handling and assembling of this component to prevent damage and/or degradation which may be induced by ESD.

Figure 5. LGA Package Outline Drawing

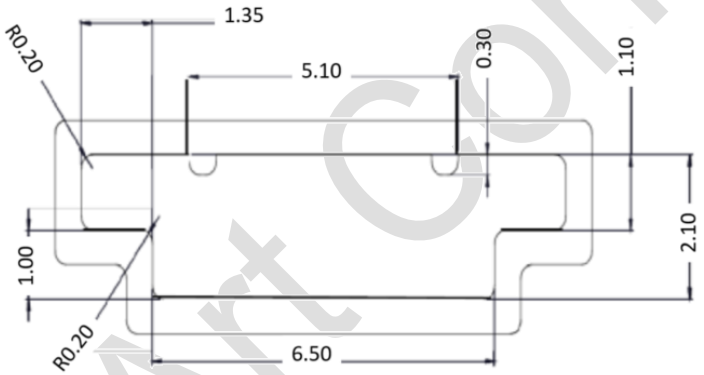
3.3 Packing Information

Parameter	Description
Part Number	PAT9136E1-TXQT
Package Type	16 Pins LGA
Tube Quantity	80 pcs
Packing	Vacuum Pack
Inner Box Quantity	2000 units
Shipping Box Quantity	24,000 units
Inner box size	89 x 540 x 58 mm^3
Shipping Box size	310 x 560 x 270 mm^3

Top View



Side View



Tube
Material: CLEAR PVC ANTISTATIC COATED
Marking: As above and add "MADE IN THAILAND" with ESD logo, PVC recycle logo and "Good" at center of tube.
Tolerance: ± 0.15mm unless specify.
Units are in mm.

Figure 6. Tube Dimension

Figure 7. Moisture Barrier Bag

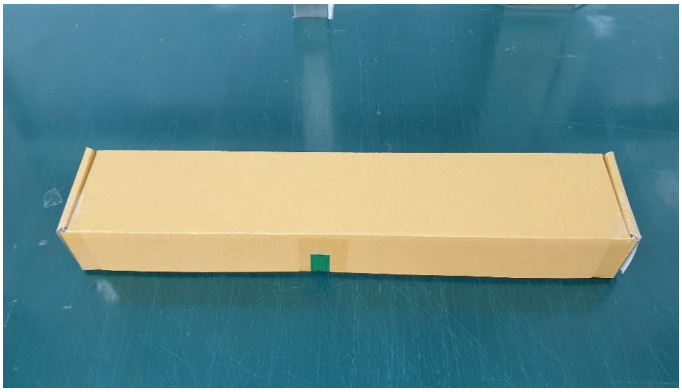


Figure 8. Inner Box

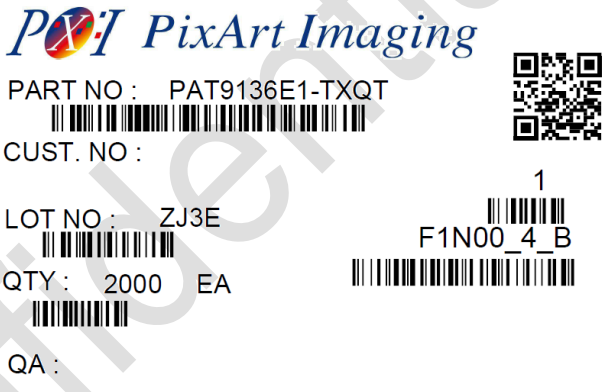


Figure 9. Inner Box Label

Figure 10. Shipping Box

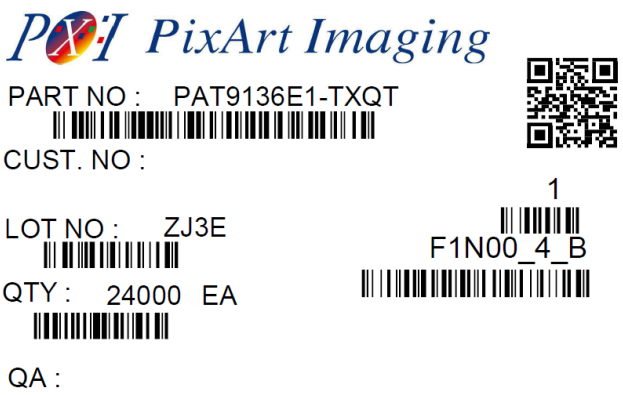
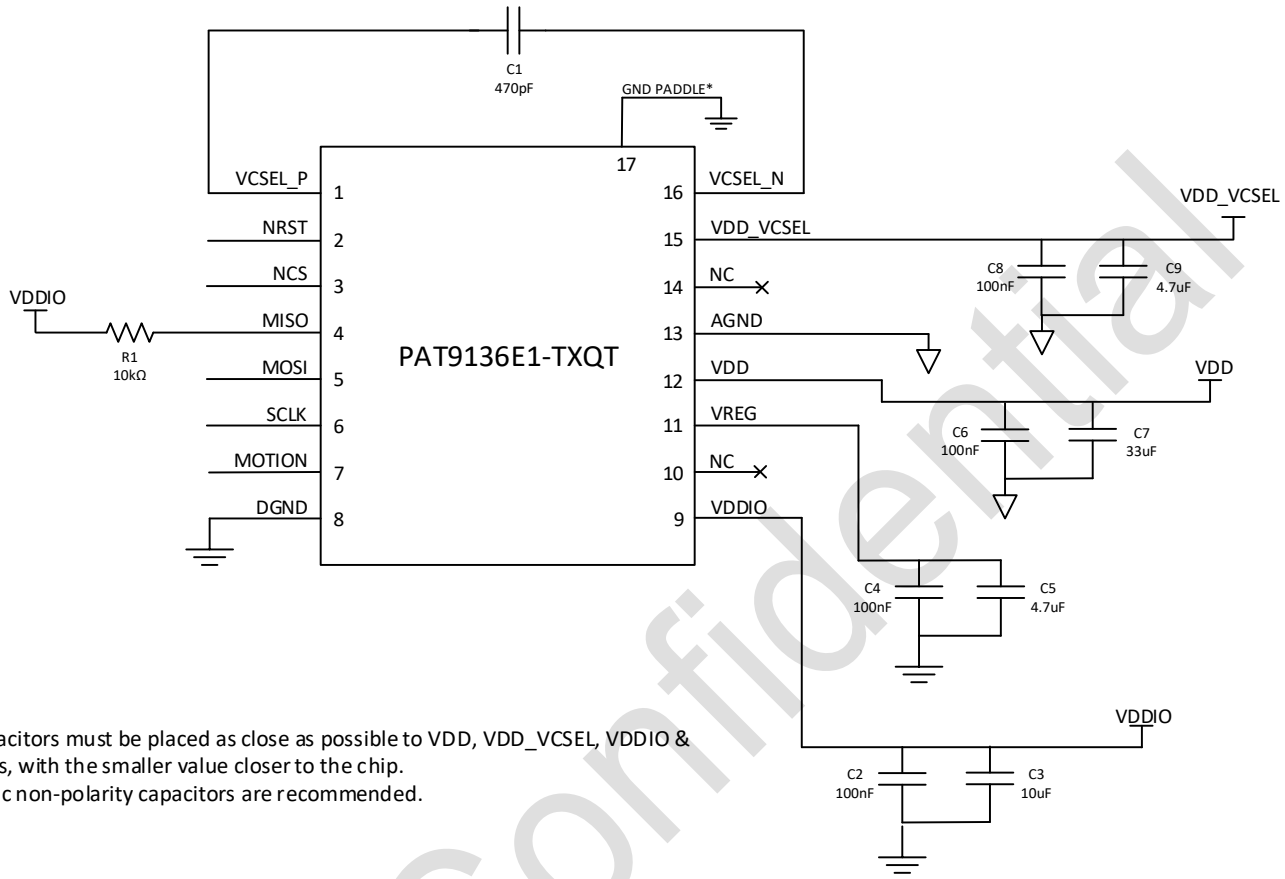


Figure 11. Shipping Box Label

4.0 Design Reference

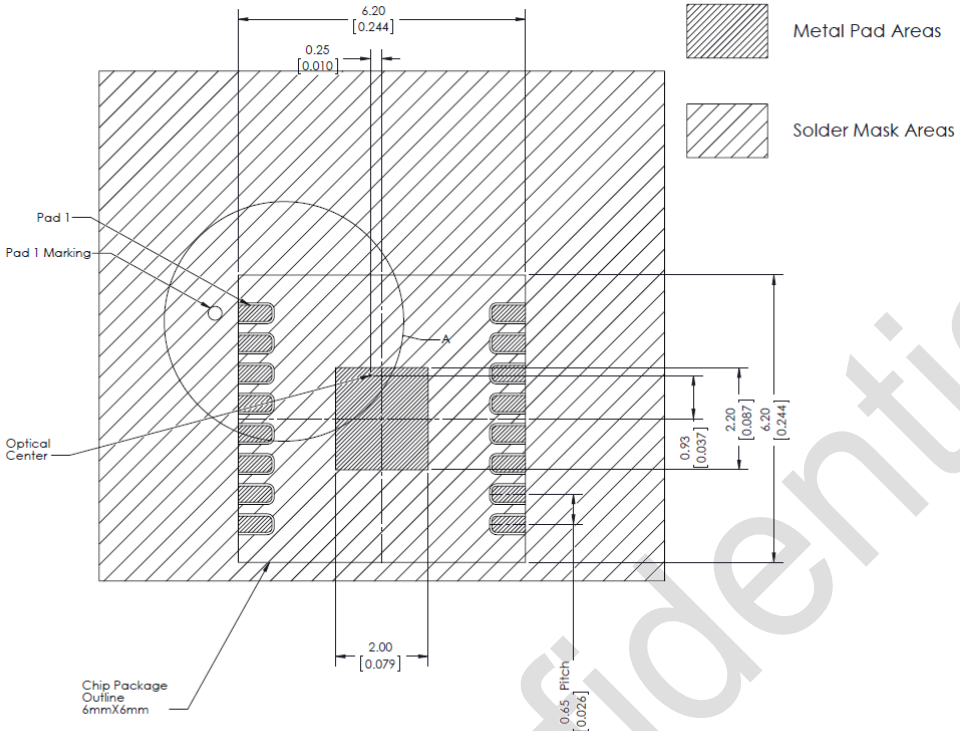
4.1 General Reference Schematic



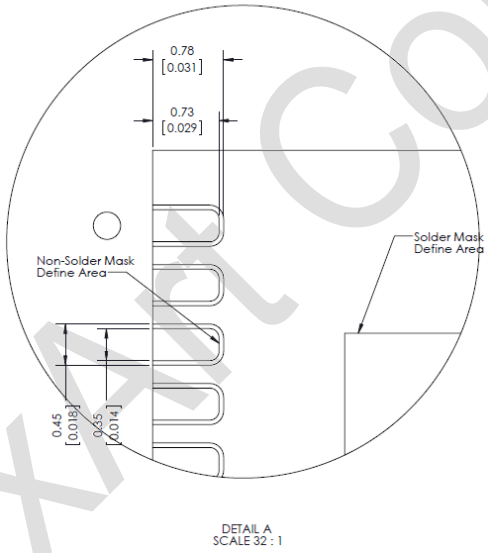
Note:
1. All capacitors must be placed as close as possible to VDD, VDD_VCSEL, VDDIO & VREG pins, with the smaller value closer to the chip.
2. Ceramic non-polarity capacitors are recommended.

Figure 12. Reference Schematic

4.2 Recommended PCB Foot Print



Note: Bottom center pad of LGA package must be connected to circuit ground



Notes:

1. Dimensions in milimeter [inches]
2. Dimensional tolerance: ±0.1mm
3. Coplanarity of lead:0.1mm
4. Lead pitch tolerance: ±0.15mm
5. Non-cumulative pitch tolerance: ±0.15mm
6. Angular tolerance: ±3°
7. Brackets () indicate reference dimension

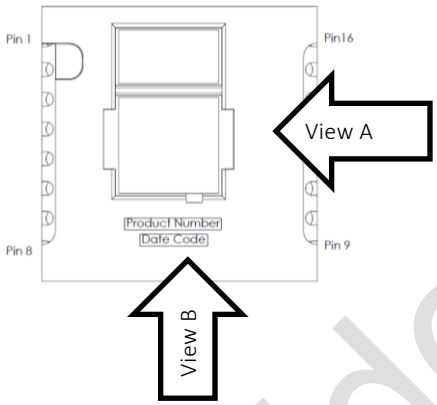
Figure 13. Recommended PCB Layout in mm [inch]

4.3 Chip Assembly Tilt

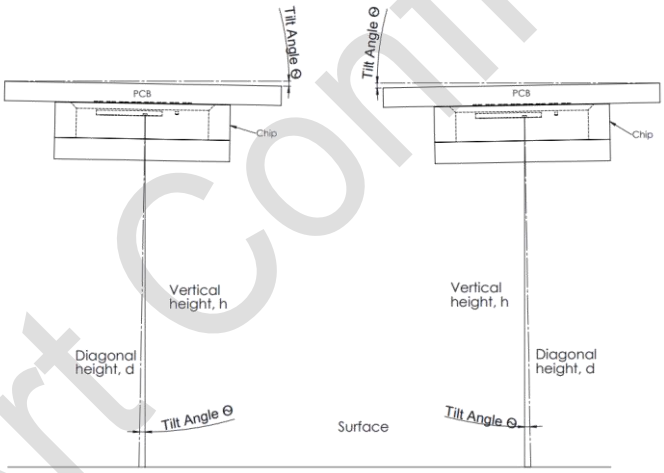
For optimal performance, there should be minimal tilt to the assembly of the chip on the PCB. The tilt should not be more than 3 degrees for trackable surfaces.

If the tilt angle is larger than 3 degrees, the Resolution Variation % will increase significantly over the working range stated in Table 3.

Chip Tilt Angles are defined per below drawings from view A and view B.



View A



View B

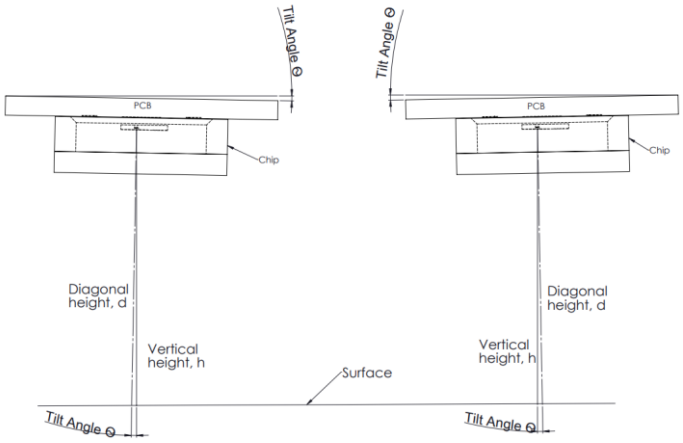


Figure 14. Tilt Definition

4.4 Keep Out Area

A keep out area of 30° angle is recommended to ensure the optical path of the chip is not blocked.

The 30° angle is from the top of the protective cover for the chip.

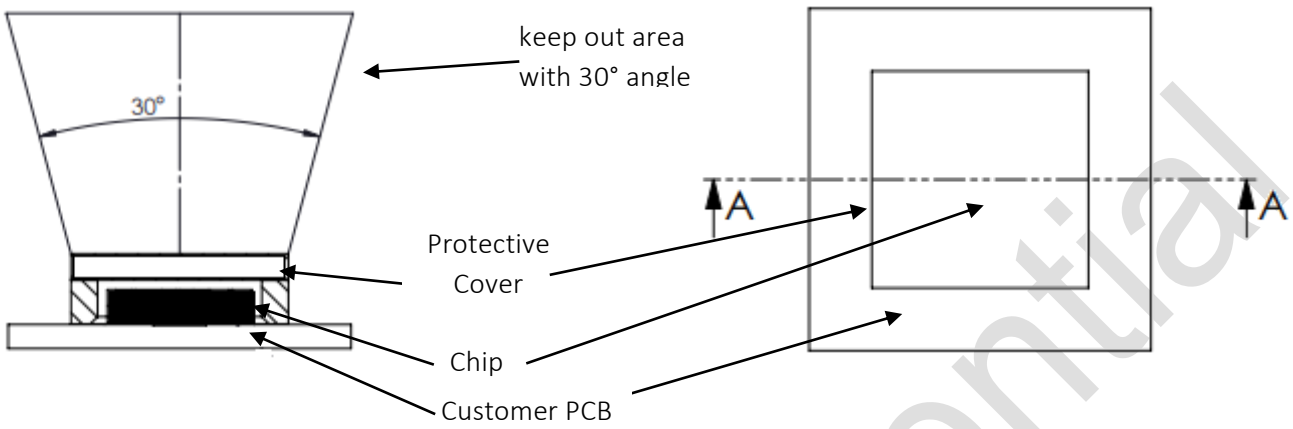


Figure 15. Side View and Top View of Keep Out Area

4.5 Recommended Protective Cover Characteristic and Design

For optimum performance of PAT9136E1-TXQT when used with protective cover, below are guidelines on the design and characteristics of the protective cover.

4.5.1 Recommended Operating Condition

Table 8. Recommended Operating Condition

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Z_GAP (Cover Bottom to top of the chip)	Z_{GAP}			0.7	mm	Measured from bottom of cover to chip top surface

4.5.2 Protective Cover Characteristics

- Based on the operating principle of the chip, the wavelength range of 800 to 900 nm is critical to the chip's performance. As such, the recommended protective cover material is double sided AR coating with transmissivity of >97% over wavelength of 800 to 900nm.
- Protective cover holder below is used to hold the protective cover which can be custom made per customer's requirement
- Both sides of the cover are coated with anti-reflective material.
- Recommended thickness for the cover is 1.1±0.1mm and placed above the chip as below:

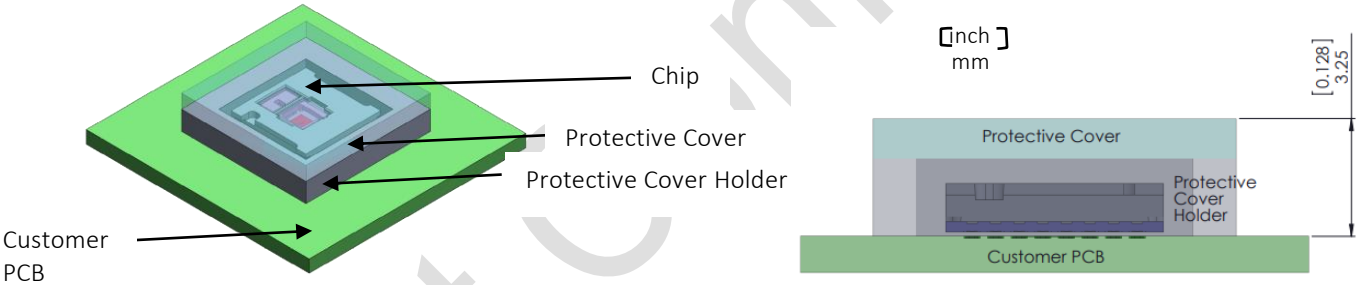
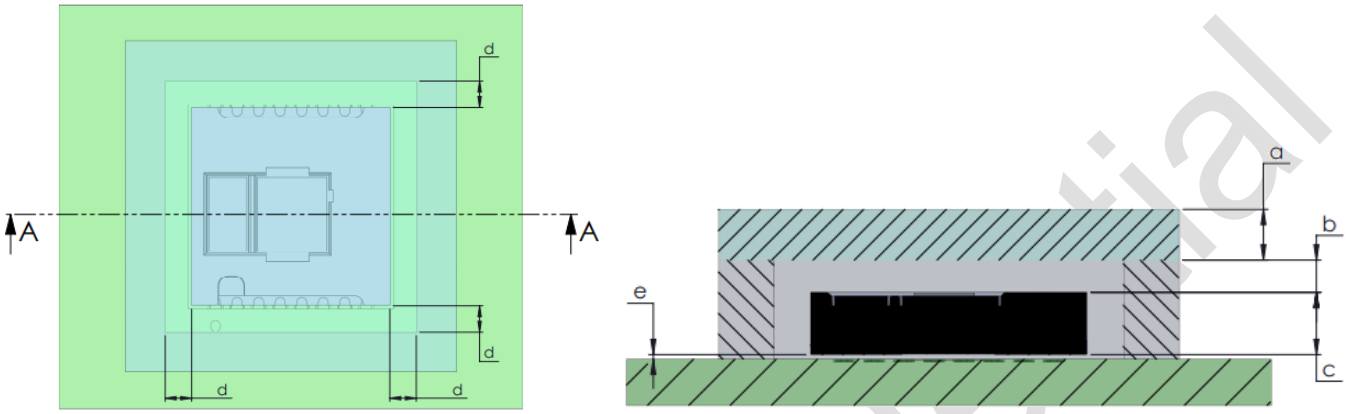


Figure 16. Chip with Flat Cover and Side View

4.5.3 Recommended Protective Cover Design

Cross-sectional view in Figure 17 below shows the recommended protective cover design, which is with the cover sitting above the chip (example below is with maximum Z_{GAP} of 0.7mm). Dimensions d (gaps between chip and cover holder) just need to be larger than the chip when mounted on the customer PCB.



	Dimension	Value
a.	Cover Thickness	1.10mm
b.	Z_{GAP} between chip and cover	0.70mm
c.	Chip Thickness	1.35mm
d.	X/Y gap between chip and cover holder	> 0mm
e.	Chip solder thickness	0.10mm

Figure 17. Cross-sectional View A-A

4.6 Assembly Guide

4.6.1 Handling Precaution of Moisture Sensitivity During Assembly Processes

This product is classified as moisture sensitivity device at Level 3 (MSL 3). Thus, the following moisture sensitive precaution and handling steps are required during the Assembly processes.

Storage Control of Unopened box/ Seal bag

This product is shipped in a vacuum sealed Moisture Barrier bag (MBB) together with desiccant and a moisture indicator card inside.

The shelf life in the unopened sealed bag is 12 months at storage condition of < 40°C/90% relative humidity (RH). It is advised that the vacuum sealed MBB only be opened at the START of assembly process.

Control of Opened Seal bag

After the vacuum sealed MBB is opened, the product MUST be subjected to reflow solder and PCB mounting within 168 hours of the factory condition < 30°C/60% RH.

Control of Un-reflow Units

Any balance of un-reflow units need to be sealed back to the MBB with desiccant at < 5% RH.

The product requires Baking, before mounting, if the following conditions happen:

- Assembly floor life exceeded 168 hours after the sealed MBB is opened.
- Humidity Indicator Card (HIC) is > 10% when read at 23°C ± 5°C.

Recommended Baking condition is 125°C ± 10°C for 48 hours. Refer to IPC/JEDEC J-STD-033 for Baking procedures.

Note: The shipping Tube cannot be subjected to high temperature baking. Transfer to an appropriate container for baking.

4.6.2 Assembly Recommendation

For surface mount the chip and all other components onto PCB:

1. Reflow the entire assembly in a no-wash solder process.

   Note: Recommended to generate a stencil for the reflow process.

2. Remove the protective Kapton tape on top of the chip's package, which is meant to protect the cover glass in Figure 4. from contamination.

   Note: After the Kapton tape is removed, please take note to keep the cover glass (on the top of the chip's package) from contamination.

4.6.3 ESD Precaution

This chip is a sensitive device, ESD awareness is mandatory to prevent premature damage during handling.

Below are recommended procedures to prevent electrostatic discharge towards semiconductor devices:

- Equalize potentials of terminals during transportation or storage.
- Equalize the potentials of all electronic devices, work station, and operator's body that may have possible contact with the chip.
- Ensure maintaining an ESD free environment at all times. For example, maintain relative humidity in the work area to around 50%.

Operator

- Operators must wear wrist straps in contact with bare skin.
- Wear cotton or anti-static treated materials, clothing and gloves.
- Wear conductive shoes whenever a conductive mat is used.
- Do not touch the pins, hold the body of the chip instead.

Equipment and Tools

- Any electrical equipment and tool placed on the workbench must be isolated from the work bench's surface, and need to be grounded properly.
- Conductive mat (or conductive material) must be used on workbench's surface. These conductive materials must be grounded with a 1 MΩ resistor.

Transportation, Storage and Packing

- Use conductive or anti-static shielding bags to store chips.

Soldering Operation

- Use a soldering iron with a grounding wire.
- During manual soldering operation, the operator must wear wrist straps.
- Do not use the solder removal pump when detaching the chip from PCB. Use solder wick or equivalent tools.

4.6.4 IR Reflow Soldering Profile

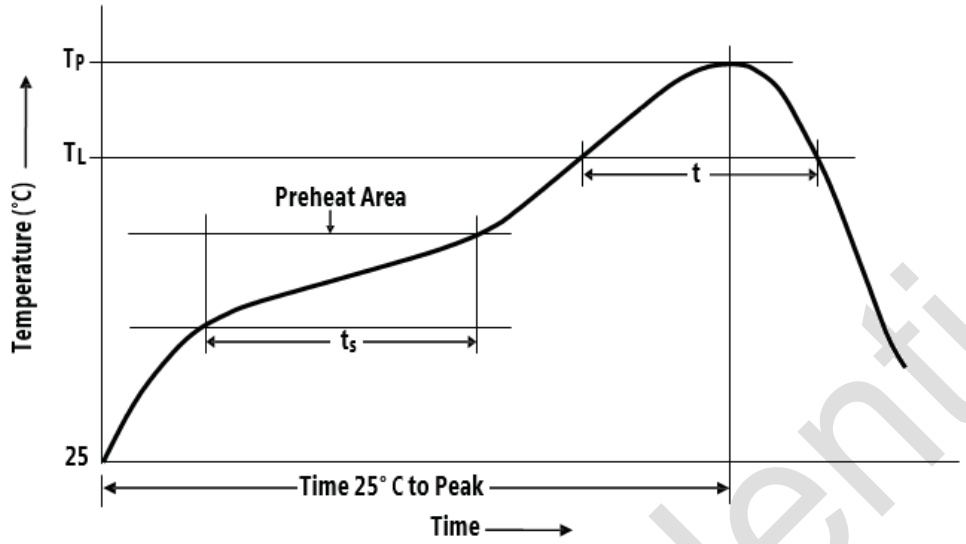


Figure 18. Solder Reflow Profile

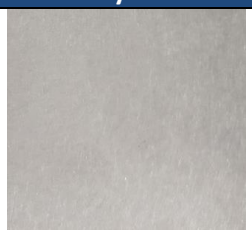
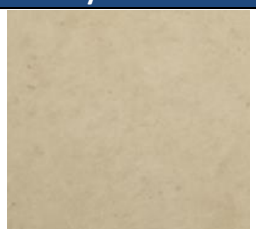
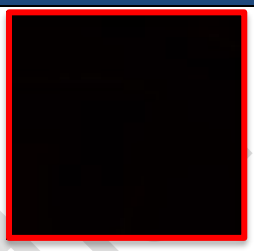
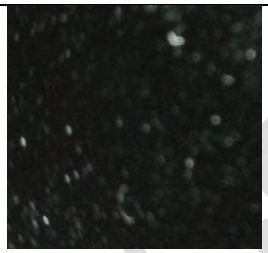
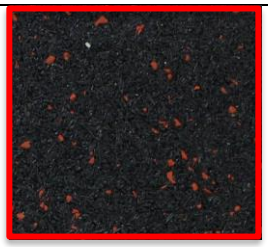
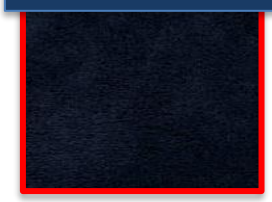
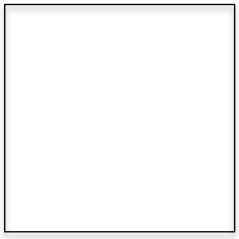
Table 9. Soldering Profile

Parameter	Specification
Max. Rising Slope	0° to 3°C/sec
Preheat Duration (150 – 190°C), t_s	60 to 120 sec
Time above Reflow (T_L = 220°C), t	30 to 60 sec
Peak Temperature, T_p	230 to 260°C

Note: T_L is the Melting Temperature

4.7 Surface Coverage

While the chip can track on a variety of common surfaces such as glossy metal, glossy non-metal and tiles, there are some challenges to track on dark, absorptive, and very rough surfaces (highlighted in red below), where tracking performance or working range may be impacted. Refer to below figure for examples of the surfaces mentioned.

Glossy Metal	Glossy Non-Metal	Wood	Others
 Aluminum	 Glossy Gypsum Flooring	 Laminated Wood	 Dark Absorptive Art Paper
 Glossy Stainless Steel	 Glossy Grey Vinyl Flooring	 Light Brown Wood	 Very Rough Tiles
 Black Painted Metal	 Dark Granite	 Dark Plywood	 Dark Absoptive Rubber Mat (with or without Color Spots)
	 Glossy Photo Paper	Carpet  Black Carpet	 Rough Vinyl Flooring (Wood Pattern)
	 Green ESD Mat	 Crimson Carpet	 Diffuse A4 Paper

5.0 Power Management

5.1 Power Supply

The chip has a total of three Power Supply input (VDD, VDDIO and VDD_VCSEL). VDD is the main power supply. VDDIO is the supply for I/O reference voltage. VDD_VCSEL is the power supply to the VCSEL.

5.2 Power Sequence

5.2.1 Power On

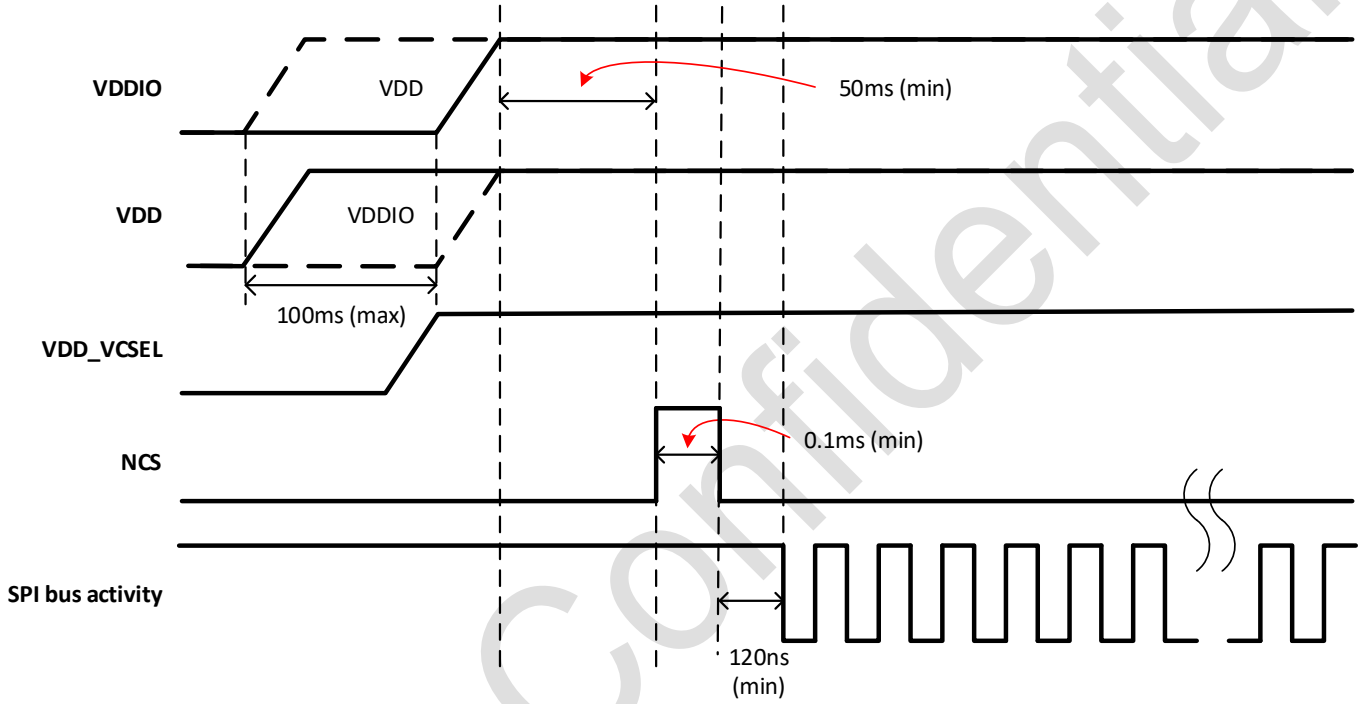


Figure 19. Power-on Sequence Requirement

The appropriate sequence is as below:

1. Apply power to VDD and VDDIO in any order, with a maximum of 100ms delay in between each supply. VDD_VCSEL should be powered up together with the second power supply (VDD or VDDIO, depending on whether VDD or VDDIO is powered up first).
2. Wait for at least 50 ms.
3. Drive NCS to high state at least for 0.1ms to reset the SPI port[1]. The SPI port is always in a reset state whenever NCS is held high.
4. SPI bus activity can be executed after asserting NCS by driving NCS to low state and wait for a minimum 120 ns.
5. Write 0x5A to register 0x3A (Power_Up_Reset) or alternatively toggle NRST pin for >20us for hardware reset.

Note:

1. skip step 3 if NCS is already at high state.

Refer to Section 7.1.2 Performance Optimization Setting to configure the required registers to achieve optimum performance of the chip.

5.2.2 Power Off

It is recommended to power off VDD, VDD_VCSEL and VDDIO at the same time.

5.3 Power State

5.3.1 State Description

Table 10. Power State Description

State	Description
OFF	No power supply, all the voltage rails and clocks are gated.
Run	▪ Upon powered on, the chip enters Ready state mainly for loading the initial and customized chip parameter settings. The chip will not be activated until host command is fully executed. ▪ The chip enters Run state upon receiving the host commands to load its required setting. This is the state where the chip executes and deliver the required data according to the host command.
Shutdown	The chip enters this state for power saving purpose upon receiving Shutdown command.

5.3.2 State Diagram

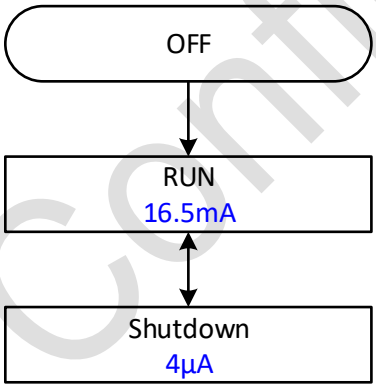


Figure 20. State Diagram

5.3.3 State Transition

Table 11. State Transition

State	Control Type	Description
OFF to Run	Power up	After power up the chip, the SPI interface will be ready in 50ms. Upon SPI interface is ready, initialize the chip by loading the performance optimization settings (refer to Section 7.1.2 for more details) from the host. When initialization is completed, the chip enters Run state automatically.
Run to Shutdown	Command	Shutdown of the chip can be achieved by Write 0xB6 to register 0x3B (Shutdown) to set the chip to Shutdown state. NCS pin is recommended to be pulled to high state during Shutdown.
Shutdown to Run	Command	To wake up from Shutdown state, write 0x5A to register 0x3A (Power_Up_Reset) through SPI interface. Initialize the chip by loading the initial settings (refer to Section 7.1.2 for more details) from the host. When the chip initialization is completed, it enters Run State automatically.

5.4 Reset and Shutdown State

There are three approaches to trigger chip reset. All previous registers value will be cleared after each reset.

Table 12. State of Signal Pins during Reset and After Reset

State of Signal Pins after VDD & VDDIO are valid		
Pin	**During Reset**	**After Reset**
NRST	Functional	Functional
NCS	Ignored	Functional
MISO	Undefined	Depends on NCS
SCLK	Ignored	Depends on NCS
MOSI	Ignored	Depends on NCS
MOTION	Undefined	Functional

The table below shows the state of the various pins during Shutdown.

Table 13. State of Signal Pins during Shutdown

Pin	Status during Shutdown State
NRST	High
NCS	High
MISO	Hi-Z
SCLK	Ignore if NCS = 1
MOSI	Ignore if NCS = 1
MOTION	High

5.4.1 Power-on Reset

During power-on, the chip performs power-on reset. Refer to Section 2.2 for power supply specification detail to ensure power on reset is successful.

5.4.2 Hardware Reset

The NRST pin can be used to perform a complete chip reset. When the NRST pin is asserted, it performs the same function as the Power_Up_Reset register. The NRST pin needs to be asserted (held to logic 0) for at least 20µs. The NRST pin cannot be left floating or unconnected.

5.4.3 Software Reset

The chip can also be reset by writing value 0x5A to register 0x3A (Power_Up_Reset). Upon a software reset being executed, all register settings in Section 7.1.2 must be reloaded according to the selected Option.

Upon a software reset is executed, the host must wait for at least 120ms for next valid motion.

5.5 Related Register

Usage	Name	Bank	Address
Enter Shutdown state	Shutdown	0	0x3B
Exit Shutdown state and reset	Power_Up_Reset	0	0x3A

6.0 Serial Port Interface Communication

6.1 Signal Description

The 4-wire synchronous serial port interface is used to write or read registers in the chip. The host is a SPI master device where it drives SCLK, MOSI, and NCS (active low) to initiate the communication. The interface supports single or multi-chip (slaves) with NCS control.

Table 14. 4-Wire SPI Signal Description

Pin	Description
SCLK	Clock input, generated by the master (host).
MOSI	Input data (Master Out / Slave In).
MISO	Output data (Master In / Slave Out).
NCS	Chip select input (active low).

6.2 Chip Select Operation

The serial port is activated after NCS is asserted. If NCS is de-asserted during a transaction, the entire transaction is aborted and the serial port will be reset. After a transaction is aborted, the host needs to follow the normal address-to-data or transaction-to-transaction delay timing requirement before beginning the next transaction.

When the NCS pin is high, the SPI's inputs are ignored and the SPI's output are in tri-state. NCS can also be used to reset the serial port communication in case of an error occur.

To improve communication reliability, all serial transactions should be framed by NCS assertion. The port should not be remained enabled when not in use to prevent misinterpret ESD and EFT/B events and put the chip into an unknown state.

6.3 Protocol

The transmission protocol is a 4-wire link, half duplex protocol between the host and the chip. All data changes at SCLK falling edge and latched at SCLK rising edge. The host controller always initiates communication and the chip never initiates data transfers.

The transmission protocol consists of the two type operations:

- Write Operation
- Read Operation

Both of the two operation modes consist of two bytes. The first byte contains the register address (seven bits) and bit [7] as MSB to indicate data direction. The second byte contains the data.

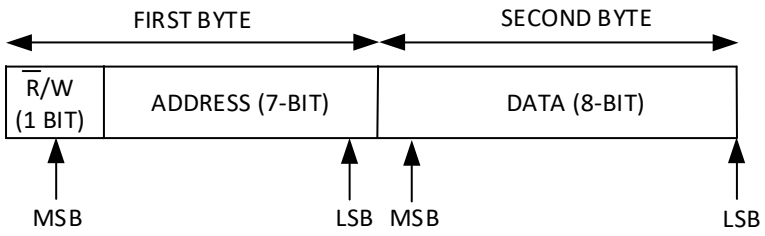


Figure 21. Transmission Protocol

6.4 Write Operation

Write operation, defined as data going from the micro-controller to the chip, is always initiated by the host and consists of two bytes. The first byte contains the address (7-bit) and has a "1" as its MSB to indicate data direction. The second byte contains the data. The chip reads MOSI on rising edges of SCLK.

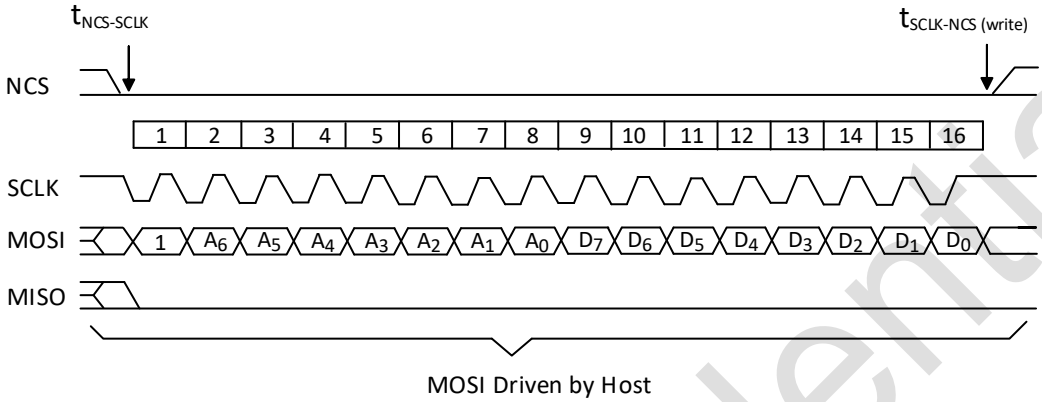


Figure 22. Write Operation

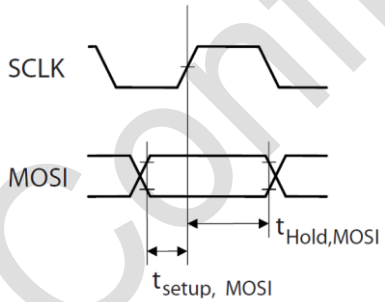


Figure 23. MOSI Setup and Hold Time

6.5 Read Operation

A read operation, defined as data going from the chip to the micro-controller, is always initiated by the host and consists of two bytes. The first byte contains the address, is sent by the host over MOSI, and has a "0" as its MSB to indicate data direction. The second byte contains the data and is driven by the chip over MISO. The chip outputs MISO bits on falling edges of SCLK and samples MOSI bits on every rising edge of SCLK.

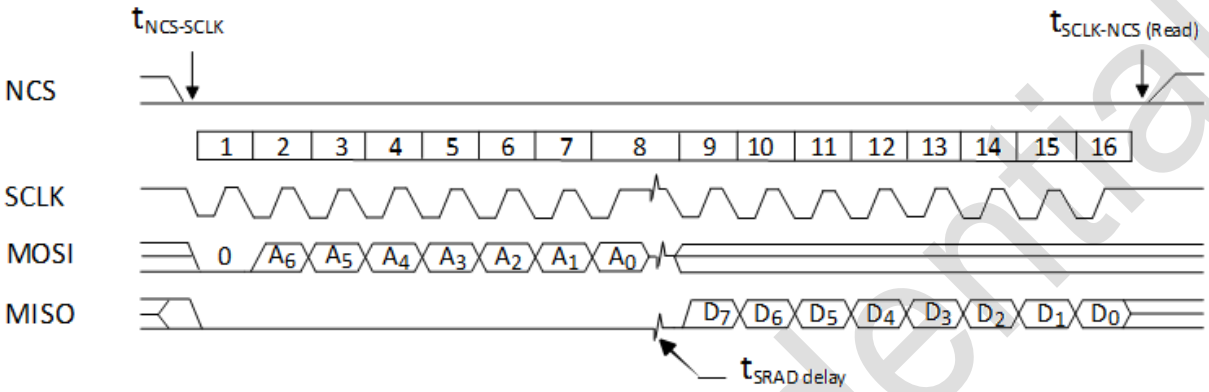


Figure 24. Read Operation

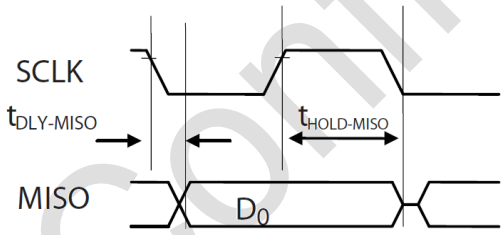


Figure 25. MISO Delay and Hold Time

Note: The minimum high state of SCLK is also the minimum MISO data hold time of the chip. Since the falling edge of SCLK is the start of the next read or write command, the chip will hold the state of data on MISO until the falling edge of SCLK.

6.6 Burst Mode

Burst read is a special serial port interface operation mode which can be used to reduce the serial transaction time for Motion Read. The speed improvement is achieved by continuous data clocking to read multiple registers with a single dedicated address and not requiring the delay period between data bytes. Refer to section 7.2.2 for the detail.

NCS must be de-asserted to terminate burst mode after each burst read operation transaction is completed. However, the host can terminate the Burst Read operation as needed through de-assert the NCS.

After sending the register address, the host wait for t_{SRAD}, and then begin reading data. All data bits can be read with no delay between bytes by driving SCLK at the normal rate. The data are latched into the output buffer after the last address bit is received. After the burst transmission is complete, the host must raise the NCS line for at least t_{BEXIT} to terminate burst read operation. The serial port is not available for use until it is reset with NCS (asserted), even for a second burst transmission.

Procedure to start motion burst:

1. Pull NCS low.
2. Wait for $t_{NCS-SCLK.}$
3. Send register 0x16 (Motion_Burst). After sending this address, MOSI remain either hold high or low until the burst transmission is complete.
4. Wait for $t_{SRAD.}$
5. Start reading SPI data continuously up to 12bytes. Motion burst is terminated by pulling NCS high for at least t_{BEXIT}.
6. To read new motion burst data, repeat from step 2.
7. If a non-burst register read operation is executed; then, to read new burst data, start from step 1 instead.

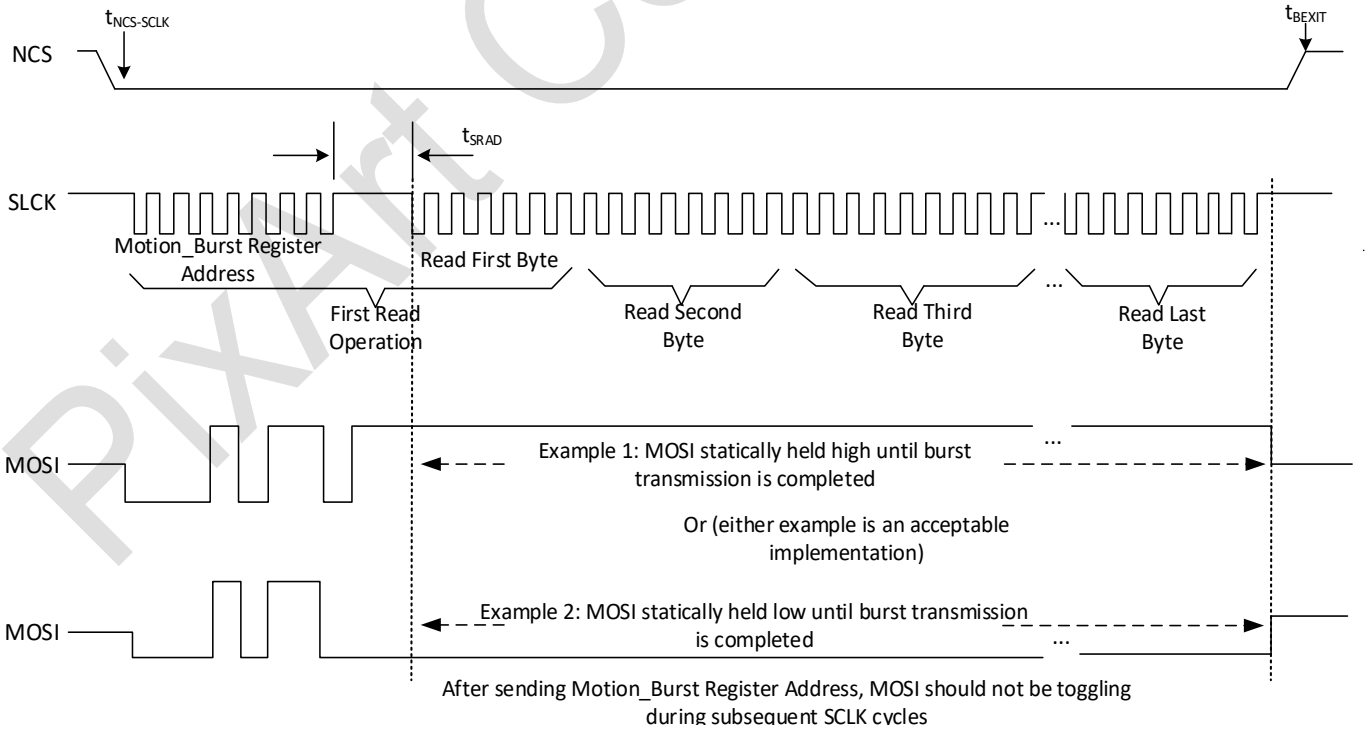


Figure 26. Burst Read Timing

6.7 Required Timing Between Read and Write Commands (t_{SXX})

There are minimum timing requirements between read and write commands on the serial port.

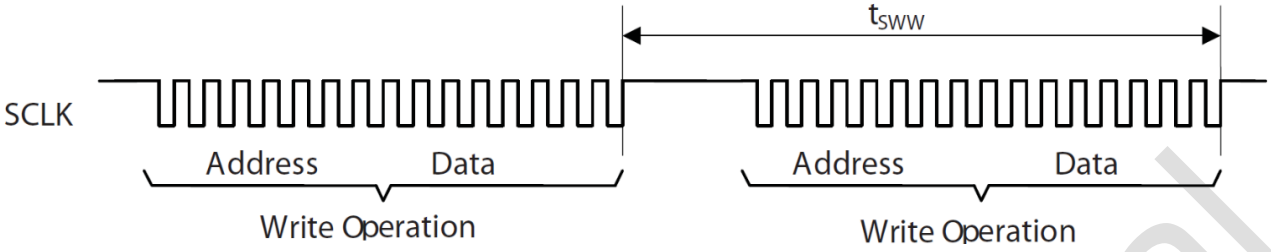


Figure 27. Timing Between Two Write Commands

If the rising edge of the SCLK for the last data bit of the second write command occurs before the t_{SWW} delay, then the first write command may not complete correctly.

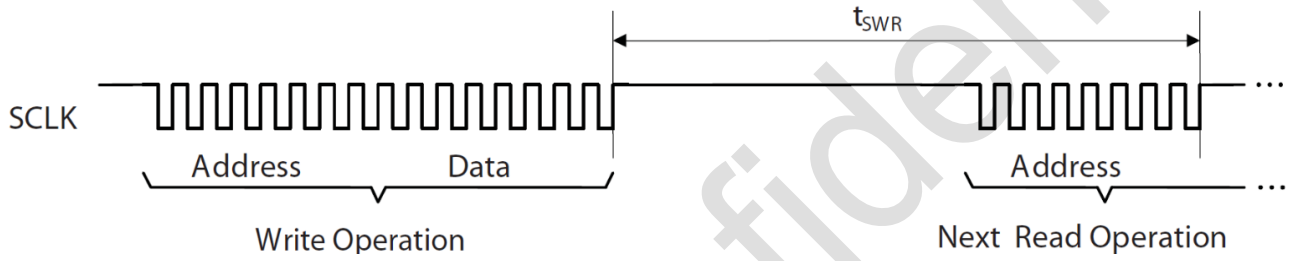


Figure 28. Timing Between Write and Read Commands

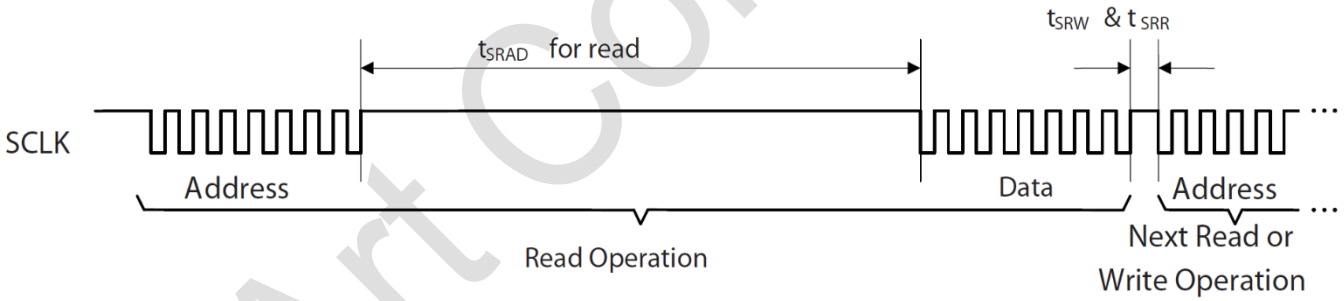


Figure 29. Timing Between Read and Either Write or Subsequent Read Commands

If the rising edge of SCLK for the last address bit of the read command occurs before the t_{SWR} required delay, the write command may not complete correctly. During a read operation, SCLK should be delayed at least t_{SRAD} after the last address data bit to ensure that the chip has time to prepare the requested data.

The falling edge of SCLK for the first address bit of either the read or write command must be at least t_{SRR} or t_{SRW} after the last SCLK rising edge of the last data bit of the previous read operation.

7.0 System Control

7.1 System Initialization

The chip is required to follow the system initialization flow to load setting for optimal performance. The initial flow consists of initial setting and performance optimization setting.

The expected resolution is governed by the values set to the Resolution registers. By default, upon powering-up and initialization of the register settings (per Section 7.1.2), the resolution is set to 2000 cpi (787 count/cm). To set the chip to other resolution value, please refer to register 0x47 to 0x4B.

7.1.1 Initialization Flow

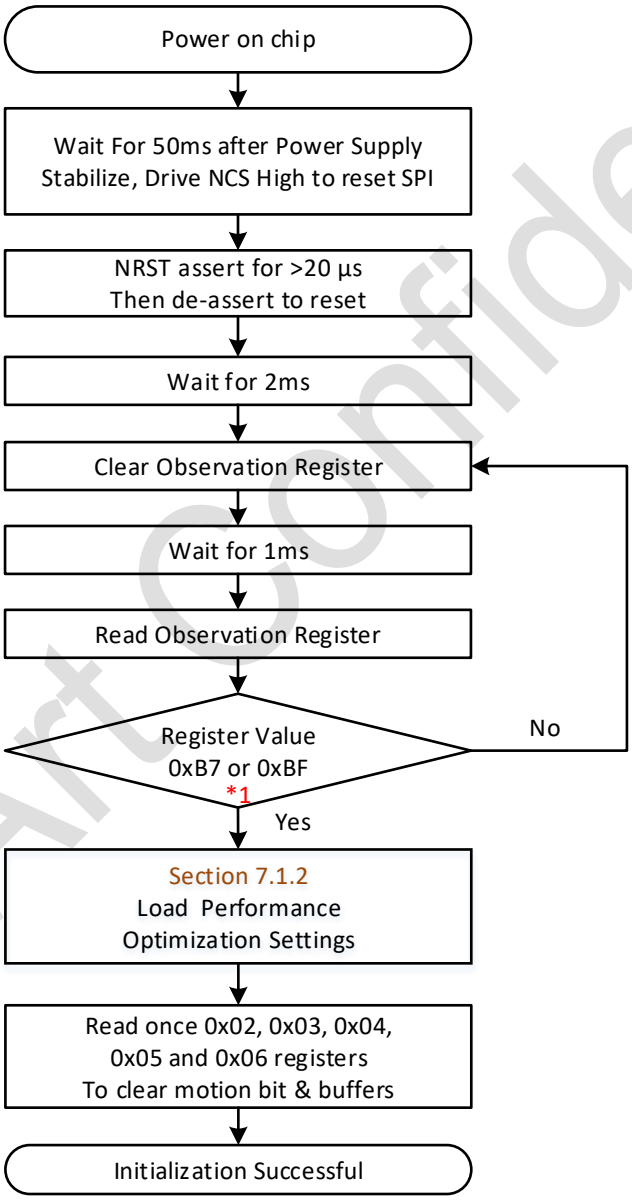


Figure 30. Initialization Flow

Note:

*1: If unable to read the correct value for Observation Register, it is recommended to power off and power on the chip again. If the problem persists, do check the SPI interface connection and settings.

7.1.2 Performance Optimization Setting

Step in sequence as follow:

1. Write register 0x3A with value 0x5A
2. Write register 0x7F with value 0x00
3. Write register 0x40 with value 0x80
4. Write register 0x7F with value 0x14
5. Write register 0x4D with value 0x00
6. Write register 0x53 with value 0x0D
7. Write register 0x4B with value 0x20
8. Write register 0x42 with value 0xBC
9. Write register 0x43 with value 0x74
10. Write register 0x58 with value 0x4C
11. Write register 0x79 with value 0x00
12. Write register 0x7F with value 0x0E
13. Write register 0x54 with value 0x04
14. Write register 0x7F with value 0x0E
15. Write register 0x55 with value 0x0D
16. Write register 0x58 with value 0xD5
17. Write register 0x56 with value 0xFB
18. Write register 0x57 with value 0xEB
19. Write register 0x7F with value 0x15
20. Read register 0x58

    If register 0x58 Bit [7] = 0

    a. Write register 0x58 with value 0x04
    b. Write register 0x57 with value 0x80
    c. Continue to Step 21

    If register 0x58 Bit [7] = 1

    a. Write register 0x58 with value 0x84
    b. Write register 0x57 with value 0x00
    c. Continue to Step 21
21. Write register 0x7F with value 0x07
22. Write register 0x40 with value 0x43
23. Write register 0x7F with value 0x13
24. Write register 0x49 with value 0x20
25. Write register 0x7F with value 0x14
26. Write register 0x54 with value 0x02
27. Write register 0x7F with value 0x15
28. Write register 0x60 with value 0x00
29. Write register 0x7F with value 0x06
30. Write register 0x74 with value 0x50
31. Write register 0x7B with value 0x02
32. Write register 0x7F with value 0x00
33. Write register 0x64 with value 0x74
34. Write register 0x65 with value 0x03
35. Write register 0x72 with value 0x0E
36. Write register 0x73 with value 0x00
37. Write register 0x7F with value 0x14
38. Write register 0x61 with value 0x3E
39. Write register 0x62 with value 0x1E
40. Write register 0x63 with value 0x1E
41. Write register 0x7F with value 0x15
42. Write register 0x69 with value 0x1E
43. Write register 0x7F with value 0x07
44. Write register 0x40 with value 0x40
45. Write register 0x7F with value 0x00
46. Write register 0x61 with value 0x00
47. Write register 0x7F with value 0x15
48. Write register 0x63 with value 0x00
49. Write register 0x62 with value 0x00
50. Write register 0x7F with value 0x00
51. Write register 0x61 with value 0xAD
52. Write register 0x7F with value 0x15
53. Write register 0x5D with value 0x2C
54. Write register 0x5E with value 0xC4
55. Delay for 100ms
56. Write register 0x5D with value 0x04
57. Write register 0x5E with value 0xEC
58. Write register 0x7F with value 0x05
59. Write register 0x42 with value 0x48
60. Write register 0x43 with value 0xE7
61. Write register 0x7F with value 0x06
62. Write register 0x71 with value 0x03
63. Write register 0x7F with value 0x09
64. Write register 0x60 with value 0x1C
65. Write register 0x61 with value 0x1E
66. Write register 0x62 with value 0x02
67. Write register 0x63 with value 0x04
68. Write register 0x64 with value 0x1E
69. Write register 0x65 with value 0x1F
70. Write register 0x66 with value 0x01

71. Write register 0x67 with value 0x02
72. Write register 0x68 with value 0x02
73. Write register 0x69 with value 0x01
74. Write register 0x6A with value 0x1F
75. Write register 0x6B with value 0x1E
76. Write register 0x6C with value 0x04
77. Write register 0x6D with value 0x02
78. Write register 0x6E with value 0x1E
79. Write register 0x6F with value 0x1C
80. Write register 0x7F with value 0x05
81. Write register 0x45 with value 0x94
82. Write register 0x45 with value 0x14
83. Write register 0x44 with value 0x45
84. Write register 0x45 with value 0x17
85. Write register 0x7F with value 0x09
86. Write register 0x47 with value 0x4F
87. Write register 0x4F with value 0x00
88. Write register 0x52 with value 0x04
89. Write register 0x7F with value 0x0C
90. Write register 0x4E with value 0x00
91. Write register 0x5B with value 0x00
92. Write register 0x7F with value 0x0D
93. Write register 0x71 with value 0x92
94. Write register 0x70 with value 0x07
95. Write register 0x73 with value 0x92
96. Write register 0x72 with value 0x07
97. Write register 0x7F with value 0x00
98. Write register 0x5B with value 0x20
99. Write register 0x48 with value 0x13
100. Write register 0x49 with value 0x00
101. Write register 0x4A with value 0x13
102. Write register 0x4B with value 0x00
103. Write register 0x47 with value 0x01
104. Write register 0x54 with value 0x55
105. Write register 0x5A with value 0x50
106. Write register 0x66 with value 0x03
107. Write register 0x67 with value 0x00
108. Write register 0x7F with value 0x07
109. Write register 0x40 with value 0x43
110. Write register 0x7F with value 0x05
111. Write register 0x4D with value 0x00
112. Write register 0x6D with value 0x96
113. Write register 0x55 with value 0x62
114. Write register 0x59 with value 0x21
115. Write register 0x5F with value 0xD8
116. Write register 0x6A with value 0x22
117. Write register 0x7F with value 0x07
118. Write register 0x42 with value 0x30
119. Write register 0x43 with value 0x00
120. Write register 0x7F with value 0x06
121. Write register 0x4C with value 0x01
122. Write register 0x54 with value 0x02
123. Write register 0x62 with value 0x01
124. Write register 0x7F with value 0x09
125. Write register 0x41 with value 0x01
126. Write register 0x4F with value 0x00
127. Write register 0x7F with value 0x0A
128. Write register 0x4C with value 0x18
129. Write register 0x51 with value 0x8F
130. Write register 0x7F with value 0x07
131. Write register 0x40 with value 0x40
132. Write register 0x7F with value 0x00
133. Write register 0x40 with value 0x80
134. Write register 0x7f with value 0x09
135. Write register 0x40 with value 0x03
136. Write register 0x44 with value 0x08
137. Write register 0x4f with value 0x08
138. Write register 0x7f with value 0x0A
139. Write register 0x51 with value 0x8E
140. Write register 0x7f with value 0x00
141. Write register 0x66 with value 0x11
142. Write register 0x67 with value 0x08

7.1.3 Matte Textured Surface Performance Improvement Setting

This is an optional setting dedicated for Matte Textured Surface. Load below register settings after the regular Initial Setting is completed.

1. Write register 0x7F with value 0x05.
2. Write register 0x4d with value 0x01.
3. Write register 0x7f with value 0x06.
4. Write register 0x54 with value 0x01.
5. Write register 0x62 with value 0x01.
6. Write register 0x7f with value 0x00.

7.2 Register Access

The host can access register through SPI interface. Refer to Section 6.0 for detail.

7.2.1 Register Address Mapping

The chip has two type of register assignment. They are register bank and register address mapping. Each register bank consists of 7 bits width address mapping (0x00 to 0x7F).

7.2.2 Burst Read

Burst read operation is a special serial port interface operation mode which is used to reduce the serial transaction time for motion read. The speed improvement is achieved by continuous data clocking from the host for multiple registers read without further specify the register address. In the burst read operation, NCS must be remained asserted until burst mode transaction is fully completed.

Note: A single read of any motion related registers (0x02 to 0x06) should be avoided during burst mode.

Reading the *Motion_Burst* register activates Burst Mode. The chip will respond with the following motion burst report in order.

BYTE [00]= Motion
BYTE [01]= Observation
BYTE [02]= Delta_X_L
BYTE [03]= Delta_X_H
BYTE [04]= Delta_Y_L
BYTE [05]= Delta_Y_H
BYTE [06]= SQUAL
BYTE [07]= RawData_Sum
BYTE [08]= Maximum_RawData
BYTE [09]= Minimum_RawData
BYTE [10]= Shutter_Upper
BYTE [11]= Shutter_Lower

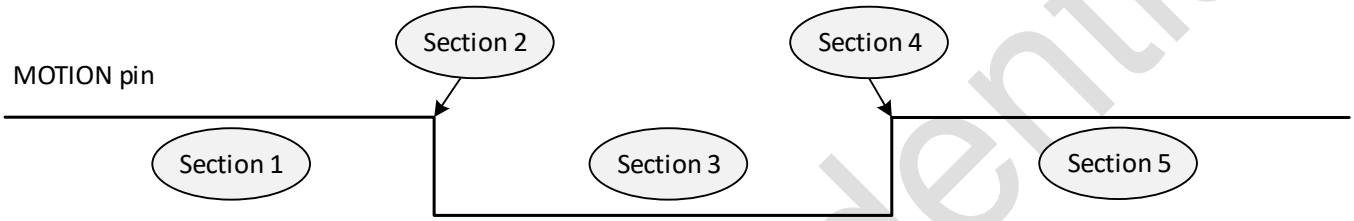
7.3 Output

7.3.1 Motion Bit and Motion Pin Interrupt

The motion bit in register 0x02 (Motion) is an indicator flag for motion detection. Prior reading motion data registers, the host must check motion bit in register 0x02 (Motion). Motion bit will be updated as 1 if the motion data in the motion registers are available.

The motion pin is an interrupt (active low) pin that triggers the host when motion has occurred. The MOTION pin goes low whenever the motion bit in register 0x02 (Motion) is "1".

Note: No pull-up resistor is required at the MOTION pin or at the host side to reduce power when motion pin is in low state.



Section 1 : No motion detected, motion data are invalid. Motion bit=0 and motion pin de-asserted.
Section 2 : When motion detected, motion pin is asserted, motion bit=1 and motion data accumulation begins.
Section 3 : Motion data accumulation in progress and wait for host to access.
Section 4 : Upon motion data register is accessed, motion bit=0, interrupt pin is de-asserted and motion data registers are automatic cleared.
Section 5 : No motion detected, motion data are invalid. Motion bit=0 and motion pin de-asserted.

Figure 31. Motion Interrupt Pin Function

7.3.2 Output Access

The accumulated motion data are stored in Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H registers. The data can be accessed through single or burst read operation as needed.

Single read access the motion data by using normal read operation when the data in register Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H are available. Burst mode operation is a special serial port operation mode which is used to reduce the serial transaction time for motion read, do refer to Section 7.2.2 for the detail.

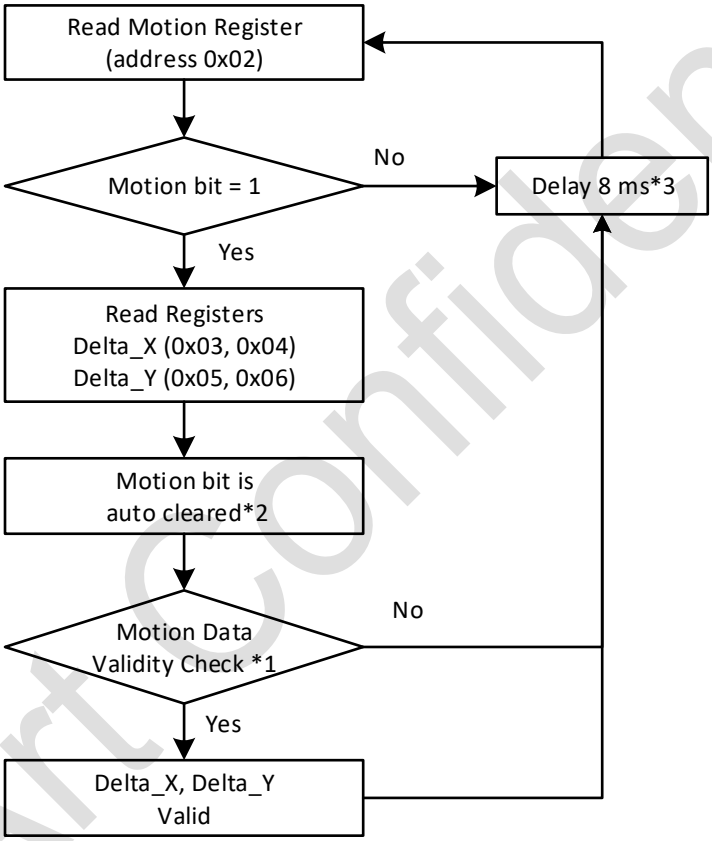
There are two methods to access the motion data:

- Polling method
- Interrupt method

- Polling Method

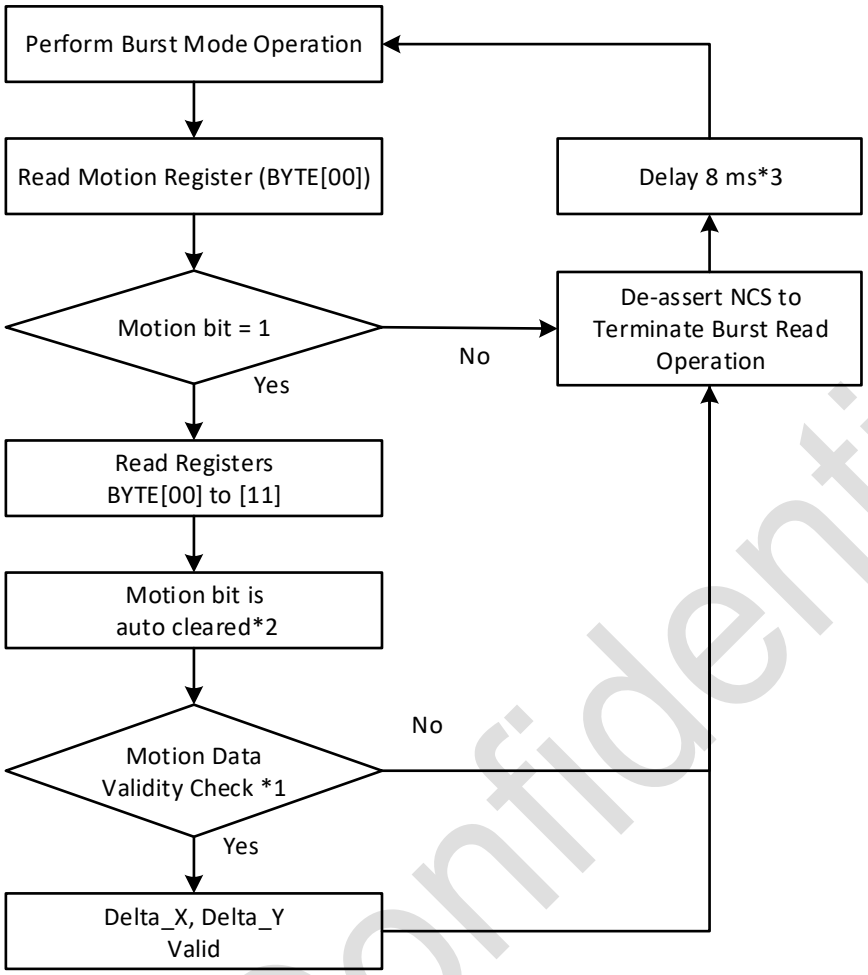
The motion bit in register 0x02 (Motion) is an output that signals the host when motion has occurred. The motion bit turns to “1" whenever the motion is detected; in other words, whenever there is non-zero data in the Delta_X_L, Delta_X_H, Delta_Y_L or Delta_Y_H registers. Motion bit is cleared to “0” by reading or writing to MOTION register.

By reading and checking Motion register periodically, the host can get the motion data through SPI interface. This register enables the user to determine if new motion event has occurred since the previous motion data has been accessed. If the Motion register bit [7] = 1, the host can read register 0x03, 0x04, 0x05 and 0x06 to get the accumulated motion data.



Note:
*1: Refer to section 7.3.3
*2: Motion bit is auto cleared after reading MOTION register
*3: The polling Interval is configured by the host

Figure 32. Polling Method – Single Read

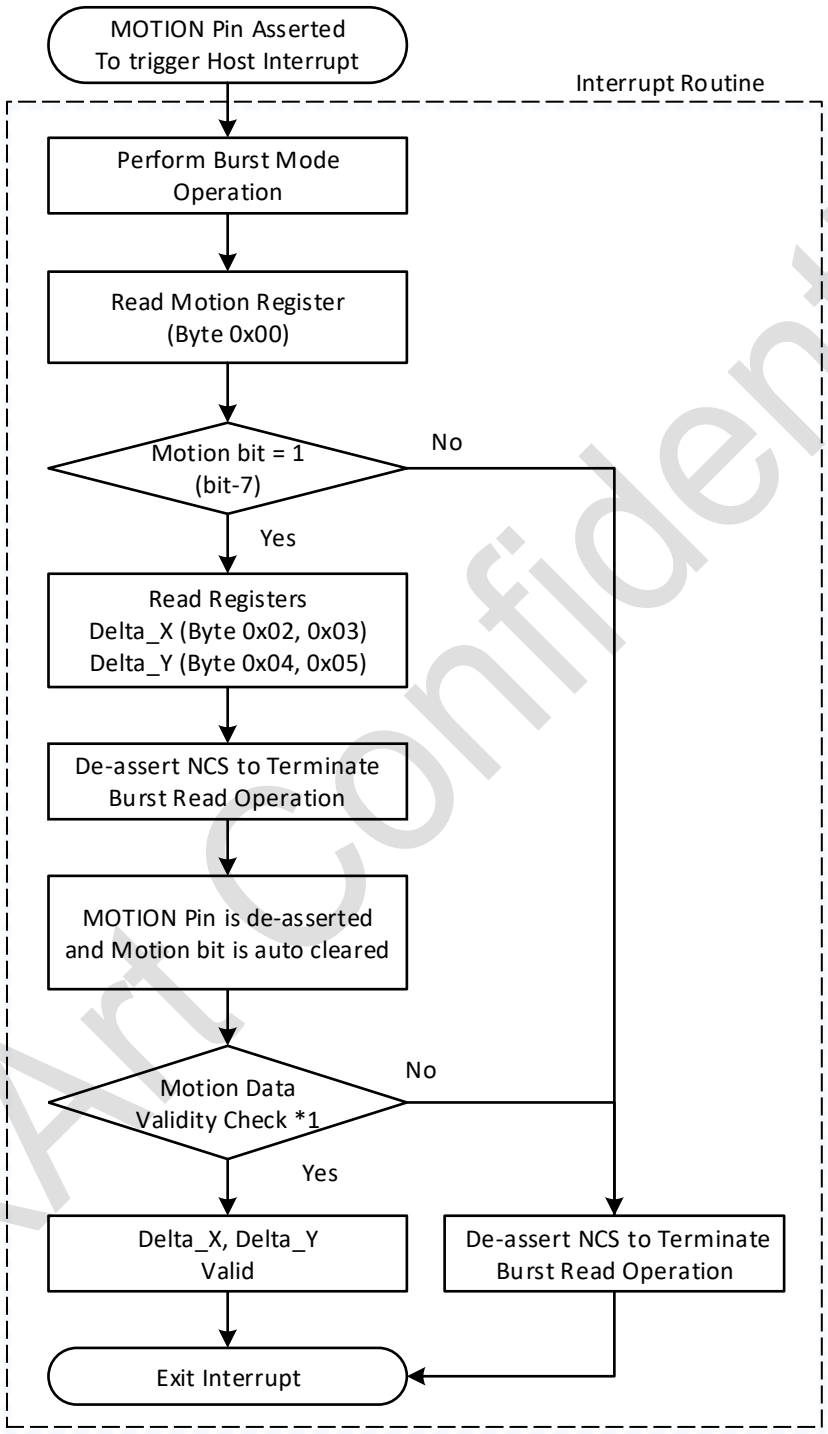


Note:
*1: Refer to section 7.3.3
*2: Motion bit is auto cleared after reading MOTION register
*3:The polling Interval is configured by the host

Figure 33. Polling Method – Burst Read

- Interrupt Method

When MOTION pin is low, the data registers are pending to be accessed by the host. Otherwise, the MOTION pin goes high when the register is cleared. When the chip detects the occurrence of motion, the MOTION pin is asserted and triggers the host to read data.



Note:
*1: Refer to section 7.3.3

Figure 34. Motion Data Access - Interrupt Method

7.3.3 Invalid Motion Data Condition

Additional verification is required to check for validity of the motion data, as detailed below:

Read Observation register bit [6] and bit [7] to check the current operation mode. The read back value should be 0xB7 or 0xBF.

7.3.4 Data Lost and Corruption

Motion data register storage limit is -32768 to 32767 for X-axis and Y-axis respectively. When motion is detected, motion data will be generated, accumulated and stored in registers. If host didn't read out motion data before data reach the limit, the data corruption may occur.

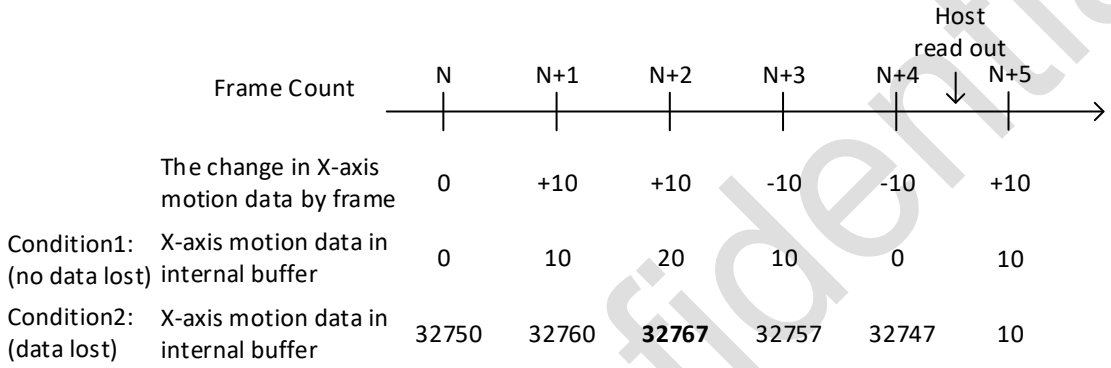


Figure 35. Example of Data Lost When Internal Buffer Reach Limit

From frame N to frame N+4, the total change of motion data is 0.

- Condition1

  If motion data register value is 0 in frame N, the host may read motion data value 0 in between frames N+4 and N+5.

- Condition2

  If motion data register value is 32750 in frame N, the host may read motion data value 32747 in between frames N+4 and N+5.

Above two movement conditions behavior are identical. However, condition 2 register hitting limit of 32767, host read value 32747 instead of 32750 where some motion data are lost.

As prevention,

1. The host requires to response to interrupt triggering as soon as possible for read motion data register.
2. The host need to shorten the polling interval.
3. The host require to monitor and avoid hitting motion data of -32768 to 32767 limit respectively.
4. The chip resolution can be optimized.

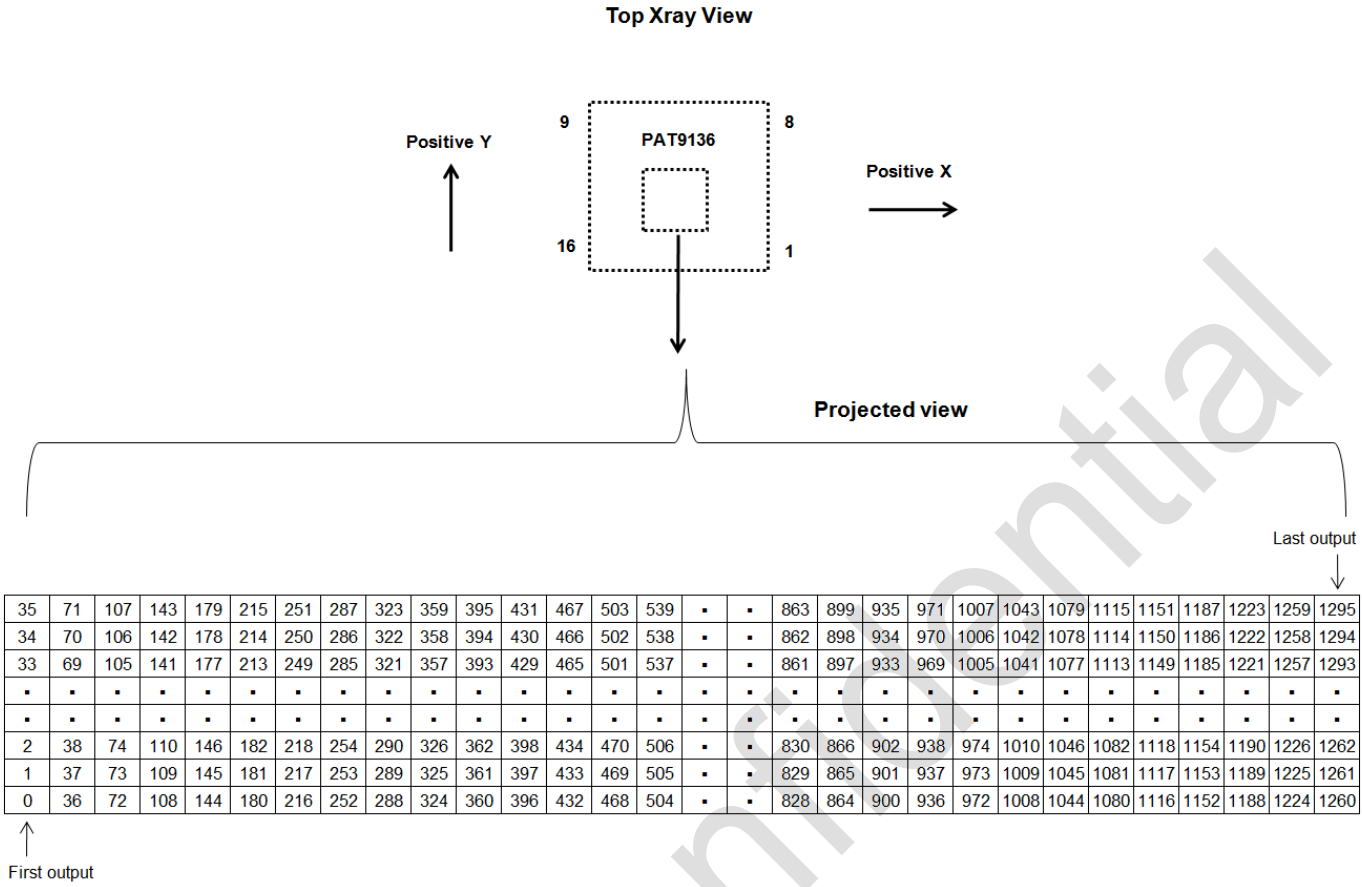
7.3.5 Frame Capture Mode

Frame Capture is the method to download the full array of raw data values using register read operation. This mode disables navigation and no other SPI activity is allowed during this period. A hardware reset is required to exit from the Frame Capture mode.

Power-Up sequence must complete before performing Frame Capture. The device needs to be placed in stationary position during Frame Capture.

Frame Capture procedure is outlined below:

1. Write register 0x7F with value 0x00.
2. Write register 0x55 with value 0x04.
3. Write register 0x50 with value 0x01.
4. Write register 0x40 with value 0x80.
5. Read register 0x02 (Motion) continuously until both bit [1] and bit [0] returns 0.
6. Write register 0x58 with value 0xFF.
7. Poll register 0x59 (RawData_Grab_Status) until both bit [6] and bit [7] are set before proceeding to the next step.
8. Read the first raw data from register 0x58 (RawData_Grab).
9. Poll register 0x59 (RawData_Grab_Status) until bit[7] is set.
10. Read register 0x58 (RawData_Grab) for 7-bits ADC data.
11. Repeat steps (9) and (10) for 1295 times to form a complete array of raw data values.
12. [Optional] To capture another frame, repeat Steps from (1) to (11).
13. To exit Frame Capture mode, perform register write operation as shown below:
    a. Write register 0x40 with value 0x00.
    b. Write register 0x50 with value 0x00.
    c. Write register 0x55 with value 0x00.



35	71	107	143	179	215	251	287	323	359	395	431	467	503	539	▪	▪	863	899	935	971	1007	1043	1079	1115	1151	1187	1223	1259	1295
34	70	106	142	178	214	250	286	322	358	394	430	466	502	538	▪	▪	862	898	934	970	1006	1042	1078	1114	1150	1186	1222	1258	1294
33	69	105	141	177	213	249	285	321	357	393	429	465	501	537	▪	▪	861	897	933	969	1005	1041	1077	1113	1149	1185	1221	1257	1293
▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪
▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪
2	38	74	110	146	182	218	254	290	326	362	398	434	470	506	▪	▪	830	866	902	938	974	1010	1046	1082	1118	1154	1190	1226	1262
1	37	73	109	145	181	217	253	289	325	361	397	433	469	505	▪	▪	829	865	901	937	973	1009	1045	1081	1117	1153	1189	1225	1261
0	36	72	108	144	180	216	252	288	324	360	396	432	468	504	▪	▪	828	864	900	936	972	1008	1044	1080	1116	1152	1188	1224	1260

Figure 36. Raw Data Map

7.4 Related Register

Usage	Name	Bank	Address
Product ID	Product_ID	0	0x00
	Revision_ID	0	0x01
	Reverse_Product_ID	0	0x5F
Output Access	Motion	0	0x02
	Delta_X_L	0	0x03
	Delta_X_H	0	0x04
	Delta_Y_L	0	0x05
	Delta_Y_H	0	0x06
	Motion Burst	0	0x16
Raw Data Output	RawData_Grab_Status	0	0x59
	RawData_Grab	0	0x58

8.0 Register

8.1 Register List

The chip registers are accessible via the serial port. The registers are used to read motion data and status as well as to set the device configuration.

Table 15. Register Map

Address	Bit Field	Name	Access	Bit Field Default Value	Register Default Value
0x00	-	Product_ID	R	-	0x4F
0x01	-	Revision_ID	R	-	0x00
0x02	-	Motion	R/W	-	0x00
0x03	-	Delta_X_L	R	-	0x00
0x04	-	Delta_X_H	R	-	0x00
0x05	-	Delta_Y_L	R	-	0x00
0x06	-	Delta_Y_H	R	-	0x00
0x07	-	Squal	R	-	0x00
0x08	-	RawData_Sum	R	-	0x00
0x09	-	Maximum_RawData	R	-	0x00
0x0A	-	Minimum_RawData	R	-	0x00
0x0B	-	Shutter_Lower	R	-	0x00
0x0C	-	Shutter_Upper	R	-	0x01
0x15	-	Observation	R/W	-	0x80
0x16	-	Motion_Burst	R/W	-	0x00
0x17	-	Squal2	R	-	0x00
0x3A	-	Power_Up_Reset	W	-	-
0x3B	-	Shutdown	W	-	-
0x47	-	Set_Resolution	W	-	0x00
0x48	-	Resolution_X_Lower	R/W	-	0x63
0x49	-	Resolution_X_Upper	R/W	-	0x00
0x4A	-	Resolution_Y_Lower	R/W	-	0x63
0x4B	-	Resolution_Y_Upper	R/W	-	0x00
0x58	-	RawData_Grab	R/W	-	0x00
0x59	-	RawData_Grab_Status	R	-	0x00
0x5B	-	Orientation	R/W	-	0x60
	Bit [7:5]	ORT [7:5]	R/W	3	
0x5C	-	Motion_Control	R/W	-	0x02
	Bit [7]	MOTC [7]	R/W	0	
	Bit [1]	MOTC [1]	R/W	1	
0x5F	-	Inverse_Product_ID	R	-	0xB0

8.2 Register Description

8.2.1 Product ID

Register Name	Product_ID		
Bank	0	**Address**	0x00
Access	R	**Default Value**	0x4F
Description	This value is a unique identification assigned to this model only. The value in this register does not change; it can be used to verify that the serial communications link is functional.		

Register Name	Revision_ID		
Bank	0	**Address**	0x01
Access	R	**Default Value**	0x00
Description	This register contains the current IC revision. It is subject to change when new IC versions are released.		

Register Name	Inverse_Product_ID		
Bank	0	**Address**	0x5F
Access	R	**Default Value**	0xB0
Description	This value is the inverse of the Product_ID. It is used to test the SPI port hardware.		

8.2.2 Reset and Shutdown Registers

Register Name	Power_Up_Reset		
Bank	0	**Address**	0x3A
Access	W	**Default Value**	-
Description	Write 0x5A to this register to reset the chip. All settings will revert to default values. Reset is required after recovering from Shutdown State and to restore normal operation after Frame Capture.		

Register Name	Shutdown		
Bank	0	**Address**	0x3B
Access	W	**Default Value**	-
Description	Write 0xB6 to this register to set the chip to Shutdown State. Refer to Section 5.3 for more details and on the recovery procedure.		

8.2.3 Operational Control

Register Name	Set_Resolution		
Bank	0	**Address**	0x47
Access	W	**Default Value**	0x00
Description	This register sets the X and Y resolutions of the chip, after the respective values are written in Resolution_X and Resolution_Y registers. This is achieved by setting bit 0 of this register to 1.		

Bit Field	Name	Default Value	Description
0	SRES	0	Set / Update resolution setting 0: No 1: Yes

Register Name	Resolution_X_Lower		
Bank	0	**Address**	0x48
Access	R/W	**Default Value**	0x63
Register Name	**Resolution_X_Upper**		
Bank	-	**Address**	0x49
Access	R/W	**Default Value**	0x00
Description	This register sets the resolution of the X-axis of the chip. Write to Resolution_X_Lower register first, and then followed by Resolution_X_Upper register. These two registers should be written consecutively. Upon these registers write, set bit 0 of Set_Resolution register to 1 to kick in the resolution setting. To calculate the resolution value of each register setting, use the formula below: Resolution = (Register Value + 1) x 100 Set X-axis resolution: 0x0000: 100 cpi (minimum); 39 counts/cm 0x0001: 200 cpi 0x0002:300 cpi … 0x0013: 2000 cpi … 0x00C7: 20,000 cpi (maximum)		

Register Name	Resolution_Y_Lower		
Bank	0	**Address**	0x4A
Access	R/W	**Default Value**	0x63
Register Name	**Resolution_Y_Upper**		
Bank	0	**Address**	0x4B
Access	R/W	**Default Value**	0x00
Description	This register sets the resolution of the Y-axis of the chip. Write to Resolution_Y_Lower register first, and then followed by Resolution_Y_Upper register. These two registers should be written consecutively. Upon these registers write, set bit [0] of Set_Resolution register to 1 to kick in the resolution setting. To calculate the resolution value of each register setting, use the formula below: Resolution = (Register Value + 1) x 100 Set Y-axis resolution: 0x0000: 100 cpi (minimum); 39 count/cm 0x0001: 200 cpi 0x0002: 300 cpi … 0x0013: 2000 cpi … 0x00C7: 20,000 cpi (maximum)		

Register Name	Orientation		
Bank	0	**Address**	0x5B
Access	R/W	**Default Value**	0x60
Description	This register sets the orientation of the reported X and Y positions. This includes swapping of X and Y; and flipping (inverting) the direction of X and Y axis. If both are selected, swapping is done before flipping.		

Bit Field	Name	Default Value	Description
7	ORT[7]	0	Swap X and Y 0: No swap 1: Swap
6	ORT[6]	1	Invert Y direction 0: Not inverted 1: Inverted
5	ORT[5]	1	Invert X direction 0: Not inverted 1: Inverted

Register Name	Motion_Control		
Bank	0	**Address**	0x5C
Access	R/W	**Default Value**	0x02
Description	This register configures the behavior of the motion pin, and the selection of the X-axis and Y-axis resolution mode.		

Bit Field	Name	Default Value	Description
7	MOTC [7]	0	0: Motion = Active low 1: Motion = Active high
1	MOTC [1]	1	0: Both the X-axis and Y-axis resolutions are defined by Resolution_X_Lower and Resolution_X_High registers. 1: The X-axis resolution are defined by Resolution_X_Lower and Resolution_X_High registers; and the Y-axis resolution are defined by Resolution_Y_Lower and Resolution_Y_High registers. (Default)

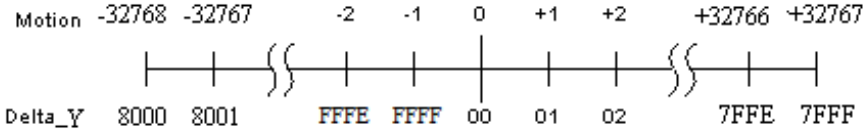
8.2.4 Motion Related Registers

Register Name	Motion		
Bank	0	**Address**	0x02
Access	R/W	**Default Value**	0x00
Description	This register allows user to determine if motion has occurred since the last time it was read. The procedure to read the motion registers is as follows: 1. Read the Motion register. This will freeze the Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H register values. **Note:** Burst read will clear the Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H registers, and thus should not be executed at this stage. 2. If Bit[7] is set, Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H registers should be read in sequence to get the accumulated motion. **Note:** If Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H registers are not read before the motion register is read for the second time, the data in Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H will be lost. 3. To read a new set of motion data (Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H), repeat from Step (1). **Note:** Writing anything to this register clears the Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H registers.		

Bit Field	Name	Default Value	Description
7	MOT [7]	0	Motion since last report 0: No motion 1: Motion occurred, data ready for reading in Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H registers.

Register Name	Delta_X_L		
Bank	0	**Address**	0x03
Access	R	**Default Value**	0x00

Register Name	Delta_X_H		
Bank	0	**Address**	0x04
Access	R	**Default Value**	0x00
Description	16-bit 2's complement number. X movement counts since last report. Absolute value is determined by resolution. Reading it clears the register.  **Note:** It is recommended that registers 0x02, 0x03, 0x04, 0x05 and 0x06 to be read sequentially.		

Register Name	Delta_Y_L		
Bank	0	**Address**	0x05
Access	R	**Default Value**	0x00
Register Name	**Delta_Y_H**		
Bank	0	**Address**	0x06
Access	R	**Default Value**	0x00
Description	16-bit 2's complement number. Y movement counts since last report. Absolute value is determined by resolution. Reading it clears the register.  **Note:** It is recommended that registers 0x02, 0x03, 0x04, 0x05 and 0x06 to be read sequentially.		

Register Name	Motion_Burst		
Bank	0	**Address**	0x16
Access	R/W	**Default Value**	0x00
Description	The Motion_Burst register is used for high-speed access of up to 12 register bytes. See Section 7.2.2 for usage details.		

8.2.5 Operational Check Related Registers

Register Name	SQUAL		
Bank	0	**Address**	0x07
Access	R	**Default Value**	0x00
Description	The SQUAL (Surface quality) register is a measure of the number of valid features visible by the chip in the current frame. Use the following formula to find the total number of valid features: Number of Features = SQUAL Register Value x 4 The maximum SQUAL register value is 0xFF. Since small changes in the current frame can result in changes in SQUAL, variations in SQUAL when looking at a surface are expected. SQUAL values are only valid in Run State.		

Register Name	RawData_Sum		
Bank	0	Address	0x08
Access	R	Default Value	0x00
Description	This register is used to find the average raw data value. To find the average raw data value, use the formula below: Average Raw Data = (Register Value x 1024) / 1296 The maximum register value is 0xA0. The minimum register value is 0. The RawData_Sum value can change every frame.		

Register Name	Maximum_RawData		
Bank	0	Address	0x09
Access	R	Default Value	0x00
Description	Maximum raw data value in current frame. Minimum value = 0, maximum value = 127. The maximum raw data value can change every frame.		

Register Name	Minimum_RawData		
Bank	0	Address	0x0A
Access	R	Default Value	0x00
Description	Minimum raw data value in current frame. Minimum value = 0, maximum value = 127. The minimum raw data value can change every frame.		

Register Name	Shutter_Lower		
Bank	0	Address	0x0B
Access	R	Default Value	0x00

Register Name	Shutter_Upper		
Bank	0	Address	0x0C
Access	R	Default Value	0x01

Bit Field	Name	Default Value	Description
3:0	S[11:8]	0	Upper 4-bit of the 12-bit *Shutter* register.
Description	12-bit Shutter register. Unit is clock cycles of the internal oscillator. Read Shutter_Upper first, then Shutter_Lower. They should be read consecutively. The shutter is adjusted to keep the average raw data values within normal operating range. The shutter value is checked and automatically adjusted to a new value if needed on every frame.		

Register Name	SQUAL2		
Bank	0	**Address**	0x17
Access	R	**Default Value**	0x00
Description	The SQUAL2 (Surface quality 2) register is a measure of the number of stronger valid features visible by the chip in the current frame. Use the following formula to find the total number of stronger valid features: Number of Features = SQUAL2 Register Value x 4 The maximum SQUAL2 register value is 0xFF. Since small changes in the current frame can result in changes in SQUAL2, variations in SQUAL2 when looking at a surface are expected. SQUAL2 values are only valid in Run State. This value can be used as a reference for tracking ability on a particular surface. A lower value indicates the tendency of poorer tracking performance on that surface. From actual test results (based on the condition stated in Table 3), on a very dark carpet where the sensor is not able to track, the SQUAL2 values are always less than 50; while on a good surface such as aluminum, the SQUAL2 values are always greater than 100.		

8.2.6 Troubleshooting Related Registers

Register Name	Observation		
Bank	0	**Address**	0x15
Access	R/W	**Default Value**	0x80
Description	User must clear the register by writing 0x00, wait for 1 ms, and read the register. The active processes OB [7:0] will have set their corresponding bits. The read back value should be 0xB7 or 0xBF.		

Register Name	RawData_Grab		
Bank	0	**Address**	0x58
Access	R/W	**Default Value**	0x00
Description	This register is used to read out the full array of raw data values. The chip needs to be held stationary for the duration of grabbing raw data until the full array is completely read out, as the information is read out one data at a time. Refer to Section 7.3.5 for more details.		

Register Name	RawData_Grab_Status		
Bank	0	**Address**	0x59
Access	R	**Default Value**	0x00
Description	This register provides status of raw data grab process. Refer to Section 7.3.5 for more details.		

Bit Field	Name	Default Value	Description
7	RDGS [7]	0	0: Raw data grab is not valid 1: Raw data grab is valid
6	RDGS [6]	0	0: Raw data is not from coordinate 0,0 1: Raw data is from coordinate 0,0

Revision History

Revision Number	Date	Description
0.5	20 Mar 2020	Initial draft copy
0.7	2 Oct 2020	Page 1 Add in Setting1 (Low Power) Specifications Page 9-10: Split the Setting1 & Setting2 Speed and Z-Height per Surface Categories for Recommended Operating Condition and DC Characteristics Page 14: Add in packing information Page 19-22: Add Power-up Setup Time Page 28: Add System Control Initialization Flow Page 29-32 Add in Performance Optimization Register Settings Page 34: Add Output data section
0.71	4 Aug 2021	Page 1: Speed changed from 2.5m/s to 5m/s Page 1: Working Distance to Tracking Surface change from 10-35mm to 10-30mm Page 1: Typical power consumption from 8.5mA to 16.5mA Section 2.2 & Section 2.3: Removed Setting 1 Section 2.2: Z for Diffuse surface changed from 15-20mm to 17-22mm Section 2.2: Added Note 6 for Matte Textured Tiles Section 2.4: Table 5 change both $t_{MOT-RST}$ and t_{WAKEUP} from 50ms to 120ms Section 3.3: Edited packing information with per tube quantity Section 7.1: Edited Figure 20. Initialization Flow Section 7.1.2: Add Figure 21. Power-On Check Routine Section 7.1.2.1: Add 7.1.2.1 Power-On Check Steps Section 7.1.2.2: Add Laser Power Setting Section 7.1.2: Edit Performance Optimization Setting if Laser flag=0 Section 7.1.4: Add Performance Optimization Setting if Laser flag=1 Section 7.1.4.1: Add Laser Power Registers Setting Validation Section 7.1.5: Add Chip Settings Validation Section 7.1.3: Add Matte Textured Surface Performance Improvement Setting
0.8	29 Aug 2022	Replaced all VDD2 with VDD and VDD3 with VDD_VCSEL Section 1.1 and Section 1.3: Change LASER_N and LASER_P to VCSEL_N and VCSEL_P Section 1.3: Add note and red box to the 4 pads at the bottom of the chip – “The 4 pads in Figure 2 (red boxed) should be left unconnected “ Section 2.2: Z for Glossy non-metal surfaces changed from 10-30mm to 10-27mm Section 2.2: Z for Diffuse surface changed from 17-22mm to 17-21mm Section 3.3: Add Packing Information Section 4.3: Add Chip Assembly Tilt Section 4.4: Add Keep Out Area Section 4.6.1: Add section 4.5.1 Handling Precaution of Moisture Sensitivity During Assembly Processes Section 4.7: Add Surface Coverage Section 5.2.1: Changed $t_{NCS-SCLK}$ from 20ms to 120ns as per in Table 5. AC Electrical Specification Section 7.1.1: Edited Initialization Flow Removed Section 7.1.2.1: Power-On Check Steps

Revision Number	Date	Description
		Removed Section 7.1.2.2: Laser Power Setting Removed Section 7.1.4: Performance Optimization Setting if Laser flag=1 Removed Section 7.1.4.1: Laser Power Registers Setting Validation Removed Section 7.1.5: Add Chip Settings Validation Removed Appendix
0.81	10 Jan 2023	Section 2.2: Table 3. Added $Z_{C,}$ distance from top of cover Section 2.2: Add cross section view with Z_S, Z_C and Z_{GAP} Section 2.2: Add Note 7 in Table 3.0 for Z_S, Z_C and Z_{GAP} Section 4.5: Added protective cover design section Section 7.1.2: Added Line Drift Improvement code (Step 134 to 142)
0.82	15 Sept 2023	Table 2: Revised absolute maximum values for VDD, VDD_VCSEL, VDDIO and V_{IN} Section 5.2.1 and Figure 19: Revised the sequence to power on VDD, VDDIO and VDD_VCSEL
0.83	24 Nov 2023	Section 4.5.2: Revised the require wavelength range to 800 to 900 nm Section 8.1 and 8.2.5: Added *Squal2* register (address 0x17) Section 5.2.1: Revised the statement for NCS to reset SPI port