Leveraging true heterogeneous compute for autonomous systems

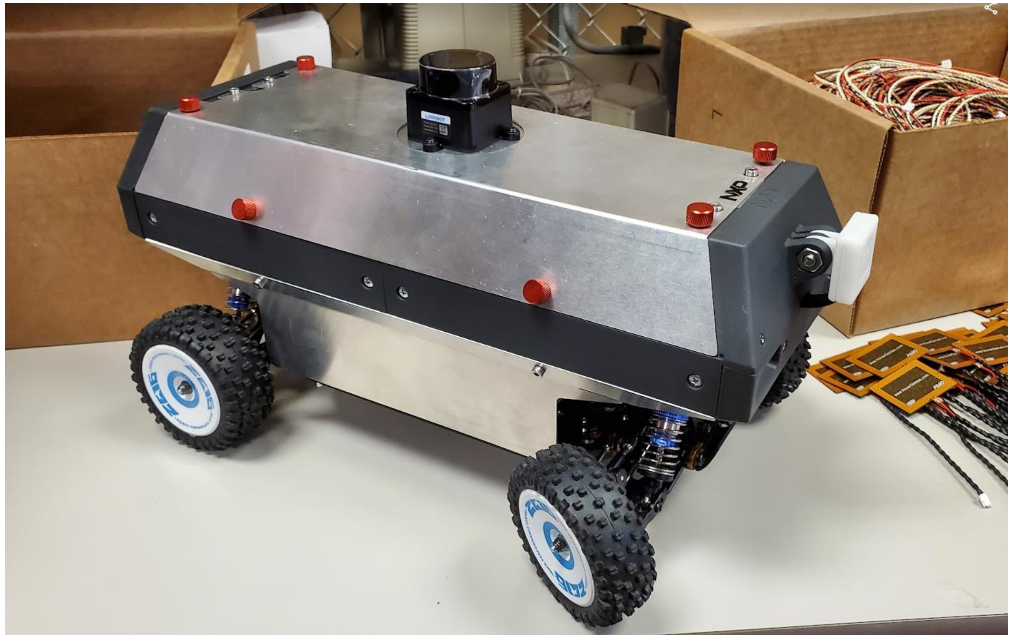
Peter van der Perk

Introduction

Peter van der Perk - NXP Semiconductors, CTO Systems Innovations

Mobile Robotics team

- Multinational team: Netherlands, Germany, USA, Canada
- Reference designs and development platforms for autonomous rovers and drones
- Many of our systems support Cognipilot & Zephyr:
  - i.MXRT
  - IMX95
  - MCXN
  - S32K344

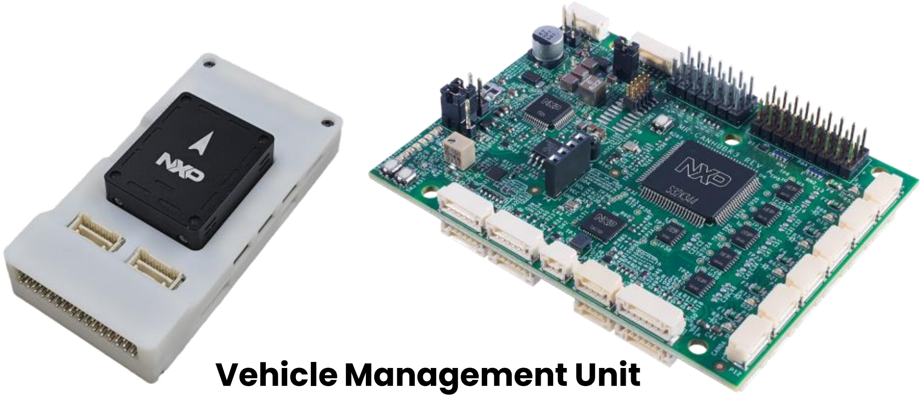


Notes and sources

From Real-Time to ROS 2: Streamlining Control on a Single SoC

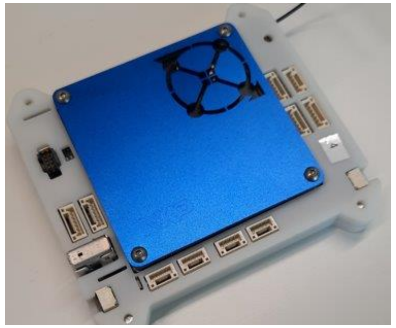
- How can we integrate:
  - Low-level real-time control
  - High-level ROS 2-based control
  - Safety-critical ready features
- On a single System-on-Chip (SoC)?
  - What are the benefits?
  - How to deal with complexity?
  - How to deal with real-time and non-real-time tasks?

Scope – Present situation



Vehicle Management Unit
Vehicle control
Path planning
Nuttx / PX4
i.MX RT 1170
MR-CANHUBK344

Data exchange
CAN/Ethernet

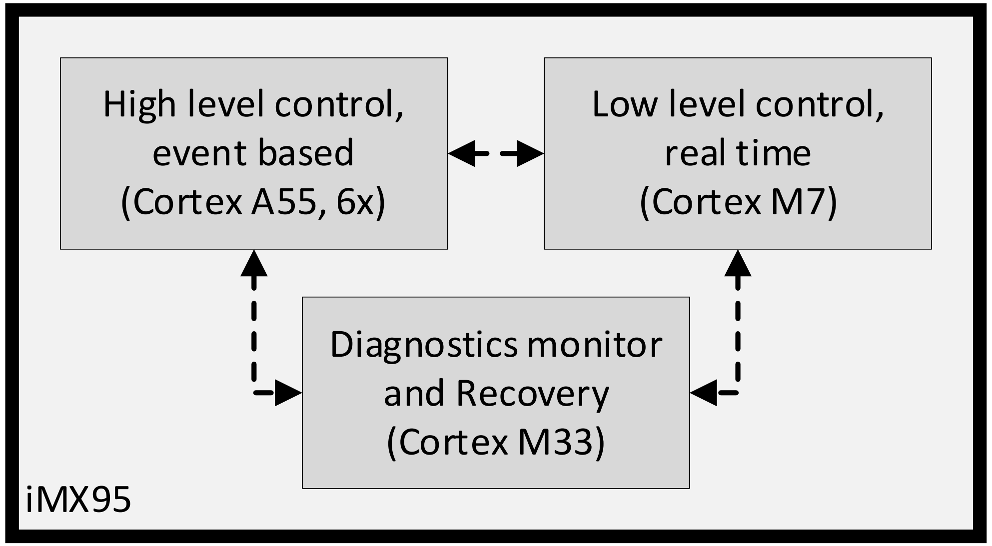


Companion computer
High level control
Compute intense functions
Linux
i.MX 8M+
NavQ+

 Notes and sources

Scope - Targeted situation

Companion computer
High level control
Compute intense functions
Trajectory calculation
Linux
ROS2
Cognipilot



Vehicle Management Unit
Vehicle control
Motor control
Trajectory execution
Zephyr / Nuttx

Diagnostics
Zephyr

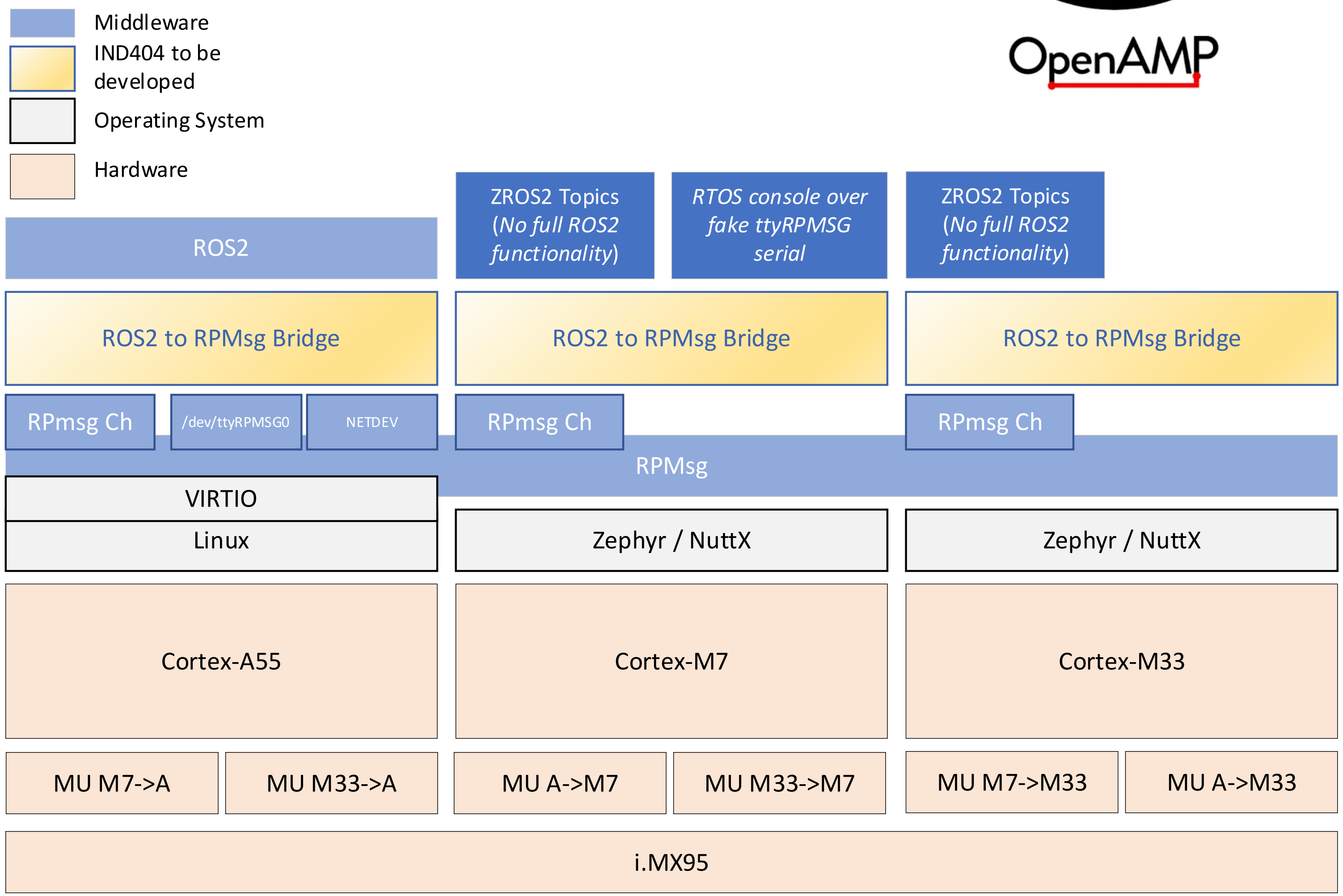
Target application
AMR
Rovers
Drones

Data exchange
On chip - RpMsg

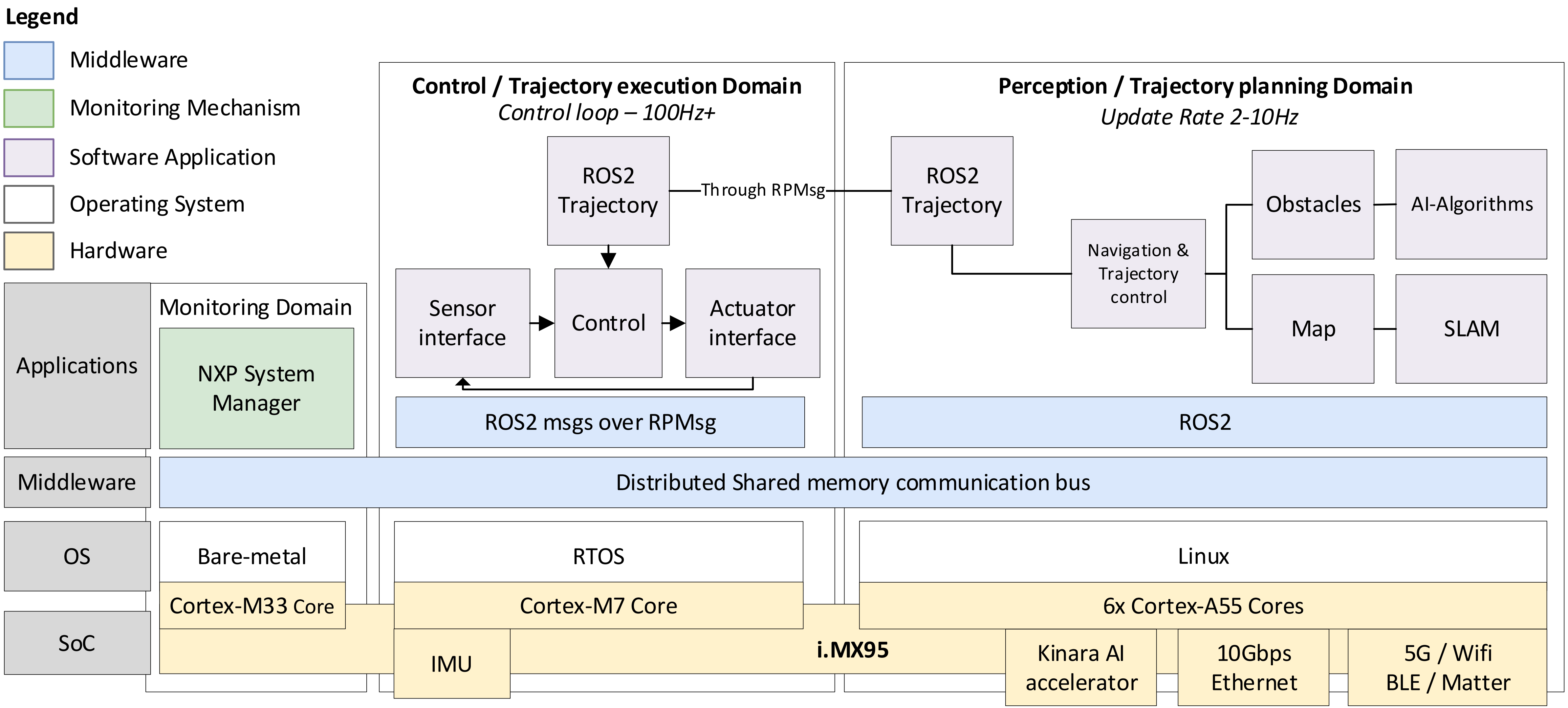
Notes and sources

i.MX OpenAMP/RPMsg implementation

- Linux already has RPMsg implemented on top VIRTIO exposing:
  - RPMsg communication channels
  - Virtual TTY over shared memory
  - Netdevice: IP networking to RPMsg
- Zephyr also implements RPMsg albeit “a bit basic”
  - Our goal is to improve the Zephyr implementation to simplify heterogeneous compute and ease ROS2 integration.

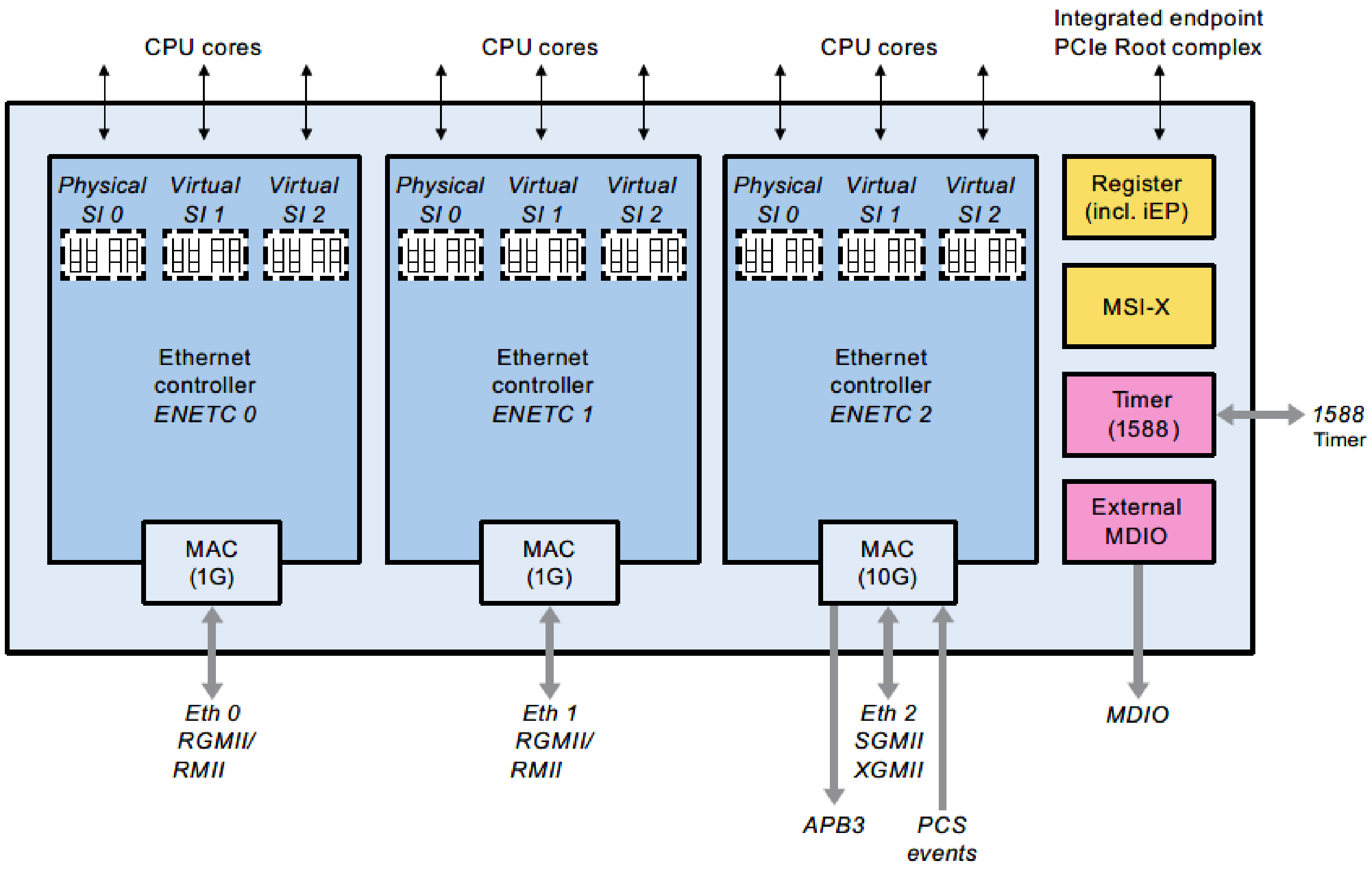


NavQ95 Heterogenous Software Stack



NavQ95 Distributed Networking

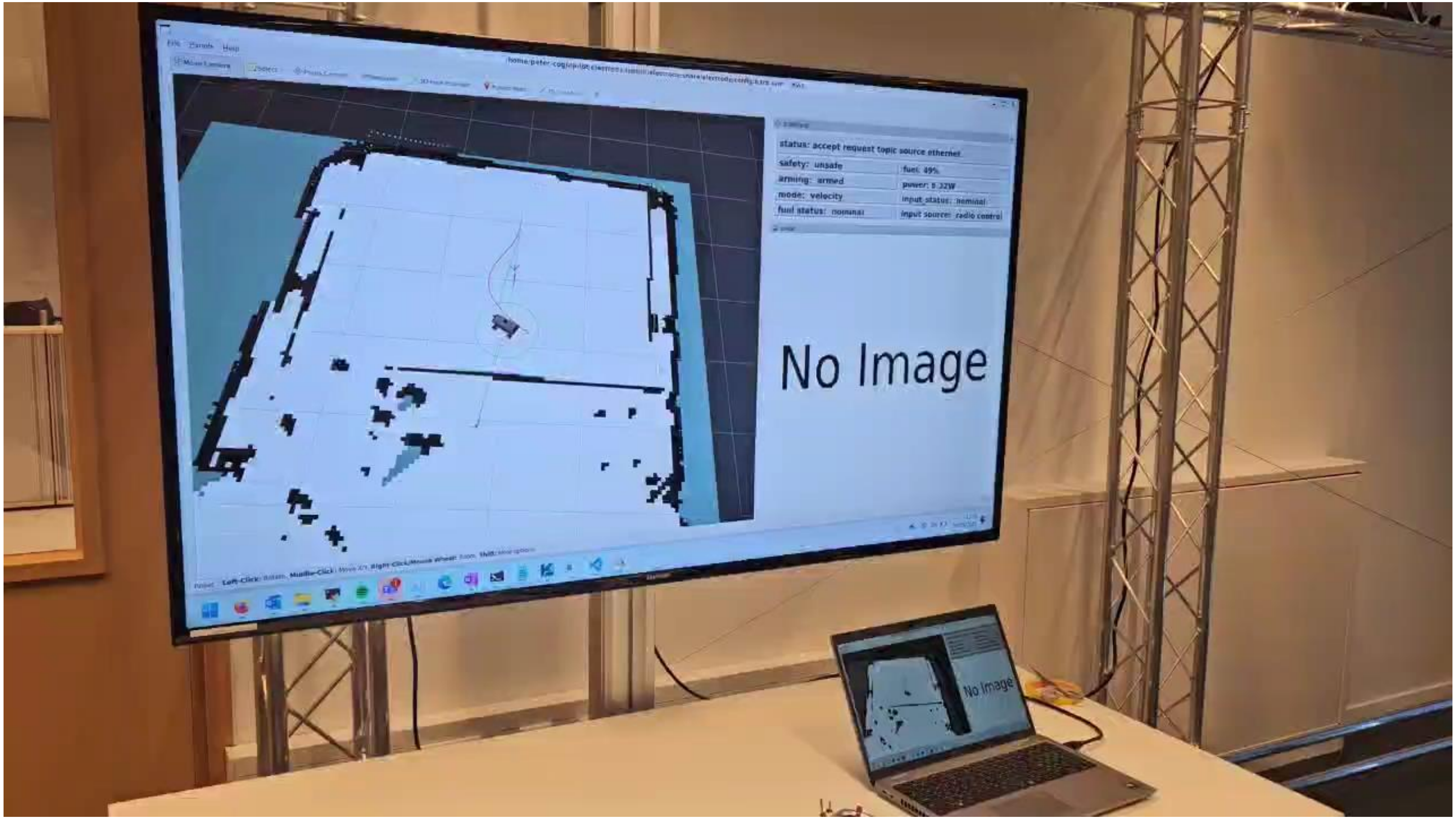
- i.MX95 has 3 NETC Ethernet Controllers
- NETC Ethernet controller has 3 interfaces to the SoC
  - 1 Physical
  - 2 Virtual
- Each interfaces can be either
  - Cortex-A Core
    - Virtualized Domain inside
  - Cortex-M Core
- External/Internal routing
  - External packets from a single port can be routed to different cores
  - Different cores can also communicate with each-other over ethernet



MR-B3RB-M “Buggy3 RevB”

Small Robotic Rover for developers.
Used in HoverGames, RoverGames, AIM, NXP-CUP

B3RB NavQ95 Heterogenous demo



Current results and Future Goals

Create a combination of low-level real-time control with high-level vehicle control and safety functions.

Results

- Prototype hardware based on i.MX 95
- Nuttx + RpMsg on M7 core — contributed to open source
- Zephyr + RpMsg on M7 core — contributed to open source

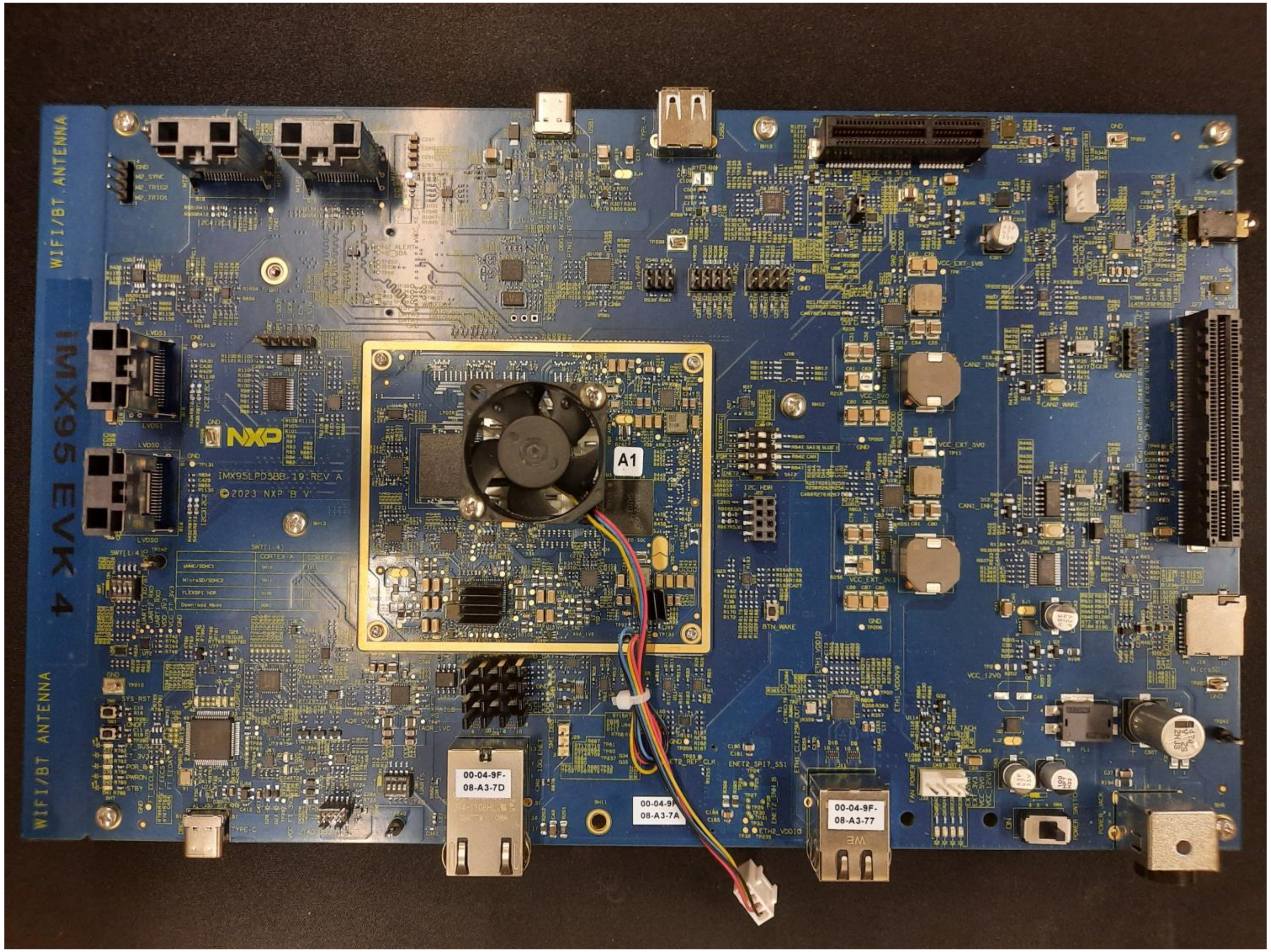
Current software goals

- Streamline software deployment on different cores (bootloader enablement)
- Improve shared message bus
  - ideally first-class Zenoh shared memory transport integration
  - Alternative means for serialization ROS2 / DDS / CDR is quite inefficient
- Virtual NETC implemantion for Zephyr

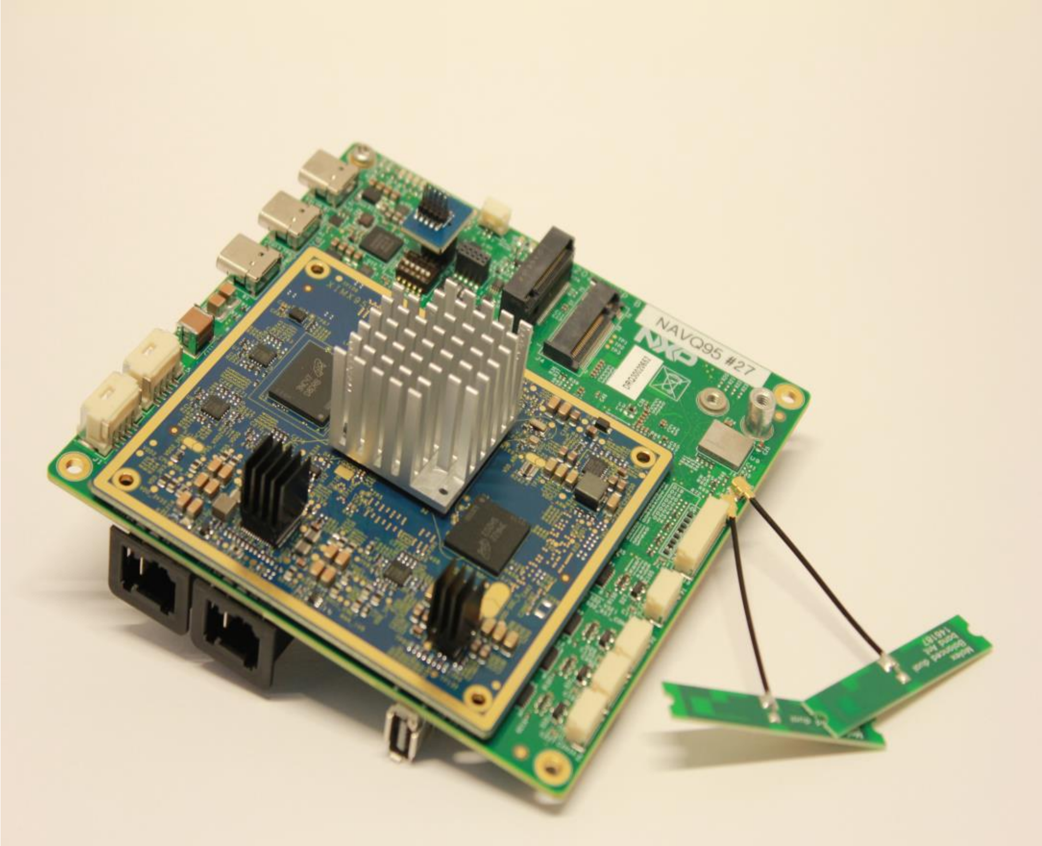
01

Hardware

NavQ95v1 2024 PoC Board

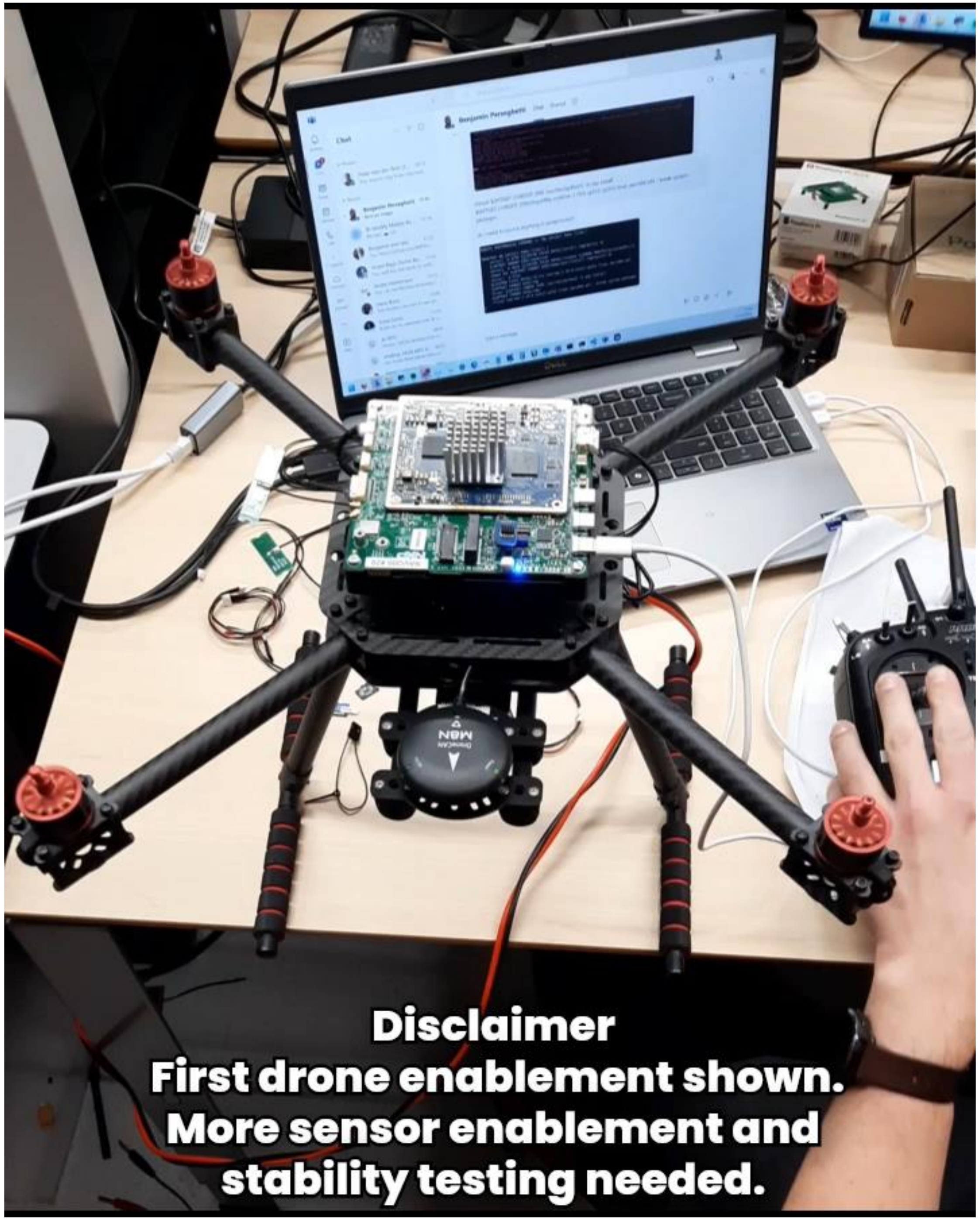


i.MX 95 EVK

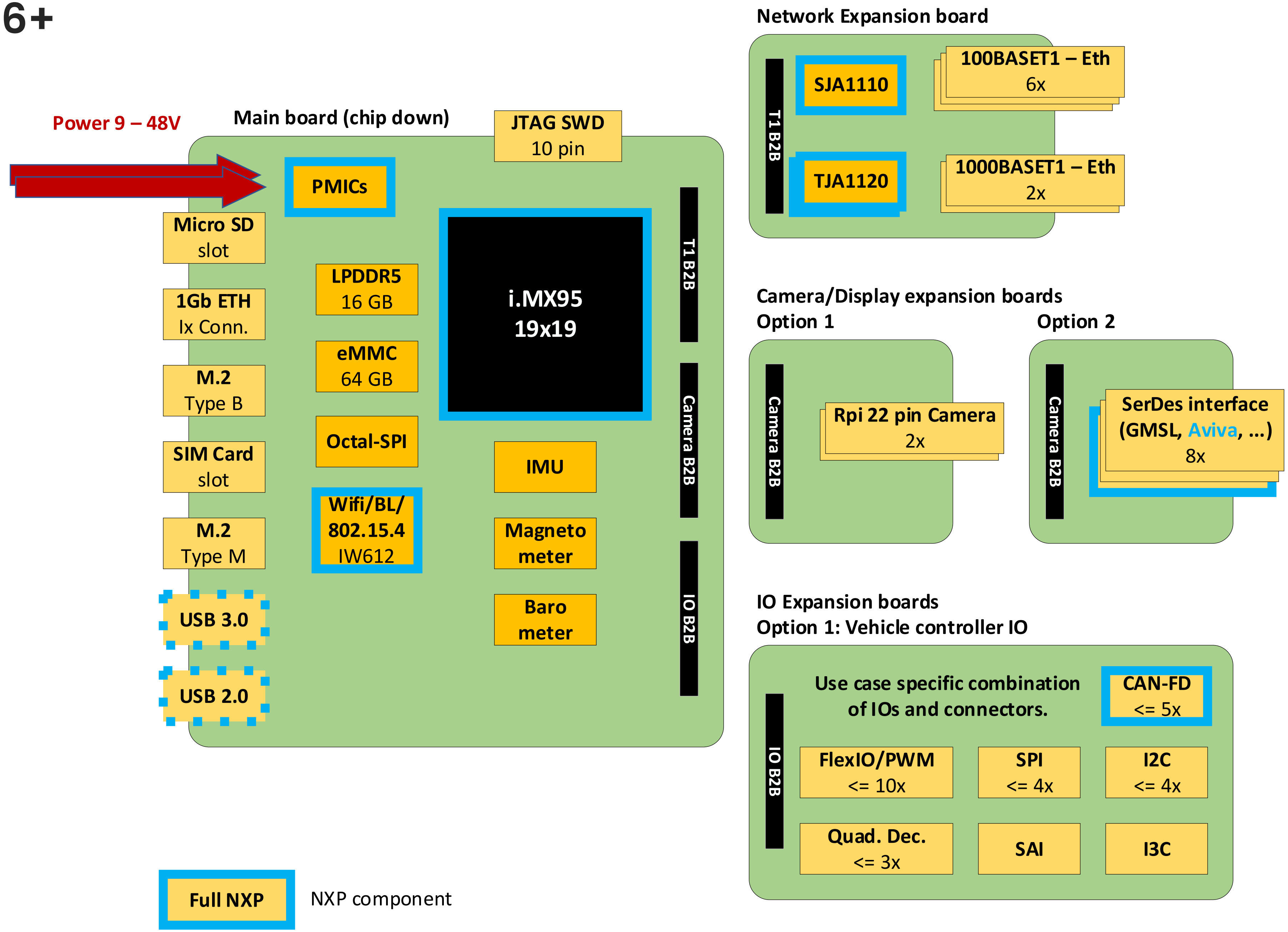


NavQ95

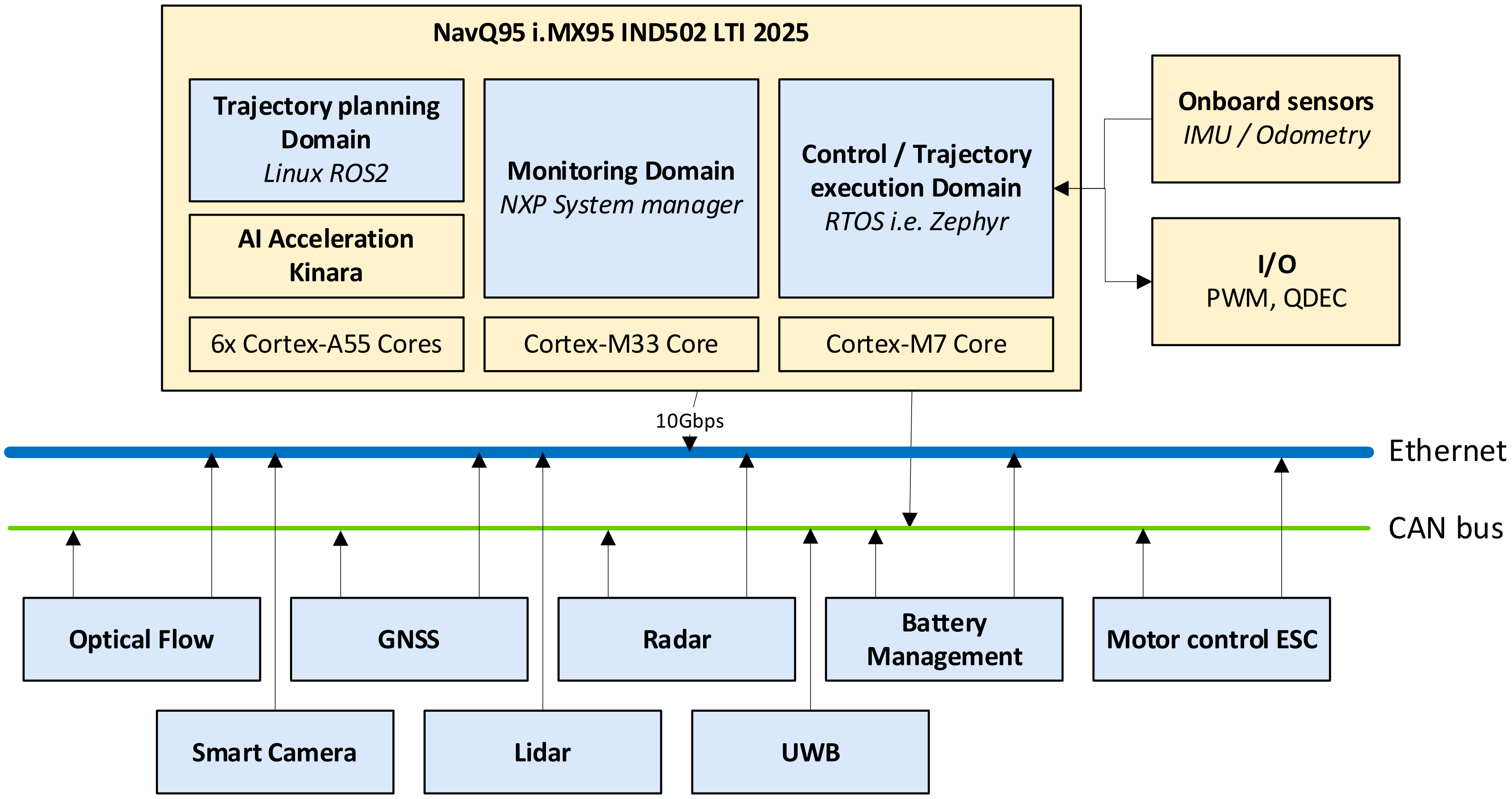
NavQ95v1 2024 – Drone test



NavQ95 V2 2026+



NavQ95 Distributed Networking Architecture



Questions

Peter van der Perk
Peter.vanderperk@nxp.com

nxp.com

i.MX95 Shared Memory architecture