MSP430G2x53, MSP430G2x33, MSP430G2x13, MSP430G2x03 Device Erratasheet

1 Current Version

See Appendix A for prior silicon revisions.

✓ The checkmark indicates that the issue is present in the specified revision

Device	Rev:	BCL12	CPU4	EEM20	SYS15	TA12	TA16	TA22	USCI20	USCI22	USCI23	USCI24	USCI25	USCI26	USCI29	USCI30	XOSC5
MSP430G2113	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430G2153	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430G2203	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430G2213	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430G2233	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430G2253	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430G2303	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430G2313	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430G2333	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430G2353	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430G2403	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430G2413	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430G2433	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430G2453	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430G2513	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430G2533	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430G2553	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

2 Package Markings

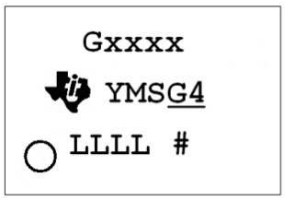
N20

PDIP (N), 20 Pin

YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision

PW20

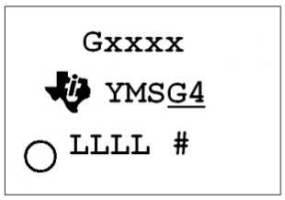
TSSOP (PW), 20 Pin



YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision
o = PIN 1

PW28

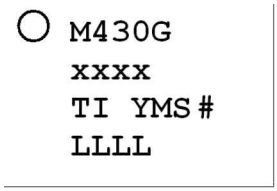
TSSOP (PW), 28 Pin



YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision
o = PIN 1

RHB32

QFN (RHB), 32 Pin



YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision
o = PIN 1

3 Detailed Bug Description

BCL12 *Basic Clock Module*

Function Switching RSEL can cause DCO dead time

Description After switching RSELx bits (located in register BCSCTL1) from a value of >13 to a value of <12 OR from a value of <12 to a value of >13, the resulting clock delivered by the DCO can stop before the new clock frequency is applied. This dead time is approximately 20 µs. In some instances, the DCO may completely stop, requiring a power cycle.

Workaround

- When switching RSEL from >13 to <12, use an intermediate frequency step. The intermediate RSEL value should be 13.

CURRENT RSEL	TARGET RSEL	RECOMMENDED TRANSITION SEQUENCE
15	14	Switch directly to target RSEL
14 or 15	13	Switch directly to target RSEL
14 or 15	0 to 12	Switch to 13 first, and then to target RSEL (two step sequence)
0 to 13	0 to 12	Switch directly to target RSEL

- When switching RSEL from <12 to >13, ensure that the maximum system frequency is not exceeded during the transition. This can be achieved by clearing the DCO bits first (DCOCTL control register, bits 7–5), then increasing the RSEL value, and finally applying the target frequency DCO bit values. For more details, see the examples in the "TLV Structure" chapter in the *MSP430F2xx Family User's Guide* (SLAU144).

CPU4 *CPU Module*

Function PUSH #4, PUSH #8

Description The single operand instruction PUSH cannot use the internal constants (CG) 4 and 8. The other internal constants (0, 1, 2, –1) can be used. The number of clock cycles is different:

PUSH #CG uses address mode 00, requiring 3 cycles, 1-word instruction

PUSH #4/#8 uses address mode 11, requiring 5 cycles, 2-word instruction

Workaround Workaround implemented in assembler. No fix planned.

EEM20 *Enhanced Emulation Module*

Function Debugger might clear interrupt flags

Description During debugging, read-sensitive interrupt flags might be cleared as soon as the debugger stops. This is valid in both single-stepping and free-run modes.

Workaround None

SYS15 *System Module*

Function LPM3 and LPM4 currents exceed specified limits

Description LPM3 and LPM4 currents may exceed specified limits if the SMCLK source is switched from DCO to VLO or LFXT1 just before the instruction to enter LPM3 or LPM4 mode.

Workaround After clock switching, a delay of at least four new clock cycles (VLO or LFXT1) must be implemented to complete the clock synchronization before going into LPM3 or LPM4.

TA12 *Timer_A Module*

Function Interrupt is lost (slow ACLK)

Description Timer_A counter is running with slow clock (external TACLK or ACLK) compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by one with the occurring compare interrupt (if TAR = CCRx).

Due to the fast MCLK, the CCRx register increment (CCRx = CCRx + 1) happens before the Timer_A counter has incremented again. Therefore, the next compare interrupt should happen at once with the next Timer_A counter increment (if TAR = CCRx + 1). This interrupt is lost.

Workaround Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterward.

TA16 *Timer_A Module*

Function First increment of TAR erroneous when IDx > 00

Description The first increment of TAR after any timer clear event (POR/TACLR) happens immediately following the first positive edge of the selected clock source (INCLK, SMCLK, ACLK, or TACLK). This is independent of the clock input divider settings (ID0, ID1). All following TAR increments are performed correctly with the selected IDx settings.

Workaround None

TA22 *Timer_A Module*

Function Timer_A register modification after watchdog timer PUC

Description Unwanted modification of the Timer_A registers TACTL and TAIV can occur when a PUC is generated by the watchdog timer (WDT) in watchdog mode and any Timer_A counter register TACCRx is incremented/decremented (Timer_A does not need to be running).

Workaround Initialize TACTL register after the reset occurs using a MOV instruction (BIS or BIC may not fully initialize the register). TAIV is automatically cleared following this initialization.

Example

```
MOV.W #VAL, &TACTL
```

Where VAL = 0, if Timer is not used in application; otherwise, user defined per desired function.

USCI20 *USCI Module*

Function I^2C mode multi-master transmitter issue

Description When configured for I^2C master-transmitter mode and used in a multi-master environment, the USCI module can cause unpredictable bus behavior if all of the following conditions are true:

1. Two masters are generating SCL.
   and
2. The slave is stretching the SCL low phase of an ACK period while outputting NACK on SDA.
   and
3. The slave drives ACK on SDA after the USCI has already released SCL, and then the SCL bus line is released.
   and
4. The transmit buffer has not been loaded before the other master continues communication by driving SCL low.

The USCI remains in the SCL high phase until the transmit buffer is written. After the transmit buffer has been written, the USCI interferes with the current bus activity and may cause unpredictable bus behavior.

Workaround

- Ensure that slave does not stretch the SCL low phase of an ACK period.
  or
- Ensure that the transmit buffer is loaded in time.
  or
- Do not use the multi-master transmitter mode.

USCI22 *USCI Module*

Function I^2C master receiver with 10-bit slave addressing

Description Unexpected behavior of the USCI_B can occur when configured in I^2C master receive mode with 10-bit slave addressing under the following conditions:

1. The USCI sends first byte of slave address, the slave sends an ACK and when second address byte is sent, the slave sends a NACK.
2. Master sends a repeat start condition (if UCTXSTT = 1).
3. The first address byte following the repeated start is acknowledged.

However, the second address byte is not sent; instead, the master incorrectly starts to receive data and sets UCBxRXIFG = 1.

Workaround Do not use a repeated start condition; instead, set the stop condition UCTXSTP = 1 in the NACK ISR prior to the following start condition (USTXSTT = 1).

USCI23 *USCI Module*

Function UART transmit mode with automatic baud rate detection

Description Erroneous behavior of the USCI_A can occur when configured in UART transmit mode with automatic baud rate detection. During transmission if a "Transmit break" is initiated (UCTXBRK = 1), the USCI_A does not deliver a stop bit of logic high; instead, it sends a logic low during the subsequent synch period.

Workaround

- Follow user's guide instructions for transmitting a break/synch field following UCSWRST = 1.
  or
- Set UCTXBRK = 1 before an active transmission; that is, check for bit UCBUSY = 0 and then set UCTXBRK = 1.

USCI24 *USCI Module*

Function Incorrect baud rate information during UART automatic baud rate detection mode

Description Erroneous behavior of the USCI_A can occur when configured in UART mode with automatic baud rate detection. After automatic baud rate measurement is complete, the UART updates UCAxBR0 and UCAxBR1. Under oversampling mode (UCOS16 = 1), for baud rates that should result in UCAxBRx = 0x0002, the UART incorrectly reports it as UCAxBRx = 0x5555.

Workaround When break/synch is detected following the automatic baud rate detection, the flag UCBRK flag is set to 1. Check if UCAxBRx = 0x5555 and correct it to 0x0002.

USCI25 *USCI Module*

Function TXIFG is not reset when NACK is received in I^2C mode

Description When the USCI_B module is configured as an I^2C master transmitter, the TXIFG is not reset after a NACK is received if the master is configured to send a restart (UCTXSTT = 1 and UCTXSTP = 0).

Workaround Reset TXIFG in software within the NACKIFG interrupt service routine.

USCI26 *USCI Module*

Function t_{buf} parameter violation in I^2C multi-master mode

Description In multi-master I^2C systems, the timing parameter t_{buf} (bus free time between a stop condition and the following start) is not ensured to match the I^2C specification of 4.7 µs in standard mode and 1.3 µs in fast mode. If the UCTXSTT bit is set during a running I^2C transaction, the USCI module waits and issues the start condition on bus release, causing the violation to occur.

NOTE: It is recommended to check if UCBBUSY bit is cleared before setting UCTXSTT = 1.

Workaround None

USCI29 *USCI Module*

Function

Timing of USCI I2C interrupts may result in call to a reserved ISR location

Description

When certain USCI I2C interrupt flags (IFG) are set and an automatic flag-clearing event on the I2C bus occurs, the device makes a call to the TRAPINT interrupt vector. This happen only if the IFG is cleared within a critical time window (~6 CPU clock cycles) after a USCI interrupt request occurs and before the interrupt servicing is initiated. The affected interrupts are UCBxTXIFG, UCSTPIFG, UCSTTIFG, and UCNACKIFG.

The automatic flag-clearing scenarios are described in the following situations:

- A pending UCBxTXIFG interrupt request is cleared on the falling SCL clock edge following a NACK.
- A pending UCSTPIFG, UCSTTIFG, or UCNACKIFG interrupt request is cleared by a following Start condition.

Workaround

1. Define an ISR for the reserved interrupt vector at location 0xFFE0 containing an RETI instruction. If the failure condition occurs; a call to the reserved ISR is made following which the device returns to the application code and continues execution.

   Sample code for ISR definition:

```
; Dummy ISR
;-----------------------------------------

IntSR07  ; ISR call at 0xFFE0h
   reti  ; return to application
;-----------------------------------------
```

2. Poll the affected flags instead of enabling the interrupts.

USCI30 *USCI Module*

Function

I2C mode master receiver / slave receiver

Description

The USCI I2C module, when configured as a receiver (master or slave), performs a double-buffered receive operation. For example, in a transaction of two bytes, after the first byte is moved from the receive shift register to the receive buffer, the byte is acknowledged and the state machine allows the reception of the next byte.

If the receive buffer has not been cleared of its contents by reading the UCBxRXBUF register by the time the seventh bit of the following data byte is received, an error condition may occur on the I2C bus. Depending on the USCI configuration, the following may occur:

- If the USCI is configured as an I2C master receiver, an unintentional repeated start condition can be triggered or the master can switch into an idle state (I2C communication aborted). The reception of the current data byte is not successful in this case.
- If the USCI is configured as I2C slave receiver, the slave can switch to an idle state, stalling I2C communication. The reception of the current data byte is not successful in this case. The USCI I2C state machine notifies the master of the aborted reception with a NACK.

Note that the error condition described above occurs only within a limited window of the seventh bit of the current byte being received. If the receive buffer is read outside of this window (before or after), then the error condition does not occur.

Workaround

The error condition can be avoided by servicing the UCBxRXIFG in a timely manner. This can be done by (a) servicing the interrupt and ensuring UCBxRXBUF is read promptly or (b) using the DMA to automatically read bytes from receive buffer upon UCBxRXIFG being set.

OR

If the receive buffer cannot be read out in time, test the I2C clock line before the UCBxRXBUF is read out to ensure that the critical window has elapsed. This is done by checking if the clock line low status indicator bit UCSCLLOW is set for at least three USCI bit clock cycles; that is, $3 \times t_{BitClock}$.

NOTE: The last byte of the transaction must be read directly from UCBxRXBUF. For all other bytes, follow the workaround.

Code flow for workaround:

1. Enter RX ISR for reading receiving bytes
2. Check if UCSCLLOW.UCBxSTAT == 1
3. If no, repeat step 2 until set.
4. If yes, repeat step 2 for a time period > $3 \times t_{BitClock}$, where $t_{BitClock} = 1/ f_{BitClock}$
5. If window of $3 \times t_{BitClock}$ cycles has elapsed, it is safe to read UCBxRXBUF.

XOSC5 *LFXT1 Module*

Function LF crystal failures may not be properly detected by the oscillator fault circuitry

Description The oscillator fault error detection of the LFXT1 oscillator in low-frequency mode (XTS = 0) may not work reliably, causing a failing crystal to go undetected by the CPU; that is, OFIFG is not set.

Workaround None

Appendix A Prior Revisions

None

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