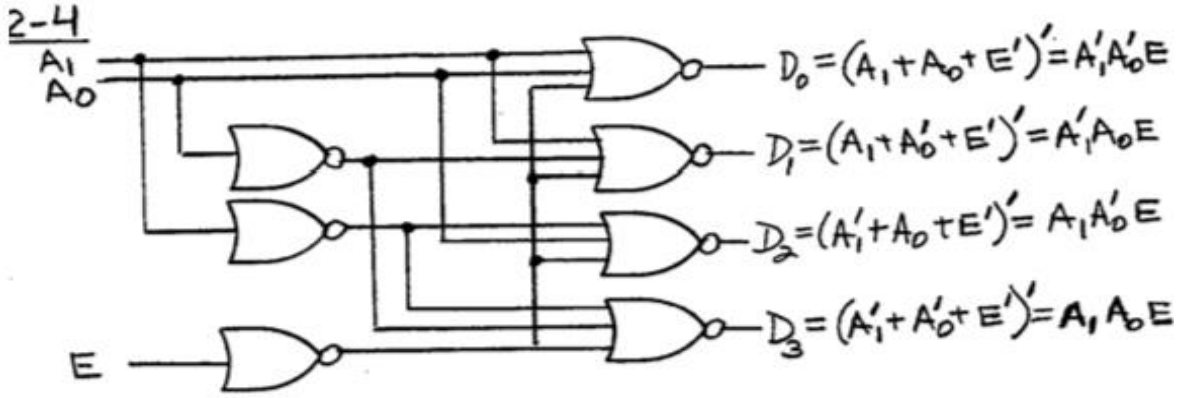
CS 2614: Computer Organization

Homework 6 Solutions

1. Problem 2-4

Draw the logic diagram of a 2-to-4-line decoder with only NOR gates. Include an enable input.

Solution:



2. Problem 2-5

Modify the decoder of Fig. 2-2 so that the circuit is enabled when E = 1 and disabled when E = 0. List the modified truth table.

Solution:

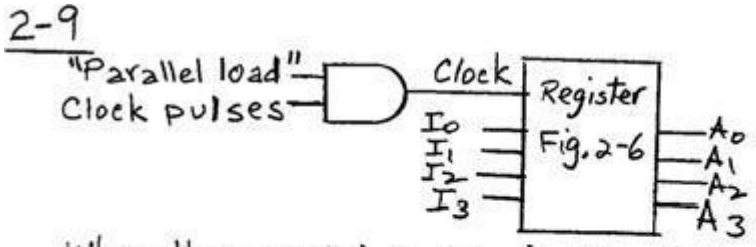
2-5 Remove the inverter from the E input in Fig. 2-2(a).

E	A1	A0	D0	D1	D2	D3
1	1	1	0	0	0	1
1	1	0	0	0	1	0
1	0	1	0	1	0	0
1	0	0	1	0	0	0
0	x	x	0	0	0	0

3. Problem 2-9

Include a two-input AND gate with the register of Fig. 2-6 and connect the gate output to the clock inputs of all the flip-flops. One input of the AND gate receives the clock pulses from the clock pulse generator. The other input of the AND gate provides a parallel load control. Explain the operation of the modified register.

Solution:



When the parallel load input = 1, the clock pulses go through the AND gate and the data inputs are loaded into the register. When the parallel load input = 0, the output of the AND gate remains at 0.

4. Problem 2-10

What is the purpose of the buffer gate in the clock input of the register of Fig. 2-7?

Solution:

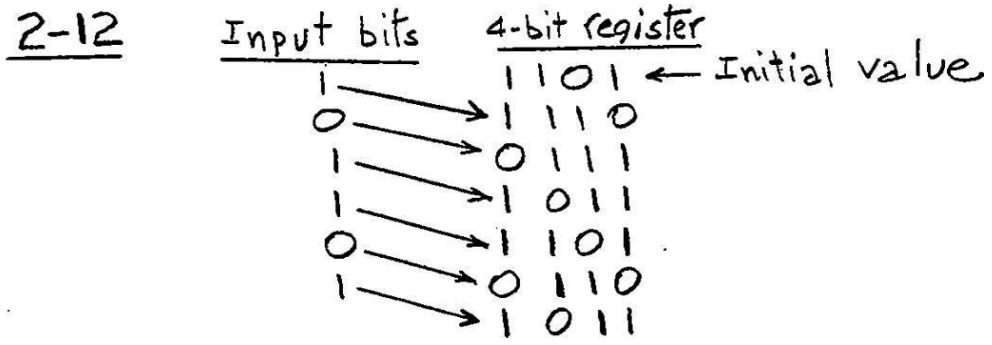
2-10

The buffer gate does not perform logic. It is used for signal amplification of the clock input.

5. Problem 2-12

The content of a 4-bit register is initially 1101. The register is shifted six times to the right with the serial input being 101101. What is the content of the register after each shift?

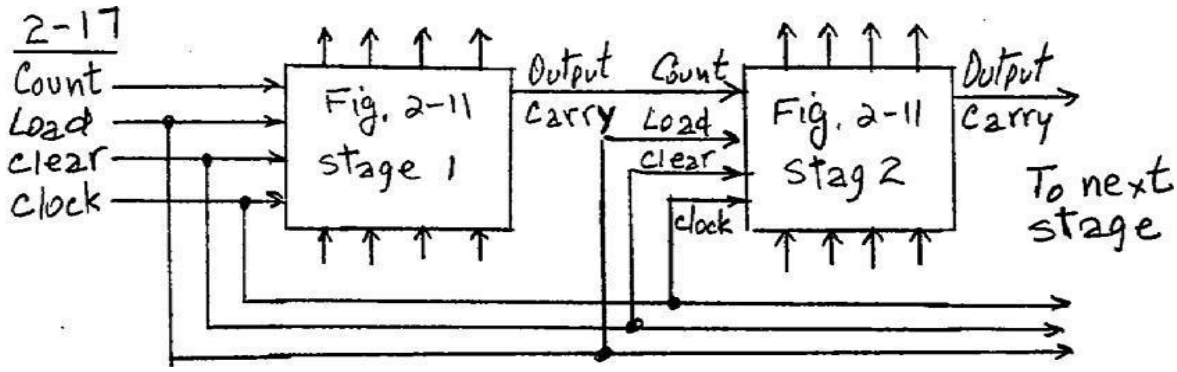
Solution:



6. Problem 2-17

Show the connections between four 4-bit binary counters with parallel load(Fig. 2-11) to produce a 16-bit binary counter with parallel load. Use a block diagram for each 4-bit counter.

Solution:



7. Problem 2-19

The following memory units are specified by the number of words times the number of bits per word. How many address lines and input-output data lines are needed in each case? (a) 2K x 16; (b) 64K x 8; (c) 16M x 32; (d) 4G x 64.

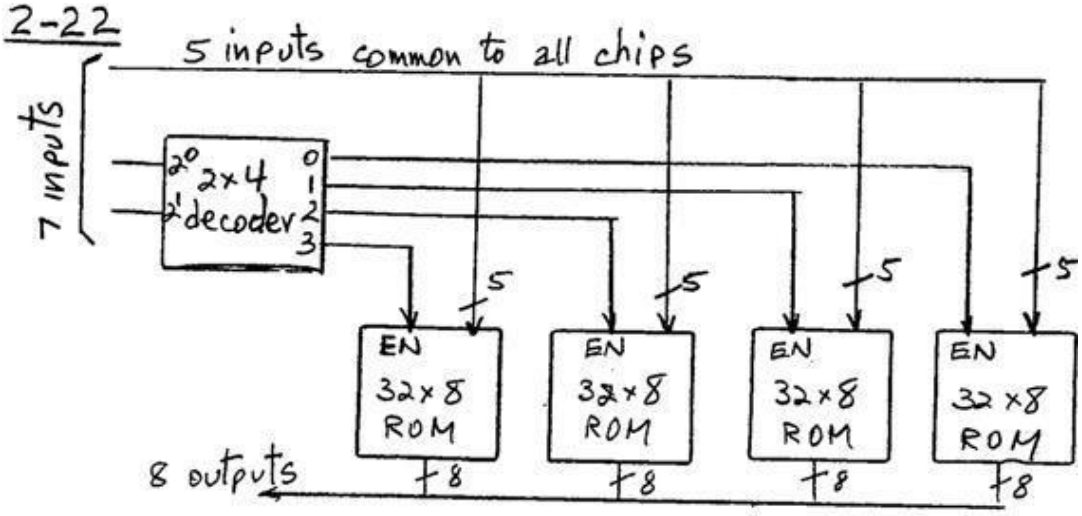
Solution:

	Address lines	Data lines
(a) $2K \times 16 = 2^{11} \times 16$	11	16
(b) $64K \times 8 = 2^{16} \times 8$	16	8
(c) $16M \times 32 = 2^{24} \times 32$	24	32
(d) $4G \times 64 = 2^{32} \times 64$	32	64

8. Problem 2-22

Given a 32 x 8 ROM chip with an enable input, show the external connections necessary to construct a 128 x 8 ROM with four chips and a decoder.

Solution:

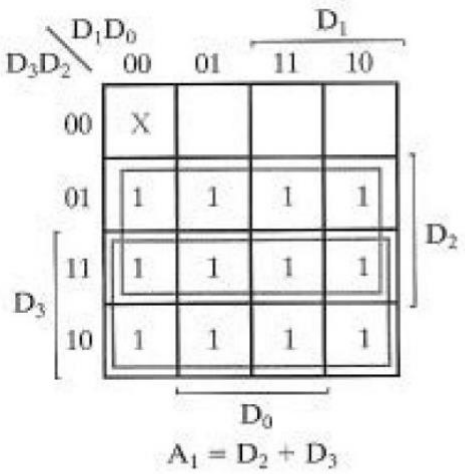


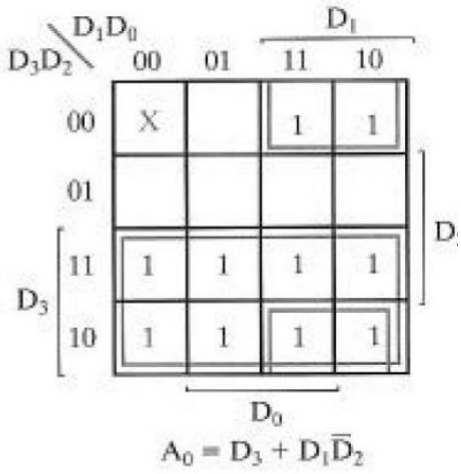
9. A priority encoder is a combinational circuit that implements a priority function. The operation of the priority encoder is such that if two or more inputs are equal to 1 at the same time, the input having the highest priority takes precedence. The truth table for a four-input priority encoder is given below. With the use of X's, this condensed truth table with just five rows represents the same information as the usual 16-row truth table.

Inputs				Outputs		
D_3	D_2	D_1	D_0	A_1	A_0	V
0	0	0	0	X	X	0
0	0	0	1	0	0	1
0	0	1	X	0	1	1
0	1	X	X	1	0	1
1	X	X	X	1	1	1

Determine the logic functions $\underline{A_1}$ and $\underline{A_0}$

Solution:





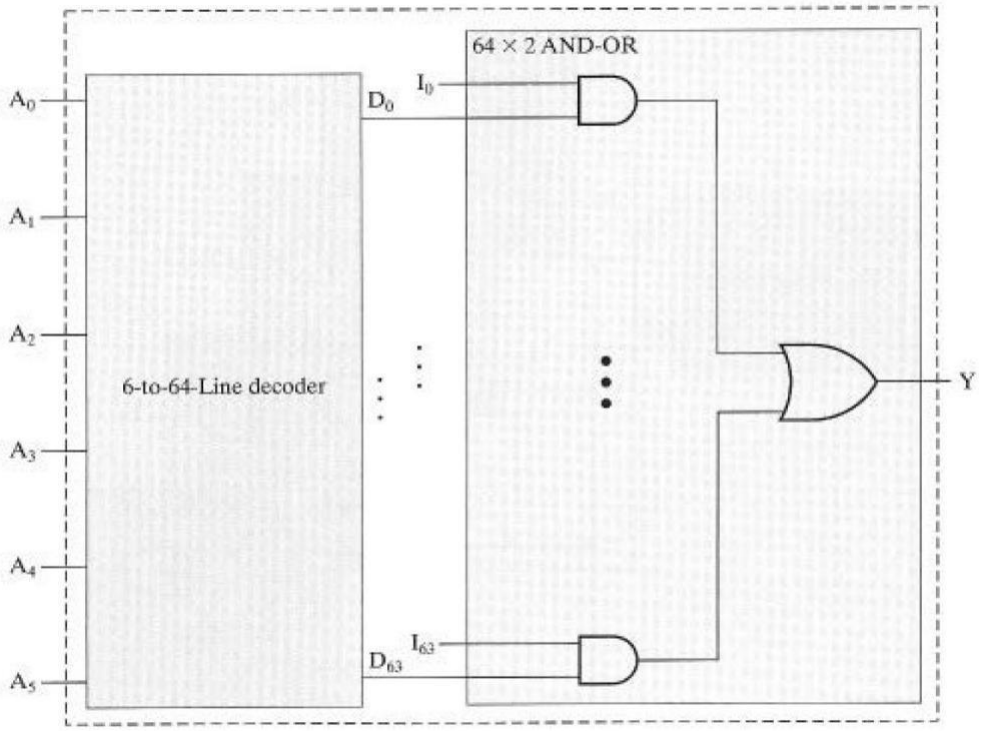
$$A_0 = D_3 + D_1\overline{D}_2$$

$$A_1 = D_2 + D_3$$

$$V = D_0 + D_1 + D_2 + D_3$$

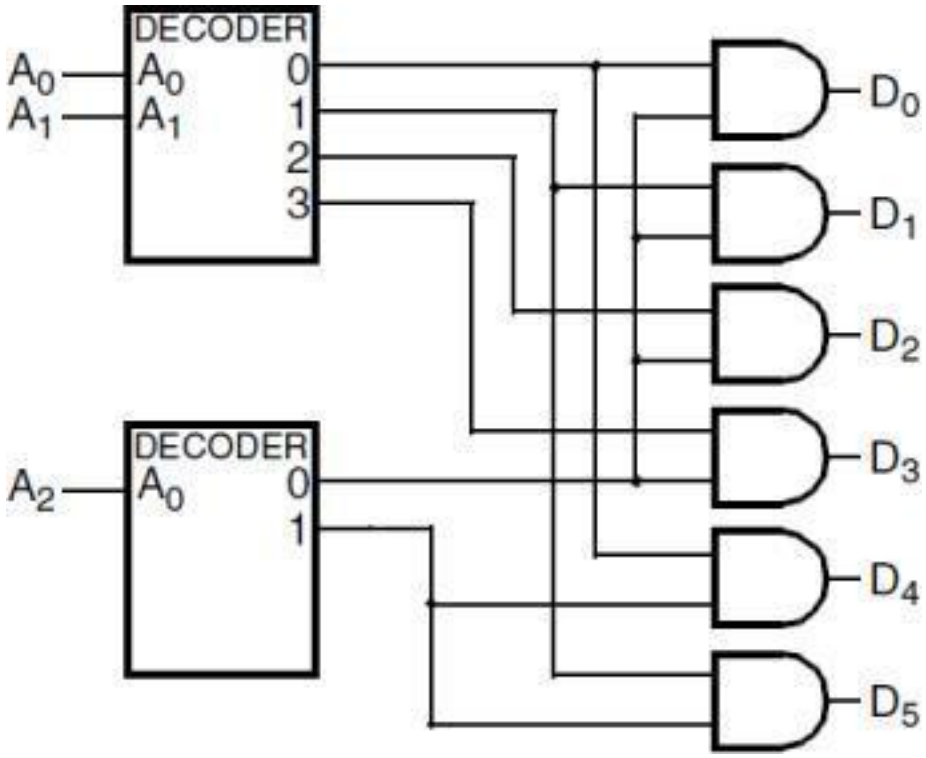
10. Design a 64 x 1 Multiplexer with a <u>6 x 64 decoder</u> and "AND" and "OR" gates.

<u>Solution:</u>



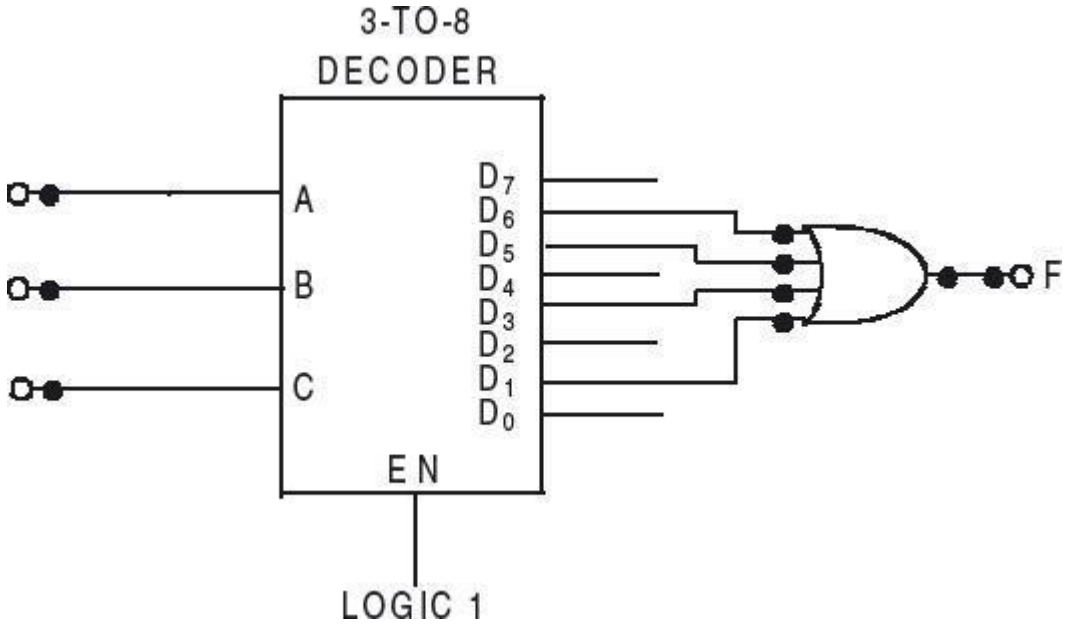
11. A special 3-to-6-line decoder is to be designed. The input codes used are 000 through 101. For a given code applied, the output D_i with i equal to the decimal equivalent of the code is 1 and all other outputs are 0. Design the 3-to-6-line decoder with a 2-to-4-line decoder, a 1-to-2-line decoder, and six 2-input AND gates, such that all decoder outputs are used at least once.

Solution:



12. Implement the function *F (A, B, C)* = ∑ (1,3,5,6) using a decoder.

Solution:



13. Using a decoder and external gates, design the combinational circuit to implement the following Boolean functions. Hint: First, convert the functions to sum of products.

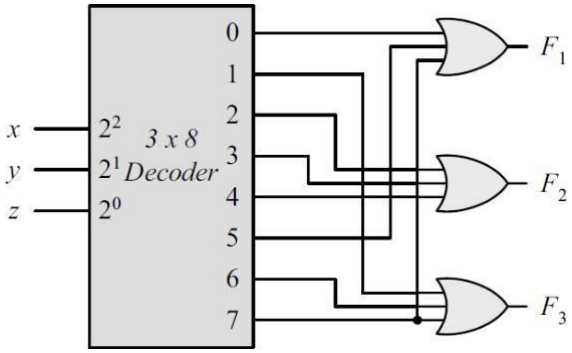
$$F_1 = x'y'z' + xz$$
$$F_2 = xy'z' + x'y$$
$$F_3 = x'y'z + xy$$

Solution:

$$F1 = x(y + y')z + x'y'z' = \sum(0, 5, 7)$$

$$F2 = xy'z' + x'y + x'y(z + z') = \sum(2, 3, 4)$$

$$F3 = x'y'z + xy(z + z') = \sum(1, 6, 7)$$



14. Tabulate the truth table (i.e. contents) for an 8 x 4 ROM that implements the following four Boolean functions. Do not use any hardware other than the ROM.

$$A(X, Y, Z) = \sum (0, 1, 2, 6, 7)$$
$$B(X, Y, Z) = \sum (2, 3, 4, 5, 6)$$
$$C(X, Y, Z) = \sum (2, 6)$$
$$D(X, Y, Z) = \sum (1, 2, 3, 5, 6, 7)$$

Solution:

Input			Output			
X	Y	Z	A	B	C	D
0	0	0	1	0	0	0
0	0	1	1	0	0	1
0	1	0	1	1	1	1
0	1	1	0	1	0	1
1	0	0	0	1	0	0
1	0	1	0	1	0	1
1	1	0	1	1	1	1
1	1	1	1	0	0	1

15. Implement the 3-variable function *F(A, B, C)* = ∑ (0, 2, 4, 7) with a 4 x 1 multiplexer.

Solution:

$$F(A, B, C) = \sum (0,2,4,7)$$

$F(A,B,C) = \Sigma (0,2,4,7)$

A	B	C	F	
0	0	0	1	$F = C'$
0	0	1	0	
0	1	0	1	$F = C'$
0	1	1	0	
1	0	0	1	$F = C'$
1	0	1	0	
1	1	0	0	$F = C$
1	1	1	1