

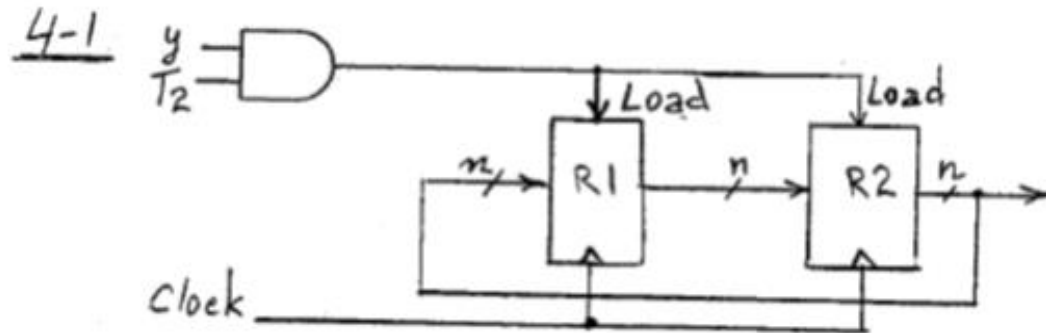
CS 2614: Computer Organization  
Homework # 7 Solutions

1. Problem 4-1

Show the block diagram of the hardware (similar to Fig. 4-2a) that implements the following register transfer statement:

$$yT_2: R2 \leftarrow R1, R1 \leftarrow R2$$

Solution:



2. Problem 4-4

What has to be done to the bus system of Fig. 4-3 to be able to transfer information from any register to any other register? Specifically, show the connections that must be included to provide a path from the outputs of register C to the inputs of register A.

Solution:

4-4

Connect the 4-line common bus to the four inputs of each register,

Provide a "load" control input in each register,

Provide a clock input for each register.

To transfer from register C to register A:

Apply  $S_1, S_0 = 10$  (to select C for the bus,)

Enable the load input of A

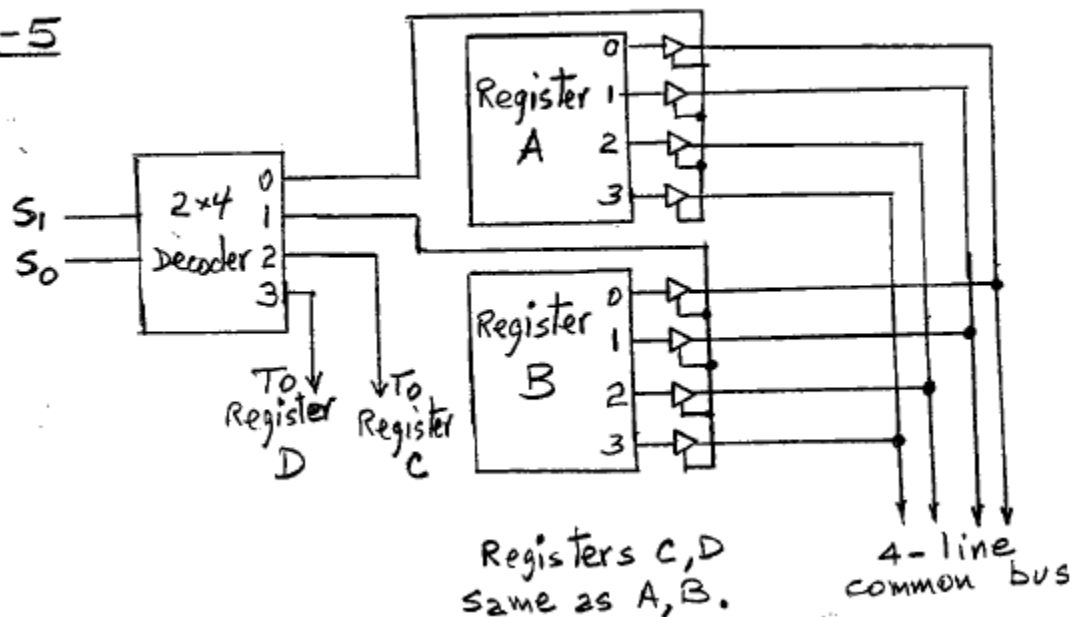
Apply a clock pulse.

3. Problem 4-5

Draw a diagram of a bus system similar to the one shown in Fig. 4-3, but use three-state buffers and a decoder instead of the multiplexers.

Solution:

4-5



4. Problem 4-8

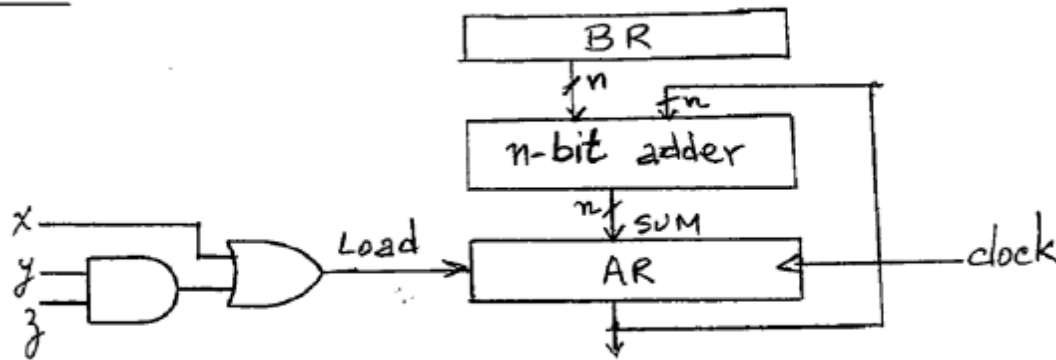
Draw the block diagram for the hardware that implements the following statements:

$$x + yz: AR \leftarrow AR + BR$$

where  $AR$  and  $BR$  are two  $n$ -bit registers and  $x$ ,  $y$ , and  $z$  are control variables. Include the logic gates for the control function. (Remember that the symbol  $+$  designates an OR operation in a control or Boolean function but that it represents an arithmetic plus in a microoperation.)

Solution:

4-8



5. Problem 4-11

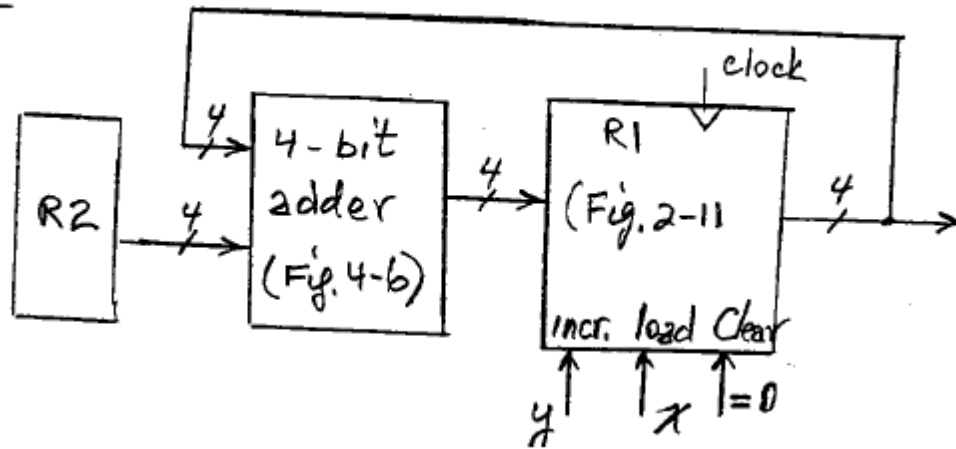
Using a 4-bit counter with parallel load as in Fig. 2-11 and a 4-bit adder as in Fig. 4-6, draw a block diagram that shows how to implement the following statements:

$$\begin{array}{ll} x: R1 \leftarrow R1 + R2 & \text{Add } R2 \text{ to } R1 \\ x'y: R1 \leftarrow R1 + 1 & \text{Increment } R1 \end{array}$$

where  $R1$  is a counter with parallel load and  $R2$  is a 4-bit register.

Solution:

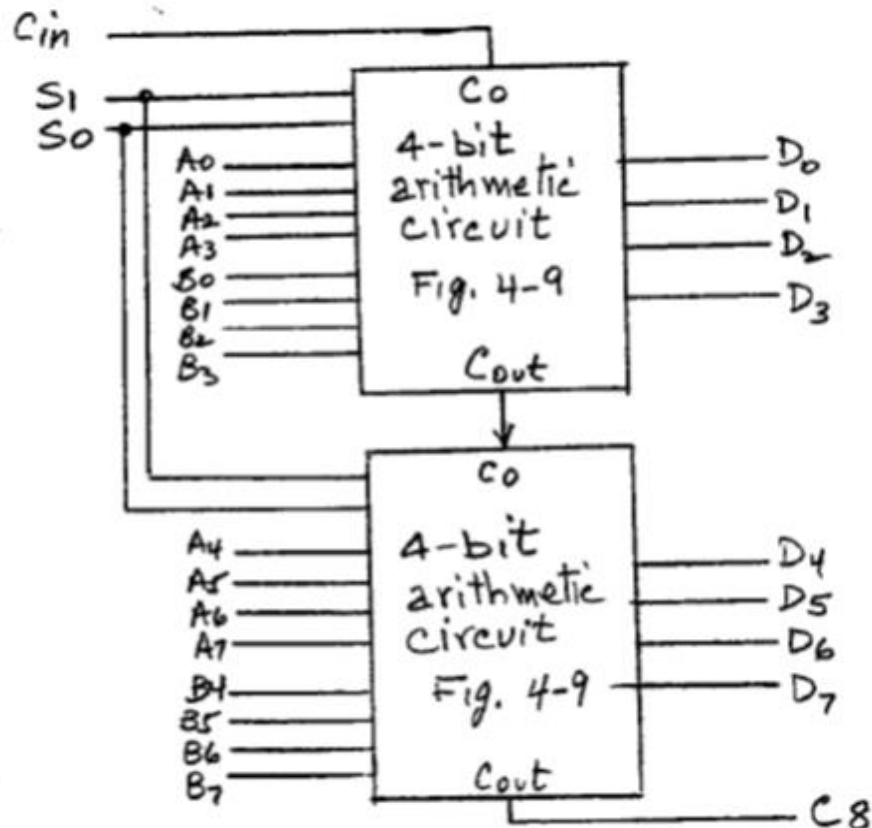
4-11



6. Problem 4-14

Assume that the 4-bit arithmetic circuit of Fig. 4-9 is enclosed in one IC package. Show the connections among two such ICs to form an 8-bit arithmetic circuit.

Solution:

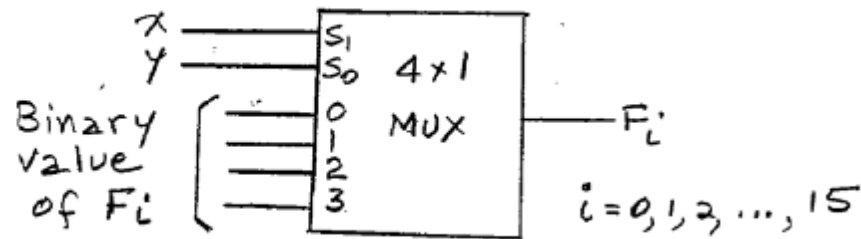


7. Problem 4-16

Derive a combinational circuit that selects and generates any of the 16 logic functions listed in Table 4-5.

Solution:

4-16



8. Problem 4-18

Register A holds the 8-bit binary 11011001. Determine the B operand and the logic microoperation to be performed in order to change the value in A to:

- a. 01101101
- b. 11111101

Solution:

4-18

$$\begin{array}{rcl} (2) & A = 11011001 & \\ & B = 10110100 \oplus & \\ A \leftarrow A \oplus B & 01101101 & \end{array}$$

$$\begin{array}{rcl} A = 11011001 & & \\ B = 11111101 \text{ (OR)} & & \\ \hline 11111101 & A \leftarrow A \vee B & \end{array}$$

9. Problem 4-20

An 8-bit register contains the binary value 10011100. What is the register value after an arithmetic shift right? Starting from the initial number 10011100, determine the register value after an arithmetic shift left, and state whether there is an overflow.

Solution:

4-20  $R = 10011100$

Arithmetic shift right:  $11001110$

Arithmetic shift left:  $00111000$

overflow because a  
negative number changed  
to positive

#### 10. Problem 4-23

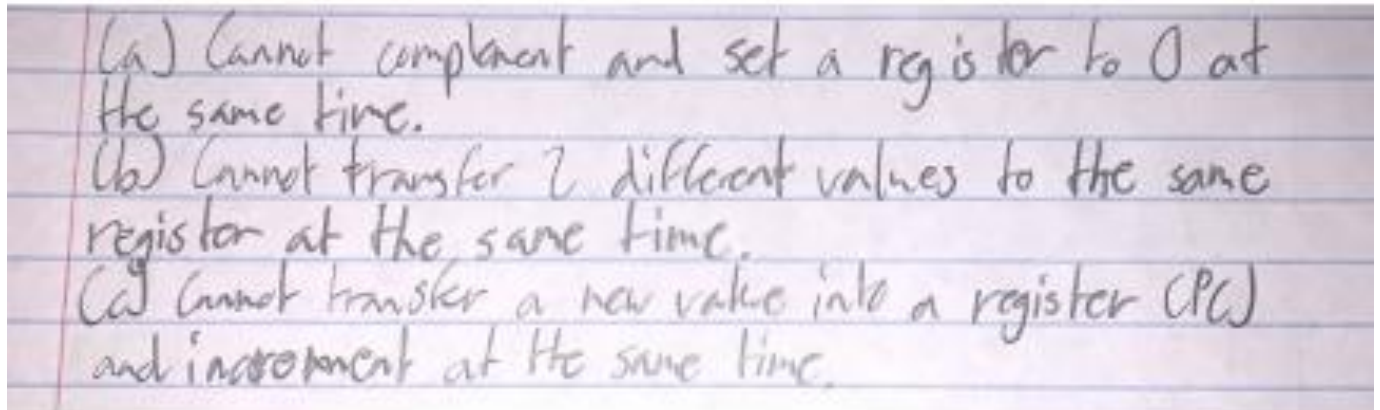
What is wrong with the following register transfer statements?

a.  $xT: AR \leftarrow \overline{AR}, AR \leftarrow 0$

b.  $yT: R1 \leftarrow R2, R1 \leftarrow R3$

c.  $zT: PC \leftarrow AR, PC \leftarrow PC + 1$

**Solution:**



(a) Cannot complement and set a register to 0 at the same time.  
(b) Cannot transfer 2 different values to the same register at the same time.  
(c) Cannot transfer a new value into a register (PC) and increment at the same time.

11. Given the 16-bit operand 00001111 10101010, what operation must be performed and what operand must be used

- to clear all even bit positions to 0? (Assume bit positions are 15 through 0 from left to right.)
- to set the leftmost 4 bits to 1?
- to complement the center 8 bits?

**Solutions:**

(a) All the even bit positions from left to right: **14, 12, 10, 8, 6, 4, 2, 0**

To clear all even bit position, perform AND operation using **1010 1010 1010 1010**

(b) The leftmost 4 bits are: **15, 14, 13, 12**



To set the leftmost 4 bits to 1, perform OR operation using **1111 0000 0000 0000**

(c) The center 8 bits are: **11, 10, 9, 8, 7, 6, 5, 4**

To complement the center 8 bits, perform XOR operation using, **0000 1111 1111 0000**

12. A switch-tail ring counter (Johnson counter) uses the complement of the serial output of a right shift register as its serial input.
- Starting from an initial state of 0000, list the sequence of states after each shift until the register returns to 0000.
  - Beginning in state 00 ... 0. how many states are there in the count sequence of an  $n$ -bit switch-tail counter?

**Solution:**

a) 0000 → 1000 → 1100 → 1110 → 1111 → 0111 → 0011 → 0001 → 0000

b) # of States =  $2n$

13. Two conditional register transfer statements are given (R1 is unchanged if condition fails):

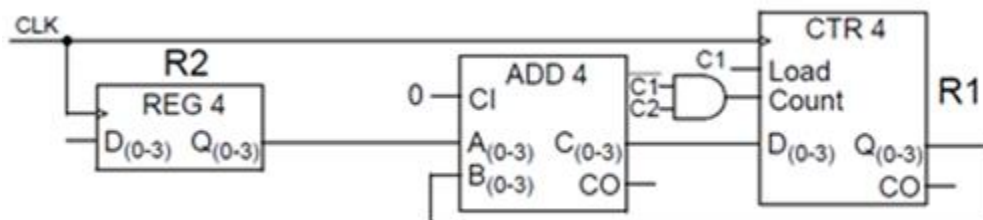
**C1 :  $R1 \leftarrow R1 + R2$     Add R2 to R1**

**C1'C2:  $R1 \leftarrow R1 + 1$     Increment R1**

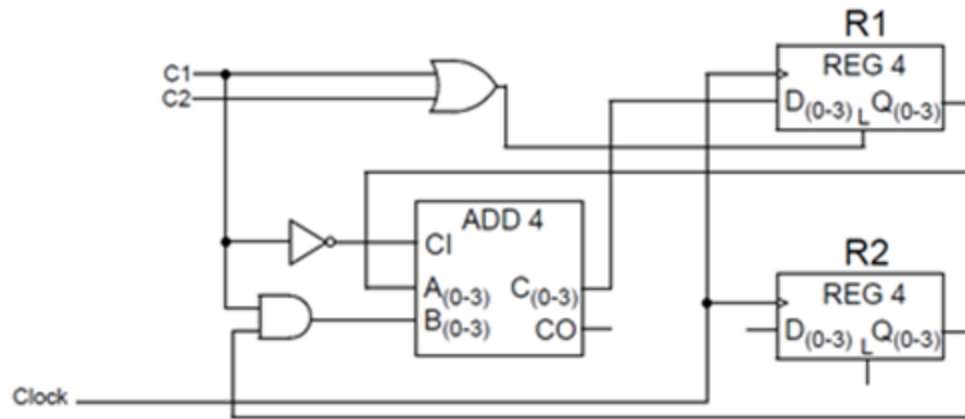
- Using a 4-bit counter with parallel load and a 4-bit adder, draw the logic diagram that implements these register transfers.
- Repeat part (a) using a 4-bit adder plus external gates as needed. Compare with the implementation in part (a).

**Solution:**

a.



b.



14. Show the diagram of the hardware that implements the register transfer statement

C3:  $R2 \leftarrow R1; R1 \leftarrow R2$

Solution:

