Tips about PCB design: Part 2 - Single-card grounding for multicard systems

Walt Kester - December 07, 2010

Most ADC, DAC, and other mixed-signal device data sheets discuss grounding relative to a single PCB, usually the manufacturer's own evaluation board. This has been a source of confusion in trying to apply the principles described here to multicard or multi-ADC/DAC systems.

The recommendation is usually to split the PCB ground plane into an analog plane and a digital plane. It is then further recommended that the AGND and DGND pins of a converter be tied together and that the analog ground plane and digital ground planes be connected at that same point as shown in **Figure C.14 below**. This essentially creates the system "star" ground at the mixed-signal device.

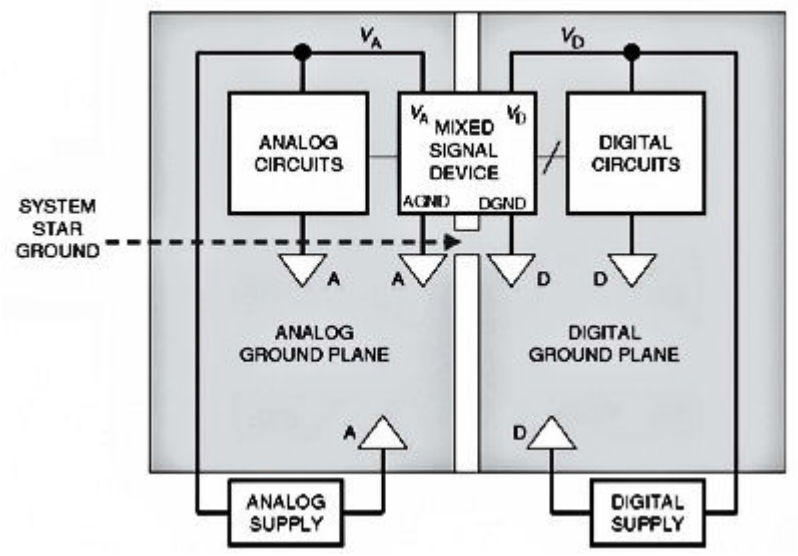

Figure C.14: Grounding mixed-signal ICs: single PC board (typical evaluation/test board).

All noisy digital currents flow through the digital power supply to the digital ground plane and back to the digital supply; they are isolated from the sensitive analog portion of the board. The system star ground occurs where the analog and digital ground planes are joined together at the mixed-signal device.

This approach will generally work in a simple system with a single PCB and single ADC/DAC, but it is not optimum for multicard mixed-signal systems. In systems having several ADCs or DACs on different PCBs (or on the same PCB, for that matter), the analog and digital ground planes become connected at several points, creating the possibility of ground loops and making a single-point "star" ground system impossible.

For these reasons, this grounding approach is not recommended for multicard systems, and the approach previously discussed should be used for mixed-signal ICs with low digital currents.

Grounding Mixed-Signal Low Digital Currents

Figure C.15 below summarizes the approach previously described for grounding a mixed-signal device which has low digital currents. The analog ground plane is not corrupted because the small digital transient currents flow in the small loop between VD, the decoupling capacitor, and DGND (shown as a heavy line).

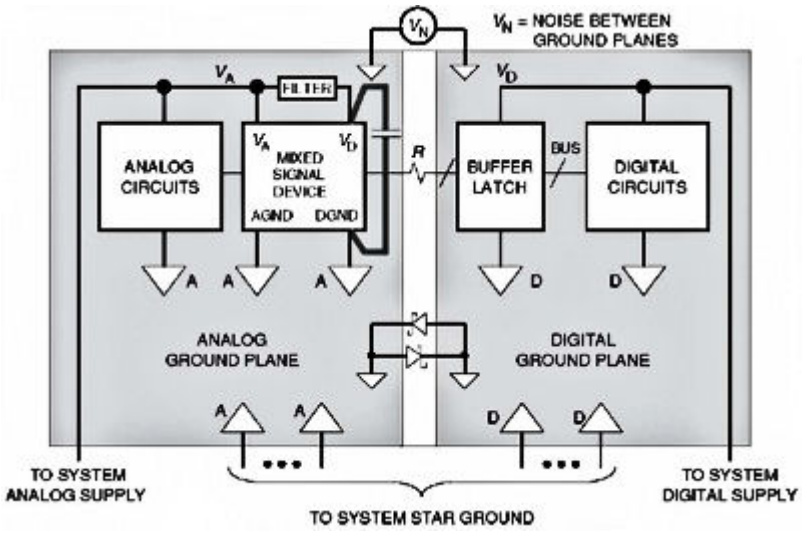

Figure C.15: Grounding mixed-signal ICs with low internal digital currents: multiple PC boards.

The mixed-signal device is for all intents and purposes treated as an analog component. The noise VN between the ground planes reduces the noise margin at the digital interface but is generally not harmful if kept less than 300 mV by using a low-impedance digital ground plane all the way back to the system star ground.

However, mixed-signal devices such as sigma-delta ADCs, codecs, and DSPs with on-chip analog functions are becoming more and more digitally intensive. Along with the additional digital circuitry come larger digital currents and noise. For example, a sigma-delta ADC or DAC contains a complex digital filter which adds considerably to the digital current in the device.

The method previously discussed depends on the decoupling capacitor between VD and DGND to keep the digital transient currents isolated in a small loop. However, if the digital currents are significant enough and have components at DC or low frequencies, the decoupling capacitor may have to be so large that it is impractical.

Any digital current that fl ows outside the loop between VD and DGND must flow through the analog ground plane. This may degrade performance, especially in high-resolution systems.

It is difficult to predict what level of digital current flowing into the analog ground plane will become unacceptable in a system. All we can do at this point is to suggest an alternative grounding method which may yield better performance.

Grounding Mixed-Signal Devices with High Digital Currents

An alternative grounding method for a mixed-signal device with high levels of digital currents is

shown in **Figure C.16 below**. The AGND of the mixed-signal device is connected to the analog ground plane, and the DGND of the device is connected to the digital ground plane.

The digital currents are isolated from the analog ground plane, but the noise between the two ground planes is applied directly between the AGND and DGND pins of the device. For this method to be successful, the analog and digital circuits within the mixed signal device must be well isolated. The noise between AGND and DGND pins must not be large enough to reduce internal noise margins or cause corruption of the internal analog circuits.

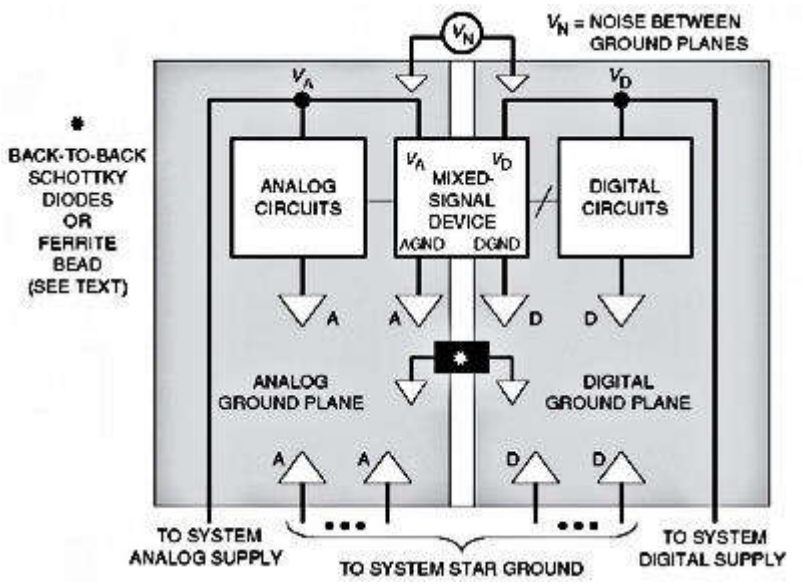

Figure C.16: Grounding alternative for mixed-signal ICs with high digital currents: multiple PC boards

Figure C.16 shows optional Schottky diodes (back-to-back) or a ferrite bead connecting the analog and digital ground planes. The Schottky diodes prevent large DC voltages or low-fre-quency voltage spikes from developing across the two planes.

These voltages can potentially damage the mixed-signal IC if they exceed 300 mV because they appear directly between the AGND and DGND pins. As an alternative to the back-to-back Schottky diodes, a ferrite bead provides a DC connection between the two planes but isolates them at frequencies above a few MHz where the ferrite bead becomes resistive.

This protects the IC from DC voltages between AGND and DGND, but the DC connection provided by the ferrite bead can introduce unwanted DC ground loops and might not be suitable for high-resolution systems.

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Grounding DSPs with Internal PLLs

As if dealing with mixed-signal ICs with AGND and DGNDs wasn’t enough, DSPs such as the ADSP21160 SHARC with internal phase-locked-loops (PLLs) raise issues with respect to proper grounding. The ADSP-21160 PLL allows the internal core clock (determines the instruction cycle time) to operate at a user-selectable ratio of 2, 3, or 4 times the external clock frequency, CLKIN.

The CLKIN rate is the rate at which the synchronous external ports operate. Although this allows using a lower-frequency external clock, care must be taken with the power and ground connections to the internal PLL, as shown in **Figure C.17 below.**

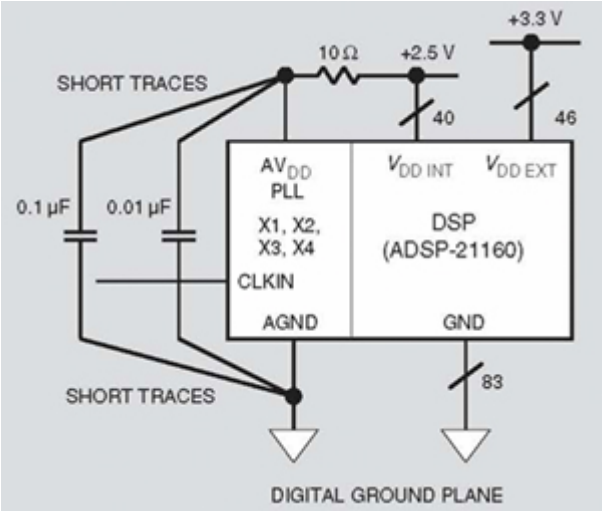

Figure C.17: Grounding DSPs with internal phase-locked loops (PLLs).

To prevent internal coupling between digital currents and the PLL, the power and ground connections to the PLL are brought out separately on pins labeled AVDD and AGND, respectively. The AVDD 2.5 V supply should be derived from the VDD INT 2.5 V supply using the fi lter network as shown.

This ensures a relatively noise-free supply for the internal PLL. The AGND pin of the PLL should be connected to the digital ground plane of the PC board using a short trace. The decoupling capacitors should be routed between the AVDD pin and AGND pin using short traces.

No single grounding method will guarantee optimum performance 100% of the time. This section has presented a number of possible options, depending upon the characteristics of the particular mixed-signal devices in question. It is helpful, however, to provide for as many options as possible when laying out the initial PC board.

It is mandatory that at least one layer of the PC board be dedicated to ground plane. The initial board layout should provide for nonoverlapping analog and digital ground planes, but pads and vias should be provided at several locations for the installation of back-to-back Schottky diodes or ferrite beads, if required. Pads and vias should also be provided so that the analog and digital ground planes can be connected together with jumpers if required.

The AGND pins of mixed-signal devices should in general always be connected to the analog ground plane. An exception to this are DSPs such as the ADSP-21160 SHARC, which have internal phase-locked-loops (PLLs). The ground pin for the PLL is labeled AGND, but should be directly connected to the digital ground plane for the DSP. See **Figure C.18 below** for a general summary of grounding philosophy.

- There is no single grounding method which is guaranteed to work 100% of the time
- Different methods may or may not give the same levels of performance
- At least one layer on each PC board MUST be dedicated to ground plane
- Do initial layout with split analog and digital ground planes
- Provide pads and vias on each PC board for back-to-back Schottky diodes and optional ferrite beads to connect the two planes
- Provide "jumpers" so that DGND pins of mixed-signal devices can be connected to AGND pins (analog ground plane) or to digital ground plane. (AGND of PLLs in DSPs should be connected to digital ground plane)
- Provide pads and vias for "jumpers" so that analog and digital ground planes can be joined together at several points on each PC board
- Follow recommendations on mixed signal device data sheet

Figure C.18: Grounding philosophy summary.

PCB Layout Guidelines for Mixed-Signal

It is evident that noise can be minimized by paying attention to the system layout and preventing different signals from interfering with each other. High-level analog signals should be separated from low-level analog signals, and both should be kept away from digital signals.

We have seen elsewhere that in waveform sampling and reconstruction systems the sampling clock (which is a digital signal) is as vulnerable to noise as any analog signal but is as liable to cause noise as any digital signal and so must be kept isolated from both analog and digital systems.

If clock driver packages are used in clock distribution, only one frequency clock should be passed through a single package. Sharing drivers between clocks of different frequencies in the same package will produce excess jitter and crosstalk and degrade performance.

The ground plane can act as a shield where sensitive signals cross. **Figure C.19 below** shows a good layout for a data acquisition board where all sensitive areas are isolated from each other and signal paths are kept as short as possible. While real life is rarely as tidy as this, the principle remains a valid one.

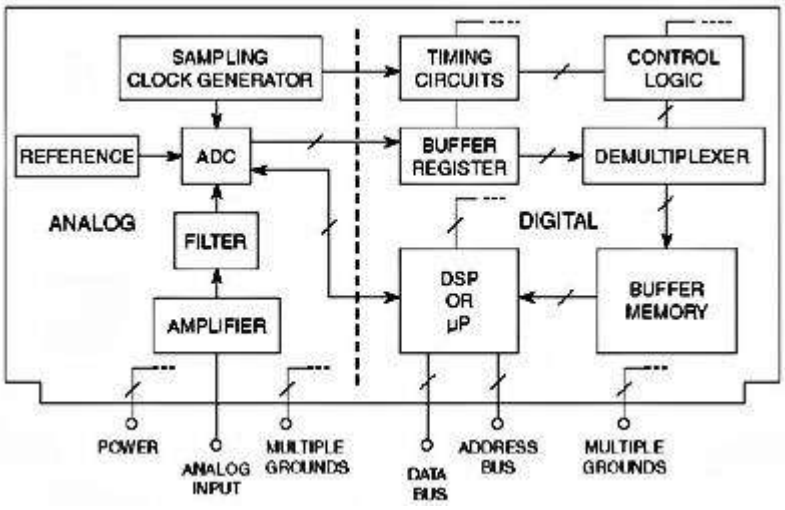

Figure C.19: Analog and digital circuits should be partitioned on PCB layout.

There are a number of important points to be considered when making signal and power connections. First, a connector is one of the few places in the system where all signal conductors must run in parallel; it is therefore imperative to separate them with ground pins (creating a Faraday shield) to reduce coupling between them.

Multiple ground pins are important for another reason: They keep down the ground impedance at the junction between the board and the backplane. The contact resistance of a single pin of a PCB connector is quite low (on the order of 10 mΩ) when the board is new; as the board gets older, the contact resistance is likely to rise and the board's performance may be compromised.

It is therefore well worthwhile to allocate extra PCB connector pins so that there are many ground connections (perhaps 30–40% of all the pins on the PCB connector should be ground pins). For similar reasons there should be several pins for each power connection, although there is no need to have as many as there are ground pins.

Analog Devices and other manufacturers of high-performance, mixed-signal ICs offer evaluation boards to assist customers in their initial evaluations and layout. ADC evaluation boards generally contain an on-board low-jitter sampling clock oscillator, output registers, and appropriate power and signal connectors. They also may have additional support circuitry such as the ADC input buffer amplifier and external reference.

The layout of the evaluation board is optimized in terms of grounding, decoupling, and signal routing and can be used as a model when laying out the ADC PC board in the system. The actual evaluation board layout is usually available from the ADC manufacturer in the form of computer CAD files (Gerber files). In many cases, the layout of the various layers appears on the data sheet for the device.

Dealing with skin effects

At high frequencies, also consider skin effect, where inductive effects cause currents to fl ow only in the outer surface of conductors. Note that this is in contrast to the earlier discussions on DC resistance of conductors.

The skin effect has the consequence of increasing the resistance of a conductor at high frequencies. Note also that this effect is separate from the increase in impedance due to the effects of the self-inductance of conductors as frequency is increased.

Skin effect is quite a complex phenomenon, and detailed calculations are beyond the scope of this discussion. However, a good approximation for copper is that the skin depth in centimeters is 661./ f (f in Hz).

A summary of the skin effect within a typical PCB conductor foil is shown in ***Figure C.20 below.*** Note that this copper conductor cross-sectional view assumes looking into the side of the conducting trace.

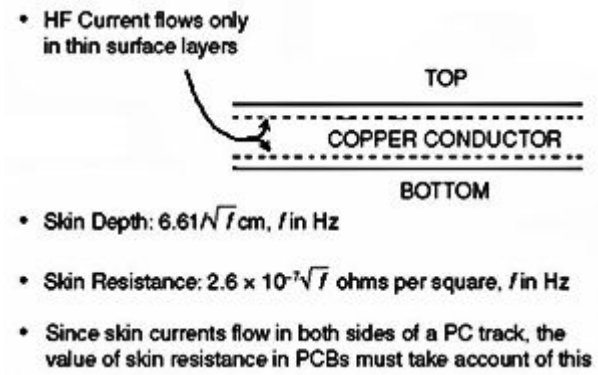

Figure C.20: Skin depth in a PC conductor.

Assuming that skin effects become important when the skin depth is less than 50% of the thickness of the conductor, this tells us that for a typical PC foil, we must be concerned about skin effects at frequencies above approximately 12 MHz.

Where skin effect is important, the resistance for copper is 26 10 7 f ohms per square. (f in Hz). This formula is invalid if the skin thickness is greater than the conductor thickness (i.e., at DC or low frequencies). **Figure C.21 below** illustrates a case of a PCB conductor with current flow, as separated from the ground plane underneath.

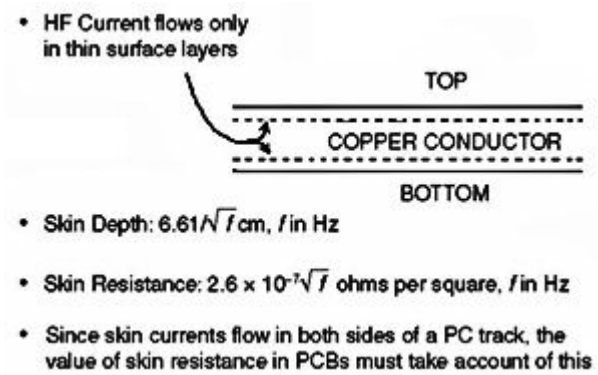

Figure C.21: Skin effect with PC conductor and ground plane.

In this diagram, note the (dotted) regions of high-frequency current flow, as reduced by the skin effect. When calculating skin effect in PCBs, it is important to remember that current generally flows in both sides of the PC foil (this is not necessarily the case in microstrip lines; see below), so the resistance per square of PC foil may be half the above value.

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Transmission line effects

We earlier considered the benefits of outward and return signal paths being close together so that inductance is minimized. As shown in **Figure C.22 below**, when a high-frequency signal flows in a PC track running over a ground plane, the arrangement functions as a micro-strip transmission line, and the majority of the return current flows in the ground plane underneath the line.

Figure C.22 below shows the general parameters for a microstrip transmission line, given the conductor width **w**, dielectric thickness **h**, and the dielectric constant **Er**.

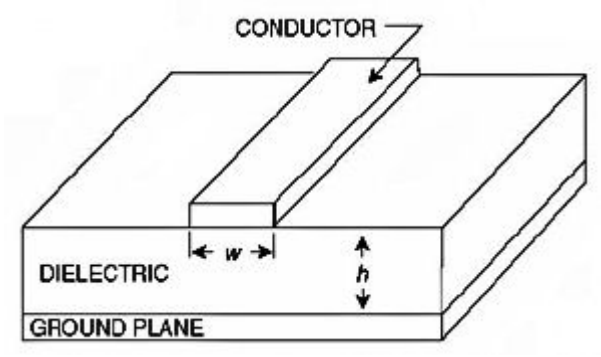

Figure C.22: A PCB microstrip transmission line is an example of a controlled impedance conductor pair.

The characteristic impedance of such a microstrip line will depend on the width of the track and the thickness and dielectric constant of the PCB material. Designs of microstrip lines are covered in more detail later in this series.

For most DC and lower-frequency applications, the characteristic impedance of PCB traces will be relatively unimportant. Even at frequencies where a track over a ground plane behaves as a transmission line, it is not necessary to worry about its characteristic impedance or proper termination if the free space wavelengths of the frequencies of interest are greater than 10 times the length of the line.

However, at VHF and higher frequencies, it is possible to use PCB tracks as microstrip lines within properly terminated transmission systems. Typically the microstrip will be designed to match standard coaxial cable impedances, such as 50 Ω, 75 Ωor 100 Ω, simplifying interfacing.

Note that if losses in such systems are to be minimized, the PCB material must be chosen for low high-frequency losses. This usually means the use of Teflon or some other comparably low-loss PCB material. Often, though, the losses in short lines on cheap glass-fiber board are small enough to be quite acceptable.

Being careful with Ground Plane Breaks

Wherever there is a break in the ground plane beneath a conductor, the ground plane return current must by necessity fl ow around the break. As a result, both the inductance and the vulnerability of the circuit to external fields are increased. This situation is diagrammed **in Figure C.23 below**, where conductors A and B must cross one another.

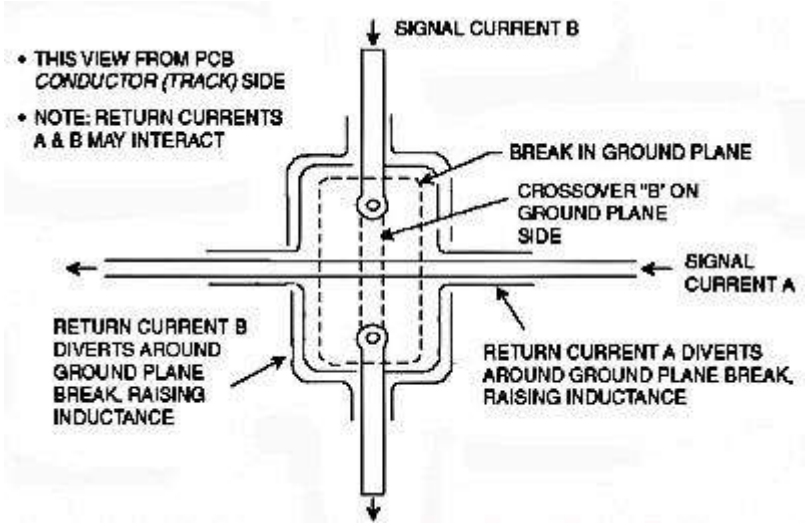

Figure C.23: A ground plane break raises circuit inductance and increases vulnerability to external fields.

Where such a break is made to allow a cross-over of two perpendicular conductors, it would be far better if the second signal were carried across both the first and the ground plane by means of a piece of wire or a resistor.

The ground plane then acts as a shield between the two signal conductors, and the two ground return currents, flowing in opposite sides of the ground plane as a result of skin effects, do not interact.

With a multilayer board, both the crossover and the continuous ground plane can be accommodated without the need for a wire link. Multilayer PCBs are expensive and harder to troubleshoot than more simple double-sided boards, but do offer even better shielding and signal routing. The principles involved remain unchanged but the range of layout options is increased.

The use of double-sided or multilayer PCBs with at least one continuous ground plane is undoubtedly one of the most successful design approaches for high-performance, mixed-signal circuitry.

Often the impedance of such a ground plane is sufficiently low to permit the use of a single ground plane for both analog and digital parts of the system. However, whether or not this is possible does depend on the resolution and bandwidth required and the amount of digital noise present in the system.

Ground Isolation Techniques

Although the use of ground planes does lower impedance and helps greatly in lowering ground noise, there may still be situations where a prohibitive level of noise exists. In such cases, the use of ground error minimization and isolation techniques can be helpful.

Another illustration of a common ground impedance coupling problem is shown in **Figure C.24 below**.

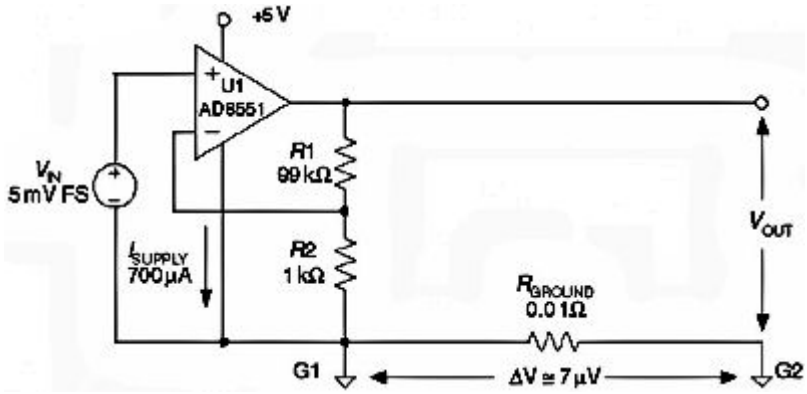

Figure C.24: Unless care is taken, even small common ground currents can degrade precision amplifier accuracy.

In this circuit a precision gain-of-100 preamp amplifies a low-level signal VIN, using an AD8551 chopper-stabilized amplifier for best DC accuracy.

At the load end, the signal VOUT is measured with respect to G2, the local ground. Because of the small 700 μA ISUPPLY of the AD8551 flowing between G1 and G2, there is a 7 μV ground error—about seven times the typical input offset expected from the op amp.

This error can be avoided by routing the negative supply pin current of the op amp back to star ground G2 as opposed to ground G1 by using a separate trace. This step eliminates the G1-G2 path power supply current and so minimizes the ground leg voltage error. Note that there will be little error developed in the "hot" VOUT lead so long as the current drain at the load end is small.

In some cases, there may be simply unavoidable ground voltage differences between a source signal and the load point where it is to be measured. Within the context of this "same-board" discussion, this might require rejecting ground error voltages of several tens of mV. Or, should the source signal originate from an "off-board" source, the magnitude of the common-mode voltages to be rejected can easily rise into a several volt range (or even tens of volts).

Fortunately, full signal transmission accuracy can still be accomplished in the face of such high-noise voltages by employing a principle discussed earlier. This is the use of a differential input, ground isolation amplifier.

The ground isolation amplifier minimizes the effect of ground error voltages between stages by processing the signal in differential fashion, thereby rejecting common-mode voltages by a substantial margin (typically 60 dB or more). Note, however, that this approach is only effective for very low-frequency signals.

Two ground isolation amplifier solutions are shown in **Figure C.25 below**. This diagram can alternately employ either the AD629 to handle CM voltages up to 270 V or the AMP03, which is suitable for CM voltages up to 20 V.

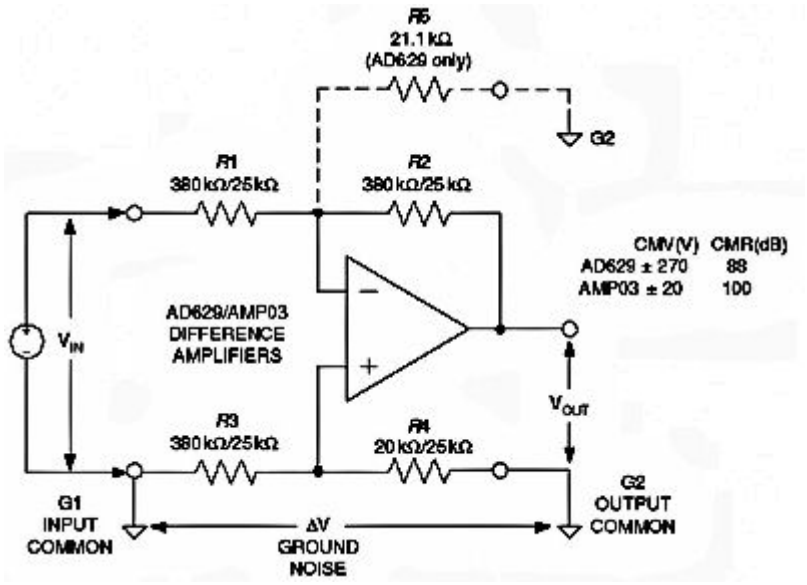

Figure C.25: A differential input ground isolating amplifier allows high transmission accuracy by rejecting ground noise voltage between source (G1) and measurement (G2) grounds.

In the circuit, input voltage VIN is referred to G1 but must be measured with respect to G2. With the use of a high CMR unity-gain difference amplifier, the noise voltage ΔV existing between these two grounds is easily rejected.

The AD629 offers a typical CMR of 88 dB, while the AMP03 typically achieves 100 dB. In the AD629, the high CMV rating is done by a combination of high CM attenuation, followed by differential gain, realizing a net differential gain of unity. The AD629 uses the first listed value resistors noted in the fi gure for R1–R5.

The AMP03 operates as a precision four-resistor differential amplifier using the 25 kΩ value R1–R4 resistors noted. Both devices are complete, one package solutions to the ground-isolation amplifier.

This scheme allows relative freedom from tightly controlling ground drop voltages or running additional and/or larger PCB traces to minimize such error voltages. Note that it can be implemented with either the fixed gain difference amplifiers shown or with a standard in amp IC, configured for unity gain. The AD623, for example, also allows single-supply use. In any case, signal polarity is also controllable by simple reversal of the difference amplifi er inputs.

In general terms, transmitting a signal from one point on a PCB to another for measurement or further processing can be optimized by two key interrelated techniques. These are the use of high impedance, differential signal handling techniques. The high impedance loading of an in amp minimizes voltage drops, and differential sensing of the remote voltage minimizes sensitivity to ground noise.

When the further signal processing is A/D conversion, these transmission criteria can be implemented without adding a differential ground isolation amplifier stage. Simply select an ADC that operates differentially. The high input impedance of the ADC minimizes load sensitivity to the PCB wiring resistance.

In addition, the differential input feature allows the output of the source to be sensed directly at the source output terminals (even if single-ended). The CMR of the ADC then eliminates sensitivity to noise voltages between the ADC and source grounds.

An illustration of this concept using an ADC with high-impedance differential inputs is shown in **Figure C.26**. Note that the general concept can be extended to virtually any signal source, driving any load. All loads, even single-ended ones, become differential input by adding an appropriate differential input stage.

The differential input can be provided by either a fully developed high Z in amp or, in many cases, it can be a simple subtractor stage op amp, such as **Figure C.25**.

To read **Part 1**, go to "**Dealing with harmful PCB effects**."
Next in Part 3: **Static and dynamic PCB effects.**

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