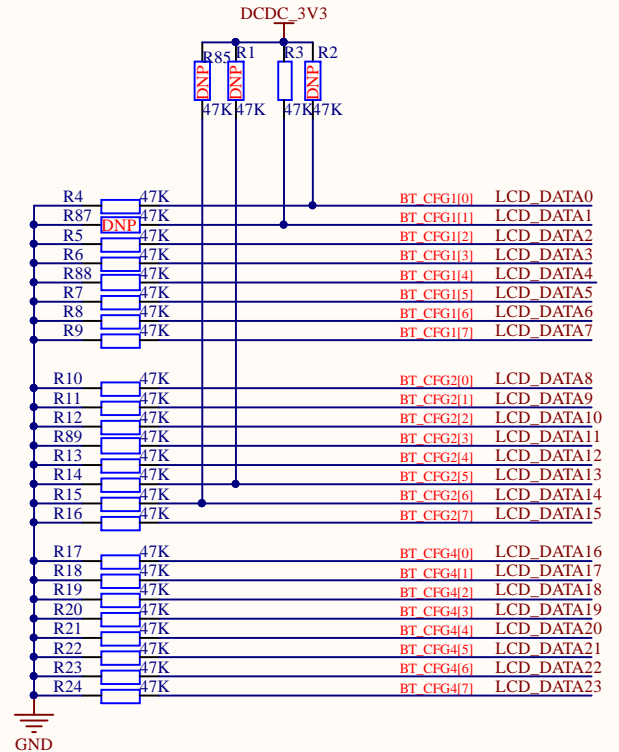


# BOOT MAP

	0/1	0/1	0/1	1	0	0	0	0
TYPE	BOOT_CFG1[7]	BOOT_CFG1[6]	BOOT_CFG1[5]	BOOT_CFG1[4]	BOOT_CFG1[3]	BOOT_CFG1[2]	BOOT_CFG1[1]	BOOT_CFG1[0]
QSPI	0	0	0	1	Reserved	DDRSMP: "000": Default "001-111"		
WEIM	0	0	0	0	Memory Type: 0 - NOR Flash 1 - OneNAND	Reserved	Reserved	Reserved
Serial-ROM	0	0	1	1	Reserved	Reserved	Reserved	Reserved
SD/eSD	0	1	0	Fast Boot: 0 - Regular 1 - Fast Boot		SD/SDMC Speed 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104		SD Power Cycle Enable 0 - No power cycle 1 - Enabled via USDHC_RST pad (uSDHC3 & 4 only)
MMC/eMMC	0	1	1	Fast Boot: 0 - Regular 1 - Fast Boot		SD/MMC Speed 0 - High 1 - Normal	Fast Boot Acknowledge Disable: 0 - Boot Ack Enabled 1 - Boot Ack Disabled	SD Power Cycle Enable 0 - No power cycle 1 - Enabled via USDHC_RST pad (uSDHC3 & 4 only)
NAND	1	BT_TOGGLEMODE	Pages In Block: 00 - 128 01 - 64 10 - 32 11 - 256		Nand Number Of Devices: 00 - 1 01 - 2 10 - 4 11 - Reserved		Nand Row address, bytes: 00 - 3 01 - 2 10 - 4 11 - 5	
	0	0	0	0	1	0	0	0
TYPE	BOOT_CFG2[7]	BOOT_CFG2[6]	BOOT_CFG2[5]	BOOT_CFG2[4]	BOOT_CFG2[3]	BOOT_CFG2[2]	BOOT_CFG2[1]	BOOT_CFG2[0]
QSPI	Reserved	Half Speed Phase Selection 0 - select sampling at non-inverted clock 1 - select sampling at inverted clock		Half Speed Delay selection 0 - one clock delay 1 - two clock delay	Half Speed Phase Selection 0 - select sampling at non-inverted clock 1 - select sampling at inverted clock	Full Speed Delay selection 0 - one clock delay 1 - two clock delay	Boot Frequencies (ARM/DSP) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved
WEIM	Muxing Scheme: 00 - A/D[16] 01 - A+DH 10 - A+DL 11 - Reserved		OneHand Page Size: 00 - 1KB 01 - 2KB 10 - 4KB 11 - Reserved		Reserved		Boot Frequencies (ARM/DSP) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved
Serial-ROM	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SD/eSD	SD Calibration Step "00" - 1 TBD		Bus Width: 0 - 1-bit 1 - 4-bit		Port Select: 00 - eSDHC1 01 - eSDHC2 10 - Reserved 11 - Reserved	Boot Frequencies (ARM/DSP) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SD1 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved
MMC/eMMC	Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 8-bit DDI (MMC 4.4) 110 - 8-bit DDI (MMC 4.4) Else - reserved		Port Select: 00 - eSDHC1 01 - eSDHC2 10 - Reserved 11 - Reserved		Boot Frequencies (ARM/DSP) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SD1 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved	Reserved
NAND	Toggle Mode (SMBus Prescaler Delay, Read Latency): "00" - 16 GPMACIA cycles "001" - 1 GPMACIA cycles "010" - 2 GPMACIA cycles "011" - 3 GPMACIA cycles "100" - 4 GPMACIA cycles "101" - 5 GPMACIA cycles "110" - 6 GPMACIA cycles "111" - 7 GPMACIA cycles		BOOT_SEARCH_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8		Boot Frequencies (ARM/DSP) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Read Time 0 - 10ms 1 - 20ms (LBA NAND)	Reserved	
	0	0	0	0	0	0	0	0
TYPE	BOOT_CFG4[7]	BOOT_CFG4[6]	BOOT_CFG4[5]	BOOT_CFG4[4]	BOOT_CFG4[3]	BOOT_CFG4[2]	BOOT_CFG4[1]	BOOT_CFG4[0]
0x450	Infinite-Loop (Debug USE only) 0 - Disable 1 - Enable	EEPROM Recovery Enable "0" - Disabled "1" - Enabled	CS select (SPI only): 00 - CS#0 (default) 01 - CS#1 10 - CS#2 11 - CS#3		SPI Addressing: 0 - 2-bytes (16-bit) 1 - 3-bytes (24-bit)	Port Select: 000 - eSPI0 001 - eSPI0 010 - eSPI0 011 - eSPI0 100 - Reserved 101 - Reserved 110 - Reserved 111 - Reserved		
0x460	L2_HW_INVALIDATE_DISABLE	Reserved	FORCE_COLD_BOOT (Reflected in SBMR2)		BT_FUSE_SEL	DIR_BT_DIS	Reserved	SEC_CONFIG[1]
Reserved (DDR3 config options)								
0x460	JTAG_SMODE[1:0]	WDG_ENABLE "0" - Disabled "1" - Enabled	SJC_DISABLE	Reserved	Reserved	Reserved	Reserved	Reserved
0x460	Reserved	Reserved	Reserved	TZASC_ENABLE	JTAG_HEO	KTE	Reserved	DLL_ENABLE 0 - Disable DLL for SD/eMMC 1 - Enable DLL for SD/eMMC
0x470	DLL Override: 0 - DLL Slave Mode for SD/eMMC 1 - DLL Override Mode for SD/eMMC	Reserved	SD2 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved	Disable SDRAM Manufacture mode 0 - Enable 1 - Disable	L1 I-Cache DISABLE	BT_MMU_DISABLE	Override Pad Settings (using PAD_SETTINGS value)
0x470	Reserved for unexpected requirements	eMMC 4.4 - RESET TO PRE-IDLE STATE	Override HYS bit for SD/MMC pads	USDHC_PAD_PULL_DOWN 0 - no action 1 - pull down	ENABLE_EMMC_22K_PULLUP 0 - 22K pullup 1 - 22K pullup	ADD_DS_SET_GPR1_16 0 - Set 1 - Don't set	USDHC_IOMUX_SION_BIT_ENABLE 0 - Disable 1 - Enable	USDHC_IOMUX_SRE Enable 0 - Disable 1 - Enable
0x470	USDHC_CMD_OE_PRE_EN (SD/MMC debug)	LPB_BOOT (Core / DDR - Bus) "00" - LPB Disable "01" - 1 GPD (def freq) "10" - Div by 2 "11" - Div by 4	BT_LPB_POLARITY (GPIO polarity)		POWER_MNG_CFG (LDO's DCDC's) (Reserved - NOT USED)			
0x470	Override NAND Pad Settings (using PAD_SETTINGS value)	MMC_DLL_DLY[6:0] Delay target for SD/eMMC DLL, it is applied to slave mode target delay or override mode target delay depends on DLL Override fuse bit value.						

#Boot map pictures reference from the NXP I.MX6ULL EVK Board Schematic

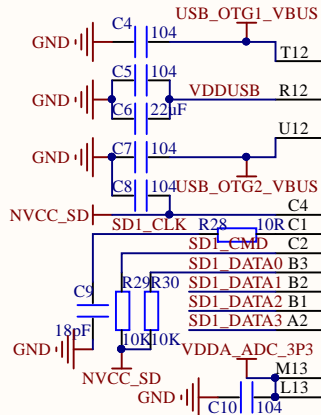
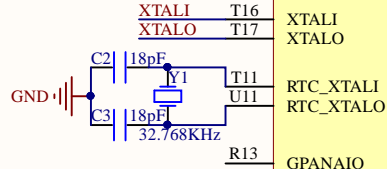
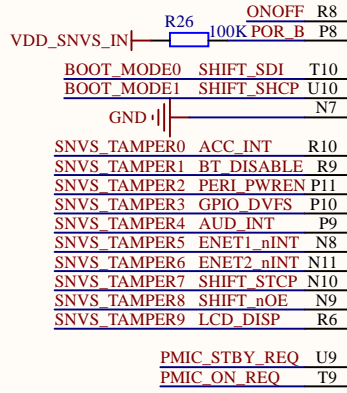


GND

BMODE[1:0]	BOOT TYPE
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot(Development)
11	Reserved

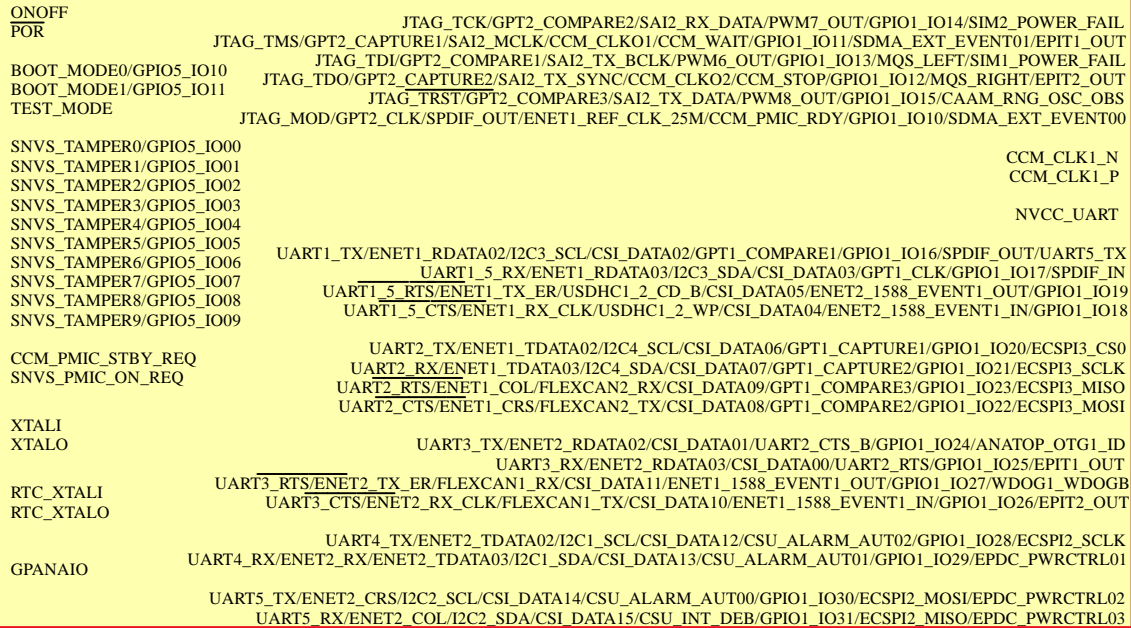
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Author: lycreturn@ALIENTEK	Size: A4	
Date: 2019-09-12	File: IMX6ULL_CORE_BOOT.SchDoc	
Revision: *	Version: V1.0	

## IMX6ULL

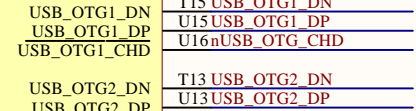


MCIMX6Y2CVM05AB

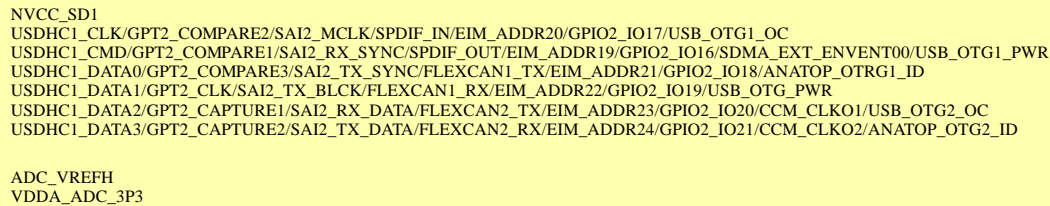
## IMX6ULL-CONTROL



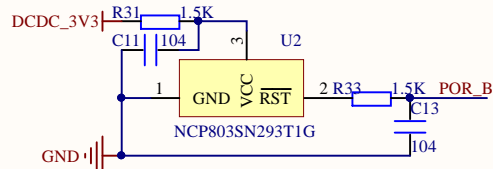
## IMX6ULL-USB



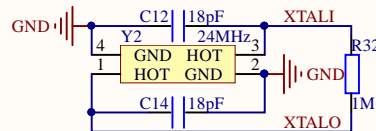
## IMX6ULL-SD1\ADC



## RESET



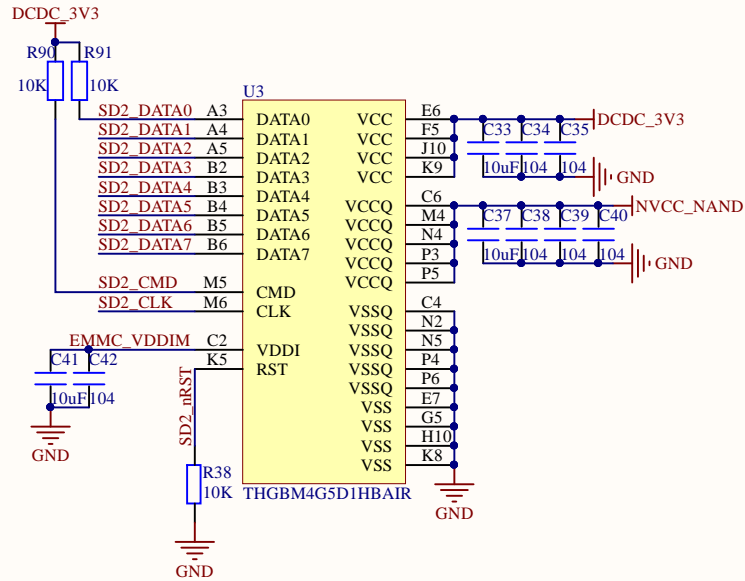
## XTAL



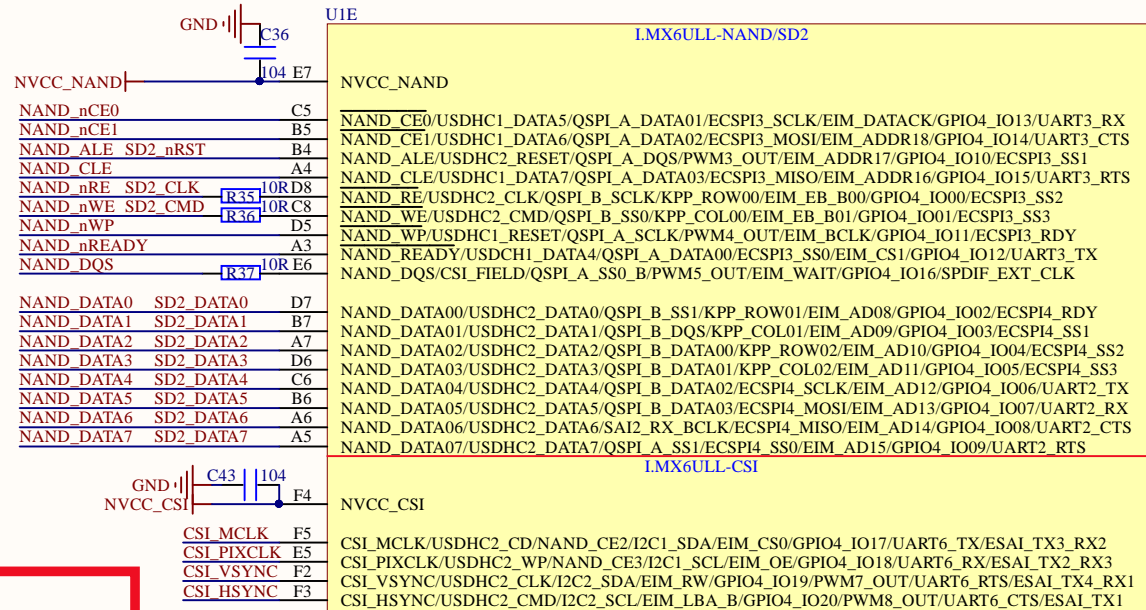
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Author:	Size:	
lycretun@ALIENTEK	A3	
Date:	File:	
2019-09-12	IMX6ULL_CORE_CONTROL.SchDoc	
Revision:	Version:	
*	V1.0	



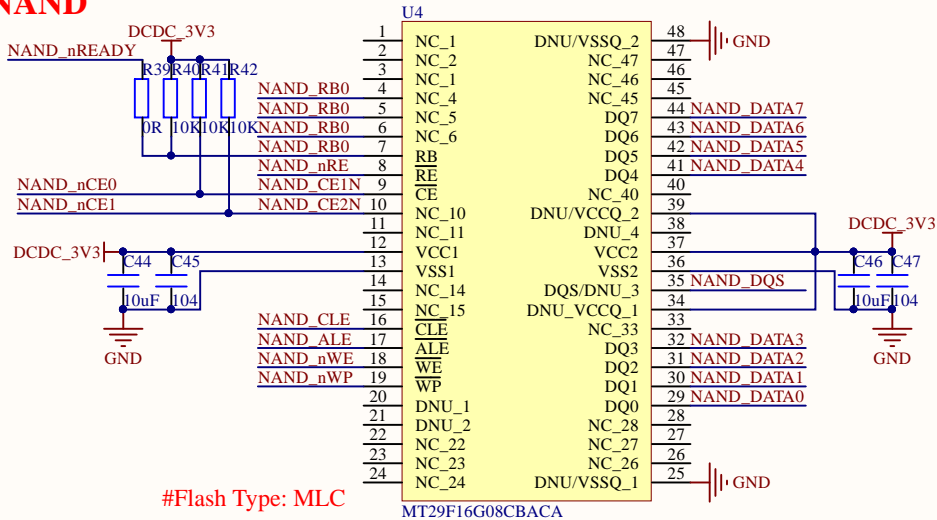
## #EMMC Storage<4.51>



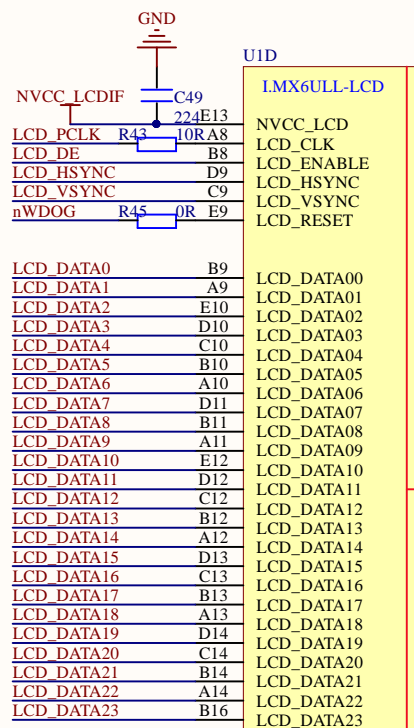
## IMX6ULL\_NAND



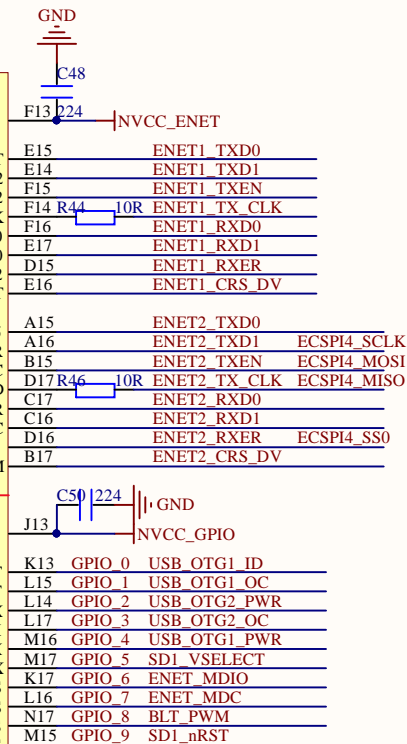
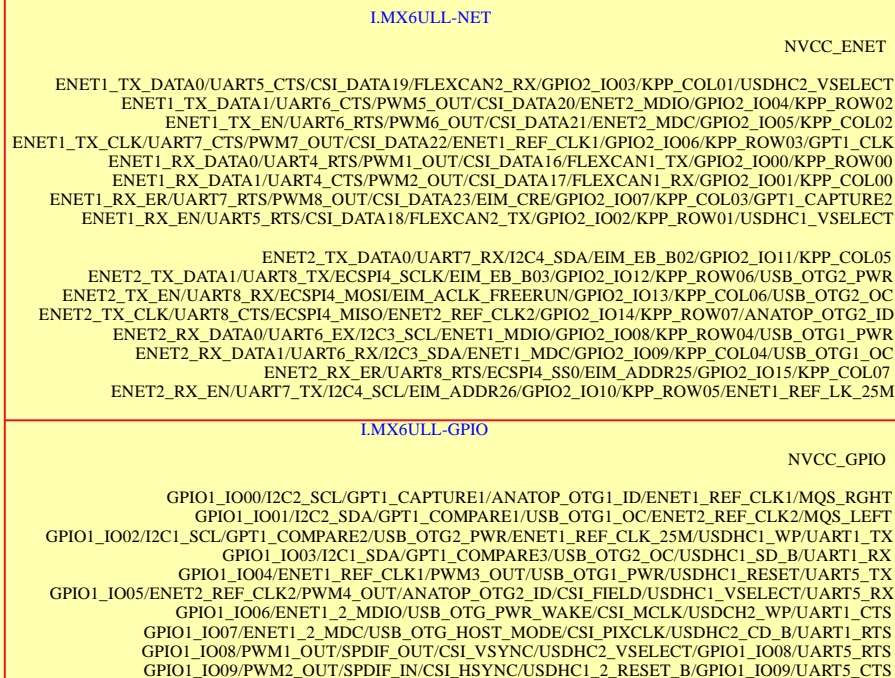
## NAND



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Author: lycretum@ALIENTEK	Size: A4	
Date: 2019-09-12	File: IMX6ULL_CORE_FLASH.SchDoc	
Revision: *	Version: V1.0	

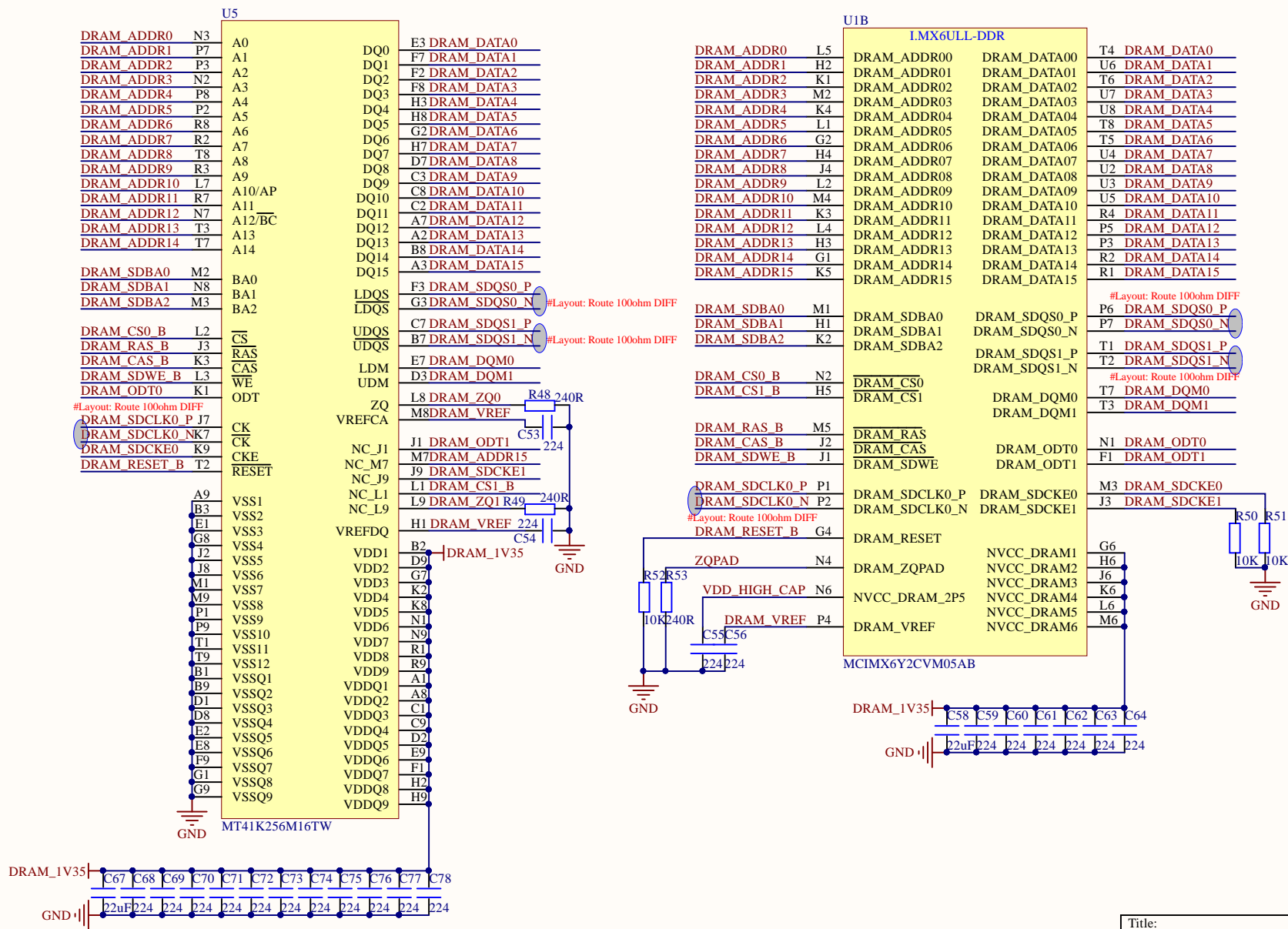


MCIMX6Y2CVM05AB

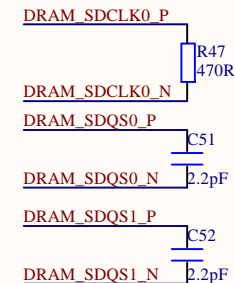


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Author: lycreturn@ALIENTEK	Size: A4	
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Revision: *	Version: V1.0	

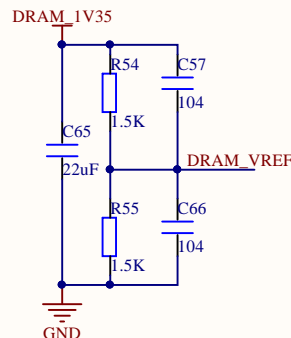




Note:  
CLK termination: Place RXX close to U2



DDR3 VREF  
#Note: 1K/1.5K are OK



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Author: lycreturn@ALIENTEK	Size: A4	
Date: 2019-09-12	File: IMX6ULL_CORE_LVDDR3.SchDoc	
Revision: *	Version: V1.0	

1

2

3

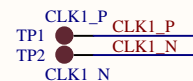
4

A

B

C

D



J1			J2		
CSI_HSYNC	1	60	CSI_VSYNC	1	60
CSI_MCLK	2	59	CSI_DATA3	2	59
CSI_DATA2	3	58	CSI_DATA7	3	58
CSI_DATA6	4	57	CSI_DATA1	4	57
CSI_PIXCLK	5	56	CSI_DATA0	5	56
CSI_DATA5	6	55	CSI_DATA4	6	55
LCD_DATA0	7	54	SD1_CLK	7	54
LCD_DATA1	8	53	SD1_CMD	8	53
LCD_DATA2	9	52	SD1_DATA2	9	52
LCD_DATA3	10	51	SD1_DATA3	10	51
LCD_DATA4	11	50	SD1_DATA1	11	50
LCD_DATA5	12	49	SD1_DATA0	12	49
LCD_DATA6	13	48	SNVS_TAMPER9	13	48
LCD_DATA7	14	47	GPIO_5	14	47
LCD_DATA8	15	46	SD1_VSELECT	15	46
LCD_DATA9	16	45	LCD_DE	16	45
LCD_DATA10	17	44	LCD_PCLK	17	44
LCD_DATA11	18	43	LCD_HSYNC	18	43
LCD_DATA12	19	42	LCD_VSYNC	19	42
LCD_DATA13	20	41	PMIC_ON_REQ	20	41
LCD_DATA14	21	40	RESET	21	40
LCD_DATA15	22	39	SNVS_TAMPER6	22	39
LCD_DATA16	23	38	ENET2_INT	23	38
LCD_DATA17	24	37	ENET2_RXD0	24	37
LCD_DATA18	25	36	ENET2_RXD1	25	36
LCD_DATA19	26	35	ENET2_TXD0	26	35
LCD_DATA20	27	34	ENET2_TXD1	27	34
LCD_DATA21	28	33	ENET2_RXER	28	33
LCD_DATA22	29	32	ENET2_CRS_DV	29	32
LCD_DATA23	30	31	ENET2_TXEN	30	31
			ENET2_TX_CLK	31	

3710M060046G3FT01

J1			J2		
DC5V	1	60	SNVS_TAMPER4	1	60
DC5V	2	59	AUD_INT	2	59
	3	58	ONOFF	3	58
	4	57	SNVS_TAMPER1	4	57
	5	56	BEEP	5	56
	6	55	SNVS_TAMPER0	6	55
	7	54	9D_INT	7	54
	8	53	BOOT_MODE0	8	53
	9	52	SHIFT_SDI	9	52
	10	51	SHIFT_SHCP	10	51
	11	50	SNVS_TAMPER8	11	50
	12	49	SHIFT_nOE	12	49
	13	48	SNVS_TAMPER7	13	48
	14	47	SHIFT_STCP	14	47
	15	46	SNVS_TAMPER5	15	46
	16	45	ENET1_INT	16	45
	17	44	SNVS_TAMPER2	17	44
	18	43	PERI_PWREN	18	43
	19	42	GPIO_2	19	42
	20	41	KEY1	20	41
	21	40	GPIO_4	21	40
	22	39	LED1	22	39
	23	38	GPIO_9	23	38
	24	37	SD1_nRST	24	37
	25	36	GPIO_8	25	36
	26	35	BLT_PWM	26	35
	27	34	JTAG_TDI	27	34
	28	33	SAI2_TX_BCLK	28	33
	29	32	JTAG_TDO	29	32
	30	31	SAI2_TX_SYNC	30	31
			JTAG_TCK		
			SAI2_RX_DATA		
			JTAG_TMS		
			SAI2_MCLK		
			JTAG_nTRST		
			SAI2_TX_DATA		
			JTAG_MOD		
			SPDIF_OUT		
			ENET1_TXD0		
			ENET1_RXD1		
			ENET1_RXD0		
			ENET1_CRS_DV		
			ENET1_RXD0		
			ENET1_TXEN		
			ENET1_TXD1		
			ENET1_TX_CLK		
			ENET1_RXER		

3710M060046G3FT01

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Author: lycretum@ALIENTEK	Size: A4	
Date: 2019-09-12	File: IMX6ULL_CORE_PIN.SchDoc	
Revision: *	Version: V1.0	

1

2

3

4

