Adder Design

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The problems in this set are due July 7, 2023, by 11:59 pm. Please submit original work.

Design the following adder components in HDL:

1. **(5 points)** Half-adder stage.
2. **(5 points)** Full-adder stage.
3. **(5 points)** Four-bit ripple-carry adder.
4. **(5 points)** Four-bit carry lookahead adder.

Using the above adder components, build the following larger components:

1. (**10 points**) 16-bit adder in the carry-ripple style.
2. (**10 points**) 16-bit carry lookahead adder by linking up four 4-bit carry lookahead adders in carry-ripple style.

Use the provided `.hdl` files as a starting point to develop your solutions. Submit the completed `.hdl` files via BBLearn as a single zip file. Do not submit any other files.