

Lab Week 6 Part 3 - Presentation of Results

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Run your project for various values of matrix size and CPU clock speed. Remember MCLK is the clock driving the CPU. Referring to the diagram on page 380 of TRM, the default primary source for MCLK is DCOCLK (Input no 3 to the Mux) . Hence $MCLK = DCOCLK / \text{Divider}$. DCOCLK must be 12 MHz if you are using UART (which is not absolutely necessary if you are executing in debug mode). You can change CPU clock speed by the following line of code where N is the divider which can be 1/2/4/8/16/32/64/128

```
CS_initClockSignal(CS_MCLK,CS_DCOCLK_SELECT,CS_CLOCK_DIVIDER_N);
```

Matrix size can be changed by altering the following line of code which already exists in the matrix multiplication code provided in the description for Part 3 (Refer page 11 of the description)

```
#define MATRIX_SIZE 40
```

Present your results by filling up the following matrix and upload it as part of your submission:

The columns correspond to different dividers and the rows correspond to different matrix sizes as given. The largest matrix size is that which can be stored in Flash memory leaving enough space for the code. You may have to experiment a bit

Size/Divider	1	4	16	64
10X10	2.843	11.487	42.125	182.353
25X25	41.812	167.250	667.125	2677.585
40X40	168.750	675.125	2700.437	10802.843
Largest possible 73	1014.289	4057.375	16231.460	64955.882