Interface Circuits for TIA/EIA-485 (RS-485)

Application Report

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ABSTRACT

This application report provides information concerning the design of TIA/EIA-485 interface circuits. The document discusses the need for balanced transmission-line standards and gives an example for a process-control design. Line loading is discussed with subtopics of signal attenuation, fault protection, and galvanic isolation. Finally, setting up and measuring using eye patterns is documented. Eye patterns are used to measure the effects of signal distortion, noise, signal attenuation, and the resultant intersymbol interference (ISI) in a data transmission system.

1 The Need for Balanced Transmission-Line Standards

This document focuses on industry's most widely used balanced transmission- line standard, ANSI/TIA/EIA-485-A [1], [2] (referred to hereafter as 485). After reviewing some key aspects of the 485 standard you are introduced to the practicalities of implementing a differential transmission configuration based on a factory automation example. Finally, new additions to TI's 485 product line are discussed along with their application, where appropriate.

Data transmission between computer-system components and peripherals over long distances and under high-noise conditions usually proves to be difficult, if not impossible, with single-ended drivers and receivers. Recommended standards for balanced digital voltage interfacing provide the design engineer with a universal solution for long-line system requirements.

The 485 is a balanced (differential) digital transmission line interface developed to improve on the TIA/EIA-232 (referred to hereafter as 232) limitations. The advantages are:

- High signaling rate – up to 50M bits/s
- Longer line length – up to 1200 meters
- Differential transmission – fewer noise emissions
- Multiple drivers and receivers

Data transmission circuits employing 485 drivers, receivers, or transceivers are used in practically any application requiring an economical, rugged interconnection between two or more computing devices. A typical application could be using 485 signaling between point-of-sales terminals and a central computer for automatic stock debiting. The low-noise coupling of balanced signaling with twisted-pair cabling and the wide common-mode voltage range of 485 allow data exchange at data signaling rates up to 50M bit/s or over distances of several kilometers at lower rates.

As a result of its versatility, an increasing number of standards committees are embracing the 485 standard as the physical layer specification of their communications standard. Examples include the ANSI (American National Standards Institute) Small Computer Systems Interface (SCSI) that is featured in the *Interface Circuits for SCSI* design notes (SLLA035), the Profibus standard, and the DIN Measurement Bus.

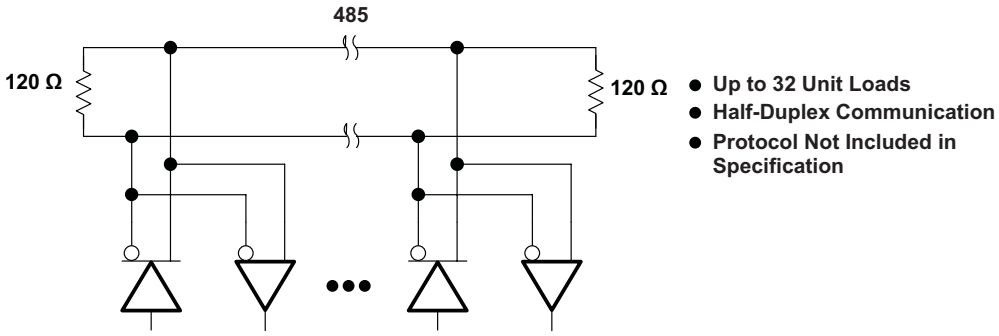


Figure 1. 485 Specification Highlights

KEY PARAMETERS	SPECIFICATION LIMITS
Maximum common-mode voltage	–7 V to 12 V
Receiver input resistance	12 kΩ minimum
Receiver sensitivity	±200 mV
Driver load	60 Ω
Driver output short-circuit limit	250 mA for V_{SHORT} –7 V to 12 V

The balanced transmission-line standard 485 was developed in 1983 to interface a host computer's data, timing, or control lines to its peripherals. The standard specifies the electrical layer only. Protocols, timing, serial or parallel data, and connector choice are all left to be defined by the designer or by a higher-level standard.

The 485 standard originally was defined as an upgrade to and a more flexible version of the TIA/EIA-422 standard, hereafter referred to as 422. Whereas 422 facilitates simplex communication (single direction on a line) only, 485 allows for multiple drivers and receivers on a single line, facilitating half-duplex (bidirectional) communication (see Figure 1). Like 422, the maximum line length is not specified, but is based on 24-AWG cable; it is nominally around 1.2 km. Maximum signaling rate is unlimited and is set by the ratio of rise time to bit time, similar to 232. In many cases, it is the length of the cable that limits the signaling rate more than the drivers, due to transmission-line effects and noise.

The differences between 485 and 422 lie primarily in the driver features that allow reliable multipoint communications. See also references[3] and [4] for comparisons of several bus standards.

2 System Design Considerations

2.1 Line Loading

The 485 standard takes into account the need for line termination and the subsequent loading on the transmission line. The decision on whether to terminate the line is system dependent and is affected by the choice of the maximum line length and signaling rate.

Line Termination: The test for whether a transmission line is to be considered as a distributed- or a lumped-parameter model depends on the relationship of signal transition time, t_t, at the driver output and the propagation time, t_{pd}, of the signal down the cable.

If $2t_{pd} \geq t_t/5$, the line should be treated as a distributed parameter model and terminated accordingly; otherwise, it can be treated as a lumped-parameter model and termination is unnecessary.

Unit Load Concept: The maximum number of drivers and receivers that can be placed on a single 485 communication bus depends on their loading characteristics relative to the definition of a unit load (UL). The 485 standard specifies a maximum of 32 ULs per line.

One UL (worst case) is defined as a steady-state load allowing 1 mA of current under a maximum common-mode voltage stress of 12 V or 0.8 mA at -7 V. ULs may consist of drivers or receivers and failsafe resistors, but they do not include the ac termination resistors.

The example in Figure 2 shows a UL calculation for the SN75ALS176B. Because this device is connected internally as a transceiver (i.e., driver output and receiver input connected to the same bus), it is difficult to obtain separate driver leakage and receiver input currents. For this calculation, reference is made to the receiver input resistance, 12 kΩ, giving a transceiver current of 1 mA. This can be taken to represent 1 UL, which allows up to 32 devices to be connected to the line.

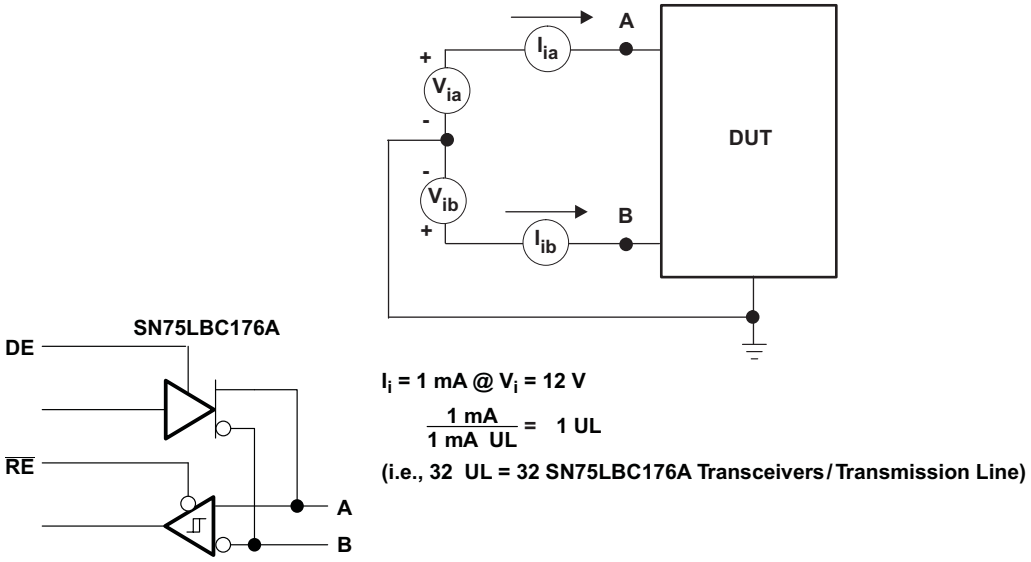


Figure 2. Unit Load Concept

As long as the receivers all have input resistance greater than the 12 kΩ, thus preventing loading of the line, it is possible to connect more than 32 receivers.

2.2 Signal Attenuation and Distortion

A useful rule for allowable attenuation is –6 dB at the maximum signaling rate in Hz. Attenuation figures usually are supplied by cable manufacturers. The curve in Figure 3 shows the attenuation change versus frequency for a 24-AWG cable.

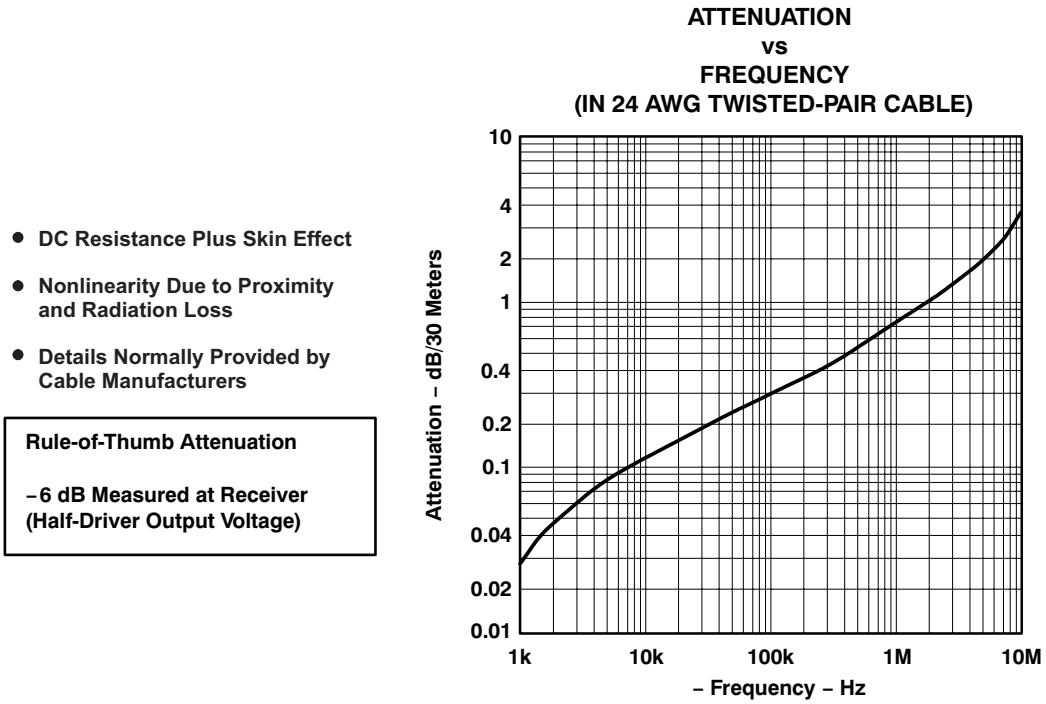


Figure 3. Signal Attenuation

The simplest way to determine the effects of random noise, jitter, attenuation, and dispersion is with the use of eye patterns. For information on how to set up eye patterns, refer to section *Eye Patterns* in this document. Figure 4 shows the distortion of the signal at the receiving end of 500 meters of 20 AWG twisted-pair cable at different signaling rates. When the signaling rate is increased further, the effects of jitter then become noticeable. In this case, at 1M bits/s, a 5% jitter is seen. At 3.5M bit/s the signal begins to be lost completely and the quality of transmission is severely degraded. The maximum allowable jitter in a system is generally held to less than 5%.

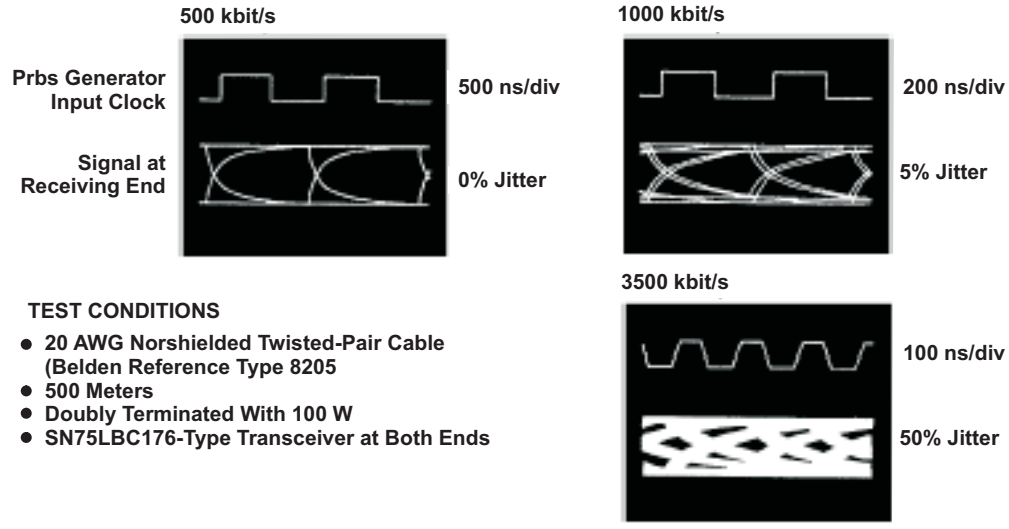


Figure 4. 485 Signal Distortion vs Signaling Rate

2.3 Fault Protection and Failsafe Operation

Fault Protection: As with any system design, consideration must be given to the natural and induced environmental conditions to be encountered during operation. Factory-controlled applications generally require protection against excessive noise voltages. The noise immunity afforded by the differential transmission scheme, and, in particular, the wide common-mode voltage range of 485, may be insufficient. Protection can be accomplished in a number of ways, the most effective being through galvanic isolation, which is discussed later. Galvanic isolation provides good system-level protection but results in higher cost. A more popular and less-expensive solution is the use of protection diodes. The tradeoff using the diode approach over galvanic isolation is a lower level of protection. Examples of external and integrated transient protection diodes are given in the following figures:

Figure 5 shows how external diodes offer transient spike protection for the 485 transceiver, SN75ALS176.

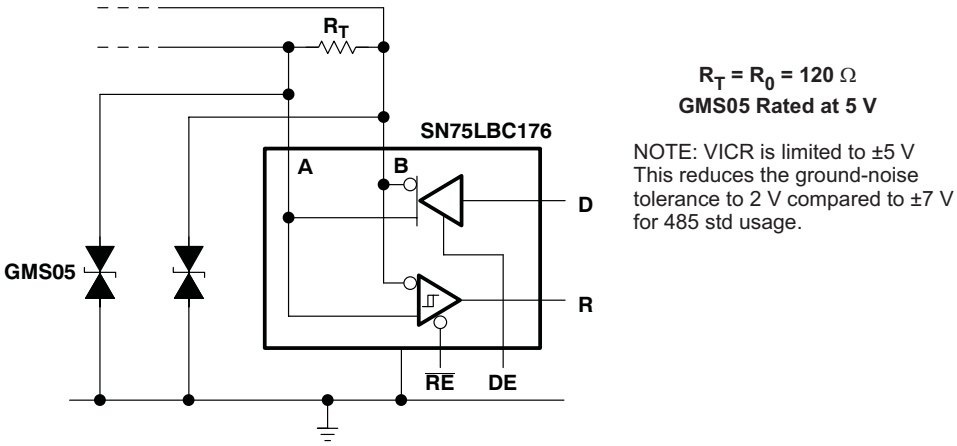
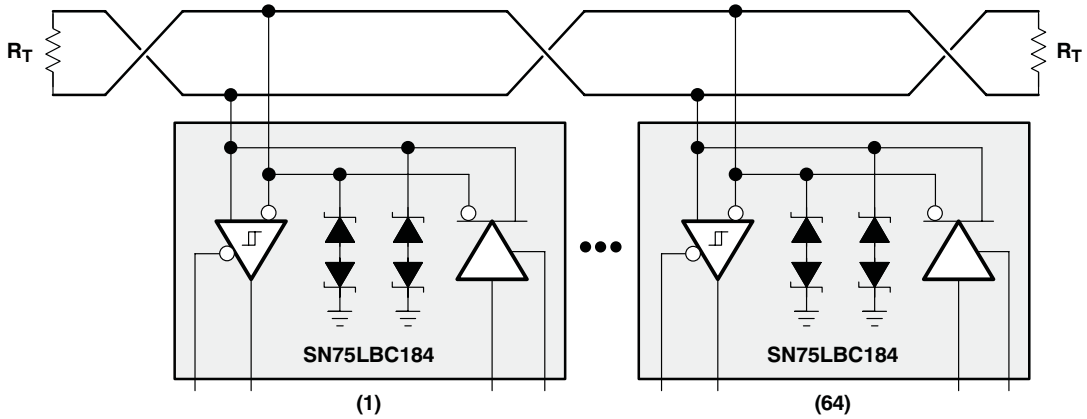


Figure 5. Input Protection for Noisy Environments

R_T is the usual termination resistance and is equivalent in value to the characteristic impedance, R_0, of the line.

Figure 6 shows integrated transient suppression diodes for those applications where board space is a premium and full 485 performance is desired. The SN75LBC184 ('LBC176 footprint) offers built-in protection against high-energy transients for electrically noisy environments.



- Transceiver with integrated transient suppression
- Protects against pulses of 400 W peak
- 250 kbit/s in electrically noisy environment
- Slew rate controlled for longer stub lengths

Figure 6. Integrated Transient Voltage Protection for Noisy Environments0

Failsafe Operation: The feature of failsafe protection also is a requirement in many 485 applications; however, its usefulness needs to be considered and understood at an application level.

The Need for Failsafe Protection: In any party-line interface system with multiple driver/receivers, long periods of time occur when the driving devices are inactive. This state is known as *line idle* and occurs when the drivers place their outputs into a high-impedance state. During line idle, the voltage along the line is left floating (i.e., indeterminate—neither logic-high nor logic-low state). As a result, the receiver can be falsely triggered into either a logic-high or logic-low state, depending on the presence of noise and the last polarity of the floating lines. Obviously, this is undesirable, as the circuitry following the receiver could interpret this as valid information. It is best to detect such a situation and place the receiver outputs into a known and predetermined state. The name given to methods that ensure this condition is *failsafe*. An additional, desirable feature that a failsafe provides is to protect the receiver from shorted line conditions, which can again cause erroneous processing of data.

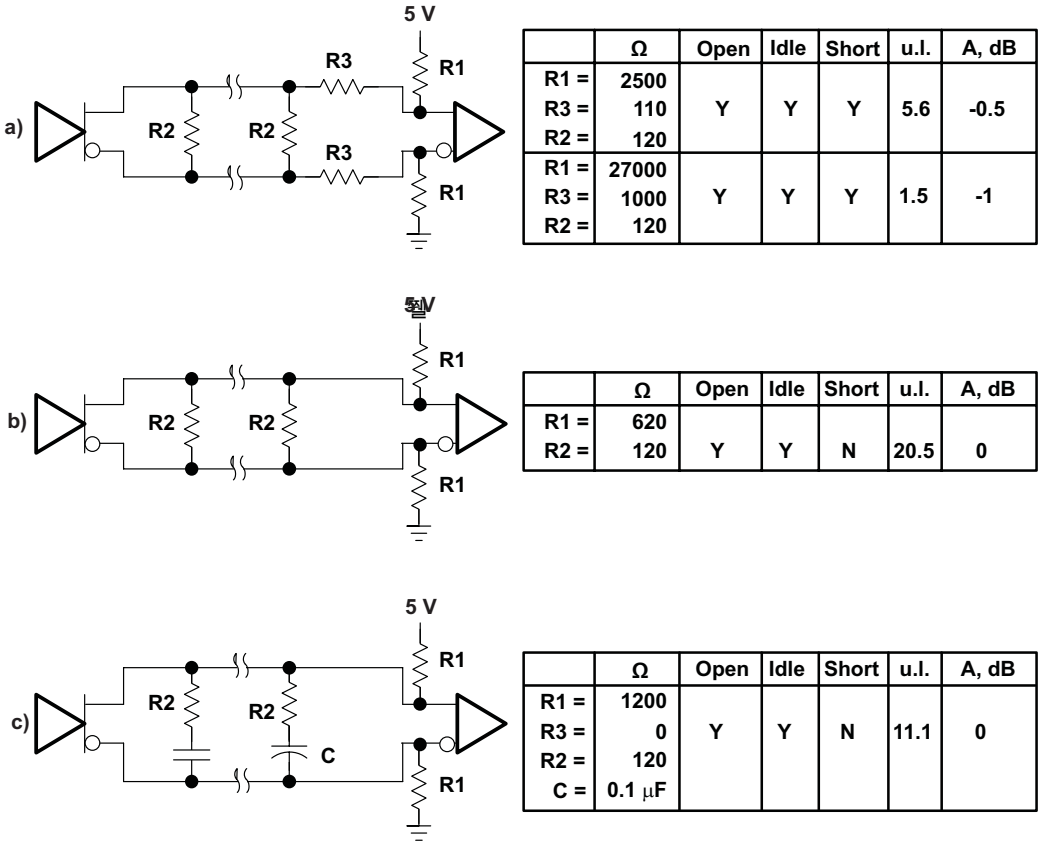
Among the several ways to implement a failsafe feature, including a hard-wired failsafe, is the use of protocols. Protocols, although complicated to implement, are the preferred method. However, because most system designers, hardware designers in this case, prefer to implement such functions in hardware, a hard-wired failsafe most often is implemented.

A hard-wired failsafe must provide a defined voltage across the receiver's input, regardless of whether the signal pair is shorted together or is left open circuited. The failsafe also must be incorporated into the line termination, if present, when at the extremes of the line.

Internal Failsafe: Manufacturers have begun to facilitate failsafe design by including some form of open-line failsafe circuitry within the integrated circuits. Quite often, the extra circuitry is just a large pullup resistor on the noninverting receiver input and a large pulldown resistor on the inverting input of the receiver. These resistors normally are in the vicinity of 100 kΩ and, when used with line-termination resistors (typically 50 Ω to 100 Ω) to form a potential divider, only a few millivolts are generated differentially. As a result, this voltage (receiver threshold voltage) is insufficient to switch the receiver state. To use these internal resistors effectively means no line-termination resistors can be used, which reduces the allowed reliable signaling rate significantly.

External Failsafe for Open-Line and Terminated Conditions: Figure 7 shows some common circuits used to provide an external hard-wired failsafe for a 485 interchange circuit. The purpose of each is to maintain a voltage at the receiver inputs above the minimum input threshold and a known logic state under one or more of three fault conditions. In each, R2 represents the resistors for impedance matching of the transmission line and becomes part of a voltage divider creating the steady-state bias voltage. Each receiver is assumed to represent one UL.

The tables to the right of the schematics indicate some typical resistor or capacitor values, the types of failsafe provided, the number of ULs used, and the signal attenuation. The next section goes through the resistance value calculations for the shorted-line failsafe circuit for some insight on how the values can be modified for a particular design.



	Ω	Open	Idle	Short	u.l.	A, dB
R1 =	2500					
R3 =	110	Y	Y	Y	5.6	-0.5
R2 =	120					
R1 =	27000					
R3 =	1000	Y	Y	Y	1.5	-1
R2 =	120					

	Ω	Open	Idle	Short	u.l.	A, dB
R1 =	620					
R2 =	120	Y	Y	N	20.5	0

	Ω	Open	Idle	Short	u.l.	A, dB
R1 =	1200					
R3 =	0	Y	Y	N	11.1	0
R2 =	120					
C =	0.1 μF					

Figure 7. External 485 Failsafe Circuits

External Failsafe With Shorted-Line Conditions: To implement protection from the shorted-line condition, more resistors are required. When the line is shorted, the transmission line's impedance goes to zero and the termination resistors also are shorted. Putting extra resistors in series with the input to the receiver provides shorted-line failsafe protection.

The extra resistors R3 in Figure 8 can be added only when using devices with separate driver outputs and receiver inputs. Internally wired transceivers cannot be used for shorted-line failsafe. If this form of protection is required, then a device such as the SN75LBC180, with its separate driver outputs and receiver inputs, is recommended. If a transceiver-type of device is used, then the extra R3 resistors cause extra attenuation of the output signal. The 'ALS180 has its driver outputs fed directly to the line, then bypassing the R3 resistors.

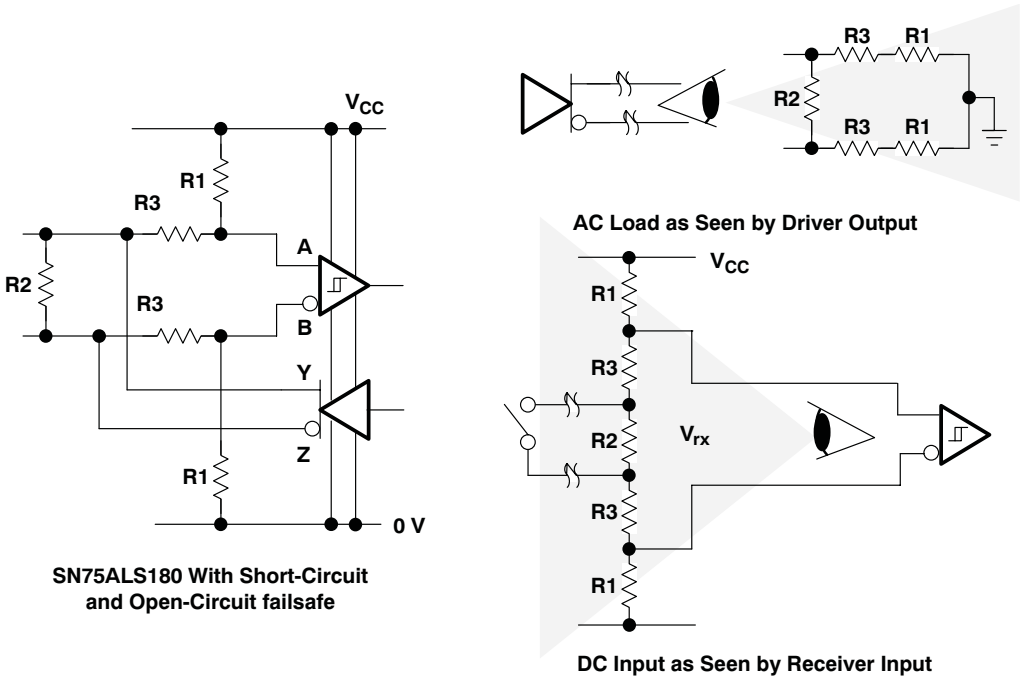


Figure 8. Short-/Open-Circuit Fail-Safe

Calculating the Resistor Values: If the line becomes shorted, R2 is removed from the circuit, leaving a voltage across the receiver inputs of:

$$V_{ID} = V_{CC} \times \frac{2R3}{2R1 + 2R3} \quad (1)$$

For 485 applications, the standard specifies the maximum input voltage threshold (V_{IT}) to be less than 200 mV. So, a known state can be assumed when $V_{ID} > V_{IT}$ or $V_{ID} > 200$ mV. This condition becomes the first design constraint.

$$V_{CC} \times \frac{2R3}{2R1 + 2R3} > 200 \text{ mV} \quad (2)$$

When the line goes into a high-impedance state, the receiver is affected the two R3s in series, with R2 plus the two R1s pulling up and down on either input. The receiver input voltage is now:

$$V_{ID} = V_{CC} \times \frac{R2 + 2R3}{2R1 + R2 + 2R3} \quad (3)$$

This gives the second design constraint:

$$V_{CC} \times \frac{R2 + 2R3}{2R1 + R2 + 2R3} > 200 \text{ mV} \quad (4)$$

The transmission line is affected by an effective line-termination resistance, R2, in parallel with twice the sum of R1 and R3. This matches the transmission line's characteristic impedance, Z_O, and therefore provides a third constraint of:

$$Z_0 = 2R2 \times \frac{R1 + R3}{2R1 + R2 + 2R3} \quad (5)$$

Other design constraints include the additional line loading presented by the failsafe circuit and the attenuation caused by R3, R1, and the input resistance of the receiver.

Note: See the SN75HVD10 3.3-V family of 485 transceivers and other new products for an integrated short-/open-circuit failsafe.

2.4 Galvanic Isolation

Computer and industrial serial interfacing are areas where noise can seriously affect the integrity of data transfer. A tested method of improving noise performance for any interface circuit is galvanic isolation.

Isolation in data communication systems is achieved without direct galvanic connection (wires) between drivers and receivers. Magnetic linkage from transformers provides the power for the system, and TI's capacitively coupled digital isolators provide the data connection. Galvanic isolation removes ground-loop currents and the resulting noise voltage that corrupts data is eliminated. Also, common-mode noise effects and many forms of radiated noise can be reduced to negligible limits using this technique.

As an example, consider the case of a process control system where the interface node, shown in Figure 9, is connected between a data logger and a host computer via a 485 link.

When an adjacent electric motor starts up, a momentary difference in ground potentials of the data logger and the computer often occur due to a surge in current. If no isolation scheme is employed in the data communication path, data may be lost during the surge interval and, in the worst case, damage to the computer can occur.

Circuit Description: The schematic shown in Figure 9 forms a one-node interface for a distributed supervisory, control, and regulation (DSCRS) system. Such a scheme is often used in process control applications. Data is transmitted over a two-wire bus formed by a twisted-pair and ground wire with an overall shield. Low power is useful in this type of application because many remote out-stations are either battery operated or require battery-backup capability. In addition, with low power, the isolation transformer can be small. The bus transceiver shown in Figure 9, the SN65HVD10 or any of TI's 3.3-V transceivers with low power consumption, may be used. Of course, any of TI's 3.3-V or 5-V RS-485, 3.3-V TIA/EIA-644 LVDS, or 3.3-V TIA/EIA-899 M-LVDS transceivers can be used in this circuit.

Theory of Operation: The example presented in Figure 9 provides for either 3.3-V or 5-V galvanic isolation through the use of digital isolators and an isolation transformer. Because the 485 transceiver requires an isolated power supply, the TPS7101 adjustable LDO voltage regulator must also be isolated. This is accomplished by using a NAND-gate oscillator to drive an isolation transformer. The output of the transformer is then rectified, filtered, and used to bias the regulator. In high-EMI environments, this approach is often used to prevent noise from being coupled into the main power source where it can be passed along to other subsystems connected to the same source. Also, the TPS7101 can be used to power other components and has been tested with regulator loads up to 500 mA. The device can be configured as a 3.3-V or 5-V regulator by adjusting the biasing resistors as listed in the BOM for the circuit.

Galvanic isolation of the data lines is provided by a triple channel digital isolator, the ISO7231M. This device is chosen for its 150-Mbps signaling rate, low 25-ns typical prop delay, 2.5-kV(rms) voltage isolation and typical 50-kV/μs voltage transient protection. The ISO7231M is designed for use in high-speed digital interface applications that require high-voltage isolation between the input and the output. Its use is strongly recommended in high-ground-noise or induced noise environments.

Components are available from several vendors that provide many of the functions displayed in Figure 9. However, this discrete component solution provides much better power supply isolation and is significantly less expensive.

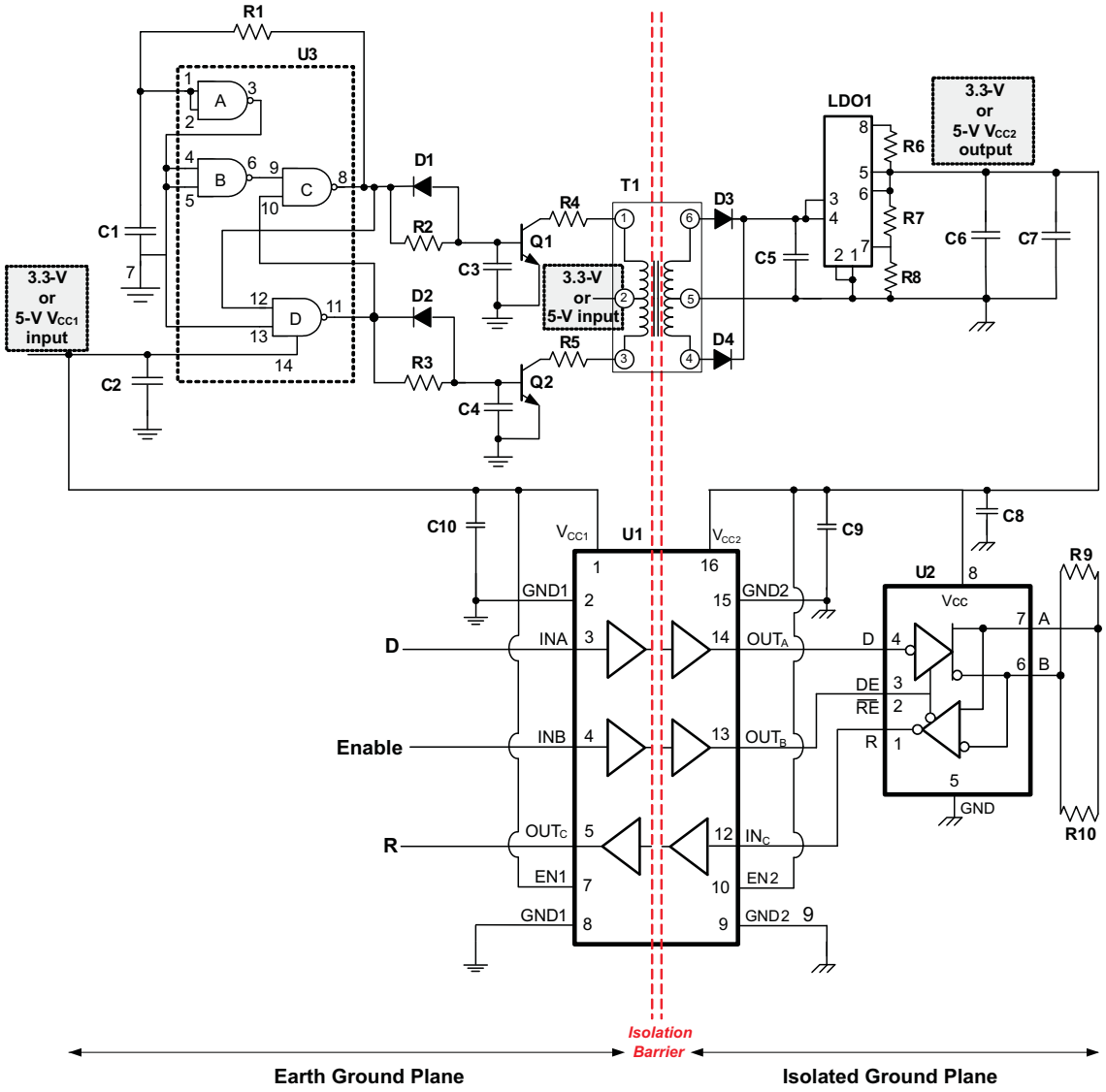


Figure 9. Isolated 3.3-V or 5-V RS-485 Node

Note that any of TI's 3.3-V 485 transceivers such as the SN65HVD10 or 5-V devices like the SN65LBC176A can be used in this circuit.

Table 1. Isolated 3.3-V or 5-V RS-485 Node BOM

Reference Designator	Description
U1	ISO7231M Digital Isolator
U2	3.3-V or 5-V RS-485 Full-Duplex Transceiver
U3	SN74HC132, Quad Positive NAND
LDO 1	TPS7101, Adjustable LDO Voltage Regulator
R1	Resistor, 2 kΩ 1/4 W, 1%
R2, R3	Resistor, 1 kΩ 1/4 W, 1%
R4, R5	Resistor, 10 Ω 1/4 W, 1%
R6	Resistor, 250 kΩ 1/4 W, 1%

Table 1. Isolated 3.3-V or 5-V RS-485 Node BOM (continued)

Reference Designator	Description
R7	3.3-V output Resistor, 309 kΩ 1/4 W, 1%
	5-V output Resistor, 549 kΩ 1/4 W, 1%
R8	Resistor, 169 kΩ 1/4 W, 1%
R9, R10	Resistor, 120 Ω 1/4 W, 1%
C1, C7	Capacitor, 0.01 µF, 100 V, 10%
C2	Capacitor, 0.001 µF, 100 V, 10%
C3, C4	Capacitor, 100 pF, 100 V, 10%
C5	Capacitor, 1 µF, 100 V, 10%
C6	Capacitor, 47 µF, 100 V, 10%
C8, C9, C10	Capacitor, 0.1 µF, 100 V, 10%
D1, D2	Diode, 1N4148
D3, D4	Diode, 1N5817
Q1, Q2	Transistor, 2N2222
T1	Transformer, TGRTI340NA, haloelectronics.com

3 Process-Control Design Example

To gain more knowledge in the design of a 485 system, it is beneficial to look at a specific example. Consider a factory automation system with a host controller and several outstations. Each outstation is capable of both transmitting and receiving data.

The system has the following features, and a general system specification is shown in Figure 10.

- Furthest outstation is 500 m from the host controller.
- Requires up to 31 outstations on the line (with the host controller, a total of 32 stations).
- System signaling rate is 500K bit/s.
- Only one signal pair is used for data transmission operating in half-duplex mode.

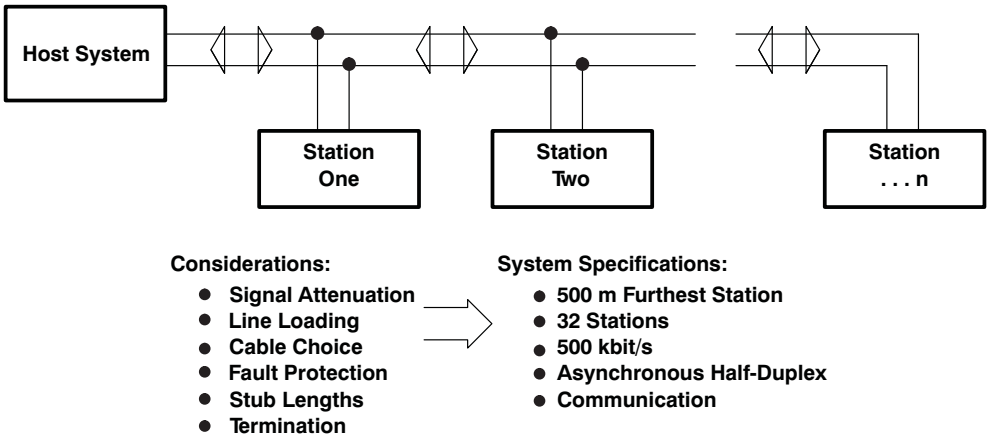


Figure 10. Process-Control Design Example

To transmit data at the design goal of 500K bits/s and comply with the 485 standard, the driver output transition time can be no more than 0.3 times the unit interval (UI). This establishes an upper limit on the transition time of:

$t_t \leq 0.3 \times UI$

$$t_t \leq 0.3\left(\frac{1}{500 \times 10^3}\right) \quad (6)$$

$t_t \leq 600$ ns

If a cable with a phase velocity equal to the speed of light in vacuum could be obtained, the propagation delay, t_{pd}, of the cable would be 3.33 ns/m multiplied by 500 m or 1667 ns. Checking the criteria for determining whether there is a transmission line (refer to Section 2.1):

$$2t_{pd} \geq \frac{t_t}{5} \quad (7)$$

3333 > 120

With the slowest possible signal transition and the fastest phase velocity, there is indeed a transmission line. Furthermore, using real-world components only underscores the fact that the 500-m, half-duplex transmission line must be terminated at both ends.

As concerns attenuation, although the fundamental frequency of a 500K bits/s signaling rate is 250 kHz, the attenuation at 500 kHz is chosen so as to include the high-frequency components of the signal. For 500 meters of cable and using the 6-dB rule (see section 2.2), the maximum attenuation that can be tolerated is 0.36 dB/30 meters. As shown on the graph in Figure 3, the attenuation is a little over 0.5 dB/30m, exceeding the design constraint by 0.14 dB/30m. This is satisfactory in this example because it is acceptable to operate at slightly less noise margin than the conservative rule provides.

4 Eye Patterns

To measure the effects of signal distortion, noise and signal attenuation, and the resultant intersymbol interference (ISI) in a data transmission system, the eye pattern is used. ISI is the effect of preceding pulses in a pulse train interfering with succeeding pulses; it forces a reduction in the signaling rate for a given line length in order to maintain adequate distinction between adjacent pulses. The eye pattern is displayed on an oscilloscope, with the term *eye* coming from the appearance of the trace on the CRT.

4.1 Setting Up the Eye Pattern

The eye pattern is obtained by transmitting a pseudo-random nonreturn-to-zero (NRZ) code down the transmission line under test. This represents nearly all possible pulse combinations. The signal at the receiving end of the line is connected to the vertical amplifier of an oscilloscope, with the scope triggered using the synchronization clock to the NRZ code generator on a separate trace (see Figure 11).

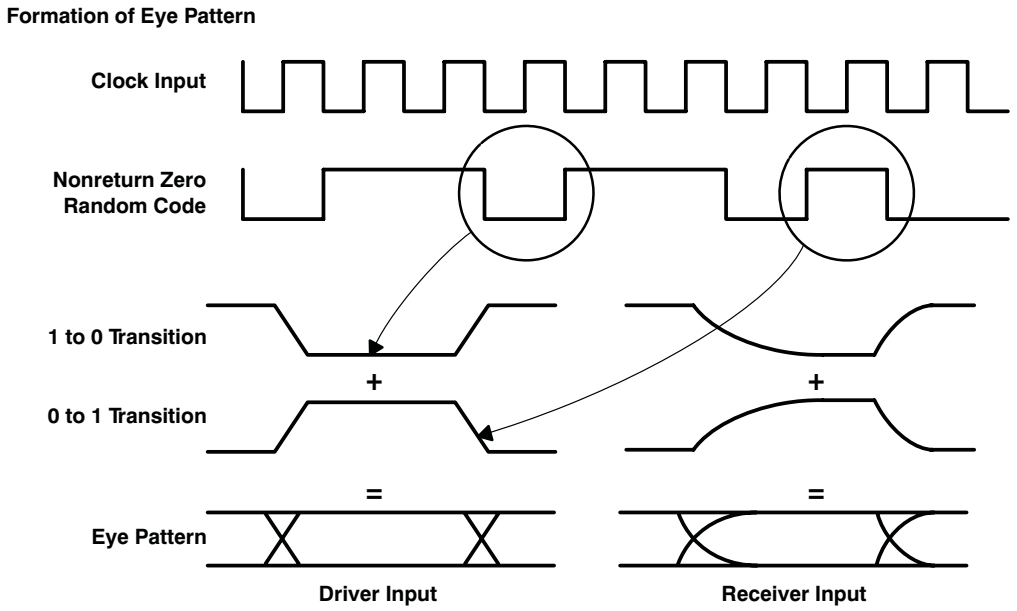


Figure 11. Signal Distortion Using Eye Patterns

Over any one unit interval, the pseudo-random code generator produces a combination of signals. The resulting signals then can be viewed on the oscilloscope over a one-unit interval; each unit interval resembles an eye similar to that shown in Figure 12. For differential transmission, both signals at the end of the transmission line are applied to separate amplifiers on the oscilloscope and then summed using the summation facility on the oscilloscope.

Figure 13 shows a circuit that generates the NRZ code. In this case, it was used to test the 485 SN75176-type transceiver.

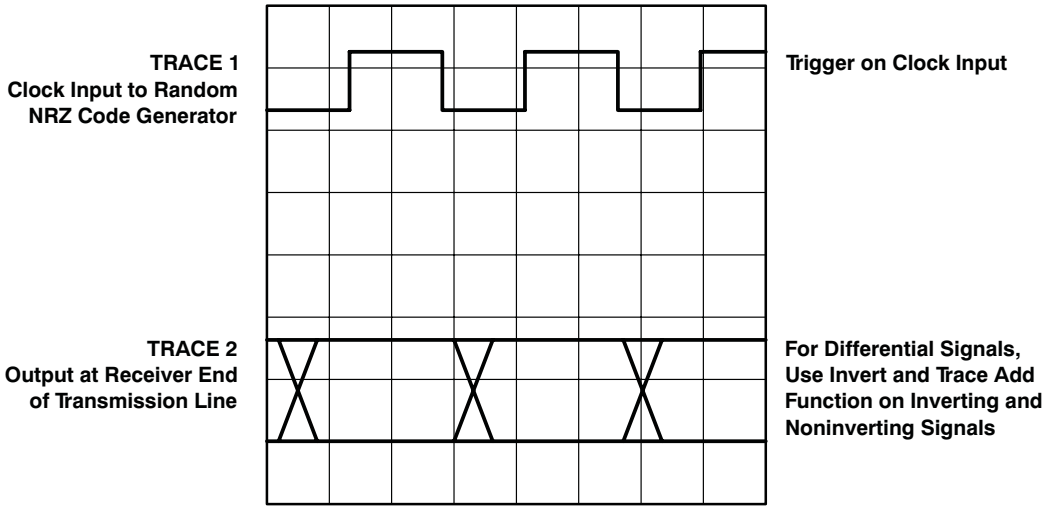


Figure 12. Eye Pattern Oscilloscope Trace

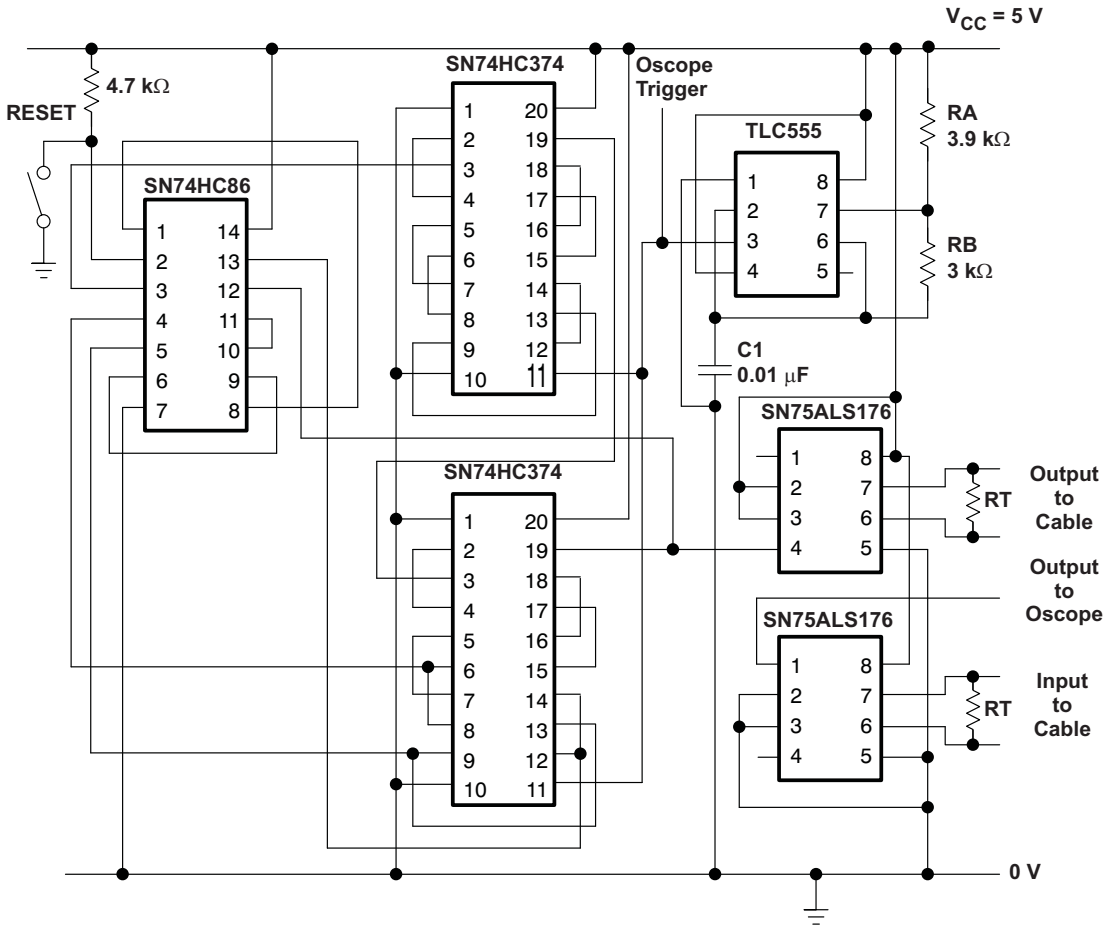


Figure 13. NRZ Random Code Generator

4.2 Taking Measurements From Eye Patterns

Before considering actual measurements, the first key indicator on the performance of the transmission system can be seen by simply looking at the eye pattern. The openness of the eye is an indication of the quality of the transmitted signal and is an indication of the noise and distortion tolerance of the system.

For actual measurements, the decision points of the transceiver are superimposed on the eye pattern. The vertical distance between the decision points and the signal trace is an approximate indication of the noise margin of the system. The horizontal appearance of the eye can be used to determine the maximum time jitter of the system. The maximum allowable jitter depends on the timing accuracy of the receiving circuitry. A conservative guide used by cable manufacturers to determine signaling rate versus line-length curves is no more than 5% jitter, where percent jitter is defined as the ratio of threshold crossing skew to unit interval as shown in Figure 14. Jitter is caused by a number of factors, including signal frequency, noise, and crosstalk. Noise frequency can modulate the transmitted signal, for example, 50-Hz hum or noise from other low-frequency sources. Also the effect of threshold misalignment can cause severe problems with the received signal, reducing the detected pulse width considerably.

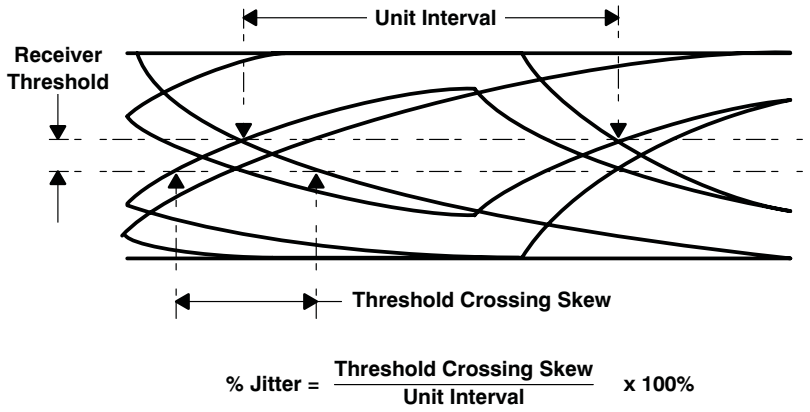


Figure 14. Measuring Signal Transmission Quality

5 References

1. *ANSI TIA/EIA-485-A Electrical Characteristics of Generators and Receivers for Use in Balanced Digital Multipoint Systems*, Global Engineering Documents, www.global.ihs.com
2. *TSB89 Application Guidelines for TIA/EIA-485*, Global Engineering Documents, www.global.ihs.com
3. *422 and 485 Standards Overview and Systems Configurations* application report (SLLA070)
4. *Comparing Bus Solutions* application report (SLLA067)

6 Summary

Data transmission circuits using Texas Instruments 485 drivers, receivers, and transceivers can be used wherever an application requires a rugged, economical interface between two or more devices. The balanced differential signals and wide common-mode voltage range at 485 provide a low-noise, reliable communications channel for signaling rates up to 50 million bits per second, and operation for distances up to 1200 meters.

Attention to design details such as transmission line termination and circuit loading gives optimum performance in a wide variety of applications.

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