RS-485 basics: When termination is necessary, and how to do it properly

Many signal integrity and communication issues with RS-485 networks stem from terminations, either from a lack of termination or improper termination. In this installment of the RS-485 basics series, I'll talk about when you can get away without terminating your RS-485 network, and if you need termination, how to use standard (parallel) terminations and alternating current (AC) termination networks.

As I discussed in the last installment of this series, an RS-485 transceiver's driver must be able to drive 1.5V across 32 unit loads and two 120Ω terminations. I didn't mention it in the post, but the 120Ω value for termination resistors stems from what is known as the differential-mode characteristic impedance of the twisted-pair bus wires. Simply put, the wire gauge, insulation type and thickness, and number of twists per unit length all contribute to an impedance that high-speed data signals "see." This impedance is denoted in ohms and typically ranges from 100Ω to 150Ω for twisted-pair cables. The writers of the RS-485 standard choose 120Ω as the nominal characteristic impedance; therefore, to match this impedance the termination resistors also have a default value of 120Ω.

Why termination networks exist

Matching the characteristic impedance of the cabling to the termination network enables the receiver on the end of the bus to see the maximum signal power. By leaving a transmission line unterminated, or terminated with some value unequal to the impedance of the cable, you are introducing a mismatch that creates reflections at the ends of the network. A reflection is where some of the energy of the signal literally returns back up the line, which can then constructively or destructively interfere with the next bits propagating down the bus. A destructive example is if the reflected signal which bounces back is out of phase with the incoming signal, resulting in the receiver seeing a smaller incoming signal. If the mismatch is large enough, the energy reflected back can cause subsequent bits to be misinterpreted and incorrectly decoded by the receiver.

Equation 1 shows that for the reflection coefficient, to approach zero, the input impedance, Z_L, needs to match the source impedance, Z_S. If there is a large discrepancy in load and source impedance, almost the entire signal can reflect.

$$\Gamma = \frac{Z_L - Z_S}{Z_L + Z_S} \qquad (1)$$

As you can see, for optimal signal integrity, it is always best to match the AC line impedance with a termination of equal value. Why wouldn't all designers want to do this? Because adding termination networks adds cost to the overall system, and these termination networks also add a parallel load to the drivers, causing larger steady-state load currents. In power-sensitive applications where lowering power consumption is critical (such as in battery-powered applications), one option to save power is to leave the bus unterminated. Let's discuss when removing termination is a viable option.

Networks that do not need termination

One situation in which you don't need termination networks is when the two-way loop time of the network is much greater than a single bit time (~<0.1×two-way loop delay). In such scenarios, the reflections will lose energy each time they reach an end of the network.

As you can see from Figure 1, the amplitude of the reflections will continue to decay each time the signal reflects at the end of the cable. Figure 1 shows three round trips for the signal and a total of six reflections.

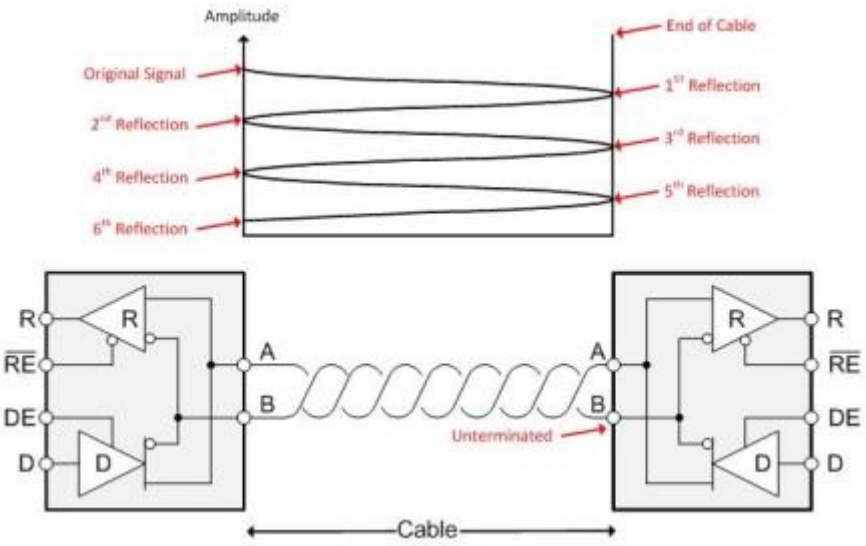

Figure 1: Amplitude of reflection decay each time a reflection occurs

Estimating that the unterminated end of the bus has a 96kΩ input impedance (a one-eighth unit load), and the source impedance of the driver is 60Ω, the signal reflections would decay according to the calculations listed in Table 1.

Signal	Percentage of signal	Calculation $\left(\frac{Z_L - Z_S}{Z_L + Z_S}\right)$
Original signal	100%	
After first reflection	99.75%	$1 * \left(\frac{96{,}000 - 120}{96{,}000 + 120}\right) = 0.9975$
After second reflection	-33.24%	$.9975 * \left(\frac{60 - 120}{60 + 120}\right) = -0.3324$
After third reflection	-33.16%	$-.3324 * \left(\frac{96{,}000 - 120}{96{,}000 + 120}\right) = -.3317$
After fourth reflection	11.05%	$-.3317 * \left(\frac{60 - 120}{60 + 120}\right) = 0.1106$
After fifth reflection	11.02%	$0.1106 * \left(\frac{96{,}000 - 120}{96{,}000 + 120}\right) = 0.1102$
After sixth reflection	-3.68%	$0.1102 * \left(\frac{60 - 120}{60 + 120}\right) = -0.0368$

Table 1: Example signal-decay calculations

As Table 1 shows, by the time the signal reflects for the sixth time, it has decayed to under 4% of its original magnitude. After this point it is safe to say that the reflections are no longer capable of causing signal-integrity issues. Since the sample point of a bit typically occurs between 50-75% of the way through the bit, you would want to make sure that these three round-trip delays occur before the sample point.

Networks that need termination

For applications where the bit time is not substantially longer than the loop time of the cable, termination is crucial for minimizing reflections. The most basic termination networks, which are known as standard termination or parallel

termination networks, consist of a single resistor (Figure 2).

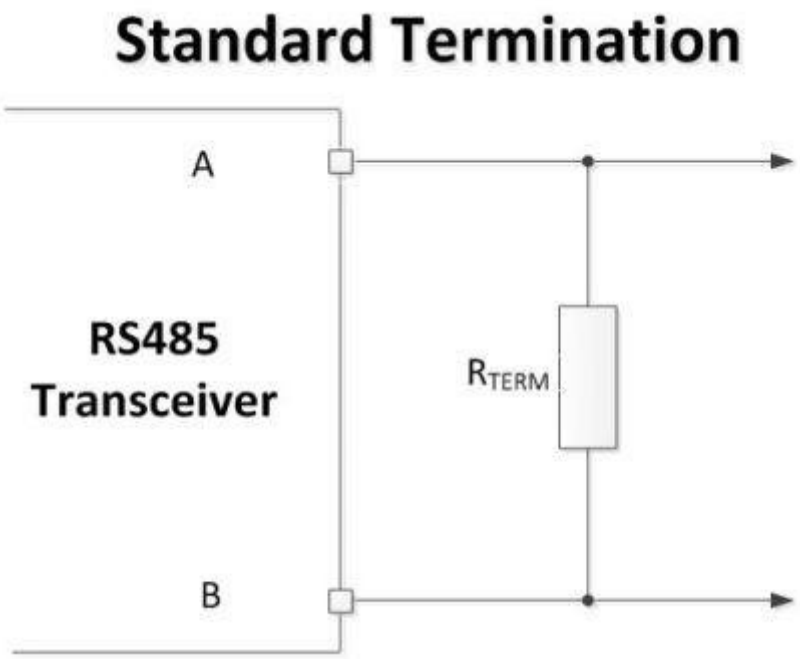

Figure 2: Standard termination network

For standard termination, you would match the termination resistor value with the differential-mode characteristic impedance of the cabling on both ends of the network. This ensures the proper termination of signals traveling in both directions on the bus. As I mentioned before, the major drawback for this type of termination scheme is that whenever the driver is active, the resistors are placing a direct current (DC) load on the driver.

Using AC terminations helps alleviate this power dissipation without having as long of a bit-time requirement with respect to bus length. Figure 3 shows an AC termination scheme.

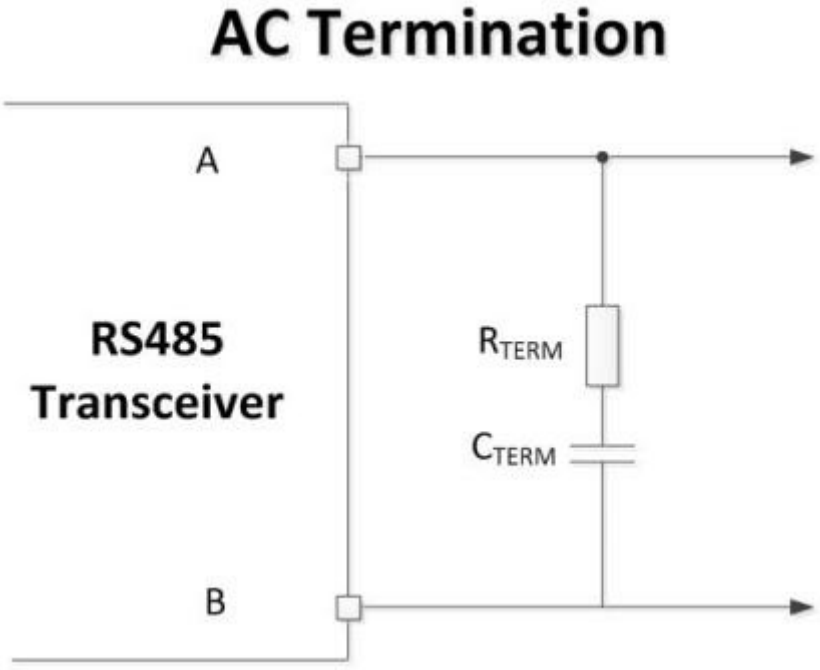

Figure 3: AC termination network

Since current typically flows from one side of an RS-485 driver through the termination network, then through the other side of the driver, by placing a series capacitor the steady state current goes to zero. The two caveats of this type of termination are that it requires one extra component on each termination network, and the series resistor and capacitor

introduce a resistor-capacitor (RC) delay. The RC time constant will slow the rising and falling edge of the differential signal and limit the maximum data rate of the network.

Table 2 summarizes the three termination scenarios.

Termination network	Power dissipation	Data rate	Signal integrity
No termination	Low	Low	Good at low data rates, poor at high data rates
Standard termination	High	High	Great
AC termination	Low	Medium	Good

Table 2: Summary of termination techniques

For optimal signal integrity, it is always best to match the differential-mode characteristic impedance of the cable with a termination of equal impedance. But if you take the proper steps, it is also possible to successfully implement AC terminations or avoid termination altogether.

As always, log in and leave a comment if there are any RS-485 topics you would like to hear more about.

Additional resources

- Read the RS-485 basics series on the Analog Wire and Industrial Strength blogs.
- Search TI's complete RS-485 portfolio.
- Share questions and knowledge with fellow engineers in the TI E2E™ Community Industrial Interface forum.

Guoxin Zhou Hi, John:

I'm studying the RS485 bus. I have a problem about whether the termination is needed in a RS485 bus.

I read a document, Interface Circuits for TIA/EIA-485 (RS-485),doc number SLLA036D.

From the section2.1 , I get information below:

The test for whether a transmission line is to be considered as a distributed- or a lumped-parameter model depends on the relationship of signal transition time, Tt, at the driver output and the propagation time, Tpd, of the signal down the cable.

If 2Tpd≥ Tt/5, the line should be treated as a distributed parameter model and terminated accordingly;otherwise, it can be treated as a lumped-parameter model and termination is unnecessary.

Summary1: If 10Tpd≥Tt, termination is necessary.

In your blog, I get information below:

One situation in which you don't need termination networks is when the two-way loop time of the network is much less than a single bit time (~<0.1×two-way loop delay). In such scenarios, the reflections will lose energy each time they reach an end of the network.

Summary2: If Tt<0.1 x two-way loop delay, temination is unnecessary.

I'm confused with these two summaries.

For a rs485 bus with 9600bps(communication baud rate) and 500 meters length cable, using summary1, termination is not needed. using summary2, termination is needed.

Could you give more explaination about the summary2.Best wishes.

John Griffith Hi Guoxin!

First I would like to apologize for missing this question and not responding sooner. Secondly, I would like to thank you for posting and brining the discrepancy to my attention. I made a mistake in my blog post and I meant to say is:

“One situation in which you don’t need termination networks is when the two-way loop time of the network is much greater than a single bit time (~ >10×two-way loop delay).”

Furthermore, if you then compare the application note you read which says 10 * TPD > tT to the summary of my statement in this blog of tBIT > 10 * tLOOP, they no longer contradict. The two way loop delay can be estimated for unshielded twisted pair copper to be 5ns/meter, multiplied by the length of the bus, multiplied by 2.

Thanks,

John

George Dishman Hi John,

I think it is important to note that the capacitor solution needs to have a time constant much less than the bit duration, otherwise the capacitor sits at zero volts (assuming there are ads many '1's as '0's) and does nothing to reduce power. If the capacitor fully charges during each bit, the drawback is that the stored voltage adds to the change of signal voltage at the start of the next bit hence the transient current through the resistor is double the value for resistor-only termination. Make sure there is enough drive power for the signal to be able to reach the receiver threshold and you don't get a hit on the data rate. If not, you can get delays that are data-dependent which can produce some interesting effects.

Best regards

George

John Griffith Hi George,

Thanks for the comment and additional details. I absolutely agree with you. I didn’t go into details but that is what I was referring to when I said “The RC time constant will slow the rising and falling edge of the differential signal and limit the maximum data rate of the network.” The bigger the RC constant the lower your maximum data rate can be. Said your way, the faster the data rate needed, the lower the maximum RC time constant can be (much less than bit duration).

In terms of driver strength I also I have aways seen AC termination capacitors smaller than a few nano-Farads and therefore the time constant is well under a micro-second. In my mind the limiting factor is not driver strength since there is a series 120Ω resistance limiting charge current, it is time. As long as you hold each bit time for more an a couple time constants the capacitor on the termination will charge and discharge. I like your point that the current charge in one state is of opposite polarity and 2 times that charge needs to be overcome to change to the opposite state.

Thanks again!

Marc Liu Hi John,

Thanks for your sharing.

About AC termination, I have a question: the total resistance is R+1/jwC, from which we can see the higher the frequency or capacitor, the lower the resistance, which helps get better signal integrity. Am I right?

But on the other hand, I think the lower the capacitor, the faster the signal reversal, which means better signal integrity.

Could you help with the relationship between capacitor value, signal integrity, and power consumption saving?

Thanks and best regards,

Marc

John Griffith Hi Marc,

Thanks for the question. I apologize; I don't have a formula readily available to share about the relationship of the capacitor and the data rate. Below is an app note that has some oscilloscope screen shots of an example set-up in the lab.

www.ti.com/.../slla070d.pdf

Also, I would recommend placing any additional questions on the industrial interface forum for product specific help from the current applications team. Below is a link to the forum:

e2e.ti.com/.../

Thanks,

John

John Griffith Hi Marc,

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Thanks,

John

Hao L Marc,

You can find some discussion in section 5 on page 7 of this app note www.ti.com/.../snla034b.pdf. It explains how to choose the cap value. If you still have questions, you're welcome to post them on e2e.ti.com. We would love to continue the discussion.

Regards,

Hao