Project Report of RISC-V CPU

(Course Project of Computer Architecture)

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1 Introduction

GitHub repository of my CPU project: https://github.com/Evensgn/RISC-V-CPU
This project is a RISC-V CPU with five-stage pipeline, implemented in Verilog HDL.

2 Design

Feature	RISC-V CPU
ISA	RISC-V (RV32I subset)
Pipelining	5 stages
Data forwarding	complete forwarding path
Cache	N-way set associate I-cache and D-cache

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3 Discusstion

4 Acknowledgements

Special thanks would go to Zhanghao Wu (吴章昊) for his instructive discusstions and useful suggestions on this project. I would like to express my gratitude to TA Zhekai Zhang (张哲恺) as well, for his MIPS CPU project (especially the code of cache and UART module) and much work for this assignment. I am also indebted to many other classmates for their direct and indirect help to me.

References

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