Low Cost FPGA based Implementation of a DRFM system

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***Abstract*—Digital Radio Frequency Memory (DRFM) is a technique used to record an incoming Radio Frequency (RF) signal, in turn applying a series of time-delays, amplitude scalings and frequency shifts and retransmitting the signal. This technique is used widely in the electronic defense industry as a form of radar jamming, in that it allows for the synthesis of artificial targets. This paper discusses the design of implementation of a DRFM system on a low cost FPGA system and documents this system's performance. Describe results of the implementation sdf sadf sdf asdf asdf asdfsdfasdfadfsd fsdlfjlsdjflsj sdjfl sdjfl jsdlf jsdlf jsdlfj sdljsdlfjsdl jasdfsdjl asdjflsdjl sdjfsdlfj sldfjaslf jdlfjsdlfaljflasjflk jsdlf jasdlfjaslfjsdflsjadlfsjadlf jsdfl jasdlf jsdlkf jasdlf jasdl jasdlasdjl asdjlj lfjadlfjsfjasdflajsflajsfljas lkasdf lsadj lfjsdfl a asdf asdf asd fasf asdf asd asd fasd fasdf asdf asdf asdf asd asd afasd fasdf sdfasf asdfsfsdfsdfsd dfg dfg dfg dfg sr wer sdfl ;'**

I. Introduction

A. Digital Radio Frequency Memory

Digital Radio Frequency Memory (DRFM) systems digitize and store incoming RF input signals at specific frequencies and bandwidths. The captured signals undergo time delays, frequency shifts and amplitude scalings, after which they are retransmitted. DRFM is used in order to synthesize false targets for radar systems by exploiting the radar assumptions of target identification. This is achieved by retransmitting a time delayed, amplitude scaled and frequency shifted coherent replica of the inputted signal, thereby making it, from the radar's perspective, indistinguishable from other genuine signals [1].

The reason why a radar system is deceived is due to its fundamental operation. A pulsed Doppler radar operates by transmitting pulses on a target and measuring the time delay and frequency shift of the return pulse from the target in order to infer information about a target's location and velocity. The implications of this are such that if we simulate echos with certain frequency shifts and time delays it is possible for a radar to identify a target incorrectly.

An illustration of a DRFM system may be seen in Fig. 1. It can be seen that the input signal is mixed down to intermediate frequency and then is sampled by an Analog to Digital Converter (ADC). The sample rate of the ADC is equal to the bandwidth of the incoming RF signal as the ADC is sampling complex I/Q data. The digitized signal is then stored in memory and may be manipulated by means of the control interface. The control interface is used to designate the various time delays, frequency shifts and amplitude scalings.

B. FPGA based acceleration

Due to the high data rates and the Digital Signal Processing (DSP) requirements the implementation DRFM systems are highly implementable on Field Programmable Gate Arrays (FPGA). Therefore this paper describes the design and implementation of a DRFM system on a low cost FPGA, namely the Altera MAX 10 [2].

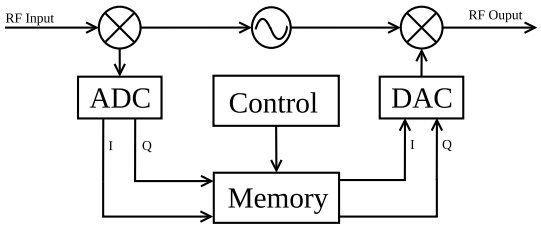

Fig. 1: Illustration of DRFM System

C. Plan of Development

This paper begins by discussing the conceptual design of the proposed DRFM architecture by giving an overview of its implementation. After which, the details of each subsystem is described. Finally, results are shown and conclusions are drawn based on the prototype design.

II. Overview

For means of explanation, the architecture of the FPGA based implemented DRFM system can be described by three subsystems. These being, the interfacing and control system, the external peripherals and the DSP system. Whereby each of the constituent systems are monitored and controlled by the top-level controller module. This simplified architecture may be seen in Fig. 2.

This being said, it must be noted that the architecture described in Fig. 2 has not yet been integrated into a RF front end and therefore this paper is a review of the work in progress. The implications of this are that although real time signal processing and data storage are realizable at the speeds dictated by the RF front-end, it has not been shown that this architecture is in fact capable of achieving such speeds.

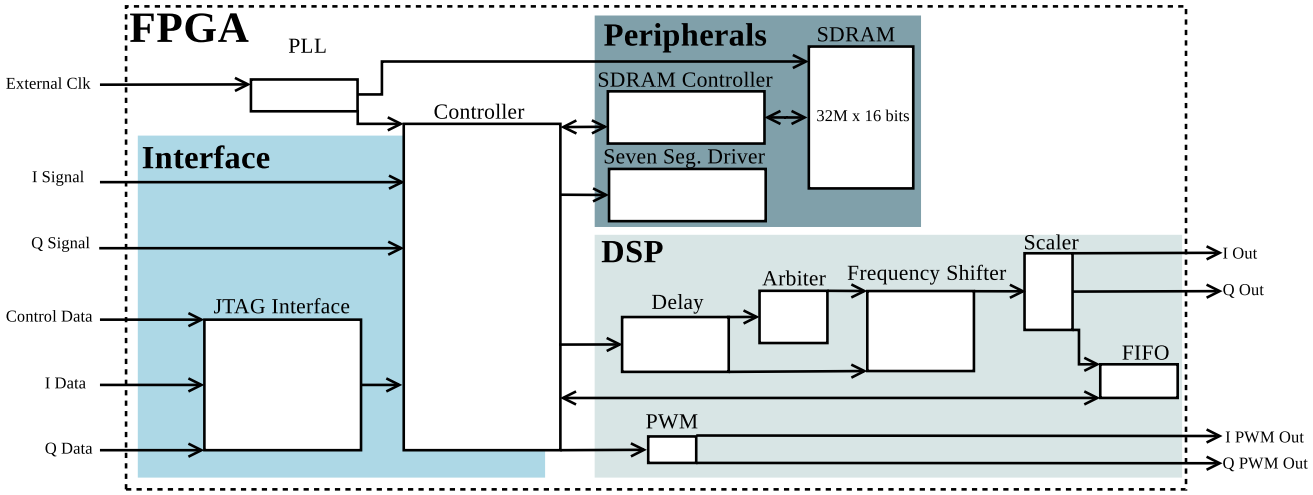

Fig. 2: Illustration of the implementation of the FPGA based DRFM System

A. JTAG Interface

Joint Action Test Group (JTAG) was originally used as a simplified standard for interconnectivity testing for PCB manufacturing. It was created as a result of Integrated Circuits (IC) pins becoming more densely spaced and therefore classical interconnectivity test approaches were infeasible. The JTAG protocol mitigated the need for physical access to an IC's pins through the use of shift register chains.

In the JTAG standard (IEEE 1149.1) the collections of shift registers are referred to as Boundary Scan Cells (BSCs) which sample and hold data from and to the pin interface. As a result the BSCs can be configured into a serial shift chain thereby allowing to be driving by a serial interface.

The JTAG interface implemented on the DRFM system allows for software based monitoring, updating and controlling of the DRFM system through the JTAG port. Through the use of the Altera Virtual JTAG Intellectual Property (IP) core it is possible to access to the JTAG control signals that are routed to the FPGA core, which allow for a fine control over the JTAG resources thereby granting real-time general purpose serial communication [3].

Through the use of a Python based User Interface (UI) that runs a TCL JTAG server it is possible to direc

B. External Peripherals

C. Signal Processing

1) *Time Delay:*
2) *Frequency shifting:*
3) *Fractional Amplitude Scaling:*

III. Methodology

IV. Design

A. System Peripherals

1) *PLL:*
2) *SDRAM Controller:*
3) *External SDRAM:*
4) *PWM:*

B. Interface

1) *JTAG Interface:*
2) *Controller:*

C. DRFM Subsystem

1) *Delay:*
2) *Arbiter:*
3) *Frequency Shifter:*
4) *Scaler:*

V. Results

VI. Conclusions and Future Work

A. Future Work

– Streaming to file. – DAC for sensing.

References

[1] S. J. Roome, "Digital radio frequency memory."
[2] *DE10-Lite User Manual*.
[3] *Virtual JTAG (altera_virtual_jtag) IP Core User Guide*.