ECE 440 - Project #6

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1 Trials and Tribulations

I ended up struggling the most with the net-selection part of the Debug Wizard. I found that selecting nets on the *outside* of the memory module led to a very weird name convention, but this was solved (after many iterations of Synthesis) by selecting the signals from within the memory instance.

Other than that, I thought I had done something wrong a few times because they post-debug Synthesis gave warnings of the constraints file containing unmatchable net-names. However, I suspect that the Debug Wizard creates these **set_property** commands in the constraints file for use during re-Synthesis, and those net names become obsolete afterwards – resulting in the warning. Ignoring this solved my 'problem.'

2 Debugging Results

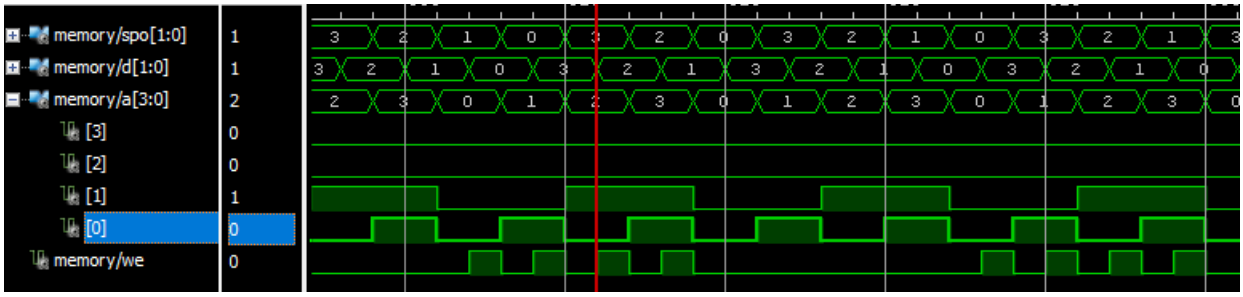

Figure 2.1: Results of the VIvado Debug window immediately before and after a trigger.