

Format: 120 minutes, 100 points, open notes, open book, calculator permitted.

***Please show all work to receive partial credit!***

1. (30) Dr. J is having trouble with his “xface” module on the final project and needs your help. The module supports two different interfaces: (1) an AXI Stream interface to the AXI Stream FIFO; and (2) a bundled data interface to the factorial module relying on “go” and “done” pulses, each 1-cc wide, to indicate when the data can be sampled.
  - (a) Develop a block diagram of the datapath for the xface module.
  - (b) Provide state graphs of any finite state machines, and a brief description of how the module operates.
2. (35) Jim decides he needs an FPGA system for calculating an arbitrary Fibonacci number,  $F_n$ , defined by the recurrence relation  $F_n = F_{n-1} + F_{n-2}$  and initialized with seed values  $F_0=0$  and  $F_1=1$ . This relation defines the Fibonacci sequence: 0, 1, 1, 2, 3, 5, 8, ...
  - (a) First, define how your system will interface to the “Outside World.” (clock, reset, etc.)
  - (b) Next, neatly sketch a complete datapath for your system
  - (c) Finally, neatly sketch the state graph of any finite state machines and a brief description of the system’s operation
3. (35) Develop a testbench that will generate random AXI Stream write transactions that could have been used to test the final project, as an alternative to using the traffic generator and stream FIFO.