ECE 440 - Project #2

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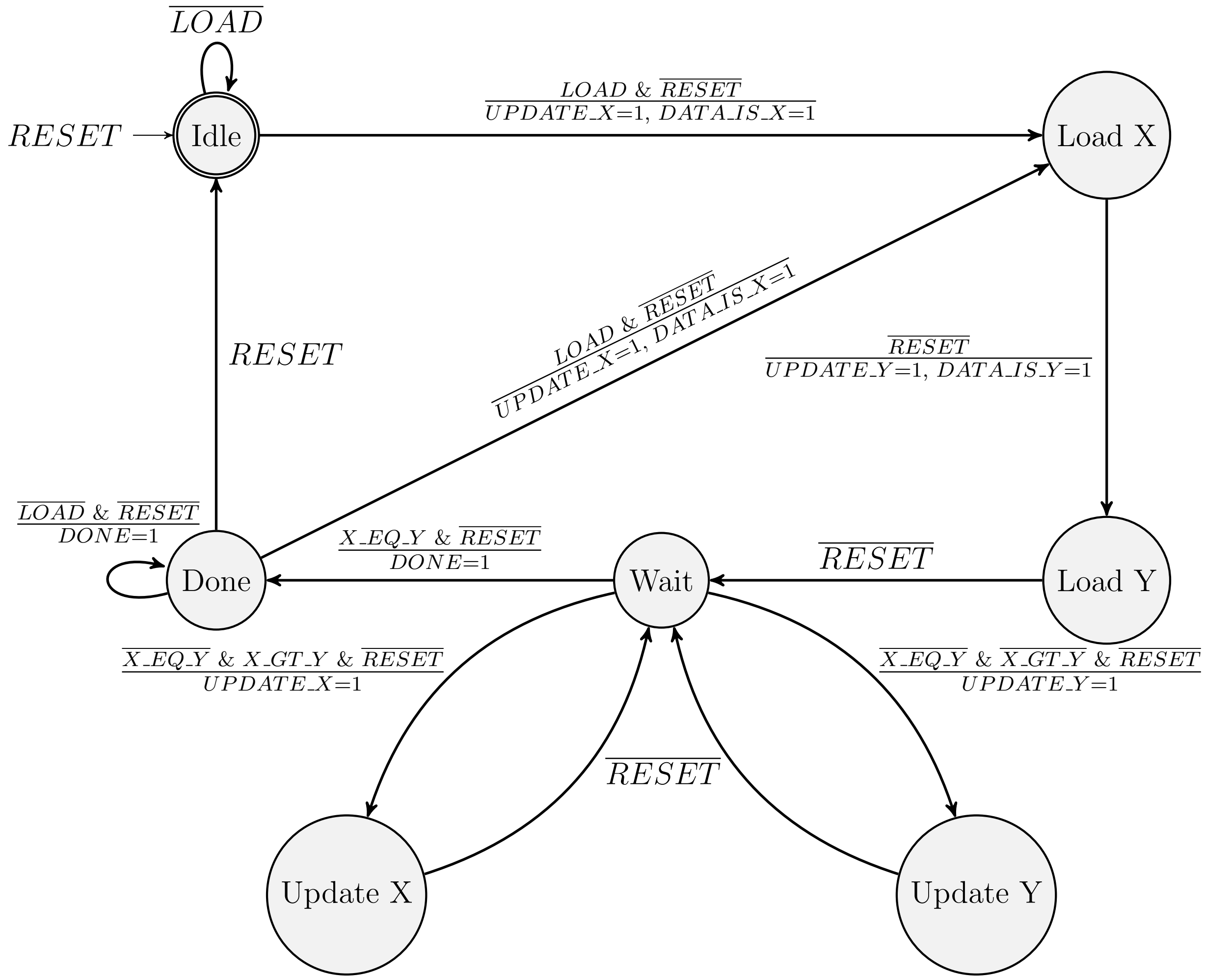
1 Design

1.1 Mealy Finite State Machine

The first step in my design process was to develop my mealy finite state machine, shown in **Figure 1.1**.



$\overline{LOAD}$
$RESET$
Idle
$\frac{LOAD \ \& \ \overline{RESET}}{UPDATE\_X{=}1,\ DATA\_IS\_X{=}1}$
Load X
$RESET$
$\frac{LOAD \ \& \ \overline{RESET}}{UPDATE\_X{=}1,\ DATA\_IS\_X{=}1}$
$\frac{\overline{RESET}}{UPDATE\_Y{=}1,\ DATA\_IS\_Y{=}1}$
$\frac{\overline{LOAD} \ \& \ \overline{RESET}}{DONE{=}1}$
Done
$\frac{X\_EQ\_Y \ \& \ \overline{RESET}}{DONE{=}1}$
Wait
$\overline{RESET}$
Load Y
$\frac{\overline{X\_EQ\_Y} \ \& \ X\_GT\_Y \ \& \ \overline{RESET}}{UPDATE\_X{=}1}$
$\frac{\overline{X\_EQ\_Y} \ \& \ \overline{X\_GT\_Y} \ \& \ \overline{RESET}}{UPDATE\_Y{=}1}$
$\overline{RESET}$
Update X
Update Y

Figure 1.1: Mealy Finite State Machine

The addition of the *Done* state is what specifically allows for the **DONE** signal to be asserted once a calculation has completed. One thing to note about this FSM is that the *Update X* and *Update Y* states are somewhat superfluous because the outputs are asserted on the transitions themselves. However, I kept these states inside the FSM to allow for the datapath to perform any necessary arithmetic (in this case $x - y$ and $y - x$) without worrying about the time required to properly evaluate **X_EQ_Y** and **X_GT_Y**. I did remove these states in my first design of this project, but it resulted in x and y being updated when they were not supposed to be, underflowing the result and timing out the simulation.

1.2 Datapath

The only required change (relative to the starting DP1 code) to my datapath was to utilize two subtractors to compute $x - y$ and $y - x$ simultaneously. This affected my implementation by requiring one less input to the datapath module (because there is no need to select which values to subtract). Otherwise, the GCD algorithm itself was implemented identically.

1.3 Problems

I first encountered a problem when the *Vivado*-generated inputs and outputs to my modules – those specified at the creation of the module itself – were not given the keyword **signal**. This resulted in me assuming it was superfluous, and thus my simulation failed for (seemingly) random reasons. I eventually realized the IDE did not insert the **signal** keyword, but it was necessary nonetheless.

One more error I made was failing to define the vector size for the **gcd_result** signal. This was not identified by *Vivado* as an error, but resulting in a simulation in which only bit 0 of the vector was being utilized by my datapath, and thus the algorithm was not performing as expected.

The final problem I encountered was due to me incorrectly creating the testbench **SystemVerilog** file, and I utilized it as a design source instead of exclusively a simulation source. This only became relevant when performing my post-synthesis simulation, and was inevitably fixed by treating that file as just a simulation source.

As I mentioned previously, attempting to implement the FSM without the *Update X* and *Update Y* states resulted in improper behavior. In the post-synthesis simulation the previous output of $UPDATE\_X = 1$ resulted in the sequential logic of the datapath module updating x and y (as at the clock-edge the output was still high, as the state transition hadn't completed) one too many times, and underflowing. This was only rectified by adding those states, slowing down the algorithm – but since we were not given specific timing requirements, this implementation is adequate.

2 Simulations

2.1 Behavioral Simulation

Due to the length of the simulation, I captured the Behavioral Simulation in four parts, shown below. My simulation was done with an input $x = 63$, and $y = 12$.

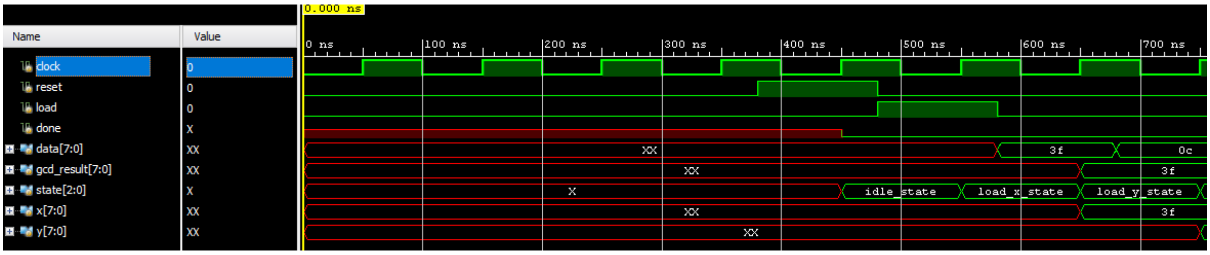
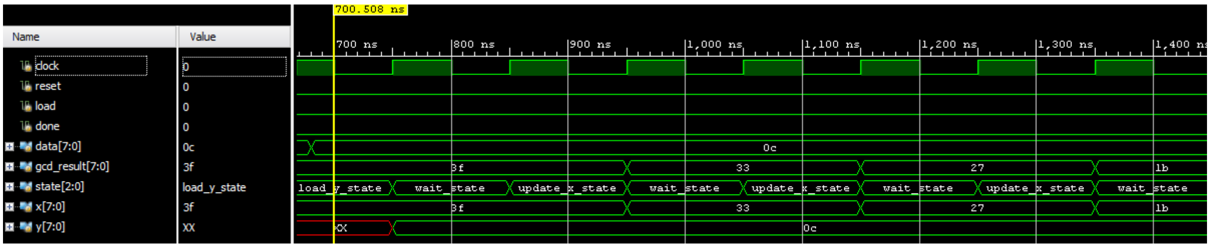
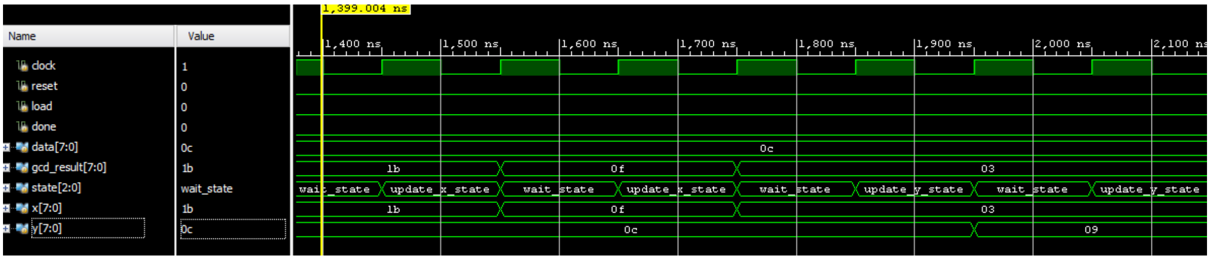


Figure 2.1: First 700 nanoseconds of the Behavioral Simulation.



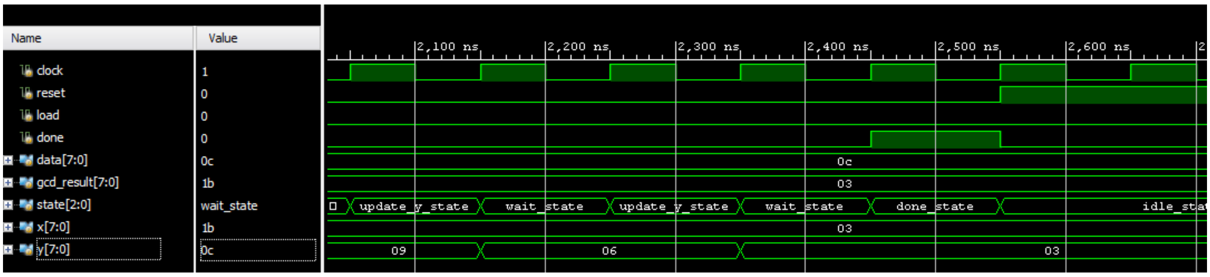
Name	Value
clock	0
reset	0
load	0
done	0
data[7:0]	0c
gcd_result[7:0]	3f
state[2:0]	load_y_state
x[7:0]	3f
y[7:0]	XX

Figure 2.2: Second 700 nanoseconds of the Behavioral Simulation.



Name	Value
clock	1
reset	0
load	0
done	0
data[7:0]	0c
gcd_result[7:0]	1b
state[2:0]	wait_state
x[7:0]	1b
y[7:0]	0c

Figure 2.3: Third 700 nanoseconds of the Behavioral Simulation.



Name	Value
clock	1
reset	0
load	0
done	0
data[7:0]	0c
gcd_result[7:0]	1b
state[2:0]	wait_state
x[7:0]	1b
y[7:0]	0c

Figure 2.4: Final 500 nanoseconds of the Behavioral Simulation.

As evident in the behavioral simulation, each relevant module functions as expected. After approximately 300 nanoseconds of resetting, the FSM transitions between the **Idle**, **Load X**, and **Load Y** states in three sequential clock cycles.

Afterwards, the changing values of **x** and **y** can be seen in the following pictures. The two values decrease in their respective states, until they're equal with a value of 3 (the correct result). Then, the **done** signal is asserted, followed by **reset**.

2.2 Post-Synthesis Simulation

I was able to capture the post-synthesis simulation with a single image, and the result exactly matches those of my behavioral simulation. Even the time it takes for the **done** signal to be asserted was identical to my previous simulation (which is good!).

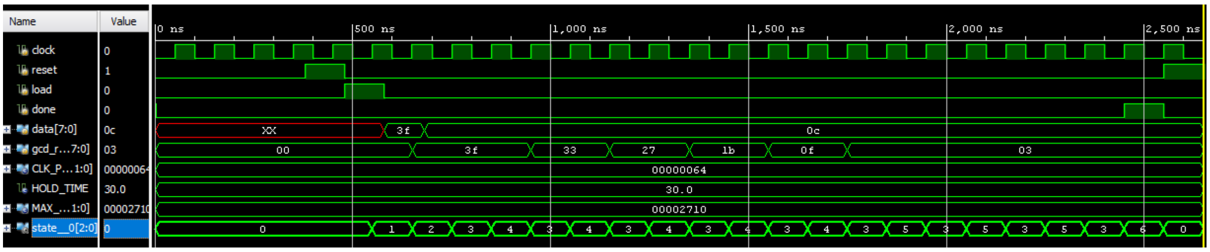


Figure 2.5: Complete Post-Synthesis Simulation.

3 Synthesis Report

```
#----------------------------------------------------------------------
# Vivado v2016.4 (64-bit)
# SW Build 1756540 on Mon Jan 23 19:11:23 MST 2017
# IP Build 1755317 on Mon Jan 23 20:30:07 MST 2017
# Start of session at: Tue Jan 28 15:37:08 2020
# Process ID: 396
# Current directory: U:/ECE 440/Project_2/Project_2.runs/synth_1
# Command line: vivado.exe -log gcd_core.vds -product Vivado -
    mode batch -messageDb vivado.pb -notrace -source gcd_core.tcl
# Log file: U:/ECE 440/Project_2/Project_2.runs/synth_1/gcd_core
    .vds
# Journal file: U:/ECE 440/Project_2/Project_2.runs/synth_1\
    vivado.jou
#----------------------------------------------------------------------
Sourcing tcl script 'C:/Xilinx/Vivado/2016.4/scripts/init.tcl'
source gcd_core.tcl -notrace
Command: synth_design -top gcd_core -part xc7z010clg400-1
Starting synth_design
Attempting to get a license for feature 'Synthesis' and/or
    device 'xc7z010'
INFO: [Common 17-349] Got license for feature 'Synthesis' and/or
     device 'xc7z010'
INFO: Launching helper process for spawning children vivado
    processes
INFO: Helper process launched with PID 21964
---------------------------------------------------------------------------------

Starting RTL Elaboration : Time (s): cpu = 00:00:05 ; elapsed =
    00:00:11 . Memory (MB): peak = 325.527 ; gain = 113.668
---------------------------------------------------------------------------------

INFO: [Synth 8-638] synthesizing module 'gcd_core' [U:/ECE 440/
    Project_2/Project_2.srcs/sources_1/new/gcd_core.sv:3]
INFO: [Synth 8-638] synthesizing module 'dp' [U:/ECE 440/
    Project_2/Project_2.srcs/sources_1/imports/new/dp.sv:2]
```

```
INFO: [Synth 8-256] done synthesizing module 'dp' (1#1) [U:/ECE
   440/Project_2/Project_2.srcs/sources_1/imports/new/dp.sv:2]
INFO: [Synth 8-638] synthesizing module 'fsm' [U:/ECE 440/
   Project_2/Project_2.srcs/sources_1/new/fsm.sv:2]
INFO: [Synth 8-155] case statement is not full and has no
   default [U:/ECE 440/Project_2/Project_2.srcs/sources_1/new/
   fsm.sv:30]
INFO: [Synth 8-256] done synthesizing module 'fsm' (2#1) [U:/ECE
    440/Project_2/Project_2.srcs/sources_1/new/fsm.sv:2]
INFO: [Synth 8-256] done synthesizing module 'gcd_core' (3#1) [U
   :/ECE 440/Project_2/Project_2.srcs/sources_1/new/gcd_core.sv
   :3]
---------------------------------------------------------------------------------

Finished RTL Elaboration : Time (s): cpu = 00:00:06 ; elapsed =
   00:00:12 . Memory (MB): peak = 362.766 ; gain = 150.906
---------------------------------------------------------------------------------


Report Check Netlist:
+------+------------------+-------+---------+-------+------------------+

|      |Item              |Errors |Warnings |Status |Description
          |
+------+------------------+-------+---------+-------+------------------+

|1     |multi_driven_nets |      0|        0|Passed |Multi
   driven nets |
+------+------------------+-------+---------+-------+------------------+

---------------------------------------------------------------------------------

Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:06 ;
   elapsed = 00:00:13 . Memory (MB): peak = 362.766 ; gain =
   150.906
---------------------------------------------------------------------------------

INFO: [Device 21-403] Loading part xc7z010clg400-1
INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints
Initializing timing engine
Parsing XDC File [U:/ECE 440/Project_2/Project_2.srcs/constrs_1/
   imports/Project_1/lab1_zybo.xdc]
WARNING: [Vivado 12-584] No ports matched 'swt[0]'. [U:/ECE 440/
   Project_2/Project_2.srcs/constrs_1/imports/Project_1/
   lab1_zybo.xdc:5]
```

```
CRITICAL WARNING: [Common 17-55] 'set_property' expects at least
     one object. [U:/ECE 440/Project_2/Project_2.srcs/constrs_1/
    imports/Project_1/lab1_zybo.xdc:5]
 Resolution: If [get_<value>] was used to populate the object,
    check to make sure this command returns at least one valid
    object.
WARNING: [Vivado 12-584] No ports matched 'swt[0]'. [U:/ECE 440/
    Project_2/Project_2.srcs/constrs_1/imports/Project_1/
    lab1_zybo.xdc:6]
CRITICAL WARNING: [Common 17-55] 'set_property' expects at least
     one object. [U:/ECE 440/Project_2/Project_2.srcs/constrs_1/
    imports/Project_1/lab1_zybo.xdc:6]
 Resolution: If [get_<value>] was used to populate the object,
    check to make sure this command returns at least one valid
    object.
WARNING: [Vivado 12-584] No ports matched 'swt[1]'. [U:/ECE 440/
    Project_2/Project_2.srcs/constrs_1/imports/Project_1/
    lab1_zybo.xdc:7]
CRITICAL WARNING: [Common 17-55] 'set_property' expects at least
     one object. [U:/ECE 440/Project_2/Project_2.srcs/constrs_1/
    imports/Project_1/lab1_zybo.xdc:7]
 Resolution: If [get_<value>] was used to populate the object,
    check to make sure this command returns at least one valid
    object.
WARNING: [Vivado 12-584] No ports matched 'swt[1]'. [U:/ECE 440/
    Project_2/Project_2.srcs/constrs_1/imports/Project_1/
    lab1_zybo.xdc:8]
CRITICAL WARNING: [Common 17-55] 'set_property' expects at least
     one object. [U:/ECE 440/Project_2/Project_2.srcs/constrs_1/
    imports/Project_1/lab1_zybo.xdc:8]
 Resolution: If [get_<value>] was used to populate the object,
    check to make sure this command returns at least one valid
    object.
WARNING: [Vivado 12-584] No ports matched 'swt[2]'. [U:/ECE 440/
    Project_2/Project_2.srcs/constrs_1/imports/Project_1/
    lab1_zybo.xdc:9]
CRITICAL WARNING: [Common 17-55] 'set_property' expects at least
     one object. [U:/ECE 440/Project_2/Project_2.srcs/constrs_1/
    imports/Project_1/lab1_zybo.xdc:9]
 Resolution: If [get_<value>] was used to populate the object,
    check to make sure this command returns at least one valid
    object.
WARNING: [Vivado 12-584] No ports matched 'swt[2]'. [U:/ECE 440/
    Project_2/Project_2.srcs/constrs_1/imports/Project_1/
    lab1_zybo.xdc:10]
CRITICAL WARNING: [Common 17-55] 'set_property' expects at least
     one object. [U:/ECE 440/Project_2/Project_2.srcs/constrs_1/
    imports/Project_1/lab1_zybo.xdc:10]
```

```
Resolution: If [get_<value>] was used to populate the object,
    check to make sure this command returns at least one valid
    object.
WARNING: [Vivado 12-584] No ports matched 'swt[3]'. [U:/ECE 440/
    Project_2/Project_2.srcs/constrs_1/imports/Project_1/
    lab1_zybo.xdc:11]
CRITICAL WARNING: [Common 17-55] 'set_property' expects at least
     one object. [U:/ECE 440/Project_2/Project_2.srcs/constrs_1/
    imports/Project_1/lab1_zybo.xdc:11]
Resolution: If [get_<value>] was used to populate the object,
    check to make sure this command returns at least one valid
    object.
WARNING: [Vivado 12-584] No ports matched 'swt[3]'. [U:/ECE 440/
    Project_2/Project_2.srcs/constrs_1/imports/Project_1/
    lab1_zybo.xdc:12]
CRITICAL WARNING: [Common 17-55] 'set_property' expects at least
     one object. [U:/ECE 440/Project_2/Project_2.srcs/constrs_1/
    imports/Project_1/lab1_zybo.xdc:12]
Resolution: If [get_<value>] was used to populate the object,
    check to make sure this command returns at least one valid
    object.
WARNING: [Vivado 12-584] No ports matched 'led[0]'. [U:/ECE 440/
    Project_2/Project_2.srcs/constrs_1/imports/Project_1/
    lab1_zybo.xdc:17]
CRITICAL WARNING: [Common 17-55] 'set_property' expects at least
     one object. [U:/ECE 440/Project_2/Project_2.srcs/constrs_1/
    imports/Project_1/lab1_zybo.xdc:17]
Resolution: If [get_<value>] was used to populate the object,
    check to make sure this command returns at least one valid
    object.
WARNING: [Vivado 12-584] No ports matched 'led[0]'. [U:/ECE 440/
    Project_2/Project_2.srcs/constrs_1/imports/Project_1/
    lab1_zybo.xdc:18]
CRITICAL WARNING: [Common 17-55] 'set_property' expects at least
     one object. [U:/ECE 440/Project_2/Project_2.srcs/constrs_1/
    imports/Project_1/lab1_zybo.xdc:18]
Resolution: If [get_<value>] was used to populate the object,
    check to make sure this command returns at least one valid
    object.
WARNING: [Vivado 12-584] No ports matched 'led[1]'. [U:/ECE 440/
    Project_2/Project_2.srcs/constrs_1/imports/Project_1/
    lab1_zybo.xdc:19]
CRITICAL WARNING: [Common 17-55] 'set_property' expects at least
     one object. [U:/ECE 440/Project_2/Project_2.srcs/constrs_1/
    imports/Project_1/lab1_zybo.xdc:19]
Resolution: If [get_<value>] was used to populate the object,
    check to make sure this command returns at least one valid
    object.
```

```
WARNING: [Vivado 12-584] No ports matched 'led[1]'. [U:/ECE 440/
    Project_2/Project_2.srcs/constrs_1/imports/Project_1/
    lab1_zybo.xdc:20]
CRITICAL WARNING: [Common 17-55] 'set_property' expects at least
     one object. [U:/ECE 440/Project_2/Project_2.srcs/constrs_1/
    imports/Project_1/lab1_zybo.xdc:20]
Resolution: If [get_<value>] was used to populate the object,
    check to make sure this command returns at least one valid
    object.
WARNING: [Vivado 12-584] No ports matched 'led[2]'. [U:/ECE 440/
    Project_2/Project_2.srcs/constrs_1/imports/Project_1/
    lab1_zybo.xdc:21]
CRITICAL WARNING: [Common 17-55] 'set_property' expects at least
     one object. [U:/ECE 440/Project_2/Project_2.srcs/constrs_1/
    imports/Project_1/lab1_zybo.xdc:21]
Resolution: If [get_<value>] was used to populate the object,
    check to make sure this command returns at least one valid
    object.
WARNING: [Vivado 12-584] No ports matched 'led[2]'. [U:/ECE 440/
    Project_2/Project_2.srcs/constrs_1/imports/Project_1/
    lab1_zybo.xdc:22]
CRITICAL WARNING: [Common 17-55] 'set_property' expects at least
     one object. [U:/ECE 440/Project_2/Project_2.srcs/constrs_1/
    imports/Project_1/lab1_zybo.xdc:22]
Resolution: If [get_<value>] was used to populate the object,
    check to make sure this command returns at least one valid
    object.
WARNING: [Vivado 12-584] No ports matched 'led[3]'. [U:/ECE 440/
    Project_2/Project_2.srcs/constrs_1/imports/Project_1/
    lab1_zybo.xdc:23]
CRITICAL WARNING: [Common 17-55] 'set_property' expects at least
     one object. [U:/ECE 440/Project_2/Project_2.srcs/constrs_1/
    imports/Project_1/lab1_zybo.xdc:23]
Resolution: If [get_<value>] was used to populate the object,
    check to make sure this command returns at least one valid
    object.
WARNING: [Vivado 12-584] No ports matched 'led[3]'. [U:/ECE 440/
    Project_2/Project_2.srcs/constrs_1/imports/Project_1/
    lab1_zybo.xdc:24]
CRITICAL WARNING: [Common 17-55] 'set_property' expects at least
     one object. [U:/ECE 440/Project_2/Project_2.srcs/constrs_1/
    imports/Project_1/lab1_zybo.xdc:24]
Resolution: If [get_<value>] was used to populate the object,
    check to make sure this command returns at least one valid
    object.
Finished Parsing XDC File [U:/ECE 440/Project_2/Project_2.srcs/
    constrs_1/imports/Project_1/lab1_zybo.xdc]
Completed Processing XDC Constraints
```

```
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

 Constraint Validation Runtime : Time (s): cpu = 00:00:00 ;
   elapsed = 00:00:00 . Memory (MB): peak = 653.980 ; gain =
   0.000
---------------------------------------------------------------------------------

 Finished Constraint Validation : Time (s): cpu = 00:00:13 ;
   elapsed = 00:00:22 . Memory (MB): peak = 653.980 ; gain =
   442.121
---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

 Start Loading Part and Timing Information
---------------------------------------------------------------------------------

 Loading part: xc7z010clg400-1
---------------------------------------------------------------------------------

 Finished Loading Part and Timing Information : Time (s): cpu =
   00:00:13 ; elapsed = 00:00:22 . Memory (MB): peak = 653.980 ;
    gain = 442.121
---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

 Start Applying 'set_property' XDC Constraints
---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

 Finished applying 'set_property' XDC Constraints : Time (s): cpu
    = 00:00:13 ; elapsed = 00:00:22 . Memory (MB): peak =
   653.980 ; gain = 442.121
---------------------------------------------------------------------------------

INFO: [Synth 8-802] inferred FSM for state register 'state_reg'
   in module 'fsm'
INFO: [Synth 8-5544] ROM "state" won't be mapped to Block RAM
   because address size (3) smaller than threshold (5)
INFO: [Synth 8-5544] ROM "state" won't be mapped to Block RAM
   because address size (1) smaller than threshold (5)
INFO: [Synth 8-5544] ROM "state" won't be mapped to Block RAM
   because address size (1) smaller than threshold (5)
```

```
-----------------------------------------------------------------------

                 State |                      New Encoding |
                           Previous Encoding
-----------------------------------------------------------------------

            idle_state |                               000 |
                                  000
          load_x_state |                               001 |
                                001
          load_y_state |                               010 |
                                010
            wait_state |                               011 |
                                  011
        update_x_state |                               100 |
                              100
        update_y_state |                               101 |
                              101
            done_state |                               110 |
                                  110
-----------------------------------------------------------------------

INFO: [Synth 8-3354] encoded FSM with state register 'state_reg'
    using encoding 'sequential' in module 'fsm'
-----------------------------------------------------------------------

 Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:13 ;
   elapsed = 00:00:22 . Memory (MB): peak = 653.980 ; gain =
   442.121
-----------------------------------------------------------------------


 Report RTL Partitions:
+-+--------------+-----------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+-----------+----------+
+-+--------------+-----------+----------+
-----------------------------------------------------------------------

 Start RTL Component Statistics
-----------------------------------------------------------------------

 Detailed RTL Component Info :
+---Adders :
           3 Input      8 Bit       Adders := 2
+---Registers :
                        8 Bit     Registers := 2
                        1 Bit     Registers := 5
```

```
+---Muxes :
           2 Input      8 Bit        Muxes := 2
          11 Input      3 Bit        Muxes := 1
           6 Input      1 Bit        Muxes := 6
---------------------------------------------------------------------------------
Finished RTL Component Statistics
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start RTL Hierarchical Component Statistics
---------------------------------------------------------------------------------
Hierarchical RTL Component report
Module dp
Detailed RTL Component Info :
+---Adders :
           3 Input      8 Bit       Adders := 2
+---Registers :
                        8 Bit    Registers := 2
+---Muxes :
           2 Input      8 Bit        Muxes := 2
Module fsm
Detailed RTL Component Info :
+---Registers :
                        1 Bit    Registers := 5
+---Muxes :
          11 Input      3 Bit        Muxes := 1
           6 Input      1 Bit        Muxes := 6
---------------------------------------------------------------------------------
Finished RTL Hierarchical Component Statistics
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Part Resource Summary
---------------------------------------------------------------------------------
Part Resources:
DSPs: 80 (col length:40)
BRAMs: 120 (col length: RAMB18 40 RAMB36 20)
---------------------------------------------------------------------------------
Finished Part Resource Summary
---------------------------------------------------------------------------------
```

```
---------------------------------------------------------------------------------
Start Cross Boundary and Area Optimization
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Cross Boundary and Area Optimization : Time (s): cpu =
   00:00:14 ; elapsed = 00:00:23 . Memory (MB): peak = 653.980 ;
    gain = 442.121
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+-----------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+-----------+----------+
+-+--------------+-----------+----------+
---------------------------------------------------------------------------------
Start Timing Optimization
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Applying XDC Timing Constraints
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Applying XDC Timing Constraints : Time (s): cpu =
   00:00:22 ; elapsed = 00:00:31 . Memory (MB): peak = 653.980 ;
    gain = 442.121
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Timing Optimization : Time (s): cpu = 00:00:22 ;
   elapsed = 00:00:31 . Memory (MB): peak = 653.980 ; gain =
   442.121
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+-----------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+-----------+----------+
+-+--------------+-----------+----------+
---------------------------------------------------------------------------------
Start Technology Mapping
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Technology Mapping : Time (s): cpu = 00:00:22 ; elapsed
    = 00:00:31 . Memory (MB): peak = 653.980 ; gain = 442.121
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start IO Insertion
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Flattening Before IO Insertion
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Flattening Before IO Insertion
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Final Netlist Cleanup
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Final Netlist Cleanup
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished IO Insertion : Time (s): cpu = 00:00:22 ; elapsed =
   00:00:31 . Memory (MB): peak = 653.980 ; gain = 442.121
---------------------------------------------------------------------------------
```

```
Report Check Netlist:
+------+------------------+-------+---------+------+------------------+
|      |Item              |Errors |Warnings |Status |Description
         |
+------+------------------+-------+---------+------+------------------+
|1     |multi_driven_nets |      0|        0|Passed |Multi
   driven nets |
+------+------------------+-------+---------+------+------------------+
---------------------------------------------------------------------------
Start Renaming Generated Instances
---------------------------------------------------------------------------
---------------------------------------------------------------------------
Finished Renaming Generated Instances : Time (s): cpu = 00:00:22
    ; elapsed = 00:00:31 . Memory (MB): peak = 653.980 ; gain =
   442.121
---------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------
Start Rebuilding User Hierarchy
---------------------------------------------------------------------------
---------------------------------------------------------------------------
Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:22 ;
   elapsed = 00:00:31 . Memory (MB): peak = 653.980 ; gain =
   442.121
---------------------------------------------------------------------------
---------------------------------------------------------------------------
Start Renaming Generated Ports
---------------------------------------------------------------------------
```

```
---------------------------------------------------------------------------------
Finished Renaming Generated Ports : Time (s): cpu = 00:00:22 ;
   elapsed = 00:00:31 . Memory (MB): peak = 653.980 ; gain =
   442.121
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Handling Custom Attributes
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Handling Custom Attributes : Time (s): cpu = 00:00:22 ;
    elapsed = 00:00:31 . Memory (MB): peak = 653.980 ; gain =
   442.121
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Renaming Generated Nets
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Renaming Generated Nets : Time (s): cpu = 00:00:22 ;
   elapsed = 00:00:31 . Memory (MB): peak = 653.980 ; gain =
   442.121
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-------+------+
|      |Cell   |Count |
+------+-------+------+
|1     |BUFG   |     1|
|2      |CARRY4 |     5|
|3      |LUT2   |    16|
|4      |LUT3   |    18|
|5      |LUT4   |    12|
|6      |LUT5   |     4|
|7      |LUT6   |     3|
|8      |FDRE   |    24|
|9      |IBUF   |    11|
|10     |OBUF   |     9|
+------+-------+------+

Report Instance Areas:
+------+-----------+-------+------+
|      |Instance   |Module |Cells |
+------+-----------+-------+------+
|1     |top        |       |   103|
|2     |  datapath |dp     |    65|
|3     |  fsm      |fsm    |    17|
+------+-----------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:22 ;
   elapsed = 00:00:31 . Memory (MB): peak = 653.980 ; gain =
   442.121
---------------------------------------------------------------------------------
Synthesis finished with 0 errors, 0 critical warnings and 0
   warnings.
Synthesis Optimization Runtime : Time (s): cpu = 00:00:12 ;
   elapsed = 00:00:16 . Memory (MB): peak = 653.980 ; gain =
   112.254
Synthesis Optimization Complete : Time (s): cpu = 00:00:22 ;
   elapsed = 00:00:32 . Memory (MB): peak = 653.980 ; gain =
   442.121
INFO: [Project 1-571] Translating synthesized netlist
INFO: [Netlist 29-17] Analyzing 16 Unisim elements for
   replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU
   seconds
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

INFO: [Common 17-83] Releasing license: Synthesis
26 Infos, 16 Warnings, 16 Critical Warnings and 0 Errors
   encountered.
synth_design completed successfully
```

```
synth_design: Time (s): cpu = 00:00:20 ; elapsed = 00:00:24 .
   Memory (MB): peak = 653.980 ; gain = 410.898
INFO: [Common 17-600] The following parameters have non-default
   value.
general.maxThreads
INFO: [Common 17-1381] The checkpoint 'U:/ECE 440/Project_2/
   Project_2.runs/synth_1/gcd_core.dcp' has been generated.
report_utilization: Time (s): cpu = 00:00:00 ; elapsed =
   00:00:00.015 . Memory (MB): peak = 653.980 ; gain = 0.000
INFO: [Common 17-206] Exiting Vivado at Tue Jan 28 15:37:42
   2020...
```

4 Source Code

Listing 4.1: Finite State Machine Module

```
‘timescale 1ns / 1ps
module fsm(
  input logic clock,
  input logic reset,
  input logic load,
  input logic x_equal_y,
  input logic x_greater_y,
  output logic update_x,
  output logic data_is_x,
  output logic update_y,
  output logic data_is_y,
  output logic done);

// State machine enumeration
typedef enum logic [2:0] {idle_state, load_x_state,
   load_y_state, wait_state, update_x_state, update_y_state,
    done_state} statetype;
statetype state;  // Current state of the machine

always_ff @(posedge clock)
begin
if (reset)  // Move to the idle state if RESET is asserted
  begin
  state <= idle_state;
  update_x = 0;
  data_is_x = 0;
  update_y = 0;
  data_is_y = 0;
  done = 0;
  end
else
  case (state)
```

```
      idle_state:
        begin
        if (load)
          begin
          state <= load_x_state;
          update_x = 1;
          data_is_x = 1;
          update_y = 0;
          data_is_y = 0;
          done = 0;
          end
        else
          begin
          state <= idle_state;
          update_x = 0;
          data_is_x = 0;
          update_y = 0;
          data_is_y = 0;
          done = 0;
          end
        end
      load_x_state:
        begin
        state <= load_y_state;
        update_x = 0;
        data_is_x = 0;
        update_y = 1;
        data_is_y = 1;
        done = 0;
        end
      load_y_state:
        begin
        state <= wait_state;
        update_x = 0;
        data_is_x = 0;
        update_y = 0;
        data_is_y = 0;
        done = 0;
        end
      wait_state:
        begin
        if (~x_equal_y && x_greater_y) // Replacing x state
          begin
          state <= update_x_state;
          update_x = 1;
          data_is_x = 0;
          update_y = 0;
          data_is_y = 0;
          done = 0;
          end
         else if (~x_equal_y && ~x_greater_y)
          begin
          state <= update_y_state;
          update_x = 0;
          data_is_x = 0;
          update_y = 1;
          data_is_y = 0;
          done = 0;
          end
        else
          begin
          state <= done_state;
          update_x = 0;
          data_is_x = 0;
          update_y = 0;
          data_is_y = 0;
          done = 1;
          end
        end
      update_x_state, update_y_state:
        begin
        state <= wait_state;
        update_x = 0;
        data_is_x = 0;
        update_y = 0;
        data_is_y = 0;
        done = 0;
        end
      done_state:
        begin
        if (~load)
          begin
          state <= done_state;
          update_x = 0;
          data_is_x = 0;
          update_y = 0;
          data_is_y = 0;
          done = 1;
          end
        else
          begin
          state <= load_x_state;
          update_x = 1;
          data_is_x = 1;
          update_y = 0;
          data_is_y = 0;
          done = 0;
          end
        end
    endcase
  end

  endmodule
```

Listing 4.2: Datapath Module

```
`timescale 1ns / 1ps
module dp(
    input logic clock,
    input logic update_x,
    input logic data_is_x,
    input logic update_y,
    input logic data_is_y,
    input logic [7:0] data,
    output logic x_equal_y,
    output logic x_greater_y,
    output logic [7:0] gcd_result);

// Internal Signals
logic [7:0] x_min_y, y_min_x;   // Result of x-y, and y-x
logic [7:0] x, y;               // Storage containers for x,
    y

// Generate output comparison signals
assign x_equal_y = (x == y);
assign x_greater_y = (x > y);

// Compute internal subtraction results
assign x_min_y = (x - y);
assign y_min_x = (y - x);

// Update values of x and y
always_ff @(posedge clock)
begin
if (update_x)
    x <= (data_is_x ? data : x_min_y);

if (update_y)
    y <= (data_is_y ? data : y_min_x);
end
```

```
// Assert temporary output as (x)
assign gcd_result = x;

endmodule
```

Listing 4.3: GCD Core Module

```
`timescale 1ns / 1ps

module gcd_core(
    input logic clock,
    input logic reset,
    input logic load,
    input logic [7:0] data,
    output logic [7:0] gcd_result,
    output logic done);

    logic update_x, data_is_x, update_y, data_is_y,
       x_equal_y, x_greater_y;

    dp datapath(.*);
    fsm fsm(.*);
endmodule
```

Listing 4.4: Testbench

```
`timescale 1ns / 1ps

module testbench();
    parameter CLK_PRD = 100;
    parameter HOLD_TIME = (CLK_PRD * 0.3);
    parameter MAX_SIM_TIME = (100 * CLK_PRD);

    // Internal logic signals
    logic clock, reset, load, done;
    logic [7:0] data, gcd_result;

    // Instantiate the GCD core as a UUT
    gcd_core uut(.*);

    initial #(MAX_SIM_TIME) $finish;

    initial begin
        clock <= 0;
        forever #(CLK_PRD / 2) clock = ~clock;
    end
    initial begin
        reset = 0; load = 0;
        data = 8'bx;

        // Global Reset
        #100;

        // Stimulate
        @(posedge clock);

        #HOLD_TIME;

        repeat(2) #CLK_PRD;
        reset = 1; #CLK_PRD; reset = 0;

        // Assert Load, X, Y
        load = 1;                     #CLK_PRD;
        load = 0; data = 8'd63; #CLK_PRD;
        data = 8'd12;              #CLK_PRD;

        begin: run_loop
            forever begin
                @(posedge clock);
                if (done) begin
                    reset = 1; #CLK_PRD;
                    $finish;
                end
            end
        end

        $finish;
    end
endmodule
```