ECE 440 - Project #1

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1 Vivado Messages

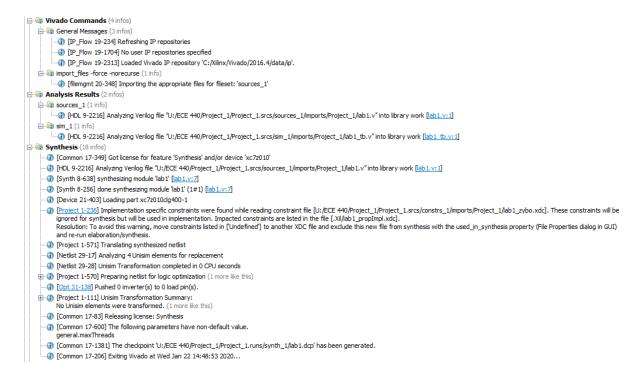


Figure 1: Screenshot 1 of the Vivado Messages screen.

```
implementation (3 warnings, 74 infos)
   Design Initialization (8 infos)
         (1) [Netlist 29-17] Analyzing 4 Unisim elements for replacement

    (I) [Netlist 29-28] Unisim Transformation completed in 1 CPU seconds

         (1) [Project 1-479] Netlist was created with Vivado 2016.4
         (1) [Device 21-403] Loading part xc7z010clg400-1

    (i) [Project 1-570] Preparing netlist for logic optimization.

         (1) [Project 1-111] Unisim Transformation Summary:
             No Unisim elements were transformed.
          (i) [Project 1-604] Checkpoint was created with Vivado v2016.4 (64-bit) build 1756540
         (i) [Vivado_Td 4-424] Cannot write hardware definition file as there are no IPI block design hardware handoff files present
   infos)
         (1) [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7z010'
         (1) [Project 1-461] DRC finished with 0 Errors
         (i) [Project 1-462] Please refer to the DRC report (report_drc) for more information.
         (1) [Timing 38-35] Done setting XDC timing constraints.
         (i) [Opt 31-49] Retargeted 0 cell(s).
       in [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s). (1 more like this)

    (i) [Opt 31-10] Eliminated 0 cells.

       ⊕ (1 more like this)
       (1 more like this)
         (1) [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.</p>

    (1) [Common 17-83] Releasing license: Implementation

         (1) [Common 17-600] The following parameters have non-default value.
             general.maxThreads
         (i) [Common 17-1381] The checkpoint 'U:/ECE 440/Project_1/Project_1.runs/impl_1/lab1_opt.dcp' has been generated.
       (Coretcl 2-168) The results of DRC are in file lab1 drc opted.rpt.
   Place Design (13 infos)
         (1) [Chipscope 16-241] No debug cores found in the current design.
             Before running the implement debug core command, either use the Set Up Debug wizard (GUI mode)
             or use the create_debug_core and connect_debug_core Tcl commands to insert debug cores into the design.
         (1) [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7z010'
       in [DRC 23-27] Running DRC with 8 threads (1 more like this)
       ⊕ ⊕ (I more like this)
⊕ (1 more like this)
       ⊕ (Ivivado_Td 4-199) Please refer to the DRC report (report_drc) for more information. (1 more like this)
         (1) [Place 30-611] Multithreading enabled for place_design using a maximum of 8 CPUs
         (1) [Timing 38-35] Done setting XDC timing constraints.
         (1) [Common 17-83] Releasing license: Implementation
         (1) [Common 17-600] The following parameters have non-default value.
             general.maxThreads
          (1) [Common 17-1381] The checkpoint 'U: /ECE 440/Project_1/Project_1.runs/impl_1/lab1_placed.dcp' has been generated.
```

Figure 2: Screenshot 2 of the Vivado Messages screen.

```
Route Design (2 warnings, 19 infos)
       (i) [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7z010'
       (1) [Vivado_Tcl 4-198] DRC finished with 0 Errors
       (i) [Vivado Tcl 4-199] Please refer to the DRC report (report drc) for more information.
       (i) [Route 35-254] Multithreading enabled for route_design using a maximum of 8 CPUs
      1 [Route 35-64] No timing constraints were detected. The router will operate in resource-optimization mode.
       (1) [Route 35-16] Router Completed Successfully
      ·· (1) [Common 17-83] Releasing license: Implementation
      (Common 17-600) The following parameters have non-default value.
           general.maxThreads
      (Common 17-1381) The checkpoint 'U:/ECE 440/Project_1/Project_1.runs/impl_1/lab1_routed.dcp' has been generated.
   (1 more like this)
       (i) [Coretd 2-168] The results of DRC are in file lab1 drc routed.rpt.
       (1) [DRC 23-133] Running Methodology with 8 threads
      (Coretd 2-1520) The results of Report Methodology are in file <a href="mailto:lab1 methodology drc routed.rpt">lab1 methodology drc routed.rpt</a>.
   (2 more like this)
      (Timing 38-91) UpdateTimingParams: Speed grade: -1, Delay Type: min_max.
      (1) [Timing 38-191] Multithreading enabled for timing update using a maximum of 8 CPUs

    [] [Timing 38-313] There are no user specified timing constraints. Timing constraints are needed for proper timing analysis.

      (1) [Power 33-232] No user defined docks were found in the design! Resolution: Please specify docks using create_dock/create_generated_dock for sequential elements. For pure combinatorial circuits, please specify a virtual dock, otherwise the vectorless estimation might be inaccurate
(i) [Netlist 29-17] Analyzing 4 Unisim elements for replacement
       (i) [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

    [Project 1-479] Netlist was created with Vivado 2016.4

       (1) [Device 21-403] Loading part xc7z010clg400-1
       (i) [Project 1-570] Preparing netlist for logic optimization

    [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

       (i) [Project 1-604] Checkpoint was created with Vivado v2016.4 (64-bit) build 1756540
       (1) [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7z010'
      (I) [DRC 23-27] Running DRC with 8 threads
      -(1) [DRC 23-20] Rule violation (ZPS7-1) PS7 block required - The PS7 cell must be used in this Zynq design in order to enable correct default configuration.
       (i) [Vivado 12-3199] DRC finished with 0 Errors, 1 Warnings
       (i) [Vivado 12-3200] Please refer to the DRC report (report_drc) for more information.
       (i) [Vivado 12-1842] Bitgen Completed Successfully.

    (Project 1-120) WebTalk data collection is mandatory when using a WebPACK part without a full Vivado license. To see the specific WebTalk data collected for your design, open the usage_statistics_webtalk.html or usage_statistics_webtalk.xml file in the implementation directory.
    (Common 17-83) Releasing license: Implementation

       (i) [Vivado_Tcl 4-395] Unable to parse hwdef file lab 1.hwdef
```

Figure 3: Screenshot 3 of the Vivado Messages screen.

```
infos) implemented Design (2 errors, 11 warnings, 34 infos)
   infos)

    [Netlist 29-17] Analyzing 4 Unisim elements for replacement

          (I) [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
          (Project 1-479) Netlist was created with Vivado 2016.4
          (i) [Project 1-570] Preparing netlist for logic optimization
          (1) [Project 1-111] Unisim Transformation Summary:
             No Unisim elements were transformed.
         [1] [Timing 38-313] There are no user specified timing constraints. Timing constraints are needed for proper timing analysis.
   infos) aunch_simulation -mode post-implementation -type timing (18 infos)
          (i) [SIM-utils 51] Simulation object is 'sim_1'
          (i) [SIM-utils 31] Writing simulation netlist file for design 'impl_1'...
          🚯 [SIM-utils 32] write_verilog -mode timesim -nolib -sdf_anno true -force -file "U:/ECE 440/Project_1/Project_1.sim/sim_1/impl/timing/lab1_tb_time_impl.v"
          (i) [SIM-utils 34] Writing SDF file...
          🚯 [SIM-utils 35] write_sdf -mode timesim -process_corner slow -force -file "U:/ECE 440/Project_1/Project_1.sim/sim_1/impl/timing/lab1_tb_time_impl.sdf"
          (i) [SIM-utils 36] Netlist generated:U:/ECE 440/Project 1/Project 1.sim/sim 1/impl/timing/lab1 tb time impl.v
          (i) [SIM-utils 37] SDF generated:U:/ECE 440/Project_1/Project_1.sim/sim_1/impl/timing/lab1_tb_time_impl.sdf
          (i) [USF-XSim 37] Inspecting design source files for 'lab1_tb' in fileset 'sim_1'...
          (i) [USF-XSim 2] XSim::Compile design
          (I) [USF-XSim 3] XSim::Elaborate design
       🖫 🕕 [USF-XSim 61] Executing 'COMPILE and ANALYZE' step in 'U:/ECE 440/Project_1/Project_1.sim/sim_1/impl/timing' (2 more like this)
       ⊕ 1 [USF-XSim 69] 'compile' step finished in '2' seconds (1 more like this)
          (i) [USF-XSim 4] XSim::Simulate design
          (I) [USF-XSim 98] *** Running xsim
         source lab1_tb.tcl (2 infos)
         (1) [USF-XSim 96] XSim completed, Design snapshot 'lab1 tb time impl' loaded.
         ·· 🕕 [USF-XSim 97] XSim simulation ran for 200ns
   image connect_hw_server (3 infos)
         (1) [Labtools 27-2285] Connecting to hw_server url TCP:localhost:3121
          (1) [Labtools 27-2222] Launching hw_server...
          (1) [Labtools 27-2221] Launch Output:
              ***** Xilinx hw_server v2016.4
              **** Build date : Jan 23 2017-19:37:29
              ** Copyright 1986-2016 Xilinx, Inc. All Rights Reserved.
```

Figure 4: Screenshot 4 of the Vivado Messages screen.

```
info)
          [Labtoolstd 44-466] Opening hw_target localhost:3121/xilinx_tcf/Digilent/210279A430C8A
    info) refresh_hw_device -update_hw_probes false [lindex [get_hw_devices xc7z010_1] 0] (1 info)
         [Labtools 27-1435] Device xc7z010 (JTAG device index = 1) is not programmed (DONE status = 0).
    program_hw_devices [lindex [get_hw_devices xc7z010_1] 0] (1 info)
          [Labtools 27-3164] End of startup status: HIGH
    refresh_hw_device [lindex [get_hw_devices xc7z010_1] 0] (2 errors, 10 warnings, 3 infos)
         . [Labtoolstd 44-130] No matching hw_ilas were found. (7 more like this)
            ① [Labtools 27-2269] No devices detected on target localhost:3121/xilinx_tcf/Digilent/210279A430C8A.
Check cable connectivity and that the target board is powered up then
use the disconnect_hw_server and connect_hw_server to re-register this hardware target.
            • [Labtoolstd 44-513] HW Target shutdown. Closing target: localhost:3121/xilinx_tcf/Digilent/210279A430C8A

    [Labtoolstcl 44-466] Opening hw_target localhost:3121/xilinx_tcf/Digilent/210279A430C8A

         1 [Labtools 27-1434] Device xc7z010 (JTAG device index = 1) is programmed with a design that has no supported debug core(s) in it. (1 more like this)
         [Labtools 2/-5123] The debug nub core was not detected at Ose State Chain. 2 St. St. Resolution:

1. Make sure the clock connected to the debug hub (dbg_hub) core is a free running clock and is active OR

2. Manually launch hw server with e "set xsdb-user-bscan <C_USER_SCAN_CHAIN scan_chain_number" to detect the debug hub at User Scan Chain of 2 or 4. To determine the user scan chain setting, open the implemented design and use: get_property C_USER_SCAN_CHAIN [get_debug_cores dbg_hub]. (1 more like this)
■ Simulation (2 infos)
            (IXSIM 43-3451] SDF backannotation process started with SDF file "lab1_tb_time_impl.sdf", for root module "lab1_tb/dut".
            (I) [XSIM 43-3452] SDF backannotation was successful for SDF file "lab1_tb_time_impl.sdf", for root module "lab1_tb/dut".
```

Figure 5: Screenshot 5 of the Vivado Messages screen.

2 Vivado Synthesis Report

```
# IP Build 1755317 on Mon Jan 23 20:30:07 MST 2017
```

Start of session at: Wed Jan 22 14:48:18 2020

Process ID: 17812

Current directory: U:/ECE 440/Project_1/Project_1.runs/synth_1

Command line: vivado.exe -log lab1.vds -product Vivado -mode batch -messageDb vivad

Log file: U:/ECE 440/Project_1/Project_1.runs/synth_1/lab1.vds

Journal file: U:/ECE 440/Project_1/Project_1.runs/synth_1\vivado.jou

#-----

Sourcing tcl script 'C:/Xilinx/Vivado/2016.4/scripts/init.tcl'

source lab1.tcl -notrace

Command: synth_design -top lab1 -part xc7z010clg400-1

Starting synth_design

Attempting to get a license for feature 'Synthesis' and/or device 'xc7z010'

INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7z010'

INFO: Launching helper process for spawning children vivado processes

INFO: Helper process launched with PID 5396

Starting RTL Elaboration : Time (s): cpu = 00:00:05 ; elapsed = 00:00:12 . Memory (MB

INFO: [Synth 8-638] synthesizing module 'lab1' [U:/ECE 440/Project_1/Project_1.srcs/s

INFO: [Synth 8-256] done synthesizing module 'lab1' (1#1) [U:/ECE 440/Project_1/Proje

Finished RTL Elaboration : Time (s): cpu = 00:00:06; elapsed = 00:00:12. Memory (MB

Report Check Netlist:

1 multi_driven_nets 0 0 Passed Multi driven nets		Item		J		Description	 +
++	1		1	•	•	•	•

Finished RTL Optimization Phase 1: Time (s): cpu = 00:00:06; elapsed = 00:00:13. M

INFO: [Device 21-403] Loading part xc7z010clg400-1

INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints

Initializing timing engine

Parsing XDC File [U:/ECE 440/Project_1/Project_1.srcs/constrs_1/imports/Project_1/lab Finished Parsing XDC File [U:/ECE 440/Project_1/Project_1.srcs/constrs_1/imports/Proj INFO: [Project 1-236] Implementation specific constraints were found while reading co Resolution: To avoid this warning, move constraints listed in [.Xil/lab1_propImpl.xdc Completed Processing XDC Constraints

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.006 . M
Finished Constraint Validation : Time (s): cpu = 00:00:13 ; elapsed = 00:00:23 . Memo
Start Loading Part and Timing Information
Loading part: xc7z010clg400-1
Finished Loading Part and Timing Information : Time (s): cpu = 00:00:13 ; elapsed = 0
Start Applying 'set_property' XDC Constraints
Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:13 ; elapsed
Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:13 ; elapsed = 00:00:23 . M
Report RTL Partitions:
RTL Partition Replication Instances
+-++ ++
Start RTL Component Statistics
Detailed RTL Component Info :
Finished RTL Component Statistics
Start RTL Hierarchical Component Statistics
Hierarchical RTL Component report
Finished RTL Hierarchical Component Statistics
Start Part Resource Summary
Part Resources: DSPs: 80 (col length:40) BRAMs: 120 (col length: RAMB18 40 RAMB36 20)
Finished Part Resource Summary

Start Cross Boundary and Area Optimization
Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:13 ; elapsed =
Report RTL Partitions:
RTL Partition Replication Instances
Start Timing Optimization
Start Applying XDC Timing Constraints
Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:22 ; elapsed = 00:00
Finished Timing Optimization : Time (s): cpu = 00:00:22 ; elapsed = 00:00:32 . Memory
Report RTL Partitions:
RTL Partition Replication Instances
Start Technology Mapping
Finished Technology Mapping : Time (s): cpu = 00:00:22 ; elapsed = 00:00:32 . Memory
Report RTL Partitions:
RTL Partition Replication Instances
Start IO Insertion
Start Flattening Before IO Insertion

	ed Flattening Before							
Start	Final Netlist Cleanu	p						
 Finish	ed Final Netlist Cle							
	ed IO Insertion : Ti	me (s): cpu = 00:0	0:22 ; e	lapsed	= 00:00	:32 .	Memory (MB)	:
	Check Netlist:		.	4			ı	
		Errors Warnings	Status	Descri	iption		1	
1	-+ multi_driven_nets -+	0 0	Passed	Multi	driven	nets	I	
Finish Report +-+ RTL +-+	ed Renaming Generate RTL Partitions: Partition Replicat	d Instances : Time						32
 Start :	Rebuilding User Hier	archy						
Finish	ed Rebuilding User H				:22 ; el	apsed	= 00:00:32	•
 Start :	Renaming Generated P	 orts 						
Finish	ed Renaming Generate	d Ports : Time (s)	 : cpu =	00:00:2	22 ; ela	 .psed :	= 00:00:32 .	M
 Start :	Handling Custom Attr							

```
Finished Handling Custom Attributes: Time (s): cpu = 00:00:22; elapsed = 00:00:32.
   -----
Start Renaming Generated Nets
Finished Renaming Generated Nets: Time (s): cpu = 00:00:22; elapsed = 00:00:32. Me
______
Start Writing Synthesis Report
Report BlackBoxes:
+-+----+
| |BlackBox name |Instances |
+-+----+
+-+----+
Report Cell Usage:
+----+
    |Cell |Count |
+----+
    |LUT1 |
12
    |LUT2 |
  |LUT3 | 1|
|IBUF | 4|
13
   |OBUF | 4|
15
+----+
Report Instance Areas:
+----+
    |Instance |Module |Cells |
+----+
    ltop
           +----+
______
Finished Writing Synthesis Report: Time (s): cpu = 00:00:22; elapsed = 00:00:32. M
______
Synthesis finished with 0 errors, 0 critical warnings and 0 warnings.
Synthesis Optimization Runtime: Time (s): cpu = 00:00:12; elapsed = 00:00:17. Memo
Synthesis Optimization Complete: Time (s): cpu = 00:00:22; elapsed = 00:00:32. Mem
INFO: [Project 1-571] Translating synthesized netlist
INFO: [Netlist 29-17] Analyzing 4 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in O CPU seconds
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Opt 31-138] Pushed O inverter(s) to O load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.
```

INFO: [Common 17-83] Releasing license: Synthesis

15 Infos, O Warnings, O Critical Warnings and O Errors encountered.

synth_design completed successfully

synth_design: Time (s): cpu = 00:00:20 ; elapsed = 00:00:25 . Memory (MB): peak = 642

INFO: [Common 17-600] The following parameters have non-default value.

general.maxThreads

INFO: [Common 17-1381] The checkpoint 'U:/ECE 440/Project_1/Project_1.runs/synth_1/lareport_utilization: Time (s): cpu = 00:00:00; elapsed = 00:00:00.015. Memory (MB):

INFO: [Common 17-206] Exiting Vivado at Wed Jan 22 14:48:53 2020...