ECE 440 - Homework #5

Collin Heist

10th February 2020

1 Timing Diagrams

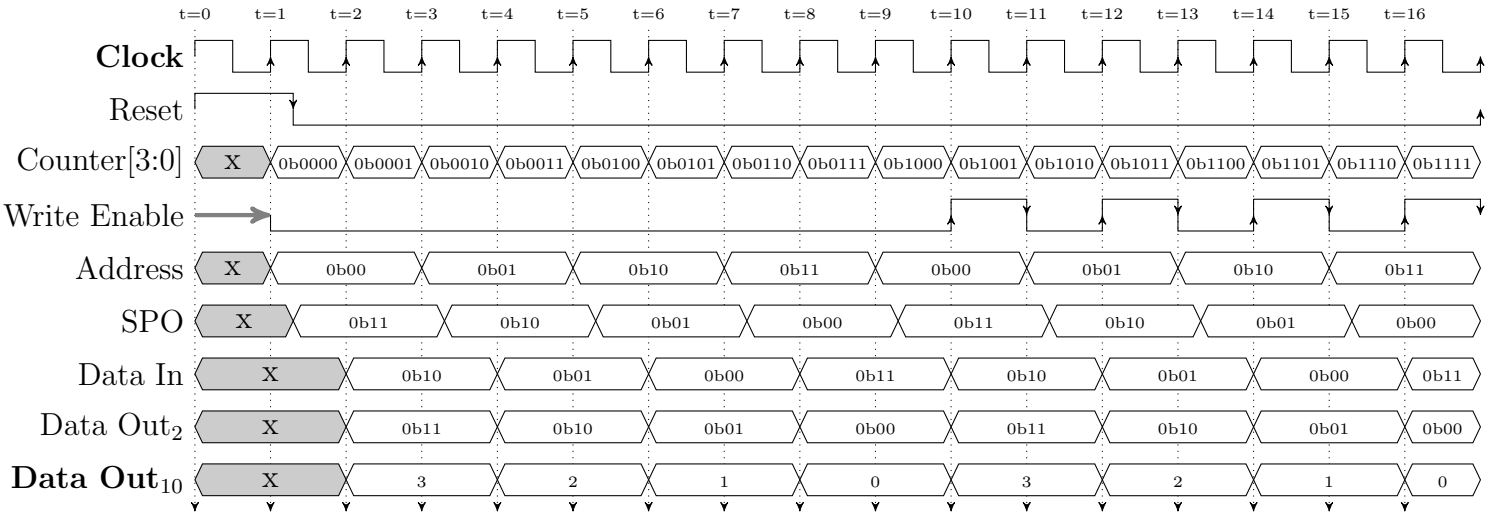

Figure 1: First counter cycle.

During each full cycle of the 4-bit counter, the **Write-Enable** signal goes high four times (at time 9, 11, 13, and 15). During each of these periods, the currently selected address (in order 0, 1, 2 and 3) is overwritten with one less than its current value. The output is a sequential reading of the memory module (repeated twice), reading 3-2-1-0 at first.

The second full-sequence of the timer shows the pattern of this circuit completely.

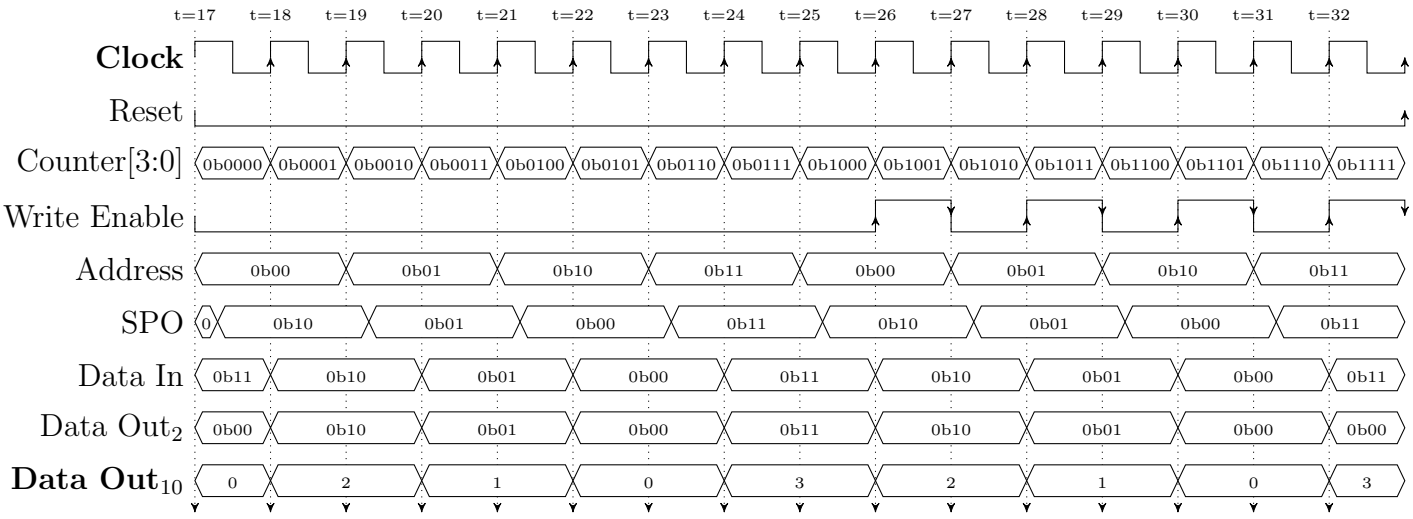

Figure 2: The second counter cycle.

As discussed previously, on each of the write-enable pulses the currently-selected address is written with its current value minus one. Now the output of the entire circuit is that newly-subtracted values; resulting in 2-1-0-3 (a rotating shift on the original contents in memory).

The following two cycles of the counter follow this same pattern, resulting in the same sequence of events, but a further rotated output that is: 1-0-3-2 and then 0-3-2-1. The timing diagrams for these cycles are shown below.

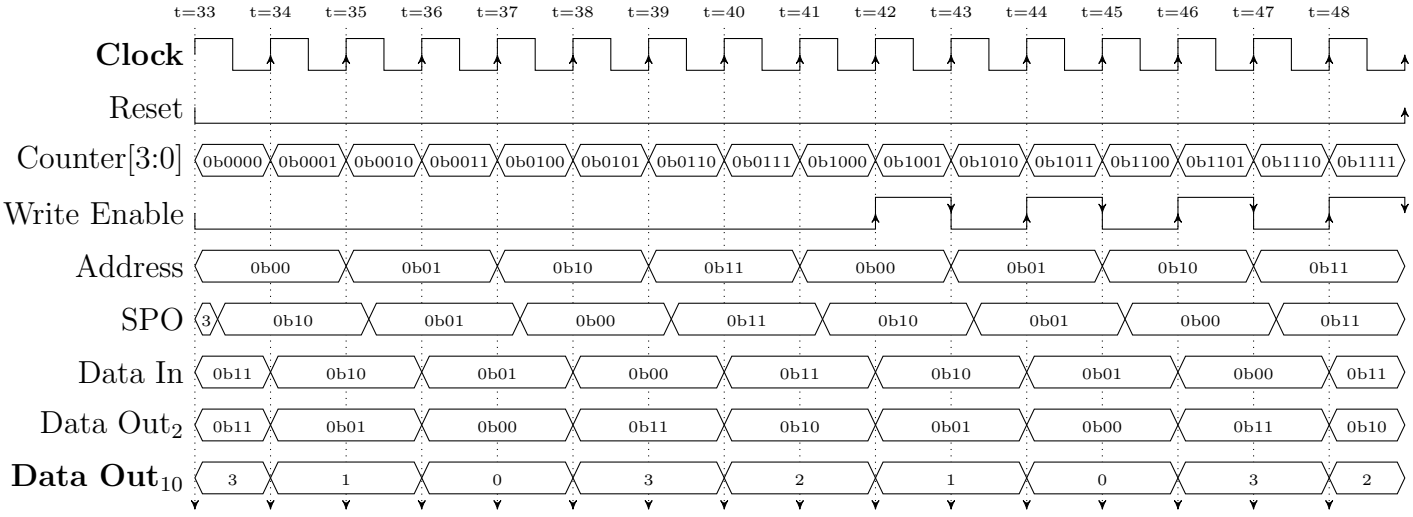

Figure 3: The third counter cycle.

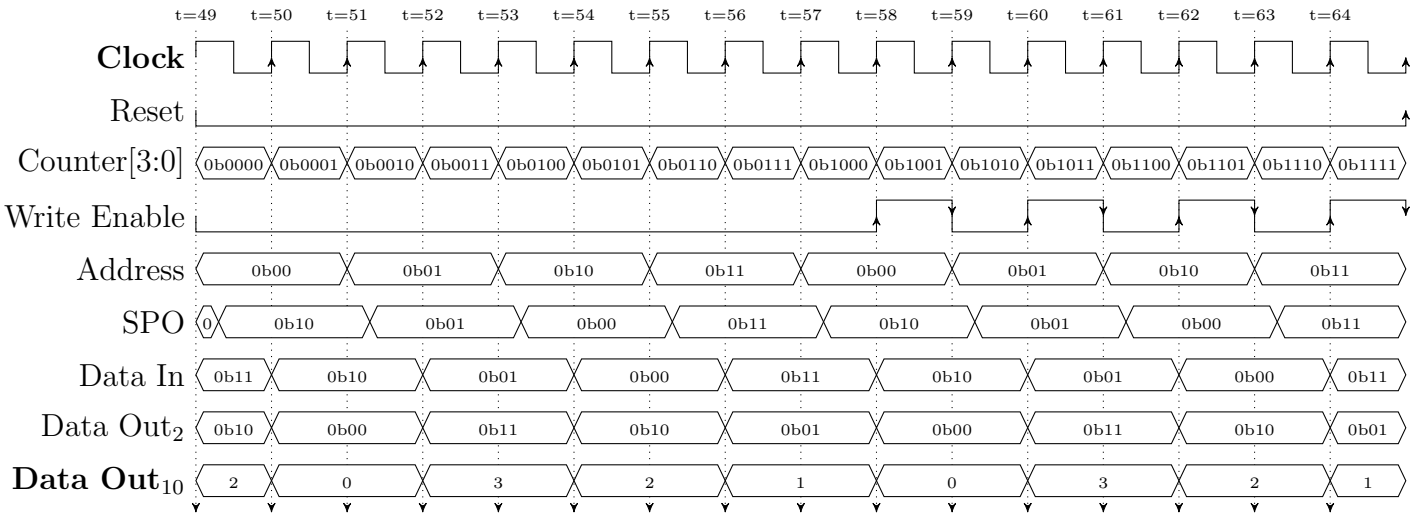

Figure 4: The fourth counter cycle.

2 Summary

In summary, the output of the circuit is as follows:

Outputs				Continued Sequence		
3	**2**	**1**	**0**	-	-	-
3	**2**	**1**	**0**	-	-	-
2	1	0	**3**	**2**	**1**	**0**
2	1	0	**3**	**2**	**1**	**0**
1	0	**3**	**2**	**1**	**0**	-
1	0	**3**	**2**	**1**	**0**	-
0	**3**	**2**	**1**	**0**	-	-
0	**3**	**2**	**1**	**0**	-	-
⋮	⋮	⋮	⋮	⋮	⋮	⋮

After these four cycles, the sequence is complete and restarts from the beginning.