ECE 440- Final Exam

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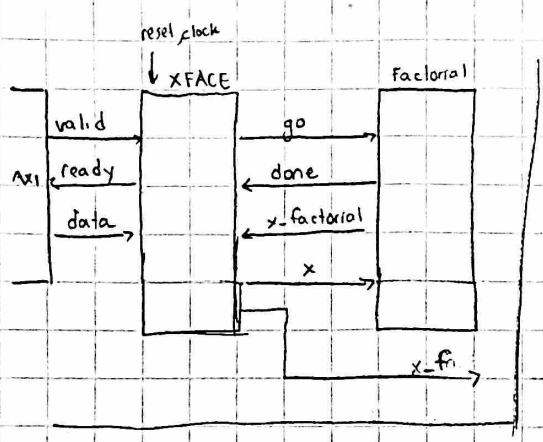
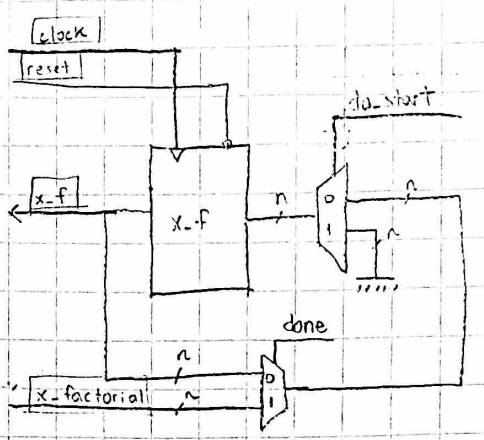
1) A

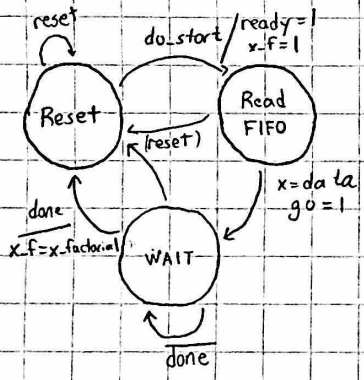
XFACE: inputs: Master_valid, done, x_factorial[n], fifo data_in

outputs: slave_ready, go




B




The do_start signal is just a control signal of:

assign do_start = valid & (state == reset_state);

used to prevent clearing x_f when valid goes high on the AXI interface. this module operates by initiating a read from the AXI stream FIFO when all previous computations are done, and valid is asserted. There, the internal register for x_f is cleared, and the FIFO data is sent to the factorial module, along with a single go pulse, the next clock cycle. Then done is waited for, at which point the result is stored in the internal x_f registers until another valid or reset is asserted.