

ECE 440 - Project #7

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1 Project Results

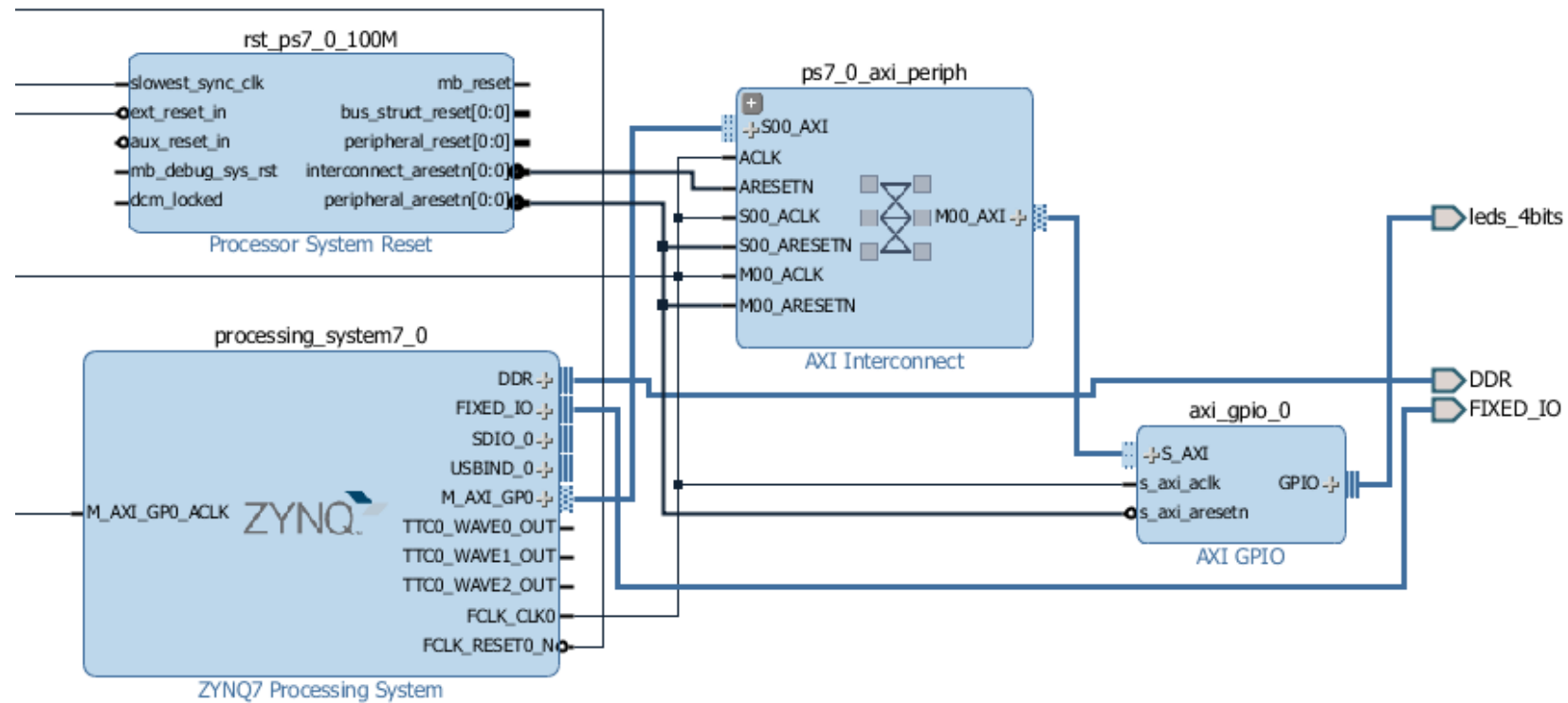


Figure 1.1: Block Diagram of the Vivado Processing Window – wires connect on the left (not shown).

ZC702_hw_platform Hardware Platform Specification

Design Information

Target FPGA Device: 7z010
 Part: xc7z010clg400-1
 Created With: Vivado 2016.4
 Created On: Wed Mar 11 11:35:07 2020

Address Map for processor ps7_cortexa9_0-1]

Cell	Base Addr	High Addr	Slave I/f	Mem/Reg
ps7_intc_dist_0	0xf8f01000	0xf8f01fff		REGISTER
ps7_gpio_0	0xe000a000	0xe000afff		REGISTER
ps7_scutimer_0	0xf8f00600	0xf8f0061f		REGISTER
ps7_slcr_0	0xf8000000	0xf8000fff		REGISTER
axi_gpio_0	0x41200000	0x4120ffff	S_AXI	REGISTER
ps7_scuwdt_0	0xf8f00620	0xf8f006ff		REGISTER
ps7_l2cachec_0	0xf8f02000	0xf8f02fff		REGISTER
ps7_scuc_0	0xf8f00000	0xf8f000fc		REGISTER
ps7_qspi_linear_0	0xfc000000	0xfcffffff		MEMORY
ps7_pmu_0	0xf8893000	0xf8893fff		REGISTER
ps7_afi_1	0xf8009000	0xf8009fff		REGISTER
ps7_afi_0	0xf8008000	0xf8008fff		REGISTER
ps7_qspi_0	0xe000d000	0xe000dfff		REGISTER
ps7_usb_0	0xe0002000	0xe0002fff		REGISTER
ps7_afi_3	0xf800b000	0xf800bfff		REGISTER
ps7_afi_2	0xf800a000	0xf800afff		REGISTER
ps7_globaltimer_0	0xf8f00200	0xf8f002ff		REGISTER
ps7_dma_s	0xf8003000	0xf8003fff		REGISTER
ps7_iop_bus_config_0	0xe0200000	0xe0200fff		REGISTER
ps7_xadc_0	0xf8007100	0xf8007120		REGISTER
ps7_dds_0	0x00100000	0x1fffffff		MEMORY
ps7_ddrc_0	0xf8006000	0xf8006fff		REGISTER
ps7_ocmc_0	0xf800c000	0xf800cfff		REGISTER
ps7_pl310_0	0xf8f02000	0xf8f02fff		REGISTER
ps7_uart_1	0xe0001000	0xe0001fff		REGISTER
ps7_coresight_comp_0	0xf8800000	0xf88fffff		REGISTER
ps7_ttc_0	0xf8001000	0xf8001fff		REGISTER
ps7_scugic_0	0xf8f00100	0xf8f001ff		REGISTER
ps7_ethernet_0	0xe000b000	0xe000bfff		REGISTER
ps7_dev_cfg_0	0xf8007000	0xf80070ff		REGISTER
ps7_dma_ns	0xf8004000	0xf8004fff		REGISTER
ps7_scd_0	0xe0100000	0xe0100fff		REGISTER

Figure 1.2: Top portion of the HDF file.

LED_test_bsp Board Support Package

[Modify this BSP's Settings](#)[Re-generate BSP Sources](#)

Target Information

This Board Support Package is compiled to run on the following target.

Hardware Specification: U:\ECE440_P7\first_zynq_design\first_zynq_design.sdk\ZC

Target Processor: ps7_cortexa9_0

Operating System

Board Support Package OS.

Name: standalone

Version: 6.1

Description: Standalone is a simple, low-level software layer. It provides access to input and output, profiling, abort and exit.

Documentation: [standalone v6.1](#)

Peripheral Drivers

Drivers present in the Board Support Package.

axi_gpio_0	gpio	Documentation	Import Examples
ps7_afi_0	generic	Documentation	
ps7_afi_1	generic	Documentation	
ps7_afi_2	generic	Documentation	
ps7_afi_3	generic	Documentation	
ps7_coresight_comp_0	coresightps_dcc	Documentation	
ps7_ddr_0	ddrps	Documentation	
ps7_ddrc_0	generic	Documentation	
ps7_dev_cfg_0	devcfg	Documentation	Import Examples
ps7_dma_ns	dmapi	Documentation	Import Examples
ps7_dma_s	dmapi	Documentation	Import Examples
ps7_ethernet_0	emacps	Documentation	Import Examples
ps7_globaltimer_0	generic	Documentation	
ps7_gpio_0	gpiops	Documentation	Import Examples
ps7_gpv_0	generic	Documentation	
ps7_intc_dist_0	generic	Documentation	
ps7_iop_bus_config_0	generic	Documentation	
ps7_l2cachec_0	generic	Documentation	
ps7_ocmc_0	generic	Documentation	
ps7_pl310_0	generic	Documentation	
ps7_pmu_0	generic	Documentation	
ps7_qspi_0	qspi	Documentation	Import Examples

Figure 1.3: Top portion of the MSS file.



```
11:47:07 INFO : Registering command handlers for SDK TCF services
11:47:08 INFO : Launching XSCT server: xsct.bat -interactive U:/ECE440_P7/first_zynq_design/first_zynq_design.sdk/temp_xsdb_launch_script.tcl
11:47:12 INFO : XSCT server has started successfully.
11:47:12 INFO : Successfully done setting XSCT server connection channel
11:47:17 INFO : Successfully done setting SDK workspace
12:00:46 INFO : SDK has detected change in the last modified timestamps for source hardware specification file Source:1583952217637, Project:148522
12:00:46 INFO : Copied contents of U:/ECE440_P7/first_zynq_design/first_zynq_design.sdk/first_zynq_system_wrapper.hdf into \ZC702_hw_platform\system
12:00:50 INFO : Synchronizing projects in the workspace with the hardware platform specification changes.
12:01:05 INFO :
12:01:06 INFO : Updating hardware inferred compiler options for LED_test.
12:01:06 INFO : Clearing existing target manager status.
12:01:08 INFO : Closing and re-opening the MSS file of ther project LED_test_bsp
12:01:09 INFO : Workspace synchronized with the new hardware specification file. Cleaning dependent projects...
12:01:11 WARN : Linker script will not be updated automatically. Users need to update it manually.
12:01:59 INFO : Connected to target on host '127.0.0.1' and port '3121'.
12:02:01 INFO : 'targets -set -filter {jtag_cable_name =~ "Digilent Zybo 210279A430C8A" && level==0} -index 1' command is executed.
12:02:02 INFO : FPGA configured successfully with bitstream "U:/ECE440_P7/first_zynq_design/first_zynq_design.sdk/ZC702_hw_platform/first_zynq_syste
12:06:10 INFO : 'targets -set -filter {jtag_cable_name =~ "Digilent Zybo 210279A430C8A" && level==0} -index 1' command is executed.
12:06:10 INFO : 'fpga -state' command is executed.
12:06:10 INFO : Connected to target on host '127.0.0.1' and port '3121'.
12:06:11 INFO : Jtag cable 'Digilent Zybo 210279A430C8A' is selected.
12:06:11 INFO : 'jtag frequency' command is executed.
12:06:11 INFO : Sourcing of 'U:/ECE440_P7/first_zynq_design/first_zynq_design.sdk/ZC702_hw_platform/ps7_init.tcl' is done.
12:06:11 INFO : Context for 'APU' is selected.
12:06:11 INFO : Hardware design information is loaded from 'U:/ECE440_P7/first_zynq_design/first_zynq_design.sdk/ZC702_hw_platform/system.hdf'.
12:06:11 INFO : Context for 'APU' is selected.
12:06:11 INFO : 'stop' command is executed.
12:06:11 INFO : 'ps7_init' command is executed.
12:06:11 INFO : 'ps7_post_config' command is executed.
12:06:11 INFO : Context for processor 'ps7_cortexa9_0' is selected.
12:06:11 INFO : Processor reset is completed for 'ps7_cortexa9_0'.
12:06:11 INFO : Context for processor 'ps7_cortexa9_0' is selected.
12:06:12 INFO : The application 'U:/ECE440_P7/first_zynq_design/first_zynq_design.sdk/LED_test/Debug/LED_test.elf' is downloaded to processor 'ps7_c
12:06:12 INFO : -----XSDB Script-----
connect -url tcp:127.0.0.1:3121
source U:/ECE440_P7/first_zynq_design/first_zynq_design.sdk/ZC702_hw_platform/ps7_init.tcl
targets -set -nocase -filter {name =~ "APU*" && jtag_cable_name =~ "Digilent Zybo 210279A430C8A"} -index 0
loadhw U:/ECE440_P7/first_zynq_design/first_zynq_design.sdk/ZC702_hw_platform/system.hdf
targets -set -nocase -filter {name =~ "APU*" && jtag_cable_name =~ "Digilent Zybo 210279A430C8A"} -index 0
stop
ps7_init
ps7_post_config
targets -set -nocase -filter {name =~ "ARM*#0" && jtag_cable_name =~ "Digilent Zybo 210279A430C8A"} -index 0
rst -processor
targets -set -nocase -filter {name =~ "ARM*#0" && jtag_cable_name =~ "Digilent Zybo 210279A430C8A"} -index 0
dow U:/ECE440_P7/first_zynq_design/first_zynq_design.sdk/LED_test/Debug/LED_test.elf
-----End of Script-----
```

Figure 1.4: The first part of the SDK log window.

```
dow U:/ECE440_P7/first_zynq_design/first_zynq_design.sdk/LED_test/Debug/LED_test.elf
-----End of Script-----

12:06:12 INFO    : Memory regions updated for context APU
12:06:12 INFO    : Context for processor 'ps7_cortexa9_0' is selected.
12:06:12 INFO    : 'con' command is executed.
12:06:12 INFO    : -----XSDB Script (After Launch)-----
targets -set -nocase -filter {name =~ "ARM*#0" && jtag_cable_name =~ "Digilent Zybo 210279A430C8A"} -index 0
con
-----End of Script-----

12:06:12 INFO    : Launch script is exported to file 'U:/ECE440_P7/first_zynq_design/first_zynq_design.sdk/.sdk/launch_scripts/xilinx_c-c++_application
```

Figure 1.5: The second part of the SDK log window.