ECE 440 - Homework #7

Collin Heist

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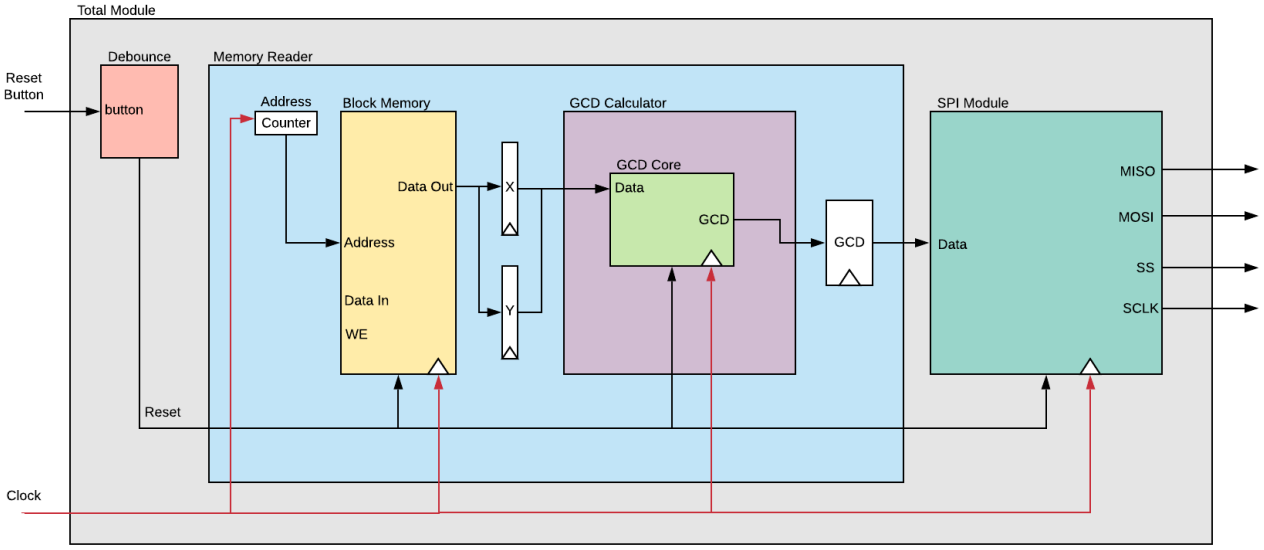

Figure 1: Block Diagram of my approach to Project #5.

For simplicity, I did not show all connections to registers, nor the modules within the GCD core. Also, *WE* and *Data In* are not shown to be connected, but they are internally unused (grounded) as no writing to the block memory is utilized.

My approach to the project will be to create a memory reader module that interacts with the block memory unit, reading the pairs of data one at a time (one pair at a time), and then interacting with the GCD module through a GCD wrapper of sorts. This wrapper will take the X and Y data and interact with the GCD with the required timing, sending the final GCD result back to the memory reader module. Once this has been done for the current pair, the GCD data will be sent to an SPI module that implements the SPI protocol that serves as an output for the total module. This will be repeated for each pair of data read in the block memory, until the memory reader identifies a zero.

The SPI module will utilize a parameterized *down-clocking* of sorts, where a specified count x can be given, and each x clock pulses, the SPI FSM will increment - allowing for easily configured timing of SCLK, without the need for dummy states within the FSM.

Of course, when implemented on hardware, this will utilize the debounce module to reset all modules and registers within the circuit.