SmallPond Reference sheet

Instruction Set

NAME	MNEMONIC	OP	$INST_{hex}$

A type

Add	*ADD*	RD = RS1 + RS2	0x01
And	*AND*	RD = RS1 & RS2	0x02
Airth Shift R	*ASR*	RD = RS1 >> RS2	0x03
Logical Shift L	*LSL*	RD = RS1 << RS2	0x04
Logical Shift R	*LSR*	RD = RS1 >> RS2	0x05
Not And	*NAND*	RD = ~(RS1 & RS2)	0x06
Not Or	*NOR*	RD = ~(RS1 | RS2)	0x07
Not	*NOT*	RD = ~ RS	0x08
Or	*OR*	RD = RS1 | RS2	0x09
Subtraction	*SUB*	RD = RS1 - RS2	0x0A
X Not Or	*XNOR*	RD = RS1 ⊙ RS2	0x0B
X Or	*XOR*	RD = RS1 ⊕ RS2	0x0C

I type

Addition w/ Imm	*ADDI*	RD = RS + #Imm	0x18
And w/ Imm	*ANDI*	RD = RS & #Imm	0x19
Airth Shift R Imm	*ASRI*	RD = RS << #Imm	0x1A
Load Word	*LDR*	RD = [RS + #Imm]	0x1B
Load Byte	*LDRB*	$RD_{7:0}$ = [RS + #Imm]	0x1C
Load B Unsigned	*LDRBU*	$RD_{7:0}$ = [RS + #UImm]	0x1D
Load Halfword	*LDRH*	$RD_{15:0}$ = [RS + #Imm]	0x1E
Load Halfword Unsigned	*LDRHU*	$RD_{15:0}$ = [RS + #UImm]	0x1F
Logical Shift L Imm	*LSLI*	RD = RS >> #Imm	0x20
Logical Shift R Imm	*LSRI*	RD = RS << #Imm	0x21
Load Upper Imm	*LUI*	$RD_{31:16}$ = [RS + #Imm]	0x22
Not And Imm	*NANDI*	RD = ~(RS & #Imm)	0x23
Not Or Imm	*NORI*	RD = ~(RS | #Imm)	0x24
Or Imm	*ORI*	RD = RS | #Imm	0x25
Store Word	*STR*	[RD] = RS + #Imm	0x26
Store Byte	*STRB*	[RD] = $(RS + \#Imm)_{7:0}$	0x27
Store Halfword	*STRH*	[RD] = $(RS + \#Imm)_{15:0}$	0x28
Subtract Imm	*SUBI*	RD = RS - #Imm	0x29
X Not Or Imm	*XNORI*	RD = RS ⊙ #Imm	0x2A
X Or Imm	*XORI*	RD = RS1 ⊕ #Imm	0x2B

J type

Jump	J	PC = PC + #Imm	0x3F

B type

Branch	*B*	PC = PC + #Imm	0x3C
Branch and Link	*BL*	PC = PC + #Imm	0x3D
Branch and Return	*BR*	PC = PC + #Imm	0x3E

INSTRUCTION FORMAT

A type:

Inst.	**RD**	**RS1**	**RS2**	**S**	**C**	**Unused**	**Cond**
31:26	25:21	20:16	15:11	10	9	8:4	3:0

I type:

Inst.	**RD**	**RS1**	**Immediate**
31:26	25:21	20:16	15:0

J type:

Inst.	**Immediate**
31:26	25:0

B type:

Inst.	**C**	**Unused**	**Immediate**	**Cond.**
31:26	25	24:22	21:4	3:0

REGISTER NAME, NUMBER, USE

NAME	NUMB	USE
Zero	0	The constant value 0
Arg_#(0-3)	1 - 4	Argument
Tmp_#(0-7)	5 - 12	Temporary use registers
Svd_#(0-5)	13 - 18	Saved temporaries
Pos/Neg	19	Pair of 2's comp registers. Value is reflected across regs.
Neg/Pos	20	
+ Counter	21	Pair of reflected count registers.
- Counter	22	
HP	23	Heap pointer
FP	24	Frame pointer
LR_#(0-3)	25 – 29	Link registers used for routine addresses
PC	30	Program counter
CPSR	31	Current program status register

DATA ALIGNMENT

WORD			
HALFWORD		HALFWORD	
BYTE	BYTE	BYTE	BYTE
31 25	24 17	16 8	7 0