Katana – Measurements

Jean-Paul CHAPUT

24 novembre 2021

The Test Bench

Those test benchs have been run with :
— CORIOLIS git commit `ca499e024c20b50ea48a8e21f30225b60efb4527`.
— `alliance-check-toolkit` git commit `afb3d074279f8dd417a4d7c63f9fad481bba4014`.
All the designs have been placed with the «golden industrial router».

There is a bug in the power build, it's runtime is exponential whithout reason. So for the purpose of the test, I did disable the power build in `metal1`.

Be aware that the all the curves uses logarithmic scale on both axis.

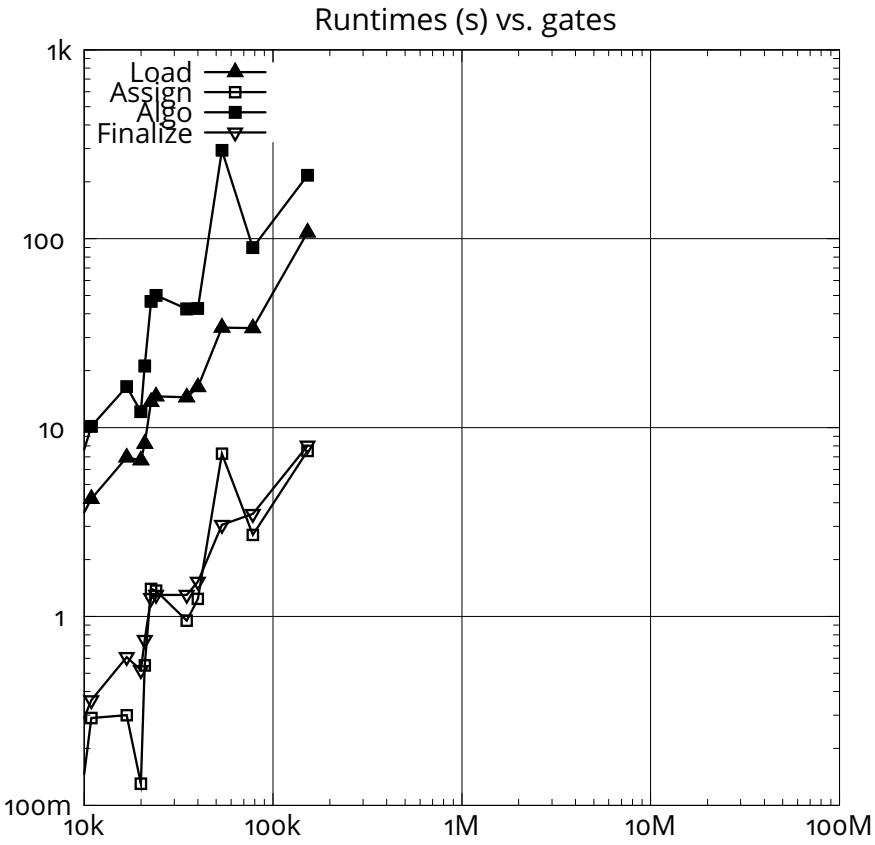
The figures shows that :

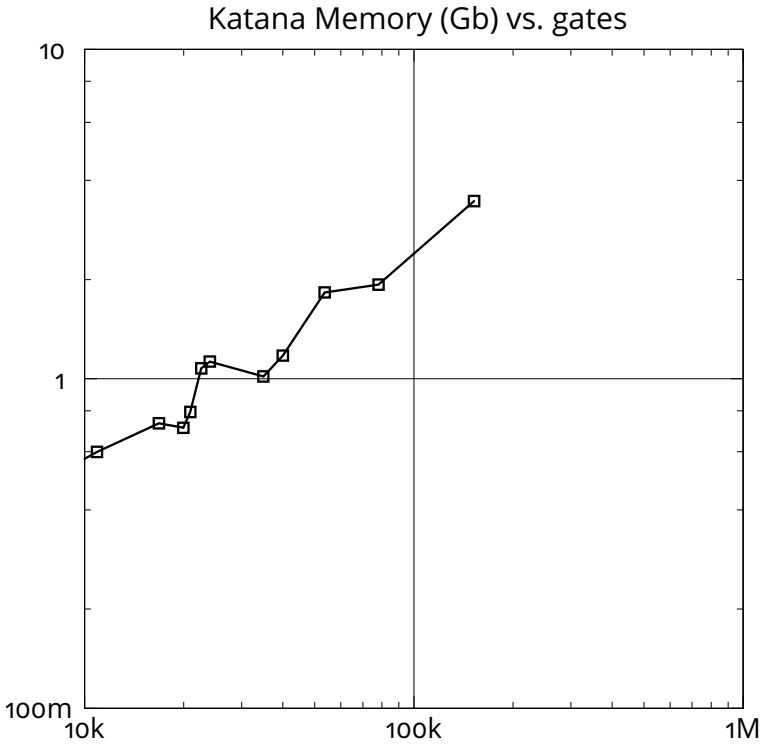
1. The runtime is quasi-linear.
2. The memory footprint is getting better as the design size increase...

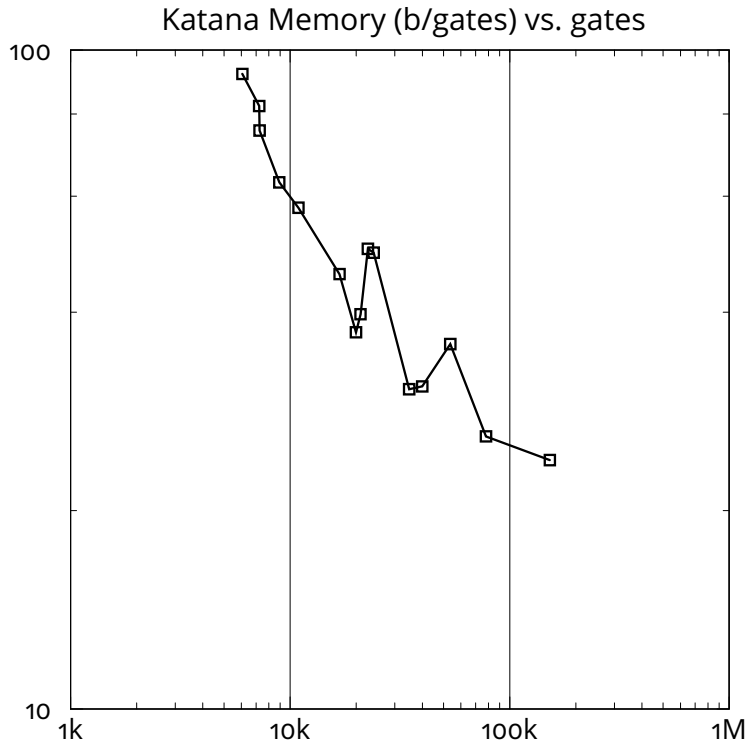
design	#gates	LoadT (s)	LoadS (Mb)	AssignT (s)	AlgoT (s)	AlgoS (Mb)	FinT (s)	#segments	#events
SoC benchmark									
operator_lvl3	6065.00	2.71	489	0.20	7.19	545	0.19	44246	123736
operator_lvl2	7221.00	3.31	509	0.23	9.58	580	0.28	54543	156869
operator_lvl1	7256.00	2.61	489	0.10	5.30	535	0.21	41468	86832
operator_lvl0	8926.00	2.86	500	0.06	5.29	549	0.22	45307	88261
matrix_4_4	10909.00	4.20	531	0.29	10.16	614	0.36	69680	161390
dct_lvl1	16803.00	6.95	626	0.30	16.46	750	0.61	106011	258152
dct_lvl0	19958.00	6.71	621	0.13	12.13	727	0.52	97739	190554
matrix_4_8	20933.00	8.21	653	0.55	21.17	812	0.75	133852	312033
dct_lvl3	22603.00	13.66	819	1.40	46.55	1102	1.25	209892	683126
dct_lvl2	24011.00	14.63	851	1.37	50.16	1155	1.30	225257	736835
ieee_division	34870.00	14.47	814	0.95	42.50	1041	1.30	200840	443572
matrix_8_8	39973.00	16.37	898	1.24	42.76	1205	1.53	256077	603617
vld	53614.00	33.86	1204	7.27	294.07	1874	3.05	432612	1693758
matrix_8_16	78101.00	33.63	1374	2.70	89.58	1977	3.49	501136	1183305
matrix_16_16	152341.00	108.01	2398	7.52	216.86	3549	8.03	978567	2334437

design	#gates	#gcells	#globals	#segments	Detailed WL	#events	#unique events
SoC benchmark							
operator_lvl3	6065	5328	18790	44246	2358982+0	123736	44246
operator_lvl2	7221	6399	23252	54543	2905308+57	156869	54543
operator_lvl1	7256	5402	17933	41468	1996269+0	86832	41468
operator_lvl0	8926	6160	19480	45307	2113569+0	88261	45307
matrix_4_4	10909	7656	30904	69680	3603849+0	161390	69680
dct_lvl1	16803	12768	44847	106011	5027615+0	258152	106011
dct_lvl0	19958	12995	41011	97739	4367356+57	190554	97739
matrix_4_8	20933	14696	59544	133852	7017462+0	312033	133852
dct_lvl3	22603	22648	86257	209892	11387979+57	683126	209892
dct_lvl2	24011	24335	93617	225257	12132523+47	736835	225257
ieee_division	34870	21608	84333	200840	9757088+27	443572	200840
matrix_8_8	39973	28056	113961	256077	13555832+0	603617	256077
vld	53614	53130	181215	432612	36198106+4265	1693758	432612
matrix_8_16	78101	54936	223208	501136	26681520+0	1183305	501136
matrix_16_16	152341	107256	435976	978567	52378464+0	2334437	978567

Times & Speeds






Katana Memory (b/gates) vs. gates
100
10
1k
10k
100k
1M