

ALLIANCE & CORIOLIS Checker Toolkit

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Toolkit Purpose

This toolkit has been created to allow developpers to share through `git` a set of benchmarks to validate their changes in ALLIANCE & CORIOLIS before committing and pushing them in their central repositories. A change will be considered as validated when all the developpers can run successfully all the benches in their respective environments.

As a consequence, this repository is likely to be *very* unstable and the commits not well documented as they will be quick corrections made by the developpers.

Toolkit Contents

The toolkit provides:

- Three benchmark designs:

Design	Technology	Cell Libraries
adder	MOSIS	msxlib, mpxlib, msplib
AM2901	ALLIANCE dummy	sxlib, pxlib
SNX	MOSIS	msxlib, mpxlib, msplib

- Three cell libraries.

All thoses libraries are for use with the MOSIS technology. We provides them as part of the toolkit as we are still in the process of validating that technology, and we may have to perform quick fixes on them. The design are configured to use them instead of those supplied by the ALLIANCE installation.

- `msxlib` : Standard Cell library.
- `mpxlib` : Pad library, compliant with CORIOLIS.
- `msplib` : Pad library, compliant with ALLIANCE / `ring`. Cells in this library are *wrappers* around their counterpart in `mpxlib`, they provides an outer layout shell that is usable by `ring`.
- The RDS file for the MOSIS technology `scn6m_deep_09.rds`, for the same reason as the cell libraries.
- Miscellenous helper scripts.

Benchmark Makefiles

The main body of the Makefile has been put into `benchs/etc/rules.mk`.

It provides the following targets:

ALLIANCE	core.ap	The placement of the design's core
	\$(CHIP)_alc.ap	The complete layout of the design (P&R).
	druc	Symbolic layout checking
	lvx	Perform LVS.
	graal	Launch graal in the Makefile's environnement
	dreal	Launch dreal in the Makefile's environnement, and load the gds file of the design.
CORIOLIS	\$(CHIP)_crl.ap	The complete layout of the design (P&R).
	druc-crl	Symbolic layout checking
	lvx-crl	Perform LVS.
	cgt-interactive	Launch cgt and prep it to perform P&R
	cgt	Launch cgt in the Makefile's environnement

A top Makefile in a bench directory must define at least the following variables:

```

CORE = adder
CHIP = chip
MARGIN = 2
GENERATE_CORE_VST = Yes
USE_MOSIS = Yes

include ../etc/rules.mk

export      MBK_IN_LO = vst
export      MBK_OUT_LO = vst
export      RDS_IN = gds
export      RDS_OUT = gds

```

Where variables have the following meaning:

Variable	Usage
CORE	The name of the <i>core</i> model
CHIP	The stem of the <i>chip</i> model. It is declined in two versions, one for ALLIANCE (suffix <i>_alc</i>) and one for CORIOLIS (suffix <i>_crl</i>). This is needed because the two core uses different sets of pads.
GENERATE_CORE_VST	Tells if the rules to generate the core has to be included. If set to No, then the core <i>must</i> be present and will be considered as a primary file.
USE_MOSIS	Tells whether or not use the MOSIS technology.

CORIOLIS Configuration Files

Unlike ALLIANCE which is entirely configured through environnement variables or system-wide configuration file, CORIOLIS uses configuration files in the current directory. They are present for each bench:

- `<cwd>/coriolis techno.conf` : Select which symbolic and real technology to use.
- `<cwd>/coriolis.conf` : Override for any system configuration, except for the technology.

COROLIS and Clock Tree Generation

When COROLIS is used, it create a clock tree which modificate the original netlist. The new netlist, with a clock tree, has a postfix of `_clocked`.

**Note**

Trans-hierarchical Clock-Tree. As COROLIS do not flatten the designs it creates, not only the top-level netlist is modiflicated. All the sub-blocks connected to the master clock are also duplicateds, whith the relevant part of the clock-tree included.

RHEL6 and Clones

Under RHEL6 the developpement version of COROLIS needs the `devtoolset-2`. `rules.mk` tries, based on `uname` to switch it on or off.