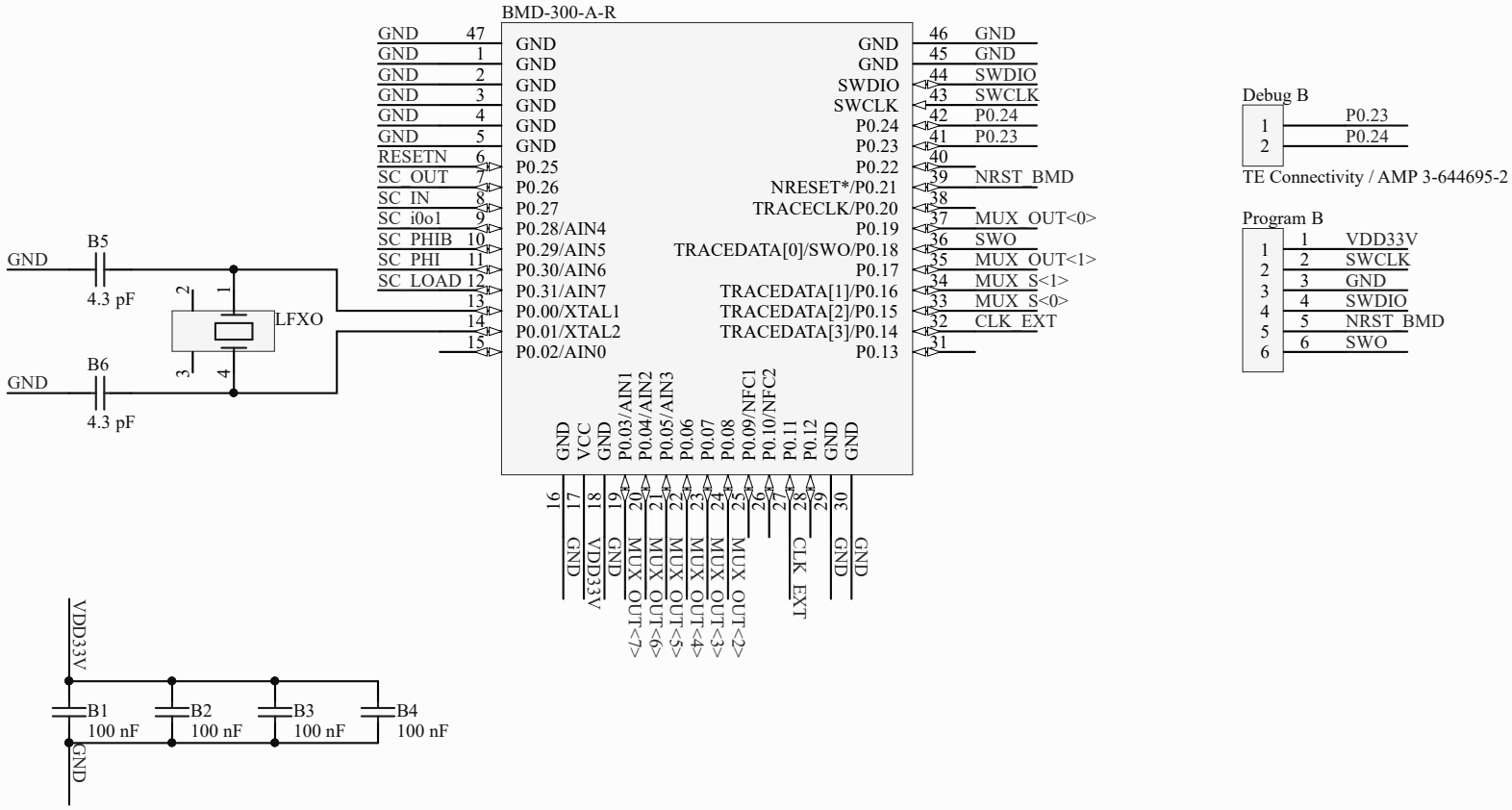
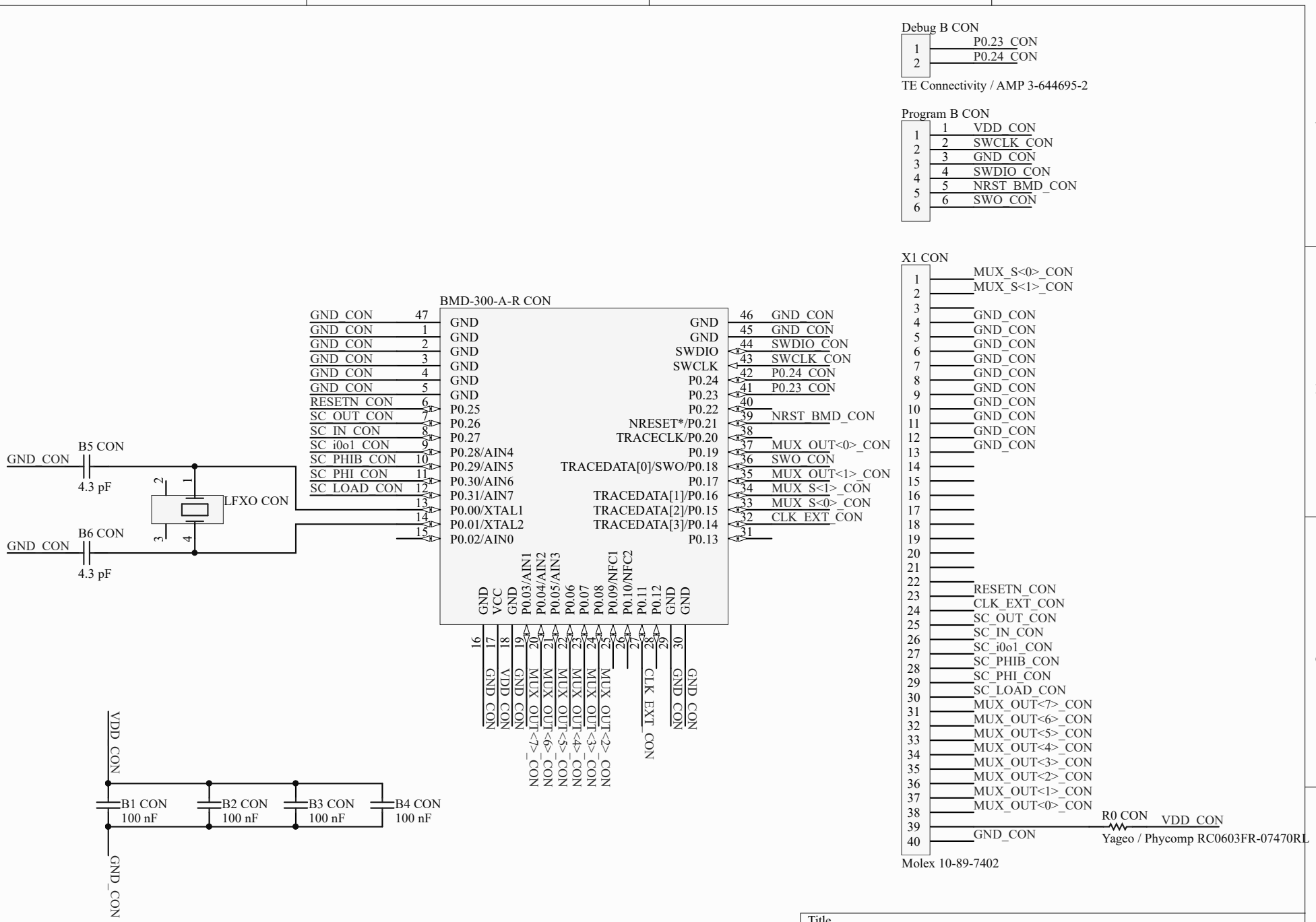
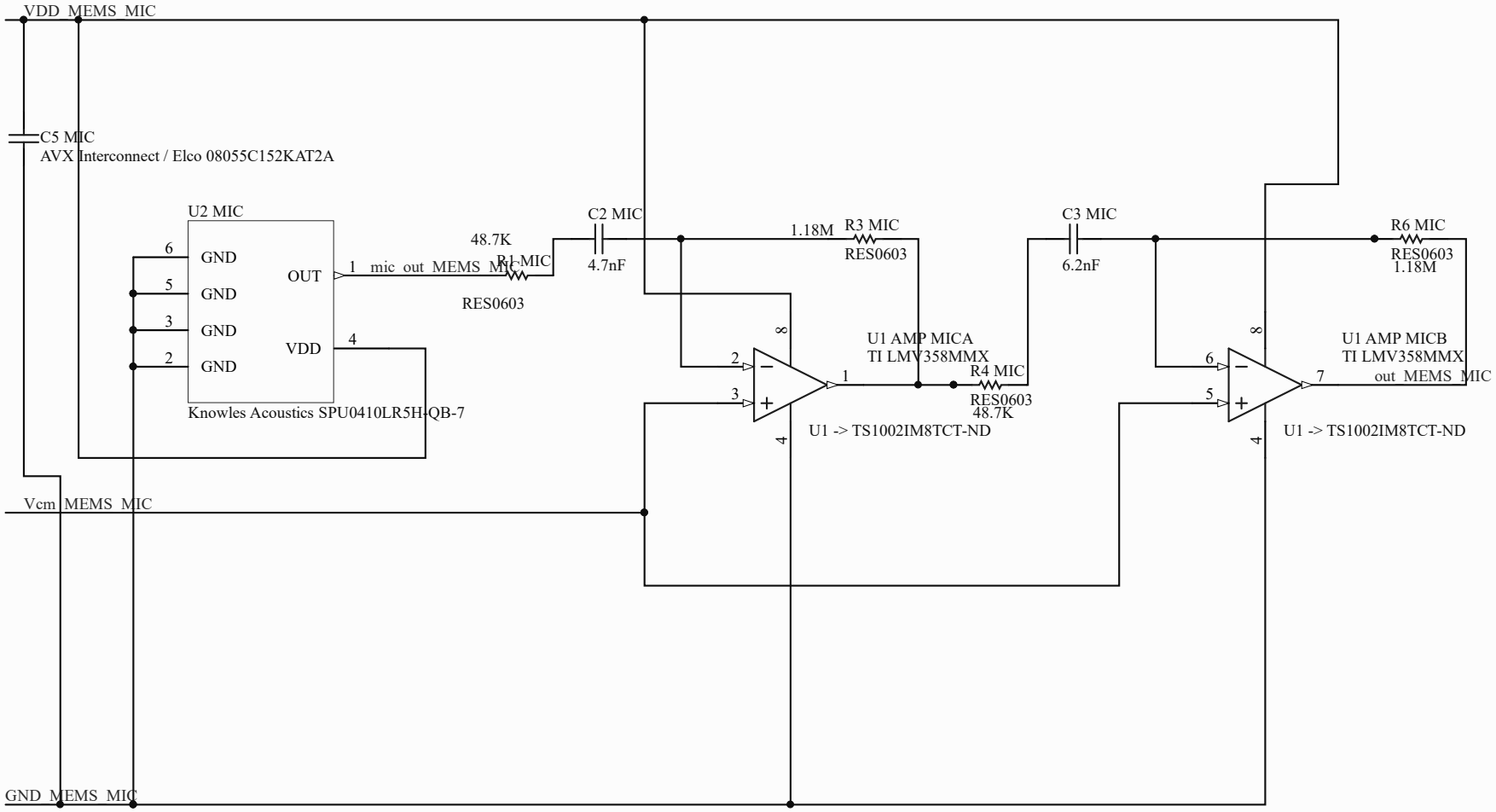
Board S

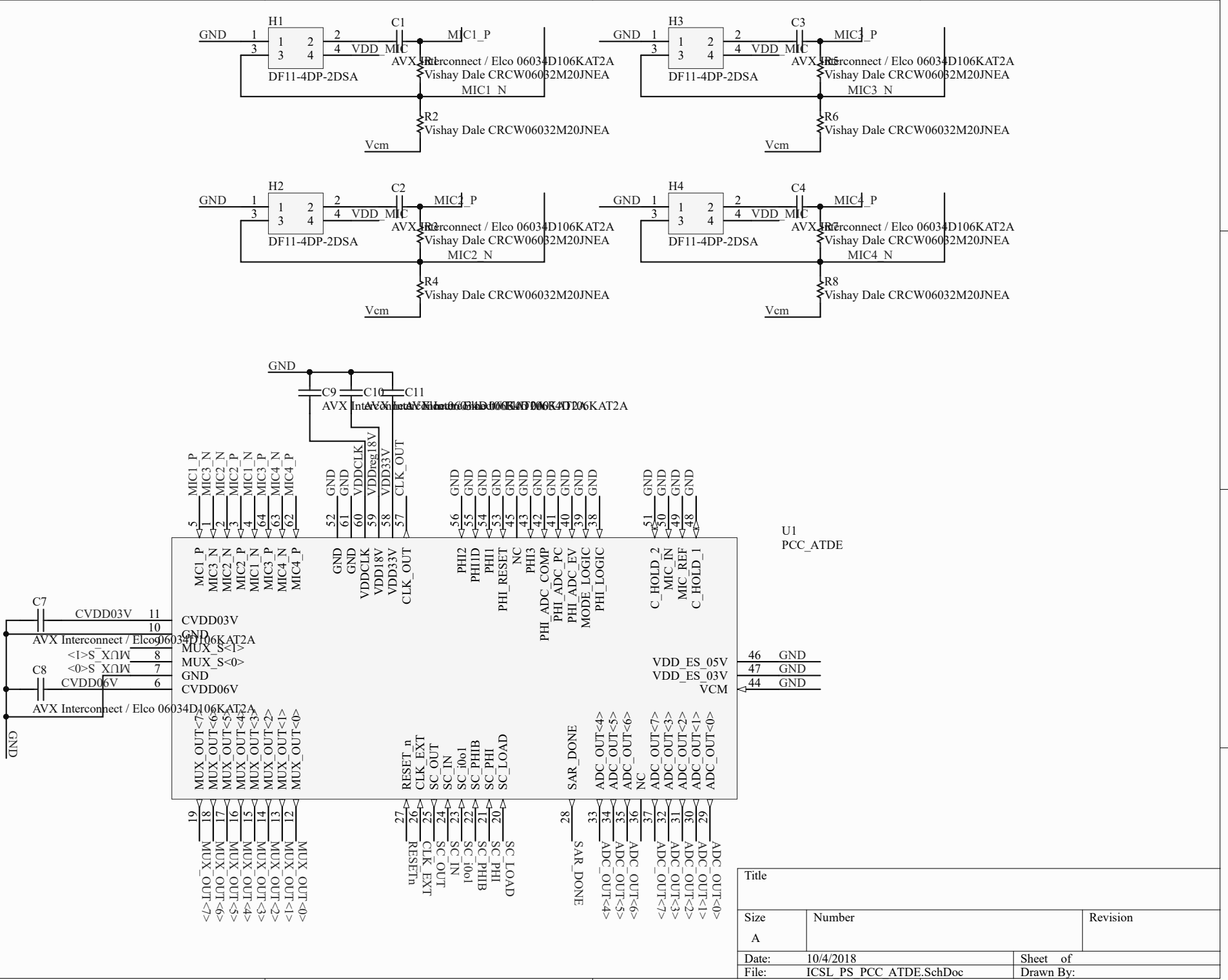


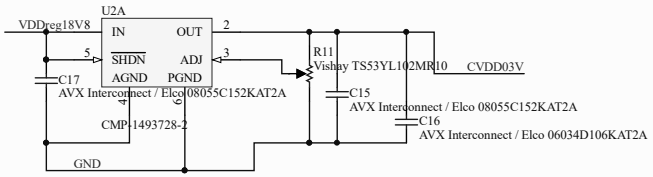
Title		
Size A	Number	Revision
Date: 10/4/2018		Sheet of
File: ICSL_PS_BMD.SchDoc		Drawn By:

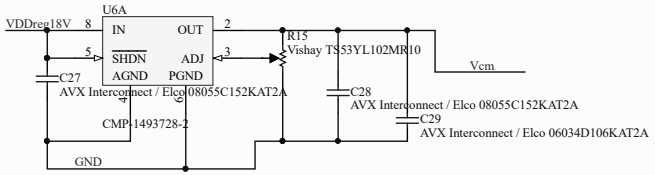

Debug B CON
P0.23_CON
P0.24_CON
TE Connectivity / AMP 3-644695-2
Program B CON
VDD_CON
SWCLK_CON
GND_CON
SWDIO_CON
NRST_BMD_CON
SWO_CON
X1 CON
MUX_S<0>_CON
MUX_S<1>_CON
RESETN_CON
CLK_EXT_CON
SC_OUT_CON
SC_IN_CON
SC_i0o1_CON
SC_PHIB_CON
SC_PHI_CON
SC_LOAD_CON
MUX_OUT<7>_CON
MUX_OUT<6>_CON
MUX_OUT<5>_CON
MUX_OUT<4>_CON
MUX_OUT<3>_CON
MUX_OUT<2>_CON
MUX_OUT<1>_CON
MUX_OUT<0>_CON
R0 CON
Yageo / Phycomp RC0603FR-07470RL
Molex 10-89-7402
BMD-300-A-R CON
B5 CON
B6 CON
4.3 pF
LFXO CON
B1 CON
B2 CON
B3 CON
B4 CON
100 nF
Title
Size
A
Number
Revision
Date: 10/4/2018
File: ICSL_PS_CON.SchDoc
Sheet of
Drawn By:

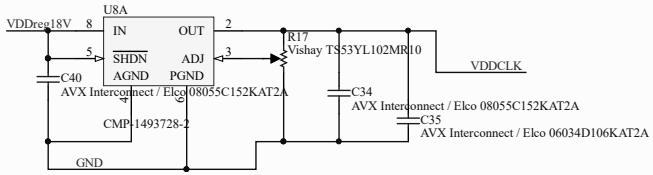


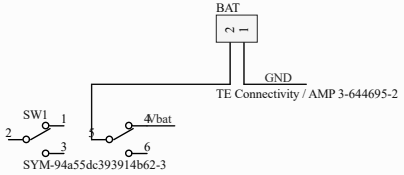
Title		
Size: A	Number	Revision
Date: 10/4/2018		Sheet of
File: ICSL_PS_MEMS_MIC_V1.SchDoc		Drawn By:

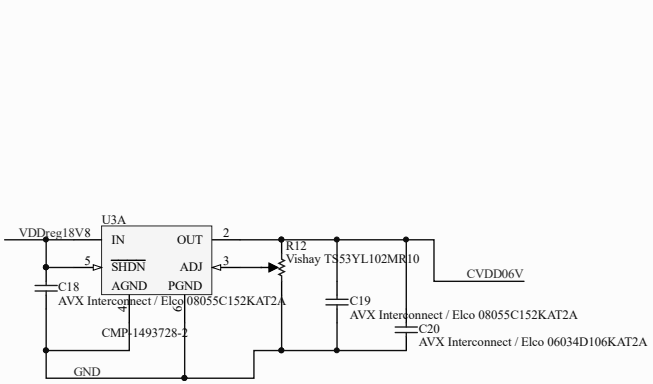

H1
C1
GND
MIC1_P
VDD_MIC
AVX Interconnect / Elco 06034D106KAT2A
Vishay Dale CRCW06032M20JNEA
DF11-4DP-2DSA
MIC1_N
R2
Vcm
H3
C3
MIC3_P
MIC3_N
R6
H2
C2
MIC2_P
MIC2_N
R4
H4
C4
MIC4_P
MIC4_N
R8
C9
C10
C11
MIC1_P
MIC3_N
MIC2_P
MIC2_N
MIC1_N
MIC3_P
MIC4_N
MIC4_P
VDDCLK
VDDreg18V
VDD33V
CLK_OUT
PHI2
PHI1D
PHI1
PHI_RESET
NC
PHI3
PHI_ADC_COMP
PHI_ADC_PC
PHI_ADC_EV
MODE_LOGIC
PHI_LOGIC
C_HOLD_2
MIC_IN
MIC_REF
C_HOLD_1
U1
PCC_ATDE
C7
C8
CVDD03V
CVDD06V
MUX_S<1>
MUX_S<0>
VDD_ES_05V
VDD_ES_03V
VCM
MUX_OUT<7>
MUX_OUT<6>
MUX_OUT<5>
MUX_OUT<4>
MUX_OUT<3>
MUX_OUT<2>
MUX_OUT<1>
MUX_OUT<0>
RESET_n
CLK_EXT
SC_OUT
SC_IN
SC_i0o1
SC_PHIB
SC_PHI
SC_LOAD
SAR_DONE
ADC_OUT<4>
ADC_OUT<5>
ADC_OUT<6>
NC
ADC_OUT<7>
ADC_OUT<3>
ADC_OUT<2>
ADC_OUT<1>
ADC_OUT<0>
Title
Size
A
Number
Revision
Date:
10/4/2018
Sheet of
File:
ICSL_PS_PCC_ATDE.SchDoc
Drawn By:

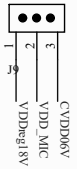


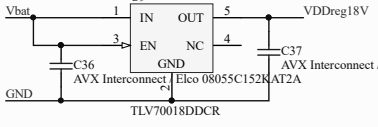


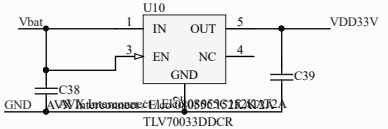




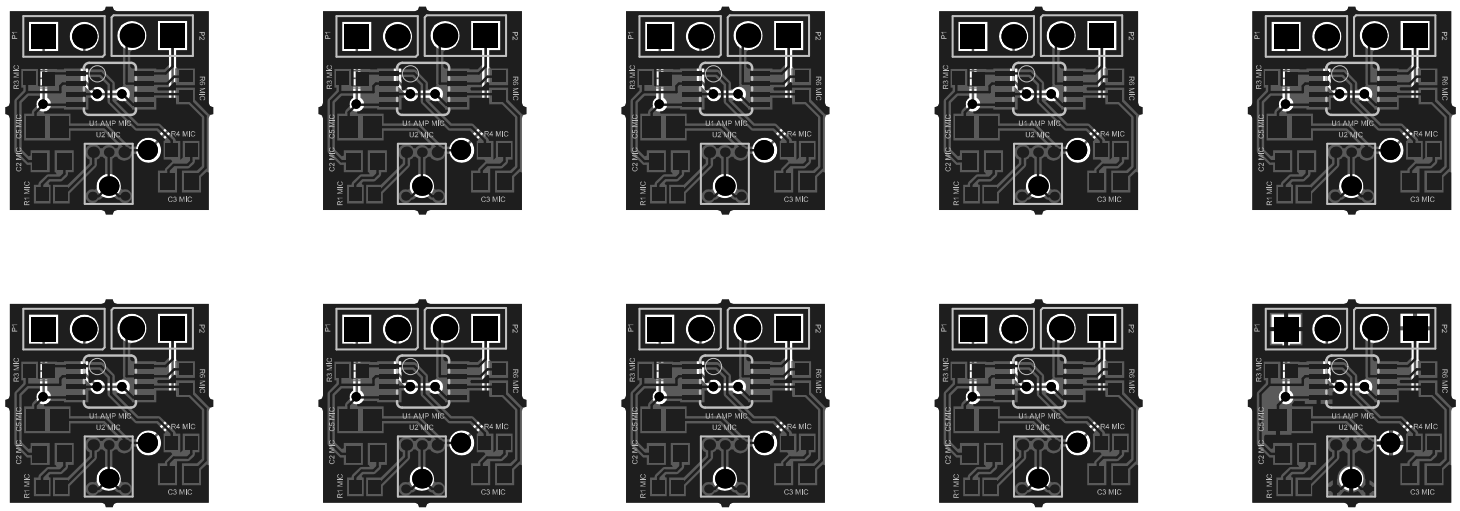


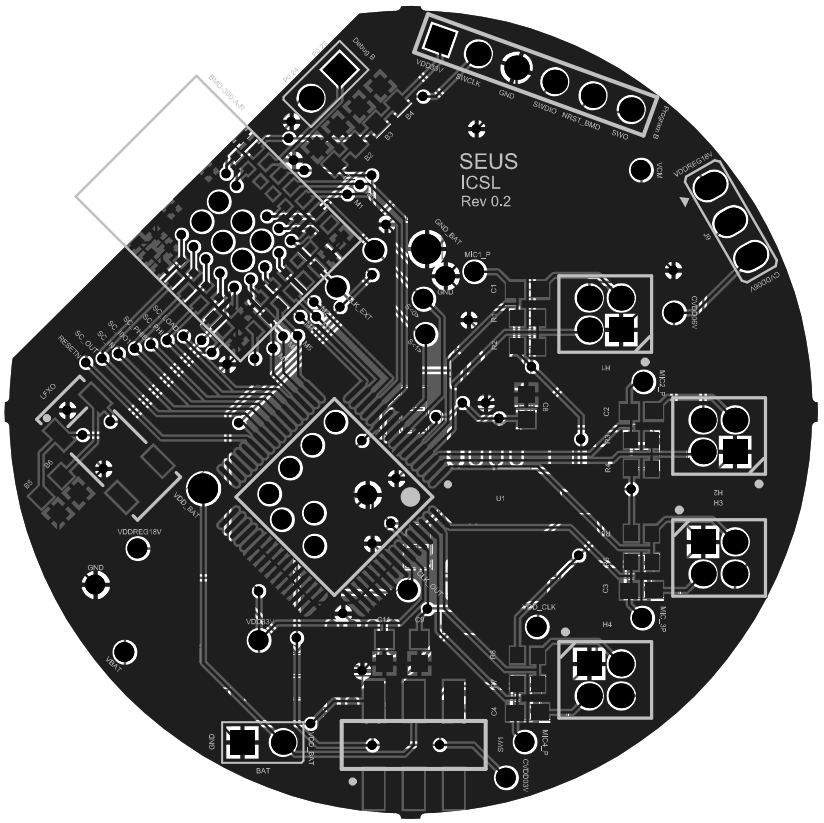


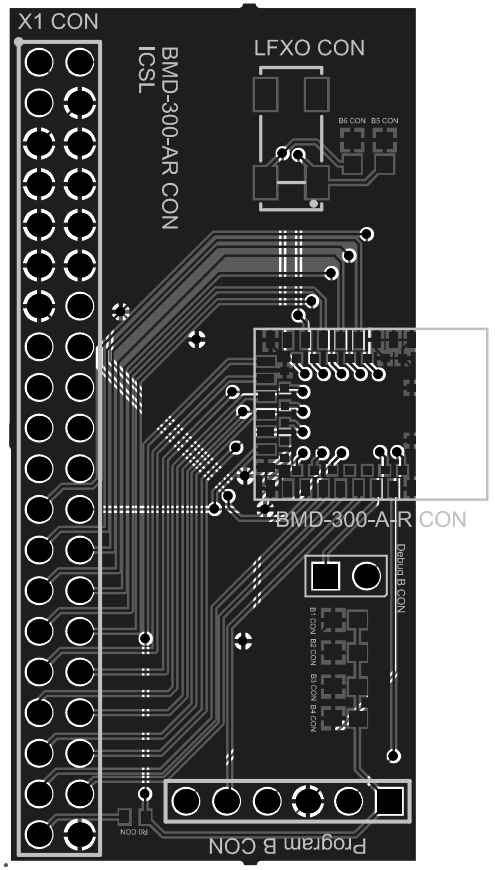




Title		
Size: A	Number	Revision
Date: 10/4/2018		Sheet of
File: ICSL_PS_POWER.SchDoc		Drawn By:




SEUS
ICSL
Rev 0.2


X1 CON
BMD-300-AR CON
ICSL
LFXO CON
BMD-300-A-R CON
Debug B CON
Program B CON

SEUS
ICSL
X1 CON
BMD-300-AR CON
ICSL
LFXO CON
BMD-300-A-R CON
Program B CON