BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY
DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING
CSE 306 JANUARY 2019 SEMESTER
COMPUTER ARCHITECTURE SESSIONAL

Assignment on 4-bit MIPS Design and Simulation

August 11, 2019

1 DESIGN SPECIFICATION

- There will be a multiplexed Address and Data bus with 8-bits width.
- Data will be of 4-bits while address will be of 8-bits.
- You must have to design the following temporary registers:

  $zero, $t0, $t1, $t2, $t3, $t4

  The assembly code that will be provided to simulate your design will use only these mentioned registers.
- The Control unit should be microprogrammed. The control signals associated with the operations should be stored in a special memory (you can use a separate ROM for this purpose) units as Control Words.
- During the simulation, as Assembly Code will be given and you have to convert it into your designed MIPS machine code. The conversion process should be automatic. For example, you can write code in your preferred programming language for this conversion.
- Marks will vary according to the efficiency of design.

2 Instruction Set Description

Instruction ID	Instruction Type	Instruction
A	Arithmetic	add
B	Arithmetic	addi
C	Arithmetic	sub
D	Arithmetic	subi
E	Logic	and
F	Logic	andi
G	Logic	or
H	Logic	ori
I	Logic	sll
J	Logic	srl
K	Logic	nor
L	Memory	sw
M	Memory	lw
N	Control	beq
O	Control	bneq
P	Control	j

3 MIPS Instruction Format

Our MIPS Instructions will be 20-bits long with the following three formats.

- R-type

Opcode	Src Reg 1	Src Reg 2	Dst Reg	Shft Amnt
4-bits	4-bits	4-bits	4-bits	4-bits

- I-type

Opcode	Src Reg 1	Src Reg 2	Address / Immediate
4-bits	4-bits	4-bits	8-bits

- J-type

Opcode	Target Jump Address	0	0
4-bits	8-bits	4-bits	4-bits

4 Memory Considerations

You need to consider three types of memory:

- Instruction Memory (accessed through program counter, pc)
- Data Memory (accessed through address)
- Stack Memory (accessed through stack pointer, sp Sample instruction: **sw $t0, 0($sp)** or **lw $t1, 4($sp)**)

5 Instruction Set Assignment

The opcodes of the instruction will be between 0 to 15 based on the sequence of instruction id given below. Sequence ABCDEFGHIJKLMNOP means add instruction's opcode will be 0, addi instruction's opcode will be 1, sub instruction's opcode will be 2, and so on.

Group ID	Section A1	Section A2	Section B1	Section B2
1	LEJBHKFIGACONMPD	AGOJPKFNCIMBLEHD	GDOMBACPKFLENHJI	AEHKFCIJLODNPBMG
2	MPNGOKCJILFDBEAH	JFMGKLNEPBCHDAIO	DCJOGPAFBINHEKLM	MPOEGBJAKHCILNFD
3	OFLAJDBCEKIMNHPG	HCNJKAGMBDEFPIOL	EFLAIDPKCHOBNGMJ	MDHKCPOALIENBGFJ
4	FELDBNJKAIOHMGPC	NFPKOLAJEIBHGMCD	PGMAJLBFHNCKOEDI	PJDKHOBAGNCFLIME
5	HGIADLKMJBFECOPN	CKPIBEJHDLFMGANO	PEJHODFLNAKGBIMC	MBJNKEFOGDHCALPI
6	IDFGJMLHOKNCBEAP	GOCFJDBLEMIAHPNK	PNDBCAMLHIJOKEGF	CDEFGMBOAJHIKPLN

6 Report Content

Contents of the report are recommended as follows:

- Introduction
- Instruction Set
- Circuit Diagram printed in drawing paper (Will discuss about this point in the class)
- How to write and execute a program in this machine
- Special Features Implemented if any (may carry bonus marks)
- ICs used with their count
- Discussion

7 Submission Guideline

- Create a folder named "<Lab Group>_<Group ID>_Simulation" and put all the necessary simulation files in this folder.
- Create a second folder named "<Lab Group>_<Group ID>_Necessary_Content" and put all your codes to convert assembly codes into mips machine codes (or any others extra contents that will be necessary to simulate you pc).
- Finally create a third folder named "<Lab Group>_<Group ID>_Submission" and put your report along with the previously prepared two folders. Now zip this final folder and upload the zip file in moodle submission link (single submission from each group).
- Remember that proper submission will carry 10% of total assignment marks.

Submission Deadline: September 2 (Monday) upto 7am.
N.B. This doc may be updated several times. I will post in the news forum as soon as any kind of correction is made. For any kind of confusion, feel free to mail at `tmadnan10@gmail.com` with the subject "MIPS Simulation".