
MCXC0S/C1S/C1SU AS

Project SCE General Purpose MCU

Component MCX C0S/C1S/C1SU

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1. Architecture Specification

1.1. Log

Rev	Date	Owner	Updates
0.1	2025-5-26	Eric Wu	Initial Version based A20-256 AS v0.51
0.2	2025-6-11	Eric Wu	<p>Drop the requirement to split CORE domain to WAKE and MAIN to support 1.5uA leakage with UART on.</p> <p>Don't place one WWDT to System Domain to save cost.</p> <p>Drop the requirement to output CMP 8bit DAC through OPAMP</p> <p>Add back Testport.</p> <p>Reduce LPUART to 3.</p> <p>Drop MTB.</p> <p>Update IO Port Arbiter requirement</p> <p>Update WUU table</p> <p>64byte FMC cache is dropped.</p> <p>Drop Boundary Scan.</p> <p>Add detail information in Debug Chapter</p> <p>Add more information in Boot chapter based on the discussion with ROM team.</p> <p>SLOW clock divider is updated to 4, which is better for wake-up speed.</p>
0.3	25-6-27	Eric Wu	<p>Keep boundary scan per TE's request. It will take extra effort to remove it, and saving is smaller.</p> <p>Drop I3C and add 2x UART</p> <p>Update Password DBG Auth. Implementation detail based on the discussion with SOC and ROM team.</p> <p>Allocate one more input from pin for OPAMP reference.</p> <p>Add FlexPWM, eQDC to peripheral clock table.</p>
0.4	2025-7-11	Eric Wu	<p>Add the support of configurable reset vector for CR MCXC0S-2</p> <p>Drop 5V TOL IO</p> <p>Move GPIO address to IPS bridge space because of the support of IO Port.</p> <p>Fix the error of spec tables' sharepoint link.</p> <p>Add side channel resistance requirement for Password DBG Auth RTL implementation.</p> <p>Add ADC reference connection requirement.</p> <p>Update OPAMP diagram to show external reference connection.</p> <p>Fix typo of ADC channel 2/3 connection to compatible with A18.</p> <p>CMP CH2 and CH4/5 INN are reserved. CH4/5 INP should be connected to OPAMP.</p>
0.5	2025-8-6	Eric Wu	<p>Remove UART4, eQDC, and set max speed to 72MHz per CCB MCXC0S-3</p> <p>Update WUU table to align with pinout.</p> <p>Request to close NVM timing with 2 wait state at 72MHz.</p> <p>Update PORT parameter to align with pinout.</p>
0.6	2025-10-28	Jimmy Mo	Add C1SU, C1S initial version.
0.7	2025-12-2	Jimmy Mo	Update PIT, QTMR, FTM, PWT clock gen. Update key features

			Update clock definition/summary, peripheral clock summary Update OPAMP and CMP instances
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Note:

The difference between MCX A and C0S are marked with yellow.

The changes comparing with last version is marked with red.

The difference between MCX CxS and C0S are marked with **Blue**.

1.2. General Requirement

1.2.1. Block Diagram

1.2.2. Scope

C0S, [C1SU](#) and [C1S](#) is a ultra-low cost sub-family of MCX. It is based on CM23 core.

1.2.3. Key Features

C0S key features:

Shall implement CM23 core. Trustzone and MPU are not required. Fast Divider and Fast IO are required.

Shall support [72MHz](#) at SD mode. Drop MD mode to save design effort.

Shall implement 128KB flash, but marketing may only open 64KB in main flash to customer. FMC shall support the line buffer and prefetch buffer. Shall implement MBC to project flash permission.

Shall implement 8KB RAM with ECC and 4KB RAM w/o ECC. Total 12KB SRAM.

Shall implement Bootloader in IFR0 and the 48KB main flash starting from 0x0001_0000.

Shall implement 1x 16bit SE ADC.

Shall implement 1x OPAMP w/ PGA(from A18/N10) and support two positive inputs.

Shall implement 1x CMP

Shall implement DMA w/ 4 CH

Shall implement 1x CRC

Shall implement WUU

Shall implement 1x TRNG

Shall implement 1x LPI2C

Shall implement [4x](#) LPUART.

Shall implement 1x LPSPI.

Shall implement 1x FlexPWM w/ 3SM [and 1x eQDC](#).

Shall implement 2x CTimer.

Shall implement peripheral input mux.

Shall implement RTC w/o calendar.

Shall implement 1x LPTMR

Shall implement 2x WWDT

Shall implement 1x FRO192M, 1x FRO12M, 1x FRO16K and 1x OSC32K

Shall reuse A20-256 PMC/LDO but LDO driver instance should be reduced 1 to provide 12mA drive capability.

Shall keep pin compatibility with MCXA

Shall implement 4x GPIO/PORT groups. GPIO should support CM23 fast IO interface.

2x 5V TOL IO is not required.

Comparison	C0S	C1S	C1SU	C2S
Core: CM23, Trustzone and MPU are not required	Yes, 72 MHz	Yes, 72 MHz @SD mode	Yes, 96 MHz @OD mode	
Flash	128KB flash, but marketing may only open 64KB in main flash to customer.	256KB flash, support 128KB flash phantom option.	128KB flash, support 64KB flash phantom option.	
FMC: shall support the line buffer and prefetch buffer. Shall implement MBC to project flash permission.	Yes	Yes	Yes	
RAM	8KB w ECC, 4KB w/o ECC, total 12KB SRAM	8KB w ECC, 24KB w/o ECC, total 32KB SRAM	8KB w ECC, 8KB w/o ECC, total 16KB SRAM	
ROM	No ROM, as bootloader placed in the reserved flash space.	96KB	No ROM, as bootloader placed in the reserved flash space.	
Bootloader	in IFR0 and the 48KB main flash starting from 0x0001_0000	in ROM	in IFR0 and be starting from 0x0100_0000	
ADC	1x 16bit SE ADC	1x 16bit SE ADC	1x 16bit Dual ADC(Nevis4)	
OPAMP	1x OPAMP w/ PGA(from A18/N10) and support two positive inputs.	-	1x OPAMP w/ PGA and support differential inputs.	
CMP	1x CMP	1x CMP	2x CMP with 2 DAC. DAC0/1 are	

			being shared with CMP0/1/2.	
PHD	-	-	Phase Detection (PHD) are implemented by 3x CMP with 1x DAC. Refer to SD8 phase detection.	
DMA	1x 4CH	1x 8CH	1x 4CH	
CRC	1x CRC	1x CRC	1x CRC	
WUU	Yes	Yes	Yes	
TRNG	1x TRNG	1x TRNG	-	
AES	-	1x AES256	-	
LPI2C	1x LPI2C	3x LPI2C	1x LPI2C	
LPUART	4x LPUART	5x LPUART 2x w/ Modbus feature	3x LPUART, 1x w/ Modbus feature	
LPSPI	1x LPSPI	2x LPSPI	1x LPSPI	
I3C	-	1x I3C	-	
TSI	-	1x TSI	-	
SLCD	-	1x SLCD w/ 56x8	-	
FlexPWM	1x FlexPWM w/ 3SM	1x FlexPWM w/ 4SM	1x FlexPWM w/ 4SM	
CTimer	2x CTimer	3x CTimer	-	
Frequency measurement timer (FREQME)	1x FREQME	1x FREQME	1x FREQME	
Quad Timer (QTMR)	-	-	1x QTMR	
Flextimer (FTM)	-	-	1x FTM w/ 2CH	
Pulses Width Timer (PWT)	-	-	2x PWT	

Periodic Interrupt Timer (PIT)	-	-	1x PIT	
Peripheral input mux	Yes	Yes	Not required, but support XBAR	
XBAR	-	-	Yes, There's filter between Package IO and XBAR_IN.	
AOI	-	Yes	Yes	
RTC	1x RTC w/o calendar	1x RTC w/o calendar (reuse c0s)	-	
LPTMR	1x LPTMR	1x LPTMR	-	
WWDT	2x WWDT	2x WWDT	1x WWDT	
FRO12M	Yes	Yes	No	
FRO192M/144M	Yes, FRO144M	Yes, FRO144M	Yes, support generating 192MHz/96MHz/12MHz	
FRO16K	Yes	Yes	Yes	
OSC40M	-	-	-	
CLK_IN	Yes	Yes	Yes	
OSC32K	Yes	Yes	-	
PMC/LDO	Yes, with 1x LDO	Yes, with 1x LDO	Yes, with 1x LDO	
GPIO/PORT	4x GPIO/PORT groups, support fast IO interface	5x GPIO/PORT groups, support fast IO interface	4x GPIO/PORT groups, support fast IO interface	
PIN compatibility	MCXA	MCXC0S, MCXA	MCXC0S, MCXA	
Temperature Range (T _J)	-40 °C to 125 °C	-40 °C to 125 °C	-40 °C to 135 °C	

1.2.4. Power Target

C0S/C1S/C1SU:

Shall achieve 50uA/MHz/50uA/MHz/75uA/MHz running CoreMark from flash.

Because of no LPCAC, 50uA/MHz run CM from flash will be a risk.

C0S/C1S: Shall achieve 5uA leakage in PD mode.

C1S: Shall achieve 10uA leakage in low power mode with supporting TSI wakeup.

C0S: Shall achieve 400nA leakage in DPD w/o RTC and RAM retention. Wake up with 2ms.

1.2.5. Process

Shall use TSMC40ULPESF3 process.

To save cost, it is expected to use 7T library. If decides to use 7T library, the risk of 7T library can be migrated with below comments.

1. The Scan Vmin issue found in K4W1 happens in MD mode. It is recorded in CR19 K4W1 Change Request - VDD_CORE Scan Vmin Raise.pptx.
C0S drops MD mode and only keep SD mode. Scan Vmin issue is migrated. Increasing VDD_CORE in SD mode is the backup solution.
2. There is requirement to implement synchronizer with std. structure. However, the std. structure may not be ready for 7T library before C0S TO. BE team needs extra effort to do it semi-manually. Can't meet the schedule. The flow to replace std. structure was added to BE flow after K4W1 TO. Didn't receive any K4W1 customer failure caused by std. structure. The risk of using K4W1 flow to implement the synchronizer is low. C0S can follow K4W1 flow to meet schedule.

1.2.6. Temperature Range

C0S/C1S: -40 °C to 125 °C. Same requirement with MCX A.

C1SU: -40 °C to 135 °C

1.2.7. Comparison with A10

	Base Line: A10	C0S	C1S	C1SU	Comments
CPU	CM33 (96MHz)	CM23 (96MHz)	CM23 (72MHz)	CM23 (96MHz)	Single run mode to reduce design effort. CM23 supports divider.
Run mode	MD, SD	SD	SD	OD	
Debug	Jtag/SWD/ITM/DWT	SWD	SWD	SWD	
Bus Matrix	Multilayer AHB Matrix APB Bridge, AIPS Bridge	Multilayer AHB Matrix AIPS Bridge	Multilayer AHB Matrix AIPS Bridge	Multilayer AHB Matrix AIPS Bridge	Better change Peri. Input Mux to APB bus to remove the APB bridge.
SRAM	32KB, 8KB with ECC, 4KB cache	12KB, 8KB w/ ECC	32KB, 8KB w/ ECC	16KB, 8KB w/ ECC	
Flash	128KB w/ LPCAC	128KB	256KB	128KB	64KB flash is required. Can implement boot code in flash to save cost and speed up schedule.
ROM	16KB	NA (implement Boot in flash)	96KB	NA (implement Boot in flash IFR)	
Safety	EIM, ERM, WDT	EIM, ERM, 2x WDT	EIM, ERM, 2x WDT	EIM, ERM, 1x WDT	Auto need SWT, but single is enough.
System	DMA, InputMux, CMC, WUU, VBAT, CRC	DMA, InputMux, CMC, WUU, VBAT, CRC, TRNG	DMA, InputMux, AOI, CMC, WUU, VBAT, CRC, TRNG, AES256	DMA, InputMux, AOI, XBAR, CMC, WUU, VBAT, CRC, TRNG	
Communication Interface & HMI	LPUART, LPI2C, LPSPI, USB FS, I3C, FlexIO	4x LPUART, LPI2C, 1x LPSPI, 1x I3C, GPIO	5x LPUART, 3x LPI2C, 2x LPSPI, 1x I3C, TSI, SLCD, GPIO	3x LPUART, 1x LPI2C, 1x LPSPI, GPIO	Should update GPIO to support Fast IO.
Timers	FlexPWM, eQDC, Ctimer, LPTMR, Wake Timer, uTick	FlexPWM, eQDC, Ctimer, LPTMR, RTC	FlexPWM w/ 4SM, eQDC, Ctimer, LPTMR, RTC w/o calendar	FlexPWM w/ 4SM, eQDC, Ctimer, LPTMR, RTC, 1x Quad Timer, 1x Flextimer, 2x PWT, 1x PIT	Request to compatible with MCX 0C and S32K1
Clock	FRO192M, FRO12M, FRO16K, 8~50MHz OSC	FRO192M, FRO12M, FRO16K, OSC32K	FRO192M, FRO12M, FRO16K, OSC32K, OSC40M	FRO192M, FRO12M, FRO16K, OSC32K	
Analog	16bit SE ADC, CMP	16bit SE ADC, CMP, 1x OPAMP w/ PGA	16bit SE ADC, CMP, 4x OPAMP w/ PGA	16bit Dual ADC, 7x CMP, 3x OPAMP w/ PGA	
PMC	Capless LDO VDD PoR, VDD LVD/HVD/AGDET VDD_CORE LVD, SRAM Retention	Capless LDO VDD PoR, VDD LVD/HVD/AGDET VDD_CORE LVD, SRAM Retention LDO	Capless LDO VDD PoR, VDD LVD/HVD/AGDET VDD_CORE LVD, SRAM Retention LDO	Capless LDO VDD PoR, VDD LVD/HVD/AGDET VDD_CORE LVD, SRAM Retention	AGDET can be disabled if don't want to use it but will not make design change to

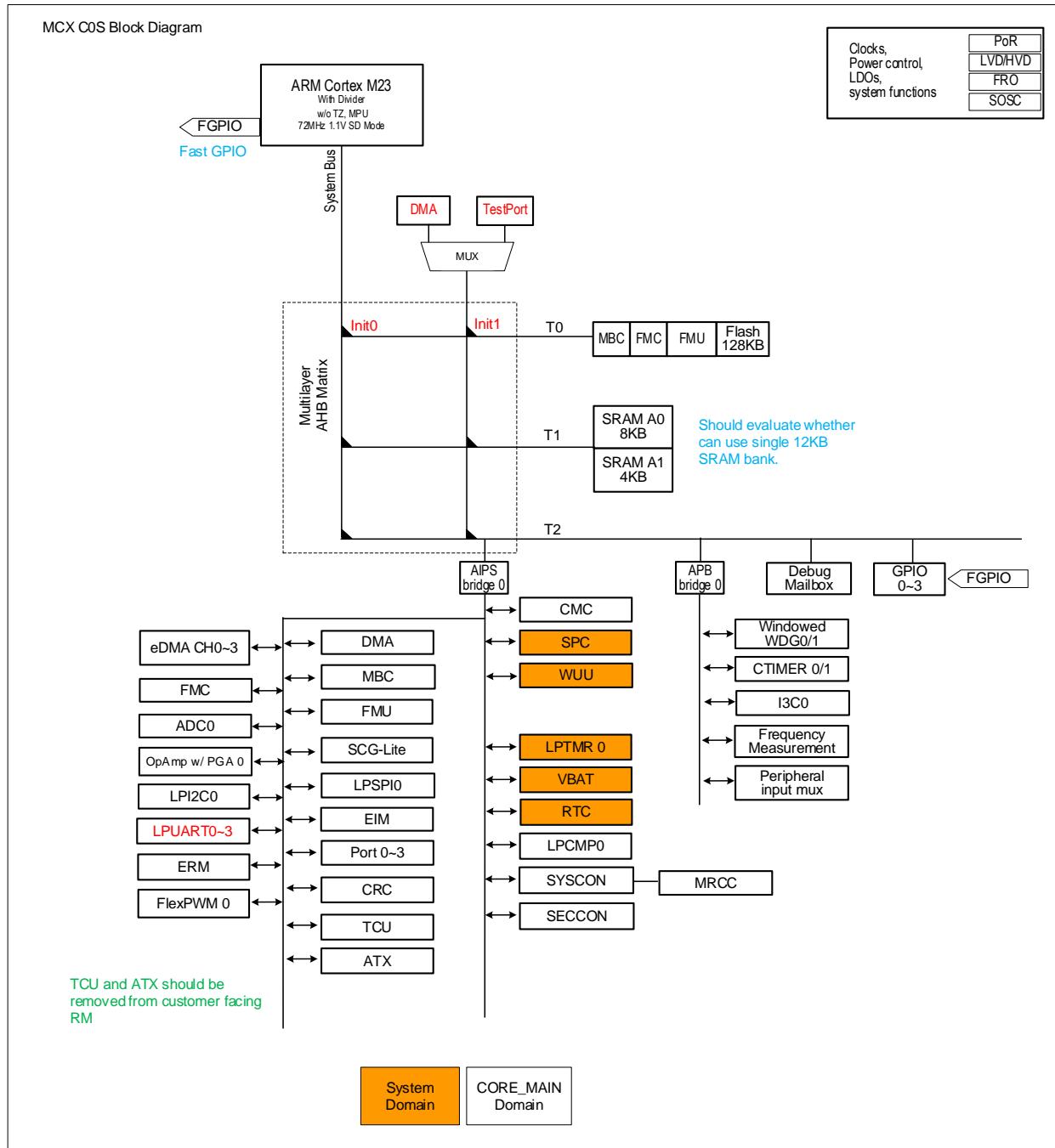
	LDO			LDO	remove it.
Power Domain	Core Domain (GO1) System Domain (DGO)	Core Domain (GO1) System Domain (GO2)	Core Domain (GO1) System Domain (GO2)	Core Domain (GO1) System Domain (GO2)	
Power	60uA/MHz CoreMark, 520nA w/ waketimer 790nA w/ waketimer, 8KB RAM	50uA/MHz CoreMark, 400nA w/o RTC, RAM Retention	50uA/MHz CoreMark, 400nA w/o RTC, RAM Retention	75uA/MHz CoreMark, 400nA w/o RTC, RAM Retention	Drop the requirement to support 1.5u leakage w/ RTC, 12KB RAM Retention and UART on.
Process	TSMC40ULPESF 3 9T (TJ125)	TSMC40ULPESF3 7T (TJ125) 1.1V	TSMC40ULPESF3 7T (TJ125) 1.1V	TSMC40ULPESF3 7T (TJ135) 1.2V	
Pinmux		Should be compatible with MCX A	Should be compatible with MCX A	Should be compatible with MCX A	Should consider the compatibility with MCX0C04x (KL)
Quality Level	Level2 (400ppm)	Level2 (400ppm)	Level2 (400ppm)	Level2 (400ppm)	

The difference between A10 and C0S are marked with **yellow**.

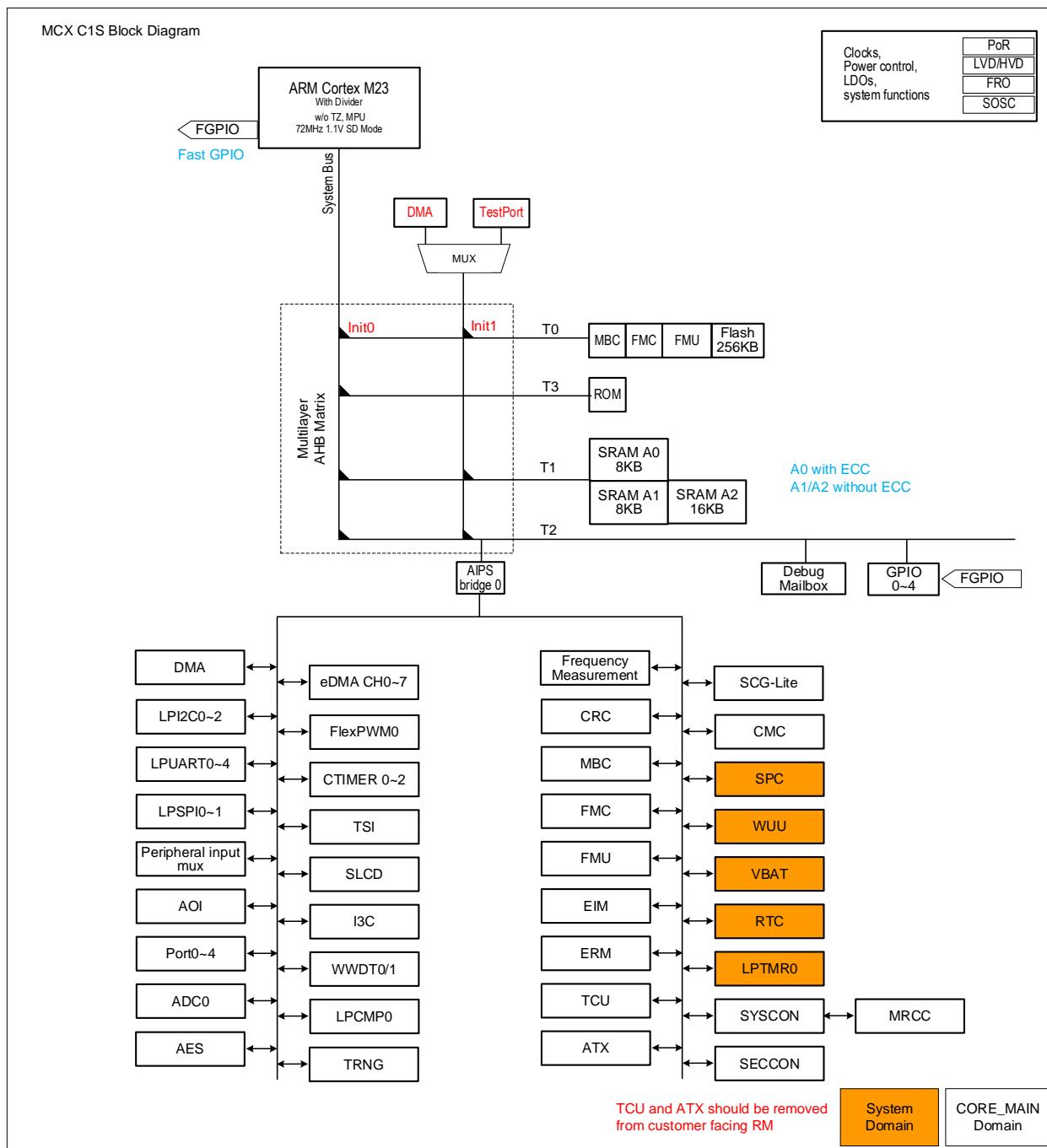
The difference between C1S/C1SU and C0S are marked with **blue**.

1.3. System bus

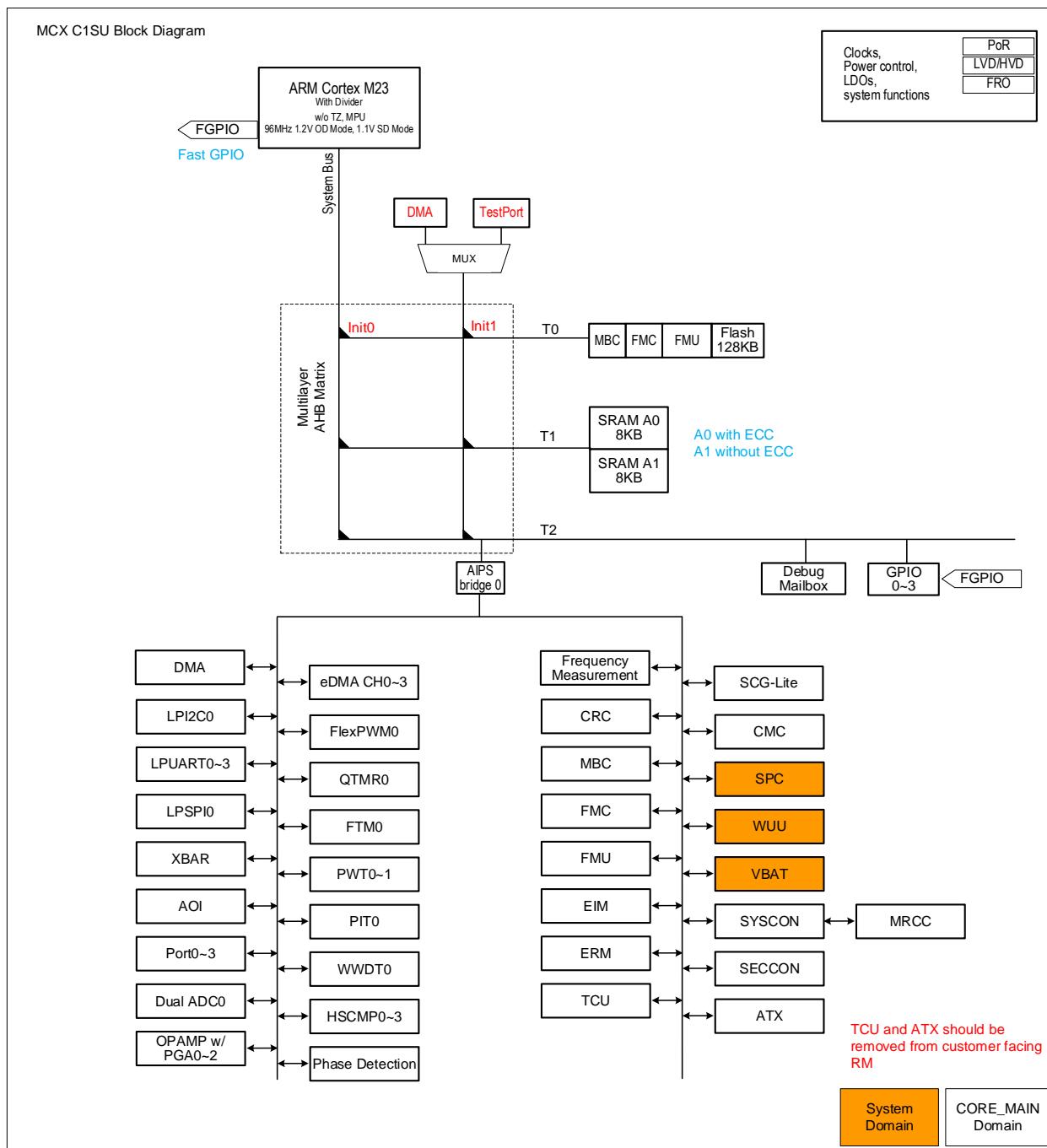
1.3.1. System Bus Diagram



MCX C0S Block Diagram



MCX C1S Block Diagram



MCX C1SU Block Diagram

1.3.2. BUS Architecture

Multi-layer AHB Matrix

One multi-layer AHB matrix is implemented. There are two bus initiator ports and three/four target ports.

AHB Matrix priority control register

Bit	Initiator Name	Initiator AHB ID	Reset Value
1:0	CM23 System Bus	0x0	0x0
3:2	Reserved	0x1	0x0
5:4	Reserved	0x2	0x0
7:6	Reserved	0x3	0x0
9:8	eDMA0 Controller AHB Bus	0x5	0x0
	Test Port		
11:10	Reserved	0x4	0x0
13:12	Reserved	0xC	0x0
15:14	Reserved	0x7	0x0
17:16	Reserved	0x8	0x0
19:18	Reserved	0x9	0x0
21:20	Reserved	0xA	0x0
23:22	Reserved	0xB	0x0
25:24	Reserved	0x6	0x0
27:26	Reserved	0xD	0x0
29:28	Reserved	0xE	0x0
31:30	Reserved	Reserved	0x0

For C1S and C1SU, prefer to remove the APB bridge and use AIPS bridge to instead of that.

AHB to AIPS Bridge

The bridge connects IPS/APB interface peripherals. There is PPMR inputs of AIPS bridge. PPMR signal is used to indicate whether a peripheral is power down or clock gated. SoC should correctly generate the PPMR signal and connect it to AIPS PPMR inputs.

VPB to APB wrapper

Peripheral Input Mux, WWDT and CTimer are VPB interface. If there is VPB to APB wrapper, can save the AHB to APB bridge. It is nice to have, if can meet the schedule.

1.4. Processor Core

1.4.1. Cortex-M23 configuration

ACG : Yes, include architecture level clock gating

BE: No, little-endian

BKPT: 2

BUSPROT: 0, no parity check for AHB/IO/SBIT APB bus

DBG: Yes

FLOPPARITY: No

HWF: No, fetch instructions using 32bit AHB-lite access whenever possible.

IOP: Yes

IRQDIS0: 0x6B08_D3C1

IRQDIS1:0x7302_0E70

IRQDIS2:0xFFFF_F87E

MPU_NS: 0

MPU_S: 0

NUMIRQ: **75**

RAR: 0, the registers in the design that do not require a reset have no reset

SAU:0

SDIV: 0, include the fast 21 cycle divider

SECEXT: No

SMUL: NO, implement the fast single cycle multiplier.

SYST: 1, include systick timer

VTOR: Yes, include vector table offset register

WPT: 2, watch point unit number

CTI: No

ETM: No

MTB: No

MTBWIDTH: 11, 2KB

WIC: Yes

WICLINE: TBD, depending on NVIC table.

AHBSLV: No, the SLV port implements a CM23 processor DAP-specific protocol

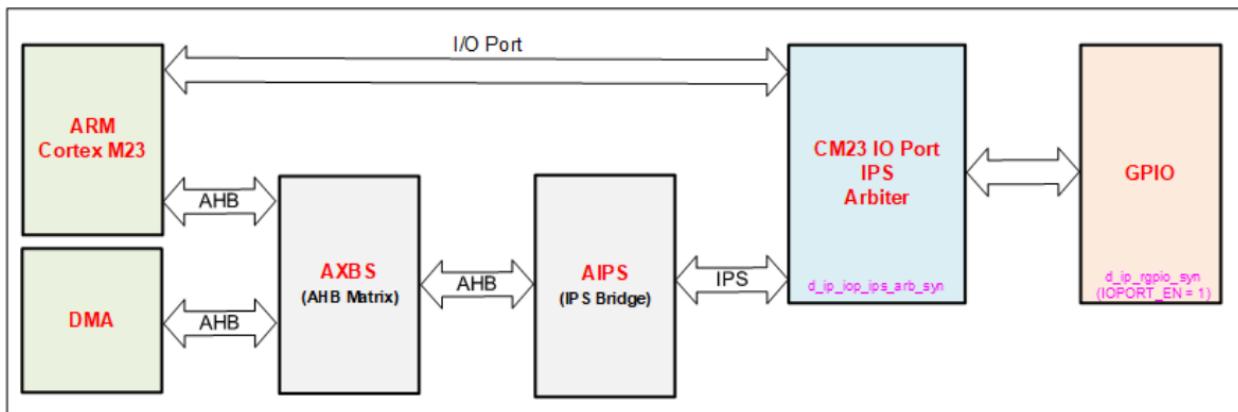
BASEADDR: **0xE00FF003**

HALTEV: No, exclude halt event signaling support, debugger should read DHCSR.SA_HALL register to identify whether CPU is halt.

JTAGnSW: No, implement SWD
 SWMD: No, no multi drop
 TARGETID: TBD
 SBISTC: No, STL hardware feature is not implemented.
 SBIST_DL_CYCLES: 0xA0
 SBIST_DL_RESET:0
 SBIST_PSI: 0xF

1.4.2. CM23 I/O Port

I/O Port Diagram



SOC should implement an IO Port IPS Arbiter for AIPS bridge and I/O Port to access GPIO. I/O port access priority is higher than IPS bridge.

I/O Port bus doesn't support wait state. IO Port Arbiter should not insert wait state.

GPIO supports auto clock gating. It takes extra clock cycles to recover the clock. To simplify IO Port arbiter design, SW should close GPIO auto clock gating if CM23 needs access the corresponding GPIO mode through I/O Port.

The IO Port IPS Arbiter should implement a 20-bit parameter to configure the base address of the GPIO module when it is accessed from IO Port. GPIO base address should be remapped as below.

C0S	AHB Access Base Address	IO Port Access Base Address
GPIO0	0x400F_3000	0xF800_1000
GPIO1	0x400F_4000	0xF800_2000
GPIO2	0x400F_5000	0xF800_3000
GPIO3	0x400F_6000	0xF800_4000

C1SU	AHB Access Base Address	IO Port Access Base Address
GPIO0	0x4007_3000	0xF800_1000
GPIO1	0x4007_4000	0xF800_2000
GPIO2	0x4007_5000	0xF800_3000
GPIO3	0x4007_6000	0xF800_4000

C1S	AHB Access Base Address	IO Port Access Base Address
GPIO0	0x4007_3000	0xF800_1000
GPIO1	0x4007_4000	0xF800_2000
GPIO2	0x4007_5000	0xF800_3000
GPIO3	0x4007_6000	0xF800_4000
GPIO4	0x4007_7000	0xF800_5000

Shall implement IO Port IPS Arbiter for each GPIO module.

GPIO IOPORT_EN parameter should be enabled.

1.4.3. Nested Vectored Interrupt Controller (NVIC)

1.4.3.1. Non-Maskable Interrupt (NMI)

Same implementation with A10.

1.4.3.2. CPU0 interrupt channel assignments

[NVIC_Configuration_MCXAC0S.xlsx.url](#)

[NVIC_Configuration_MCXC1S.xlsx.url](#)

[NVIC_Configuration_MCXC1SU.xlsx.url](#)

1.4.4. Memory Map

[memory_map_MCXC0S.xlsx.url](#)
[memory_map_MCXC1S.xlsx.url](#)
[memory_map_MCXC1SU.xlsx.url](#)

1.5. System Peripherals

1.5.1. AND/OR/INVERT (AOI)

C0S: AOI is not required.

C1S/C1SU: 1x AOI.

1.5.2. Cyclic Redundancy Check (CRC)

C0S/C1S/C1SU: This device implements 1x CRC.

1.5.3. enhanced Direct Memory Access (eDMA3)

C0S /C1SU: This device implements 1x DMA with 4 CHs.

C1S: This device implements 1x DMA with 8 CHs.

Same implementation with A10.

Channel Multiplexor

[DMA_Configuration_MCXC0S.xlsx.url](#)

[DMA_Configuration_MCXC1S.xlsx.url](#)

[DMA_Configuration_MCXC1SU.xlsx.url](#)

1.5.4. Error Injection Module (EIM)

C0S/C1S/C1SU: This device implements 1x EIM.

Channel 0 is assigned to SRAM A0.

1.5.5. Error Record Module (ERM)

C0S/C1S/C1SU: This device implements 1x EIM.

Channel 0 is assigned to SRAM A0.

Channel 1 is assigned to Flash.

1.5.6. Master Block Checker (MBC)

C0S/C1S/C1SU: This device implements MBC to protect flash access permission. IFR1 and IFR0 granularity is 2KB. Main flash granularity is 8KB

```
S0_BLKSZL2(13),  
S1_BLKSZL2(11),  
S2_BLKSZL2(11),  
S3_BLKSZL2(0),  
S0_NUMBLK(16/32), /* C0S/C1SU: 16, C1S:32 */  
S1_NUMBLK(16),  
S2_NUMBLK(4),  
S3_NUMBLK(0),
```

MBC default access permission configuration should be same with A10.

1.5.7. Peripheral Input Mux

[MCXAC0S_Peripheral_Input_Assignments.xlsx.url](#)

[MCXC1S_Peripheral_Input_Assignments.xlsx.url](#)

1.5.8. XBAR

[MCXC1SU_XBAR_ADC_CMP_PHD_TABLE.xlsx.url](#)

1.5.9. MAU

C0S/C1S/C1SU: Not required.

1.5.10. SYSCON

C0S/C1S/C1SU: Reuse A2TS SYSCON + SECCON.

It needs to implement extra registers to support the requirement recorded in other chapters.

1.5.11. Wakeup Unit (WUU)

Need to be update for C1S, C1SU

WUU Input	Source Description (C0S)	Source Description (C1S)	Source Description (C1SU)
WUU_P0	Reserved		
WUU_P1	Reserved		
WUU_P2	P0_16		
WUU_P3	Reserved		
WUU_P4	Reserved		
WUU_P5	Reserved		
WUU_P6	P1_0 / LPTMR0_ALT3		
WUU_P7	P1_3		
WUU_P8	Reserved		
WUU_P9	Reserved		

WUU_P10	P1_8		
WUU_P11	P1_11		
WUU_P12	Reserved		
WUU_P13	Reserved		
WUU_P14	Reserved		
WUU_P15	Reserved		
WUU_P16	Reserved		
WUU_P17	Reserved		
WUU_P18	P2_0		
WUU_P19	P2_3		
WUU_P20	P2_12		
WUU_P21	Reserved		
WUU_P22	P3_0		
WUU_P23	P3_8		
WUU_P24	P3_11		
WUU_P25	P3_14		
WUU_P26	P3_28		
WUU_P27	P3_29		
WUU_P28	Reserved		
WUU_P29	Reserved		
WUU_P30	Reserved		
WUU_P31	CMP0_OUT, CMP0 Hard output		
WUU_M0IF	SPC Interrupt		
WUU_M1IF	RTC		

WUU_M2IF	Reserved		
WUU_M3IF	Reserved		
WUU_M4IF	Reserved		
WUU_M5IF	Reserved		
WUU_M6IF	LPTMR0 Interrupt		
WUU_M7IF	Reserved (LPTRM1)		
WUU_M8IF	Reserved		
WUU_M9IF	Reserved		
WUU_M0DR	Reserved		
WUU_M1DR	Reserved		
WUU_M2DR	Reserved		
WUU_M3DR	Reserved		
WUU_M4DR	LPTMR0 DMA Request		
WUU_M5DR	Reserved		
WUU_M6DR	LPTMR0 Trig		
WUU_M7DR	Reserved		
WUU_M8DR	Reserved		
WUU_M9DR	Reserved		

1.5.12. VBAT Wrapper

C0S/C1S: VBAT wrapper should support FRO16K and OSC32K.

C1SU: VBAT wrapper should support FRO16K.

Wakeup_b pin is not required.

1.6. Memory

1.6.1. Flash

C0S: 1x 128KB flash array is implemented. Same with A10.

C1S: 1x 256KB flash array is implemented. Same with A10.

C1SU: 1x 128KB flash array is implemented. Same with A10.

1.6.1.1. Flash ECC

Same with A10.

1.6.1.2. Flash Cache

C0S/C1S/C1SU: FMC cache is not required.

C0S/C1S/C1SU: Line buffer and prefetch buffer configuration should be same with FMC.

1.6.1.3. Flash Swap

C0S/C1S/C1SU: Flash swap (remap) function is dropped.

1.6.1.4. Flash Performance

C0S/C1S: SD mode: -40°C/125°C, 0.99V, 72 MHz, 1 wait state must have. Based on silicon results, flash hard macro can support 36MHz access speed in SD mode. BE should try to close timing with 1 wait state at 72MHz. Boot CPU frequency: 48MHz.

C1SU: OD mode: -40°C/135°C, 1.2V, 96 MHz, 1 wait state must have. Based on silicon results, flash hard macro can support 48MHz access speed in OD mode. BE should try to close timing with 1 wait state at 96MHz.

1.6.1.5. Flash Mass Erase

Same with A20.

1.6.1.6. Flash IFR0 Erase

Same with A20.

1.6.1.7. FMU Test APB

Same with A20.

1.6.2. LPCAC

Not required

1.6.3. SRAM

SRAM configuration:

C0S/C1S/C1SU: Should implement 8KB SRAM A0 with ECC per 32bit.

C0S: Should implement 4KB SRAM A1 w/o ECC.

C1S/ C1SU: Should implement 8KB SRAM A1 w/o ECC.

C1S: Should implement 16KB SRAM A2 w/o ECC.

SRAM Execute Permission control:

- SRAM_XEN[0] reserved. Expect no real register.
- C0S/C1SU: SRAM_XEN[1] reserved. Expect no real register.
- **C1S:** SRAM_XEN[1] controls RAM A2 16KB.
- SRAM_XEN[2] controls RAM A0 8KB.
- SRAM_XEN[3] controls RAM A1 4KB/8KB.

1.6.4. Read Only Memory (ROM)

C0S/C1SU: No ROM.

C1S: 96KB ROM

1.7. Security

1.7.1. Security Features.

- MPU
 - No MPU
- Crypto Algorithm Accelerator
 - No crypto accelerator
- Key Management
 - No key management
- C0S/C1S: Random number Generator. **C1SU:** No RNG
 - The chip should implement 1x TRNG.
 - Should implement an async IPS gaster for TRNG to use FRO12M.
- Access control
 - Same with A20.
- Security Sensors
 - LVD/HVD/AGDET implementation is same with A20-256.
 - No CDOG.
- Security Violation Reset
 - Same with A20-256
- Security Storage auto Zeroize
 - Not required.
- **C0S/C1S/C1SU:** Lifecycle
 - Reference boot chapter
- **C0S/C1S/C1SU:** ROP
 - Reference boot chapter
- **C1S:** AES256 hardware IP
 - The chip should implement 1x AES and support AES256.

1.7.2. GLIKEY

Not required.

1.7.3. TDET

No TDET

1.7.4. UDF

C0S/C1SU: No UDF

C1S: UDF

1.7.5. CMC Boot Statue Register

Same with A20.

1.7.6. Password Based Debug Authentication

C0S/C1S/C1SU:

During boot, NXP bootloader should copy the debug authentication a password from customer configure region in IFR0 to register.

When there is a need to enable debug, while customer's application is running, user should input the password from debug port. HW should compare password with the one recorded in SECCON register. If it is matched, and LC is in ROP1 states, HW should enabled debug port.

DBG Mailbox will be updated to support the change.

- Implements one 128bit password register for Bootloader copy the password from OEM_CFG region.
 - Accessed from AHB bus.
 - R/W can be locked by 4bits registers
 - Boot loader should lock the register before jump to user image.
- Password comparison
 - Should implement SCR (Side Channel Resistance) parameter to select whether SCR is required.
 - SCR = 0
 - A 32bit password for user input through SWD/Jtag interface
 - Input from debugger.
 - Write once and write only
 - User should input the 128bit password from word0 to word3 sequentially.
 - HW compare the word0 to word3 whenever a word is input and record the compare results of the word. Final results should be provided after all 4 words are input. The compare results in the middle should not be readable by SW.
 - HW can enabled debug port if password is matched and in ROP1 states.
 - SCR = 1
 - Should record the whole 128bit password.
 - Can implement a start comparison register for user to start comparison, after input the 128bit password.
 - The comparison should be done continuously.

Decide to use the configuration w/o side channel resistance to save cost.

- The function of hardware password debug authentication can be disabled and locked.
- Password authentication should also control the connection between CM23 AP and DAP. When password authentication passed in ROP1 state, should enable the connection between CM23 AP and DAP. (C0S/C1S should implemented password authentication, C1SU nice to have)

1.8. Timers

1.8.1. Code Watchdog (CDOG)

Not required.

1.8.2. Standard Counter/Timers (CTimer)

C0S: Shall implement 2x Ctimers.

C1S: Shall implement 3x Ctimers.

C1SU: Not required.

1.8.3. FlexPWM

C0S: Shall implement 1x 3SM FlexPWM.

Same configuration with A10.

C1S: Shall implement 1x 4SM FlexPWM.

C1SU: Shall implement 1x 4SM FlexPWM.

1.8.4. Quad Decode (eQDC)

eQDC is not required.

1.8.5. Frequency Measurement Unit (FREQME)

C0S/C1S/C1SU: Shall implement FME.

1.8.6. LPTMR

C0S/C1S Shall implement 1x LPTMR.

C1SU: Not required.

1.8.7. OS Event Timer

Not required.

1.8.8. Micro-Tick Timer (UTICK)

Not required.

1.8.9. Wakeup Timer

Not required.

1.8.10. RTC

C0S: Shall implement 1x RTC without calendar

Same with A20.

C1S: Shall implement 1x RTC without calendar

C1SU: Not required.

1.8.11. Windowed Watchdog Timer (WWDT)

C0S/C1S: Shall implement 2x WWDT.

Same with A2TS.

C1SU: Shall implement 1x WWDT.

1.8.12. Quad Timer (QTMR)

C0S/C1S: Not required.

C1SU: Shall implement 1x Quad Timer(QTMR).

1.8.13. Flextimer (FTM)

C0S/C1S: Not required.

C1SU: Shall implement 1x Flextimer (FTM) with 2 channels.

1.8.14. Pules Width Timer (PWT)

C0S/C1S: Not required.

C1SU: Shall implement 2x PWT.

1.8.15. Periodic Interrupt Timer (PIT)

C0S/C1S: Not required.

C1SU: Shall implement 1x PIT.

1.9. Communication Peripherals

1.9.1. FlexCAN

No required.

1.9.2. FlexIO

Not required.

1.9.3. I3C

C1S: Shall implement 1x I3C.

C0S/C1SU: Not required.

1.9.4. LPI2C

C0S/C1SU: Shall implement 1x LPI2C.

C1S: Shall implement 3x LPI2C.

Same configuration with A20-256.

1.9.5. LPSPI

C0S/C1SU: Shall implement 1x LPSPI.

C1S: Shall implement 2x LPSPI.

Same configuration with A20-256

1.9.6. LPUART

C0S: Shall implement 4x LPUART.

LPUART 0~3 configuration are with A20-256.

C1S: Shall implement 5x LPUART, shall support RS485.

C1SU: Shall implement 3x LPUART.

1.9.7. USB FS

Not required

1.10. Analog Peripherals

1.10.1. ADC

C0S/C1S: Should implement 1x 16bit SE ADC.

ADC configuration is same with A20-256.

ADC Reference:

VREFH0 = VDD_ANA

VREFH1 = VREFI (from IO)

VREFH2 = VDD_ANA

VREFL = VSS_ANA

ADC channel table is to be updated.

Notes: C1S shall remove **OPAMP**.

Logical	Physical	ADC0	Description
0	0	ADC0_A0	VDD domain, 40 Ohm
1	1	ADC0_A1	VDD domain, 40 Ohm
2	2	ADC0_A2	VDD domain, 40 Ohm
3	3	OPAMPO_INT/	VDD domain, 40 Ohm
4	4	ADC0_A4	VDD domain, 40 Ohm
5	5	ADC0_A5	VDD domain, 40 Ohm
6	6	ADC0_A6	VDD domain, 40 Ohm
7	7	ADC0_A7/VREFI	VDD domain, (Analog port resistor TBD)
8	8	ADC0_A8	VDD domain, analog mux
9	8	ADC0_A9	VDD domain, analog mux
10	8	ADC0_A10	VDD domain, analog mux
11	8	ADC0_A11	VDD domain, analog mux
12	8	ADC0_A12	VDD domain, analog mux
13	8	ADC0_A13	VDD domain, analog mux

14	8	ADC0_A14	VDD domain, analog mux
15	8	ADC0_A15	VDD domain, analog mux
16	8	ADC0_A16	VDD domain, analog mux
17	8	ADC0_A17	VDD domain, analog mux
18	8	ADC0_A18	VDD domain, analog mux
19	8	ADC0_A19	VDD domain, analog mux
20	ADC0/2/ 3/: 8 ADC1:9	ADC0_A20	VDD domain, analog mux
21	ADC0/2/ 3/: 8 ADC1:9	ADC0_A21	VDD domain, analog mux
22	ADC0/2/ 3/: 8 ADC1:9	ADC0_A22	VDD domain, analog mux
23	8	ADC0_A23	VDD domain, analog mux
24	10	VSSA	
25	11	ATX2	
26	14	Tempeature+	
27	15	PMC BG	ADC Internal PMC Bandgap, pmc_1vbuf_ana_1p8v
28	9	OpAMP0_OBS	,
29	11	VDDA/4	PMC Resistive dividers
30	12	ATX0	
31	13	ATX1	

C1SU: 1x 16bit dual ADC, **need to add C1SU ADC requirement, refer to Nevis4**

1.10.2. Analog Comparator (CMP)

C0S/C1S: Should implement 1x CMP.

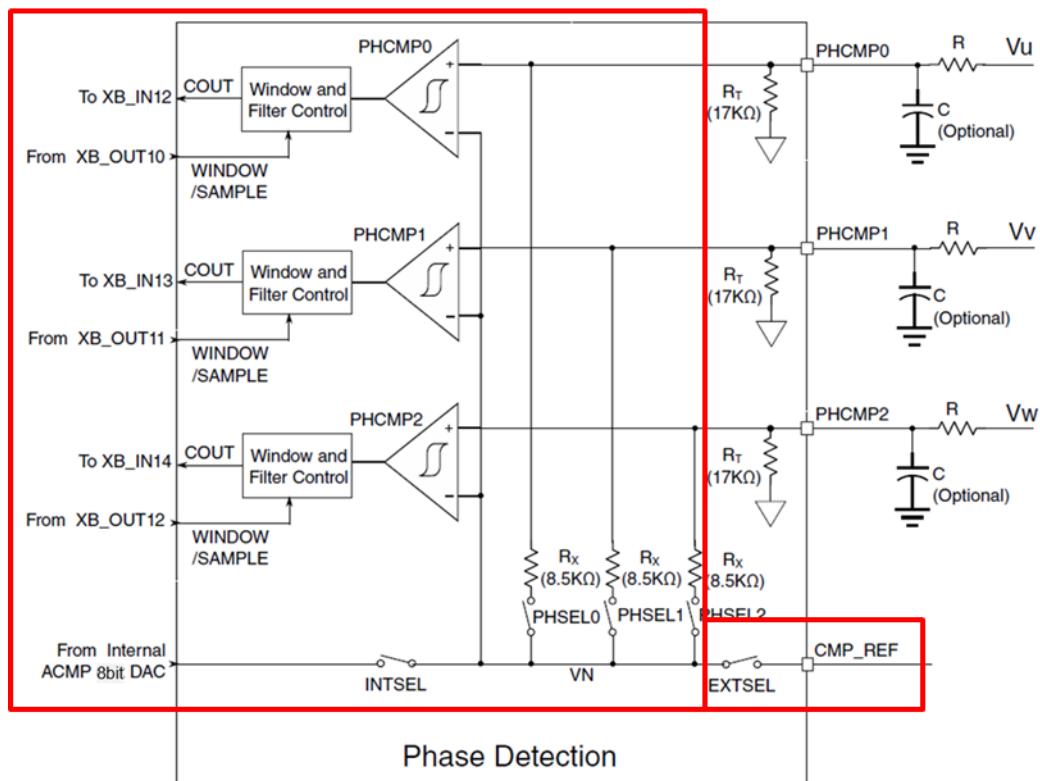
CMP channel table. Notes: C1S shall remove OPAMP.

Channel	CMP0_P	CMP0_N	Domain
0	CMP0_IN0	CMP0_IN0	VDD
1	CMP0_IN1	CMP0_IN1	VDD
2	Reserved	Reserved	VDD
3	CMP0_IN3	CMP0_IN3	VDD
4	OPAMP0_OUT	Reserved	VDD_ANA
5	OPAMP0_INT	Reserved	VDD_ANA
6	ATX0	ATX0	VDD
7	CMP0_DAC	CMP0_DAC	Internal

C1SU: 2x CMP, **need to add C1SU CMP requirement**

1.10.3. Phase Detection (PHD)

C1SU: shall implement 1x PHD with 3x CMP and 1x DAC, refer to SD8.



1.10.4. 12bit DAC

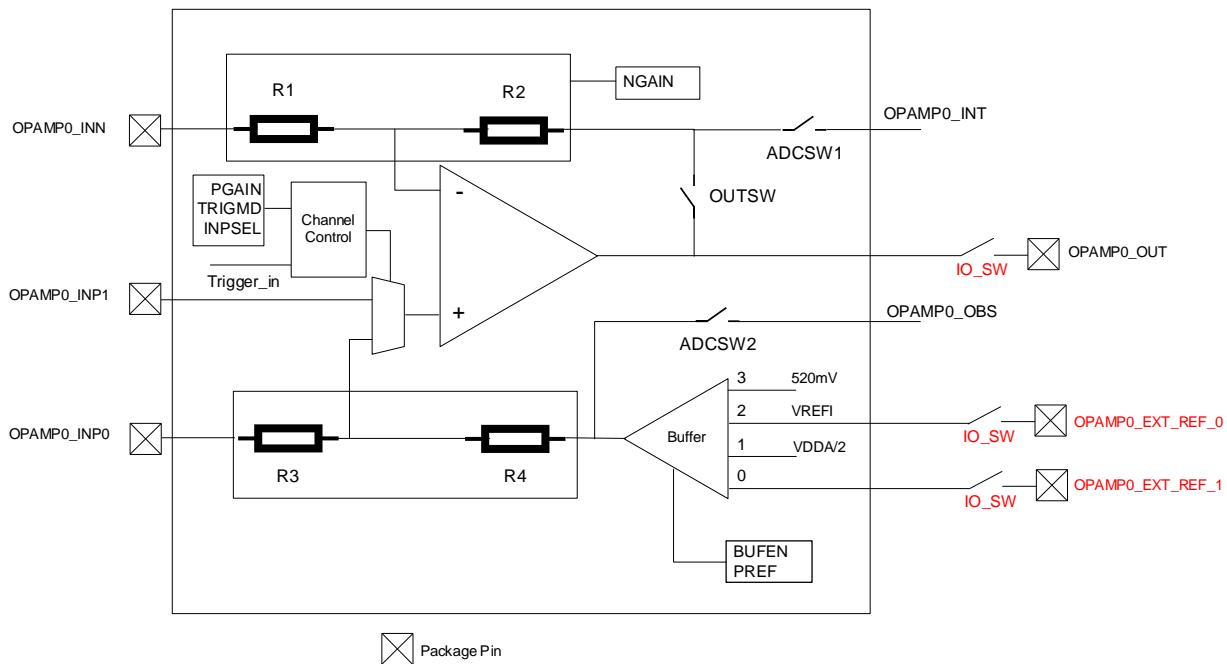
Not Required

1.10.5. OpAMP

C0S: Should implement 1x OPAMP with PGA.

C1SU: Should implement 3x OPAMP with PGA and offset. Need to change IP.

C1S: Not required.



OPAMP0_OUT should be connected to pin through the IO analog channel with switch (IO_SW). By default, analog mux is disabled. OPAMP0_OUT will be assigned a PIN MUX function number. If the pin is configured to OPAMP0_OUT function, the analog mux should be enabled.

Auto trig function to select positive input source is disabled. Should use SW to select the positive. input source.

Allocate two locations on pin to provide reference externally. The enable of the input should be controlled by IO mux.

When OPAMP is configured to buffer mode, must enable OPAMP_OUT mux and use ADC channel in OPAMP_OUT pin to measure OPAMP output.

The above requirements are for C0S.

C1SU:

- 3x OPAMP
- Use PGA wrapper + A20 hard Marco
- **Offset: $\frac{1}{4}$, $\frac{1}{2}$ VDDA.**
- Not support rail to tail
- Support differential inputs, and positive and negative inputs of amplifier connect to external channels.
- Supports using internal resistor and capacitor to build feedback loop. Configurable internal resistance net determines different gain. Configurable Gain: 3/4/5/6.5/9/11/14/19.
- Each output of OPAMP should be connected to ADC input.
- Not support output to pad

- Bandwidth (GBW): 6MHz
- Refer to A20.

1.11. Human Machine Interface (HMI)

1.11.1. General Purpose Input/Output (GPIO)

C0S/C1SU: Should implement 4x RPGIO module.

C1S: Should implement 5x RPGIO module.

C0S/C1S/C1SU: RGPI0 should enable IOPORT_EN parameter to support CM23 fast IO.

1.11.2. Port Control (PORT)

POR Parameter ([Will be updated in AS v0.4](#))

Design and Verification can reference Pinout table.([Need to be updated](#))

Parameter	PORT0	PORT1	PORT2	PORT3	PORT4
PIN_DIS	32'hFFFC_FFB0	32'h1FFF_F0F0	32'h18CC_CFC0	32'h18FF_70FC	
PINPUS_RST	32'h0000_0009	32'h2000_0000	32'h0000_0000	32'h2000_0000	
PINPUE_RST	32'h0000_000B	32'h2000_0000	32'h0000_0000	32'h2000_0000	
PINPUV_RST	32'h0000_0000	32'h0000_0000	32'h0000_0000	32'h0000_0000	
PINSRE_RST	32'h0000_0000	32'h0000_0000	32'h0000_0000	32'h0000_0000	
PINPFE_RST	32'h0000_0000	32'h2000_0000	32'h0000_0000	32'h0000_0000	
PINODE_RST	32'h0000_0000	32'h2000_0000	32'h0000_0000	32'h0000_0000	
PINDSE0_RST	32'h0000_0005	32'h0000_0000	32'h0000_0000	32'h0000_0000	
PINDSE1_RST	32'h0000_0000	32'h0000_0000	32'h0000_0000	32'h0000_0000	
PINMUX_RST	32'h0000_000F	32'h2000_0000	32'h0000_0000	32'h2000_0000	
PINIBE_RST	32'h0000_000B	32'h0000_0000	32'h0000_0000	32'h2000_0000	
PINPUS_DIS	32'h0000_0000	32'h0000_0000	32'h0000_0000	32'h0000_0000	
PINPUE_DIS	32'h0000_0000	32'h0000_0000	32'h0000_0000	32'h0000_0000	
PINPUV_DIS	32'hFFFF_FFFF	32'hDFFF_FEFF	32'hFFFF_FFFF	32'hFFFF_FFFF	
PINSRE_DIS	32'h0000_0000	32'h0000_0000	32'h0000_0000	32'h0000_0000	

Parameter	PORT0	PORT1	PORT2	PORT3	PORT4
PINPFE_DIS	32'h FFFF _FFFF	32'h FFFF _FCFC	32'h FFFF _FFFF	32'h FFFF _FFF C	
PINODE_DIS	32'h0000_0000	32'h0000_0000	32'h0000_0000	32'h0000_0000	
PINDSE0_DIS	32'h0000_0000	32'h0000_0000	32'h0000_0000	32'h0000_0000	
PINDSE1_DIS	32'h FFFF _FFFF	32'h3FFF_FCFF	32'h FFFF _FFFF	32'h FFFF _FFF C	
PINMUX0_DIS					
PINMUX1_DIS					
PINMUX2_DIS					
PINMUX3_DIS					
PINLOCK_DIS					
PINEFT_DIS	32'h FFFF _FFFF	32'h FFFF _FFFF	32'h FFFF _FFFF	32'h FFFF _FFFF	
PINIBE_DIS	32'h0000_0000	32'h0000_0000	32'h0000_0000	32'h0000_0000	
PININV_DIS	32'h0000_0000	32'h0000_0000	32'h0000_0000	32'h0000_0000	
PINAUX_DIS	32'h FFFF _FFFF	32'h FFFF _FFFF	32'h FFFF _FFFF	32'h FFFF _FFFF	
PINMUX_NUM	14	14	14	14	
CALIB_WD6	6	6	1	6	
CALIB_RST	24	24	0	24	
ASYNC_EN	0	0	0	0	

1.11.3. SLCD

C0S/C1SU: Not required

C1S: shall implement 56x8 segments and support up to 64 segments and up to 8 commons.

1.11.4. TSI

C0S/C1SU: Not required

C1S: shall support 70 channels and require supporting TSI sensing and wakeup for low power mode. The current should be lower than 10uA with 100Hz in low power mode. IP is based on A2TS.

1.12. Clock Architecture

1.12.1. Clock Management

C0S/C1S:

The chip implements FRO192M, FRO12M, FRO16K and OSC32K.

SOSC is removed, but SCG should support clk_in from IO.

FRO192MHz should be trimmed to 144MHz by default to support 72MHz CPU clock.

SCG FIRCCFG.FREQ_SEL should be configured as below to support 144MHz:

- 010b, reset value, 48MHz FIRC clock is selected.
- 000b, 36MHz FIRC clock is selected.
- 100b, 72MHz FIRC clock is selected.
- 110b, 144MHz FIRC clock is selected.

C1SU:

The chip implements FRO192M and FRO16K.

SOSC is removed, but SCG should support clk_in from IO.

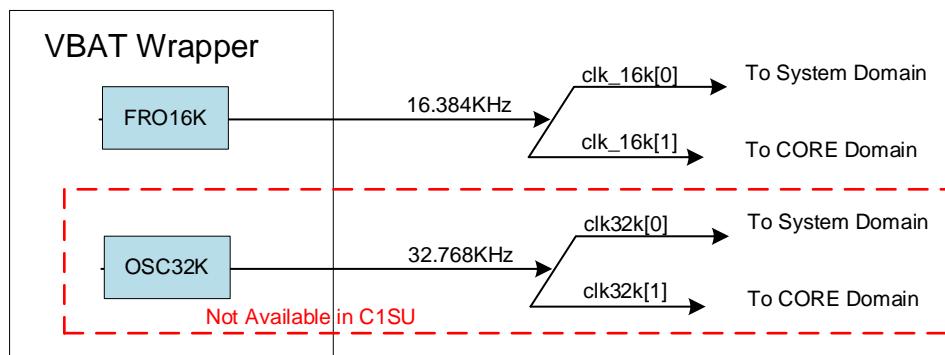
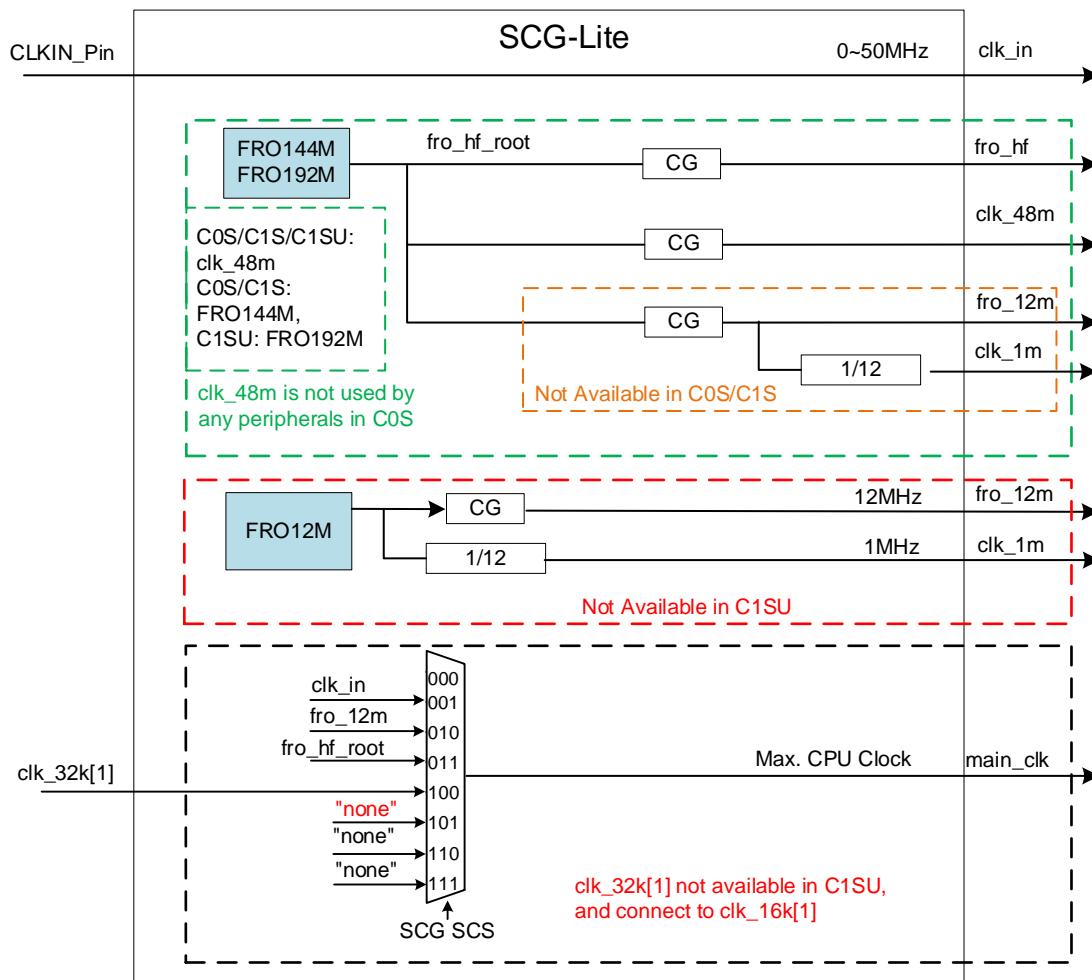
FRO192MHz should be trimmed to 192MHz by default to support 96MHz CPU clock.

SCG FIRCCFG.FREQ_SEL should be configured as below to support 192MHz:

- 001b, reset value, **48MHz FIRC clock is selected.**
- 011b, 64MHz FIRC clock is selected.
- 101b, 96MHz FIRC clock is selected.
- 111b, 192MHz FIRC clock is selected.

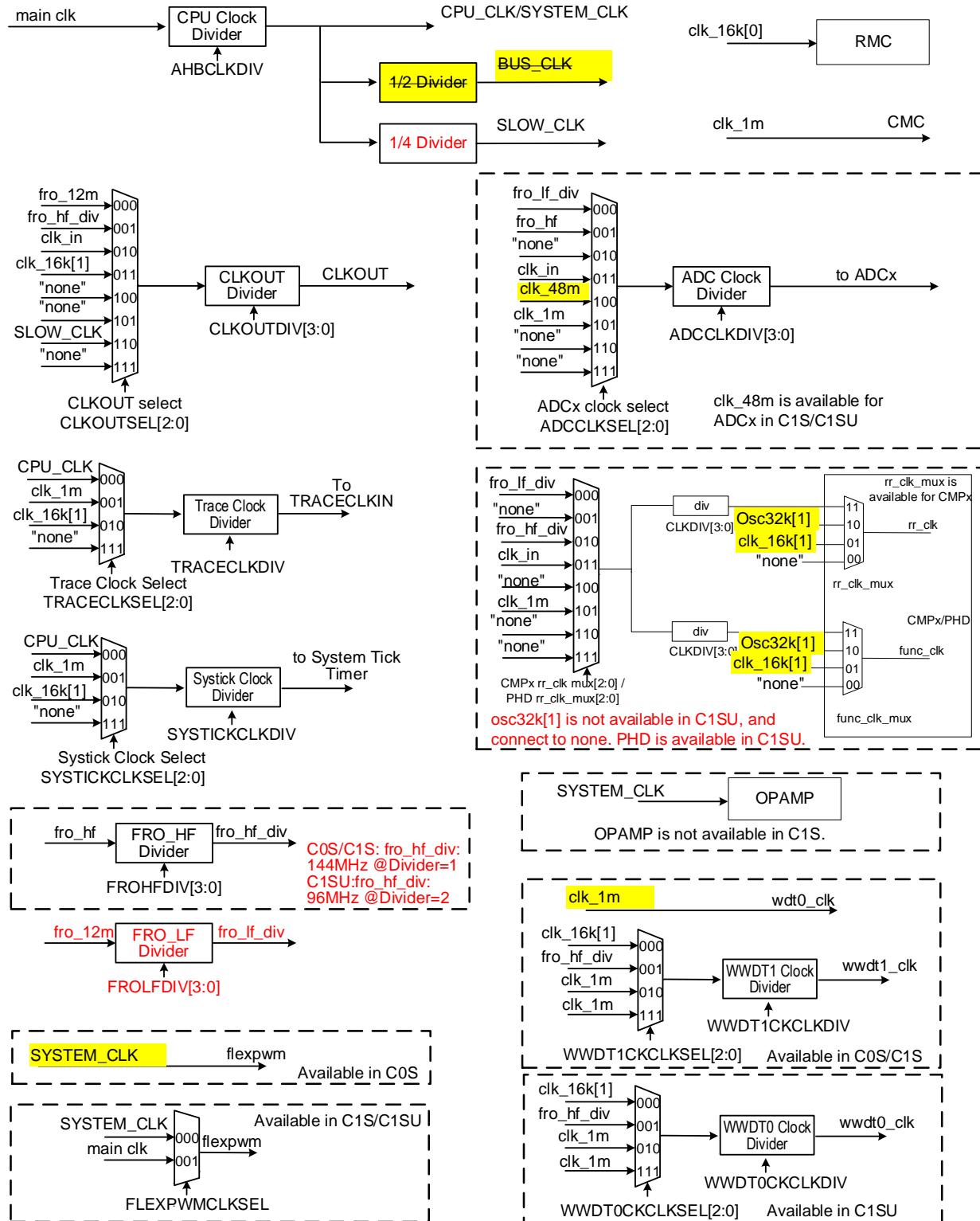
1.12.2. Clock Diagram

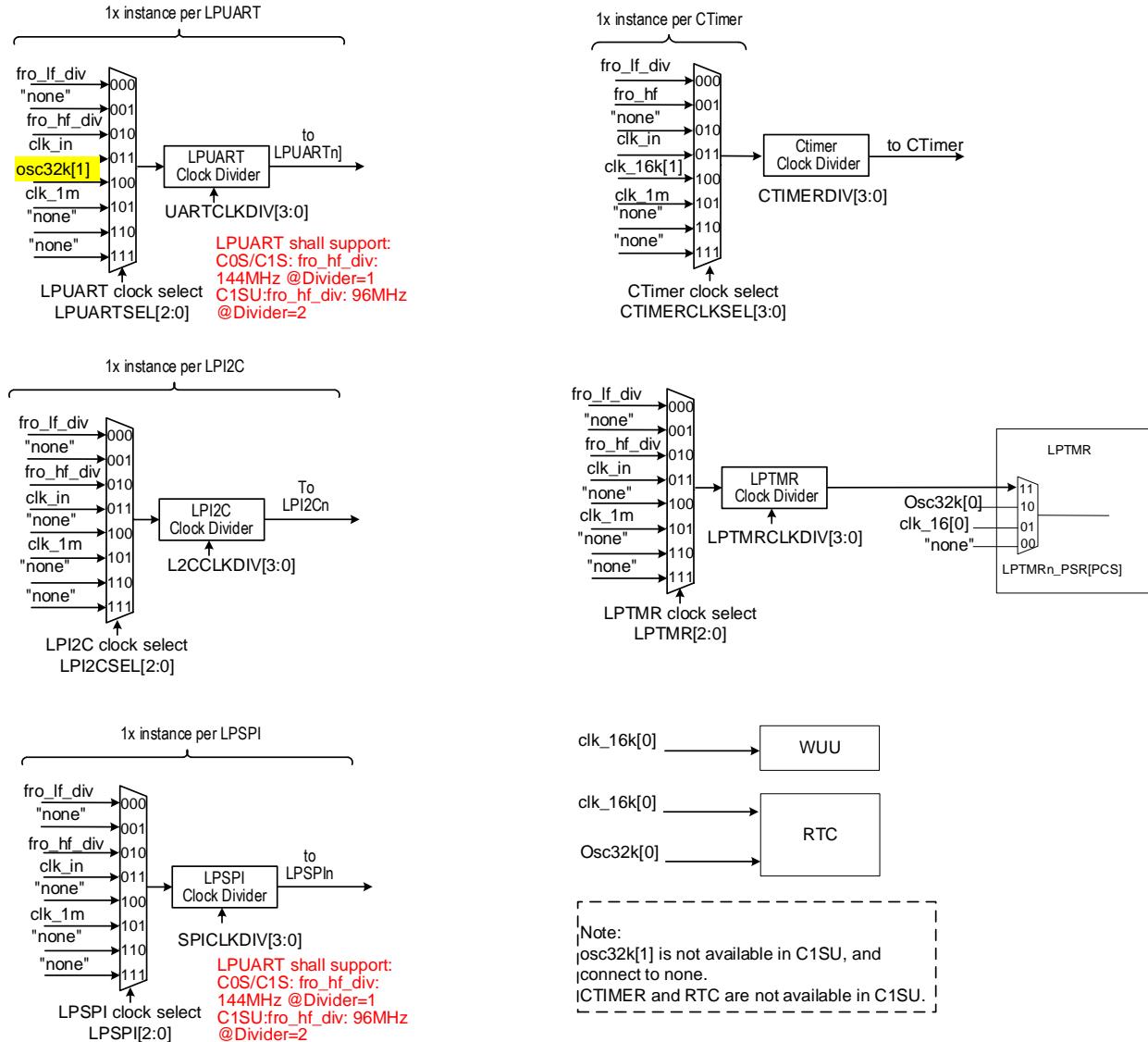
System Clock Sources

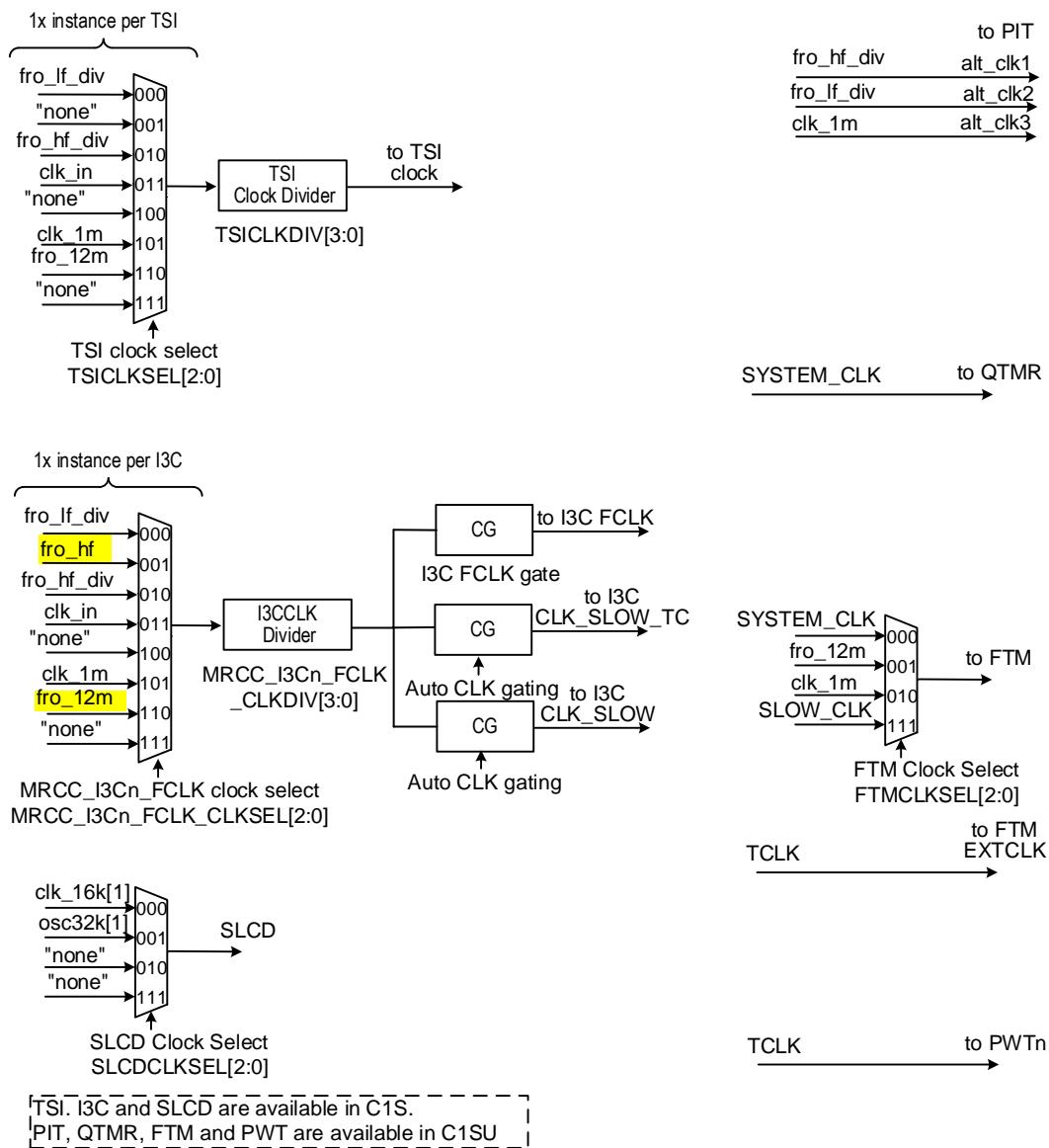


Text marked is internal information.

CLK_GEN

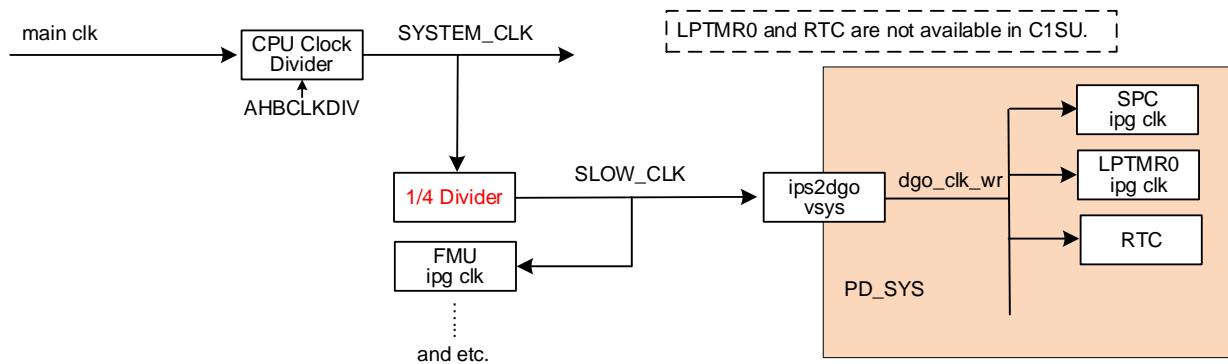






DGO Domain ipg_clk connection (to be updated)

Generally speaking, all peripherals' bus clock in System Domain should be clocked through the ips2dgo wrapper.



1.12.3. Clock definitions

Clock Name	Description	C0S	C1S	C1SU
clk_16[0]	It is the 16.384KHz clock output from FRO16K. It is the clock of peripherals in System domain.	Y	Y	Y
clk_16[1]	It is the 16.384KHz clock output from FRO16K. It is the clock of by peripherals in core domain.	Y	Y	Y
osc32k [0]	It is the 32.768KHz clock output from OSC32K. It is the clock of peripherals in System domain.	Y	Y	-
osc32k[1]	It is the 32.768KHz clock output from OSC32K. It is the clock of by peripherals in core domain.	Y	Y	-
clk_in	It is external input from IO.	Y	Y	Y
fro_hf	It is the clock output from FRO192M. The frequency is controlled by SCG-Lite FIRC RANGE register. (If FRO is trimmed to 160MHz by default, it will be FRO160M)	Y	Y	Y
fro_hf_div	It is the clock divided by fro_hf	Y	Y	Y
clk_48M	It is the clock derived from FRO192M	-	Y	Y
fro_12m	It is the 12MHz clock output from FRO12M	Y	Y	Y
fro_if_div	It is clock derived from fro_12m	Y	Y	Y
clk_1M	It is the 1MHz clock generated from FRO12M	Y	Y	Y
main_clk	It is main clock used by the CPU, AHB bus, APB bus, IPS bus, and some peripherals.	Y	Y	Y
CPU_CLK	It is the clock of CPU.	Y	Y	Y
SYSTEM_CLK	It is the clock of AHB bus, APB bus, IPS bus. The frequency is same with CPU_CLK	Y	Y	Y
BUS_CLK	It is the SYSTEM_CLK divided by 2. Most peripherals' APB and IPS bus is clocked by BUS_CLK	-	-	-
SLOW_CLK	It is the SYSTEM_CLK divided by 4	Y	Y	Y

1.12.4. Clocks summary

PLL is removed in A20-256

Clock Name	C0S/C1S	C1SU
	Max. Clock Frequency Run mode	Max. Clock Frequency Run mode
	SD Mode VDD_CORE = 1.1V typ.	OD Mode VDD_CORE = 1.2V typ.
clk_16[0]/clk_16[1]	16.384KHz	16.384KHz
osc32k[0]/osc32k[1]	32.768KHz	-
clk_in	50MHz	50MHz
fro_hf	144MHz must have	192MHz must have
fro_hf_div	72MHz must have	96MHz must have
clk_48M	48MHz	48MHz
fro_12M	12MHz	12MHz @generated by FRO192M
fro_lf_div	12MHz	12MHz
clk_1m	1MHz	1MHz
main_clk	160MHz must have, 192MHz nice to have	192 must have
CPU_CLK	72MHz must have	96MHz must have
SYSTEM_CLK	72MHz must have	96MHz must have
BUS_CLK	48MHz	48MHz
SLOW_CLK	24MHz must have	24MHz must have

fro_12M default trim value should make untrimmed fro_12M output frequency below 12MHz.

1.12.5. Peripheral Clock Summary

SD mode is available in C0S/C1S. OD mode is available in C1SU.

Modules	Bus Cock Source and frequency	Max Functional Clock	Max Functional IO Clock	Notes
CPU & System Modules				
CM23	SD/OD: 72MHz/96MHz		-	.
CPU_CLK/SYSTEM_CLK	SD/OD: 72MHz/96MHz		-	
BUS_CLK	SD:1/2 SYSTEM_CLK	-	-	-
SLOW_CLK	SD/OD: 1/4 SYSTEM_CLK		-	
DMA0	SYSTEM_CLK		-	hclk, ipg_clk
CRC	SYSTEM_CLK			
AHB Matrix	SYSTEM_CLK		-	
APB Bridge	SYSTEM_CLK		-	
AIPS Bridge	SYSTEM_CLK		-	
All System Masters' AHB bus	SYSTEM_CLK		-	
SYSTICK CLK		SD/OD: 24MHz		It is the output from SYSTICK CLK mux in clk_gen
SYSCON	SYSTEM_CLK			
SCG	SLOW_CLK			

SPC	SLOW_CLK			
WWDT0	SYSTEM_CLK	SD: 1MHZ	-	
WWDT1	SYSTEM_CLK	SD: 24MHz		
CMC	SLOW_CLK			ipg_clk_s, cmc_clk, core_clk, lpo_1k_clk
RMC	SLOW_CLK			ipg_clk_lv, lpo_1k_lv
Peripheral Input Mux	SYSTEM_CLK			
TRNG	SLOW_CLK	FRO12M		Should implement the async gasket for TRNG

Debug				
Modules	Bus Cock Source and frequency	Max Functional Clock	Max Functional IO Clock	Notes
Jtag/SWD CLK			SD/OD: 24MHz	
TRACKCLKIN			SD/OD: 24MHz	

Memory Modules				
Modules	Bus Cock Source and frequency	Max Functional Clock	Max Functional IO Clock	Notes
SRAM	SYSTEM_CLK			

EIM	SYSTEM_CLK			
ERM	SYSTEM_CLK		-	
FMC Controller	SYSTEM_CLK		-	One clock
FMU APB Interface	SLOW_CLK			soc_apb_clk
FMU AHB Interface	SYSTEM_CLK			soc_ahb_clk, soc_fixed_clk

Communication Modules				
Modules	Bus Cock Source and frequency	Max Functional Clock	Max Functional IO Clock	Notes
LPUART0~4	SYSTEM_CLK	SD: 144MHz OD: 96MHz	SD: 24M bps	ipg_clk,lpuart_clk,ipt_clk
LPSPI0~1	SYSTEM_CLK	SD: 144MHz OD: 96MHz	(Reference Package and IO chapter)	ipg_clk,lpspi_clk,ipt_clk
LPI2C0~2	SYSTEM_CLK	SD: 72MHz OD: 96MHz	3.4 Mbps	ipg_clk,ipi2c_clk,ipt_clk
I3C	SYSTEM_CLK	SD: 144MHz	25MHz	

Timer Modules				
Modules	Bus Cock Source and frequency	Max Functional Clock	Max Functional IO Clock	Notes
LPTMRx	SLOW_CLK	24MHz	-	ipg_clk_irclk, ipg_clk_1khz, ipg_clk_32khz,

				ipg_clk_erclk, ipt_clk
Ctimer 0/1	SYSTEM_CLK	SD: 72MHz/144MHz		pclk, ctclk
FREQME	SYSTEM_CLK	SD: 72MHz OD: 96MHz		Pclk
RTC	SLOW_CLK	32.768KHz		
FlexPWM	SYSTEM_CLK	SD: 72MHz/144MHz OD: 192MHz		
eQDC	SYSTEM_CLK	OD: 96MHz		
PIT	SYSTEM_CLK	OD: 96MHz		
QTMR	SYSTEM_CLK	OD: 96MHz		
PWT	SYSTEM_CLK	OD: 96MHz		

HMI Modules				
Modules	Bus Cock Source and frequency	Max Functional Clock	Max Functional IO Clock	Notes
GPIO0~4	SYSTEM_CLK		-	hclk and ipt_clk
PORT0~4	SLOW_CLK		-	Only one clock, 22.5MHz follow A18

Analog Modules				
Modules	Bus Cock Source and frequency	Max Functional Clock	Max Functional IO Clock	Notes
ADC	SYSTEM_CLK	SD: 72MHz	-	Need to make sure the path from clk_in to ADC

		OD: 192MHz		functional clock input can achieve 64MHz . ipg_clk, adc_clk, ipt_se_gatedclk
CMP0~1	SLOW_CLK	24MHz in all mode	-	ipg_clk,func_clk,rr_clk,ipt_clk
PHD	SLOW_CLK	24MHz in all mode	-	ipg_clk,func_clk,ipt_clk
OPAMP	SLOW_CLK			
POR/VMON	SLOW_CLK		-	
PMC	SLOW_CLK	10MHz	-	ipg_clk_s, ipt_clk_1p8v
TSI	SYSTEM_CLK			
SLCD	SLOW_CLK			

MISC Modules				
Modules	Bus Cock Source and frequency	Max Functional Clock	Max Functional IO Clock	Notes
VBAT Wrapper	SLOW_CLK	32.768kHz		Pclk
WUU	SLOW_CLK	16.384KHz		ipg_clk_3v,pmc_clk_1khz_3v,ipt_clk_3v
CLKOUT		SD: 72MHz OD: 96MHz		

Test Modules				
Modules	Bus Cock Source and frequency	Max Functional Clock	Max Functional IO Clock	Notes

TCU	SLOW_CLK			
ATX	SLOW_CLK			

1.13. Debug

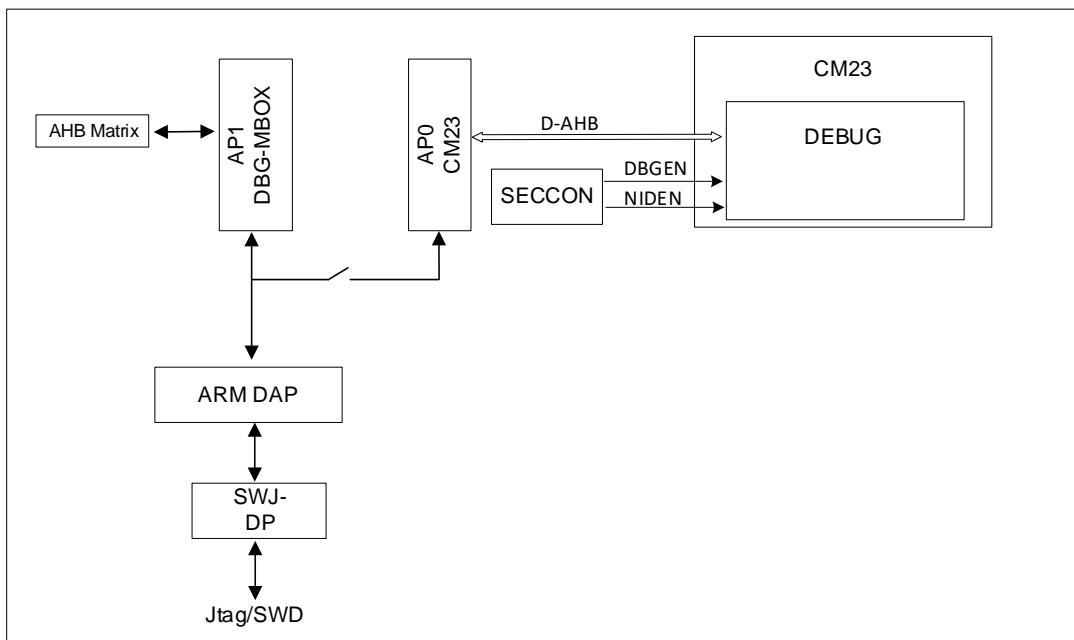
1.13.1. Introduction

The debug of this device is based on the ARM CoreSight™ architecture and is configured to provide the maximum flexibility as allowed by the restrictions of the pinout and other available resources.

It provides register and memory accessibility from the external debugger interface, basic run/halt control plus 2 breakpoints and 2 watchpoints.

Both Jtag and SWD debug interface is supported. By default, SWD interface is selected.

1.13.2. Debug Architecture



1.13.3. Debug/Trace Components

D-AHB interface

The 32-bit Debug AHB (D-AHB) interface implements the AMBA 5 AHB protocol. It can be used with a CoreSight AHB-AP to provide debugger access to all processor control and debug resources, and a view of memory that is consistent with that observed by load/store instructions acting on the processor.

AHB-AP debug access port

The AHB-AP is an optional debug access port into the processor system that provides access to all memory and registers in the system, including processor registers through the SCS. System access is independent of the processor status. SWJ-DP is used to access the AHB-AP.

ISP-AP

Debug Access port for Debug Mailbox, to allow the debugger to communicate with onboard ROM code. This port is always enabled.

Breakpoint Unit

The CM23 Breakpoint Unit (BPU) module comprises up to 2 instruction address comparators. It provides breakpoint functionality on all instructions fetched across the entire address range in which code can be located.

Watchpoint Unit (To be finish)

1.13.4. Test and debug port connectivity

JTAG/SWD/Trace signals summary

Pin Name	JTAG		SWD		Trace		Internal pull up/ down
	Type	Description	Type	Description	Type	Description	
TMS/SWDIO	I/O	Mode selection	I/O	Data	--		Pull-up
TCLK/SWCLK/TRACECLKIN	I	Clock	I	Clock	I	Clock	Pull-down
TDI	I	Data input	--		--		Pull-up
TDO	O	Data output	--		O	Data	N/A

SWDIO and SWCLK should be the default function of the pin.

TDI and TDO pin default status is disabled. If SWD interface is switched to JTAG, TDI/TDO function of the pin should be enabled automatically.

Boundary Scan is required. (internal use)

1.14. Boot

Boot Flow

After POR and warm reset, CPU controls the boot process. When reset is released, CPU has its reset vector at either 0x0001_0000 or 0x0100_0000 depending on phantom. Reset vector address should be selected by IFR1 SOCTRIM configuration.

0101b: CM23 reset vector is 0x0100_0000.

All other value: CM23 reset vector is 0001_0000.

Default: 1010b

C0S: For normal 64KB and 32KB phantom, NXP Bootloader is implemented in IFR0 and the 48KB starting from 0x0001_0000. The chip should boot from 0x0001_0000.

C0S/C1SU: For 128KB phantom, NXP Bootloader is implemented in IFR0 sector0. The chip should boot from 0x0100_0000.

C1S: For 128KB/256KB phantom, NXP Bootloader is implemented in ROM. The chip should boot from ROM.

In the end of NXP boot flow, the control of CPU will be transferred to user image in main flash starting from 0x0000_0004.

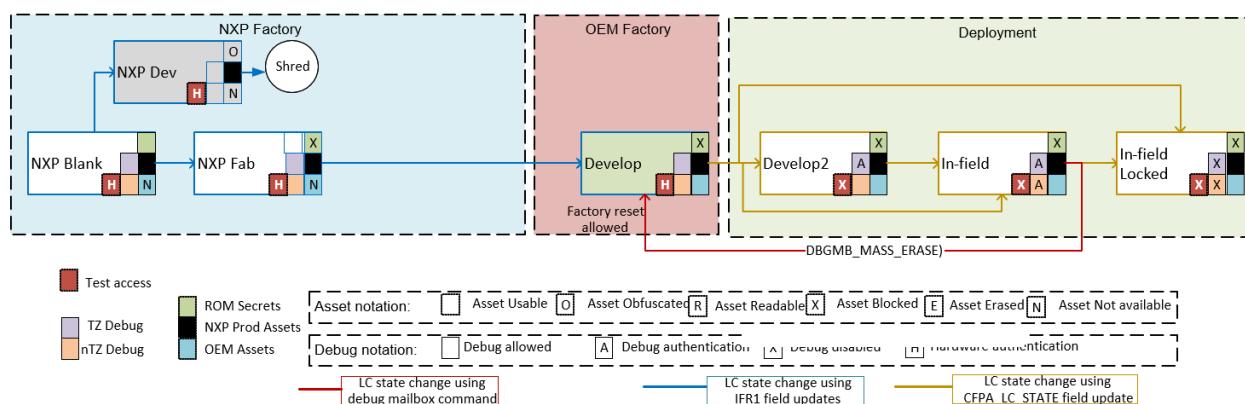
After POR and warm reset, the chip will boot from SD mode, and default boot speed is 48MHz (or 40MHz, if can't achieve 96MH).

Life Cycle

Hardware Life cycle decoding definition reuses A2TS.

Life Cycle Transition

Because MCX C0S security A2TS is much simpler than A2TS, can't support A2TS life cycle transition scheme. Below is the proposed LC transition.



NXP_FA and OEM_RETURN states are supported by OEM_DEV state. The chip can go back to OEM_DEV from In-Field states by DBGMB_MASS_ERASE command. NXP Bootloader may implement password based authentication for DBGMB_MASS_ERASE comment, but it is exceed the scope of HW AS.

OEM_DEV state is equivalent ROP0 state. NXP bootloader will enable debug port.

Develop2 state is equivalent ROP1 state. NXP bootloader will not enable debug port, but user code can enable debug port.

In-field state is equivalent ROP2 state. NXP bootloader will not enable debug port and lock debug port.

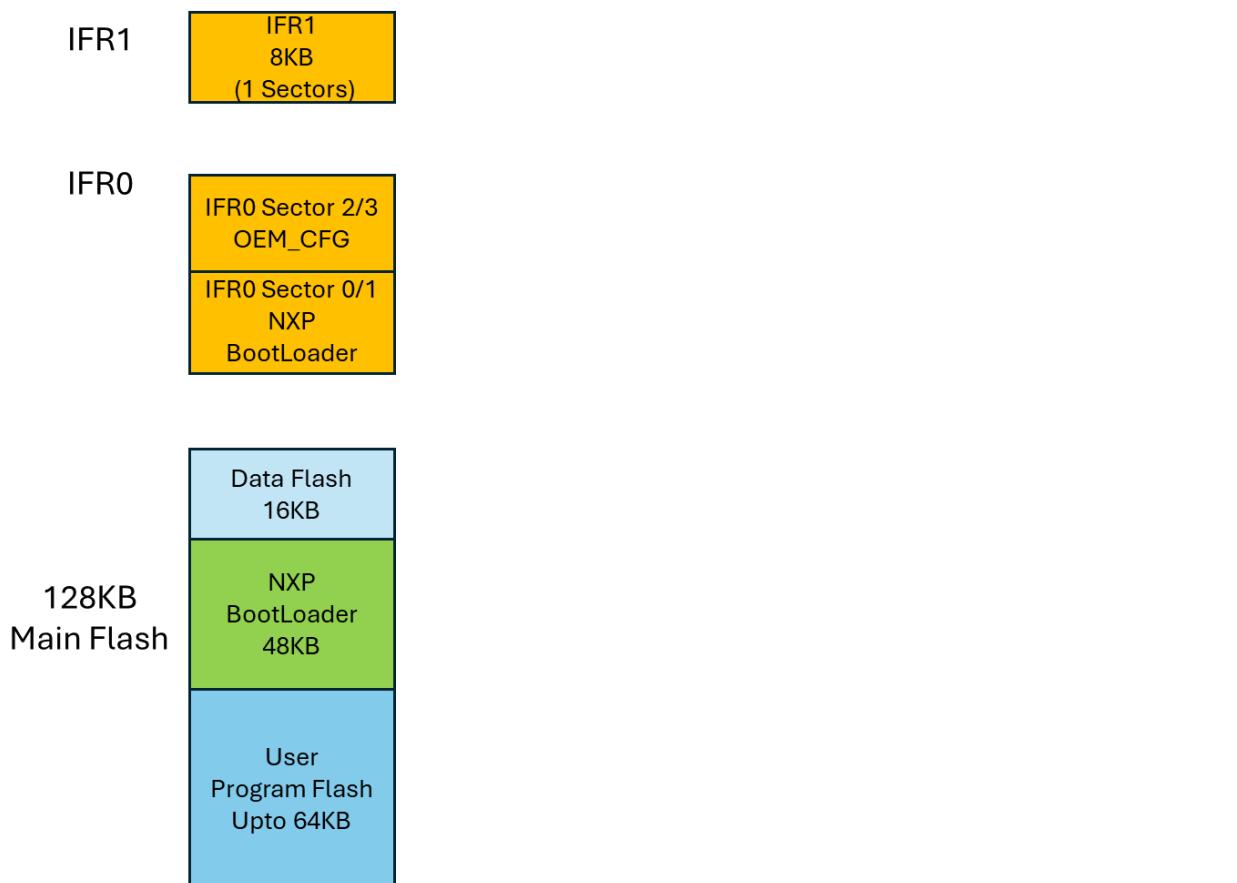
Bootloader can simplify the State from SW point of view, but HW decoding logic will not be changed.

Test Entry Control

Test entry control is based on life cycle, and the rule is same with A2TS.

To support the re-phantom of the chip, must keep the options to reprogram IFR1 in OEM_DEV state. The option can be controlled by IFR1 SOCTRIM. ([Confirming with TE/PE whether it is mandatory.](#))

C0S Flash Layout



IFR1 usage is same with A20-256.

IFR0 Sector0/1 is allocated for NXP Bootloader. And when CM23 reset vector is point to base address of IFR0.

IFR0 Sector2/3 is allocated for OEM_CFG for user to configure the boot options.

Main Flash lower 64KB is allocated to user as program flash. For 32KB phantom, the lower 32KB is allocated to user program flash.

The top 16KB in main flash is also open to customer. Customer can use it as data flash.

The flash between the Data Flash and Program Flash are also allocated for NXP Bootloader. So, total 64KB flash can be used to implement Bootloader.

For 64KB and 32KB phantom, Bootloader boot from address 0x0001_0000. When AHB bus access the 48KB space starting from 0x0001_0000, access type should be fixed to data access type. (Will be updated based on CCB MCXC0S-2)

Flash Access Permission Control

Out of reset, Read/Write/Execute permissions to flash are enabled in MBC. To support deny by default, SOC shall implement a wrapper, which only enable the Execute permission of IFR0 sector 0/1. NXP bootloader should disable the write permission of Program Flash, Data Flash and IFR0 Sector2/3 in MBC, then disable the SOC level X permission control. In the end of boot flow, Bootloader should enable Program Flash X permission.

Before Bootloader jump to user application, must properly hide the access of Bootloader region and disable write permission. IFR0 MBC granularity is 2KB. If Bootloader needs to open any information to user, the data/code should be place to IFR0 region.

Before Bootloader jump to user application, bootloader shall disable flash mass erase operation by MSF Configuration Register MASS_ERASE_DIS bit. ROM_LOCK register can also disable mass erase operation, although ROM is not implemented. The redundancy is helpful to security.

IFR0 sector2/3 write permission should be properly handled based on ROP level.

Flash Phantom should be controlled by Bootloader. In 32KB flash phantom, Bootloader shall disable the access of main flash sector 4~7 by MBC.

Test in OEM_DEV/NXP_FA states

It needs to support test function in OEM_DEV/NXP_FA states. If Bootloader detect a test request in the beginning of boot flow, bootloader shall hide the access of flash from AHB bus by MBC, then copy CFPA_LC_STATE from IFR0 to SECCON and stop at while(1) loop. The code to do it can be allocated in IFR0 Sector0/1, because IFR0 MBC granularity is 2KB.

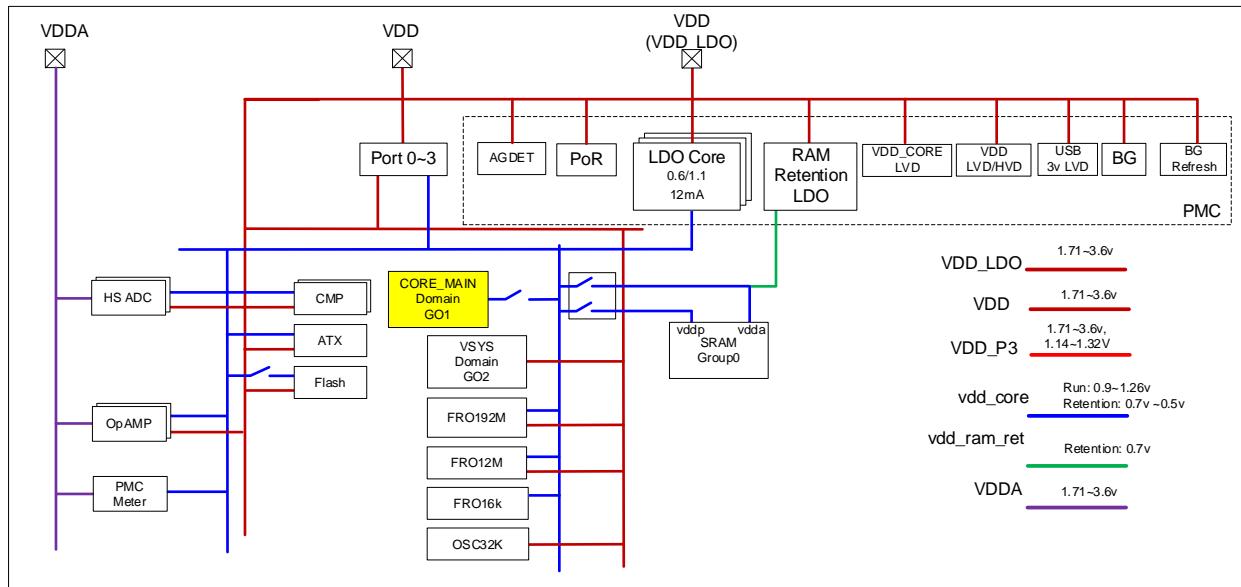
Please note when chip test mode and FMU test interface is enabled, the data in flash can be read through FMU test interface. This is the known risk.

1.15. Reset

Reset architecture is same with A20-256. TDET and CDOG reset are not available.

1.16. Power

1.16.1. Power Architecture Block Diagram



C0S/C1S: RAM_RET_LDO.

Switch0: RAM A0/A1/A2(A2 for C1S only)

C1SU: Not required.

1.16.1.1. Voltage monitors

Same with A20-256.

1.16.1.2. PMC Reference

Same with A20-256.

1.16.1.3. Power Domain

Power Domain (Digit)	Description
VDD_CORE_MAIN	Std. Cell type is GO1.
VSYS	Std. Cell type is GO2

1.16.2. Core Mode Controller (CMC)

1.16.2.1. Low Power Interface

Same with A20-256

1.16.2.2. Dynamic Q-Channel Clock Gating

Same with A20-256.

1.16.2.3. Power Mode

	CMC LPMOD	CORE_LDO Output Level	RAM Retention LDO	CORE_MAIN Domain	VSYS Domain	Flash	RAM
Standard Drive (SD)	-	1.1V +- 10%	0.7V	Up to 96MHz	Up to 24 MHz	On/Std. by/Sleep	On
Sleep	4'b0000	1.1V +-10% Or LP mode	0.7V	CPU sleep, clock gated	Up to 24MHz	On/Std. by/Sleep	On
Deep Sleep (was DS0 in A1x)	4'b0001	1.1V +- 10% or LP mode	0.7V	CPU_CLK/YSTEM_CLK /SLOW_CLK are clock gated Async Operation	Up to 24MHz	Std by/ Sleep/	Retention
Power Down	4'b0011	0.5~0.7V LP mode	0.7V	Static	Up to 32.768KHz	PD	Retention or Off
Deep Power Down	4'b1111	Off	Optional ON	Off	Up to 32.768KHz	Off	Optional Retention

1.16.3. Peripheral Power Domain Assignments

Peripherals in VSYS domain:

- RMC
- SPC
- VBAT Wrapper
- WUU
- LPTMR0
- RTC

Other peripherals are in CORE domain.

1.16.4. Module operation in low power modes

Module	Sleep	Deep Sleep	Power Down	Deep Power Down	NON_C UST
Core Modules					
Multi-Layer AHB Matrix	On ¹	Static ²	Static	Off ³	
CM23	Static	Static	Static	Off	
System Modules					
CRC	On	Static	Static	Off	
CMC	On	On	Static	Off	
eDMA3	On	LP ⁴ /Static	Static	Off	
EIM	On	Static	Static	Off	
ERM	On	Static	Static	Off	
MBC	On	Static	Static	Off	
Peripheral Input Mux	On	On/Static	Static	Off	
RMC	On	On	On	On	
SCG-Lite	On	On/Static	Static	Off	
SPC	On	On	On	On	
SYSCON	On	On/Static	Static	Off	
WUU	On	On	On	On	
VBAT Wrapper	On	On	On	On	
FRO192M	On/Off	On/Off	Off	Off	
FRO12M	On	On/Off	On/Off	Off	
FRO16K	On/Off	On/Off	On/Off	On/Off	
OSC32K	On/Off	On/Off	On/Off	On/Off	
PMC Sub Module					
BG	On	On/Off	Off	Off	
LDO_CORE	On	LP/Off	LP	Off	
PoR	On	On	On	On	
RAM_Retention_LDO	On/Off	On/Off	On/Off	On/Off	
VDD_LVD/HVD	On/Off	On	Off	Off	
VDD_LV_LVD	On/Off	On	Off	Off	
Flash Array	On	Static	Off	Off	
FMC	On	Static	Static	Off	
FMU	On	Static	Static	Off	
SRAM	On	Retention	Retention/ OFF	Retention/OFF	
Timers					

CTimer0~1	On	Static/LP	Static	Off	
FME	On	Static/LP	Static	Off	
LPTMR	On	Static/LP	Static/ LP	Static/LP	
WWDT0	On	Static/LP	Static	Static/LP	
WWDT1	On	Static/LP	Static	Off	
QTMR	On	Static/LP	Static	Off	
PIT	On	Static/LP	Static	Off	
PWT	On	Static/LP	Static	Off	
Communication					
LPI2C0~2	On	Static/LP	Static	Off	
LPSSPI0~1	On	Static/LP	Static	Off	
LPUART1~4	On	Static/LP	Static	Off	
LPUART0	On	Static/LP	Static	Off	
Analog					
16bit ADC Digital	On	Static/LP	Static	Off	
16bit ADC Analog	On/Off	On/Off	Off	Off	
CMP0~1 Digital	On	Static/LP	Static	OFF	
CMP0~1 Analog	On/Off	On/Off	On/Off	On/Off	
PHD Digital	On	Static/LP	Static	OFF	
PHD Analog	On/Off	On/Off	On/Off	On/Off	
OPAMP Digital	On	Static/LP	Static	OFF	
OPAMP Analog	On/Off	On/Off	On/Off	On/Off	
TSI Digital	On	Static/LP	Static	OFF	
TSI Analog	On/Off	On/Off	On/Off	On/Off	
SLCD Digital	On	Static/LP	Static	OFF	
SLCD Analog	On/Off	On/Off	On/Off	On/Off	
HMI					
GPIO1~4	On	Static/LP	Static	Off	
GPIO0	On	Static/LP	Static	Off	
PORT1~4	On	Static	Static	Off	
P1~3 Pin Output	On	On	Static	Static	
PORT0	On	Static	Static	Off/LP	
P0 Pin Output	On	On	Static	Static	
Debug and Test					
JTAG and SWD	On	Static	Static	Off	
SWO	On	Static	Static	Off	
TCU	On	Static	Static	Off	
ATX Digital	On	Static	Static	Off	NON_CUST

ATX Analog	On/Off	On/Off	Off	Off	NON_CUST
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1. On means module is functional and accessible via memory map. For analog module, means it is enabled.
2. Static means the module is not active in state retention status.
3. Off means the module can be powered off.
4. LP means that the module is in low power state (clock gated, asynchronous operation, etc). For digital module, it can be active with async functional clock.

NON_CUST means the line should be hidden in RM.

1.16.5. Wake Up Source

Same with A20.

1.16.6. Power mode transitions

Same with A20

1.16.7. Power Sequence

Same with A20

1.16.8. Power Estimation

To be provided

1.17. Phantom

C0S RAM phantom options

	12KB	6KB	
SRAM Address	0x0400_0000~0x0400_2FFF 0x2000_0000~0x2000_2FFF	0x0400_0000~0x0400_17FF 0x2000_0000~0x2000_17FF	

Flash should support 64KB and 32KB phantom. It is realized by NXP Bootloader.

Peripheral Phantom control logic should be same with A20-256.

C1S/C1SU not required RAM phantom.

1.17.1. Package

C0S:

Shall be pin compatible with A10.

Shall support TSSOP20, QFN16/24/32/48, LQFP48 and WLCSP.

Leading package is LQFP48, QFN48/32

The second release packages shall be supported via CCB.

Packages to be supported ***initially***:

- QFN16: 3x3x0.65, P 0.5mm
- TSSOP20: 6.5x4.4x1.1, P 0.65mm
- QFN24: 4x4x0.65, P 0.5mm
- QFN32: 5x5x0.9, P 0.5mm
- QFN48: 7x7x0.9, P 0.5mm
- LQFP48, 7x7x1.4, P 0.5mm

C1S:

Shall be pin compatible with A10.

Shall support QFN32, QFN48, LQFP48, LQFP64, **LQFP80**, **BGA64** and **WLCSP**.

Packages to be supported ***initially***:

- QFN32: 5x5x0.9, P 0.5mm
- QFN48: 7x7x0.9, P 0.5mm
- LQFP48, 7x7x1.4, P 0.5mm
- LQFP64, 10x10x1.4, P 0.5mm
- LQFP80, 12x12x1.4, P 0.5mm
- BGA64: 5x5x1.2, P 0.5mm
- WLCSP

C1SU:

Shall be pin compatible with A10.

Shall support **QFN28 with pre-driver**, **QFN32 with pre-driver**, **QFN48 with pre-driver** and **LQFP48 without pre-driver**.

Packages to be supported *initially*:

- QFN32: 4x4x0.9, P 0.4mm w/ pre-driver
- QFN48: 7x7x0.9, P 0.5mm w/ pre-driver
- LQFP48, 7x7x1.4, P 0.5mm w/o pre-driver

1.17.2. IO General

5V TOL IO is not required.

C0S/C1SU: 4 HD IOs are required.

C1S: 8 HD IOs are required.

1.17.3. I/O performance

Same requirement with A10

1.17.4. PinOut Table

[MCXC0S_Pinout.xlsx.url](#)

[MCXC1SU_Pinout.xlsx.url](#)

[MCXC1S_Pinout.xlsx.url](#)

1.18. Architecture Level Use Case

Please reference FRS.