

RT2660

Hardware Architecture Specification

Rev. 0.91 — 1 Sep 2024

HW.AS

Table 1. Document information

Info	Content
Author	Benjamin Qian
Author Role	SoC architect
Keywords	
Abstract	

Table 2. Revision history

Revision	Date	Description	Author
0.1	20 Nov 2023	Initial version	Maurice Meijer
0.2	6 Feb 2024	Initial SoC HW.AS version for PCA baseline Updated functionality to align to PRD 0.7 and RS 0.4 Updated architecture definition versus revision 0.1	Maurice Meijer
0.3	12-Feb-2024	New initial SoC HW.AS version for PCA baseline Updated functionality to align to PRD 1.1 and RS 0.5 Updated clock section	Maurice Meijer
0.4	26-Feb-2024	initial SoC HW.AS update Updated architecture definition versus revision 0.3 Added initial pinmux, interrupt table & DMA channels Added debug infrastructure description	Maurice Meijer
0.5	12-March-2024	initial SoC HW.AS update Updated architecture definition versus revision 0.4 Updated memory map, PMU, VBAT_SS, ZV wrapper, boot flow, clock section, pad section, pinmux Added initial analog block specs, sleepcon, powercon, use-case information	Maurice Meijer
0.6	2-April-2024	initial SoC HW.AS update Updated architecture definition versus revision 0.5 Updated clock section, control infrastructure section, power architecture, security chapter Added initial pinlist, cross-trigger network, OTP function	Maurice Meijer
0.7	23-April-2024	Initial SoC HW.AS update Updated architecture definition versus revision 0.6 Moved to NXP EFSPRAM compiler Updated DAC, ACMP, memory map, DMA channels, clock section, pad section, pinmux, cross-trigger network, power architecture, system boot section	Maurice Meijer
0.8	4-July-2024	Initial SoC HW.AS update Updated architecture definition versus revision 0.7, links to machine readable tables added SoC HW.AS 0.7 review comments addressed, and architectural compromises done as per BL guidance Last-Level Cache, Xeno Phy, DMAC added	Maurice Meijer

1. Document Purpose

This document describes the hardware architecture specification of the i.MX RT2660 SoC.

This revision of the SoC HW AS is related to the i.MX RT2660 Product Requirement Document Rev 1.1 [1], and the i.MX RT2660 Product Requirement Specification Rev 0.78 [2].

From the described architecture, requirements for sub-systems can be derived. This document also serves as a design guide to the i.MX RT2660 design teams. Additional documentation is provided in the form of hardware architecture specification of the i.MX RT2660 SoC subsystems. These documents provide a more detailed description of the subsystems as compared to the i.MX RT2660 SoC HW.AS document. Refer to table below.

Table 3. **i.MX RT2660 SoC subsystem & -functions HW.AS documents**

Name	DRI	Group	Reference
Subsystem HW.AS documents			
CMPT_SS	Maurice Meijer/Steven Millburn	MME Architecture	[3]
MAIN_SS	Martin Mienkema	MME Architecture	[4]
MEDIA_SS	Benjamin Qian	MME Architecture	[5]
AUDIO_SS	Naveen Raina	MME Architecture	[6]
COMM_SS	Benjamin Qian	MME Architecture	[7]
WAKE_SS	Martin Mienkema	MME Architecture	[8]
PMC_SS	Marianne Maleyran	BL SCE WCS Analog	[9]
Function HW.AS documents			
Control infrastructure	Simon Gallimore	MME Architecture	[10]
Power architecture	Anand Savanth	MME Architecture	See Chapter 8
Security architecture	Nipun Mahajan	CTO Security	[11]
DFT architecture	Tiger Sun	MME	[12]

Disclaimers

The current version of the document concerns is close to a PDA candidate release, however there are several blocking items that prevent this as PDA candidate release. These blocking items are clearly indicated in the related sections; actions owners are in place to provide a resolution to these blocking items but so far this is still work in progress. Moreover, several CRs that impact PRD Rev 1.1 are being formulated that require further update of the SoC HW.AS document prior to PDA milestone. These CRs are still work in progress.

Aside from upcoming CRs, note that there are also RS updates ongoing independent from these CRs. Since the RS updates have not been finalized yet, they have not accounted for in the current this document. It has been indicated with "*Open: Req. update ongoing*" in the requirements traceability table where an RS update is envisioned.

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2. Key Data

Table 4. Key data table

Process	GF 22FDXP, 10M_2Mx_5Cx_1Jx_2Qx_LB
Die size (incl seal, excl saw lane)	16.5mm ² estimated. Die area range with uncertainty margin: 15.7-17.3 mm ² To be updated.
Complexity	Digital logic ~4.7 mm ² (6.75T HD logic library) Memories ~4.5 mm ² (includes 1.5MByte SRAM in total for user application) Analog ~3.1 mm ² (analog includes on-chip PMU) PHY ~0.9 mm ² (hard macros excluding digital) Up to 354 pads (all assumed to be staggered)
Mission profile(s)	Automotive Grade2, Industrial, Consumer
Package	BGA289, 14mmx14mm, 0.8mm pitch BGA196, 10mmx10mm, 0.65mm pitch BGA196, 12mmx12mm, 0.8mm pitch BGA169, 9mmx9mm, 0.65mm pitch A SiP package with serial NOR flash to be determined
Bonding	Copper wire, 20µm wire diameter
Thermal aspects	Ambient temperature range : -40°C ... +105°C; Junction temperature range : -40°C ... +125°C

Table 5. IC requirements traceability: Key Performance Indicator requirements

AS/RS identifier	Content	Classification	Covered
iMXRT2660_KPI_1-3	The Cortex-M85 core shall achieve at least 4,375 CoreMark. This is achievable with 1x Cortex-M85 at 700MHz (assuming 6.25CM/MHz). Note: According to ARM, 6.28CM/MHz. [13]	Must have	During design phase
iMXRT2660_KPI_1-4	The TensorFlow Lite benchmark application (MobileNetv1.0 224) on NPU scenario should achieve a performance of, at maximum, 16 ms, with N256S.	Must Have	During design phase
iMXRT2660_KPI_1-5	This MCU device shall support graphics processing up to 720p60, 24bpp and 1080p30, 24bpp.	Must have	Targeted
iMXRT2660_KPI_1-6	This MCU device shall support concurrent 720p camera and display and ML for face identification as described in the Building Control use case.	Must have	Yes as per specified UC
iMXRT2660_KPI_1-7	This MCU device shall achieve 550MBps effective DRAM bandwidth when up to 5 bus initiators concurrently performing Reads and Writes transactions to the external pSRAM device.	Must have	No, only up to 380MBps may be achievable in multi-master scenarios
iMXRT2660_PWR_5-5	Usage scenario: Active 1 - CM85 executes CoreMark at 700MHz from TCMs - Digital core voltage is at normal drive level. - All bus clocks and peripheral clocks are at their max frequency, without any data activity - NPU clock is gated - Media, Audio and Comms subsystems are off Target	Must have	Yes, as per estimation w/ booting at 250MHz

AS/RS identifier	Content	Classification	Covered
iMXRT2660_PWR_5-16	<ul style="list-style-type: none"> - Power consumption: =< 250mW Usage scenario: Deep Sleep - CPU core in WFI - Core, system bus, and peripheral clocks gated - Recovery time: equal of less than 150us - All SRAM contents retained <p>Target</p> <ul style="list-style-type: none"> - Power consumption: =< 3.5mW 	Must have	Open: Req. update ongoing
iMXRT2660_KPI_1-10	This MCU device shall consume less than 500uW while performing voice detection in Deep Sleep mode.	Must have	Open: Req. update ongoing
iMXRT2660_KPI_1-11	The die area of this processor shall be less than 16mm ² .	Must have	No, as per estimation
iMXRT2660_KPI_1-12	This MCU device shall have at least 125 functional IO pins in BGA-196 package	Must have	Yes

3. Introduction

3.1 i.MX RT2660 overview

The i.MX RT2660 is the first product of the next-generation i.MX RT2K cross-over processor family, targeting implementation in Global Foundries' 22FDX+ process. It features NXP's first implementation of the ARM Cortex®-M85 core while operating at speeds up to 700MHz to provide high CPU performance and also best real-time response. It offers advanced Machine Learning (ML) inference capabilities through embedded hardware acceleration based on NXP's Neutron Neural Processing Unit (NPU) enabling up to 256 MACs/cycle. The i.MX RT2660 has total of 1.5MB on-chip SRAM, and offers EdgeLock 500B security certification.

Like other i.MX RT processors, the i.MX RT2660 contains a rich set of peripherals for audio & video applications. This includes MIPI 2-lane camera/display serial interfaces, parallel camera/display interfaces, basic 2.5D graphics core, SPDIF and I2S audio interfaces. Moreover, the i.MX RT2660 offers various external memory interfaces, including SDRAM, NOR/NAND SPI FLASH, SD/eMMC, and a wide range of other interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, microphones, displays, and camera sensors. Last but not least, it integrates advanced power management module with DCDC and LDO that reduces complexity of external power supply and simplifies power sequencing.

The i.MX RT2660 is targeting, but not limiting to, the following main applications:

- MCU processor in IOT applications including Smart Home, Smart Appliances, Generic Edge ML, Consumer Audio, and many others ;
- MCU processor in industrial applications including Machine Vision, Building Control and many others ;
- MCU processor in automotive applications without FuSa requirements.

3.2 Block diagram

i.MX RT2660

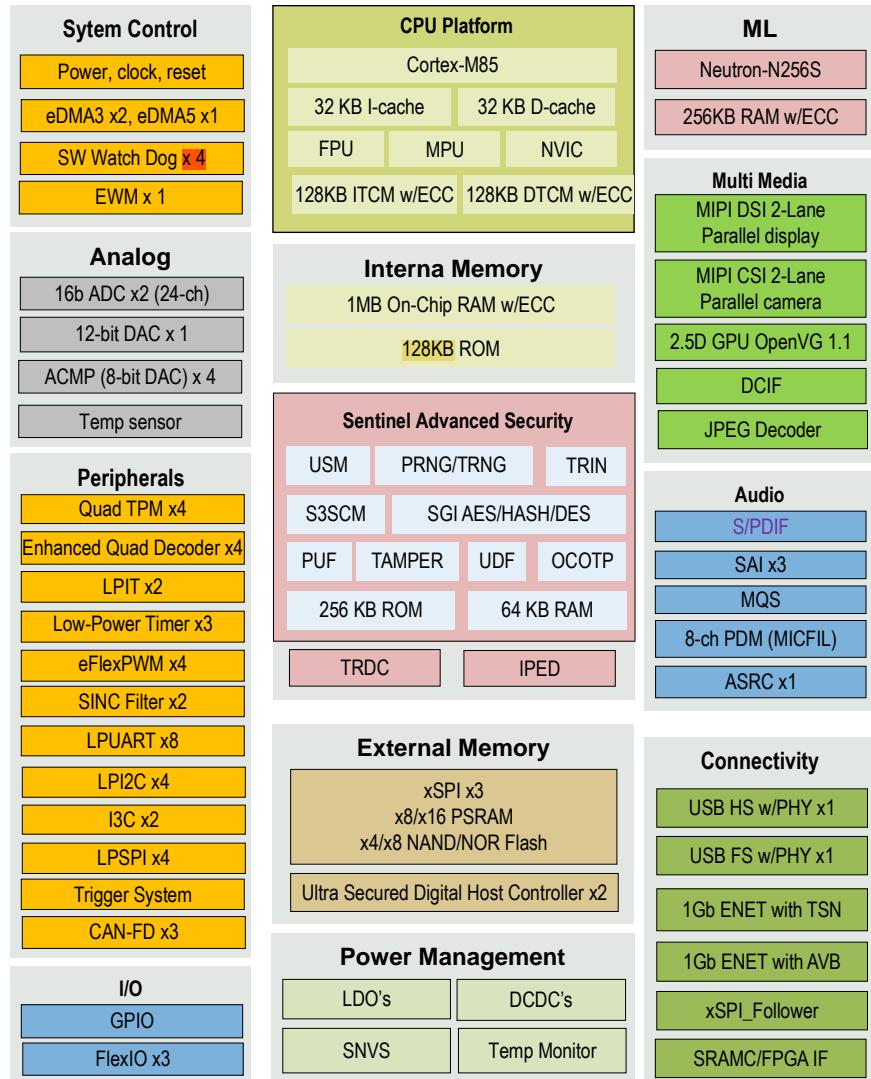


Fig 1. i.MX RT2660 feature diagram

3.3 Features

The i.MX RT2660 has the following key features:

- Cortex-M85 based microcontroller platform
 - Cortex-M85 processor
 - 32 KB L1 I-Cache and 32 KB L1 D-Cache, both ECC-protected ;
 - Memory Protection Unit (MPU), up to 16 individual protection regions ;
 - Full featured Floating Point Unit (FPU) ;
 - ARM Helium's M-Profile Vector Extension (MVE) ;

- TrustZone-M including Pointer Authentication and Branch Target Identification (PACBTI) Extension ;
- ARMv8.1-M Thumb instruction set ;
- Up to 256 KB TCM for instruction and data in total; ECC-protected ;
- Target maximum operating frequency of up to 700MHz in Normal Run mode ;
- CoreSight™ components integration for debug ;
- Neutron 256-S based Machine Learning (ML) inference platform
 - Neutron machine learning inference engine IP
 - Up to 256 MACs/cycle of ML inference performance ;
 - 8-/16-bit data and 8-/16-bit weights ;
 - DNN layers: CONV1D/2D, depth-wise CONV, LSTM, GRU, max pooling ;
 - Activation functions: None, ReLU, ReLUx, Sigmoid, Tanh ;
 - 256 KB TCM in total; ECC-protected ;
 - Target maximum operating frequency of up to 700MHz in Normal Run mode ;
- On-chip shared SRAM of 1.5 MB in total ;
- Boot ROM of 128 KB;
- DMA controller for peripheral-to-memory, memory-to-memory and memory-to-peripheral communications ;
- Security
 - Sentinel 110 (S110) IP supporting a wide range of cryptographic algorithms and providing strong key isolation from the rest of SoC
 - Compliance with Edgelock 500B and **ARM PSA L3** ;
 - Tamper detection monitoring tamper attacks on device power supply, processor- or secure module clock, chip temperature and up to 2 tamper pins ;
 - Secure boot support with ROM mechanism to support SHA-256, ECDSA p256/p384 and PQC authentication, and fully encrypted boot flow ;
- External memory interfaces
 - Three xSPI interfaces with on-the-fly encryption/decryption. One xSPI module targets SPI Flash memories, supporting eXecute In-Place (XIP), address-remapping to support dual-image boot, and garbage collection capabilities. DMA supported ;
 - Support for Octal/Quad/Dual/Single SPI Flash memories up to 200MHz operation ;
 - Support for x1, x2, x4, x8, x16 pSRAM (HyperRAM) memories with up to 250MHz operation ;
 - Two Ultra Secure Digital Host Controller (uSDHC) memory card interfaces with dedicated DMA controller ;
 - eMMC 5.1 compliance with HS400/DDR operation ;
 - SD/SDIO 3.0 compliance with 200MHz SDR signaling to support up to 100MB/sec ;
- Multimedia
 - Generic 2.5D Vector Graphics Processing Unit supporting common operations and multiple pixel formats (RGB, YUV444, YUV422, YUV420, YUV400) for displays ;

- MIPI Camera Serial Interface with on-chip PHY supporting 2 lanes ;
- Camera Parallel Interface supporting 8/16/24 bit inputs ;
- MIPI Display Serial Interface with on-chip PHY supporting 2 lanes ;
- Display Parallel Interface supporting up to 1080p resolution ;
- One JPEG decoder supporting baseline & extended ISO/IEC 10918-1 JPEG streams;
- Audio
 - Digital microphone (DMIC) interface supporting up to 8 microphone channels with associated decimators and Voice Activation Detect ;
 - One S/PDIF Input & Output, supporting 32-bit IEC60958 formatted data ;
 - Three SAI (synchronous audio interface) modules supporting I2S, AC97, TDM, and codec/DSP interfaces ;
 - **Two** MQS interfaces for medium quality audio via GPIO pads, with sigma-delta modulator output for low system-BoM cost stereo audio output ;
 - Asynchronous Sample Rate Conversion ;
- Connectivity
 - Two USB interfaces One USB 2.0 controller with integrated USB 2.0 (HS) PHY interface and another USB 1.1 controller with integrated USB 1.1 (FS) PHY interface ;
 - Two 1Gbps Ethernet controller interfaces with support for IEEE1588. One Ethernet interface supports Time-Sensitive Networking (TSN) ;
 - Three CAN-FD modules as per CAN2.0B specification and ISO11898-1 specification;
 - Two I3C Master/Slave modules supporting SDR mode and HDR-DDR mode as per MIPI Alliance I3C specification ;
 - Four I2C Master/Slave modules supporting 100kbps (Standard mode), 400kbps (Fast mode), and 1Mbps (Fast mode Plus) ;
 - Six SPI Master/Slave modules, one supporting up to 75MHz and others up to 60MHz;
 - Eight universal asynchronous receiver/transmitter (UARTs) modules, supporting data rates of up to 12Mbps (Profibus) ;
 - Three Flexible Input-Output (FLEXIO) modules ;
- Timers and PWMs
 - Four Quad Timer/PWM modules (QTPMs), each with up to 2-channels and 32-bit resolution ;
 - Two Low-Power Periodical Interrupt Timers (LPITs) that operate as a 32-bit counter and generating a periodic interrupt on counter timeout ;
 - Two Low-Power Timers (LPTMRs) that operate as a time counter with optional prescaler, or as a pulse counter with optional glitch filter ;
 - Four Flexible Pulse Width Modulators (FlexPWMs) with up to 8 individual PWM channels, and 16-bit resolution PWM to generate various switching patterns, including highly sophisticated waveforms. It is ideal for controlling switch mode power supplies topologies and motor control ;
 - Four Enhanced Quadrature Decoder (eQDCs) modules ;

- IO and Pin Multiplexing
 - Digital Input-Output (IO) operating at 1.8V and 3.3V signaling levels ;
 - General-Purpose Input-Output (GPIO) modules with interrupt capability ;
 - Input-Output Multiplexing Controller (IOMUXC) to provide centralized pad control ;
- Analog
 - Two 16-bit analog-digital converters (ADCs) supporting up to 4MSPS sample rate and up to 24-channels ;
 - One 12-bit digital-to-analog converter (DAC) ;
 - Four analog comparators (ACMPs) with 8-bit DAC control ;
 - Temperature sensor with programmable trim points ;
- Power Management
 - 1.71V up to 3.6V input power supply range ;
 - 1.8V typ. when powered by external Power Management IC (PMIC) ;
 - 3.3V typ. when powered by external PMIC ;
 - 3.0V typ. when powered from a LiMnO₂ battery ;
 - Full PMIC integration including on-chip DC-DC converter and Low-Dropout (LDO) regulator, with bypass option to support external PMIC ;
 - Various operating- & power modes for dynamic power-performance control ;
- System Debug
 - ARM CoreSight™ compliant debug and trace architecture ;
 - Trace Port Interface Unit (TPIU) to support off-chip real-time trace ;
 - Cross Triggering Interface (CTI) ;
 - Support for 5-pin JTAG and SWD debug interface ;
- Package
 - 14mm x 14mm BGA, 0.8mm pitch, 289 Balls ;
 - 10mm x 10mm BGA, 0.65mm pitch, 196 Balls ;
 - 12mm x 12mm BGA, 0.8mm pitch, 196 Balls ;
 - 9mm x 9mm BGA, 0.65mm pitch, 169 Balls ;
 - Supporting 4-layer PCB design and 2-layer substrate ;
- Industrial & AEC Q100 Grade 2 mission profiles support. T_j range: -40 °C to +125°C ;

3.4 Endianness support

The i.MX RT2660 supports little endian only.

4. General Requirements

This Chapter provides a description of the i.MX RT2660 SoC general requirements.

4.1 XEA-1 platform

The Crossover Evolved Architecture 1 (XEA-1) Platform is intended to answer the needs for the evolution of the i.MX RT crossover line from i.MX RT1060, i.MX RT1170, i.MX RT1180, i.MX RT700 and beyond. In addition, it is meant to address the needs identified for future wireless crossover i.MX RT products. Re-using subsystems and architectures from i.MX RT700 will leverage the expertise, investment, and effort exerted there. By defining a platform based on configurable, reusable, and extendable subsystems, that meet the needs of a family of products defined up front, the development time and budget of the entire family is minimized while delivering a compelling family of products to the market.

The i.MXRT2K product family will include members serving the Lite Smart Edge, Industrial IOT, and Lite Automotive markets, with next-generation ARM Cortex-M cores, integrated machine learning, and versatile graphics and HMI. While competitors have announced products based on the same next-generation ARM Cortex-M cores, such as the Cortex-M85, the i.MXRT2K product family will leap-frog those competitors with better performance, features, and integration at competitive cost.

The i.MX RT2660 is the first product based on the XEA-1 platform [14]. Please refer to Chapter 0 SoC Architecture, for more details about XEA-1 Platform re-use.

4.2 Process technology choice

The i.MX RT2660 target process technology is 22FDX+. Table 6 provides a high-level overview of the selected process technology. The technology flavor is consistent across XEA-1 platform products (i.MX RT2660, i.MX RT2520W, i.MX RT2770) as well as WCS products such as Hood and Fuji.

Table 6. Process technology choice for i.MX RT2660

Parameter	Item	Comment
Technology	GF 22FDXP	22nm FDSOI CMOS, namely 22FDX+
Metal stack	10M_2Mx_5Cx_1Jx_2Qx_LB 10 interconnect metal layers	M1-M7: thin metal M8: thick metal M9-M10: ultra thick metal
Flavor	Baseline technology	No MRAM or RRAM required
Required process options	<ul style="list-style-type: none"> • Flipped well (SLVT/LVT) • AEC-Q100 Grade 2 	for power-efficient high-performance digital Automotive Grade 2 compliance
Maximum voltages		Core: 0.945V max., 0.65V to 0.9V typ., 0.55V min. SLVT/LVT I/O EG: 1.98V max., 1.2V/1.5V/1.8V typ. LDMOS: 3.3V typ., 5.0V typ., 6.5V typ.

Note: synopsys 6.75T 104CPP cell 0.9Vnom is not available yet.

Note: RT2660 design/implementation will not cover 0.55Vmin, but will test in silicon to understand more about 22FDX process node.

4.3 Foundation IP choice

Table 7 provides a high-level overview of the selected 22FDX+ foundation IP.

Table 7. Foundation IP choice for i.MX RT2660

Parameter	Item	Comment
Logic	(1) Synopsys 6.75T HD (104CPP) logic libraries SLVT/LVT, FBB supported, multi-channel length support (2) NXP 6.75T optimized logic libraries where applicable (3) Synopsys 6.75T ULL logic libraries for VBAT_SS UHVT	Maximize long-channel LVT usage for reducing leakage => concerns at 125°C Maximize the usage of multibit flip-flops to benefit clock tree and timing closure Make use of AI/ML optimized standard cells as this can benefit timing, area and routability in the high-performance processor cores
DGO	Synopsys 10T GO2 logic library LVT	
SRAM	NXP EFVSRAM with P124 bitcell SLVT/LVT periphery with FBB supported, Low power modes supported	NXP EFVSRAM is a new SRAM compiler development with i.MX RT2660 as lead vehicle
Register file	Synopsys ADSPREG with P124 bitcell SLVT/LVT periphery with FBB supported.	
2-Port Regfile	Synopsys AD2PREG with P124 bitcell SLVT/LVT periphery with FBB supported. Synopsys AU2PREG with P124 bitcell SLVT/LVT periphery with FBB supported.	Consider use of Synopsys (Invecas) R2PL with TP185SL bitcell; LVT periphery with FBB supported. This off-the-shelf 2PREG compiler is 0.65V capable, but not yet NXP internalized.
ROM	Synopsys ADV1ROM	
OTP	Synopsys DWC NVM OTP XBC GF 22nm FDX 1.8V shfg2_gf22fdx18_1kx42_cm16s1_ac	42Kbit (1024 x 42bit) OTP core
IO	NXP IO libraries? Discussions ongoing with NXP IO team to move from Synopsys IO baseline to NXP IO libraries. It is unclear whether i.MX RT2K IO requirements can be honored.	PDA blocking item – no complete IO solution for i.MX RT2660 confirmed as per today

4.4 Package choice

Table 8. Package choice for i.MX RT2660

Description	Requirement/Required	Remarks
Required package(s)	BGA289, 14mmx14mm, 0.8mm pitch BGA196, 10mmx10mm, 0.65mm pitch	From product marketing: BGA289 as superset package

Description	Requirement/Required	Remarks
	BGA196, 12mmx12mm, 0.8mm pitch BGA169, 9mmx9mm, 0.65mm pitch	A SiP package with serial NOR flash to be determined by marketing

Blocking for PDA:

- Initial assessment revealed that the total amount of needed pinout does not fit a BGA196 package. No package solution can be confirmed yet ; New package proposal from product marketing: [BGA289 ; Change Request to be made!](#).
- Package DRI to complete package assessment with BGA289 package, which requires a placed padring which is to be provided SoC Design DRI.

Table 9. IC requirements traceability: package requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_PKG_1-3	1) BGA-196, 0.65mm pitch, 10x10mm body	Must have	Open
iMXRT2660_PKG_1-4	2) BGA-196, 0.8mm pitch, 12x12mm body	Must have	Open
iMXRT2660_PKG_1-5	3) BGA-169, 0.65mm pitch, 9x9mm body	Must have	Open
iMXRT2660_PKG_1-6	4) A SiP package with serial NOR flash to be determined	Should have	No
iMXRT2660_PKG_1-8	BGA289 is the superset, 14x14, Pitch 0.8mm. Requires Industrial and Auto qualification	Should have	No

4.4.1 Pinning

A i.MX RT2660 design study concluded that about 280 functional pads for bringing out the required SoC functionality for the targeted use-case scenarios. Refer to Section 6.10.2.

Blocking for PDA:

- Soc Design DRI to provide placed padring solution for die pad placement information ;
- Package DRI to complete package assessment for substrate and ballout information.

4.4.2 Pin description

The following table lists the description of all the pin of the i.MX RT2660. It provides the assignment of these pins for the different supported packages and associated pad types.

The different pad types are:

- PWR: supply pad
- GND: ground pad
- A: analog pad
- DIO: regular digital IO pad
- HSDIO: high-speed digital IO pad
- LLDIO: low-leakage digital IO pad
- OD: Open-Drain IO pad

The JTAG functions TCK, TMS, TDI, TDO and TRSTN are available and are selected default on corresponding pins. Reference to share point [Peripheral Input Mux](#) for detailed information.

The following table lists the description of all the pin of the i.MX RT2660. It provides the assignment of these pins for the different supported packages and associated pad types.

Table 10. **RT2660 Pin list**

BGA289 pin	BGA196 pin	Symbol	Die pad number	Pad type	Reset state	IO external supply rail	IO internal supply rail	Main function	Comment
Power- and ground related pins									
VDD_PMU				PWR	-	-	-	INPUT SoC Vdd	
VBAT_AON				PWR	-	-	-	INPUT Always-On SoC Vdd	
VBATPWR0V8				PWR	-	-	-	INPUT DCDC	Short to VDD_PMU on BGA substrate?
LX_CORE				A	-	-	-	DCDC inductor connection	
VDD_CORE				PWR	-	-	-	Digital Core Vdd decoupling	0.5-0.9V typ. for logic & memories & IO
VDD_0V8				PWR	-	-	-	0.8V Core Vdd decoupling	Fixed 0.8V for PHYs & IO WAKE_SS when VDD_CORE is not 0.8V.
VDD_MIPI_0V8				PWR	-	-	-		Double bond to VDD_0V8
VDD_1V8				PWR	-	-	-	1.8V Core Vdd decoupling	Fixed 1.8V for PHYs & Body bias
VDD_MIPI_1V8				PWR	-	-	-		Double bond to VDD_1V8
VDDA_1V8				PWR	-	-	-	1.8V Clean Analog Vdd decoupling	Fixed 1.8V typ.
VDD_USB_3V3				PWR	-	-	-	INPUT 3.3V external USB Vdd	3.3V typ.
VDDIO_AON				PWR	-	-	-	INPUT Vdd Always-On pads	1.8V or 3.3V typ.
VDDIO1				PWR	-	-	-	INPUT Vdd 1 st pad section	1.8V or 3.3V typ.
VDDIO2				PWR	-	-	-	INPUT Vdd 2 nd pad section	1.8V or 3.3V typ.
VDDIO3				PWR	-	-	-	INPUT Vdd 3 rd pad section	1.8V or 3.3V typ.
VSS_MIPI				GND	-	-	-		Short to VSS on BGA substrate
VSS_USB				GND	-	-	-		Short to VSS on BGA substrate
VSS				GND	-	-	-	Ground	Assumes connection of all ground on BGA substrate
Clock related pins									
XTALIN				A	-	-	-	SXOSC crystal in	
XTALOUT				A	-	-	-	SXOSC crystal out	
RTCXIN				A	-	-	-	OSC32K crystal in	
RTCXOUT				A	-	-	-	OSC32K crystal out	
Analog related pins									
VREFP				A	-	-	-	Reference voltage HIGH	External reference ADCs and DAC
VREFN_ANA				A	-	-	-	Reference voltage LOW	
DACOUT				A	-	-	-	DAC 1.8V output	
AC0_BUS				A	-	-	-	CGU analog test bus	
AC1_BUS				A	-	-	-	CGU analog test bus	
PHY related dedicated pins									
MIPI_CSI_CLKP				DIO		VDD_MIPI_CSI	VDD_0V8		
MIPI_CSI_CLKN				DIO					
MIPI_CSI_D0P				DIO					
MIPI_CSI_D0N				DIO					
MIPI_CSI_D1P				DIO					
MIPI_CSI_D1N				DIO					
MIPI_DSI_CLKP				DIO			VDD_0V8		

BGA289 pin	BGA196 pin	Symbol	Die pad number	Pad type	Reset state	IO external supply rail	IO internal supply rail	Main function	Comment
		MIPI_DSI_CLKN		DIO		VDD_MIPI_DSI			
		MIPI_DSI_D0P		DIO					
		MIPI_DSI_D0N		DIO					
		MIPI_DSI_D1P 		DIO					
		MIPI_DSI_D1N 		DIO					
		USB0_VBUS		DIO		VDD_USB0	VDD_0V8		
		USB0_DM		DIO					
		USB0_DP		DIO					
		USB1_DM		DIO		VDD_USB1	VDD_0V8		
		USB1_DP		DIO					
Always-On IO pins									
PIO0_0		LLDIO	Output (drive low)	VDDIO_AON	VBAT_0V8	PMIC_MODE[0]			
PIO0_1		LLDIO	Output; (drive low)	VDDIO_AON	VBAT_0V8	PMIC_MODE[1]			
PIO0_2		LLDIO	HiZ	VDDIO_AON	VBAT_0V8	Tamper pin input/output			
PIO0_3		LLDIO	HiZ	VDDIO_AON	VBAT_0V8	Tamper pin input/output			
PIO0_4		LLDIO	HiZ	VDDIO_AON	VBAT_0V8	WAKEUP			
RESET_B		LLDIO	BiDir; PU	VDDIO_AON	VBAT_0V8				RESET_b, JTAG, BOOT_MODE and serial ISP interfaces should be all in the same VDDIO domain.
POR_B		LLDIO	Input	VDDIO_AON	VBAT_0V8	Included in PMU_SS?			
TEST_MODE		LLDIO	Input	VDDIO_AON	VBAT_0V8	Test Mode			

Multi-function IO pins See [Peripheral Input Mux](#) for detailed information.

4.5 Industrialization requirements

Table 11. Industrialization requirements

Description	Requirement/Required	Remarks
Automotive qualified	AEC-Q100 Grade 2	Automotive Grade 2
Industrial qualified	Extended Industrial	
Consumer qualified	<i>Mission profile to be provided</i>	
PPM target level	< 10	NXP Quality Maturity Level 3 [12]. <ul style="list-style-type: none"> • Stuck-At scan coverage of 99% ; • Transition delay scan coverage of 90% ; • 100% of memory Bist coverage.
SoC temperature range	-40°C up to +125°C	This concerns junction temperature
SoC input supply voltage range @SoC pins	1.71V up to 3.6V	SoC input supply and chip-to-chip signaling
Maximum voltage @SoC pins	3.6 V	
ESD Human Body Model (HBM)	2 kV	
ESD Charged Device Model (CDM)	500 V	
Latch up	±100mA	

Table 12. IC requirements traceability: Industrialization requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_REL_1-2	This processor shall support a junction temperature operating range of -40C to 125C	Must have	Yes as per design target. <i>To be confirmed during industrialization phase</i>
iMXRT2660_REL_1-3	This processor shall support 5000 Power-On Hours at a junction temperature of +125°C operating at maximum frequency.	Must have	<i>During industrialization phase</i>
iMXRT2660_REL_1-4	This processor shall support 15000 Power-On Hours at a junction temperature of +105°C operating at maximum frequency.	Must have	<i>During industrialization phase</i>
iMXRT2660_REL_1-5	PPM target is <10 (target should be NXP quality maturity level 3)	Must have	<i>During industrialization phase</i>
iMXRT2660_REL_1-6	This processor shall comply with AEC-Q100 Grade 2 qualification with PPAP.	Must have	<i>During industrialization phase</i>
iMXRT2660_IOP_1-6	All IO pads shall provide following ESD protection levels: - Human Body Model (HBM): 2kV - Charged Device Model (CDM): 500V	Must have	Yes as per design target. <i>To be confirmed during industrialization phase</i>

4.6 SoC performance requirements

The i.MX RT2660 needs to achieve a given set of performance requirements for achieving the use-case performance as well as for implementing a competitive product. The i.MX RT2660 shall make use of Forward Body Biasing (FBB) capabilities of the 22FDX+ process technology for achieving the highest performance for the high-performance regions of the SoC. In the non-performance critical regions of the SoC, the i.MX RT2660 shall utilize Zero Body Biasing (ZBB) in order to save leakage current. Reverse Body Biasing (RBB) will not be implemented in order to reduce design complexity and integration cost, as the expected leakage power savings for RT2660 are limited.

Per today, 22FDX+ process technology does not allow supply voltage higher than 0.88V for the digital core in case of an Automotive Grade 2 product. However, the i.MX RT2660 shall be designed to support up to 0.945V supply voltage bound for the digital core; this to benefit further application use-cases in Automotive, Industrial and Consumer market segments.

The following table provides an overview of the main performance targets for the i.MX RT2660.

Table 13. [i.MX RT2660 performance target per function](#)

Category	Function	Target
Maximum frequency	ARM Cortex-M85	Up to 700 MHz at supply normal drive level (0.8V) More than 700 MHz at supply overdrive level (0.9V)
	Neutron 256S	Up to 700 MHz at supply normal drive level (0.8V) More than 700 MHz at supply overdrive level (0.9V)
Performance	CPU benchmark	At least 4,375 CoreMark with ARM Cortex-M85
	NPU benchmark	Up to 358.4 GOPS with Neutron-256S
	NPU ML benchmark	MobileNetv1.0 224 benchmark running on Neutron-256S NPU with a maximum inference time of 16ms
	CPU ML benchmark	The CMSIS-NN average output performance on a fully connected layer with 8-bit weight and 8-bit activation on Cortex-M85 shall be 7x improvement over Cortex-M7 on RT1170 at the same frequency.

As per ARM, the ARM Cortex-M85 achieves a maximum performance of 6.28 Coremark/MHz [13]. When running at a 700MHz operating clock, this translates to a Coremark performance of 4,396. The i.MX RT2660 design shall target to achieve these performance reference points as input to the chip implementation phase.

The Neutron-256 NPU offers a theoretical maximum compute performance of 256 multiply-accumulates per cycle (MACs/cycle). When it runs at a 700MHz clock frequency, a theoretical maximum performance of 179.2 GMAC per second is achieved (Int8). Since every MAC concerns 2 operations per second (OPS), the maximum achievable performance with Neutron-256 at 700MHz clock is 358.4 GOPS. By choosing the Neutron-256 as NPU core, the required theoretical NPU benchmark performance of 358.4 GOPS can be met.

Table 14. [IC requirements traceability: Performance requirements](#)

AS/RS identifier	Requirement	Classification	Covered
iMXRT2660_CPU_2-2	The Cortex-M85 core shall achieve at least 4,396 CoreMark. This is achievable with 1x Cortex-M85 at 700MHz (assuming 6.28CM/MHz).	Must Have	During design phase
iMXRT2660_ML_3-2	The NPU shall achieve theoretically 360GOPS with N256S.	Must have	358.4 GOPS
iMXRT2660_ML_3-3	The TensorFlow Lite benchmark application (MobileNetv1.0 224) on NPU scenario should achieve a performance of, at maximum, 16ms, with N256S.	Must have	During design phase

AS/RS identifier	Requirement	Classification	Covered
iMXRT2660_ML_4-2	The CMSIS-NN average output performance should reach ARM theoretical performance with performance optimized configuration.	Must have	During design phase

4.7 SoC area target

The first and primary optimization priority of the i.MX RT2660 SoC design concerns **low-cost**, given that the SoC performance requirements can be met (refer to Section 4.6). The i.MX RT2660 shall target a maximum die size of up to 16.5mm² including seal-ring.

In order to achieve a small chip area, the chip implementation shall be done by making use of the smallest track-height digital logic libraries for which the SoC can still meets its performance target. A power-performance-area (PPA) analysis has been performed for a place-and-routed ARM Cortex-M85 design in 22FDX+ by the i.MX RT2660 SoC design team. Up to 700MHz operation seems achievable with 6.75T digital core for the 0.8V scenario with FBB enabled. At the maximum speed point, the 6.75T digital logic design remains to be smaller than a 9T design. Hence, we conclude that the i.MX RT2660 digital core shall be based on 6.75T digital logic libraries only.

SRAM-wise, the chip implementation shall be done with the largest size SRAM instances for which the SoC can still meets its performance target.

IO-wise, the chip implementation could be pad constrained as initial study has showed that about 290 die pads will be required. Hence, maximum usage of staggered pad placement shall be done in order to minimize IO related die area.

Table 15 shows an initial first-order SoC area estimation, which gives a high-level impression of the estimated SoC area as per current state. **Note that there exists a high degree of uncertainty due to use of new to be developed IP, while the SoC design phase has not started yet.**

Table 15. i.MX RT2660: initial SoC area estimation

		CMPT_SS	MAIN_SS	MEDIA_SS	AUDIO_SS	COMM_SS	WAKE_SS	Rest	RT2660 SoC						
Analog core	IP area [mm ²]	-	~0.43	-	-	-	~0.35	~2.25	~3.1						
	PHY area [mm ²]	-	-	~0.58	-	-0.32	-	-	~0.9						
	total area [mm ²]	-	~0.43	~0.58	-	-0.32	~0.35	~2.25	~4.0						
Digital core (excl. memories)	DGO library	-	-	-	-	-	Tbd								
	Gate count [kG]	-	-	-	-	-	~5.1	~13	~55kG						
	logic library	6.75T HD					6.75T HD								
	Gate count [kG]	~3,990	~4,438	~3,064	~906	~2,278	~489	~103	~15.3MG						
Memories	Digital area [mm ²]	~1.22	~1.36	~0.94	~0.28	~0.70	~0.15	~0.03	~4.7						
	Memory area [mm ²]	~2.86	~0.94	~0.38	~0.09	~0.19	-	~0.03	~4.5						
Core area	[mm ²]	~4.08	~2.73	~1.89	~0.37	~1.21	~0.50	~2.38	~13.2						
IO sections on 4 sides	# IOs							290							
	[mm ²]							~2.2							
Estimated total SoC area - 5% uncertainty margin								~ 15.7 mm²							
Estimated total SoC area – midpoint target (incl. seal-ring and excl. scribe lane)								~ 16.5 mm²							

	CMPT_SS	MAIN_SS	MEDIA_SS	AUDIO_SS	COMM_SS	WAKE_SS	Rest	RT2660 SoC
Estimated total SoC + 5% uncertainty margin ~ 17.3 mm²								

Assumptions: up to 290 pads in IO section, only staggered pad placement with tall pad frame (165µm height) at 70µm pitch for high-speed IOs (translating to 140µm pad pitch single row) and 35µm pitch for other IO (translating to 70µm pad pitch single row), utilization factors: logic 55%, dgo 45%, memory macros 95%, and analog macros 85%.

Table 16. **IC requirements traceability: key performance indicator requirements**

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_KPI_1-11	The die area of this processor shall be less than 15mm ²	Must have	18.7mm ² , or 20.57 with 10% margin

4.8 SoC power consumption targets

The second optimization priority of the i.MX RT2660 SoC design concerns **low-power consumption**, given that the SoC performance requirements can be met (refer to Section 4.6) and SoC area target are not compromised (refer to Section 4.7). This concerns optimization for both SoC dynamic power consumption as well as leakage power consumption.

In order to minimize area/cost implications, the i.MX RT2660 shall make use of a single digital supply voltage rail for the digital core. This choice makes digital logic and memories to operate from the same power supply rail.

The i.MX RT2660 shall implement various active and standby operating modes, such that SoC power consumption can be optimized for each use-case application. The different operating modes offer a trade-off between functionality and power consumption, while they can be selected dynamically during functional operation of the SoC.

Table 17 shows the proposed targeted power consumption for the i.MX RT2660, which has been determined after a detailed assessment during PDA phase. The listed power targets are based on the following assumptions:

- Power consumption at SoC input supply pin including the main supply as well as the battery-backup domain. Power consumption by IO supply rails are not included ;
- The power targets are set for typical process condition and room temperature at 25°C.

Note that the SoC design shall target design for lower SoC power consumption when feasible.

During PDA phase, SoC Design has raised concerns about the implementation effort for several low-power design techniques that have proposed by SoC architecture; the concern is schedule related. BL has stated that hitting schedule is more important than low-power operation, while it shall be ensured that the i.MX RT2660 can achieve competitive power consumption. Therefore, a number of architectural compromises have been made – Refer to Section 6.1.5.

The further required low-power techniques to be supported are shown in Chapter 8.

Table 17. **i.MX RT2660 preliminary targeted power consumption from input supply pin**

Scenario	Power target @1.8V supply (typical process, 25°C)	Functionality needs
Active1	≤ 250 mW	Digital core voltage is at normal drive level ARM Cortex-M85 running Coremark from TCM at 700MHz

		All bus- and peripheral clocks are on and set at maximum frequency, without any data activity NPU clock is gated Media, Audio and Comms subsystems are off
Active2	≤ 140 mW	Digital core voltage is at normal drive level ARM Cortex-M85 running Coremark from TCM at 500MHz System operating clock provided by 192MHz FRO + Main PLL All bus are on and peripheral clocks are off NPU clock is gated Media, Audio and Comms subsystems are off
Active3	≤ 100 mW	Digital core voltage is at normal drive level ARM Cortex-M85 running Coremark from TCM at 192MHz System operating clock provided by 192MHz FRO All bus clocks are on and peripheral clocks are off, except for 1 DMA, 1 I2C, 1 UART in the wake subsystem running on divided system clock NPU clock is gated Media, Audio and Comms subsystems are off
Sleep	≤ 32 mW	Digital core voltage is at normal drive level All clocks are gated An I2C in the low-power subsystem and the voice detection block in the DMIC are still functional, running on low frequency clock source Media and Comms subsystems are off; Audio is also off except DMIC portion
Deep Sleep	≤ 1.8mW	The SoC is mostly in a static state where all clocks are stopped, but the state of the logic and all memory is still maintained Digital core voltage is dropped to the lowest level possible. Some power domains are optionally turned off for power reduction An I2C in the low-power subsystem and the voice detection block in the DMIC are still functional, running on low frequency clock source
Power Down	≤ 150 µW	Digital core voltage is dropped to the lowest level possible All logic and memory are turned off via internal regulator and power switch 64KB SRAM is retained for fast wake up
Deep Power Down	≤ 15 µW (@3V)	DCDC converter and all LDOs in the main SoC are turned off All logic and memory in the main SoC are off Battery-backup domain registers are memory is retained RTC clock is active Full reboot needed when the power reapplied to this processor

Table 18 shows the targeted wake-up time for the i.MX RT2660 operating modes, after detailed assessment during PDA phase. The wake-up time is quoted until first code execution of the ARM Cortex-M85 processor.

Table 18. [i.MX RT2660 preliminary targeted wakeup times from each power mode](#)

Scenario	Wakeup time target @1.8V supply (typical process, 25°C)	Functionality needs
Active 1/2/3	Instantaneous	Active operation mode of the SoC – wake-up time dictated by ungating of the operating clocks
Sleep	≤ 10 µs	All clocks are gated and digital core voltage at normal level.
Deep Sleep	≤ 150 µs	All clocks stopped. Logic and memory is fully state retained, with digital core supply voltage dropped to the lowest level possible.



Power Down	$\leq 650 \mu\text{s}$	All clocks stopped. All logic and memory are turned off. 64KB SRAM is retained for fast wake up.
Deep Power Down	Boot time	Only the battery-backup domain is powered, rest of the SoC is turned off. The battery-backup domain is functional. Full reboot needed when the power reapplied to this processor.

Table 19. IC requirements traceability: Power target requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_PWR_5-2	<p>Following are power target for different setpoints.</p> <ul style="list-style-type: none"> - The usage scenario is summarized - Power target include dynamic and leakage powers consumed by the SoC, including the battery-backup domain. Power consumption by IO supply rails are not included. - The power target is set for typical room temperature at 25C - Power consumption goals are based on a single 1.8V input to the SoC device. 	Information	-
iMXRT2660_PWR_5-3	Setpoint 1	Heading	-
iMXRT2660_PWR_5-4	<p>Usage scenario: Active 1</p> <ul style="list-style-type: none"> - CM85 executes coremark at 700MHz from TCMs - All bus clocks and peripheral clocks are at their max frequency 	Must have	Yes see Table 17 Open: Req. update ongoing
iMXRT2660_PWR_5-5	Target: Power consumption: 250mW	Must have	Open: Req. update ongoing
iMXRT2660_PWR_5-6	Setpoint 2	Heading	-
iMXRT2660_PWR_5-7	<p>Usage scenario: Active 2</p> <ul style="list-style-type: none"> - CM85 executes coremark at 500MHz from TCMs. - CM85 runs on HS FRO (or equivalent clock source) - All bus clocks and peripheral clocks are off, except for the bus clocks required for memory access. 	Must have	Yes see Table 17 Open: Req. update ongoing
iMXRT2660_PWR_5-8	Target: Power consumption: 140mW	Must have	Open: Req. update ongoing
iMXRT2660_PWR_5-9	Setpoint 3	Heading	-
iMXRT2660_PWR_5-10	<p>Usage scenario: Active 3</p> <ul style="list-style-type: none"> - CM85 executes coremark at 192MHz from TCMs. - CM85 runs on FRO192 clock. - All bus clocks and peripheral clocks are off, except for 1 DMA, 1 I2C, 1 UART in the low-power subsystem running on divided clock from FRO192. 	Must have	Yes see Table 17 Open: Req. update ongoing
iMXRT2660_PWR_5-11	Target: Power consumption: 100mW	Must have	Open: Req. update ongoing
iMXRT2660_PWR_5-12	Setpoint 4	Heading	-
iMXRT2660_PWR_5-13	<p>Usage scenario: Sleep</p> <ul style="list-style-type: none"> - Digital core voltage is at normal drive level. - All clocks are gated. - An I2C in the low-power subsystem and the voice detection block in the DMIC are still functional, running on local low frequency clock source. 	Must have	Yes see Table 17 Open: Req. update ongoing
iMXRT2660_PWR_5-14	Target: Power consumption: 32mW, Recovery time: 10us	Must have	Open: Req. update ongoing
iMXRT2660_PWR_5-15	Setpoint 5	Heading	-
iMXRT2660_PWR_5-16	<p>Usage scenario: Deep Sleep</p> <ul style="list-style-type: none"> - The SoC is mostly in a static state where all clocks are stopped, but the state of the logic and memory is still maintained. 	Must have	Yes see Table 17 Open: Req. update ongoing

AS/RS identifier	Contents	Classification	Covered
	<ul style="list-style-type: none"> - Digital core voltage is dropped to the lowest level possible. Bias is enabled. - Some power domains are optionally turned off for power reduction. - An I2C in the low-power subsystem and the voice detection block in the DMIC are still functional, running on local low frequency clock source. 		
iMXRT2660_PWR_5-17	Target: Power consumption: 1.8mW, Recovery time: 150us	Must have	Open: Req. update ongoing
iMXRT2660_PWR_5-18	Setpoint 6	Heading	-
iMXRT2660_PWR_5-19	Usage scenario: Power Down <ul style="list-style-type: none"> - All logic and memory are turned off via internal regulator and power switch. - 64KB SRAM is retained for fast wake up. - Bias is enabled for SRAM retention. 	Must have	Yes see Table 17 Open: Req. update ongoing
iMXRT2660_PWR_5-20	Target: Power consumption: 150uW, Recovery time: 650us	Must have	Open: Req. update ongoing
iMXRT2660_PWR_5-21	Setpoint 7	Heading	-
iMXRT2660_PWR_5-22	Usage scenario: Deep Power Down <ul style="list-style-type: none"> - DCDC converter and all LDOs in the main SoC are turned off. All logic and memory in the main SoC are off. - Battery-backup domain is functional. - Wakeup and execute from pSRAM, which was in self-refresh when the chip in Deep Power Down state. 	Must have	Yes see Table 17 Open: Req. update ongoing
iMXRT2660_PWR_5-23	Target: Power consumption: 65uW, Recovery time: 1ms	Must have	Rejected, boot time recovery Open: Req. update ongoing
iMXRT2660_PWR_5-24	Setpoint 8	Heading	-
iMXRT2660_PWR_5-25	Usage scenario: VBAT <ul style="list-style-type: none"> - Only the battery-backup domain is powered. - RTC clock is active - All tamper functions in this domain are enabled. - Other supplies to the chip are turned off. - Full reboot needed when the power reapplied to this processor. 	Must have	Dropped Open: Req. update ongoing
iMXRT2660_PWR_5-26	Target: Power consumption: 12uW, Recovery time: Boot time	Must have	Dropped Open: Req. update ongoing

5. Functional Description

This Chapter provides a functional description of the i.MX RT2660 SoC.

5.1 Functional block diagram

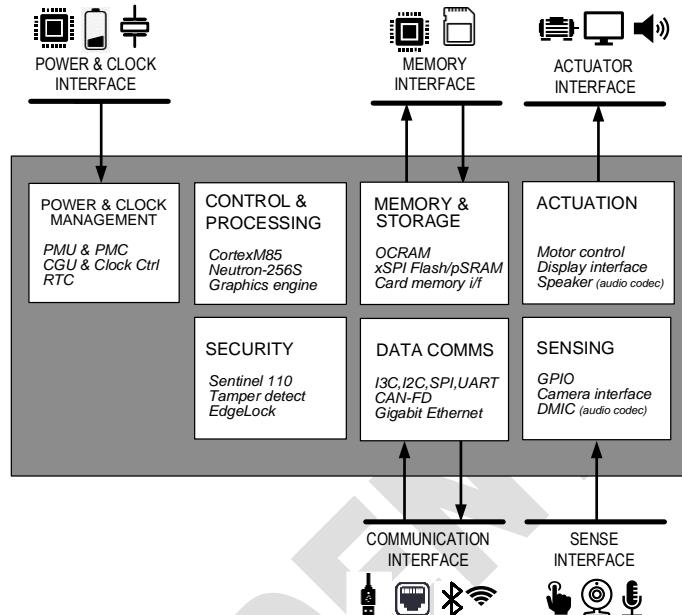


Fig 2. i.MX RT2660 functional diagram

Fig 2 shows the functional diagram of the i.MX RT2660. The i.MX RT2660 shall implement the following main functionalities:

- Sensing
 - MIPI 2-lane camera serial interface (CSI-2) with on-chip PHY;
 - Parallel Camera Sensor Interface supporting 8/16/24 bit CSI input;
 - Digital microphone supporting up to 4 input lines with two channels per line;
 - S/PDIF audio input interface;
 - Synchronous audio interface (SAI) supporting I2S, AC97, TDM, and Codec/DSP;
 - General-purpose input/output (GPIO) modules;
- Control & processing
 - ARM Cortex-M85 for high-performance processing and control;
 - NXP Neutron-256S for machine learning inference application;
 - DMA controller for memory-to-peripheral, peripheral-to-memory and memory-to-memory communications;
 - Generic 2.5D Graphics engine supporting common operations and multiple pixel formats (RGB, YUV444, YUV422, YUV420, YUV400) for displays;
- Memory & storage
 - On-chip total static random access memory of 1.5 MB;
 - xSPI (octal/quad/dual/single) Flash interface up to 200MHz operation. Support for on-the-fly decryption and encryption for eXecute In-Place (XIP), dual-image boot, and garbage collection capabilities;

- xSPI interface supporting pSRAM (HyperRAM) memory (x1, x2, x4, x8, x16) with up to 250MHz operation. Support for on-the-fly decryption and encryption ;
- uSDHC memory card interface supporting eMMC 5.1 (HS400) and SD/SDIO 3.0;
- Actuation
 - MIPI 2-lane display serial interface (DSI) with on-chip PHY;
 - Parallel Camera Sensor Interface supporting 8/16/24 bit CSI input;
 - S/PDIF audio output interface;
 - Synchronous audio interface (SAI) supporting I2S, AC97, TDM, and Codec/DSP;
 - General-purpose input/output (GPIO) modules;
- Data communication
 - 1Gbps Ethernet interface with support for IEEE1588 ;
 - Two USB interfaces, one USB 2.0 controller with integrated USB 2.0 (HS) PHY and the other one USB 1.1 controller with integrated USB 1.1 (FS) PHY ;
 - I3C, I2C, SPI, UART interfaces supported ;
 - CAN interface with flexible data rate (CAN-FD) supported ;
- Security
 - Sentinel 110 (S110) IP supporting a wide range of cryptographic algorithms and providing strong key isolation from the rest of SoC;
 - Tamper detection monitoring tamper attacks on device power supply, processor- or secure module clock, operation temperature and tamper pins;
- Power & Clock management
 - Integrated power management for (internal) digital, analog and IO supplies;
 - Integrated clock generation, -management and -control that includes a 16-40MHz and 32kHz crystal based input clock;

Table 20. IC requirements traceability: general functional requirements

AS/RS identifier	Content	Classification	Covered
iMXRT2660_CPU_1-3	This processor shall utilize the Cortex-M85 as the main CPU for target applications. This core was selected for various reasons, including: - Over 15% Coremark uplift from Cortex-M7 - MVE to enable DSP processing, ML post-processing, light ML processing without the NPU - TrustZone-M architecture to enable robust levels of software security protection - General customer's preference	Must have	Yes
iMXRT2660_ML_1-2	ML shall be supported in this processor via two mechanisms:	Information	-
iMXRT2660_ML_1-3	The main CPU: This is often the option for running ML algorithms which don't require significant inference processing. This is achievable with the MVE implemented in the Cortex-M85.	Must have	Yes
iMXRT2660_ML_1-4	The NPU: This is a dedicated NPU designed to work with its own set of TCM, on chip SRAM, and relatively low bandwidth DRAM to efficiently process CNN based deep neural networks and will be the primary focus of the requirements herein.	Must have	Yes
iMXRT2660_MEM_2-2	The total on-chip SRAM is 1.5MB with ECC, including: - 256KB CM85 TCMs - 256KB NPU TCMs - 1MB System RAM by default..	Must have	Yes
iMXRT2660_MEM_2-3	The total on-chip SRAM is 2.0MB with ECC, including: - 512KB CM85 TCMs	Should have	Rejected, SoC area constraint

AS/RS identifier	Content	Classification	Covered
	- 512KB NPU TCMS - 1MB System RAM by default.		
iMXRT2660_MEM_2-5	ECC shall be implemented for TCMs and system RAMs.	Must have	Yes
iMXRT2660_MEM_2-6	When ECC in System RAM is not enabled, the ECC memory shall be repurposed as general purpose SRAM.	Must have	No, not supported
iMXRT2660_PWR_1-3	This processor requires simplified power architecture to minimize the PMIC requirements. The intention is to be able to use very inexpensive external components.	Information	Yes w/ integrated PMU
iMXRT2660_AUD_7-2	This device shall support audio streaming over USB communication.	Must have	Yes
iMXRT2660_AUD_8-2	This device shall support audio streaming over Ethernet communication.	Must have	Yes

5.2 Power supply scenarios

The i.MX RT2660 targets application into a wide range of applications that may provide a different input power supply source to the SoC. The following six power supply source options shall be supported at the power supply inputs of the SoC:

1. 1.8V single-input power supply source ;
2. 3.3V single-input power supply source ;
3. 1.8V and 3.3V dual-input power supply source ;
4. Double Alkaline batteries ;
5. External PMIC with on-chip DCDC converter bypassed ;
6. External PMIC with on-chip DCDC converter enabled.

The i.MX RT2660 shall offer two power supply source inputs i.e. a main supply domain input (V_{DD_PMU}) and a battery backup domain input (V_{BAT}). Fig 3 shows example power supply configuration scenarios to illustrate the voltage range that shall be supported on the various SoC power supply pins. USB_3V3 will always be powered from off-chip PMIC (similar to RT700).

For more details about the i.MX RT2660 integrated power management, please refer to Sections 0 and 6.9.3 for the power management units in main and battery backup domain, respectively.

Table 21. IC requirements traceability: power supply source requirements

AS/RS identifier	Content	Classification	Covered
iMXRT2660_PWR_2-3	Single 1.8V supply voltage rail	Must have	Yes
iMXRT2660_PWR_2-4	Single 3.3V supply voltage rail	Must have	Yes
iMXRT2660_PWR_2-5	1.8V and 3.3V supply voltage rails	Must have	Yes
iMXRT2660_PWR_2-6	Double Alkaline batteries	Must have	Yes
iMXRT2660_PWR_2-7	External PMIC with on-chip DCDC converter bypassed	Must have	Yes
iMXRT2660_PWR_2-8	External PMIC with on-chip DCDC converter enabled	Must have	Yes
iMXRT2660_PWR_2-9	The battery-backup domain shall draw power from the main supply, and it will switch to a standby voltage, which is supplied from a battery, to retain the content of the backup domain.	Must have	Yes

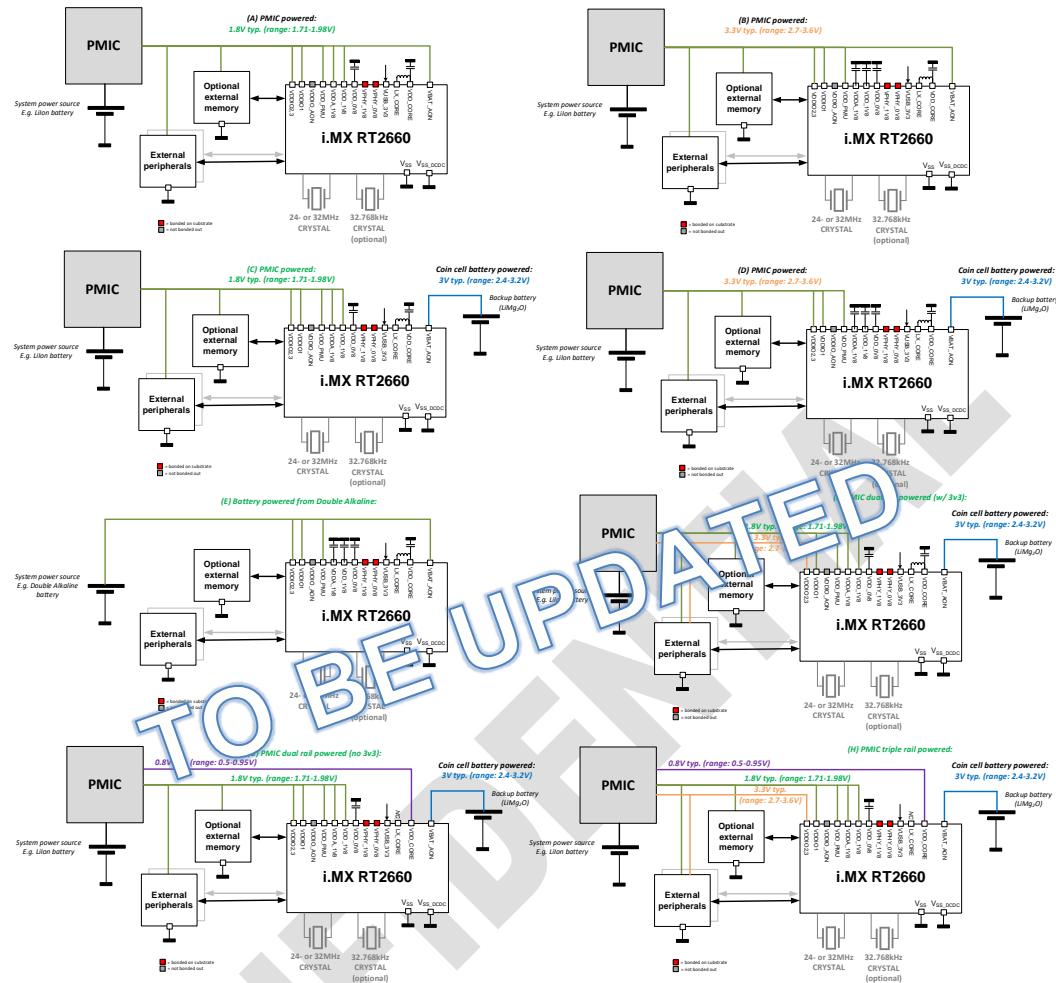


Fig 3. i.MX RT2660 example power supply configuration scenarios

5.3 Chip block diagram

Main sub-system boundaries of i.MX RT2660 are based on functionality, while accounting enabling a reusable and scalable architecture for future i.MX as outlined by the XEA-1 platform. Hence, the i.MX RT2660 is partitioning into three main functional domains as shown in Fig 4. These are:

- MAIN-COMPUTE domain;
- AUDIO-VISUAL domain;
- COMMON domain.

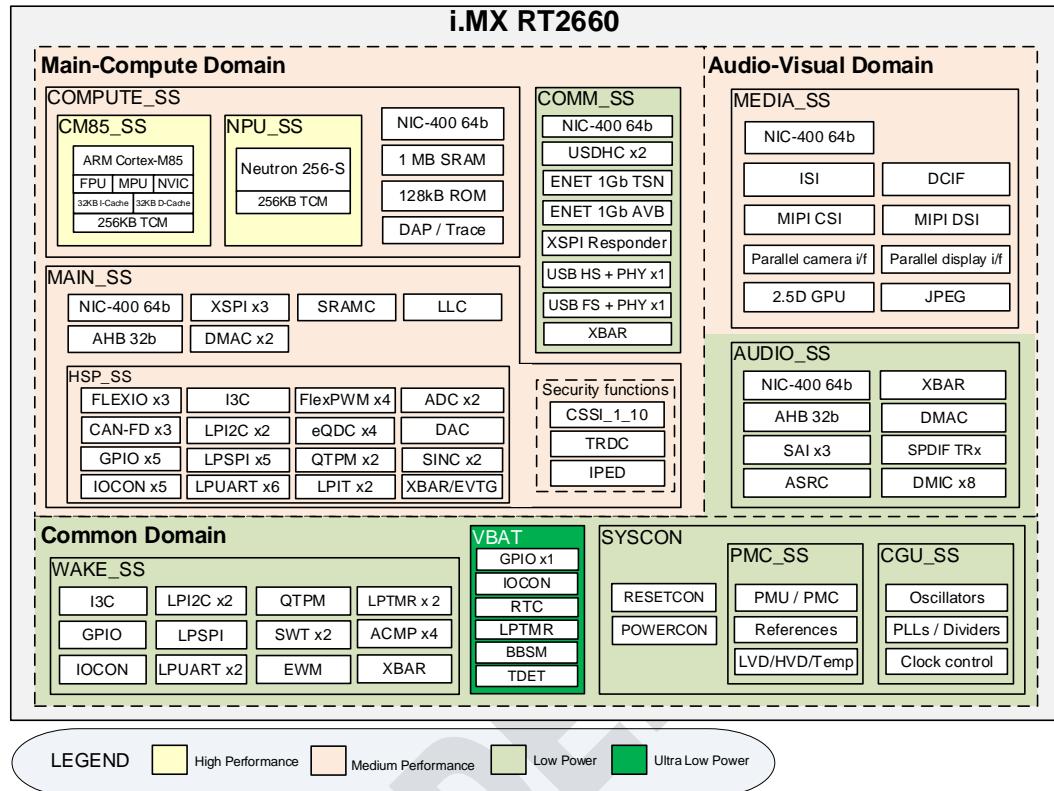


Fig 4. i.MX RT2660 high-level block diagram

The MAIN-COMPUTE Domain concerns the high/medium-performance CMPT_SS, MAIN_SS and the COMM_SS. The CMPT_SS includes:

- CPU subsystem, concerning the ARM Cortex-M85 processor and related blocks ;
- NPU subsystem, concerning the Neutron-256S machine learning inference sub-system ;
- A dedicated performance-optimized NIC-400 bus fabric ;
- On-chip total SRAM of up to 1.5 MB ;
- Boot ROM of 128 kB ;
- Other blocks like debug and trace.

The MAIN_SS includes:

- Medium-performance NIC-400 system bus fabric with DMA controller ;
- XSPI external memory interfaces supported by Last Level Cache ;
- A SRAM controller for external FPGA devices ;
- Medium-performance AHB multi-layer as peripheral bus fabric with DMA controller;
- CSSI_1_10 secure enclave, also known as Sentinel 110 ;
- A low-latency high-speed peripheral subsystem.

The COMM_SS concerns the medium-performance general connectivity interfaces.

The AUDIO-VISUAL Domain concerns the medium-performance MEDIA_SS and AUDIO_SS that include video/graphics- and audio related peripherals and interfaces.

The COMMON Domain containing the low-power peripheral subsystem and infrastructure IP:

- WAKE_SS as the low-power subsystem that includes a standard set of low-power communication peripherals, low-power timers, GPIO, analog comparators ;

- S Y S C O N , concerning the power management unit, clock generation unit, and related system control functionality such as power management-, root clock- and reset control ;
- V B A T _ S S , concerning the ultra-low-power Always-ON functionality including a Real-Time Clock (RTC), Lower Power Timer, GPIO, Battery Backed Security Module (BBSM) and Tamper Detect (TDET).

The LVD/HVD/AGDET and Temperature Detect should located in VBAT power domain.

The more detailed description of the SoC architecture and subsystems can be found in Chapter 0.

Table 22. **IC requirements traceability: general functional requirements (part-II)**

AS/RS identifier	Content	Classification	Covered
iMXRT2660_PWR_1-6	<p>The Device shall implement a Low-power subsystem, which includes low speed peripherals and timers. A small system DMA may be included in this subsystem.</p> <p>The peripherals shall have the ability to request DMA transfer without wakeup the main CPU from Sleep mode.</p> <p>At least one instances of following peripherals need to be included in the Low-Power subsystem: LPI2C, I3C, LPUART, LPSPI, TPM, LPTMR, CMP.</p>	Must have	Yes, WAKE_SS with DMAC in MAIN_SS
iMXRT2660_PWR_1-7	The Low-power subsystem can be functional in Sleep and even Deep Sleep modes while the rest of the SoC is clock gated or optionally power gated.	Must have	Yes, WAKE_SS
iMXRT2660_PWR_1-8	<p>The Device shall implement a battery-backup domain, which include RTC, tamper functions, backup register, and backup RAM.</p> <p>The battery-backup domain shall draw current from the main supply, and it will switch to a standby voltage, which is supplied from a battery, to retain the content of the backup domain.</p>	Must have	Yes VBAT in Common Domain

5.4 Modes of operation

This Section specifies the operating modes of the i.MX RT2660 IC.

5.4.1 Chip operating modes

The i.MX RT2660 IC implements the chip operating modes described by Table 23. The transition dependency between the different modes is illustrated in Fig 5. The chip operating modes are a mixture of hardware and software modes.

A detailed description of the hardware operating modes is provided in Section 8.4.

Table 23. **SoC operating modes**

Mode	Entry	Exit	Functionality
POR	hardware or software POR event	PMU and main oscillator ready	Transitory, constrained
BOOT	POR mode exit	boot process ready, or PMU NOK event	Transitory, constrained
ACTIVE	BOOT mode ready	Software event, PMU NOK event, or brownout condition	Resident, normal operation
STANDBY	Software	wake-up event or PMU NOK event	Resident, constrained

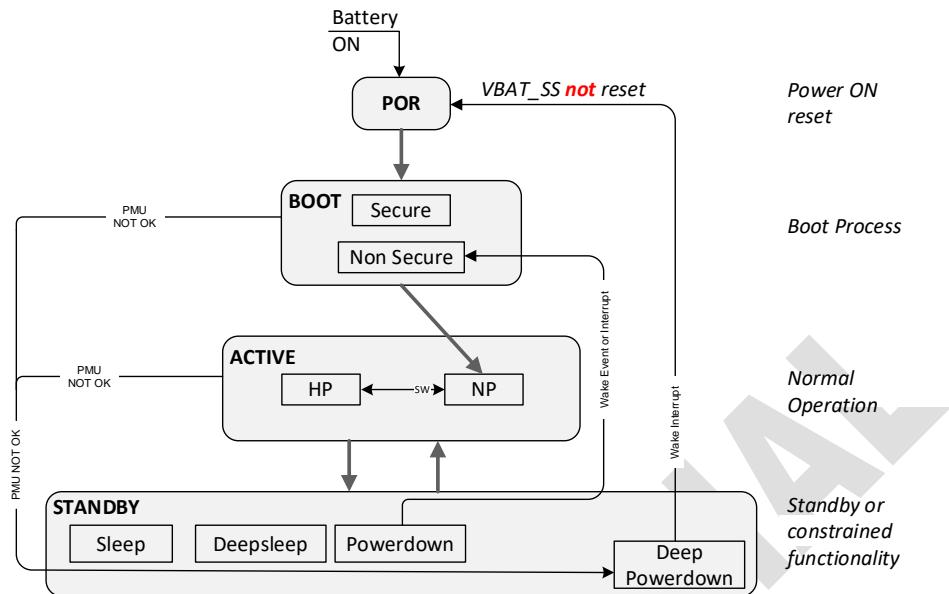


Fig 5. High-level overview of i.MX RT2660 operating modes

5.4.1.1 POR mode

The Power-On-Reset (POR) mode is the initial start-up mode of the i.MX RT2660 IC, which is started from a hardware power-on-reset condition (cold reset) or entered from a software power-on-reset (warm reset) condition. This mode is also entered from any other operating mode when the PMU output voltage(s) are found to be no longer reliable.

The POR mode is a transitional mode.

In POR mode, the PMU, oscillators (FRO192M and SXOSC) and main PLL are started. This process is completely performed under hardware control. The SoC shall be setup to operate in Normal Run mode setting at ZBB condition, i.e., CPU frequency shall run at 500MHz and main clock at 250MHz during BOOT mode. Any associated stored trim values for analog IP shall be automatically restored under hardware control; this may concern a subset of all stored trim values.

POR mode is terminated when all of the following conditions are met:

- PMU output voltages have reached their target set point ;
- Start-up of the oscillators and main PLL are completed ;
- A indication signal on POR mode completion shall be provided.

5.4.1.2 BOOT mode

This is a further start-up mode of the i.MX RT2660 IC, which succeeds the POR mode.

The BOOT mode is a transitional mode.

Different types of BOOT modes can be distinguished (refer to Chapter 10):

- Normal Boot ;
- Fast Boot.

The BOOT mode comprises two main phases: a first phase in which the application processor executes on-chip Boot ROM code, and a second phase where optionally a BOOTLOADER is downloaded to the i.MX RT2660 IC. Refer to Section 10.1.

The BOOT mode is terminated once the Boot ROM code has been executed, and code execution starts from on-chip RAM or external SPI Flash memory.

5.4.2 ACTIVE operation mode

This is the regular operational mode of the IC. All functionality is available unless constrained by software. When in Active mode, there exists two types of performance modes, namely the “High-Performance Run” and “Normal Run” mode. Refer to Table 24.

Table 24. **Active operation mode: Voltage and Frequency specification**

Mode	VDD_CORE [V]	High-performance domain				Low-power domain			
		compute_clk [MHz]	main_clk [MHz]	media_clk [MHz]	Body Bias	audio_clk [MHz]	comm_clk [MHz]	wake_clk [MHz]	Body Bias
High-Performance Run	0.9 typ.	>700,	F _{cmpt_clk} /2	F _{cmpt_clk} /2	FBB	≤ 200	≤ 200	≤ 100	ZBB
	0.945 max.	F _{max tbd}							
	0.81 min.								
Normal Run	0.8 typ.	≤ 700	≤ 350	≤ 350	FBB				
	0.88 max.	≤ 500	≤ 250	≤ 250	ZBB				
	0.72 min.								

Both High-Performance and Normal Run mode shall utilize FBB or ZBB for reaching the required performance level. The Normal Run mode shall operate at the typical supply voltage of 0.8V, while the High-Performance Run mode shall operate at the typical supply voltage of 0.9V. The SoC shall be designed for these default operation corners, i.e. 0.8V ±10% and 0.9V-10%/+5% (TODO, 0.9V-10%/+5% is not ready in standard cell library). Conventional timing signoff shall be performed during design phase. For enabling High-Performance Run mode, at least hold timing shall be closed for VDD_CORE voltage up to 0.945V in order to allow further maximum compute frequency increase determined by silicon characterization. The maximum compute frequency in High-Performance Run mode shall be determined during design phase, and based on what design team can achieve.

As default, the Normal Run mode with Zero Body Bias (ZBB) configuration shall be entered after exiting POR mode. The SoC shall remain in this mode during the boot process. After Boot has been completed, firmware shall take care of other SoC performance mode selection or bias setting.

The SoC shall be capable to move to a STANDBY mode regardless of the performance mode in which the SoC operates. After wake-up from STANDBY mode, the SoC shall resume operation in the same performance mode as it is left before entering STANDBY mode. More details on supported ACTIVE and STANDBY mode transitions can be found in Section 8.4.4.

Table 25. **IC requirements traceability: active operation mode requirements**

AS/RS identifier	Content	Classification	Covered
iMXRT2660_PWR_6-3	This device shall support dynamic voltage scaling on the main digital supply and dynamic frequency scaling on CM85, NPU, and system bus clocks.	Must have	Yes
iMXRT2660_PWR_6-4	Three operating points are: - 700MHz (CM85 & NPU), 350MHz (System bus) at 0.8V (nominal) - 500MHz (CM85 & NPU), 250MHz (System bus) at 0.7V (nominal) - 200MHz (CM85 & NPU), 100MHz (System bus) at 0.6V (nominal)	Must have	No <0.72V during Active operation Open: Req. update ongoing

5.4.3 STANDBY operation mode

STANDBY operation mode is intended as low-power standby mode and is invoked by software. Clock and hardware is chosen to be shutdown by firmware and sequenced in hardware.

There exists five types of standby operating modes. Each mode provides a different functional constraints, thereby allowing different trade-off between power consumption and wake-up time. A high-level overview of the different supported modes is provided in Table 26.

Table 26. **Standby operation mode: low-power standby modes**

Mode	V_{DDCORE} [V]	Body Bias	Clocks	CPU	Peripherals	SRAM retention	IO supply
Sleep	High Performance Run	FBB	Clocks shall be configured prior to entering Sleep mode	WFI	Peripheral operation shall be configured prior to entering Sleep mode	Full	on
	Normal Run	FBB/ZBB					
Deep Sleep	0.65 typ.	ZBB	All off except RTC and LPOSC	WFI	Clk gated and optional power-gated	Configurable up to full retention, 64kB default	on
Power Down	0.65 typ. 0.55 min.	ZBB	All off except RTC	Power-gated	Power-gated	up to 64kB	on
Deep Power Down	off	ZBB	All off except RTC	Power-gated	Power-gated	up to 2kB	off, except VBAT IO

The STANDBY mode is terminated after a wake-up event is triggered, or after a power-on reset condition. Typically, ACTIVE mode is resumed after wake-up from SLEEP or DEEP SLEEP modes. The wake-up from POWER DOWN and DEEP POWER DOWN modes require a non-secure or secure boot process, respectively. More details on supported transitions between ACTIVE and STANDBY modes can be found in Section 8.4.4.

5.4.4 Requirements traceability

Table 27. **IC requirements traceability: power mode requirements**

AS/RS identifier	Requirement	Classification	Covered
iMXRT2660_PWR_3-3	In Active power mode: - The main CPU core is on running. - Peripherals are functional, but they can be clock gated if the peripherals are not in use. - Voltage and bias are controlled by software.	Must have	Yes
iMXRT2660_PWR_3-4	In Sleep power mode: - The clock of the CPU core is gated off. - Peripheral clocks can be still running depending on the need of the application. - Voltage and bias are controlled by software	Must have	Yes
iMXRT2660_PWR_3-5	In Deep Sleep power mode: - The SoC is mostly in a static state where all clocks are stopped, but the state of the logic and memory is still maintained. - Deep Sleep may have different levels of granularity where Deep Sleep power is traded off for recovery time. - Some low-power peripherals, including ADC, low power timer, analog comparator, and DMIC audio detection, may optionally kept on from a local low frequency clock source. - Internal voltage is reduced as low as possible. - All memory are retained.	Must have	Yes ADC has no low speed peripheral clock source
iMXRT2660_PWR_3-6	In Power Down power mode: - The power to the logic are turned off via internal regulator and power switch. - A small amount of SRAM are retained for fast recovery. The size of SRAM retention is configurable by software. - The only power consumed by the main SoC is the leakage through the internal regulators and retained memory. - Wake up is done through an external pin or an RTC wake-up match.	Must have	Yes

AS/RS identifier	Requirement	Classification	Covered
iMXRT2660_PWR_3-7	In Deep Power Down power mode: - The power to the logic are turned off via internal regulator. - The only power consumed by the main SoC is the leakage through the internal regulators. - Wake up is done through an external pin or an RTC wake-up match. - Full reboot is needed when the main power supply is re-applied.	Must have	Full reboot needed Open: Req update ongoing

5.5 Programmer's view

The section describes the i.MX RT2660 memory map, interrupt channels, DMA channels and reset-safe registers.

5.5.1 System memory map

The detailed RT2660 SoC memory map (i.MXRT2660_MemoryMap_v<version>.xlsx) can be found at the following location

- In share point: [Memory Map](#)
- Or Design Sync: [Data Sheet](#)  [Folder memory_map \(nxp.com\)](#)

Table 28 shows a high-level overview of the system memory map organization of the i.MX RT2660 SoC. It is based on the aligned XEA-1 platform memory map. The secure memory slots in the table have an offset of +1000_0000h to the start and end address for their corresponding non-secure address slots. The reserved slots have not been shown in this high-level overview.

[TO SoC integration and Verification]: If there is any mismatch between Table 28 and detailed RT2660 SoC memory map in share point or Design Sync, please reference to RT2660 SoC memory map in share point or Design Sync as single and golden source for SoC integration and Verification.

Table 28. **i.MX RT2660 system memory map**

Allocation	Start address	End address	Size	Description
CPU I-TCM alias	0000_0000	0001_FFFF	128KB	Non-Secure alias for Cortex-M85 I-TCM
	1000_0000	1001_FFFF	128KB	Secure alias for Cortex-M85 I-TCM
CPU D-TCM alias	2000_0000	2001_FFFF	128KB	Non-Secure alias for Cortex-M85 D-TCM
	3000_0000	3001_FFFF	128KB	Secure alias for Cortex-M85 D-TCM
NPU TCM	2080_0000	2083_FFFF	256KB	Non-Secure alias for NPU TCM
	3080_0000	3083_FFFF	256KB	Secure alias for NPU TCM
NPU MMR	2090_0000	2090_0FFF	4KB	Non-Secure alias for NPU MMR
	3090_0000	3090_0FFF	4KB	Secure alias for NPU MMR
NPU DTCM-Data	2090_8000	2090_BFFF	16KB	Non-Secure alias for NPU DTCM-Data
	3090_8000	3090_BFFF	16KB	Secure alias for NPU DTCM-Data
NPU DTCM-Ring	2090_C000	2090_FFFF	16KB	Non-Secure alias for NPU DTCM-Ring
	3090_C000	3090_FFFF	16KB	Secure alias for NPU DTCM-Ring
NPU ITCM	2091_0000	2091_FFFF	64KB	Non-Secure alias for NPU ITCM
	3091_0000	3091_FFFF	64KB	Secure alias for NPU ITCM
CPU I-TCM 	210E_0000	210F_FFFF	128KB	Remapped to 0x0000_0000
	310E_0000	310F_FFFF	128KB	Remapped to 0x1000_0000
CPU D-TCM	2110_0000	2111_FFFF	128KB	Remapped to 0x2000_0000
	3110_0000	3111_FFFF	128KB	Remapped to 0x3000_0000

Allocation	Start address	End address	Size	Description
CPU I-TCM alias2	21FC_0000	21FD_FFFF	128KB	2 nd Non-Secure alias for Cortex-M85 I-TCM
	31FC_0000	31FD_FFFF	128KB	2 nd Secure alias for Cortex-M85 I-TCM
CPU D-TCM alias2	21FE_0000	21FF_FFFF	128KB	2 nd Non-Secure alias for Cortex-M85 D-TCM
	31FE_0000	31FF_FFFF	128KB	2 nd Secure alias for Cortex-M85 D-TCM
SRAM P0	2200_0000	2200_FFFF	64KB	Partition 0 from On-Chip RAM (Non-Secure)
	3200_0000	3200_FFFF	64KB	Partition 0 from On-Chip RAM (Secure)
SRAM P1	2201_0000	2201_FFFF	64KB	Partition 1 from On-Chip RAM (Non-Secure)
	3201_0000	3201_FFFF	64KB	Partition 1 from On-Chip RAM (Secure)
SRAM P2	2202_0000	2202_FFFF	64KB	Partition 2 from On-Chip RAM (Non-Secure)
	3202_0000	3202_FFFF	64KB	Partition 2 from On-Chip RAM (Secure)
SRAM P3	2203_0000	2203_FFFF	64KB	Partition 3 from On-Chip RAM (Non-Secure)
	3203_0000	3203_FFFF	64KB	Partition 3 from On-Chip RAM (Secure)
SRAM P4	2204_0000	2205_FFFF	128KB	Partition 4 from On-Chip RAM (Non-Secure)
	3204_0000	3205_FFFF	128KB	Partition 4 from On-Chip RAM (Secure)
SRAM P5	2206_0000	2207_FFFF	128KB	Partition 5 from On-Chip RAM (Non-Secure)
	3206_0000	3207_FFFF	128KB	Partition 5 from On-Chip RAM (Secure)
SRAM P6	2208_0000	2209_FFFF	128KB	Partition 6 from On-Chip RAM (Non-Secure)
	3208_0000	3209_FFFF	128KB	Partition 6 from On-Chip RAM (Secure)
SRAM P7	220A_0000	220B_FFFF	128KB	Partition 7 from On-Chip RAM (Non-Secure)
	320A_0000	320B_FFFF	128KB	Partition 7 from On-Chip RAM (Secure)
SRAM P8	220C_0000	220D_FFFF	128KB	Partition 8 from On-Chip RAM (Non-Secure)
	320C_0000	320D_FFFF	128KB	Partition 8 from On-Chip RAM (Secure)
SRAM P9	220E_0000	220F_FFFF	128KB	Partition 9 from On-Chip RAM (Non-Secure)
	320E_0000	320F_FFFF	128KB	Partition 9 from On-Chip RAM (Secure)
NPU TCM alias2	2210_0000	2213_FFFF	256KB	2 nd Non-Secure alias for NPU TCM
	3210_0000	3213_FFFF	256KB	2 nd Secure alias for NPU TCM
XSPI0 Rx buffer	2400_0000	2400_03FF	1KB	XSPI0 Rx buffer (Non-Secure)
	3400_0000	3400_03FF	1KB	XSPI0 Rx buffer (Secure)
XSPI1 Rx buffer	2410_0000	2410_03FF	1KB	XSPI1 Rx buffer (Non-Secure)
	3410_0000	3410_03FF	1KB	XSPI1 Rx buffer (Secure)
XSPI2 Rx buffer	2420_0000	2420_03FF	1KB	XSPI2 Rx buffer (Non-Secure)
	3420_0000	3420_03FF	1KB	XSPI2 Rx buffer (Secure)
CSSI IMEM_XIMEM alias	2480_0000	2481_7FFF	96KB	Non-Secure CSSI IMEM+XIMEM Alias
	3480_0000	3481_7FFF	96KB	Secure CSSI IMEM+XIMEM Alias
CSSI DMEM alias	2482_0000	2482_FFFF	64KB	Non-Secure CSSI DMEM Alias
	3482_0000	3482_FFFF	64KB	Secure CSSI DMEM Alias
SRAMC CS0	2500_0000	2501_FFFF	128KB	SRAMC CS0 (Non-Secure)
	3500_0000	3501_FFFF	128KB	SRAMC CS0 (Secure)

Allocation	Start address	End address	Size	Description
SRAMC CS 	2502_0000	2503_FFFF	128KB	SRAMC CS1 (Non-Secure)
	3502_0000	3503_FFFF	128KB	SRAMC CS1 (Secure)
AUDIO_SS SRAM	2800_0000	2800_1FFF	8KB	AUDIO_SS SRAM (Non-Secure)
	3800_0000	3800_1FFF	8KB	AUDIO_SS SRAM (Secure)
-	4000_0000	4FFF_FFFF	256MB	See peripheral memory map
	5000_0000	5FFF_FFFF	256MB	
XSPI1_XEX	6000_0000	67FF_FFFF	128MB	XSPI1 access (Non-Secure)
	7000_0000	77FF_FFFF	128MB	XSPI1 access (Secure)
XSPI1_XEX Cached	6800_0000	6FFF_FFFF	128MB	XSPI1 LLC cached access (Non-Secure)
	7800_0000	7FFF_FFFF	128MB	XSPI1 LLC cached access (Secure)
XSPI2_XEX	8000_0000	87FF_FFFF	128MB	XSPI2 access (Non-Secure)
	9000_0000	97FF_FFFF	128MB	XSPI2 access (Secure)
XSPI2_XEX Cached	8800_0000	8FFF_FFFF	128MB	XSPI2 LLC cached access (Non-Secure)
	9800_0000	9FFF_FFFF	128MB	XSPI2 LLC cached access (Secure)
XSPI0_CTR_GCM	A000_0000	AFFF_FFFF	256MB	XSPI0 access (Non-Secure)
	B000_0000	BFFF_FFFF	256MB	XSPI0 access (Secure)
XSPI0_CTR_GCM Cached	C000_0000	CFFF_FFFF	256MB	XSPI0 LLC cached access (Non-Secure)
	D000_0000	DFFF_FFFF	256MB	XSPI0 LLC cached access (Secure)
Private Peripheral Bus (internal)	E000_0000	E003_FFFF	256KB	M85 IPPB
Private Peripheral Bus (external)	E004_0000	E00F_FFFF	768KB	M85 EPPB
CSSI	E7FE_0000	E7FF_7FFF	96KB	CSSI internal space: IMEM+XIMEM
CSSI	E800_0000	E800_FFFF	64KB	CSSI internal space: DMEM

5.5.2 Peripheral memory map

The detailed RT2660 peripheral memory map (i.MXRT2660_MemoryMap_v<version>.xlsx) can be found at the following location

- In share point: [Memory Map](#).
- Or Design Sync: [Data Sheet for Folder memory_map \(nxp.com\)](#)

Table 29 shows a high-level overview of the peripheral memory map organization of the i.MX RT2660 SoC. It is based on the aligned XEA-1 platform memory map. The secure memory slots in the table have an offset of +1000_0000h to the start and end address for their corresponding non-secure address slots. The reserved slots have not been shown in this high-level overview.

[TO SoC integration and Verification]: If there is any mismatch between Table 29 and detailed RT2660 peripheral memory map in share point or Design Sync, please reference to RT2660 peripheral memory map in share point or Design Sync as single and golden source for SoC integration and Verification.

Table 29. High-level overview of i.MX RT2660 peripheral memory map

Allocation	Start address	End address	Size [KB]	Description
MAIN_SS registers	4000_0000	406F_FFFF	7168	Access to MAIN_SS PBridge (Non-Secure)
	5000_0000	506F_FFFF	7168	Access to MAIN_SS PBridge (Secure)
MAIN_SS GPV	4070_0000	407F_FFFF	1024	Access to NIC_MAIN GPV (Non-Secure)
	5070_0000	507F_FFFF	1024	Access to NIC_MAIN GPV (Secure)
Debug Mailbox	41E0_0000	41E0_FFFF	64	Debug Mailbox (Non-Secure)
	51E0_0000	51E0_FFFF	64	Debug Mailbox (Secure)
CoreSight Debug	41F0_0000	41FF_FFFF	1024	CoreSight Debug (Non-Secure)
	51F0_0000	51FF_FFFF	1024	CoreSight Debug (Secure)
HSP_SS PBRIDGE0	4200_0000	427F_FFFF	8192	Access to HSP_SS PBridge0 (Non-Secure)
	5200_0000	527F_FFFF	8192	Access to HSP_SS PBridge0 (Secure)
HSP_SS PBRIDGE1	4280_0000	42FF_FFFF	8192	Access to HSP_SS PBridge1 (Non-Secure)
	5280_0000	52FF_FFFF	8192	Access to HSP_SS PBridge1 (Secure)
HSP_SS GPIO0	4380_0000	4380_FFFF	64	Access to HSP.GPIO0 (Non-Secure)
	5380_0000	5380_FFFF	64	Access to HSP.GPIO0 (Secure)
HSP_SS GPIO1	4381_0000	4381_FFFF	64	Access to HSP.GPIO1 (Non-Secure)
	5381_0000	5381_FFFF	64	Access to HSP.GPIO1 (Secure)
HSP_SS GPIO2	4382_0000	4382_FFFF	64	Access to HSP.GPIO2 (Non-Secure)
	5382_0000	5382_FFFF	64	Access to HSP.GPIO2 (Secure)
HSP_SS GPIO3	4383_0000	4383_FFFF	64	Access to HSP.GPIO3 (Non-Secure)
	5383_0000	5383_FFFF	64	Access to HSP.GPIO3 (Secure)
HSP_SS GPIO4	4384_0000	4384_FFFF	64	Access to HSP.GPIO4 (Non-Secure)
	5384_0000	5384_FFFF	64	Access to HSP.GPIO4 (Secure)
CMPT_SS registers	4400_0000	446F_FFFF	7168	Access to CMPT_SS PBridge (Non-Secure)
	5400_0000	546F_FFFF	7168	Access to CMPT_SS PBridge (Secure)
CMPT_SS GPV	4470_0000	447F_FFFF	1024	Access to NIC_MEM GPV (Non-Secure)
	5470_0000	547F_FFFF	1024	Access to NIC_MEM GPV (Secure)
WAKE_SS registers	4600_0000	467F_FFFF	8192	Access to WAKE_SS registers (Non-Secure)
	5600_0000	567F_FFFF	8192	Access to WAKE_SS registers (Secure)
AUDIO_SS registers	4800_0000	481F_FFFF	2048	Access to AUDIO_SS PBridge (Non-Secure)
	5800_0000	581F_FFFF	2048	Access to AUDIO_SS PBridge (Secure)
AUDIO_SS SPDIF	4860_0000	4861_FFFF	128	Access to SPDIF data interface (Non-Secure)
	5860_0000	5861_FFFF	128	Access to SPDIF data interface (Secure)
COMM_SS registers	4A00_0000	4A6F_FFFF	7168	Access to COMM_SS PBridge (Non-Secure)
	5A00_0000	5A6F_FFFF	7168	Access to COMM_SS PBridge (Secure)
COMM_SS GPV	4A70_0000	4A7F_FFFF	1024	Access to COMM_SS GPV (Non-Secure)
	5A70_0000	5A7F_FFFF	1024	Access to COMM_SS GPV (Secure)
MEDIA_SS registers	4C00_0000	4C6F_FFFF	7168	Access to MEDIA_SS PBridge (Non-Secure)
	5C00_0000	5C6F_FFFF	7168	Access to MEDIA_SS PBridge (Secure)

Allocation	Start address	End address	Size [KB]	Description
MEDIA_SS GPV	4C70_0000	4C7F_FFFF	1024	Access to MEDIA_SS GPV (Non-Secure)
	5C70_0000	5C7F_FFFF	1024	Access to MEDIA_SS GPV (Secure)

For the detailed peripheral assignment for a i.MX RT2660 sub-system, please refer to the architecture specification document for the given sub-system [4] [8] [3] [6] [7]

5.5.3 Interrupt vectors

The detailed RT2660 interrupt vector table (i.MXRT2660_IRQ_v<version>.xlsx) can be found at the following location: [Interrupts DMA CrossTrigger](#).

The interrupt vector table has been aligned at XEA-1 platform level, thereby covering the need for various RT2K products. In total, the i.MX RT2660 interrupt vector table contains 16 processor-dedicated interrupts and 309 further interrupts for the other building blocks. Hence, it may appear that the numbering of interrupts is not continuous for i.MX RT2660 due to reservation of interrupt slots for other RT2K products.

For further details on interrupts for a i.MX RT2660 sub-system, please refer to the architecture specification document for that given sub-system [4] [8] [3] [6] [7].

5.5.4 DMA channels

The i.MX RT2660 controller three DMA controllers in total. Two DMA controllers reside in the MAIN_SS (MAIN.DMA0: eDMA5, MAIN.DMA1: eDMA3) and one resides in the AUDIO_SS (AUDIO.DMA0: eDMA3). For each DMA controller in the i.MX RT2660, the detailed DMA channels table (i.MXRT2660_DMA_v<version>.xlsx) can be found at the following location, [Interrupts DMA CrossTrigger](#). Organized per subsystem as per XEA-1 alignment: [XEA1_DmaMap.xlsx](#)

The DMA channel allocation has been aligned at XEA-1 platform level, thereby covering the need for various RT2K products. Hence, it may appear that the numbering of DMA channels is not continuous due to reservation of given DMA channels in other RT2K products than i.MX RT2660.

6. SoC Architecture

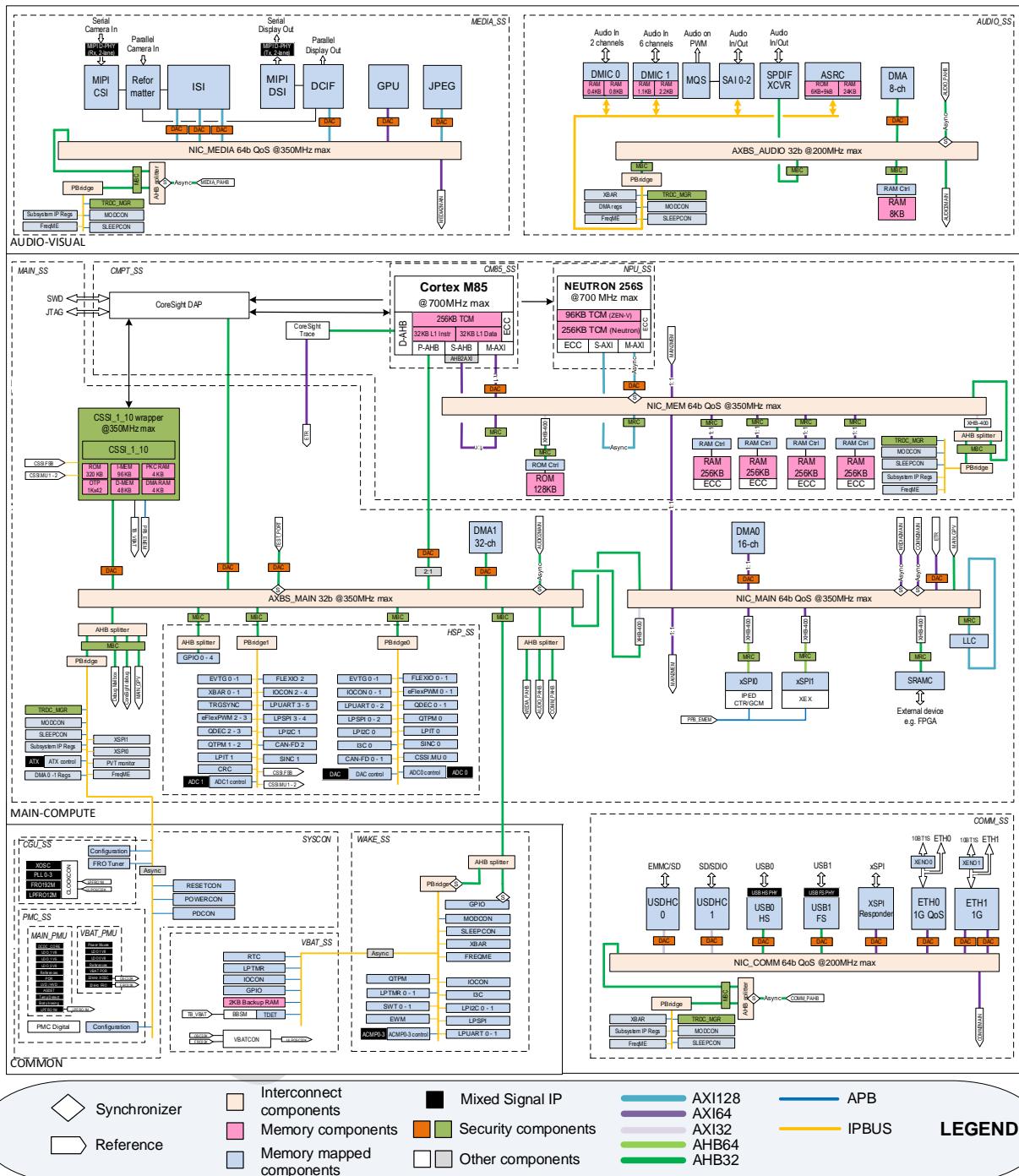
This Chapter provides a functional description of the i.MX RT2660 SoC architecture.

6.1 Overview

6.1.1 SoC functional partitioning

The i.MX RT2660 SoC architecture is based on a modular architecture comprising of multiple functional domains, as deduced from the XEA-1 platform. Each functional domain contains one or more subsystems, each with its own bus fabric and performance target for achieving the best compromise between SoC performance and power consumption.

Fig 6 shows a high-level overview of i.MX RT2660's SoC architecture; one can distinguish three main functional domains, namely MAIN-COMPUTE, AUDIO-VISUAL and COMMON Domain, and their respective subsystems.

**Fig 6. i.MX RT2660 SoC architecture functional diagram**

The MAIN-COMPUTE Domain is the heart of the i.MX RT2660. The CMPT_SS contains the ARM Cortex-M85 core that controls the rest of the chip. It further contains the NPU, a NIC-400 64-bit bus fabric (NIC_MEMORY) and the on-chip shared SRAM. The MAIN_SS implements the central part of the i.MX RT2660, connecting the various subsystems; it contains a NIC-400 64-bit fabric (NIC_MAIN), a AHB 32-bit bus fabric (AXBS_MAIN), a AHB bus fabric (AXBS_TDBG), DMA controller, CSPI

wrapper, XSPI external memory interfaces, and other related components. The i.MX RT2660 utilizes a hierarchical bus fabric organization where NIC_MEM implements a first-level for connection to on-chip memory, and NIC_MAIN implementing a second-level for connecting the various subsystems. The separation of NIC_MEM and NIC_MAIN allows for further system performance optimization by enabling high-performance compute blocks (i.e. Cortex-M85 and Neutron NPU) to interface with on-chip SRAM directly via the small-sized NIC_MEM; other subsystems interact with the on-chip SRAM via the connection between NIC_MEM and NIC_MAIN. The motivation for separating NIC_MAIN and AXBS_MAIN is to create a AXI-focused central bus fabric for streaming data next to a AHB low-latency peripheral section, each of them performance and size optimized. The COMM_SS contains the high-performance general connectivity interfaces that are connected to the MAIN_SS via a dedicated NIC-400 64-bit bus fabric (NIC_COMM). The motivation for separating the COMM_SS from the MAIN_SS is two-fold: 1) to allow for further system power/performance optimization (power management control), and 2) to enable re-use of this subsystem into future i.MX RT2K products according to XEA-1 platform vision. The performance/latency impact of such bus fabric separation is expected to be minimal.

The AUDIO-VISUAL Domain contains the MEDIA_SS and AUDIO_SS. The MEDIA_SS contains graphics/video related peripherals and interfaces, and a dedicated NIC-400 64-bit bus fabric. The AUDIO_SS contains audio related peripherals and interfaces, and a dedicated NIC-400 32-bit bus fabric. Both subsystems are connected to the MAIN-COMPUTE Domain. The motivation for the different subsystems is the same as mentioned for the COMM_SS above.

The COMMON Domain contains various low-power functionality that do not have high-speed requirements while being able to operate during standby mode. The WAKE_SS is the main subsystem in the COMMON Domain to which all others are connected to. Instead of a NIC-400, an AHB bus fabric has been used to interconnect the lower-performance low-power peripherals. The WAKE_SS is connected to the MAIN_SS. The other subsystems in the COMMON Domain are: SYSCON and VBAT_SS.

A detailed description of each domain and subsystem can be found from Section 0 onwards.

Table 30. **IC requirements traceability: SoC infrastructure requirements**

AS/RS identifier	Content	Classification	Covered
iMXRT2660_SCI_1-2	Bus interconnection	Heading	-
iMXRT2660_SCI_1-3	The bus interconnection shall be structured in a way that any bus initiators can access any memory location in the SoC, with few exceptions like boot ROM or caches.	Must have	Yes, see Fig 6
iMXRT2660_SCI_1-4	The bus interconnection shall be optimized for low latency access as specified in requirement iMXRT2660_MEM_1-7.	Must have	Yes as proposed
iMXRT2660_SCI_1-5	The bus interconnections should have multiple frequency domains and rate adaption capabilities, so that user can run each domain (or subsystem) at a different frequency. For example, the low power subsystem, which include low-speed serial peripherals, can run at a sub-divided frequency of the main interconnect.	Must have	Yes, see Fig 6
iMXRT2660_SCI_1-6	The bus interconnection shall be partitioned in a way that the low power subsystem and audio subsystem can be active, including DMA transfer between peripheral FIFOs and on-chip SRAM, while the rest of the SoC is clock gated in low power modes.	Must have	Yes, with SRAM in subsystems
iMXRT2660_SCI_1-7	The bus interconnects shall have sufficient buffers size and flexible arbitration scheme(s) for interconnect ports that have heavy bus traffic from multiple bus initiators; for example, the slave ports to on-chip SRAM or xSPI controller.	Must have	To be verified during design phase

AS/RS identifier	Content	Classification	Covered
iMXRT2660_SCI_1-8	The bus interconnects shall support Quality of Service (QoS) to regulate and prioritize the bus traffic so that the latency and bandwidth requirements are met for critical bus initiators in a given use case.	Must have	Yes for NIC_MEM/MAIN/MEDIA
iMXRT2660_SCI_2-1	DMA	Heading	-
iMXRT2660_SCI_2-2	This processor shall include multiple DMA engines.	Must have	Yes
iMXRT2660_SCI_2-3	One small DMA, shall perform DMA transfers between serial ports and local memory with minimum intervention from the CPU.	Must have	DMA1 (MAIN_SS), 32 channels
iMXRT2660_SCI_2-4	This DMA shall be able to wake up from Sleep or Deep Sleep mode to service DMA transfer without CPU intervention.	Must have	Targeted w/ eDMAv3 async feature
iMXRT2660_SCI_2-5	Another DMA, shall perform DMA transfers between audio peripherals and memory with minimum intervention from the CPU.	Must have	AUDIO.DMA0
iMXRT2660_SCI_2-6	This DMA shall support transfer of audio samples from audio peripherals to the main CPU data TCM and vice-versa in low latency less than 15 bus clock cycles overhead).	Must have	
iMXRT2660_SCI_2-7	The Device shall include at least one general purpose system DMA to perform data transfer between peripherals and memory or between memory locations.	Must have	Yes
iMXRT2660_SCI_2-8	DMA requests of all peripherals in the SoC that require DMA transfer shall be mapped	Must have	Yes
iMXRT2660_SCI_2-9	The system DMA(s) shall support operation worst case concurrent data transfers without peripheral FIFO underrun or overflow including during maximum CPU induced load.	Must have	Yes
iMXRT2660_SCI_3-1	Cross trigger	Heading	-
iMXRT2660_SCI_3-2	The Device shall implement a cross-trigger network which allows software to configure the trigger inputs and output for various peripherals in the SoC.	Must have	Yes
iMXRT2660_SCI_3-3	The Cross trigger network shall include at least 1x instance of XBARA.	Must have	Yes
iMXRT2660_SCI_3-4	The Cross trigger network shall include at least 2x instance of XBARB.	Must have	Yes
iMXRT2660_SCI_3-5	The Cross trigger network shall include at least 8x instances of AOIs.	Must have	Yes

6.1.2 SoC clocking strategy

The i.MX RT2660 SoC architecture is based on a design philosophy that simplifies clock domain crossings as much as possible, for minimizing their impact on bandwidth and latency. The CPU_SS and NPU_SS run at maximum clock frequency, independently from each other. The CMPT_SS building blocks typically operate at frequencies being a multiple of 2 times lower than the CPU clock frequency; this also applies to building blocks located within the MAIN_SS. Consequently, these building blocks face an elevated power consumption when the SoC operates in High-Performance Run mode, which is considered acceptable. The CMPT_SS and the MAIN_SS run synchronous to each other, while the NPU_SS runs asynchronously. The motivation for this is two-fold: 1) to allow CPU clock to be overdriven without a dependency to the NPU clock, and 2) an expected benefit for timing closure during SoC design. However, this comes at a latency penalty for the NPU_SS during system access due to required synchronization overhead. Current assumption is that we can allow this as no real-time process is running on NPU.

The MEDIA_SS in the AUDIO-VISUAL Domain runs asynchronous to MAIN_SS. The motivation is an expected benefit for SoC design concerning time closure. However, it comes at a latency penalty for the MEDIA_SS when accessing memory due to required synchronization overhead. As

MEDIA_SS traffic patterns typically concern a sequential data traffic pattern instead of random access traffic pattern (aside from GPU for which a solution is being investigated). Current assumption is that we can provision sequential data traffic for which asynchronous connection seems acceptable.

The COMM_SS and the WAKE_SS in the COMMON Domain do not contain performance-critical components, and run at a reduced clock frequency that is not effected by any change in compute clock frequency. This to simplify the usage of the low-power peripheral blocks in applications, at the expense of the synchronizers between domains. The COMM_SS and the WAKE_SS are running as asynchronous to the rest of the chip.

The AUDIO_SS is designed to run either at a reduced clock frequency or at a multiple of the audio sampling clock ($n \times F_s$). The subsystem is running asynchronous to the rest of the chip.

The i.MX RT2660 contains several high-speed interface IPs that reside in the MAIN-COMPUTE Domain or in the MEDIA subsystem. This concerns XSPI (up to 500MHz), uSDHC (up to 400MHz) and 1Gbit Ethernet (up to 125MHz). The high frequency IP clocks are distributed to each high-speed interface IP separately for maximum flexibility.

More details on the clock generation can be found in Chapter 7.

6.1.3 SoC memory strategy

The i.MX RT2660 is a low-cost general-purpose MCU that targets a wide range of applications. Its memory system should be designed for a balance of sufficient on-chip memory and efficient external memory needs. Fig 7 illustrates the envisioned memory hierarchy for the SoC, including targeted memory access performance in terms of cycle count.

- Level 1 Memory: this concerns caches and tightly coupled memories (TCMs) for ARM Cortex-M85 and Neutron N256S NPU, with single cycle memory access ;
- Level 2 Memory: On-chip shared SRAM of 1MB and ROM of 128KB. Access to those memories shall be within 2-8 cycles Optionally, the TCMs can be statically configured as Level 2 Memory ;
- Level 3 Memory: External memories such as NOR/NAND Flash, pSRAM or SD cards. Accessing such memories will take more than 20 cycles.

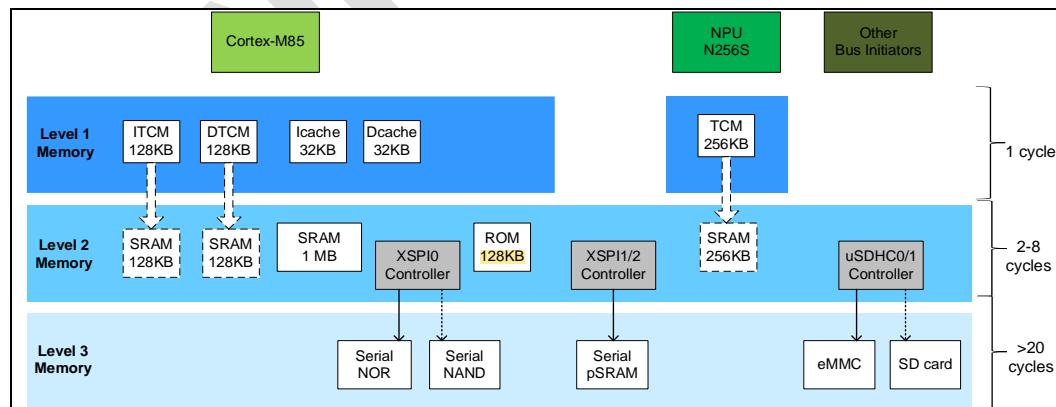


Fig 7. i.MX RT2660 SoC memory hierarchy diagram

The i.MX RT2660 SoC architecture is based on a design philosophy where the high-performance subsystems have direct access to an on-chip shared SRAM of 1MB via four memory ports concurrently. This is to offer a flexible memory allocation for different use-cases while minimizing latency of SRAM access for the high-performance subsystems.

This on-chip shared SRAM is connected to a size-optimized NIC-400 bus fabric (NIC_MEM) to which only a limited amount of bus masters have access to, namely CPU_SS, NPU_SS and MAIN_SS. Other bus masters can access the on-chip shared SRAM via NIC_MAIN within the MAIN_SS, thereby avoiding further NIC_MEM complexity at the minimum latency cost. Furthermore, NIC_MEM supports multiple SRAM ports such that multiple bus masters have concurrent access to SRAM partitions to the benefit of improved overall system performance.

More details on the memory subsystem can be found in Section 0.

Table 31. **IC requirements traceability: memory general requirements**

AS/RS identifier	Content	Classification	Covered
iMXRT2660_MEM_1-5	The memory system and bus interconnects should be implemented in a way that any bus initiator can access to any memory target, with the except of dedicated memory targets like cache memory or boot ROM.	Must have	Yes NIC_MEM & NIC_MAIN
iMXRT2660_MEM_1-6	Level 1 memories are tightly coupled to their respective core, so the core can access their level 1 memories in zero-wait state.	Must have	Yes, see Section 0

iMXRT2660_MEM_1-7	<p>Level 2 memory includes.</p> <ul style="list-style-type: none"> - System SRAM, - Cortex-M85 TCMs accessible by other bus initiators in the SoC - NPU TCM repurposed as general purpose SRAM when NPU is not used. - Prefetch buffers in xSPI controllers. <p>Access latency from any bus master to L2 memory should not more than 8 cycles of bus clock.</p>	Must have	<p>Yes for most. No for NPU TCM latency due to async</p>
iMXRT2660_MEM_1-8	<p>Level 3 memory are supported external memories supported. This processor shall support following external memories:</p> <ul style="list-style-type: none"> - Serial NOR flash via xSPI controller. - Serial NAND flash via xSPI controller. - eMMC flash via uSDHC controller. - SD removable card via uSDHC controller. - Serial pSRAM via xSPI controller. <p>Access latency to external memory are typically 20 clock cycles or more depending on memory type and operation speed.</p>	Must have	<p>Yes XSPI & uSDHC interfaces</p>

6.1.4 SoC architectural design strategy

The SoC architecture has defined new 22FDX+ IP targets with first-time deployment in RT2660.

- New NXP 22FDX+ EFVSPRAM compiler and compiler specification setting for i.Mx RT2K. Improvement of all SRAM PPA versus off-the-shelf offerings [15] ;
- New NXP 22FDX+ Body Bias generator and specification setting for improved Body Bias IP PPA and application usage versus off-the-shelf offerings [16] ;
- New small-size optimized IO Library for reduced die area – **Open: Synopsys or NXP IO**

The RT2660 SoC functional architecture has been designed to ease SoC integration.

- New XEA-1 architecture foundation with configurable subsystem partitions and common plumbing for enabling re-use across i.Mx RT2K products ;
- Introducing analog macro blocks (PMU, CGU) with core supply level interfaces to reduce SoC integration complexity, simplify SoC backend design and achieving SoC PPA ;
- New XEA-1 based clocking scheme that simplifies SoC clock tree design & timing closure as compared to legacy i.Mx RT devices.

The RT2660 SoC functional architecture has been designed to improve SoC performance.

- Improved SoC system performance in range of 15-20% when executing from OCSRAM, thanks to CPU-Bus synchronous interface versus legacy asynchronous approach ;
- Improved system performance with AXI/AHB bus infrastructure partitioning to optimize for streaming data and peripheral applications, where applicable ;
- Improved SoC system performance to external memory via xSPI pSRAM, thanks to the introduction of Last-Level Cache (LLC) to address xSPI protocol overheads ;
- High-speed peripherals subsystem to achieve low-latency and high-performance peripheral operation ;
- Low-power WAKE_SS to support low-power application use-cases at the expense of higher latency peripheral access.

6.1.5 SoC architectural trade-offs & compromises

The proposed RT2660 SoC power architecture has been designed as a balanced trade-off between SoC area, low-power and SoC integration complexity.

- Common single digital core supply rail (VDD_CORE) for logic and memories, to save PMU and power grid complexity associated with multiple generated core supplies. This comes at the cost of elevated SoC power consumption ;
- Deployment of FBB/ZBB in high-performance SoC regions only, to save power routing and reduce integration complexity ;

- No deployment of RBB for leakage reduction in low-power domains, to save power routing complexity. Only ZBB is deployed at a higher leakage costs than in case of RBB ;
- State-retentive power gating deployment for selected SoC functionalities, in order to achieve competitive standby leakage in absence of RBB ;
- New generation of power-optimized clock sources (i.e. oscillators & PLLs) while improved design for high clock accuracy for high-performance interfaces (i.e. xSPI, eMMC/SD/SDIO and Ethernet) ;
- New power-optimized XEA-1 based clocking scheme, trading-off excessive flexibility for reduced global clock power in the range of 30-60% versus RT1180 scheme.

The following compromises had to be made as consequence of pushback from SysEng, SysAppl, SW and SoC Design teams based on legacy RT 4-digit experiences and legacy design practices.

- Omitting ZEN-V Boot/System Mngr core due to design effort and schedule, and no acceptance of the benefits such core could offer [17] ;
- Clock asynchronous NPU to rest of the SoC, to decouple NPU frequency from CPU for CPU overclocking and expected benefit for SoC timing closure. This penalizes NPU latency, may impact NPU throughput, and requires a dedicated high-speed global clock branch, which increases clock power and occupies routing resources ;
- Clock asynchronous MEDIA_SS to rest of the SoC, to decouple clock for expected benefit for SoC timing closure. This penalizes latency versus expected benefits for SoC timing closure. This also requires a dedicated high-speed global clock branch, which increases clock power and occupies routing resources ;
- SysEng & SysAppl requested to support two PLLs for peripherals, one with spread spectrum mode for EMI reduction and one without for best clock accuracy. This adds silicon area ($\sim +0.13\text{mm}^2$) and power overhead ($\sim +1.5\text{mA}$) ;
- Additional PLL for display pixel clock for maximizing flexible frequency setting, as no clear requirements could be provided for custom display support, aside from standardized displays only. SysEng and SysAppl requested for a dedicated PLL to provide maximum flexibility, which adds silicon area ($\sim +0.13\text{mm}^2$) and power overhead ($\sim +1\text{mA}$) ;
- Making all MODCON clock dividers unified on request of SW team, e.g. supporting a wide divider ratios from 1...128 for all dividers. The legacy software approach is not flexible enough to help constraining this for hardware, i.e. no abstraction such as APIs are used or in place. Drawback is increased silicon area and higher power consumption.
- Dropping of Low-Power Run mode during active operation at 0.65V despite available IP and design enablement, due to SoC design effort and tapeout schedule implication. Product Marketing and SysEng accepted the compromise on product competitiveness.
- Dropping of Battery Backup mode due to similarity to Deep Power Down, for simplifying SoC design effort and tapeout schedule implication. Product Marketing and SysEng accepted the compromise in favor of improved schedule.
- SoC Design requested to minimize the amount of power domains to minimize implementation complexity and to benefit effort and schedule. SysEng confirmed no need to provision power domains to support product diversification, e.g. phantom devices.
- Marketing & SysAppl requested pin compatibility with RT1060 for BGA196 package, to ease customer adoption of the new i.MX RT2660. To enable this there are additional silicon area cost ($\sim +0.25\text{mm}^2$, ~32 extra pads) due to extra needed IO pad functionality versus the proposed area-optimized RT2660 IO section – **OPEN (CR)**

In conclusion, SoC Arch believes that a number of the aforementioned compromises are impacting the RT2660 product competitiveness, especially when considering the RT2660 product is only expected on market in a few years. Nevertheless, priority on schedule for RT2660 A0 tapeout is understood. SoC Arch strongly encourages to revisit a number of these compromises for next tapeouts, other upcoming products in the RT2K family, or in case of RT2660 A0 tapeout is delayed versus June-2025 baseline plan.

6.2 MAIN-COMPUTE Domain: Compute Sub-System (CMPT_SS)

The CMPT_SS of i.MX RT2660 is a high-/medium performance domain that takes care of both control- and data processing tasks. Its architectural block diagram is shown in Fig 8. The CMPT_SS of i.MX RT2660 is a subset of the XEA-1 platform version.

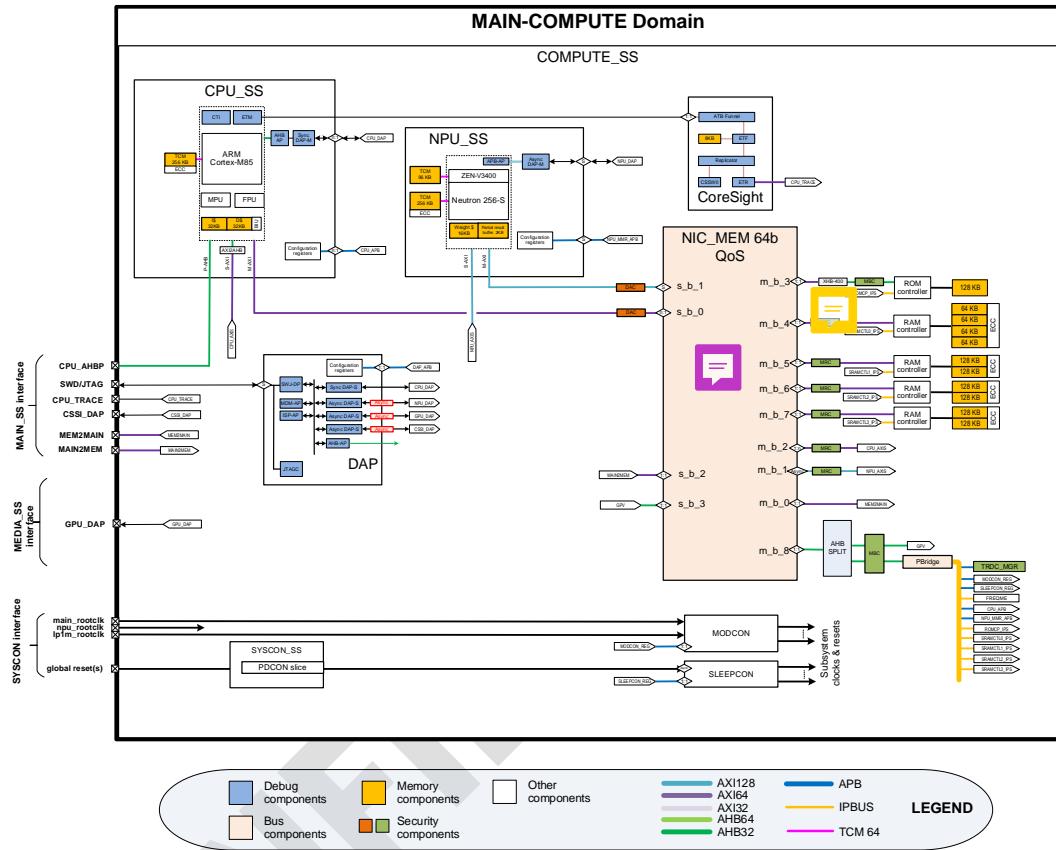


Fig 8. Architectural block diagram of i.MX RT2660's CMPT_SS [3]

The CMPT_SS includes the following building blocks: CPU_SS, NPU_SS, Boot ROM, on-chip shared SRAM and NIC_MEM bus fabric. The CMPT_SS operates at the half the clock frequency of the CPU_SS and maintain a $n:1$ clock synchronous relationship with the CPU_SS. The NPU_SS operates at the same high clock frequency as the CPU_SS while having a clock asynchronous relationship to the rest of the subsystem. This is to ensure the that CPU_SS and NPU_SS can run at independent clocks as requested by BL, to provision for CPU_SS over-clocking dependent on IC characterization outcome. Drawback is the increased latency cost for the NPU_SS which may be acceptable since it does not perform latency-critical tasks.

The CMPT_SS connects to the MAIN_SS that also resides in the MAIN-COMPUTE domain. Both subsystems are operation is a 1:1 clock synchronous.

For the origin of the main building blocks, their maturity level and their legacy i.MX sourcing product, please refer to the IP Re-Use Sheet that is listed in Chapter 15. The CMPT_SS building blocks has been described in more detail in the following sub-sections.

For more detailed information, please refer to the CMPT_SS HW AS document [3].

This document includes the RT2660 specific IP configurations.

6.2.1 Cortex-M85 Sub-System (CPU_SS)

Fig 9 shows a high-level architectural block diagram of the ARM Cortex M85 MCU subsystem.

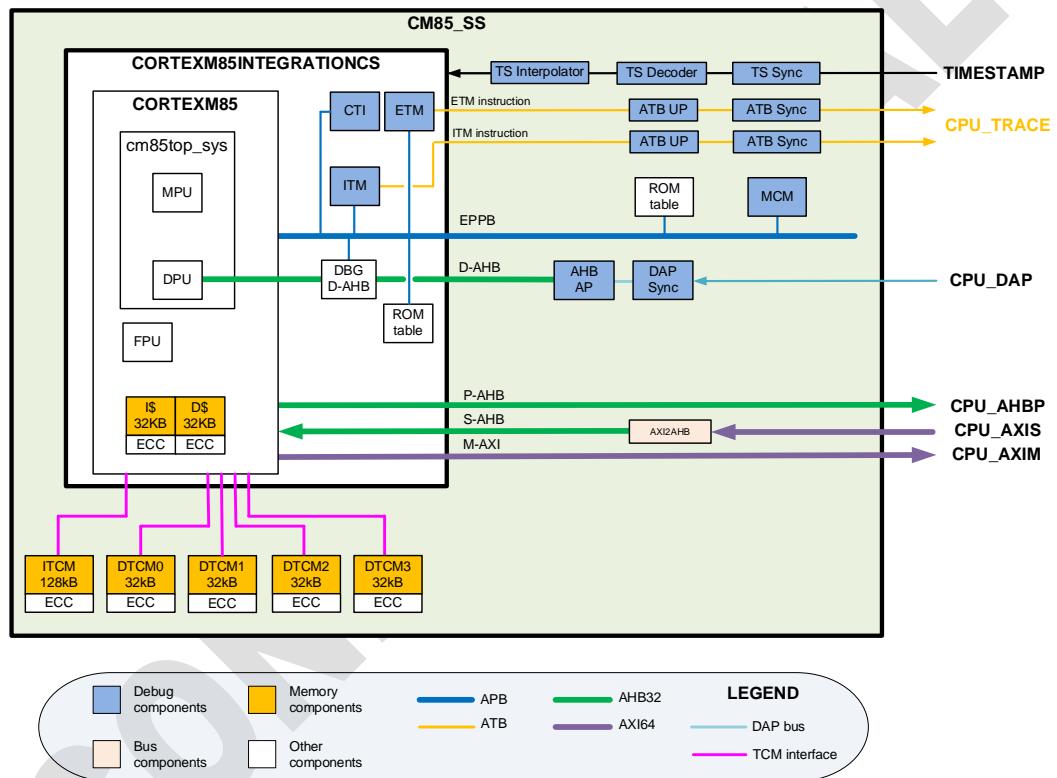


Fig 9. Architectural block diagram of ARM Cortex-M85 based CPU sub-system

6.2.1.1 ARM Cortex-M85 processor

The ARM Cortex-M85 core runs at an operating frequency of up to 700 MHz in Normal Run mode with FBB enabled.

As default, the core includes:

- NVIC, support for up to 480 external interrupts with up to 256 priority levels ;
- System tick timer (one secure, one non-secure) ;
- TrustZone for ARMv8-M ;
- Digital Signal Processing (DSP) Extension ;
- Digital Signal Processing (DSP) Debug Extension ;
- Cross Trigger Interface (CTI) unit ;
- User/Privilege support present ;

- Little-endian data endianness.

Although CM85 M-AXI and P-AHB bus provide 1-bit MASTER output to indicate the processor access or debugger access, there is no plan to differentiate between core and debug access in TRDC, so this is 1-bit MASTER can be ignored in SoC by left un-connected.

The core is configured for:

- Helium's M-Profile Vector Extension present ;
parameter MVE = 2, Integer and half and single precision floating-point MVE included. This option is only valid if FPU=1.
Note:
If FPU=1, then MVE can only be set to 0 or 2.
- Floating Point Unit (HP, SP, DP) present ;
parameter FPU = TRUE, Scalar half, single, and double-precision floatingpoint is included
- Non-Secure Memory Protection Unit with 16 programmable regions ;
parameter MPU_NS = 16
- Secure Memory Protection Unit with 16 programmable regions ;
parameter MPU_S = 16
- Security Attribution Unit (SAU) with 8 regions ;
parameter SAU = 8
- 32 kB Instruction Cache Unit (ICU) ;
parameter ICACHESZ[4:1]=0b0111 32KB instruction cache
parameter ICACHESZ[0]=1 Instruction cache is included
- 32 kB Data Cache Unit (DCU) ;
parameter DCACHESZ[4:1]=0b0111 32 KB data cache
parameter DCACHESZ[0]=1 Performance optimized MAXI data cache is included
- 128 kB Instruction TCM (I-TCM) ;
input CFGITCMSZ[3:0] = 4'b1000
- 128 kB Data TCM (D-TCM) ;
input CFGDTCMSZ[3:0] = 4'b1000
- Error Correcting Code (ECC) on all caches and TCMs ;
Parameter ECC = TRUE
- PACBTI Extension present ;
Parameter PACBTI = TRUE
- Halting Debug Support present ;
- Debug supporting eight breakpoints and eight watchpoints ;
parameter DBG_LVL = 2 Full set: Eight Data Watchpoint and Trace (DWT) comparators, up to two data value comparison, and eight Break Point Unit (BPU) comparators
Debug Monitoring mode and the Unprivileged Debug Extension (UDE) is always supported. The Performance Monitoring Unit (PMU) is always included.
- Interface for full system-level debug access.
- All synchronous states should be in a known status after reset
parameter RAR = TRUE Reset all synchronous states

Table 32. IC requirements traceability: Application CPU core configuration

AS/RS identifier	Requirement	Classification	Covered
iMXRT2660_CPU_3-1	Core configuration	Heading	-
iMXRT2660_CPU_3-2	This core should be instantiated fully to the ARM specification. Any feature that is optional in the Cortex-M85 specification and is determined to not be included shall first be confirmed with the product marketing team prior to removal	Must Have	Yes
iMXRT2660_CPU_4-1	L1 cache	Heading	-

AS/RS identifier	Requirement	Classification	Covered
iMXRT2660_CPU_4-2	The CPU complex shall include 32KB Instruction Cache and 32KB Data Cache.	Must Have	Yes
iMXRT2660_CPU_4-4	ECC shall be implemented for L1 caches	Must Have	Yes
iMXRT2660_CPU_5-1	TCM	Heading	-
iMXRT2660_CPU_5-2	The CPU complex shall include 128KB Instruction TCM and 128KB Data TCM	Must have	Yes
iMXRT2660_CPU_5-3	The CPU complex shall include 256KB Instruction TCM and 256KB Data TCM.	Should have	Rejected due to SoC area
iMXRT2660_CPU_5-5	The core shall access its TCMs in zero-wait state	Must have	Yes
iMXRT2660_CPU_5-6	ECC shall be implemented for TCMs. One bit error correction and two bit error detection is sufficient.	Must have	Yes
iMXRT2660_CPU_5-8	In case the design supports ECC memory configurable as additional TCM when ECC is disabled, the implementation shall not introduce additional latency to TCM access.	Must have	Yes
iMXRT2660_CPU_5-9	A bus interface port is enabled for bus initiators in the SoC accessing TCMs under security protection and isolation.	Must have	Yes, via CPU AHB-S

6.2.1.2 Memory configuration

Both Cache and TCM shall be implemented by SRAM and shall operate at maximum CPU core frequency without wait states. Appropriate memory instances sizes shall be implemented to achieve operation of up to 700MHz at the smallest area penalty.

The selected SRAM compiler for i.MX RT2660 has been shown in Table 7. For this SRAM compiler, the following memory instance configurations shall be used such that required performance can be achieved. Maximum number of words (bits) shall not exceed 4096 (72) in order to achieve the required SRAM performance.

Table 33. **CPU_SS: SRAM instance configurations with selected SRAM compiler**

Target	Total size	# words	# bits	# instances	Other configurations
ICache	32 KB	2048	64 (+7)	2	VT SmartMix, FBB, ECC enabled
DCache	32 KB	1024	32 (+7)	8	VT SmartMix, FBB, ECC enabled
ITCM	128 KB	4096	64 (+8)	4	VT SmartMix, FBB, ECC enabled
DTCM0	32 KB	4096	32 (+7)	2	VT SmartMix, FBB, ECC enabled
DTCM1	32 KB	4096	32 (+7)	2	VT SmartMix, FBB, ECC enabled
DTCM2	32 KB	4096	32 (+7)	2	VT SmartMix, FBB, ECC enabled
DTCM3	32 KB	4096	32 (+7)	2	VT SmartMix, FBB, ECC enabled

6.2.1.3 Bus interfaces

Bus interfaces (AXIM, AXIS and AHBS) of the CPU_SS run at the same frequency as M85 core clock. When AXIM and AXIS buses get connected to the SoC fabric, the clock frequency of those bus interfaces match the system bus clock frequency while preserving a $n:1$ clock-synchronous relationship, respectively.

The maximum operating frequencies are:

- Up to 700MHz on M85, 350MHz on NIC_MEM with 2:1 clock-synchronous setting between CPU_SS and NIC_MEM (Normal Run w/ FBB enabled, default scenario) ;

- Up to 500MHz on M85, 250MHz on NIC_MEM with 2:1 clock-synchronous setting between CPU_SS and NIC_MEM (Normal Run w/ ZBB, alternative scenario 1) ;
- Up to 350MHz on M85, 350MHz on NIC_MEM with 1:1 clock-synchronous setting between CPU_SS and NIC_MEM (Normal Run w/ FBB enabled, alternative scenario 2) ;
- Up to 250MHz on M85, 250MHz on NIC_MEM with 1:1 clock-synchronous setting between CPU_SS and NIC_MEM (Normal Run w/ ZBB, alternative scenario 3).

The AXI-M and AXI-S bus interface is connected to the NIC_MEM. The AHB-P bus interface shall be implemented as $n:1$ clock-synchronous interface and it is connected to AXBS_MAIN of the MAIN_SS. The supported maximum frequency combinations are:

- 700MHz on M85, 350MHz on AXBS_MAIN (Normal Run w/ FBB enabled, default scenario) ;
- 500MHz on M85, 250MHz on AXBS_MAIN (Normal Run w/ ZBB, alternative scenario 1) ;
- 350MHz on M85, 350MHz on AXBS_MAIN (Normal Run w/ FBB enabled, alternative scenario 2) ;
- 250MHz on M85, 250MHz on AXBS_MAIN (Normal Run w/ ZBB, alternative scenario 3).

For CM85 TCM, a backdoor access by other Initiator can be supported by alias address, a remap logic is needed to remap alias address to CM85 TCM address.

6.2.1.4 CM85 TCM ECC Initialization

It is required to initial TCM ECC by hardware, or ROM/SW need to initialize CM85 TCM by configure DMA transaction. The remap logic is a good candidate for state machine to initial CM85 TCM.

HW INIT module is required to override S-AHB like this:

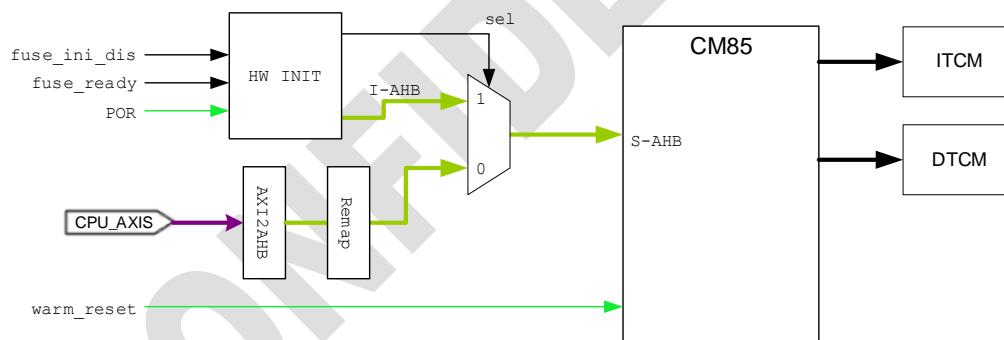


Fig 10. Hardware initialization to TCM

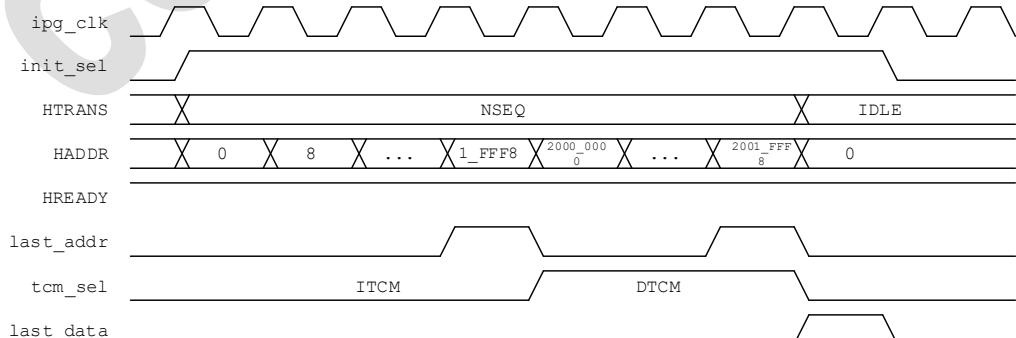


Fig 11. Demo waveform

The HW INIT module should be reset by POR to avoid initial TCM after low power exit to avoid zeroize content retained in TCM.

A Software request should be added in case TCM is power down in low power mode.

The HW INIT is enabled after fuse load completed (fuse_ready or similar signal in OCOTP controller). HW INIT feature is available by default, in case there is any design bug, need to burn fuse_ini_disable bit to disable this feature.

When I-AHB is selected (sel = 1), the HREADY to AXI2AHB gasket should be force to 0 to block any traffic from NIC.

6.2.1.5 Protect TCM from accessed by CM85.

In boot flow, System ROM need to **load image from external device to I/DTCM**, and S110 should authenticate the content in I/DTCM before CM85 can fetch instruction from I/DTCM.

To do so, **SoC need to monitor ITCMMASTER/D*TCMMASTER[3:0] which tells who access I/DTCM and assert error to ITCMERR/D*TCMERR.**

S110 or system ROM shall control a register in MODCON to block CM85 from fetching instruction from I/DTCM before I/DTCM is authenticated.

6.2.2 Neural Processing Unit Sub-System (NPU_SS)

The NPU_SS makes use of a Neutron-256S inference engine. Its main components are the Neutron accelerator, a Zen-V processor, a Data Mover including DMA controller, and weight decompressor. The Zen-V processor is fully managing the Neutron-256S internals at run-time. The NPU_SS runs an operating frequency of up to 700 MHz in Normal Run mode with FBB enabled.

Fig 12 shows a high-level architectural block diagram of the NPU_SS.

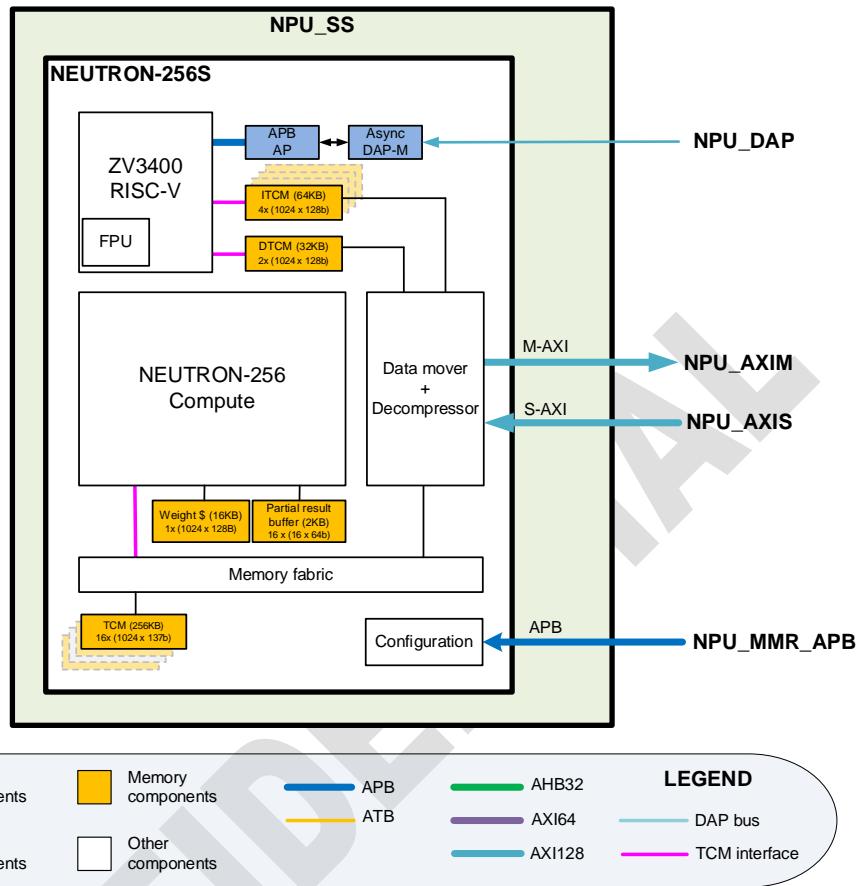


Fig 12. Architectural block diagram of Neutron-256S based NPU sub-system [3]

6.2.2.1 NXP Neutron 256-S NPU

The key features of the NXP Neutron 256-S are:

- Embedded ML inference platform supporting:
 - Multiple sizes for data and weights
 - 8-bit weights x 8-bit data ;
 - 8-bit weights x 16-bit data ;
 - 16-bit weights x 16-bit data ;
 - Multiple CNN layers: CONV1D/2D, Depthwise CONV ;
 - Multiple RNN layers: GRU, MGU, LSTM ;
 - Other DNN layers: max pooling ;
 - Multiple activation functions:
 - None, ReLU, ReLUx (16-bit saturation val), Sigmoid, Tanh ;
 - 256 KB TCM to hold data and weights of the neural network model ;
 - Security components to ensure confidentiality of neural network models.
- Enabling ML inference performance (8x8) of up to 179.2 GMACs at 700MHz in High-Performance Run mode, and up to 128 GMACs at 500MHz in Normal Run mode ;
- 128-bit AXI port for fast access to external memory (pSRAM via XSPI interface) ;
- Re-using Neutron TCM SRAM for the SoC when NPU is not in use.

The TCM shall be implemented with ECC support.

As Neutron-256S can handle memory transfers by itself, there is no need for a dedicated DMA.

To save Neutron-256S leakage, most Neutron-256S logic can be power down, however, IP design must make sure 256KB OCM can still be accessed by other bus initiators when most Neutron-256S logic is power down.

More detailed information of the Neutron S IP can be found in its block guide [18].

Table 34. IC requirements traceability: NPU core requirements

AS/RS identifier	Requirement	Classification	Covered
iMXRT2660_ML_1-6	The Device shall include the N256S NPU if die area allows.	Must have	Yes, but overhead vs N64S
iMXRT2660_ML_1-7	The NPU shall operate up to 700MHz.	Must have	Yes
iMXRT2660_ML_2-2	The NPU should include at least 256KB TCM.	Must have	Yes
iMXRT2660_ML_2-3	The TCM memory can be configured as general purpose SRAM accessible by other bus initiators in the SoC. The NPU TCM shall support the following memory partitions: - 256KB NPU TCM & 0KB general purpose SRAM (default) - 0KB NPU TCM & 256KB general purpose SRAM	Must have	Yes
iMXRT2660_ML_2-4	The NPU shall include 512KB TCM.	Should have	Rejected due to SoC area
iMXRT2660_ML_2-5	In case NPU TCM is 512KB, the TCM memory can be configured as general purpose SRAM accessible by other bus initiators in the SoC. The NPU TCM shall support the following memory partitions: - 512KB NPU TCM & 0KB general purpose SRAM (default) - 256KB NPU TCM & 256KB general purpose SRAM - 0KB NPU TCM & 512KB general purpose SRAM	Must have	Rejected, no 512kB TCM
iMXRT2660_ML_2-6	The TCM shall support ECC. One bit error correction and two bit error detection are required.	Must have	Yes

6.2.2.2 NPU TCM Configuration

Both TCM and weight memory shall be implemented by SRAM and shall operate at maximum NPU core frequency without wait states. The partial result buffer shall be implemented by a register file. Appropriate memory instances sizes shall be implemented to achieve operation of up to 700MHz.

The selected SRAM compiler and register file for i.MX RT2660 has been shown in Table 7. For this SRAM compiler, the following memory instance configurations shall be considered such that required performance can be achieved.

Table 35. NPU_SS: SRAM instance configurations with selected SRAM/regfile compiler

Target	Type	Total size	# words	# bits	# instances	Other configurations
ZEN-V controller						
ITCM	SRAM	64 KB	1024	128	4	VT SmartMix, FBB
DTCM Data	SRAM	16 KB	1024	128	1	VT SmartMix, FBB
DTCM Messaging	SRAM	16 KB	1024	128	1	VT SmartMix, FBB
Neutron 256 core						
TCM	SRAM	256 KB	1024	128(+9)	16	VT SmartMix, FBB, ECC
Weight	RF	16 KB	1024	128	1	VT, FBB
Partial result buffers	RF	2 KB	16	64	16	VT, FBB

6.2.2.3 Bus interfaces

Bus interfaces (AXIM, AXIS) of the NPU_SS run at the same frequency as NPU core clock. When AXIM and AXIS buses get connected to the SoC fabric, the clock frequency of those bus interfaces have a clock asynchronous relationship to the bus fabric. The maximum operating frequency is up to 700MHz on NPU (Normal Run, FBB enabled), and can be set independently from the bus fabric.

The AXI bus interfaces are connected to the NIC_MEM that is part of the CMPT_SS.

6.2.3 ROM Controller with Patch (ROMCP)

For i.MX RT2660 the on-chip ROM is only used by the Cortex-M85 core.

The size of the Boot ROM is 128 KB.

Table 36. IC requirements traceability: ROM requirements

AS/RS identifier	Content	Classification	Covered
iMXRT2660_MEM_3-2	The Device shall implement a ROM block for boot. Boot ROM requirements are specified in Boot section.	Must have	Yes, 128kB ROM

6.2.4 Shared SRAM

The i.MX RT2660 memory subsystem makes use of 1MB on-chip shared SRAM in total, partitioned into four SRAM portions of 256KB each. Hence, the MEM_SS contains four 64-bit AXI interfaces for enhanced system performance by allowing simultaneous access of multiple masters at the same time.

Table 37. IC requirements traceability: On-chip SRAM requirements

AS/RS identifier	Requirement	Classification	Covered
iMXRT2660_MEM_2-8	<p>There are different ways to integrate System RAM in the SoC. The selected method should:</p> <ul style="list-style-type: none"> - minimize memory access latency from all bus initiators, especially those frequently use on-chip SRAM. - allow concurrent read and write accesses from multiple bus initiators in the SoC, using target use cases as reference. - allow a system DMA to access a small block or partition System RAM without waking the entire system bus in low power mode operation. 	Must have	Yes, see Section 0
iMXRT2660_MEM_2-9	The System RAM should have multiple partitions that allow user to retain a small partition of 64KB, 128KB, or 256KB while the rest of System RAM can be powered off along with the main SoC in Power Down mode.	Must have	Yes, 64KB & 128KB
iMXRT2660_MEM_2-10	In case System RAM integration is partitioned into multiple blocks, System RAM should have contiguous address when the ECC enabled or disabled.	Must have	Yes, see Table 28

6.2.4.1 SRAM portion

For the selected SRAM compiler, the shared SRAM shall make use of instances shown in Table 38 to minimize SRAM area. For more information, please refer to the SRAM design study outcome (*refer to "Design studies" on RT2660 NPI Sharepoint*).

Table 38. Shared SRAM: SRAM instance configuration with NXP's EFSPRAM compiler

Target	Total size	# words	# bits	# instances	Other configurations
SRAM bank 0	256 KB	8192	64 (+8)	4	VT SmartMix, FBB, ECC enabled
SRAM banks 1	256 KB	16384	64 (+8)	2	VT SmartMix, FBB, ECC enabled
SRAM banks 2	256 KB	16384	64 (+8)	2	VT SmartMix, FBB, ECC enabled

SRAM banks 3	256 KB	16384	64 (+8)	2	VT SmartMix, FBB, ECC enabled
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The SRAM portion shall operate at CMPT_SS clock frequency. Hence, the SRAM can operate up to 350MHz in Normal Run mode with FBB enabled.

The SRAM instances shall be provisioned with power management infrastructure (e.g. power switches) to support low-power standby operation.

6.2.4.2 SRAM controller

The SRAM controller (SRAMCTL) acts an interface between the NIC_MEM AXI and the shared system RAM. It forwards read and write requests to the SRAM portion downstream.

Fig 13 shows a high-level block diagram of the SRAMCTL.

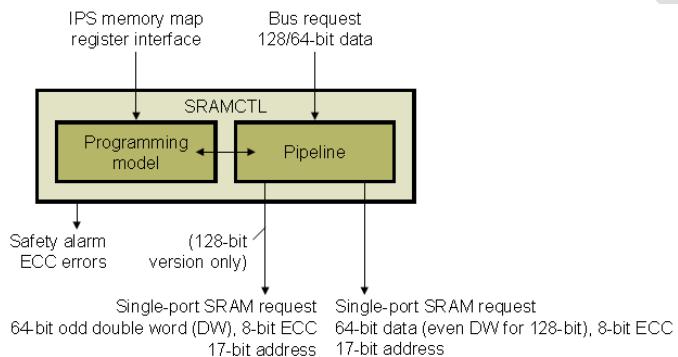


Fig 13. SRAM controller block diagram

The SRAMCTL offers the following main features

- Support for bus master requests in the AXI protocol ;
 - Single or burst transactions ;
 - Access requests are completed in the order they are received ;
- Access latency:
 - Accesses are pipelined ;
 - Latency for read is 2 to 4 ;
 - Latency for full-width write is 1 to 3 ;
 - Latency for narrow-width or parse write is 2 to 4 ;
- Support for 8 exclusive monitors ;
- A programming model that is provided via memory-mapped registers within 4 KB space ;
- Block initialization of a RAM array to place it in a valid ECC state:
 - Software- or hardware-initiated initialization ;
 - Optional wait states between bank writes ;
- Software-programmable upper bound of the valid accessible address range ;
- ECC Hsiao scheme for the RAM:
 - 64-bit data and 29-bit address ;
 - Single-bit error correction (SEC) ;
 - Double-bit error detection (DED) ;
- Safety alarm and monitors for the SRAMCTL pipeline ;
- Error injection provided by:
 - The SRAMCTL programming model (always true for SRAMCTL IP, always false for OCP2SRAM IP) ;
- Support for secure regions:
 - Restrictions on nonsecure masters for any secure region ;

- Error reporting for a secure region only to the corresponding secure master ;
- For memory built-in self-tests (MBISTs) executed by an external MBIST module: monitoring to detect a collision between MBIST operation and normal RAM accesses or initialization if they target the same memory cuts

More detailed information of the existing SRAMCTL IP can be found in its block guide [19].

6.2.5 Debug & Trace

The i.MX RT2660 is based on ARM's CoreSight Debug & Trace infrastructure. It offers the following main features:

- 1149.1 JTAG 5-pin interface supported ;
- ARM Serial Wire Device (SWD) 2-pin interface supported ;
- Support both non-intrusive trace and halt-mode debug options ;
- Supports capture of trace data using any of the following:
 - ARM CoreSight Embedded Trace FIFO (ETF) with 8kB SRAM ;
 - System memory (on-chip SRAM or external XSPI memory) via the ARM CoreSight Embedded Trace Router (ETR) ;
 - ARM CoreSight Trace Port Interface Unit with 4-pin parallel interface ;
 - ARM CoreSight Serial Wire Output (SWO) ;
- Timestamp distribution to the different trace modules ;
- Cross Triggering to pass debug events between different cores and trace components.

For more details on system debug & trace, please refer to Chapter 11.

6.2.6 Bus system

The ARM NIC-400 IP is the interconnect fabric of the CMPT_SS, referred to as NIC_MEM. It runs at an operating frequency of up to 350 MHz in Normal Run mode. NIC_MEM is configured as 64-bit bus fabric; it maintains a $n:1$ clock-synchronous relationship with CPU_SS, a clock asynchronous relationship with NPU_SS and a $1:1$ clock-synchronous relationship with others.

The following NIC_MEM configuration shall be supported:

- Hierarchical clock gating enabled ;
- Quality of Service feature enabled ;
- Arbitration shall be programmable ;
- 'Single Slave per ID' as Cyclic Dependency Avoidance Scheme (CDAS) ;

Table 39 lists the NIC_MEM path connectivity between ASIB and AMIB ports.

Table 39. Path connectivity of NIC_MEM bus fabric

ASIB port	AMIB port
-----------	-----------

	MEM2MAIN	NPU_AXIS	CPU_AXS	ROM_AXIS	MEM_AXIS0	MEM_AXIS1	MEM_AXIS2	MEM_AXIS3	PBRIDGE
CPU_AXIM	X	X	-	X	X	X	X	X	X
NPU_AXIM	X	-	X	-	X	X	X	X	-
MAIN2MEM	-	X	X	-	X	X	X	X	
GPV									

'X' indicates a connection, while '-' indicates no connection

Note that all input- and output ports, with exception of the NPU related ports, shall be configured as clock synchronous 1:1, n:1 and 1:n, depending on port type.

Table 40. Interface configuration of NIC_MEM

Interface	Protocol	Width	Sync	Up/Downsize
ASIB port				
S0 CPU_AXIM	AXI4	64b	SYNC n:1	-
S1 NPU_AXIM	AXI4	128b	ASYNC	2:1 Down
S2 MAIN2MEM	AXI4	64b	SYNC 1:1	-
S3 GPV	AHB	32b	SYNC 1:1	-
AMIB port				
M0 MEM2MAIN	AXI4	64b	SYNC 1:1	-
M1 NPU_AXIS	AXI4	128b	ASYNC	1:2 Up
M2 CPU_AXIS	AXI4	64b	SYNC 1:n	-
M3 ROM_AXIS	AXI4	32b	SYNC 1:1	-
M4 MEM_AXIS0	AXI4	64b	SYNC 1:1	-
M5 MEM_AXIS1	AXI4	64b	SYNC 1:1	-
M6 MEM_AXIS2	AXI4	64b	SYNC 1:1	-
M7 MEM_AXIS3	AXI4	64b	SYNC 1:1	-
M8 PBRIDGE	AXI4 to AHB	32b	SYNC 1:1	-

The NIC_MEM shall make use of default FIFO depth settings, in order to minimize latency impact.

6.2.7 Frequency Measure Unit (FREQME)

FREQME accurately measures the frequency of an on- or off-chip target clock signal using a selectable on-chip reference clock. For example, it can accurately determine the frequency of a low-power oscillator that varies depending on process and temperature.

Its main features are as follows:

- High-accuracy Frequency Measurement mode for on- and off-chip clocks ;
- Pulse Width Measurement (PWM) mode ;
- Reference and target clock inputs selectable from among various chip-specific options ;
- Optional measurement complete interrupt ;
- Result out-of-range detection with optional interrupt.

The main purpose of the FREQME unit to measure the frequency of the IP functional clocks and - bus clocks. The CMPT_SS includes one FREQME units to monitor MODCON_CMPT clock outputs

(CMPT.FREQME). Please refer to the CMPT_SS HW.AS for detailed information about the allocation of the measurement channels for each FREQME unit [3].

6.3 MAIN-COMPUTE Domain: Main Sub-System (MAIN_SS)

The MAIN subsystem of i.MX RT2660 is part of the MAIN-COMPUTE domain. It concerns a medium performance section that includes CSSI wrapper, DMA controllers, XSPI interfaces, Last-Level Cache (LLC), a High-Speed Peripheral subsystem (HSP_SS), and further domain infrastructure. DMA is used to handle memory transactions with peripherals and also when the CPU_SS is in sleep mode. The MAIN_SS runs at an operating frequency of up to 350 MHz in Normal Run mode. It maintains a 1:1 clock-synchronous relationship with the CMPT_SS, and clock-asynchronous relationship with others. Its architectural block diagram is shown in Fig 14. The MAIN_SS of i.MX RT2660 is a subset of the XEA-1 platform version.

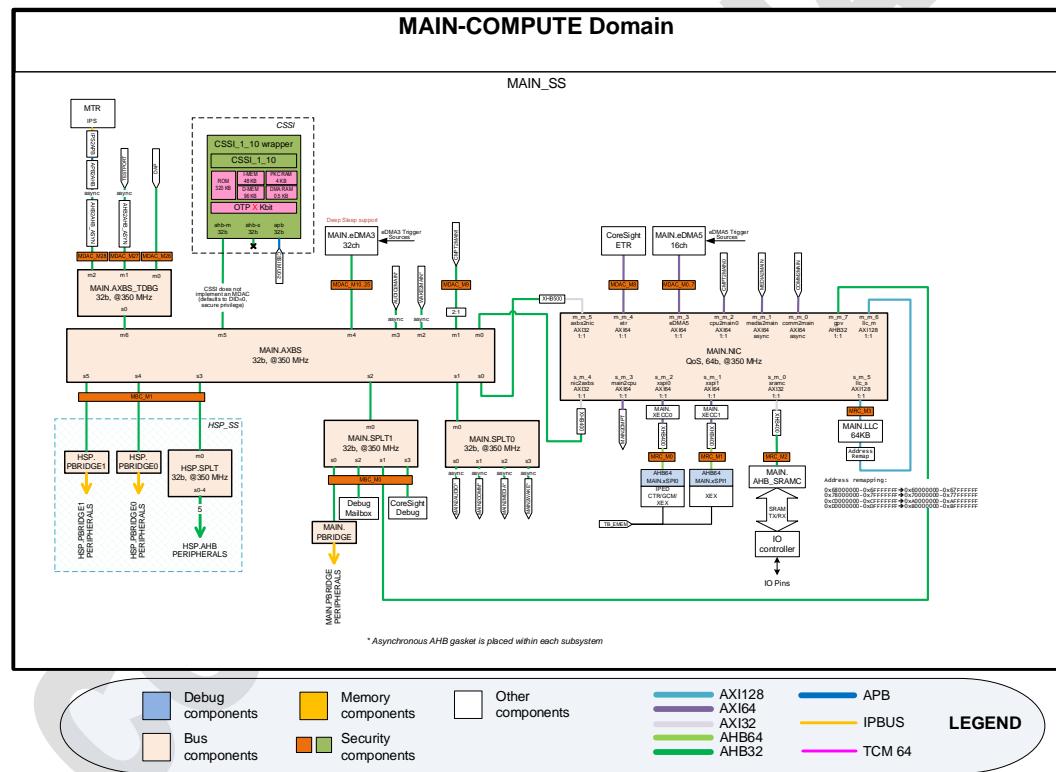


Fig 14. Architectural block diagram of i.MX RT2660's MAIN_SS [4]

For the origin of the main building blocks, their maturity level and their legacy i.MX sourcing product, please refer to the IP Re-Use Sheet that is listed in Chapter 15. The MAIN_SS building blocks has been described in more detail in the following sub-sections.

For more detailed information, please refer to the MAIN_SS HW.AS document [4].

This document includes the RT2660 specific IP configurations.

6.3.1CSSI wrapper

The i.MX RT2660 makes use of a Sentinel secure enclave, also referred to as CSSI_1_10 or S110. The S110 concerns a compact and low-latency general-purpose security enclave that includes a programmable hardware state-machine (HSM) and takes care of secure event handling.

The S110 offers the following main features:

- Platform security
 - Secure boot enforcement ;
 - SoC and S110 secure debug enforcement ;
 - SoC and S110 secure test enforcement ;
 - Lifecycle management enforcement ;
 - Trust provisioning support: key isolation and programmability ;
 - Root of Trust for measured boot and attestation ;
 - Providing keys directly to the various sub-systems.
- HSM and crypto
 - Programmable HSM for variety of personalities (SHE, EVITA, FIPS 140, etc.) ;
 - Key isolation & flexible key policy enforcement ;
 - ECC/AES 128-256 ;
 - Full programmable application crypto acceleration ;
 - Support added for Post Quantum Cryptography (PQC) ;
 - Flexible protocol support through programming.

The S110 does not support any application code execution within the secure subsystem.

For more information, please refer to Chapter 9.

6.3.2External Serial Peripheral Interface (XSPI)

i.MX RT2660 has three eXternal Serial Peripheral Interface (XSPI) modules which act as an interface to external serial flash memory devices and HyperRAM devices. Table 41 shows the XSPI module configuration for the i.MX RT2660 SoC.

Table 41. **i.MX RT2660 XSPI module configuration**

		XSPI0	XSPI1	XSPI2
Targeted external memory device		Serial NAND Flash Serial NOR Flash	Serial pSRAM	Serial pSRAM FGPA/ASIC module
Host interface bus width		x4, x8	x8, x16	X8
Clock mode	Single-ended	Yes		Yes
	Differential	No		Yes
Data rate support	SDR	Yes		Yes
	DDR	Yes		Yes
Host interface frequencies	Octal Flash@1.8V	{200,166,133,100,80} MHz		
	Octal Flash@3.3V	{133,100,80} MHz		
	Quad Flash SDR	{166,133,100,80} MHz		-
	Quad Flash DDR	80 MHz		
	pSRAM @1.8V	-	{250,200,166,133,100,80} MHz {133,100,80} MHz @3.3V	
IP clock frequency support		{400,332,266,200,160} MHz 50% duty cycle clock	{500,400,332,266,200,160} MHz, 50% duty cycle clock	
Execute in-place support		Yes	No	
Security	IPED CTR/GCM	Yes	No	
	XEX	No		Yes

The i.MX RT2660 XSPI module is a new development that is based on the XSPI module used in i.MX RT700. The XSPI host interface offers the following main features:

- Flexible sequence engine to support various flash memory vendor devices. Refer to XSPI IP block guide for example sequences [20] ;
- Single, dual, and quad modes of operation supported for Quad Flash memories ;
- Octal and single IO modes of operation supported for Octal Flash memories ;
- Supporting Single Data Rate (SDR) and Double Data Rate (DDR) modes ;
- Flash memory data strobe signal to support data sampling in SDR and DDR mode ;
- Support for HyperRAM ;
- Support for parallel writes through register-mapped interface in single I/O mode ;
- Ability to connect two identical serial flash memory devices and access them simultaneously for data read operations, forming one (virtual) flash memory with doubled readout bandwidth ;
- Programmable sequence engine to cater to future command/protocol changes and ability to support all existing vendor commands and operations. The software needs to select the corresponding sequence according to the connected flash memory device ;
 - Support for all types of addressing ;
- Support SNAND device for NAND command through IPS interface ;
- Support X16 mode of operation for pSRAM. The x16 mode of operation is supported with EIGHT PAD, which is similar to x8 mode. An additional 'DQS1' is used for the upper byte of x16 mode.

Fig 15 shows a high-level functional block diagram of the existing XSPI module used in i.MX RT700. The existing XSPI module offers the following main features at the SoC interface side, which are subject to change for the i.MX RT2660:

- AHB master to read RX buffer data through AHB (64-bit width interface) or IPS registers space (32-bit access) and fill TX buffer via IPS registers space or using AHB
 - AHB master can be a DMA with a configurable inner loop size ;
- Multi-master AHB accesses are allowed with priority
 - Flexible and configurable buffer for each master ;
 - Total available buffer size is 4096 bytes ;
- All AHB accesses to external memory devices are directly memory mapped to the SoC system memory space.

More detailed information of the existing XSPI IP module can be found in its block guide [20].

XSPI IP Change Requests:

In order to meet the i.MX RT2660 RS requirements for the XSPI module, the following changes are needed to the existing XSPI module – reviewed with DIP team:

- **TKT0633665:** Add support for serial NAND memories with 4kB page structure. Today, the XSPI IP does not support write across 2kB boundary ;
- Add support for Bad Block Management feature in order to reduce complexity in the software driver.
- **TKT0633650:** In-band reset support.
- **TKT0633668:** Allowing IPED regions to keep key after intrusion.
- **TKT0633670:** Address remap support.
- **TKT0633671:** ISI pSRAM address scheme support.

The following changes are rated as 'Should-Have' because the DIP team is not able to execute them to be on-time for i.MX RT2660 SoC A0 tape-out. However, they shall be implemented on the next xSPI IP version on IP train schedule for release in 2025.

- **TKT0633648:** Upgrade the 64-bit AHB master interface to a 64-bit AXI master interface & enhancement of the arbiter.
- **TKT0633666:** Add multi-plane read/write support for serial NAND memories. A "Plane Select" bit must be included when it issues a Read or Write command to the flash device.

- **TKT0633651:** CRC support for Read/Write parity.
- **TKT0633653:** HW ECC engine for SPI NAND.
- **TKT0633667:** Random access to RAM in IPED-XEX mode.

The i.MX RT2660 is designed to support the following list of available external memory offerings.

Table 42. External XSPI memory offerings supported by the i.MX RT2660

Supplier	Memory type	XSPIO	XSPI1/2
AP Memory	pSRAM	-	APS256XXN-OB9-WA APS256XXN-OB9
Fidelix	pSRAM	-	tbd
GigaDevice	Quad SPI NOR Flash Quad SPI NAND Flash	GD25LB256F GD5FGM7xExxG	-
Infineon	Quad SPI NOR Flash Octal SPI NOR Flash pSRAM	S25FS256S S79FS256S	-
ISSI	Octal SPI NOR Flash pSRAM	IS25WX256	-
Kioxia/Toshiba	Quad SPI NAND Flash	TC58CVG1S3HxAlx	-
Macronix	Quad SPI NOR Flash	MX25U25643G	-
	Octal SPI NOR Flash	MX25UW51345G	-
	Quad SPI NAND Flash	MX35UFxG24AD	-
	Octal SPI NAND Flash	tbd	-
Micron	Quad SPI NOR Flash	MT25QU512ABB	-
	Octal SPI NOR Flash	MT35XU256ABA	-
	Quad SPI NAND Flash	MT29F1G01ABBFDSF	-
Winbond	Quad SPI NOR Flash	W25Q256JW_DTR	-
	Octal SPI NOR Flash	W35T512NW	-
	Quad SPI NAND Flash	W25N02JWxxxF/C	-
	Octal SPI NAND Flash	W35N01jW_IT	-
	pSRAM	-	W958D8NBYA41
	pSRAM	-	W958D6NBKX4I

Table 43. MAIN.XSPI configurations.

Description	Parameter	MAIN.XSPIO	MAIN.XSPI1
IPS address width.	H_ADDR_WIDTH	16	16
Number of 64bit locations of AHB buffer	AHB_BUF_DEPTH	512	512
AHB buffer Pointer width.	AHB_PTR_WIDTH	9	9
Number of sequence entries	LUT_DEPTH	16	16
TX Buffer Pointer width (32bits wide)	TX_FIFO_PTR_WIDTH	`d8	`d8
RX Buffer Pointer width (64bits wide)	RX_FIFO_PTR_WIDTH	`d7	`d7
Module disable bit's reset value	MDIS_RES_VAL	1'b1	1'b1
Data learning enable	DATA_LEARN_EN	1'b0	1'b0
Data learning on 8 pads	DATA_LEARN_8PAD	1'b0	1'b0
Macronix Parity enable	PARITY_EN	1'b1	1'b0
Data learning enable	DFTLOOPBACK_EN	#1	1'b1
High-frequency Initiator delay chain enable	DLL_HIGH_EN	1'b1	1'b1
Low-frequency Initiator delay chain enable	DLL_LOW_EN	1'b1	1'b1
Seg-Length of high freq delay chain	DELAYCHAIN_HIGH_SEGLEN	16	16
Seg-Length of low freq delay chain	DELAYCHAIN_LOW_SEGLEN	16	16
Number of delay lines	NUM_TAPS	16	16
Base address for mem mapped serial flash	QSPI_AMBA_BASE	32'hA0000000	32'h60000000
Defines the width of the initiator id fields with AHB (HMASTER)	MSTRID_WIDTH	4'd6	4'd6
Reset value of the TOP addr for Serial Flash A1	TOP_ADDR_MEMA1	32'hB0000000	32'h68000000
Reset value of the TOP addr for Serial Flash A2	TOP_ADDR_MEMA2	32'hB0000000	32'h68000000

Reset value of the TOP addr for Serial Flash B1	TOP_ADDR_MEMB1	32'hB0000000	32'h68000000
Reset value of the TOP addr for Serial Flash B2	TOP_ADDR_MEMB2	32'hB0000000	32'h68000000
Address for RX buffer access via AHB	QSPI_ARDB_BASE	32'h24200000	32'h24000000
Maximum value for HREADY low timeout counter counts	HREADY_COUNTER	32'h0000C350	32'h0000C350
Eight pad interface enable	EIGHT_PAD_EN	1'b1	1'b1
Enable for data strobe functionality like DQS/RDS	DATA_STROBE_EN	1'b1	1'b1
Endianess reset value of QSPI_MCR(END_CFG)	ENDIAN_RES_VAL	2'b11	2'b11
BUF0 initiator id reset value QSPI_BUFOCR(MSTRID)	BUFO_MSTRID_RES_VAL	'h0	'h0
BUF1 initiator id reset value QSPI_BUF1CR(MSTRID)	BUF1_MSTRID_RES_VAL	'h1	'h1
BUF2 initiator id reset value QSPI_BUF2CR(MSTRID)	BUF2_MSTRID_RES_VAL	'h2	'h2
BUF3 initiator id reset value QSPI_BUF3CR(MSTRID)	BUF3_MSTRID_RES_VAL	'h3	'h3
Reset value of Data input to Flash QSPI_FLSHCR(TDH)	FLSH_TDH_RES_VAL	2'b01	2'b01
On-the-fly decryption engine enable	OTFAD_EN	1'b0	1'b0
Number of key blobs to be fetched	NUM_KEY	1'b0 (NA)	1'b0 (NA)
Valid key size (in multiple of 64 bits) of a single key blob	VALID_KEY_SIZE	1'b0 (NA)	1'b0 (NA)
Total allocated key size (in multiple of 64 bits)of a key blob	ALLOC_KEY_SIZE	1'b0 (NA)	1'b0 (NA)
Reset value of DQS_EN bit in QuadSPI_MCR	MCR_DQSEN_RES_VAL	1'b1	1'b1
CDC Synchronizer depth	SDEPTH	4'h2	4'h2
AHB write enable	AHBWR_EN	1'b1	1'b1
Enables port B instantiation	PORTB_EN	1'b0	1'b0
Idle cycle counter for AHB write when 32 bits data is not present remaining data is send. Used in case of HyperRAM.	AHB_IDLE_CNT	8'd32	8'd32
Streaming prefetch "n" in terms of $(2^n)*1\text{KBytes}$	STREAMING_SIZE	3'd6	3'd6
Number of EENV environments supported. More than 1 for virtualization support	NUM_EENV	1	1
Flash Data and Pad width	SIO_WIDTH	8	8
Secure flash module is present	SFP_PRESENT	1'b1	1'b1
Number of flash region address descriptors.	SFP_NUM_FRAD	8	8
Number of MDAD/ Target group queue. Access permission control for SFP descriptors.	SFP_NUM_MDAD	2	2
Tied address size width	TIE_ADDRSIZE_WIDTH	16	16
Global Initiator ID (GMID)	SFP_MGCR_GMID	6'h0 (CM85: RT2520, RT2660), 6'h1 (CM55: RT2770)	6'h0 (CM85: RT2520, RT2660), 6'h1 (CM55: RT2770)
Global initiator ID mask	SFP_MGCR_GMID_MASK	6'h3F	6'h3F
Reset value of MGCR register	SFP_MGCR_RST	32'hA8000000	32'hA8000000
Reset value of MRCR register	SFP_MRCR_RST	32'h500E07	32'h500E07
Reset value of SFP timeout register	SFP_MTIMEOUT_RST	32'hFFFF	32'hFFFF
Reset value of TG queue MDAD registers	SFP_TG_MDAD_RST	32'h0	32'h0
FRAD0 word0 reset value	SFP_FRAD0_0_RST	32'hA0000000	32'h60000000
FRAD0 word1 reset value	SFP_FRAD0_1_RST	32'hAFFFFFFF	32'h67FFFFFF
FRAD0 word2 reset value	SFP_FRAD0_2_RST	32'h0	32'h0
FRAD0 word3 reset value	SFP_FRAD0_3_RST	32'h0	32'h0
Number of bits for address compare (64KB boundary)	SFP_ADDR_CBITS	16	16

FRAD word 0 mask value	SFP_FRAD_WORD0_MASK	32'hFFFFFFF	32'hFFFFFFF
FRAD word 1 mask value	SFP_FRAD_WORD1_MASK	32'hFFFFFFF	32'hFFFFFFF
FRAD word 2 mask value	SFP_FRAD_WORD2_MASK	32'hFFFFFFF	32'hFFFFFFF
FRAD word 3 mask value	SFP_FRAD_WORD3_MASK	32'hFFFFFFF	32'hFFFFFFF
SFP MDxACP scheme sel 0 -older 3bit scheme, 1 New 2 bit scheme (without attributes check)	SFP_ACP_SEL	1'b0	1'b0
X16 mode is enabled or not	X16_MODE_ENABLE	1'b1	1'b1
IPED block is enabled or disabled	IPED_EN	1'b1	1'b1 TBC
IPED XEX block is enabled or disabled	IP_XEX_EN	1'b1	1'b1
SFM address width	ASFM_ADDR_WIDTH	28	28
IPED CTX IV	IPED_CTX0_IV	64'b0	64'b0
IPED CTX IV	IPED_CTX1_IV	64'b0	64'b0
IPED CTX IV	IPED_CTX2_IV	64'b0	64'b0
IPED CTX IV	IPED_CTX3_IV	64'b0	64'b0
IPED CTX IV	IPED_CTX4_IV	64'b0	64'b0
IPED CTX IV	IPED_CTX5_IV	64'b0	64'b0
IPED CTX IV	IPED_CTX6_IV	64'b0	64'b0
IPED CTX IV	IPED_CTX7_IV	64'b0	64'b0
IPED CTX IV	IPED_CTX8_IV	64'b0	64'b0
IPED CTX IV	IPED_CTX9_IV	64'b0	64'b0
IPED CTX IV	IPED_CTX10_IV	64'b0	64'b0
IPED CTX IV	IPED_CTX11_IV	64'b0	64'b0
IPED CTX IV	IPED_CTX12_IV	64'b0	64'b0
IPED CTX IV	IPED_CTX13_IV	64'b0	64'b0
IPED CTX IV	IPED_CTX14_IV	64'b0	64'b0
IPED CTX IV	IPED_CTX15_IV	64'b0	64'b0
IPED CTX KEY	IPED_CTX0_KEY	128'b0	128'b0
IPED CTX KEY	IPED_CTX1_KEY	128'b0	128'b0
IPED CTX KEY	IPED_CTX2_KEY	128'b0	128'b0
IPED CTX KEY	IPED_CTX3_KEY	128'b0	128'b0
IPED CTX KEY	IPED_CTX4_KEY	128'b0	128'b0
IPED CTX KEY	IPED_CTX5_KEY	128'b0	128'b0
IPED CTX KEY	IPED_CTX6_KEY	128'b0	128'b0
IPED CTX KEY	IPED_CTX7_KEY	128'b0	128'b0
IPED CTX KEY	IPED_CTX8_KEY	128'b0	128'b0
IPED CTX KEY	IPED_CTX9_KEY	128'b0	128'b0
IPED CTX KEY	IPED_CTX10_KEY	128'b0	128'b0
IPED CTX KEY	IPED_CTX11_KEY	128'b0	128'b0
IPED CTX KEY	IPED_CTX12_KEY	128'b0	128'b0
IPED CTX KEY	IPED_CTX13_KEY	128'b0	128'b0
IPED CTX KEY	IPED_CTX14_KEY	128'b0	128'b0
IPED CTX KEY	IPED_CTX15_KEY	128'b0	128'b0
IPED only CTR mode or CTR+GCM mode When DLL_CDL8_EN = 1'b1, the CDL8 related RTL logic is present	ID_CFG_PRINCE_CTR_GCM DLL_CDL8_EN	1'b1 1'b1	1'b0 TBC 1'b1
CTR,GCM or XEX modes are configurable in ip_prince_3m Block	IPED_3M	1'b1	1'b1
Double Encryption Support of IPED Block	IPED_DOUBLE_ENC	1'b0	1'b0
ARDB FIFO is present	ARDB_FIFO_PRESENT	1'b0	1'b0
AHB WRITE WRAP burst support	AHB_WRITEWRAP_EN	1'b1	1'b1

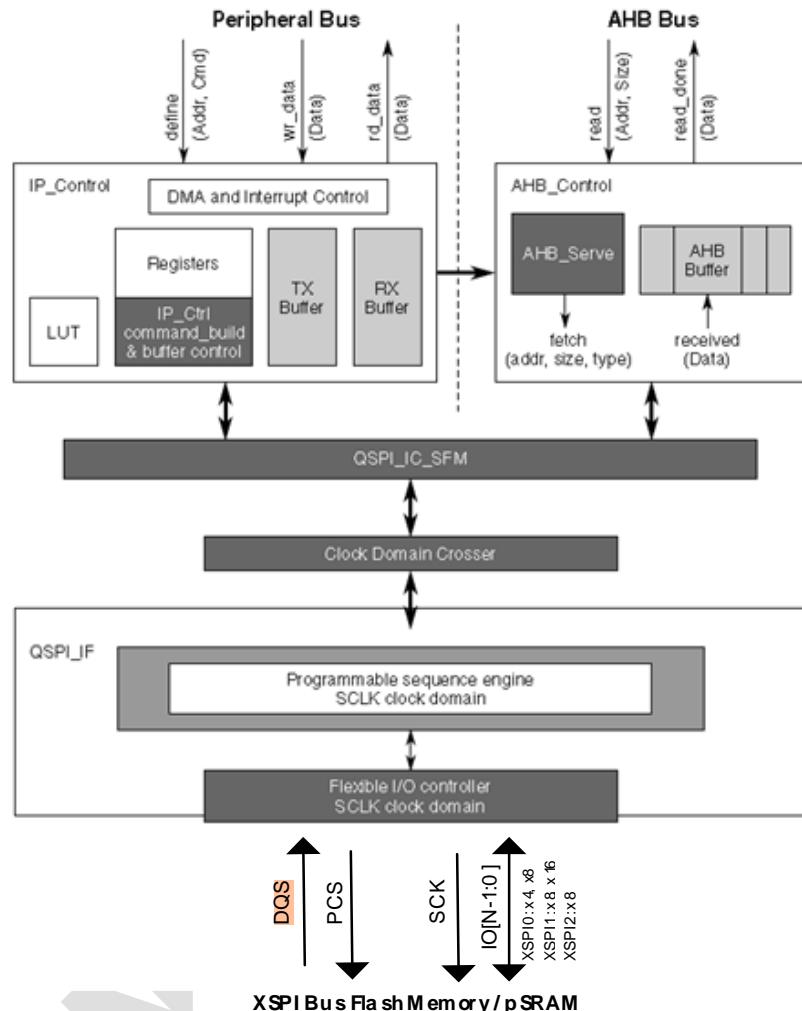
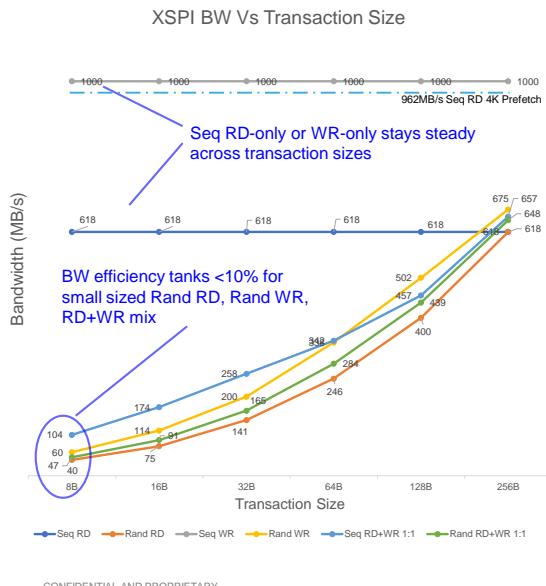


Fig 15. High-level functional block diagram of the existing xSPI module

The performance modelling team has performed a detailed xSPI performance analysis [21]. The following configuration has been considered: xSPI AHB @ 350MHz, x16 DDR pSRAM@250MHz, IPED bypass mode, 1KB AHB Buffer, Prefetch/ADAT Size = 256 Byte (sub-buffers disabled), Random RD+WR: Prefetch disabled. Refer to [21] for further configuration details. Fig 16 shows an example xSPI bandwidth as function of transaction size (8 Byte up to 256 Byte) and type of transaction (Random, Sequential) in case of a single initiator scenario.

XSPI Bandwidth Characterization (Single Master, 256B Prefetch)



- Seq RD:
 - Sequential RDs, hit in Rx buffer, >256B misses in buffer
 - BW remains constant, dependent on prefetch size but independent of transaction size
- Rand RD:
 - Random RDs, miss in Rx buffer, RDs aborts 256B prefetch of previous RD transaction
 - BW keep increasing with transaction size and matches with RD best case for 256B sized transaction.
- Seq WR:
 - Sequential WRs, TxFIFO gets full and backpressures
 - PSRAM peak BW 1GB/s is achieved
- Rand WR:
 - Random WRs, WRs wait for completion of previous WR (tail end) to complete at flash end
 - BW keep increasing with transaction size but can't go upto peak PSRAM BW
- Seq RD+WR
 - Performance is way below Seq RD or Seq WR, since RDs break Seq WR pipeline, and WRs abort RD prefetch
- Rand RD+WR
 - Performance is below Rand WR but above Rand RD, since Rand RDs are more time consuming due to prefetch start and abort process.



Fig 16. Example XSPI bandwidth (pSRAM, x16, 250MHz) vs Transaction size and -type [21]

From the previous figure it can be observed that sequential transactions and larger Bytes transactions for Random transactions perform better.

Table 44. IC requirements traceability: XSPI controller requirements

AS/RS identifier	Requirement	Classification	Covered
iMXRT2660_MEM_4-1	XSPI Controller	Heading	-
iMXRT2660_MEM_4-2	The xSPI Controller provides the host interface to external devices, including serial NOR flash, serial NAND flash, serial pSRAM, or FPGA/ASIC module.	Must have	Yes, XSPI0/1/2
iMXRT2660_MEM_4-3	The xSPI controller IP was designed to support different types of memory (or device), which may require different functions or features of xSPI IP to support. Each xSPI controller should be separately configured to support the type of memory (or device) it intended to support.	Must have	Yes, see Table 41
iMXRT2660_MEM_4-5	This processor shall implement 3x xSPI ports. Each port is controlled an xSPI controller. - xSPI0 port is for the host interface to serial NOR or serial NAND flash. - xSPI1 port is the host interface to serial pSRAM. - xSPI2 port is the host interface to FPGA or ASIC module on board (TBD). The third xSPI port can be used as the second host interface to pSRAM for additional RAM expansion for applications that need more RAM bandwidth.	Must have	Yes, see Table 41
iMXRT2660_MEM_4-7	The xSPI ports shall be compliant to JEDEC xSPI JESD251 v1.0 Specification.	Must have	Yes
iMXRT2660_MEM_4-9	The xSPI controllers shall support AXI interface for concurrent accesses to prefetch buffers and write buffers.	Must have	No, IP CR not ready on-time (TKT0633648)

AS/RS identifier	Requirement	Classification	Covered
iMXRT2660_MEM_4-10	The xSPI controllers shall implement an arbiter that: - arbitrates memory access based on priority of master ID. - has the ability to suspend active transfer to the external memory in favor of a pending access from a master ID with higher priority. - includes aging counter to guarantee pending access will get service. - Other arbitration features for performance improvement should be explored and implemented.	Must have	No, IP CR not ready on-time (TKT0633648)
iMXRT2660_MEM_5-1	xSPI host interface for flash memory	Heading	-
iMXRT2660_MEM_5-1	This xSPI port shall support x4 and x8 bus width for Quad SPI flash and Octal SPI flash, respectively.	Must have	Yes, see Table 41
iMXRT2660_MEM_5-2	This xSPI port supports only single-ended clock. Differential clock is not required.	Must have	Yes, see Table 41
iMXRT2660_MEM_5-3	This xSPI port shall support Octal SPI flash up to 200MHz at 1.8V nominal voltage.	Must have	Yes, see Table 41
iMXRT2660_MEM_5-4	This xSPI port shall support Octal SPI flash up to 133MHz at 3.3V nominal voltage.	Must have	Yes, see Table 41
iMXRT2660_MEM_5-5	This xSPI port shall support Quad SPI flash up to 166MHz in SDR mode.	Must have	Yes, see Table 41
iMXRT2660_MEM_5-6	This xSPI port shall support Quad SPI flash up to 80MHz in DDR.	Must have	Yes, see Table 41
iMXRT2660_MEM_5-7	This xSPI controller shall work in conjunction with a tightly coupled encryption block to provide encryption/decryption and integrity protection on the read and write (or program) content. This requirement is only applied for NOR flash memory.	Must have	Yes, IPED
iMXRT2660_MEM_5-10	This xSPI controller shall enforce secure flash protection. Access control policies are based on the master ID, address ranges, privilege, and secure attributes of the transactions. All accesses throughout the flash device need to be monitored to determine the validity of all accesses. If transaction from a given master has appropriate access rights, it is forwarded to flash, else the access is denied, and an error is generated.	Must have	Yes, via TRDC
iMXRT2660_MEM_6-1	NOR Flash support	Heading	-
iMXRT2660_MEM_6-2	This xSPI port shall support interrupt input from the flash device in the event of ECC or CRC error detection. The Device targets industrial and automotive applications where data integrity is important. Upon detection of ECC or CRC error condition, the memory device would assert interrupt to notify the host processor of data integrity condition.	Must have	Not supported in RT700 xSPI Open: IP CR (TKT0633651)
iMXRT2660_MEM_6-3	This xSPI port shall support address remap feature to support dual-image NOR flash boot. The address remap needs a lock mechanism. The lock should be left untouched by ROM if only a single image is used to allow a customer bootloader to use the remap if the bootloader supports dual images. In this use case it will be the customer bootloader/application responsibility to lock the remap after it is used or if determined it will not be used. If dual-image is enabled (remap offset fuses are configured), then ROM can lock the remap during boot to prevent it from being modified later.	Must have	Open: IP CR (TKT0633670)
iMXRT2660_MEM_6-4	This xSPI port shall support Quad SPI NOR flash from following vendors: - Winbond (W25Q256JW_DTR) - Micron (MT25QU512ABB) - Macronix (MX25U25643G) - GigaDevice (GD25LB256F) - Infineon (S25FS256S)	Must have	Yes, see Table 42
iMXRT2660_MEM_6-5	This xSPI port shall support Octal SPI NOR flash from following NVM vendors: - Macronix (MX25UW51345G) - Micron (MT35XU256ABA)	Must have	Yes, see Table 42

AS/RS identifier	Requirement	Classification	Covered
	- Infineon (S79FS256S) - ISSI (IS25WX256)		
iMXRT2660_MEM_7-1	NOR Flash performance	Heading	-
iMXRT2660_MEM_7-2	The Octal SPI NOR sequential read scenario should achieve a performance of, at minimum, 372 MBps without decryption or with on-the-fly decryption in CTR mode.	Must have	<i>Include in verification plan during design phase</i>
iMXRT2660_MEM_7-3	The Octal SPI NOR sequential read scenario should achieve a performance of, at minimum, 360 MBps with on-the-fly decryption in GCM mode.	Must have	<i>Include in verification plan during design phase</i>
iMXRT2660_MEM_7-4	The Quad SPI NOR sequential read scenario should achieve a performance of, at minimum, 74 MBps without decryption or with on-the-fly decryption in CTR mode.	Must have	<i>Include in verification plan during design phase</i>
iMXRT2660_MEM_7-5	The Quad SPI NOR sequential read scenario should achieve a performance of, at minimum, 70 MBps with on-the-fly decryption in GCM mode.	Must have	<i>Include in verification plan during design phase</i>
iMXRT2660_MEM_7-5	This xSPI interface shall support DQS loop back on a dummy pad in order to achieve the target QSPI frequency without using the DQS pin.	Must have	 Supported
iMXRT2660_MEM_8-1	NAND Flash support	Heading	-
iMXRT2660_MEM_8-2	This xSPI port shall support Serial NAND with 2KB-page and 4KB-page structure.	Must have	Open: IP CR (TKT0633665)
iMXRT2660_MEM_8-5	This xSPI port shall support Serial NAND with multi-plane structure.	Must have	No, IP CR not ready on-time (TKT0633666)
iMXRT2660_MEM_8-9	This xSPI port shall support Bad Block Management feature enabled on some SPI NAND products. This feature would reduce the complexity in the software driver.	Must have	IP CR to be confirmed
iMXRT2660_MEM_8-12	This xSPI port shall support Quad SPI NAND flash from following vendors: - Winbond (W25N02JWxxxF/C) - Micron (MT29F1G01ABBFDSF) - Macronix (MX35UFxG24AD) - GigaDevice (GD5FGM7xExxG) - Kioxia/Toshiba (TC58CVG1S3HxAIx)	Must have	Yes, see Table 42
iMXRT2660_MEM_8-13	This xSPI port shall support Octal SPI NAND flash from following NVM vendors: - Winbond (W35N01jW_IT) - Macronix (TBD)	Must have	Yes, see Table 42
iMXRT2660_MEM_9-1	SPI NAND performance	Heading	-
iMXRT2660_MEM_9-2	The Quad SPI NAND sequential read scenario should achieve a performance of, at minimum, 30 MBps, with ECC enabled.	Must have	<i>Include in verification plan during design phase</i>
iMXRT2660_MEM_9-3	The Quad SPI NAND sequential read scenario should achieve a performance of, at minimum, 70 MBps, with ECC disabled, i.e. ECC is performed by SW running on CM85.	Must have	<i>Include in verification plan during design phase</i>
iMXRT2660_MEM_10-1	xSPI host interface for pSRAM	Heading	-
iMXRT2660_MEM_10-2	This xSPI port shall support x8 and x16 bus width for serial pSRAM.	Must have	Yes, see Table 41
iMXRT2660_MEM_10-3	This xSPI port shall support single-ended and differential clock modes.	Must have	Yes, see Table 41
iMXRT2660_MEM_10-4	A DDR complementary differential IO pad is required for the differential clock in order to meet AC timing at high speed.	Must have	Yes, see Table 41

AS/RS identifier	Requirement	Classification	Covered
iMXRT2660_MEM_10-5	This xSPI controller shall support both xSPI protocols: Profile 1 (Octal SPI) and Profile 2 (HyperBus).	Must have	Yes
iMXRT2660_MEM_10-6	This xSPI port shall support Serial pSRAM up to 250MHz at 1.8V nominal voltage.	Must have	Yes, see Table 41
iMXRT2660_MEM_10-7	This xSPI port shall support Serial pSRAM up to 133MHz at 3.3V nominal voltage.	Must have	Yes, see Table 41
iMXRT2660_MEM_10-8	The Device shall support pSRAM from follow DRAM vendors: - Winbond (W958D8NBYA41, W958D6NBKX4I) - Infineon (S80KS2564GACHA040) - AP Memory (APS256XXN-OB9-WA, APS256XXN-OB9) - ISSI - Fidelix	Must have	Yes, see Table 42
iMXRT2660_MEM_11-1	pSRAM performance	Heading	-
iMXRT2660_MEM_11-2	The x16 pSRAM sequential read scenario should achieve a performance of, at minimum, 620 MBps without decryption.	Must have	Yes, w/ single master and large prefetch size (4kB) <i>Include in verification plan during design phase</i>
iMXRT2660_MEM_11-3	The x16 pSRAM sequential read scenario should achieve a performance of, at minimum, 620 MBps with decryption in GCM mode.	Must have	Yes, w/ single master. <i>Include in verification plan during design phase.</i>
iMXRT2660_MEM_11-4	The x16 pSRAM multiple bus initiators read and write scenario should achieve a performance of, at minimum, 550MBps, without crypto operation.	Must have	No, only up to 380MBps may be achievable in multi-master scenarios. <i>Include in verification plan during design phase</i>
iMXRT2660_MEM_12-1	xSPI port for FPGA/ASIC	Heading	-
iMXRT2660_MEM_12-2	If the third xSPI port is implemented to provide a memory-mapped interface to external FPGA/ASIC module, it would have the same requirement as the xSPI port for pSRAM, except it only supports 8-bit IO interface.	Must have	Yes, CR RT2660-31
iMXRT2660_MEM_12-3	This xSPI port shall be fully compatible with the xSPI Responder.	Must have	Yes

Table 45. IC requirements traceability: ECC/CRC support for external memory requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_MEM_17-2	The Device shall support external flash or pSRAM devices with built-in CRC and/or ECC capabilities.	Should have	Yes
iMXRT2660_MEM_17-3	The Device shall support ECC for external flash and pSRAM devices without built-in ECC or ECC disabled.	Should have	No XECC, IP CR not ready on-time (TKT0633653)

6.3.3 Last-Level Cache (LLC)

The i.MX RT2660 includes a CodaCache IP from Arteris as Last Level Cache (LLC). CodaCache is a configurable stand-alone non-coherent cache IP. It buffers memory data and services transactions without accessing main memory. Any coherence necessary between CodaCache IP and other caching agents in the system must be maintained by system software.

CodaCache IP supports an extensive set of features and configurability that allows the cache to be optimized for a very wide range of systems and requirements. CodaCache IP features include:

- 64-, 128-, 256-, or 512-bytes configurable cache line ;
- AXI 4 upstream and downstream interface ;
- AXI 4 downstream interface allows read data response interleaving between different AxIDs ;
- APB interface with write protection input for configuration ;
- Configurable cache size of up to 8MB ;
- Configurable associativity of up to 16 ways ;
- Configurable number of tag and data banks ;
- Configurable type of replacement policy ;
- Configurable scratchpad memory on a per way basis ;
- Configurable Way partitioning support ;
- Coherency management via hardware assisted cache flush ;
- Placeholder for upstream and downstream AXI4 ;
- Selectable way initialization and flush ;
- Configurable interrupt manager ;
- Optional performance monitor with optional capture registers.

For more detailed information about CodaCache IP, please refer to its reference manual [22].

CodaCache IP improves system performance while saving power, by reducing average memory access latency and by reducing the number of off chip memory accesses. The i.MX RT2660 makes use of Arteris' CodaCache IP towards xSPI external memory communication, by enabling a xSPI access with increased byte-width transaction sizes, when applicable, to improve xSPI performance efficiency.

The i.MX RT2660 LLC shall be configured for a 128B cache line and for a the minimum AXI bus-width of 128-bit.

Table 46. MAIN.LLC configuration

Description	Parameter	MAIN.LLC
AXI_data_width	AXI_data_width	128
AXI_address_width	AXI_address_width	32
AxID_width	AxID_width	11
AxUSER_width	AxUSER_width	13
Enable_QoS_bits	Enable_QoS_bits	Yes
Enable_PROT_bits	Enable_PROT_bits	No
Enable_Region_bits	Enable_Region_bits	No
Enable_Upstream_AXI_pipeline	Enable_Upstream_AXI_pipeline	No
Enable_Downstream_AXI_pipeline	Enable_Downstream_AXI_pipeline	No
Max_outstanding_memory_write_transactions_(WTT_entries)	Max_outstanding_memory_write_transactions_(WTT_entries)	4
Disable_AwID_compression	Disable_AwID_compression	Yes
Max_outstanding_memory_read_transactions_(RTT_entries)	Max_outstanding_memory_read_transactions_(RTT_entries)	4
Read_data_buffer_protection	Read_data_buffer_protection	SECDED
AdvDataBankScheduling	AdvDataBankScheduling	No
Half_speed_data_SRAM	Half_speed_data_SRAM	No
Use_SRAM_input_flop	Use_SRAM_input_flop	No
Critical_word_first	Critical_word_first	Yes
Enable_ScratchPad_support	Enable_ScratchPad_support	No
Associativity (# of ways)	Associativity (# of ways)	8
Sets	Sets	64
Tag_banks	Tag_banks	1
Data_banks	Data_banks	1
Tag_protection	Tag_protection	SECDED
Data_protection	Data_protection	SECDED

CacheLine_size [bytes]	CacheLine_size [bytes]	128
Enable_way_partitioning	Enable_way_partitioning	Yes
Way_partitioning_user_bits_width	Way_partitioning_user_bits_width	6 (master ID)
Num_of_way_partitioning_registers	Num_of_way_partitioning_registers	8
Primary_selection_bits	Primary_selection_bits	[12:7]
Tag_bank_selection_bits	Tag_bank_selection_bits	[6]
Data_bank_selection_bit	Data_bank_selection_bit	[6]
Replacement_policy	Replacement_policy	NRU
Number_of_replacement_policy_memory_ports	Number_of_replacement_policy_memory_ports	2
Enable_a_pipeline_stage_on_data_storage_input	Enable_a_pipeline_stage_on_data_storage_input	No
Enable_a_pipeline_stage_on_data_storage_output	Enable_a_pipeline_stage_on_data_storage_output	No
Enable_TLM_for_PA	Enable_TLM_for_PA	No
Enable_standalone_TLM	Enable_standalone_TLM	No
RTL_prefix_string	RTL_prefix_string	cachebuffer
Memory_type	Memory_type	SYNOPSYS
RTL_prefix_string	RTL_prefix_string	cachetag
Memory_type	Memory_type	SYNOPSYS
RTL_prefix_string	RTL_prefix_string	cacherpl
Memory_type	Memory_type	REGISTERS
RTL_prefix_string	RTL_prefix_string	buffermem
Memory_type	Memory_type	SYNOPSYS
Enable_Duplication	Enable_Duplication	No
Checker_Delay	Checker_Delay	N/A
Enable_Placeholder	Enable_Placeholder	No
Enable_PerfMonitor	Enable_PerfMonitor	Yes
PerfMonitor_Width	PerfMonitor_Width	32
PerfMonitor_freeRun	PerfMonitor_freeRun	No

The LLC shall make use of the following memory configurations.

Table 47. **LLC memory instance configurations**

Memory	Instances	Words	Bits	ECC	Total Size [B]	Cut Name	Implementation
pc_tag0	1	64	224	0	1792	w64x224b	adsreg
pc_rp0	1	64	8	0	64	w64x8b	internal (registers)
cachebuffer0	1	4096	138	0	70656	w4096x138b	efvspram
buffermem	1	64	139	0	1112	w64x139b	adsreg or efvsprom if adsreg compiler can't be used

During the PDA phase, the performance modelling team has performed a detailed analysis of the SoC performance without and with LLC for two main high-performance multi-master use-cases as provided by BL SysAppl (ref. Building Control & Auto Smart Surface UCs). The detailed analysis can be found in [21]. It has been shown that the SoC can achieve the required performance for both use-cases thanks to the LLC, providing performance headroom of about 10% to 13%.

Note: Performance modelling on RT2660 was showing some potential for dead-lock in MAIN.NIC in multi-master scenarios with the LLC looping back through MAIN.NIC. The modelling has shown the issue resolve when using Single-Slave per ID CDAS mode on the NIC. We need to ensure this case is verified in RTL simulations. – by Jira ticket <https://jira.sw.nxp.com/browse/RT2K-1220>

6.3.4SRAM Controller

The SRAM Controller (SRAMC) offers a memory-mapped interface for interacting with external devices such as FPGAs. Previously, this IP block has been used in i.MX RT1180 and is derived from the SEMC IP.

The main features of the SRAMC IP are:

- Memory-mapped SRAMC to ARM Cortex-M85 AHB-P to achieve fast access ;
- Supports Asynchronous SRAM ;

- Supports 8-/16-bit modes ;
- Supports ADMUX and Non-ADMUX modes ;
- Up to 4 Chip Select (CS) ;
- Up to 128 KB memory size each CS ;
- WAIT signal is supported.

Table 48. IC requirements traceability: SRAM controller requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_MEM_18-2	This device shall include an SRAM port to provide a memory-mapped host interface to external FPGA or ASIC device.	Must have	Yes
iMXRT2660_MEM_18-3	The SRAM interface shall support 8-bit and 16-bit bus width.	Must have	Yes

6.3.5 Bus system

6.3.5.1 NIC-400 Network Interconnect

The CoreLink NIC-400 Network Interconnect is the high-performance system AXI interconnect fabric that interconnects several subsystems, XSPI external memory interfaces and SRAMC interface for external devices.

Table 49. NIC-400 network interconnects

Port #	Master	Protocol	Data Width	Clock	s_m_0	s_m_1	s_m_2	s_m_3	s_m_4	s_m_5
Slave					sramc	xspi1	xspi0	main2cmpt	nic2axbs	l2cache_s
Protocol					axi4	axi4	axi4	axi4	axi4	axi4
Data Width					64	64	64	64	32	128
Port #					350	350	350	350	350	350
m_m_0	comm2main	axi4	64	200 (async)	X	X	X	X	X	X
m_m_1	media2main	axi4	64	350 (async)	X	X	X	X	X	X
m_m_2	cmpt2main0	axi4	64	350	X	X	X	X	X	X
m_m_3	edma5	axi4	64	350	X	X	X	X	X	X
m_m_4	etr	axi4	64	350	X	X	X	X	X	X
m_m_5	axbs2nic	ahb	64	350	X	X	X	X	X	X
m_m_6	l2cache_m	axi4	128	350	X	X	X	X	X	X
m_m_7	apb2ahb_gpv	ahb	32	350						

Table 50. MAIN.NIC ASIB Configuration.

Port	m_m_0	m_m_1	m_m_2	m_m_3	m_m_4	m_m_5	m_m_6	m_m_7
Hookup	comm2main	media2main	cmpt2main0	edma5	etr	axbs2nic	l2cache_m	apb2ahb_gpv
Protocol	AXI4	AXI4	AXI4	AXI4	AXI4	AXI4	AXI4	AHB
Clock	200	350	350	350	350	350	350	350
Addr Width	32	32	32	32	32	32	32	32
Data Width	64	64	64	64	64	32	128	32
Advanced	Prog. GPV	Prog. GPV	Prog. GPV	Prog. GPV	Prog. GPV	Prog. GPV	Prog. GPV	Config Port
Qos	From Master	From Master	From Master	Prog (def.0)	Fixed	Prog (def.0)	From Master	None
T.R.Reg	TBD	TBD	TBD	TBD	TBD	TBD	n/a	
O.T.Reg	TBD	TBD	TBD	TBD	TBD	TBD	n/a	
Lat/Period Reg	TBD	TBD	TBD	TBD	TBD	TBD	TBD	n/a
Security	Per-Access	Per-Access	Per-Access	Per-Access	Per-Access	Per-Access	Per-Access	Secure
Lock	No	No	No	No	No	No	No	No
Eewr	n/a	n/a	n/a	n/a	n/a	Yes	n/a	No
Broken Burst	n/a	n/a	n/a	n/a	n/a	n/a	n/a	Yes
Cdas	SSPID	SSPID	SSPID	SSPID	SS	SSPID	SSPID	SS
Sas ([@Sw] Entry)	No	No	No	No	No	No	No	No
User Width	13	13	13	13	13	13	13	0
Id Width	8	8	8	2	4	6	11	n/a
Id Reduction	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Local Group	grp0	grp0	grp0	grp0	grp0	grp0	grp0	n/a
Rd_Ot	8	8	8	8	1	4	4	1

Wr_Ot	8	8	8	8	32	4	4	1
Tl_Ot	n/a							
Ar Fifo	6	6	0	0	0	0	0	0
Aw Fifo	6	6	0	0	0	0	0	0
R Fifo	6	6	0	0	0	0	0	0
W Fifo	6	6	0	0	0	0	0	0
B Fifo	6	6	0	0	0	0	0	0
Tidemark	Disabled							
Slave Aw	rev	none						
Slave Ar	rev	none						
Slave R	none							
Slave W	rev							
Slave B	none							
Master Aw	none							
Master Ar	none							
Master R	none							
Master W	none							
Master B	none							

Table 51. MAIN.NIC AMIB Configuration.

Port	s_m_0	s_m_1	s_m_2	s_m_3	s_m_4	s_m_5
Hookup	sramc	xspi1	xspi0	main2cmpt	nic2axbs	l2cache_s
Protocol	AXI4	AXI4	AXI4	AXI4	AXI4	AXI4
Clock	350	350	350	350	350	350
Addr Width	32	32	32	32	32	32
Data Width	32	64	64	64	32	128
Advanced	Prog. GPV					
Qos	None	None	None	Yes	Yes	Yes
T.R.Reg	n/a	n/a	n/a	n/a	n/a	n/a
O.T.Reg	n/a	n/a	n/a	n/a	n/a	n/a
Lat/Period Reg	n/a	n/a	n/a	n/a	n/a	n/a
Security	Non-Secure	Non-Secure	Non-Secure	Non-Secure	Non-Secure	Non-Secure
Lock	No	No	No	No	No	No
Eewr	n/a	n/a	n/a	n/a	n/a	n/a
Broken Burst	n/a	n/a	n/a	n/a	n/a	n/a
Cdas	n/a	n/a	n/a	n/a	n/a	n/a
Sas ([@Sw] Entry)	n/a	n/a	n/a	n/a	n/a	n/a
User Width	13	13	13	13	13	13
Id Width	11	11	11	11	11	11
Id Reduction	Yes	Yes	Yes	Yes	Yes	Yes
Local Group	grp0	grp0	grp0	grp0	grp0	grp0
Rd_Ot	1	1	1	8	1	4
Wr_Ot	1	1	1	8	4	4
Tl_Ot	1	1	1	8	4	4
Ar Fifo	0	0	0	0	0	0
Aw Fifo	0	0	0	0	4	0
R Fifo	0	0	0	0	0	0
W Fifo	0	0	0	0	4	0
B Fifo	0	0	0	0	0	0
Tidemark	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
Slave Aw	rev	none	none	none	rev	rev
Slave Ar	rev	none	none	none	rev	rev
Slave R	none	none	none	none	none	none
Slave W	none	none	none	none	none	none
Slave B	none	none	none	none	none	none
Master Aw	none	none	none	none	none	none
Master Ar	none	none	none	none	none	none
Master R	rev	rev	rev	rev	rev	rev
Master W	rev	rev	rev	rev	rev	rev
Master B	rev	rev	rev	rev	rev	rev

The ARM NIC-400 IP is the high-performance system AXI interconnect fabric of the MAIN_SS, referred to as NIC_MAIN. It interconnects several subsystems, XSPI external memory interfaces and SRAMC interface for external devices, and Last-Level Cache. Its operating frequency scales with the processor frequency, namely it runs up to 350 MHz in Normal Run mode. NIC_MAIN is configured as 64-bit bus fabric and maintains a 1:1 clock-synchronous relationship with the other MAIN_SS building blocks. The NIC_MAIN shall be designed such that latency between slave ports and master ports is minimized.

The following NIC_MAIN configuration shall be supported:

- Hierarchical clock gating enabled ;
- Quality of Service feature enabled ;
- Arbitration shall be programmable ;
- 'Single Slave' as Cyclic Dependency Avoidance Scheme (CDAS) ;

Table 52 lists the NIC_MAIN path connectivity between ASIB and AMIB ports.

Table 52. Path connectivity of NIC_MAIN bus fabric

ASIB port	AMIB port						
	SRAMC_AXIS	XSPI2_AXIS	XSPI1_AXIS	XSPI0_AXIS	MAIN2CMPT	NIC2AXBS	LLC_AXIS
COMM2MAIN	-	X	X	X	X	-	X
MEDIA2MAIN	-	X	X	X	X	-	X
CMPT2MAIN	X	X	X	X	-	X	X
DMA0_AXIM	X	X	X	X	X	X	X
ETR	X	X	X	X	X	X	X
AXBS2NIC	X	X	X	X	X	-	X
LLC_AXIM	-	X	X	X	-	-	-
GPV							

'X' indicates a connection, while '-' indicates no connection

Note that all input- and output ports shall be configured as clock synchronous 1:1 and ASYNC, depending on port type.

Table 53. Interface configuration of NIC_MAIN

Interface	Protocol	Width	Sync	Up-Downsize
ASIB port				
M_M_0 COMM2MAIN	AXI4	64b	ASYNC	-
M_M_1 MEDIA2MAIN	AXI4	64b	ASYNC	-
M_M_2 CMPT2MAIN	AXI4	64b	SYNC 1:1	-
M_M_3 DMA0_AXIM	AXI4	64b	SYNC 1:1	-
M_M_4 ETR	AXI4	64b	SYNC 1:1	-
M_M_5 AXBS2NIC	AHB to AXI4	32b	SYNC 1:1	-
M_M_6 LLC_AXIM	AXI4	128b	SYNC 1:1	2:1 Down
M_M_7 GPV	AHB	32b	SYNC 1:1	-
AMIB port				
S_M_0 SRAMC_AXIS	AXI4	64b	SYNC 1:1	-
S_M_1 XSPI2_AXIS	AXI4	64b	SYNC 1:1	-
S_M_2 XSPI1_AXIS	AXI4	64b	SYNC 1:1	-

S_M_3	XSPI0_AXIS	AXI4	64b	SYNC 1:1	-
S_M_4	MAIN2CMPT	AXI4	64b	SYNC 1:1	-
S_M_5	NIC2AXBS	AXI4	32b	SYNC 1:1	-
S_M_6	LLC_AXIS	AXI4	128b	SYNC 1:1	2:1 Up

The NIC_MAIN shall make use of default FIFO depths in order to minimize latency.

6.3.5.2 XHB-500 Bridge

The XEA-1 architecture needs this bridge to pass TZ secure signal (hnonsec) from AHB interconnect (MAIN.AXBS) to an AXI interconnect (MAIN.NIC). The XHB-500 product provides an AMBA AHB5 to AXI5 bridge. The AHB5 to AXI5 bridge translates AHB5 transfers into the corresponding AXI transactions. The bridge has an AHB5 slave interface and an AXI5 master interface. The main features are single power and clock domain, support for early write response, supports all burst types, and buffered write error interrupt. It passes hnonsec to axprot.

Table 54. XHB-500 bridge

Peripheral	Instance	DesignPDM
AHB5 to AXI5 bridge	MAIN.XHB500	arm corelink sie-200 (xhb500_ahb_to_axi_bridge)

Table 55. XHB-500 bridge configuration

Description	MAIN.XHB500
Address bus width, which is fixed at 32bits	32
Sets the width, in bits, of the data bus	32
Sets the width, in bits, of the aruser, awuser, and hauser signals	13
Sets the width, in bits, of the wuser and hwuser signals	13
Sets the width, in bits, of the ruser and hruser signals	13
Sets the width, in bits, of the AXI ID and hmaster signals	6
Controls whether register slices are added to the address phase path	OFF
Controls whether register slices are added to the hwdata path	OFF
Controls whether register slices are added to the hrdtata path	BYPASS
Register slices are added to an AW channel	BYPASS
Register slices are added to an AR channel	BYPASS
Register slices are added to an W channel	BYPASS
Register slices are added to an R channel	BYPASS
Register slices are added to an B channel	BYPASS
Controls whether a 2-stage DFF synchronizer is inserted on the clock Qchannel input	ON
Controls how the bridge responds to an AHB locked transfer	FW_NORMAL
If the bridge receives a Modifiable undefined length incremental burst, this parameter controls the length of the AXI transaction	LENGTH_1
QoS signal	4'b0
Region identifier signal	4'b0
Non-secure Access Identifier (NSAID) signal	4'b0
Interrupt enable: HIGH = Enables the buf_write_error_irq interrupt	HIGH

Note that register slices in control, wdata and rdata AHB paths are disabled. The BE team should enable only slice in paths to be able to close the timing.

Note that register slices in AXI's AW, AR, W, R and B channels are bypassed (disabled). The BE team should enable only slices in these AXI channels to be able to close the timing. The register slices in channels can be set as bypass (no slices), forward (slice is inserted in the valid direction), reverse (slice is inserted in the ready direction) and full (slices are inserted in the valid and ready directions).

6.3.5.3 AXBS_MAIN

The NIC_MAIN is complemented with an AHB 32-bit bus fabric called AXBS_MAIN. The AXBS_MAIN serves as high-performance system AHB interconnect fabric. It interconnects the

microprocessor peripheral bus with the rest of the SoC, and interfaces the high-performance peripheral section as well as other system functions such as security, debug and test infrastructure. This AXBS_MAIN runs at an same operating frequency as NIC_MAIN while maintaining a 1:1 clock-synchronous relationship.

Table 56 lists the AXBS_MAIN master and slave ports and their path connectivity.

Table 56. Path connectivity of AXBS_MAIN bus fabric

Initiator	nic2axbs	cmpt2main1	audio2main	main.edma3	cssi	main.axbs_tbz
Protocol	ahb	ahb	ahb	ahb	ahb	ahb
Data Width	32	32	32	32	32	32

Table 57. MAIN_AXBS connectivity matrix.

Port #	Protocol	Data Width	Initiator	nic2axbs	cmpt2main1	audio2main	main.edma3	cssi	main.axbs_tbz
			Protocol	ahb	ahb	ahb	ahb	ahb	ahb
			Data Width	32	32	32	32	32	32
s0	ahb	32	Clock	350	350	350	350	350	350
s1	ahb	32		350	X	-	X	X	X
s2	ahb	32		350	X	X	-	X	X
s3	ahb	32		350	X	X	-	X	X
s4	ahb	32		350	X	X	-	X	X
s5	ahb	32		350	X	X	-	X	X
s6	ahb	32		350	X	-	-	X	X

X' indicates a connection, while '-' indicates no connection

6.3.5.4 Peripheral Bridge (PBRIDGE)

The Peripheral Bridge (PBRIDGE) controller converts the AMBA AHB interface to a peripheral interface which can either be an IP Skybus or APB interface. The peripheral interface has peripheral module enables allowing the controller to interface to multiple peripherals.

In total, the i.MX RT2660 MAIN_SS contains three PBRIDGE controllers. One PBRIDGE controller interfaces the AXBS_MAIN to downstream configuration registers and peripherals that reside in the MAIN_SS. The other PBRIDGE controllers reside in the HSP_SS. Refer to Section 5.5.2 for the peripheral memory map.

6.3.6 DMA controllers

The enhanced DMA (eDMA) controller is capable of performing complex data transfers with minimal intervention from a host processor. The hardware microarchitecture includes:

- A DMA engine that performs:
 - Source address and destination address calculations ;
 - Data movement operations.
- Local memory containing transfer control descriptors for each of the DMA channels

Fig 17 shows a high level system block diagram of the eDMA controller.

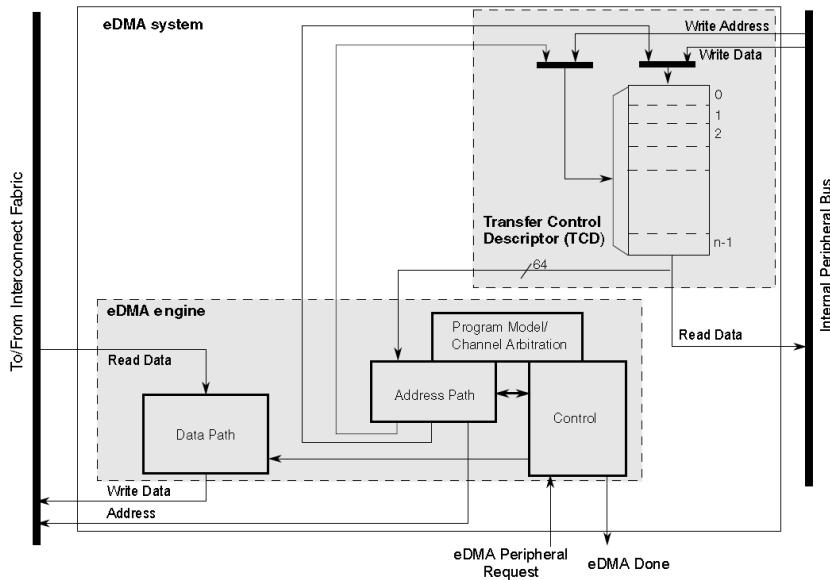


Fig 17. High-level functional block diagram of the enhanced DMA (eDMA) controller

The eDMA is a highly programmable data-transfer engine optimized to minimize any required intervention from the host processor. It is intended for use in applications where the data size to be transferred is statically known and not defined within the transferred data itself.

The i.MX RT2660 is equipped with three enhanced DMA (eDMA) controllers: a first one acting as system DMA controller to support data streaming applications (eDMA5, AXI-based), a second one acting as system DMA controller for peripherals (eDMA3, AHB-based) and a third one acting as DMA controller for the audio subsystem (eDMA3, AHB-based).

Table 58. IC requirements traceability: DMA controller requirements (part i)

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_SCI_2-7	This processor shall include at least one general purpose system DMA to perform data transfer between peripherals and memory or between memory locations.	Must have	Yes
iMXRT2660_SCI_2-8	DMA requests of all peripherals in the SoC that require DMA transfer shall be mapped	Must have	Yes, see Section 5.5.4
iMXRT2660_SCI_2-9	The system DMA(s) shall support operation worst case concurrent data transfers without peripheral FIFO underrun or overflow including during maximum CPU induced load.	Must have	Include in verification plan during design phase

6.3.6.1 eDMA5 controller

The MAIN_SS of i.MX RT2660 includes one eDMA5 engine that is connected to NIC_MAIN.

The main features of the eDMA5 module are:

- The eDMA utilizes an AMBA-AXI4 master interface with support for ACE-Lite ;
- The eDMA generates four output signals to support an external CRC module for read operations. These outputs signal start, end, valid data, and byte strobes ;
- The eDMA utilizes per channel programmer's model access via the IPS bus. Each channel is accessed via its own IPS module enable. This allows completely independent channel access and operation, thus supporting virtualization. Eternal protection mechanisms may control access to each individual channel ;

- When the number of hardware requests exceeds the number of channels, the eDMA automatically generates an internal channel multiplexor which includes additional programmer's model registers and multiplexing logic for the IPD handshake signaling ;
- The eDMA incorporates the ability to masquerade as the core that programmed its TCD on a per channel basis. When enabled, Domain/Master ID, security, and privilege level will reflect the core that programmed that channel. When disabled, the default values are presented during AXI transactions ;
- All data movement via dual-address transfers: read from source, write to destination plus a write-only initialization mode
 - Programmable source and destination addresses and transfer size ;
 - Support for complex address calculations ;
- 64-channel implementation that performs complex data transfers with minimal intervention from a host processor
 - Internal data buffer, used as temporary storage to support large multibyte transfers ;
 - Connections to the interconnect fabric for bus mastering the data movement ;
- Transfer control descriptor (TCD) organized to support two-deep, nested transfer operations
 - 48-byte TCD stored in local memory for each channel ;
 - An inner data transfer loop defined by a minor byte transfer count ;
 - An outer data transfer loop defined by a major iteration count ;
- Channel activation via one of three methods:
 - Explicit software initiation ;
 - Initiation via a channel-to-channel linking mechanism for continuous transfers ;
 - Peripheral-paced hardware requests, one per channel ;
- Fixed-priority and round-robin channel arbitration ;
- Channel completion reported via programmable interrupt requests
 - One interrupt per channel, which can be asserted at completion of major iteration count ;
 - Programmable error terminations per channel and logically summed together to form one error interrupt to the interrupt controller ;
- Programmable support for scatter/gather DMA processing ;
- Support for complex data structures.

Table 59 shows SoC configuration of MAINAIN.eDMA5, Table 60 shows TCD RAM configuration. More detailed information of the eDMA5 IP can be found in its block guide [23].

Table 59. **MAIN.eDMA5 configuration**

Description	Parameter	MAIN.eDMA5
AXI address bus width – Range: 1 to 64 – “ASZ”	AXI_ADDR_WIDTH	64
AXI data bus width – Value: 64 or 128 – “DSZ”	AXI_DATA_WIDTH	64
Number of DMA channels – Range: 1 to 64 – “nCH”	NUMBER_OF_CHANNELS	16
Number of HW IPD requests – Range: 1 to 128 – “nIPD”; If nIPD>nCH internal channel mux is generated	NUMBER_OF_HW_REQS	76
0: User, 1: Priv/Super – CHx_BSR[PAL]	DEFAULT_PROT_PAL	1'b0
0: NonSecured, 1: Secured - CHx_BSR[SEC]	DEFAULT_PROT_SEC	1'b0
0: Data, 1: Instruction – CHx_BSR[INSTR]	DEFAULT_PROT_INSTR	1'b0
1: Allow SW to write to SEC/PAL bits	ENABLE_SW_SEC_CTRL	1'b0
Attribute sideband width – Range: 0 to 8 for the field CHx_BSR[ATTR] to drive “output dma_attributes[ATTR]”	CHn_BSR_ATTR_WIDTH	0
0=AXI4, 1=ACP (ACE5-Lite subset)	AXI_USER_TYPE	1'b0
If AXI_USER_TYPE=1 : Must set to “2” for ACP “axi_aruser[1:0]”	AXI_ARUSER_WIDTH	0
If AXI_USER_TYPE=1 : Must set to “11” for ACP “axi_awuser[10:0]”	AXI_AWUSER_WIDTH	0
Width of the master ID ports – “MSZ”	MASTER_ID_WIDTH	6

Default master ID for this DMA instance	DEFAULT_MASTER_ID	6'h07
Master ID for the overflow error event "output dma_ipi_err_master_id[MSZ-1:0]"	OVFLERR_MASTER_ID	6'h00
1: Combine normal done and error IRQ per channel	COMBINED_IRQ	1
Bandwidth control feature – robust channel arbitration	ENABLE_BWC	1'b0
Functional reset per channel	ENABLE_RESET	1'b0
Local CRC support per channel	ENABLE_CRC	1'b0
Number of DATA_WIDTH-entries in the internal FIFO	FIFO_SZ [# of entries]	64

Table 60. TCD RAM configuration

Memory tcd ram	Instances 1	Words 128	Bits 64	ECC 0	Total Size [B] 1024	Cut Name w128x64b	Implementation adsreg

6.3.6.2 eDMA3 controller

The MAIN_SS of i.MX RT2660 includes one eDMA3 engine that is connected to AXBS_MAIN and acts as system DMA for peripherals.

The main features of the eDMA3 module are:

- Single design supporting 2-32 channel implementations, dependent on size of the TCD memory and design parameters ;
- Connections to the AMBA-AHB crossbar switch for bus mastering the data movement, IPI-SkyBlue (IPS) slave bus for programming the module
 - Parameterized support for 32- and 64-bit AMBA-AHB datapath widths ;
- All data movement via dual-address transfers: read from source, write to destination
 - Programmable source and destination addresses and transfer size ;
 - Support for enhanced addressing modes ;
- 32-channel implementation that performs complex data transfers with minimal intervention from a host processor
 - Internal data buffer, used as temporary storage to support 16-, 32-, and 64-byte transfers ;
 - Connections to the crossbar switch for bus mastering the data movement ;
- Transfer control descriptor (TCD) organized to support two-deep, nested transfer operations
 - 32-byte TCD stored in local memory for each channel ;
 - An inner data transfer loop defined by a minor byte transfer count ;
 - An outer data transfer loop defined by a major iteration count ;
- Channel activation via one of three methods:
 - Explicit software initiation ;
 - Initiation via a channel-to-channel linking mechanism for continuous transfers ;
 - Peripheral-paced hardware requests, one per channel ;
- Fixed-priority and round-robin channel arbitration ;
- Channel completion reported via programmable interrupt requests
 - One interrupt per channel, which can be asserted at completion of major iteration count ;
 - Programmable error terminations per channel and logically summed together to form one error interrupt to the interrupt controller ;
- Programmable support for scatter/gather DMA processing ;
- Support for complex data structures.

Table 61 shows SoC configuration of MAINAIN.eDMA3, Table 62 shows TCD RAM configuration. More detailed information of the eDMA3 IP can be found in its block guide [24].

Table 61. MAIN.eDMA3 configuration

Description	Parameter	MAIN.eDMA3
Databus width of 64	DBW	32
Number of channels	NCH	32
Number of h/w req	NPR	220
AHB priv/user default	AHB_PAL_DEFAULT	1'b0
AHB sec/nonsec default	AHB_SEC_DEFAULT	1'b0
Enable s/w wr to pal/sec	ENB_SW_SECURITY_CTRL	0
AHB attribute width	ASW	0
AHB Initiator ID width	MIW	6
AHB Initiator ID for DMA	AHB_MASTER_ID	6'h06
Enable MID replication	ENB_MID_REPL	1
Done ORed with error on ipi_int	COMBINED_IRQ	1
Invert global write en	ACTIVE_LOW_WE	0
Invert byte write en	ACTIVE_LOW_BWE	0
Endianness of the read data to the write data	BIG_ENDIAN	0
IPS slot size mask	IPS_SLOT_SIZE	14'h4000 (16KB)
Enable ch buffered write	ENB_MP_BUFFWR	0
Enable MP global control	ENB_CH_BUFFWR	1
Enable int read in mpage	ENB_MP_INT	1
Burst buffer depth in bytes	BURST BUFFER SIZE	64

Table 62. TCD RAM configuration

Memory	Instances	Words	Bits	ECC	Total Size [B]	Cut Name	Implementation
tcd ram	1	128	64	0	1024	w128x64b	adsreg

6.3.7 High-Speed Peripheral subsystem (HSP_SS)

The High-Speed Peripheral sub-system (HSP_SS) is embedded within the MAIN_SS with a maximum frequency of up to half the frequency of the CPU. This offers the CPU low-latency access to the HSP_SS. The XEA-1 platform envisions the use of a different HSP_SS configurations for different i.MX RT2K products, each comprising a set of different peripherals.

The HSP_SS contains three AHB-S interfaces that are connected to the AXBS_MAIN bus fabric of MAIN_SS. One of the AHB interfaces provides low-latency access to GPIO, while the other two AHB interfaces provide low-latency access to a PBRIDGE to which the peripherals are connected.

The following sub-subsections provides a functional description of the various peripherals used in the HSP_SS of the i.MX RT2660. Refer to Section 5.5.2 for a high-level overview of the peripheral memory map.

For more detailed information, please refer to the MAIN_SS HW.AS document [4].

*This document includes the RT2660 specific IP configurations
for both the MAIN_SS and the HSP_SS.*

6.3.7.1 Flexible IO (FLEXIO)

The i.MX RT2660 includes three Flexible Input-Output (FLEXIO) modules. All three modules shall offer a low-latency access to the microprocessor, to enable high-speed peripherals emulation.

FLEXIO is a highly configurable module providing a wide range of functionality, including:

- Emulation of various serial or parallel communication protocols ;
- Flexible 16-bit timers with support for various trigger, reset, enable, and disable conditions ;
- Programmable logic blocks which allow the implementation of digital logic functions on-chip and configurable interaction of internal and external modules ;
- Programmable state machine for offloading basic system control functions from the CPU.

Fig 18 shows a high-level functional block diagram of the FLEXIO.

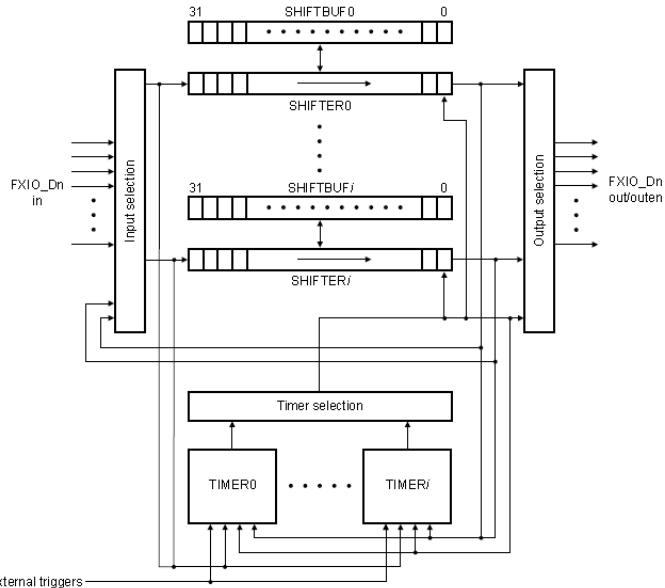


Fig 18. FLEXIO IP block diagram

FLEXIO includes the following features:

- Array of 32-bit shift registers with transmit, receive, data match, logic, and state modes:
 - Double-buffered shifter operation for continuous data transfer ;
 - Shifter concatenation to support large transfer sizes ;
 - Automatic start and stop bit generation ;
 - 1, 2, 4, 8, 16, or 32 multi-bit shift widths for parallel interface support ;
 - Interrupt, DMA, or polled transmit and receive operation.
- Highly flexible 16-bit timers with support for various internal or external trigger, reset, enable, and disable conditions:
 - Programmable baud rates independent of bus clock frequency, with support for asynchronous operation during Stop mode ;
 - Programmable logic mode for integrating external digital logic functions on-chip, or combining pin, shifter, or timer functions to generate complex outputs ;
 - Programmable state machine for offloading basic system control functions from CPU, with support for up to eight states, eight outputs, and three selectable inputs per state ;
- Integrated general-purpose input/output registers and pin rising or falling edge interrupts to simplify software support ;
- Support for a wide range of protocols, including but not limited to:
 - UART, I2C, SPI, and/or I2C ;
 - Camera I/F ;
 - Motorola 68K or Intel 8080 bus ;
 - PWM or waveform generation ;
 - Input-capture (pulse edge interval measurement), such as SENT.

More detailed information of the FLEXIO IP can be found in its block guide [25].

Table 63. IC requirements traceability: FlexIO requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_CIO_6-2	This processor shall implement three instances of the FlexIO.	Must have	Yes
iMXRT2660_CIO_6-3	The FlexIOs need to be placed and optimized for low access latency from the application CPU.	Must have	Yes, see Fig 9
iMXRT2660_CIO_6-4	Each FlexIO can be configured to support up to 8 full-duplex SPI interfaces	Must have	Yes, see Error! Reference source not found.

6.3.7.2 LPUART

The Low Power Universal Asynchronous Receiver/Transmitter (LPUART) module provides asynchronous, serial communication capability with external devices. LPUART supports non-return-to-zero (NRZ) encoding format and IrDA compatible infrared (lowspeed) SIR format. The LPUART can continue operating while the processor is in a standby mode if an appropriate peripheral clock is available. Fig 19 shows the LPUART functional block diagram.

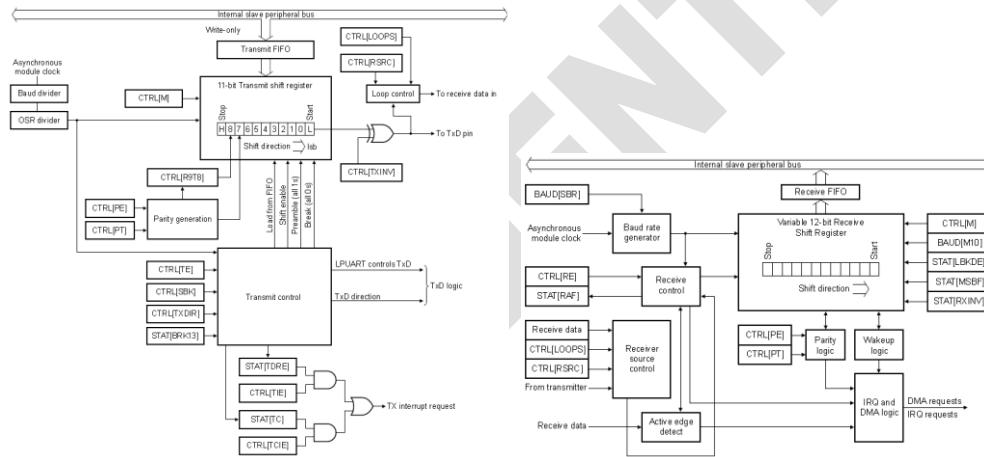


Fig 19. LPUART IP block diagram: transmitter (left), receiver (right)

Following are the main features of the LPUART module.

- Full-duplex, standard non-return-to-zero (NRZ) format ;
- Programmable baud rates (13-bit modulo divider) with configurable oversampling ratio from 4x to 32x ;
- Asynchronous operation of transmit and receive baud rate with respect to the bus clock:
 - Baud rate can be configured independently of the bus clock frequency ;
 - Supports operation in Stop modes ;
- Interrupt, DMA or polled operation:
 - Transmit data register empty and transmission complete ;
 - Receive data register full ;
 - Receive overrun, parity error, framing error, and noise error ;
 - Idle receiver detect ;
 - Active edge on receive pin ;
 - Break detect supporting LIN ;
 - Receive data match ;
- Hardware parity generation and checking ;
- Programmable 7-bit, 8-bit, 9-bit or 10-bit character length ;
- Programmable 1-bit or 2-bit stop bits ;

- Support for three receiver wakeup methods:
 - Idle line wakeup ;
 - Address mark wakeup ;
 - Receive data match ;
- Automatic address matching to reduce ISR overhead:
 - Address mark matching ;
 - Idle line address matching ;
 - Address match start, address match end ;
- Optional 13-bit/11-bit break character generation ;
- Configurable idle length detection supporting 1, 2, 4, 8, 16, 32, 64, or 128 idle characters ;
- Selectable transmitter output and receiver input polarity ;
- Hardware flow control support for request to send (RTS) and clear to send (CTS) signals ;
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse width ;
- Independent FIFO structure for transmit and receive ;
- Separate configurable watermark for receive and transmit requests ;
- Option for receiver to assert request after a configurable number of idle characters if receive FIFO is not empty.

The i.MX RT2660 contains a total of eight LPUART modules, of which six reside in the HSP_SS.

More detailed information on the LPUART IP can be found in its block guide [26].

Table 64. IC requirements traceability: UART requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_CIO_1-3	This processor shall implement at least 8x LPUART instances	Must have	Yes, HSP_SS: 6x, WAKE_SS: 2x
iMXRT2660_CIO_1-4	All UART ports are compatible with RS-232 & RS-485 protocols	Must have	IP supports
iMXRT2660_CIO_1-5	All UART modules shall support LIN protocol	Must have	IP supports (w/ break detection)
iMXRT2660_CIO_1-6	All UART modules shall support Profibus protocol	Must have	IP supports (12Mbps with x8 oversampling)
iMXRT2660_CIO_1-7	All UART modules shall support IrDA 1.4 return-to-zero-inverted operation	Must have	IP supports
iMXRT2660_CIO_1-10	All UART modules shall support 7 / 8 / 9 / 10-bit character lengths	Must have	Yes
iMXRT2660_CIO_1-11	All UART modules shall support hardware flow control for request-to-send and clear-to-send	Must have	Yes
iMXRT2660_CIO_1-12	All UART modules shall support automatic address matching on address mark matching, idle line address matching, and address match start and end.	Must have	Yes
iMXRT2660_CIO_1-13	All UART modules can wake-up from idle line, address mark, and receive data match	Must have	Yes
iMXRT2660_CIO_1-14	All UART modules shall operate down to "Sleep" mode	Must have	Yes
iMXRT2660_CIO_1-15	At least 2 UART modules shall operate down to "Deep Sleep" mode	Must have	Yes, 2x UART in WAKE_SS

6.3.7.3 LP SPI

The Low Power Serial Peripheral Interface (LP SPI) provides an efficient interface to a SPI bus, either as a master or slave. A SPI bus is a synchronous serial communication interface used in embedded systems. It is typically used to perform short distance communications between microcontrollers and peripheral devices, on printed circuit boards.

The LPSPI module uses little CPU overhead, with DMA offloading of FIFO register accesses. It can continue to operate in standby modes if an appropriate clock is available. Fig 20 shows the LPSPI functional block diagram.

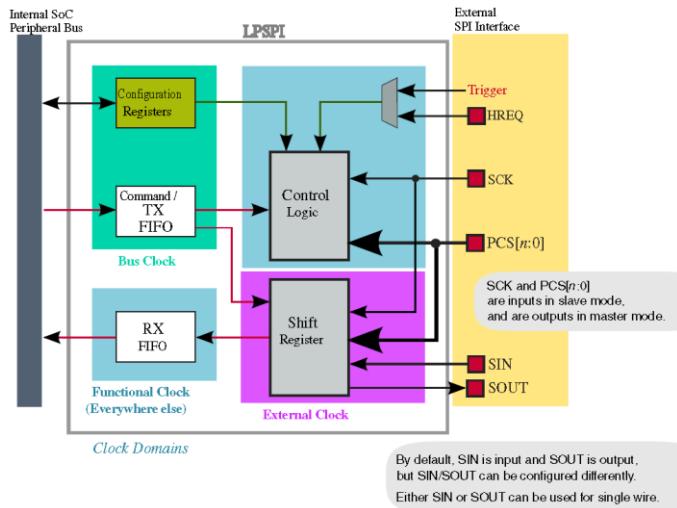


Fig 20. LPSPI IP block diagram

The following main features are supported:

- 32-bit word size ;
- Configurable clock polarity and phase ;
- Master mode - supports 4 peripheral chip selects ;
- Slave mode ;
- 16-word transmit and command FIFO ;
- 16-word receive FIFO ;
- Flexible timing parameters in Master mode, including SCK frequency and delays between PCS and SCK edges ;
- Full-duplex transfers support 1-bit transmit and receive on each clock edge ;
- Half-duplex transfers support:
 - 1-bit transmit or receive on each clock edge ;
 - 2-bit transmit or receive on each clock edge (Master mode only) ;
 - 4-bit transmit or receive on each clock edge (Master mode only) ;
- Receive data match logic supports discard of non-matching data and interrupt on data match.

The i.MX RT2660 contains a total of six LPSPI modules, of which five reside in the HSP_SS...More detailed information on the LPSPI IP can be found in its block guide [27].

Table 65. IC requirements traceability: SPI requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_CIO_2-2	This processor shall implement at least 6x LPSPI instances	Must have	Yes, HSP_SS: 5x, WAKE_SS: 1x
iMXRT2660_CIO_2-3	All SPI ports shall support Motorola SPI specification V03.06 for both Master and Slave modes	Must have	IP supports
iMXRT2660_CIO_2-4	All SPI ports shall support Dual IO SPI and Quad IO SPI in both Master and Slave modes.	Must have	Yes
iMXRT2660_CIO_2-7	All SPI ports shall operate down to "Sleep" mode	Must have	Yes
iMXRT2660_CIO_2-8	At least 1 SPI shall operate down to "Deep Sleep" mode	Must have	Yes, in WAKE_SS

6.3.7.4 LPI2C

The LPI2C is a low power Inter-Integrated Circuit (I2C) module that supports an efficient interface to an I²C bus as a master and/or as a slave. It implements logic support for Standard-mode, Fast-mode, Fast-mode plus and Ultrafast modes of operation. It also complies with the System Management Bus (SMBus) Specification, version 3.

The LPI2C module uses little CPU overhead, with DMA offloading of FIFO register accesses. It can continue to operate in standby modes if an appropriate clock is available. Fig 21 shows the LPI2C functional block diagram.

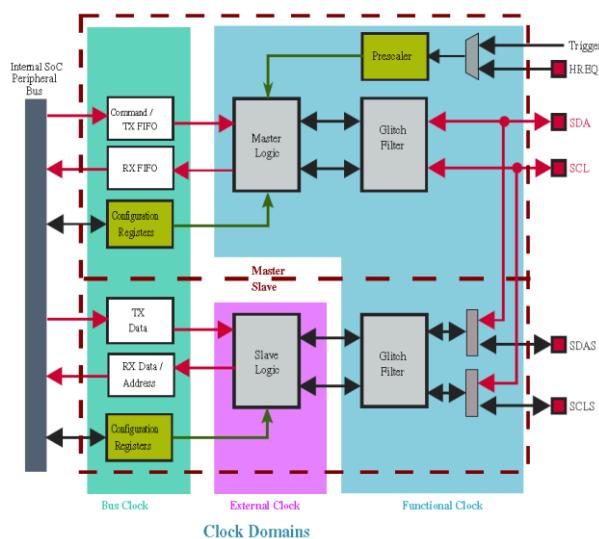


Fig 21. LPI2C IP block diagram

The following main features are supported:

- Standard, Fast, Fast+ and Ultra Fast modes are supported ;
- High speed mode (HS) in slave mode ;
- Multi-master support, including synchronization and arbitration. Multi-master means any number of master nodes can be present. Additionally, master and slave roles may be changed between messages (after a STOP is sent) ;
- Clock stretching: Sometimes multiple I²C nodes may be driving the lines at the same time. If any I²C node is driving a line low, then that line will be low. I²C nodes that are starting to transmit a logical one (by letting the line float high) can detect that the line is low, and thereby know that another I²C node is active at the same time.
 - When node detection is used on the SCL line, it is called clock stretching, and clock stretching is used as a I²C flow control mechanism for multiple slaves ;
 - When node detection is used on the SDA line, it is called arbitration, and arbitration ensures that there is only one I²C node transmitter at a time ;
- General call, 7-bit and 10-bit addressing ;
- Software reset, START byte and Device ID (also require software support).

The LPI2C master supports:

- Command/transmit FIFO of 4words (8-bit transmit data + 3-bit command) ;
- Receive FIFO of 4words (8-bit receive data) ;
- Command FIFO will wait for idle I²C bus before initiating transfer ;
- Command FIFO can initiate (repeated) START and STOP conditions and one or more master-receiver transfers ;

- STOP condition can be generated from command FIFO, or generated automatically when the transmit FIFO is empty ;
- Host request input to control the start time of an I2C bus transfer ;
- Flexible receive data match can generate interrupt on data match and/or discard unwanted data ;
- Flag and optional interrupt to signal Repeated START condition, STOP condition, loss of arbitration, unexpected NACK, and command word errors ;
- Supports configurable bus idle timeout and pin-stuck-low timeout.

The LPI2C slave supports:

- Separate I2C slave registers to minimize software overhead because of master/slave switching ;
- Support for 7-bit or 10-bit addressing, address range, SMBus alert and general call address
- Transmit data register that supports interrupt or DMA requests ;
- Receive data register that supports interrupt or DMA requests ;
- Software-controllable ACK or NACK, with optional clock stretching on ACK/NACK bit ;
- Configurable clock stretching, to avoid transmit FIFO underrun and receive FIFO overrun errors ;
- Flag and optional interrupt at end of packet, STOP condition, or bit error detection.

The i.MX RT2660 contains a total of four LPI2C modules, of which two reside in the HSP_SS.

More detailed information on the LPI2C IP can be found in its block guide [28].

Table 66. IC requirements traceability: I2C requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_CIO_3-2	This processor shall implement at least 4 LPI2C instances	Must have	Yes, HSP_SS: 2x, WAKE_SS:2x
iMXRT2660_CIO_3-3	All I2C modules shall support the NXP I2C Bus Specification (Revision 6) in following operation modes: 1) Standard-mode operation (100kbps) 2) Fast-mode operation (400kbps) 3) Fast-mode Plus operation (1Mbps) 4) High-speed mode operation (3.4Mbps)	Must have	IP supports, High-speed mode not supported due to missing IO
iMXRT2660_CIO_3-4	All I2C modules shall support SMBus operation	Must have	IP supports
iMXRT2660_CIO_3-5	All I2C modules shall support clock stretching in master and slave mode	Must have	Yes
iMXRT2660_CIO_3-6	All I2C modules shall support 7-bit and 10-bit addressing in master and slave mode	Must have	Yes
iMXRT2660_CIO_3-7	All I2C modules shall support general call address in master and slave mode	Must have	Yes
iMXRT2660_CIO_3-8	All I2C modules shall operate down to "Sleep" mode	Must have	Yes
iMXRT2660_CIO_3-9	At least 2 I2C modules shall operate down to "Deep Sleep" mode	Must have	Yes, 2x LPI2C in WAKE_SS

6.3.7.5 I3C

The MIPI Alliance Improved Inter-Integrated Circuit (MIPI I3C) improves upon the use and power of I2C, and provides an alternative to SPI for mid-speed applications. The I3C peripheral supports all required and most optional features of the MIPI Alliance Specification for I3C, v1.0 and v1.1, except for ternary data rates (HDR-TSP and HDR-TSL).

Fig 22 shows a high-level block diagram of the I3C module.

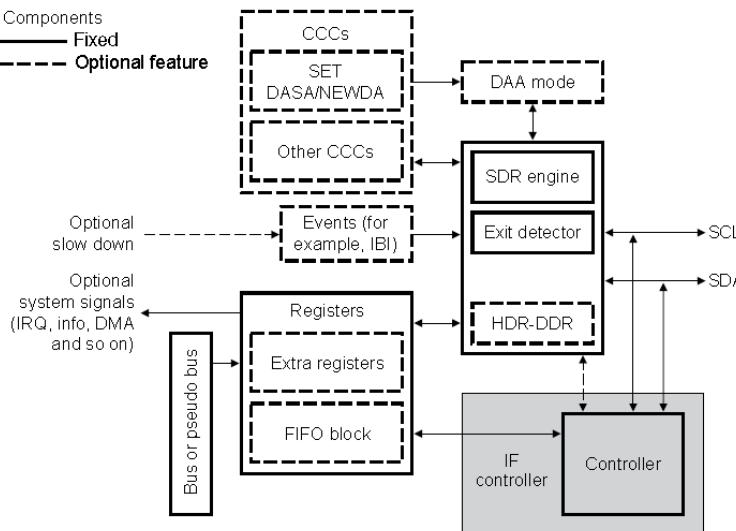


Fig 22. I3C IP block diagram

The main features of the I3C module are as follows:

- Two-wire multi-drop bus capable of 12.5 MHz clock speeds, with up to 11 devices
 - Dynamically assigns target addresses, and targets do not require static addresses. However, targets may have an I2C static address assigned at start-up, so the target can operate on an I2C bus. By default, I3C supports seven-bit I2C-style addresses ;
 - Allows targets to use the inbound SCL clock as the peripheral clock (instead of the clock from the controller) so devices can have slow or inaccurate clocks internally ;
 - Allows simple targets, such as temperature sensors, to have no internal clock.
 - I3C controller supports handoff from Open Drain to Push-Pull mode for ACK to data transfer ;
 - Normally the controller terminates the read, but for I3C, the target can also end the read ;
- In-Band Interrupts (IBI) allow targets to send notifications to a controller
 - Can be equivalent to a separate GPIO, but can also be directly data-bearing ;
 - Can be prioritized. When multiple targets send interrupts to a controller at the same time, the order is resolved ;
- Dynamic addresses establish the priority of the targets, so the controller controls the priority of the targets. Targets with lower-value dynamic addresses are higher priority level IBIs.
 - Can start interrupts even when the controller is not active on the bus. No free-running clock is needed; starting an interrupt requires a Bus Available condition ;
 - Can resolve an initial event via a time-stamping option, not requiring an interrupt;
- Built-in commands for application created in SW/FW by using register interface are kept in a separate space. These commands do not collide with normal controller-to-target messages
 - Controls bus behavior, modes and states, low-power state, inquiries, and more ;
 - Has additional room for new built-in commands to be used by other groups ;
- Organized forms of multi-controller modes:
 - Secondary controllers, which use clean handoffs between different controllers ;
- Hot-join onto I3C bus allows devices to connect to the bus later than when the bus starts
 - Enables a device or module to get onto the I3C bus when it woke up after power-up or was physically inserted onto the I3C bus ;
 - Provides a clean method for notification when new devices or modules get onto the I3C bus ;
- Can use both I2C and I3C buses

- I3C supports specific legacy I2C devices on the bus ;
- I3C target devices can operate on I2C buses ;
- Supports bridging to I2C, SPI, UART, and other buses ;
- Special mode for old-style I2C buses (no targets) with clock stretching ;
- Higher data rate modes are available:
 - Has a High Data Rate - Double Data Rate (HDR-DDR) mode, which is double the data rate of SDR ;
 - Only the controller and the specific target must support the higher data rate. The other targets can ignore it.

The I3C peripheral supports most of the I3C features, except for the ternary data rates (HDR-TSP and HDR-TSL) and peer-to-peer messaging, which are not supported.

The i.MX RT2660 includes a total of two I3C modules, of which one resides in the HSP_SS.

More detailed information on the I3C module can be found in its block guide [29].

Table 67. IC requirements traceability: I3C requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_CIO_4-2	This processor shall implement at least 2 I3C ports	Must have	Yes
iMXRT2660_CIO_4-3	All I3C modules shall support the MIPI Alliance I3C Specification: 1) I3C Single Data Rate (SDR) Mode 2) I3C Dual Data Rate (HDR-DDR) Mode	Must have	Yes
iMXRT2660_CIO_4-5	All I3C modules shall support In-Band Interrupt Requests for both Master and Slave modes	Must have	Yes
iMXRT2660_CIO_4-6	All I3C modules shall support Hot-Join Event Generation for both Master and Slave modes	Must have	Yes
iMXRT2660_CIO_4-7	All I3C modules shall support Peer-to-Peer Data Transfer Requests for both Master and Slave modes	Must have	Yes
iMXRT2660_CIO_4-8	All I3C modules shall support Requests to become Current Master for both Master and Slave modes	Must have	Yes
iMXRT2660_CIO_4-9	All I3C modules shall support Peer-to-Peer Slave Role in Slave mode	Must have	Yes
iMXRT2660_CIO_4-10	All I3C modules shall operate down to "Sleep" mode	Must have	Yes
iMXRT2660_CIO_4-11	At least 1 I3C shall operate down to "Deep Sleep" mode	Must have	Yes, 1x I3C in WAKE_SS
iMXRT2660_CIO_4-12	All I3C shall support I2C mode.	Must have	Yes

6.3.7.6 Controller Area Network with Flexible Data Rate (CANFD)

The i.MX RT2660 contains three CANFD modules.

The CANFD module is a communication controller implementing the CAN protocol according to the ISO 11898-1 and CAN 2.0B protocol specifications. The CAN protocol was primarily designed to be used as a vehicle serial data bus meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. The CANFD module is a full implementation of the CAN protocol specification, which supports both standard and extended message frames. 64 Message Buffers are supported. Fig 23 shows the CANFD functional block diagram.

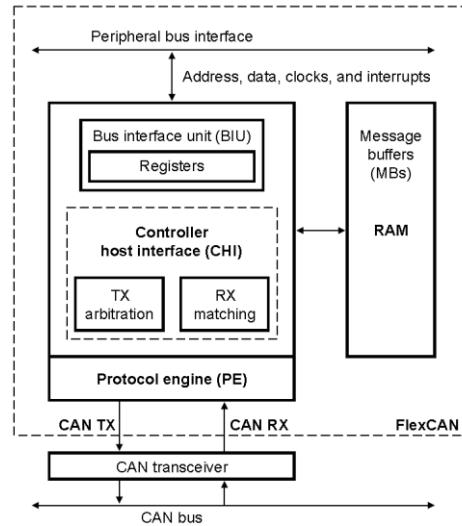


Fig 23. CANFD IP block diagram

Main features of the CANFD module are:

- Full implementation of the CAN with Flexible Data Rate (CAN FD) protocol specification and AN protocol specification, Version 2.0B:
 - Standard data and remote frames ;
 - Extended data and remote frames ;
 - Zero to eight bytes data length ;
 - Programmable bit rate up to 1Mb/sec ;
 - Content-related addressing.
- Compliant with the ISO 11898-1 standard ;
- Flexible Mailboxes of 0 to 8, 16, 32 or 64 bytes data length ;
- Each Mailbox is configurable as Rx or Tx, all supporting standard and extended messages
- Individual Rx Mask Registers per Mailbox ;
- Full featured Rx FIFO with storage capacity for 6 frames and internal pointer handling ;
- Powerful Rx FIFO ID filtering, capable of matching incoming IDs against either 128 extended, 256 standard or 512 partial (8 bits) IDs, with up to 32 individual masking capability ;
- Connect tmr_tick_ext PIT trigger out to get uniform increase on free running timer.

Table 68. FlexCAN configurations.

Description	Parameter	HSP.FLEXCAN0	HSP.FLEXCAN1	HSP.FLEXCAN2
Number of message buffer	NUMBER_OF_MB	8'd96	8'd96	8'd96
MDIS bit reset value	MDIS_RST_VALUE	1'b1	1'b1	1'b1
Locks IRMQ bit in its reset value (0)	LOCK_IRMQ	1'b0	1'b0	1'b0
IPS bus address size	ADDR_SIZE	16	16	16
Rx individual mask feature enable	IRMQ_EN	1'b1	1'b1	1'b1
Reset value for tx arbitration delay	TASD_RST_VALUE	5'd12	5'd12	5'd12
ECC feature enable	ECC_EN	1'b1	1'b1	1'b1
DMA feature enable	DMA_EN	1'b1	1'b1	1'b1
Pretended Network feature enable	PNET_EN	1'b0	1'b0	1'b0
CAN FD protocol enable	FD_EN	1'b1	1'b1	1'b1
High resolution time stamp enable	TIME_STAMP_EN	1'b1	1'b1	1'b1
Extended MB memory region enable	ENHANCE_MB_MEM	1'b0	1'b0	1'b0
Enhanced RX FIFO enable	ERX_FIFO_EN	1'b1	1'b1	1'b1
Number of Enhanced RX FIFO filter elements	ERX_FIFO_FLT_ELEM	8'd128	8'd128	8'd128
Depth of Enhanced RX FIFO	ERX_FIFO_SIZE	6'd32	6'd32	6'd32

Enables the set of registers to extend CAN bit timing variables	CIA_BIT_TIMING	1'b1	1'b1	1'b1
On-chip network feature enable	ONCHIP_NETWORK	1'b0	1'b0	1'b0

More detailed information on the CANFD IP can be found in its block guide [30].

Table 69. IC requirements traceability: CAN requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_CIO_5-2	This processor shall implement at least 3 CAN ports	Must have	Yes
iMXRT2660_CIO_5-3	All CAN modules shall support the following Controller Area Network standards: 1) CAN 2.0B Specification 2) ISO 11898-1	Must have	Yes
iMXRT2660_CIO_5-4	All CAN modules shall implement an internal 32-bit free-running timer for time stamping	Must have	Yes
iMXRT2660_CIO_5-5	All CAN modules shall support synchronized "global" network time through messaging	Must have	Yes
iMXRT2660_CIO_5-6	All CAN modules shall support "Listen-Only" operation	Must have	Yes
iMXRT2660_CIO_5-7	All CAN modules shall support transmission abort operation	Must have	Yes
iMXRT2660_CIO_5-8	All CAN modules shall implement CRC status for transmitted messages	Must have	Yes
iMXRT2660_CIO_5-9	All CAN modules shall support FD operation	Must have	Yes
iMXRT2660_CIO_5-10	CAN FD function can be disabled through fusing	Must have	Yes
iMXRT2660_CIO_5-11	All CAN modules shall operate down to "Sleep" mode	Must have	Yes

6.3.7.7 Messaging Unit (MU)

The Messaging Unit module (MU) enables two processors on a chip to communicate and coordinate by passing messages (for example, data, status, and control) through the MU interface. MU also provides the ability for one processor to signal the other processor using interrupts. The i.MX RT2660 utilizes the MU for interactions between CSSI and CPU.

Because MU can manage the messaging between processors using different clocks, MU must synchronize the accesses from one side to the other. MU accomplishes synchronization using two sets of matching registers: Processor A-facing and Processor B-facing. Fig 24 shows high-level functional block diagram of the MU.

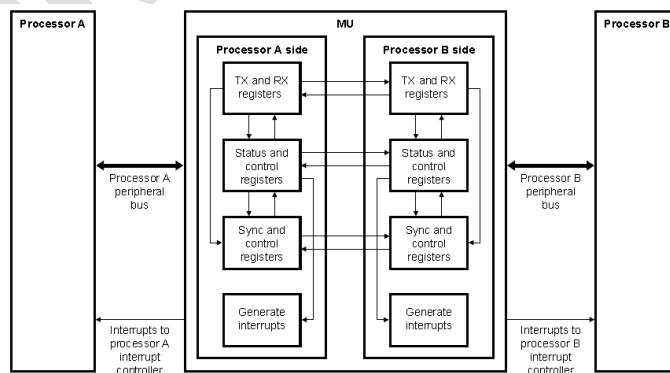


Fig 24. MU block diagram

The MU offers the following main features:

- Memory-mapped registers

- MU is connected as a peripheral under the peripheral bus on the Processor A-side and Processor B-side ;
- Synchronized message transfers between cores
 - To send data or messages from one side to the other, MUA provides 4 transmit registers and 4 receive registers, MUB provides 4 transmit registers and 4 receive registers
 - Transmit Empty and Receive Full flags facilitate the transfer of data or messages between cores on both sides of MU ;
 - Transmit and receive flags are updated via a synchronization mechanism ;
 - MU has a 3-bit flag data register, which can be used to send flag data between the two MU sides ;
- Inter-processor interrupts
 - MU has 12 interrupt sources on each side (Processor A-side, Processor B-side) for signaling the other processor. The interrupts can be used for notification of receive and transmit events and for general-purpose signaling between processors. There are 4 general-purpose interrupt requests available and 8 receive and transmit interrupt sources
 - Processor A can initiate a Non-Maskable Interrupt to Processor B ;
 - Processor B can initiate a Non-Maskable Interrupt to Processor A ;
- Flexible processor configuration
 - A processor can issue a programmed hardware reset to the other processor by writing 1 to CCR0[HR] ;
 - The processor platform clock can be enabled to continue running when the processor enters Stop mode, until the other processor also enters Stop mode. This feature allows the processor to continue accessing peripherals on the bus of the other processor, even when it has entered Stop mode.
- Reset
 - Each processor can issue a reset to the entire MU module, using CR[MUR] in each processor ;
 - CR[MUR] is a self-clearing field.

6.3.7.8 Quad Timer/PWM module (QTPM)

The Quad Timer/PWM (QTPM) module implements functionalities offered by the Quad Timer (QTimer) and Timer/PWM module (TPM) into a single component. The i.MX RT2660 contains four Quad Timer/PWM (QTPM) modules; three QTPM are located in the HSP_SS and one QTPM module is located in the WAKE_SS.

Fig 25 shows high-level functional block diagram of the QTPM.

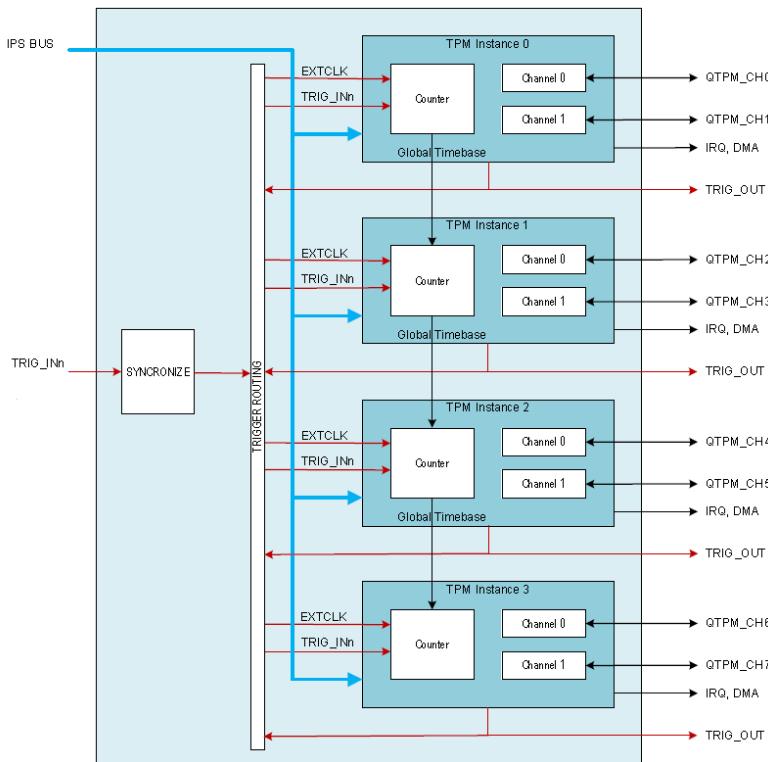


Fig 25. QTPM module block diagram

The QTPM main features are as follows

- A wrapper around four 2-channel TPM instances on same functional clock ;
- Global timebase connection supports enabling multiple counters on same clock cycle ;
- Implement common synchronization for external triggers/inputs; shared by all submodules ;
- Internal predefined trigger connections between the different submodules ;
- Software compatible with TPM, consistent software view for implementing complex timer functions that require multiple timebases.

The envisioned use-cases of the QTPM are listed below.

- Frequency measurement: Count number of pulses within a defined time period ;
- Average duty cycle: Count how often input is high during a defined time period ;
- Pulse output stream (GM heartbeat): Output defined number of output pulses of defined width at a defined periodic interval ;
- PWM output: Output defined number of PWM outputs and then stop ;
- Delayed PWM: Wait defined delay and then output defined number of PWM outputs ;
- Multiple timebases
 - Generate multiple outputs with different (synchronized) periods ;
 - Input capture with reset supports measuring time between edges ;
 - Count number of overflows during input capture.

The QTPM is a new IP that makes use of TPM as sub-modules. The TPM is configured as a 2-channel timer which supports input capture, output compare, and the generation of PWM signals to control electric motor and power management applications. The counter, compare and capture registers are clocked by an asynchronous clock that can remain enabled in low power modes. Fig 26 shows a functional block diagram of the TPM module.

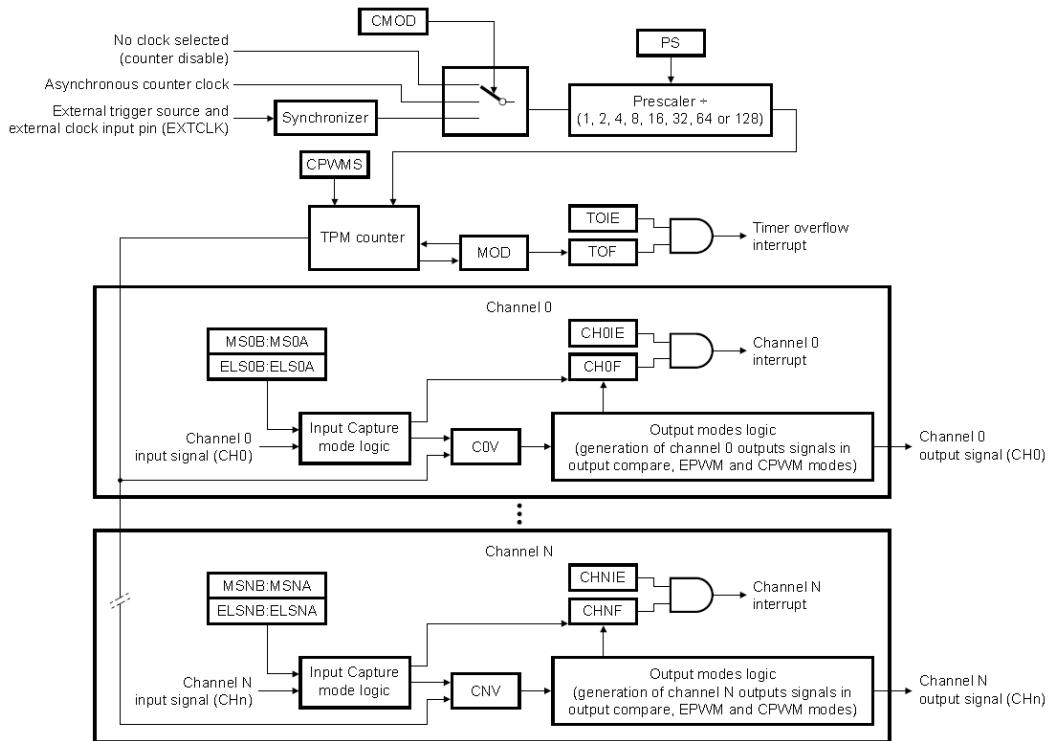


Fig 26. TPM sub-module block diagram

The TPM features include:

- TPM clock mode is selectable ;
 - Can increment on every edge of the asynchronous counter clock ;
 - Can increment on rising edge of an external clock input synchronized to the asynchronous counter clock ;
- Prescaler divide-by 1, 2, 4, 8, 16, 32, 64, or 128 ;
- TPM includes a 32-bit counter ;
 - It can be a free-running counter or modulo counter ;
 - The counting can be up or up-down ;
- Includes 6 channels that can be configured for input capture, output compare, edge-aligned PWM mode, or center-aligned ;
- PWM mode ;
 - In input capture mode the capture can occur on rising edges, falling edges or both edges ;
 - In output compare mode the output signal can be set, cleared, pulsed, or toggled on match ;
 - All channels can be configured for edge-aligned PWM mode or center-aligned PWM mode ;
- Support the generation of an interrupt and/or DMA request per channel ;
- Support the generation of an interrupt and/or DMA request when the counter overflows ;
- Support selectable trigger input to optionally reset or cause the counter to start incrementing ;
 - The counter can also optionally stop incrementing on counter overflow ;
- Support the generation of hardware triggers when the counter overflows and per channel.

The new QTPM IP shall support the following configuration options.

1. A TPM parameter to remove external input synchronizers. Implement common synchronizers shared by all submodules in QTPM wrapper ;

2. TPM parameters to minimize overlap with QDC /FlexPWM:
 - o CPWM_EN = 0 (new parameter)
 - o FILTER_EN = 0 (existing parameter)
 - o COMB_EN = 1 (new parameter)
 - o QUAD_EN = 0 (existing parameter)
 - o GTB_EN = 1 (new parameter)

Table 70. IC requirements traceability: Timer with Pulse Width Modulator requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_TMR_1-3	This processor shall include 6x instances of TPM.	Must have	Yes, HSP_SS: 3x QTPM=12x TPM WAKE_SS: 1x QTPM=4xTPM
iMXRT2660_TMR_1-5	The TPM shall support start, reset, or increment counter on trigger input and stop on compare.	Must have	Yes
iMXRT2660_TMR_1-7	Inputs and outputs of TPM should be connected to input and output channels of the XBAR.	Must have	Yes

Table 71. IC requirements traceability: QTPM requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_TMR_5-2	The Device shall include 4x instance of QTPM.	Must have	Yes
iMXRT2660_TMR_5-3	QTPM is typically used in motor control applications. Each QTPM has four 32-bit counter/timer sub-modules. Any of the four timer sub-modules can be used for rotor position detection from the quadrature encoder signals. Likewise, any of the sub-modules can be used for any timer input edge time capturing.	Must have	Yes
iMXRT2660_TMR_5-4	Each QTPM sub-module has one primary input and one secondary input. The inputs should be multiplexed on GPIO and connected to the output channel of the XBARs.	Must have	Yes

6.3.7.9 Low-Power Periodic Interrupt Timer (LPIT)

The i.MX RT2660 contains two Low-Power Periodic Interrupt Timer (LPIT) modules.

The LPIT is a basic 32 bit counter timer. It features 32-bit counter timer, programmable count modulus, clock division features, interrupt generation, and ability to chain adjacent timers to achieve longer interval. Fig 27 shows a functional block diagram of the LPIT module.

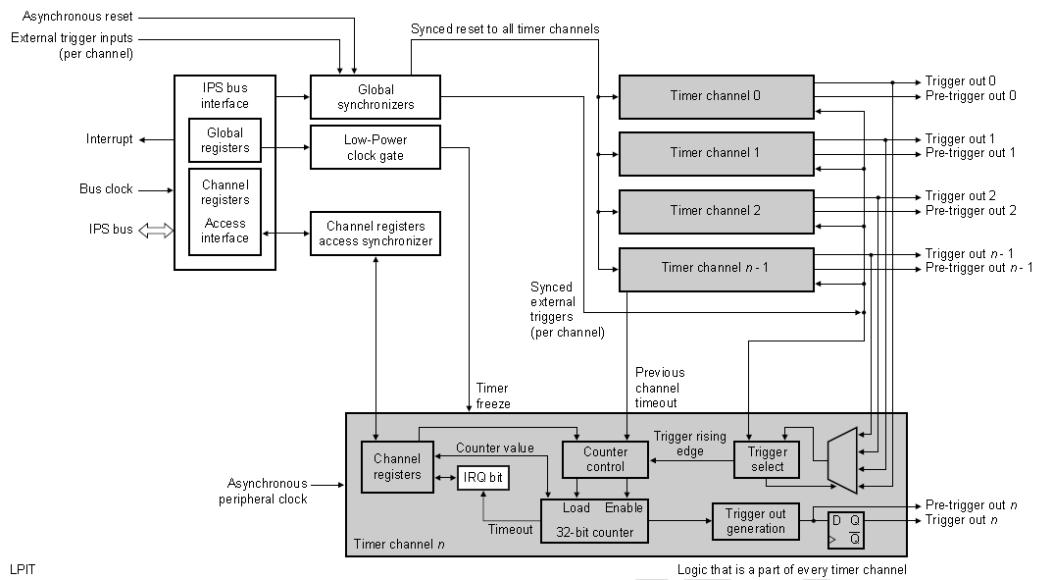


Fig 27. LPIT IP block diagram

More detailed information on the LPIT module can be found in its block guide [31].

Table 72. IC requirements traceability: Periodic Interrupt Timer requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_TMR_2-2	This processor shall include 2x instances of PIT	Must have	Yes
iMXRT2660_TMR_2-3	The LPIT is a 32-bit counter which generates a periodic interrupt on counter timeout.	Must have	Yes
iMXRT2660_TMR_2-5	The LPIT has 4 channels, and each channel has its own trigger input and output. Trigger input and output of the PIT should be connected to output and input channels of the XBAR modules.	Must have	Yes
iMXRT2660_TMR_2-6	User may chain channels to extend counter period. When one channel counter timeout, it triggers the next chained channel to start counting.	Must have	Yes

6.3.7.10 Enhanced Flexible PWM (eFLEXPWM)

The i.MX RT2660 contains four enhanced flexible pulse width modulator (eFlexPWM) modules.

The eFlexPWM module contains PWM submodules, each of which is set up to control a single half-bridge power stage. Fault channel support is provided. eFLEXPWM can generate various switching patterns, including highly sophisticated waveforms. It is ideal for controlling different Switched Mode Power Supplies (SMPS) topologies.

Fig 28 shows a high-level block diagram of the eFLEXPWM module.

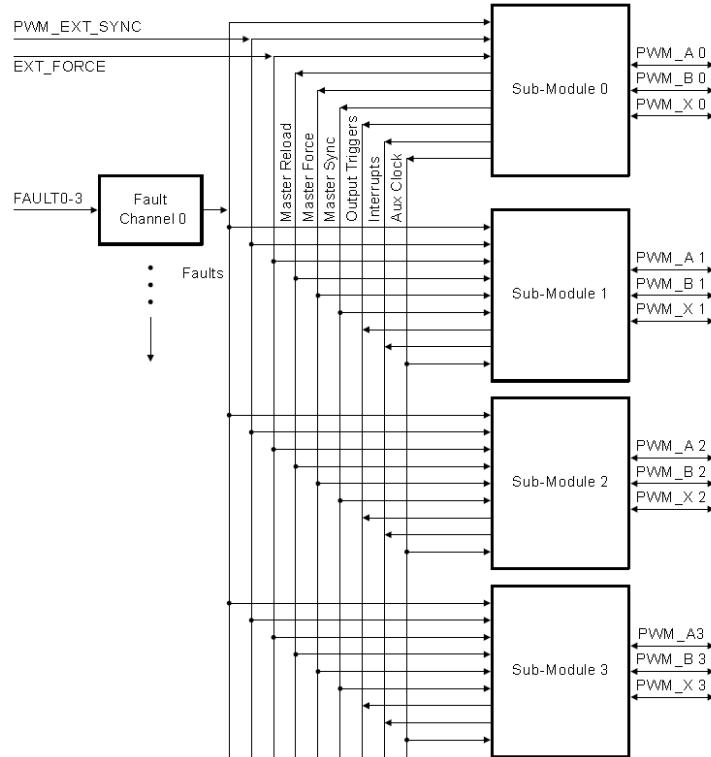


Fig 28. eFLEXPWM IP block diagram

Fig 29 shows a functional block diagram of a eFLEXPWM sub-module.

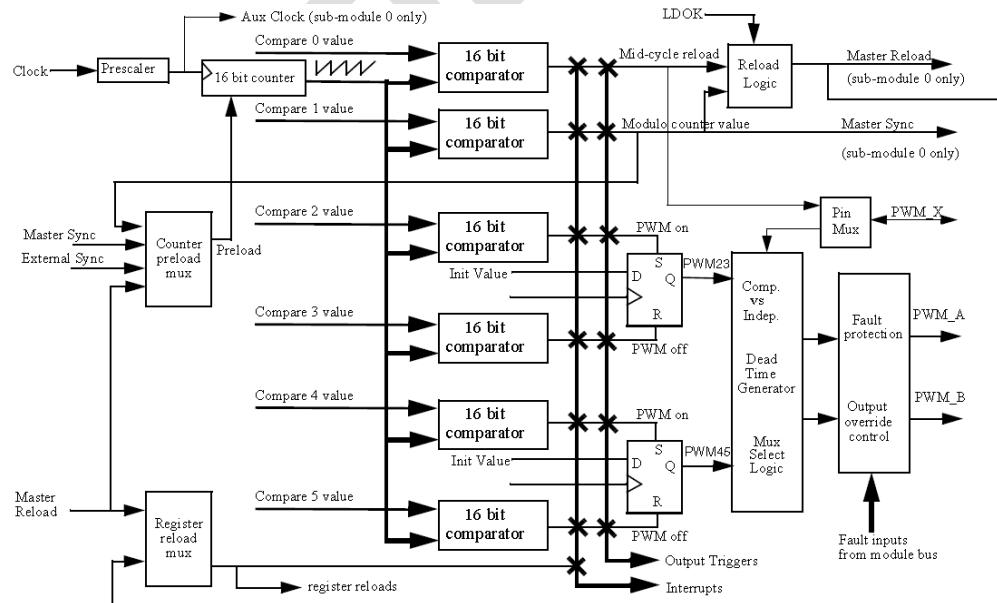


Fig 29. eFLEXPWM sub-module block diagram

The main features of eFLEXPWM are:

- 16 bits of resolution for center, edge-aligned, and asymmetrical PWMs ;
- Fractional PWM clock generation for enhanced resolution of the PWM period and duty cycle
- PWM outputs that can operate as complementary pairs or independent channels ;
- Ability to accept signed numbers for PWM generation ;
- Independent control of both edges of each PWM output ;
- Support for synchronization to external hardware or other PWM ;
- Double buffered PWM registers:
 - Integral reload rates from 1 to 16 ;
 - Half cycle reload capability ;
- Multiple output trigger events can be generated per PWM cycle via hardware ;
- Support for double switching PWM outputs ;
- Fault inputs can be assigned to control multiple PWM outputs ;
- Programmable filters for fault inputs ;
- Independently programmable PWM output polarity ;
- Independent top and bottom deadtime insertion ;
- Each complementary pair can operate with its own PWM frequency and deadtime values ;
- Individual software control for each PWM output ;
- All outputs can be programmed to change simultaneously via a FORCE_OUT event ;
- PWM_X pin can optionally output a third PWM signal from each submodule ;
- Channels not used for PWM generation can be used for buffered output compare functions;
- Channels not used for PWM generation can be used for input capture functions ;
- Enhanced dual edge capture functionality.

More detailed information on the eFlexPWM module can be found in its block guide [32].

Table 73. **IC requirements traceability: eFlexPWM requirements**

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_TMR_4-2	This processor shall include 4x instance of PWM.	Must have	Yes
iMXRT2660_TMR_4-4	Fault inputs and PWM outputs shall be multiplexed on GPIOs and connected to the output and input channel of the Trigger MUX.	Must have	Yes
iMXRT2660_TMR_4-5	Various clock sources should be used as clock options for PWM timers.	Must have	Yes 2 clock sources

6.3.7.11 Quadrature Decoder (QDC)

The i.MX RT2660 includes four enhanced quadrature decoder (QDC) modules.

The QDC module interfaces to position/speed sensors that are used in industrial motor control applications. Using 5 input signals (PHASEA, PHASEB, INDEX, TRIGGER, and HOME) from those position/speed sensors, the quadrature decoder module decodes shaft position, revolution count, and speed.

Fig 30 shows a high-level block diagram of the QDC module.

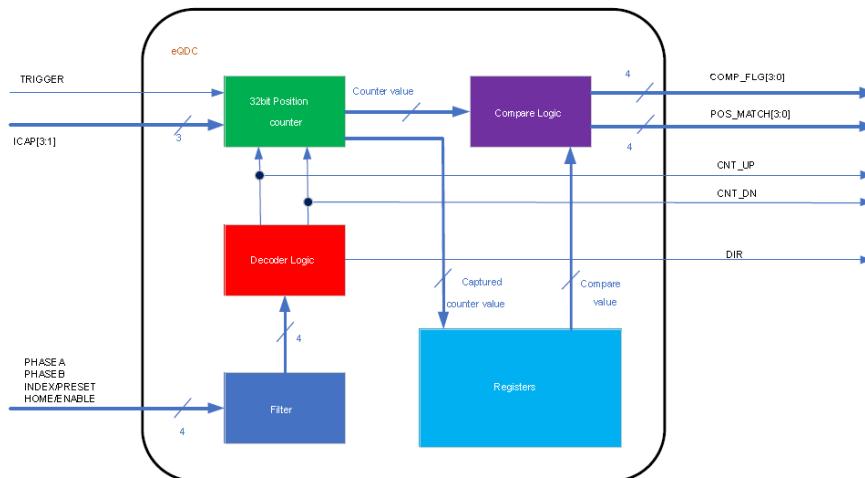


Fig 30. QDC IP block diagram

The main features of QDC are as follows:

- Includes logic to decode quadrature signals ;
- Inputs can be connected to a general purpose timer to make low speed velocity measurements ;
- Configurable digital filter for inputs ;
- Quadrature decoder filter can be bypassed ;
- 32-bit position counter capable of modulo counting ;
- Position counter can be initialized by software or external events ;
- 16-bit position difference register ;
- Compare function can indicate when shaft has reached a defined position ;
- A watchdog timer can detect a non-rotating shaft condition ;
- Preloadable 16-bit revolution counter ;
- Maximum count frequency equals the peripheral clock rate.

More detailed information on the QDC module can be found in its block guide [33].

Table 74. IC requirements traceability: Enhanced Quadrature Decoder requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_TMR_6-3	This processor shall include 4x instances of eQDC.	Must have	Yes
iMXRT2660_TMR_6-4	The 5 input signals of eQDC shall be routed through the XBAR, as shown in the diagram below.	Must have	Yes
iMXRT2660_TMR_6-5		Must have	Yes, see MAIN. XBAR0
iMXRT2660_TMR_6-6	Since this timer IP is running on the bus clock, an IPSYNC should be used on the bus interface so that when the bus change frequency, it won't affect the timer	Must have	Yes

6.3.7.12 SINC Filter (SINC)

The i.MX RT2660 contains two SINC filter modules.

The SINC module is an integrated module to convert an external ADC sigma-delta modulator bit stream to data stream. The converters are based on up to 3rd-order sinc digital decimation filters with a selectable Oversampling Rate (OSR) of up to 2048. Fig 31 shows its block diagram.

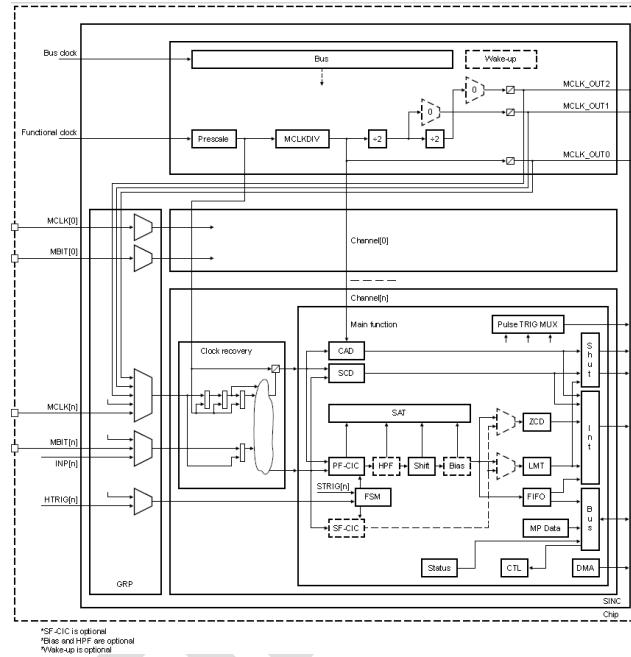


Fig 31. SINC block diagram

The main features of SINC are as follows

- Up to 4 filter channels with dedicated modulator clocks, bits, and triggers ;
- Up to 3-order programmable sinc filters with FastSinc support ;
- Up to 2048 oversampling rate ;
- Up to three modulator clock outputs ;
- One software and one hardware trigger per channel ;
- One primary filter for each channel, for 24-bit high precision ;
- Break signal outputs to turn off the external peripheral when a protection event occurs ;
- FIFO having a depth of up to 16 with watermark support for each channel ;
- Two DMA requests per channel with various event sources ;
- Interrupt support per channel ;
- Programmable high and low detection limits ;
- Support for SCD, CAD, and ZCD ;
- Programmable shift operations ;
- Programmable bias and offset operations ;
- Support for DC removal operations by using an HPF ;
- Support for a Manchester-encoded bit stream ;
- No async wakeup support ;
- Pulse-triggered output for additional control and monitoring.

More detailed information on the SINC filter module can be found in its block guide [34].

Table 75. IC requirements traceability: SINC Filter requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_AIO_6-2	The Device shall have 2x SINC Filter for converting external ADC sigma-delta modulator bitstream to data stream.	Must have	Yes

6.3.7.13 Analog-Digital Converter (ADC)

The i.MX RT2660 integrates two single-ended 16-bit Successive Approximation (SAR) ADCs. The two single ended ADC's can be configured into one pseudo differential ADC for differential measurement or increased ENOB. The input measurement range can go up to 3.3V. Different compromises in terms of speed (Conversion Rate) versus power (Icc) can be set through 12 or 16 bit resolution setting.

Fig 32 shows a high-level block diagram of the ADC module.

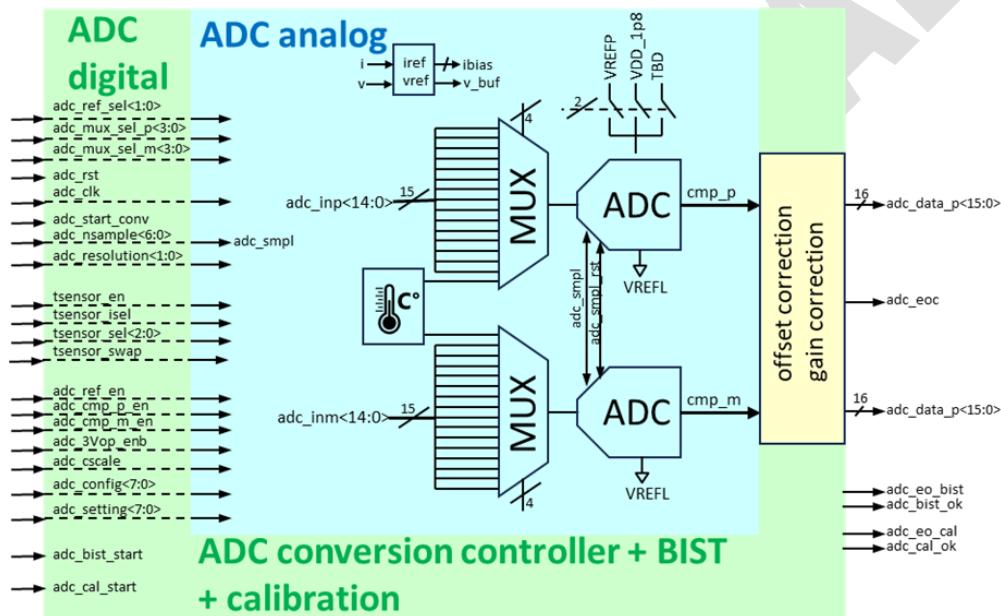


Fig 32. Analog to Digital (ADC) module high-level block diagram

Following are the features of the ADC module.

- The SAR resolution is software configurable:
 - Single-ended operation with 12/16-bit resolution (lower consumption) ;
 - 2 simultaneous single-ended conversions possible ;
 - Differential operation with 12/16-bit resolution ;
 - Up to 16-bit resolution with 14-bit accuracy ;
- Measurement of on-chip analog sources such as DAC, temperature sensor or bandgap ;
- Single- and chain-conversion modes, supporting both single or continuous conversions
 - Select external pin inputs paired for conversion as differential channel input ;
 - Up to 12 independent single-ended, or 6 independent differential input channels ;
 - Logic support for up to 30 analog channels from external pins and from internal sources ;
- Hardware- & software conversion triggers with parametrizable number of trigger inputs and programmable priority selection ;
- Includes single- or dual FIFO per channel with a depth of up to 64
 - Each FIFO has configurable watermark and overflow detection ;

- Supports user-programmable hardware averaging of conversion results, with selections in factors of 2 from 1 to at least 256 ;
- Up to 5 Msps sampling rate (12bit mode) ;
- Low-power mode functionality
 - The ADC is fully functional in low-power modes as long as the clock and the LV domain is active ;
- 2 reference-high input options
 - VDDA_1V8 ;
 - VREFH (external dedicated pin referred to as VREFP) ;
- Configurable analog input sample time ;
- Digital control
 - Supports automatic calibration and BIST: corrects linearity, gain and offset ;
 - Manages single-ended or differential operation ;
 - Up to 8 trigger sources with priority configuration. Software or hardware trigger option for each ;
 - 15 command buffers allow independent options selection and channel sequence scanning ;
 - Automatic compare for less-than, greater-than, within range, or out-of-range with "store on true" and "repeat until true" options ;
 - 2 independent result FIFOs with 64 entries each ;
 - Interrupt, DMA or polled operation ;
- Built-in temperature sensor.

Table 76 shows the targeted ADC IP key specifications.

Table 76. Targeted i.MX RT2660 ADC IP key specification items

Symbol	Parameter	Min	Typ	Max	Unit
V _{DDA_1V8}	Analog supply voltage	1.62	1.8	1.98	V
V _{DD_CORE}	Core (LV digital) regulated supply voltage	0.45	0.8	0.945	V
V _{SSAD}	Ground voltage	-0.1	0	+0.1	V
V _{REFH0}	Reference Voltage High 0		V _{REFP}		V
V _{REFH1}	Reference Voltage High 1		V _{DDA_1V8}		V
V _{REFL}	Reference Voltage Low	V _{SSAD}	V _{SSAD}	V _{SSAD}	V
Resolution	ADC resolution	12		16	bit
F _{ADCK}	ADC conversion clock frequency in 16bit mode	6		100	MHz
	ADC conversion clock frequency in 12bit mode	6		100	MHz
C _{CONV}	Conversion Cycles in 16bit mode	24		152	cycles
	Conversion Cycles in 12bit mode	19		147	cycles
R _{CONV}	Conversion Rate in 16bit mode			4	MS/s
	Conversion Rate in 12bit mode			5	MS/s
R _{CONV_int}	Max conversion rate for internal channels			0.55	MS/s
C _{ADIN}	Input capacitance in 3.6V mode (CSCALE=0)	1.9		pF	
	Input capacitance in 1.8V mode (CSCALE=1)	3.8		pF	
R _{ADIN}	Input resistance in 3.6V mode (CSCALE=0)			2.54	kΩ
	Input resistance in 1.8V mode (CSCALE=1)			1.27	kΩ
C _P	Parasitic capacitance	3		5	pF
R _{AS}	Analog Source Resistance			5	kΩ
E _{TS}	Temperature sensor error in range -40 to +105°C	±1		±2.5	°C
	Temperature sensor error in range -40 to +125°C	±1.5		±3.5	°C

More detailed information on the ADC module can be found in its user guide [35].

Table 77. IC requirements traceability: ADC requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_AIO_1-18	This device shall support 24 physical input channels, and 8 of them are shared between two ADC instances. So total 32 virtual input channels (16-ch for each ADC) are required.	Must have	Yes, 12-channels per ADC
iMXRT2660_AIO_1-3	This processor shall implement 2x 16-bit ADCs.	Must have	Yes
iMXRT2660_AIO_1-4	Each ADC has up to 16 multiplexed channels, with 6 fast channels, and 10 slow channels.	Must have	Yes 16-ch, fast channels only Open: Req. update ongoing
iMXRT2660_AIO_1-5	The ADC shall support single-ended and differential modes.	Must have	Yes
iMXRT2660_AIO_1-6	The ADC shall support 1.8V (nominal) and 3.3V (nominal) inputs. The conversion voltage range is 0 to VREFH.	Must have	Yes, up to 3.3V on pin & VREFH
iMXRT2660_AIO_1-7	The ADC can be performed in one of following conversion modes: - Single mode converts selected inputs once per trigger - Scan mode converts a selected group of analog inputs - Continuous mode converts selected input continuously - Discontinuous mode	Must have	Targeted, to be confirmed during design phase
iMXRT2660_AIO_1-8	The ADC shall support configurable resolution for 16-bit, 14-bit, and 12-bit	Must have	Yes, 14-bit dropped as agreed Open: Req. update ongoing
iMXRT2660_AIO_1-9	Conversion time is dependent on resolution. Faster conversion time by lowering resolution. Following are target conversion time for fast. - 16-bit resolution: 4Mbps - 14-bit resolution: 4.5Mbps - 12-bit resolution: 5Mbps	Must have	Targeted, to be verified during design phase (14-bit dropped) Open: Req. update ongoing
iMXRT2660_AIO_1-10	Following are target conversion time for slow channel. - 16-bit resolution: 1.2Mbps - 14-bit resolution: 1.5Mbps - 12-bit resolution: 2.5Mbps	Must have	Targeted, to be verified during design phase (14-bit dropped) Open: Req. update ongoing
iMXRT2660_AIO_1-11	The ADC shall implement an efficient low-power mode to allow very low consumption at low frequency. The ADC shall operate down to Deep Sleep mode.	Must have	Down to Sleep mode, as agreed Open: Req. update ongoing
iMXRT2660_AIO_1-12	This processor shall implement additional logic to allow - Two ADCs perform simultaneous conversion - Two ADCs perform interleaved conversion	Must have	Targeted, to be confirmed during design phase
iMXRT2660_AIO_1-13	The ADC shall support watchdog to monitor the converted voltage on some selected channels. An interrupt is generated when the converted voltage is outside the threshold.	Must have	Targeted, to be confirmed during design phase

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_AIO_1-14	In order to synchronize A/D conversion and timers, the ADCs can be triggered by FlexPWM timers, Low-Power timers, and General Purpose timer.	Must have	Yes, XBAR0/1
iMXRT2660_AIO_1-15	The ADC shall support multiple hardware trigger source, each ADC channel command can select specified trigger source	Must have	Yes, XBAR0/1
iMXRT2660_AIO_1-16	Channel FIFO: The ADC shall support ADC channel FIFO.	Must have	Yes
iMXRT2660_AIO_1-17	The ADC shall support multiple ADC results FIFO group, and each FIFO group has the DMA trigger source respectively.	Must have	Targeted, to be confirmed during design phase

Table 78. IC requirements traceability: Temperature sensor requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_AIO_5-2	This processor shall implement an temperature sensor for user's application. The Temperature sensor will generate a voltage that varies linearly with the temperature. It can measure the device ambient temperature in the supported range.	Must have	Yes
iMXRT2660_AIO_5-3	The Temperature Sensor shall support junction temperature range of -40 to +125C with a precision of +/-3%	Must have	Yes, target ±1.5°C typ, ±3.5°C max
iMXRT2660_AIO_5-4	The Temperature Sensor shall support junction temperature range of -40 to +125C with a precision of +/-1%	Should have	Yes, target ±1°C typ, ±2.5°C max
iMXRT2660_AIO_5-5	The output of the Temperature Sensor shall be connected to an ADC channel.	Must have	Yes, integrated into ADC
iMXRT2660_AIO_5-6	The Temperature Sensor shall be calibrated to obtain a good accuracy of temperature measurement. The Temperature Sensor factory calibration data are stored in OTP	Must have	Targeted, to be verified during design phase

6.3.7.14 Digital-Analog Converter (DAC)

The i.MX RT2660 includes one digital-to-analog converter (DAC) module with 12-bit resolution. The output of the DAC can be placed on an external pin or set as one of the inputs to the analog comparator, op-amps, or ADC.

The 12-bit DAC module is a low-power, high-performance voltage type DAC with on-chip programmable reference generator output. The voltage output range is from 1/4096 VREF(P) to VREF(P), and the step is 1/4096 VREF(P). Its output amplifier can drive 1.8-KΩ,100-pF load with 0.3μs code to code settling time and 0.5μs full scale settling time, suitable as waveform generator.

Fig 33 and Fig 34 show a high-level functional block diagram of the DAC analog core and -digital core, respectively.

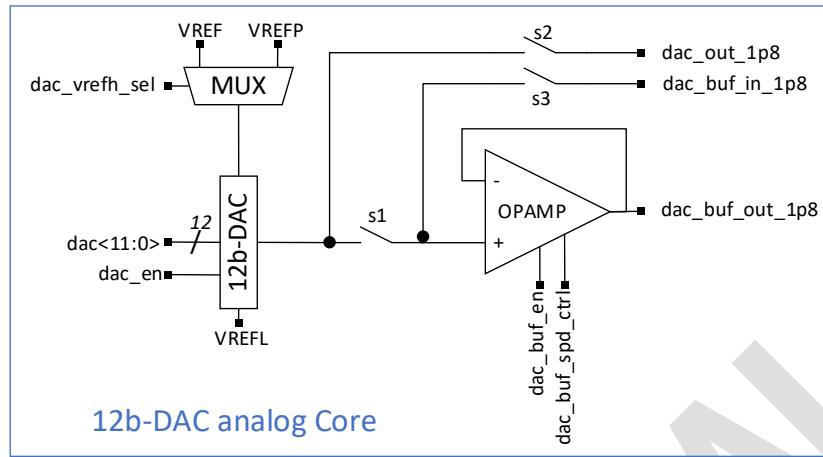


Fig 33. Digital to Analog (DAC) analog core block diagram

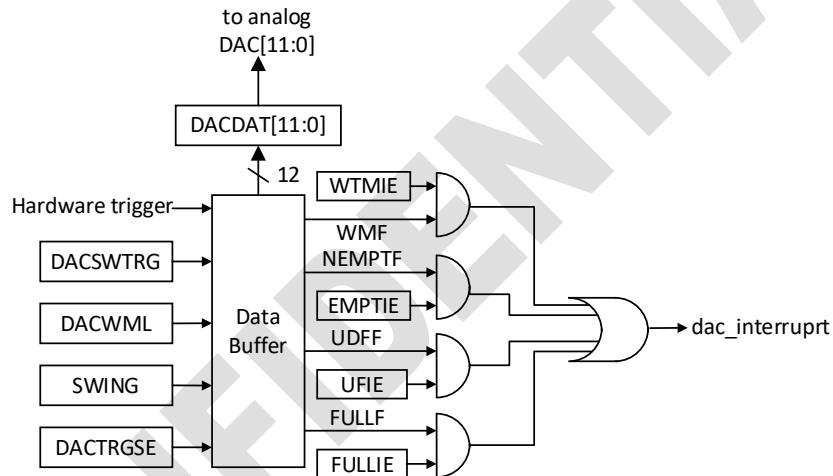


Fig 34. Digital to Analog (DAC) digital core block diagram

The main features of the DAC module include:

- No external components, support GPIO digital function and analog function swap ;
- 12-bit monotonic DAC that operates at 1.8V typical supply ;
- On-chip programmable reference generator output. The voltage output range is from 1/4096 VREF(P) to VREF(P), and the step is 1/4096 VREF(P) ;
- Supports buffered DAC operating mode and unbuffered DAC operating mode ;
- Buffered/Unbuffered DAC mode support two voltage reference source selection:
 - VREF (1.8V) applied externally via the VDDA_1V8 pin.
 - VREFP (1.8V) applied externally via the VREFP pin.
- Buffered DAC mode support normal mode and lower power mode
 - Internal current reference support $\pm 25\%$ trimming ;
- Buffered DAC mode 1Msps conversion ratio, unbuffered DAC mode output impedance 100kohm ;
- Full Rail to rail OPAMP, can drive 1.8-K Ω , 100-pF loading, 3M UG, 2.5V/ μ s Slew Rate ;
- 16 -word data buffer supported with configurable watermark and multiple operation modes, namely normal mode and swing-back mode ;

- Power down mode and scan mode and latch mode ;
- DMA support.

Table 79 shows the targeted DAC IP key electrical specifications.

Table 79. **Targeted i.MX RT2660 DAC IP key specification items**

Symbol	Parameter	Min	Typ	Max	Unit
V _{DDA_1V8}	Analog supply voltage	1.62	1.8	1.98	V
V _{DD_CORE}	Core (LV digital) regulated supply voltage	0.45	0.8	0.945	V
V _{REF}	SoC internal reference voltage		1.2		V
V _{REFP}	SoC external reference voltage		1.8		V
Resolution	DAC resolution		12		bit
R _{CONV(1)}	Conversion Rate in normal mode	1	2	200	MS/s
	Conversion Rate in low-power mode		100		kS/s
DNL (1,2)	Differential Non-Linearity	-1	±0.5	+1	LSB
INL (1,2)	Integral Non-Linearity	-2	±1	+2	LSB
FO (2)	Offset error	-0.2	±0.15	+0.2	%FSR
FO (1)	Offset error	-0.6	±0.15	+0.6	%FSR
FG (2)	Gain error	-0.2	±0.1	+0.2	%FSR
FG (1)	Gain error	-0.6	±0.15	+0.6	%FSR
C _L	Buffered DAC output loading capacitance	50	100	pF	
	Unbuffered DAC output loading capacitance		No limitation		pF
R _L	OPAMP output loading resistance	1.8	18		kΩ
TFS(1)	FS settling time in normal mode		1		μs
	FS settling time in low-power mode:				
	- Buffered		1		μs
	- Unbuffered		5		μs
TPU(1)	Power-up time		2		μs

(1) Buffered DAC mode, (2) Unbuffered DAC mode

More detailed information on the DAC module can be found in its IP User Guide [36].

Table 80. **IC requirements traceability: DAC requirements**

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_AIO_2-2	This processor shall include one DAC converter, which has one output channel.	Must have	Yes
iMXRT2660_AIO_2-3	The output of the DAC shall be multiplexed on IO pins, and set as one of the inputs to the analog comparator or ADC.	Must have	Targeted as dedicated output pad due to 1V8
iMXRT2660_AIO_2-4	Conversion voltage: The DAC shall support 1.8V (nominal)	Must have	Yes
iMXRT2660_AIO_2-5	The DAC shall support configurable resolution of 12-bit or 8-bit.	Must have	Yes, 12-bit
iMXRT2660_AIO_2-6	The DAC channel can be triggered through a timer.	Must have	Yes, via XBAR0/1

6.3.7.15 Cyclic Redundancy Check (CRC)

The Cyclic Redundancy Check (CRC) module generates 16/32 bit CRC code for error detection.

The CRC module can be configured to work as any standard CRC available today. This CRC IP provides the user with programmable polynomial, SEED and other parameters required to implement a 16-bit or 32-bit CRC standard. These parameters are detailed in further sections.

The 16/32-bit code is calculated for 8-bits/16-bits of data at a time. The data width and Transpose feature is selectable by a parameter.

Features of the CRC IP include:

- Hardware CRC generator circuit using 16-bit or 32-bit (programmable) shift register ;
- Programmable initial seed value and Polynomial ;
- Optional feature to transpose input data and CRC result via transpose register, required for certain CRC standards ;
- Final XOR of the output, some CRCs has final XOR of their CRC checksum with 0xFFFFFFFF or 0xFFFF in their protocol.

The i.MX RT2660 makes use of one CRC module that resides in the HSP_SS. It has been introduced into RT2660 to satisfy safety related requirements – please refer to Section 9.10.

More detailed information on the CRC module can be found in its IP Block Guide [37].

6.3.7.16 General Purpose Input Output (GPIO)

The General-Purpose Input-Output (GPIO) module communicates to the processor core via a zero wait-state interface for maximum pin performance. Fig 35 shows a high-level block diagram of the GPIO module.

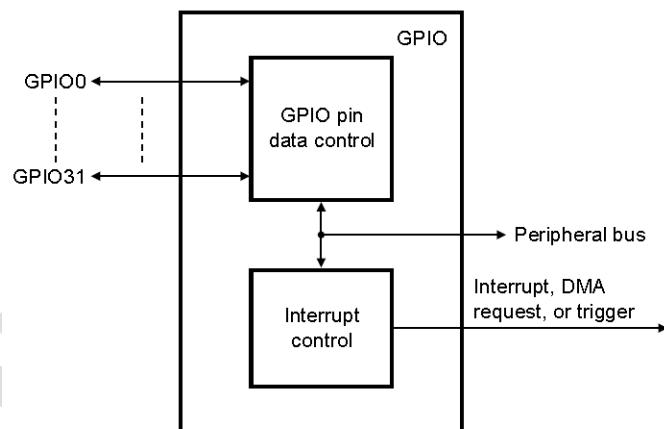


Fig 35. General Purpose IO (GPIO) block diagram

The GPIO module includes the following features:

- Port Data Input (PDIR) register displays the logic value on each pin when the pin is configured for any digital function provided the corresponding Port Control and Interrupt module for that pin are enabled ;
- Port Data Output (PDOR) register with corresponding set/clear/toggle registers controls output data of each pin when the pin is configured for the GPIO function ;
- Port Data Direction (PDDR) register controls the direction of each pin when the pin is configured for the GPIO function ;
- Port Input Disable (PIDR) register controls the disable of the input for each general-purpose pin ;
- Pin interrupts

- Interrupt flag and enable registers for each pin are functional in all digital pin muxing modes ;
- Support for interrupt, peripheral trigger, or DMA request configured per pin ;
- Support for edge sensitive (rising or falling, or both) or level sensitive (low, high) configured per pin ;
- Asynchronous wake-up in Low-Power modes ;
- GPIO module generates a total of 2 interrupts, 2 output triggers and 2 DMA requests ;
- Each pin can be used to generate a single interrupt, output trigger or DMA request ;
- Protection registers
 - Each pin is configured for Secure or Non-Secure and Privilege/Non-Privilege access ;
 - Each interrupt, trigger and DMA request domain is configured for Secure or Non-Secure and Privilege/Non-Privilege access.

The i.MX RT2660 contains multiple GPIO banks that are connected to IO pads via the IO MUX.

6.3.8MAIN_SS PBRIDGE peripherals

6.3.8.1 IO Control (IOCON)

A separate IO Control (IOCON) instance shall be defined per GPIO port and shall be implemented in each core power domain that interfaces to different pad segments. This includes the WAKE_SS and VBAT_SS domains which shall support digital pin muxing.

The IOCON shall implement the following features per pin:

- Pad setting select
 - A pad control register portion to configure specific pad settings of each pad ;
- Pad settings to be supported
 - Pull enable and select (separate strong pull enable for I3C 1k-ohm pullup option; separate pull value for tamper pins supporting up to 1M-ohm pull resistor) ;
 - Drive strength select ;
 - Slew rate select ;
 - Open drain enable (pseudo open drain; not supported for high speed pads) ;
 - Invert function (not supported for high speed pads) ;
 - Input buffer enable ;
- Digital function mux select
 - A mux control register portion to configure 1 of 12 alternate (ALT) MUX_MODE fields of each pad and to enable the forcing of an input path of the pad(s) ;
 - An input select control register portion to control the input path to a module when more than one pad drives this module input ;
 - The mux control registers may allow the forcing of pads to become input (input path enabled) regardless of the functional direction driven. This may be useful for loopback and GPIO data capture ;
- Sticky lock bit (pin configuration cannot be updated until IOCON is reset).

It is strongly recommended to implement the minimum number of registers required for simple software implementation. For example, if only ALT0 and ALT1 modes are used on Pad x then only 1-bit register is available as the MUX_MODE control field in the mux control register of Pad x ;

The IOCON may be based on the existing IOMUX Controller (IOMUXC), together with IOMUX, as used in legacy RT devices such as RT1170. It enables the SoC to share one pad to several functional blocks by multiplexing the pad's input and output signals to provide up to 12 muxing options (as referred to as ALT modes). When re-using the IOMUXC/IOMUX IP, the design team shall ensure the aforementioned IOCON features are enabled.

The following figures show possible example embodiments that are applicable in case of a IOMUXC/IOMUX based implementation.

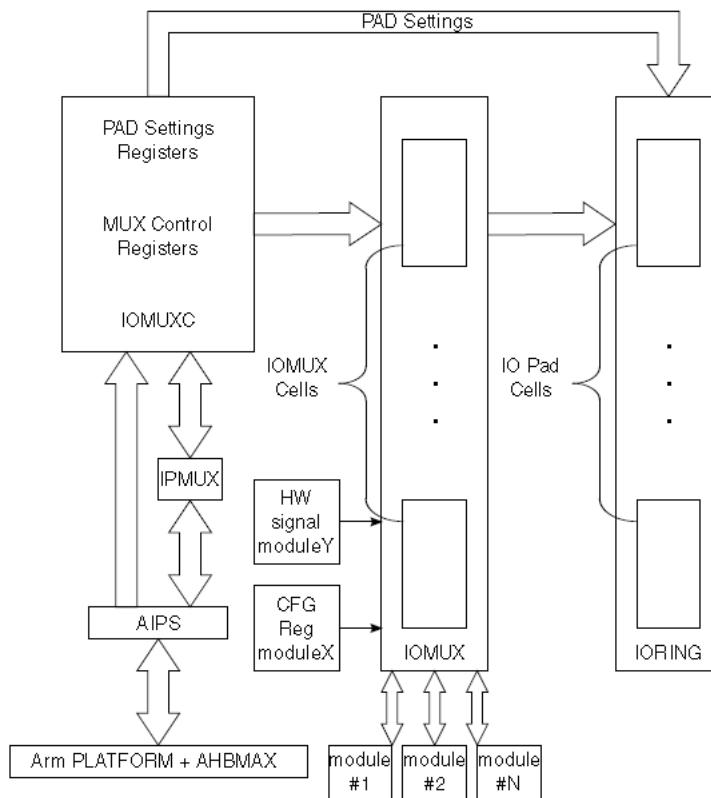


Fig 36. Example IOMUX SoC level block diagram

The IOMUX consists of a number of basic IOMUX cell units. The IOMUX cell is required whenever two or more functional modes are required for a specific pad or when one functional mode and the one test mode are required. For a dedicated IO, there may be no need for IOMUX and the signals can be connected directly from the module to the I/O.

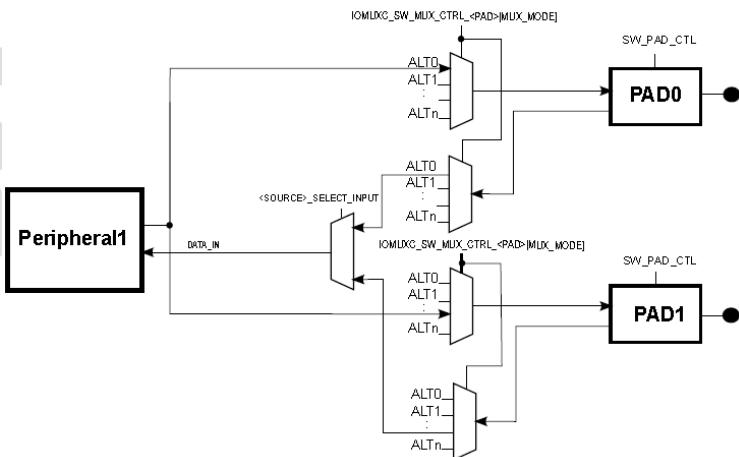


Fig 37. Example IOMUX cell functional block diagram

A detailed overview of IO multiplexing for i.MX RT2660 peripherals can be found in Section 6.10.2.

6.3.8.2 Cross-Trigger Network

The i.MX RT2660 integrates an on-chip cross trigger network. It comprises of two main components: the inter-peripheral crossbar switch (XBAR) and Event Generator (EVTG) module.

Each XBAR is an array of MUXes with shared inputs. Each mux output provides one output of the crossbar. The number of inputs and the number of MUXes/outputs is user configurable and registers are provided to select which of the shared inputs is routed to each output. The crossbar switches are used to reconfigure data paths between peripherals (peripheral output to peripheral input) as well as between peripherals and GPIO. The i.MX RT2660 MAIN_SS has two XBAR instances (XBAR[0-1] in Table 82). Refer to Subsection A.1 for more information on XBAR.

Table 81. **i.MX RT2660 XBAR instantiation**

Instance	Number of inputs (N)	Number of outputs (M)	Number of outputs with control function (P)	Select registers	Control registers
XBAR0	296	96	0	XBAR0.SEL[0-95]	n/a
XBAR1	66	186	4	XBAR1.SEL[0-185]	n/a

The EVTG module includes two And-Or-Invert (AOI) modules with some additional synchronization, filtering and feedback support. Refer to Subsection A.2 for more information.

Fig 38 shows a high-level block biagram of the on-chip cross-trigger network in i.MX RT2660.

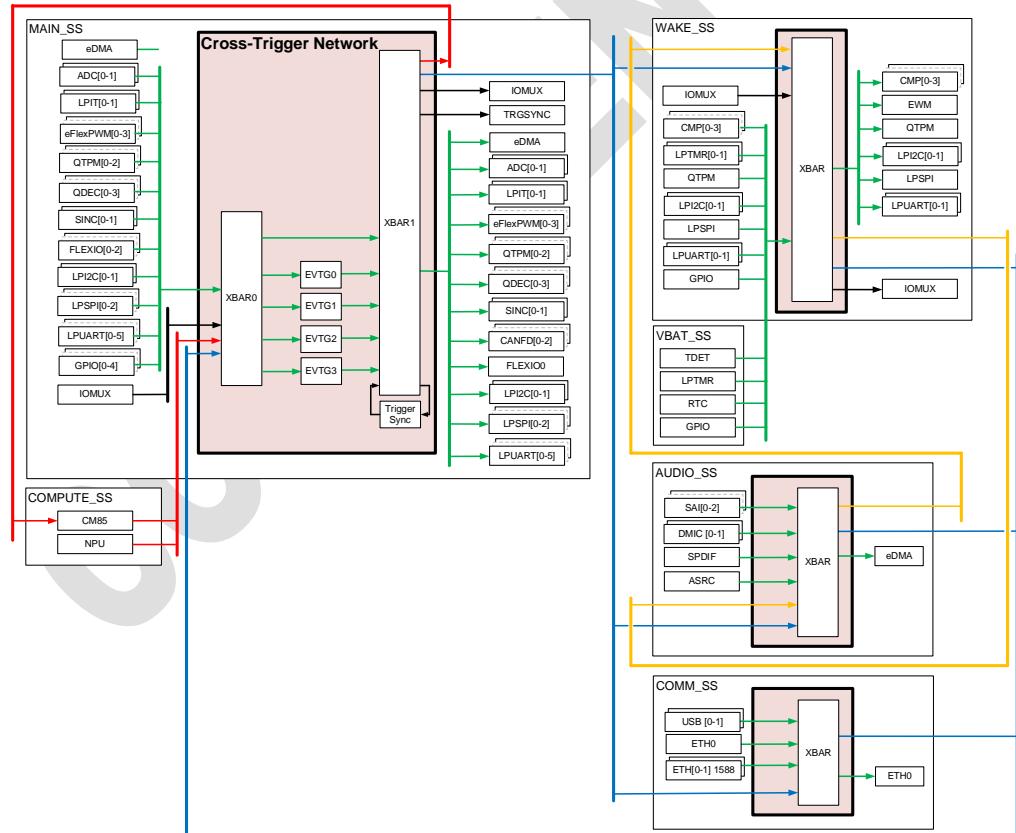


Fig 38. On-chip cross-trigger network system-level block diagram

The i.MX RT2660 detailed Cross-Trigger Network assignments in a machine-readable format can be found at the following location: [XEA1_XbarMap.xlsx](#)

The cross-trigger network description of the COMM_SS, AUDIO_SS and WAKE_SS can be found in Sections 6.4.8, 6.6.8 and 6.7.12, respectively.

Table 82. IC requirements traceability: Cross trigger requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_SCI_3-3	The Cross trigger network shall include 1x instance of XBARA.	Must have	Yes, XBAR1 Open: Req. update ongoing
iMXRT2660_SCI_3-4	The Cross trigger network shall include 2x instances of XBARB.	Must have	No, XBAR0 Open: Req. update ongoing
iMXRT2660_SCI_3-5	The Cross trigger network shall include 8x instance of AIOs.	Must have	Yes, EVTG[0-3]

A.1 Crossbar Switch (XBAR)

The XBAR implements an array of M N-input combinational muxes. All muxes share the same N inputs in the same order, but each mux has its own independent select field.

The intended application of this module is to provide a flexible crossbar switch function that allows any input (typically from external GPIO or internal module outputs) to be connected to any output (typically to external GPIO or internal module inputs) under user control. This is used to allow user configuration of data paths between internal modules and between internal modules and GPIO.

A subset of the muxes (P in total) can be configured to support edge detection and either interrupt or DMA request generation based on detected signal edges on the mux output. This allows signal transitions on the signals feeding the crossbar to trigger interrupts or initiate data transfers via DMA into or out of other system modules.

Fig 39 shows a functional block diagram of the XBAR.

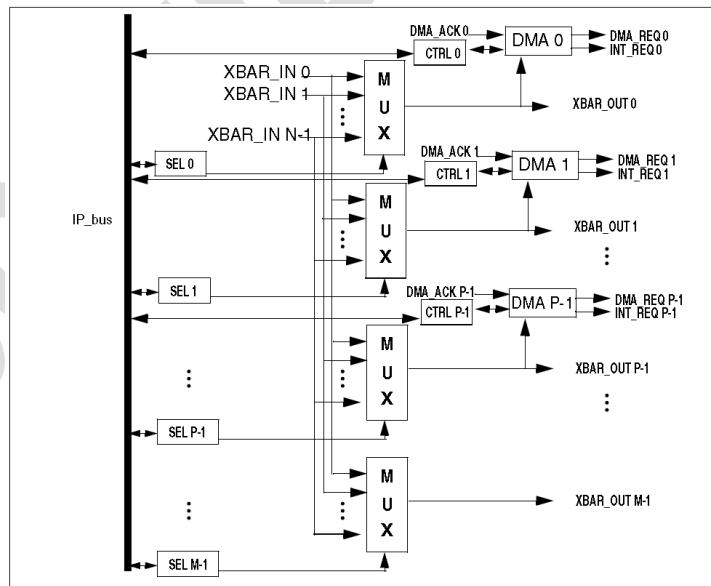


Fig 39. XBAR functional block diagram

The XBAR offers the following main features:

- M identical N-input muxes with individual select fields ;
- Edge detection with associated interrupt or DMA request generation for a subset of mux outputs (XBAR_OUT[0]~ XBAR_OUT[P-1]) ;
- Memory mapped registers with IPBus interface for select and control fields.

A.2 Event Generator (EVTG)

The i.MX RT2660 makes use of the four Event Generator (EVTG) modules. Each EVTG module includes two parts:

- Two AND/OR/INVERT (known as the AOI) modules ;
- One configurable flip-flop.

The EVTG module has been implemented on DSC and MCX N devices. It supports the generation of a configurable number of Event signals. The two AOI combinational expressions share the four associated EVTG inputs: An, Bn, Cn, and Dn. One can configure the flip-flop to make the two expressions act as the Reset port, Set port or D port, CLK port or go through to EVTG output with the flip-flop bypassed.

The EVTG module is a slave peripheral module-connecting event input indicators from various chip modules and generates event output signals that is routed to inter-peripheral crossbar switch or other peripherals. One can access its programming model through the standard IPS (sky blue) slave interface. EVTG is configurable in the integrated AOI functionality and flip-flop variety.

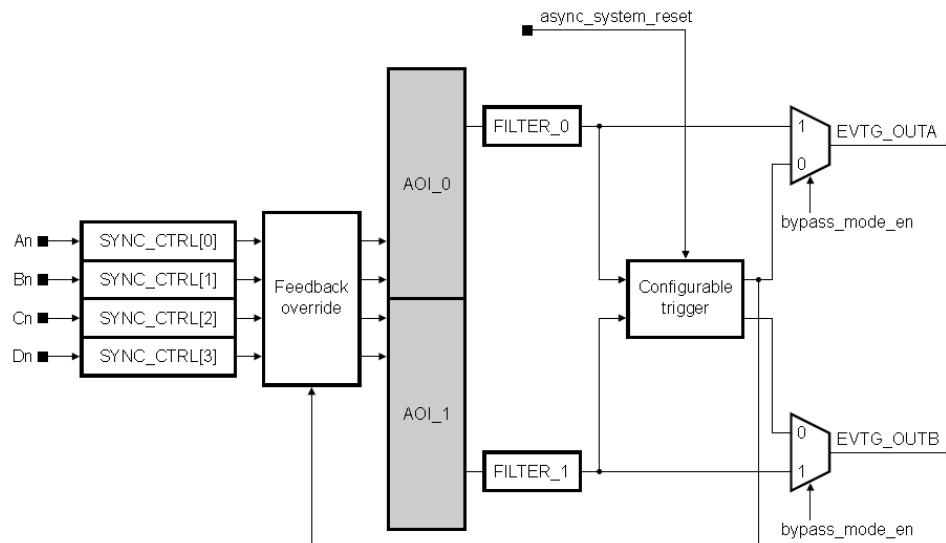


Fig 40. EVTG functional block diagram

The EVTG module offers the following main features:

- Includes a highly programmable module for creating combinational boolean events
 - Each EVTG consists of four inputs and two outputs ;
 - Each AOI evaluates a combinational boolean expression as the sum of four products, where each product term includes all four selected input sources available as true or complement values ;
 - Each EVTG consists of two groups of AOI to generate two combinational expressions ;
 - The two outputs can operate as hardware trigger signals or for other purposes ;
- Configures one flexible FF as RS, D-FF, T-FF, JK-FF, and Latch ;
- Includes a programmable filter to remove AOI output glitch ;
- Specifies that all logics are synchronous in bus clk domain ;

- Includes a memory-mapped chip connected to the slave peripheral (IPS) bus. Programming model is organized per channel for a simplified software.

6.3.8.3 PVT monitor

The i.MX RT2660 shall include a PVT monitor to measure the actual performance of the SoC for the given die sample under its operating condition.

This PVT monitor can be re-used from legacy i.MX RT or MCX devices.

6.3.8.4 Frequency Measure Unit (FREQME)

The main purpose of the FREQME unit to measure the frequency of the IP functional clocks and - bus clocks. Refer to Section 6.2.7 for a brief description about the FREQME unit

The MAIN_SS includes two FREQME units, one to monitor the CGU clock outputs (SYSCON.FREQME) and another one to monitor the MODCON_MAIN clock outputs (MAIN.FREQME). Please refer to the MAIN_SS HW.AS for detailed information about the allocation of the measurement channels for each FREQME unit [4].

6.3.8.5 On-Chip OTP

The i.MX RT2660 makes use of the Synopsys “DWC NVM OTP XBC GF 22nm FDX 1.8V” solution in combination with the Synopsys OTP controller IP. The Synopsys OTP memory makes use of Synopsys Hiper Fuse (SHFG2) High Performance macrocells; the i.MX RT2660 makes use of the OTP version qualified for Ag1 applications (product code: F544).

Fig 41 shows a high-level block diagram of the OTP memory. The i.MX RT2660 makes use of a version that includes the integrated power supply (IPS) module to allow for OTP programming in the field for customer usage in use-case applications. The OTP memory requires two power supply voltages: a low supply voltage of $0.8V \pm 10\%$ (VDD) and high supply voltage of $1.8V \pm 10\%$ (VCC); these supply voltages are provided by the i.MX RT2660 on-chip PMU. Refer to Section 8.2.

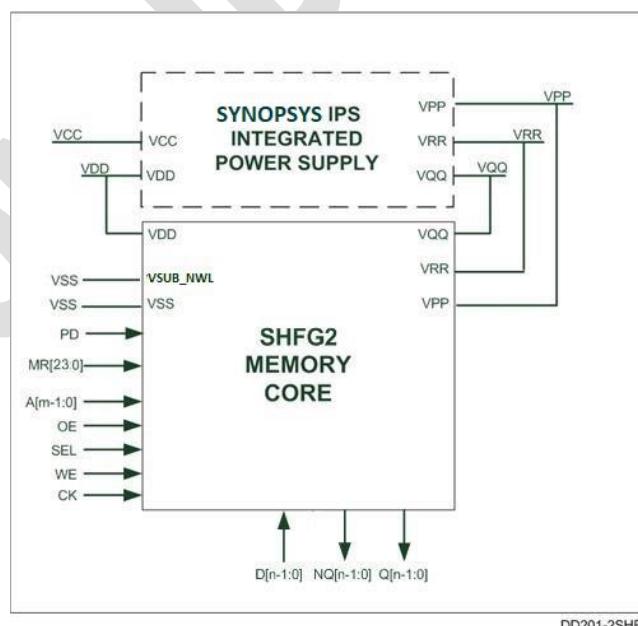


Fig 41. Synopsys OTP memory block diagram

The following OTP configuration applies for the i.MX RT2660.

Table 83. i.MX RT2660 OTP memory configuration

Instance	Module name	Configuration
OTP memory core	shfg2_gf22fdx18_1kx42_cm16s1	42 kbit: 1k x 42
IPS Integrated Power Supply	ips_gf22fdx18_l1bp1r	Read reg & Prog.pump

Next to the Synopsys OTP memory, the i.MX RT2660 utilizes the Synopsys OTP controller.

6.4 MAIN-COMPUTE Domain: Communication Sub-System (COMM_SS)

The COMM_SS of i.MX RT2660 is a medium-performance section that includes general connectivity interfaces that can operate as bus master. It runs at an operating frequency of up to 200 MHz. Its architectural block diagram is shown in Fig 42. The COMM_SS of i.MX RT2660 is a subset of the XEA-1 platform version.

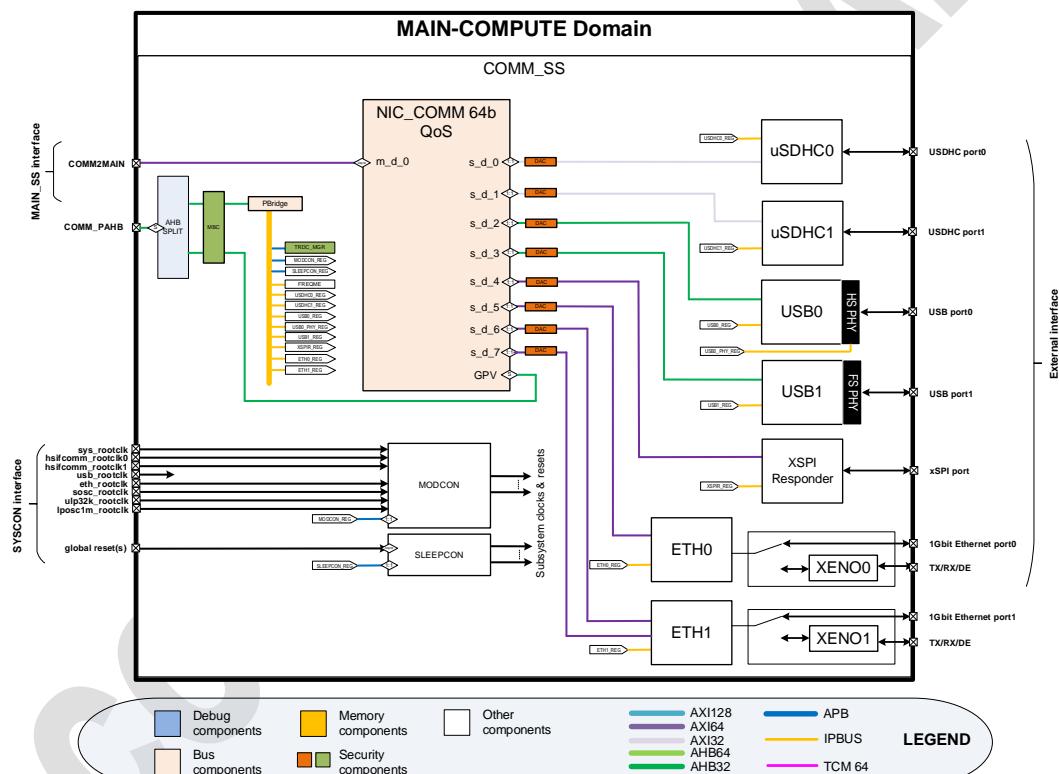


Fig 42. Architectural block diagram of i.MX RT2660's COMM_SS

For the origin of the main building blocks, their maturity level and their legacy i.MX sourcing product, please refer to the IP Re-Use Sheet that is listed in Chapter 15. The COMM_SS building blocks has been described in more detail in the following sub-sections.

For more detailed information, please refer to the COMM_SS HW.AS document [7]

This document includes the RT2660 specific IP configurations.

6.4.1 Ultra Secured Digital Host Controller (uSDHC)

The i.MX RT2660 has two Ultra Secured Digital Host Controller (uSDHC) modules for SD/SDIO/eMMC interface. The module acts as a bridge, passing host bus transactions to the SD/SDIO/MMC cards by sending commands and performing data accesses to/from the cards. It handles the SD/SDIO/MMC protocols at the transmission level.

Table 84 shows the uSDHC module configuration for the i.MX RT2660 SoC.

Table 84. **i.MX RT2660 uSDHC module configuration [to be completed]**

	uSDHC0	uSDHC1
Targeted external memory device	eMMC/SD	SDIO/SD
Host interface bit-width	MMC 1-, 4- and 8-bit SD/SDIO 1- and 4-bit	- 1- and 4-bit
Host interface frequencies	MMC {200,166,133,100,66} MHz SD/SDIO {200,50,25} MHz	- {200,50,25} MHz
Identification	up to 400kHz	up to 400kHz
Data rate mode	Single Data Rate Yes Double Data Rate Yes	Yes Yes
Data buffer size	1024 bytes	1024 bytes
IP clock frequency support	{400,332,266,200,132,100,50} MHz	{400,100,50} MHz

The uSDHC modules are re-used from i.MX RT1170. Fig 43 shows their functional block diagram.

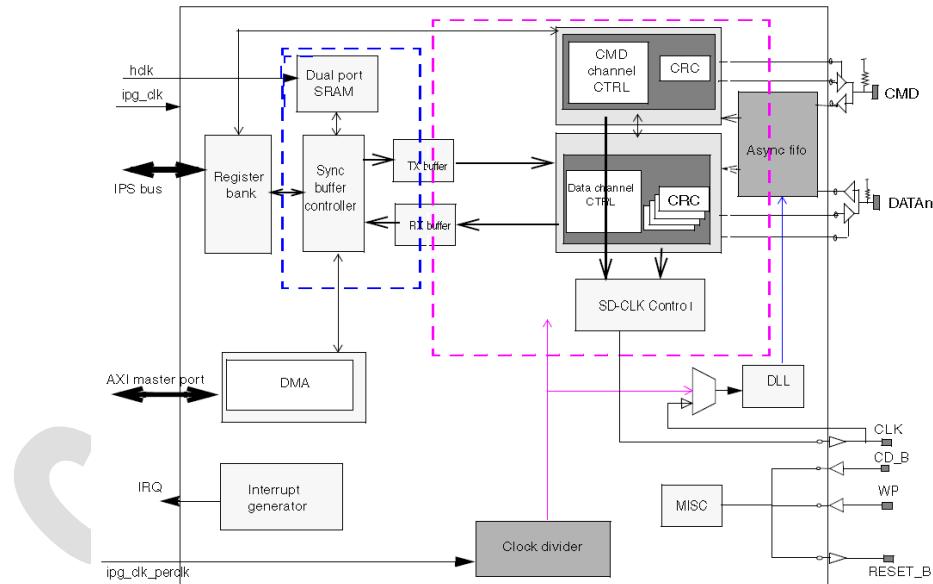


Fig 43. uSDHC IP functional block diagram

The key features of the uSDHC IP include:

- Conforms to the SD Host Controller Standard Specification version 2.0/3.0 ;
- Compatible with the MMC System Specification version 4.2/4.3/4.4/4.41/4.5/5.0/5.1 ;
- Compatible with the SD Memory Card Specification version 3.0 and supports the Extended Capacity SD Memory Card ;
- Compatible with the SDIO Card Specification version 2.0/3.0 ;

- Designed to work with SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC, MMC plus, and MMC RS cards ;
- Card bus clock frequency up to 208 MHz ;
- Supports 1-bit/4-bit SD and SDIO modes, and 1-bit/4-bit/8-bit MMC modes
 - Up to 832 Mbps of data transfer for SDIO cards using 4 parallel data lines in SDR mode
 - Up to 400 Mbps of data transfer for SDIO card using 4 parallel data lines in DDR mode
 - Up to 832 Mbps of data transfer for SDXC cards using 4 parallel data lines in SDR mode
 - Up to 400 Mbps of data transfer for SDXC card using 4 parallel data lines in DDR mode
 - Up to 1600 Mbps of data transfer for MMC cards using 8 parallel data lines in SDR mode
 - Up to 3200 Mbps of data transfer for MMC cards using 8 parallel data lines in DDR mode
- Supports single block/multi-block read and write ;
- Supports block sizes of 1 ~ 4096 bytes ;
- Supports the write protection switch for write operations ;
- Supports both synchronous and asynchronous abort ;
- Supports pause during the data transfer at block gap ;
- Supports SDIO Read Wait and Suspend Resume operations ;
- Supports Auto CMD12 for multi-block transfer ;
- Host can initiate non-data transfer command while data transfer is in progress ;
- Allows cards to interrupt the host in 1-bit and 4-bit SDIO modes; also supports interrupt period ;
- Embodies a fully configurable 128x32-bit FIFO for read/write data ;
- Supports internal DMA capabilities ;
- Support voltage selection by configuring vendor-specific register bit ;
- Supports Advanced DMA to perform linked memory access.

More detailed information of the uSDHC IP module can be found in its block guide [38].

Table 85. **IC requirements traceability: USDHC requirements**

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_MEM_13-1	uSDHC Controller	Heading	-
iMXRT2660_MEM_13-2	The uSDHC Controller provides the host interface to external devices, including eMMC, removable SD card, and SDIO device, like WiFi chip.	Must have	Yes
iMXRT2660_MEM_13-3	This processor shall implement 2 uSDHC controller: - uSDHC0 port is for the host interface to eMMC or SD card. - uSDHC1 port is the host interface to SDIO device or SD card.	Must have	Yes, uSDHC0/1
iMXRT2660_MEM_13-4	The uSDHC controllers shall be compliant to: - SD Physical Specification v3.0 - SD Host Specification v3.0	Must have	Yes
iMXRT2660_MEM_13-5	The uSDHC controllers shall fully support the ADMA as specified in the SD Host Specification v3.0.	Must have	Yes
iMXRT2660_MEM_14-1	eMMC/SD Host Interface	Heading	-
iMXRT2660_MEM_14-2	This uSDHC port shall be compliant to JEDEC eMMC v5.1.	Must have	Yes
iMXRT2660_MEM_14-3	This uSDHC port shall support following bus width: - 4-bit IO for SD host interface - 8-bit IO for eMMC host interface	Must have	Yes, see Table 84
iMXRT2660_MEM_14-5	This uSDHC port should be multiplexed out at two locations: one for host interface to eMMC and the other for SD card.	Must have	Yes
iMXRT2660_MEM_14-6	This uSDHC port shall support all eMMC speed modes, including HS400 and HS200.	Must have	Yes
iMXRT2660_MEM_14-7	This uSDHC port shall support eMMC HS400 mode up to 200MHz in DDR mode.	Must have	Yes, see Table 84

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_MEM_14-8	This uSDHC port shall support eMMC HS200 mode up to 200MHz in SDR mode.	Must have	Yes, see Table 84
iMXRT2660_MEM_14-9	This uSDHC port shall support all SD speed modes, including SDR104 mode up to 200MHz.	Must have	Yes
iMXRT2660_MEM_14-10	This uSDHC port shall support Enhanced Data Strobe feature specified in eMMC v5.1. Enhanced Data Strobe feature enable data integrity on CMD response, which is important industrial and automotive applications where data integrity is important.	Must have	Yes
iMXRT2660_MEM_15-1	eMMC performance	Heading	-
iMXRT2660_MEM_15-2	The eMMC sequential write scenario should achieve a performance of, at minimum, 150 MBps	Must have	Yes
iMXRT2660_MEM_15-3	The eMMC sequential read scenario should achieve a performance of, at minimum, 310 MBps	Must have	Yes
iMXRT2660_MEM_16-1	HS400 tunning time improvement	Heading	-
iMXRT2660_MEM_16-2	The tunning time for HS400 mode is very long. It's imperative to explore new mechanism to improve the tunning time in this mode.	Should have	Not covered at this stage
iMXRT2660_HIO_3-1	SDIO Host Interface	Heading	-
iMXRT2660_HIO_3-2	This processor shall implement one SDIO host controller, which can provide the host interface to external SDIO device such as WiFi.	Must have	Yes
iMXRT2660_HIO_3-3	The SDIO host controller can also provide the host interface to a removal SD card if it is not used for SDIO connectivity.	Must have	Yes
iMXRT2660_HIO_3-5	The SDIO host controller shall be compliant to the following standards: 1) SD Card Physical Specification v3.0 2) SDIO Specification v3.0 3) SD Host Specification v3.0 4) SD Low Voltage Supplement Specification	Must have	Yes LVS is not supported
iMXRT2660_HIO_3-7	The SDIO host controller shall fully support ADMA2 capabilites as defined in the SD host specification to perform linked memory access	Must have	Yes
iMXRT2660_HIO_3-8	The SDIO host controller shall support SDIO Read Wait operation	Must have	Yes
iMXRT2660_HIO_3-9	The SDIO host controller shall support SDIO Suspend Resume operation	Must have	Yes
iMXRT2660_HIO_3-10	The SDIO host controller shall support Auto CMD12 for multi-block transfer	Must have	Yes
iMXRT2660_HIO_3-11	The SDIO host controller shall support initiation of non-data transfer command while data transfer is in progress.	Must have	Yes

6.4.2 Ethernet (ETH)

The i.MX RT2660 contains two Ethernet 1Gb IP modules. The first module concerns a 10/100/1000 Ethernet module with Time-Sensitive Networking (TSN) feature; the second module concerns a 10/100/1000 Ethernet modules with Audio Video Bridging (AVB) feature. The following subsections will describe these IP in more details.

6.4.2.1 ETH 10/100/1000 TSN with 1588 Controller

The i.MX RT2660 includes one 10/100/1000 Ethernet modules with TSN feature. It complies with the following standards:

- IEEE 1588-2008 for precision networked clock synchronization ;
- IEEE 802.1AS-2011 and 802.1-Qav-2009 for Audio Video (AV) traffic ;

- IEEE 802.1AS-Rev/D4.0, Timing and Synchronization for Time-Sensitive Applications in Bridged Local Area Networks ;
- IEEE 802.3az-2010 for Energy Efficient Ethernet (EEE) ;
- IEEE 802.1Qbv-2015, 802.1Qbu-2016, and 802.1AS-Rev D5.0 for Time-Sensitive Networking (TSN) traffic ;
- IEEE 802.1Qaz-2011 and 802.1Qbb-2011 for Data Center Bridging (DCB) traffic ;
- RGMII/RTBI specification version 2.6 from HP/Marvell ;
- RMII specification version 1.2 from RMII consortium.

The Ethernet module is re-used from i.MX RT1170. Fig 44 shows the high-level functional block diagram of the Ethernet IP.

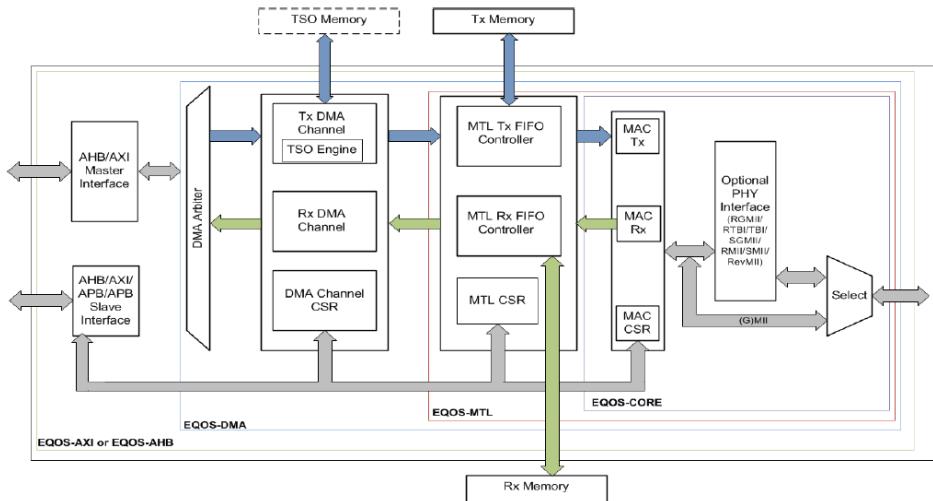


Fig 44. Functional block diagram of Ethernet 1Gb IP with TSN

The controller supports the following MAC Tx and Rx main features:

- Separate transmission, reception, and control interfaces to the application
- Configurable big-endian and little-endian mode for Transmit and Receive paths
- 10, 100, and 1000 Mbps data transfer rates with the following PHY interfaces:
 - IEEE 802.3-compliant GMII/MII (default) interface to communicate with an external Gigabit or Fast Ethernet PHY
 - IEEE 802.3z-compliant TBI interface (optional), with auto-negotiation to communicate with an external PHY
 - RTBI interface (optional) to communicate with an external gigabit PHY
 - RGMII interface (optional) to communicate with an external gigabit PHY
 - SGMII interface (optional) with auto-negotiation to communicate with an external Gigabit PHY
 - SMII interface (optional) to communicate with an external Fast Ethernet PHY
 - RMII interface (optional) to communicate with an external Fast Ethernet PHY
 - RevMII interface (optional) to directly communicate with a remote MAC
- Half-duplex operation:
 - CSMA/CD Protocol support
 - Flow control using backpressure support (based on implementation-specific white papers and UNH Ethernet Clause 4 MAC Test Suite - Annex D)
 - Packet bursting and packet extension in 1000 Mbps half-duplex operation
- Standard IEEE 802.3az-2010 for Energy Efficient Ethernet in (G)MII and Reduced Gigabit Media Independent Interface (RGMII) PHYs.
- 32-bit, 64-bit, or 128-bit data transfer interface on the application side
- Full-duplex flow control operations (IEEE 802.3x Pause packets and Priority flow control)

- Optional network statistics with RMON or MIB Counters (RFC2819/RFC2665)
- Optional module to support Ethernet packet timestamping as described in IEEE 1588-2002 and IEEE 1588-2008 (64-bit timestamps given in the Tx or Rx status of PTP packet). Both one-step and two-step timestamping is supported in TX direction.
- Flexibility to control the Pulse-Per-Second (PPS) output signal (ptp_pps_o)
- Media clock generation and recovery
- Optional MDIO (Clause 22 and Clause 45) master interface for PHY device configuration and management
- Option to select up to 16 general purpose inputs and outputs The general purpose inputs are programmable to generate interrupts on rising or falling edges.

The controller supports the following main features for MAC Tx:

- Preamble and start of packet data (SFD) insertion
- Separate 32-bit status for each packet transmitted from the application
- Automatic CRC and pad generation controllable on a per-packet basis
- Programmable packet length to support Standard or Jumbo Ethernet packets with up to 16 KB of size
- Programmable Inter Packet Gap (40–96 bit times in steps of 8)
- IEEE 802.3x Flow Control automatic transmission of zero-quanta Pause packet when flow control input transitions from assertion to de-assertion (in full-duplex mode)
- Source Address field insertion or replacement, and VLAN insertion, replacement, and deletion in transmitted packets with per-packet or static-global control
- Insertion, replacement, or deletion of up to two VLAN tags
- Option to transmit packets with reduced preamble size in full-duplex mode
- Insert, replace, or delete queue/channel-based VLAN tags
- Frame Preemption for MAC Tx

The controller supports the following main features for MAC Rx:

- Automatic Pad and CRC Stripping options
- Option to disable Automatic CRC checking
- Preamble and SFD deletion
- Separate 112-bit or 128-bit status
- Programmable watchdog timeout limit
- Flexible address filtering modes:
 - Up to 31 additional 48-bit perfect (DA) address filters with masks for each byte
 - Up to 96 additional 48-bit perfect (DA) address filters that can be selected in blocks of 32 and 64 registers
 - Up to 31 48-bit SA address comparison check with masks for each byte
 - 32 bit, 64 bit, 128 bit, or 256 bit Hash filter (optional) for multicast and unicast (DA) addresses
 - Option to pass all multi-cast addressed packets
 - Promiscuous mode to pass all packets without any filtering for network monitoring
 - Pass all incoming packets (as per filter) with a status report
- Additional packet filtering:
 - VLAN tag-based: Perfect match and Hash-based (optional) filtering. Filtering based on either outer or inner VLAN tag is possible.
 - Layer 3 and Layer 4-based: TCP or UDP over IPv4 or IPv6
 - Extended VLAN tag based filtering 4, 8, 16, or 32 filter selection
- IEEE 802.1Q VLAN tag detection and option to delete the VLAN tags in received packets
- Optional module to detect remote wake-up packets and AMD magic packets
- Optional forwarding of received Pause packets to the application (in full-duplex mode)
- Optional Receive module for Layer 3/Layer 4 checksum offload for received packets
- Optional stripping of up to two VLAN Tags and providing the tags in the status.
- Frame Preemption for MAC Rx

The controller supports the following Transaction Layer (MTL) features:

MTL Tx and Rx Common Features

- 32-bit, 64-bit, or 128-bit Transaction Layer block (bridges the application and the MAC)
- Data transfers executed using simple FIFO protocol
- Synchronization for all clocks in the design (Transmit, Receive, and Application clocks)
- Optimization for packet-oriented transfers with packets delimiters
- Option to have dual-port RAM based asynchronous FIFO controllers or Single-port RAM based synchronous FIFO controllers
- RAM memory instantiation outside the top-level module to facilitate memory testing or instantiation
- Programmable burst length, up to half the size of the MTL Rx queue or Tx queue size, to support burst data transfer in the EQOS-MTL configuration
- Programmable threshold capability for each queue (default of 64 bytes)
- Optional Debug and slave mode operation on Queue 0 (default queue)

MTL Tx Features

- Following FIFO sizes on transmission: 256 byte, 512 byte, 1 KB, 2 KB, 4 KB, 8 KB, 16 KB, 32 KB, 64 KB, or 128 KB
- Multiple queues (up to 8) on the Transmit path with a common memory for all Tx queues
- Store-and-Forward mechanism or threshold mode (cut-through) for transmission to the MAC
- Programmable queue size in configurations with multiple queues. Each queue size can be programmed in terms of 256 bytes
- Automatic retransmission of collision packets in half-duplex mode
- Discard packets on late collision, excessive collisions, excessive deferral, and under-run conditions with appropriate status
- Disabling of Data Memory RAM chip-select when inactive to reduce power consumption
- Optional module to calculate and insert IPv4 header checksum and TCP, UDP, or ICMP checksum
- Programmable interrupt options for different operational conditions
- Statistics by generating pulses for packets dropped (because of underflow) in the Tx FIFO
- Optional statistics related to bandwidth consumption by each queue of up to 16 blocks over a 125 μ s period
- Optional packet-level control for
 - VLAN tag insertion or replacement
 - Ethernet source address insertion
 - Layer3/Layer4 Checksum insertion control
 - One-step timestamp
 - Timestamp control
 - CRC and pad control
- Following scheduling algorithms in configurations with multiple queues:
 - Weighted Round Robin (WRR)
 - (When Data Center Bridging is enabled) Deficit Weighted Round Robin (DWRR)
 - (When Data Center Bridging is enabled) Weighted Fair Queuing (WFQ)
 - Strict Priority (SP)
 - (When Audio-Video Bridging is enabled) Credit-based Shaper (CBS)
 - (When TSN is enabled), Enhancement to Scheduled Traffic (EST)
 - (When TSN is enabled), Time Based Scheduling (TBS)
- Option to support dropping of Tx Status to improve the Transmit throughput

MTL Rx Features

- Following Rx queue sizes in the Receive path: 256 byte, 512 byte, 1 KB, 2 KB, 4 KB, 8 KB, 16 KB, 32 KB, 64 KB, 128 KB, or 256 KB
- Multiple queues (up to 8) on the Receive path with a common memory for all Rx queues
- Insertion of Rx Status vectors into the Rx queue after the EOP transfer (in Threshold mode) and before SOP (in Store-and-Forward mode) in EQOS-MTL configuration

- Programmable Rx queue threshold (default fixed at 64 bytes) in Threshold (or cut-through) mode
- Option to filter all error packets on reception and not forward them to the application in the store-and-forward mode
- Option to forward the undersized good packets
- Statistics by generating pulses for packets dropped (because of overflow) in the Rx FIFO
- Automatic generation of Pause packet control or backpressure signal to the MAC based on the Rx Queue fill level
- Arbitration among queues when multiple queues are present. The following arbitration schemes are supported:
 - Weighted Round Robin (WRR)
 - Weighted Strict priority (WSP)
 - Strict Priority (SP)
- Option to replicate received multicast packets for transfer by multiple Rx DMA channels
- Option to have a programmable lookup table based flexible Parser for filtering and steering the Rx packets

6.4.2.2 ETH 10/100/1000 AVB with 1588 Controller

The i.MX RT2660 includes one 10/100/1000 Ethernet modules with AVB feature. It complies the IEEE802.3-2002 standard. The MAC layer provides compatibility with half- or full-duplex 10/100 Mbit/s Ethernet LANs and full-duplex gigabit Ethernet LANs.

Fig 45 shows the high-level functional block diagram of the Ethernet IP with AVB feature.

The Ethernet MAC provides compatibility with half- or full-duplex 10/100-Mbit/s and full-duplex gigabit Ethernet LANs. The MAC operation is fully programmable and can be used in Network Interface Card (NIC), bridging, or switching applications. The module implements the remote network monitoring (RMON) counters according to IETF RFC 2819.

The Ethernet MAC implements a hardware acceleration block to optimize the performance of network controllers providing TCP/IP, UDP, and ICMP protocol services. The acceleration block implements performance-critical functions in hardware. It also implements programmable embedded FIFOs that can provide buffering on the receive path for lossless flow control. Advanced power management features are available with magic packet detection and programmable power-down modes.

A unified DMA (uDMA), internal to the Ethernet module, optimizes data transfer between the Ethernet module and the SoC, and supports an enhanced buffer descriptor programming model to support IEEE 1588 functionality.

The programmable Ethernet module with IEEE 1588 integrates a standard IEEE 802.3 Ethernet MAC with a time-stamping module. The IEEE 1588 standard provides accurate clock synchronization for distributed control nodes for industrial automation applications.

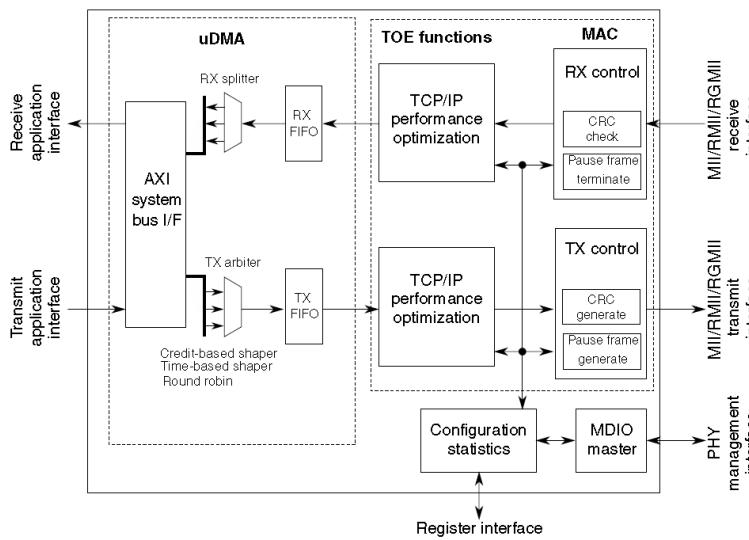


Fig 45. Ethernet IP functional block diagram

This IP is reused from i.MXRT1170 with **DFT related fixes: TKT0563453, TKT0563454, and TKT0563455 by adding a mux to introduce an explicit clock path in scan test mode.**

The Ethernet MAC offers the following main features:

- Implements the full 802.3 specification with preamble/SFD generation, frame padding generation, CRC generation and checking ;
- Supports zero-length preamble ;
- Dynamically configurable to support 10/100-Mbit/s and gigabit operation ;
- Supports 10/100 Mbit/s full-duplex and configurable half-duplex operation ;
- Supports gigabit full-duplex operation ;
- Compliant with the AMD magic packet detection with interrupt for node remote power management ;
- Seamless interface to commercial Ethernet PHY devices via one of the following:
 - a 4-bit Media Independent Interface (MII) operating at 2.5/25 MHz ;
 - a 4-bit non-standard MII-Lite (MII without the CRS and COL signals) operating at 2.5/25 MHz ;
 - a 2-bit Reduced MII (RMII) operating at 50 MHz ;
 - a (double data rate) 4-bit Reduced GMII (RGMII) operating at 125 MHz.
- CRC-32 checking at full speed with optional forwarding of the frame check sequence (FCS) field to the client ;
- CRC-32 generation and append on transmit or forwarding of user application provided FCS selectable on a per-frame basis ;
- In full-duplex mode:
 - Supports Ethernet pause frame (802.3 Annex 31A) providing fully automated flow control without any user application overhead ;
 - Pause quanta used to form pause frames, dynamically programmable ;
 - Pause frame generation additionally controllable by user application offering flexible traffic flow control ;
 - Optional forwarding of received pause frames to the user application ;
 - Implements standard flow-control mechanism ;
- In half-duplex mode: provides full collision support, including jamming, backoff, and automatic retransmission ;
- Supports VLAN-tagged frames according to IEEE 802.1Q ;
- Programmable MAC address: Insertion on transmit; discards frames with mismatching destination address on receive (except broadcast and pause frames) ;

- Programmable promiscuous mode support to omit MAC destination address checking on receive ;
- Multicast and unicast address filtering on receive based on 64-entry hash table, reducing higher layer processing load ;
- Programmable frame maximum length providing support for any standard or proprietary frame length ;
- Statistics indicators for frame traffic and errors (alignment, CRC, length) and pause frames providing for IEEE 802.3 basic and mandatory management information database (MIB) package and remote network monitoring (RFC 2819) ;
- Simple handshake user application FIFO interface with fully programmable depth and threshold levels ;
- Provides separate status word for each received frame on the user interface providing information such as frame length, frame type, VLAN tag, and error information ;
- Supports internal loopback option ;
- Programmable Clause 22 and Clause 45 MDIO Master interface for PHY device configuration and management ;
- Supports legacy FEC buffer descriptors ;
- Supports interrupt coalescing ;
- Supports credit-based shaping and round robin QoS scheme for traffic shaping bandwidth distribution. Either policy can be combined with time-based shaping ;
- AVB (Audio Video Bridging, IEEE 802.1Qav) features:
 - Credit-based bandwidth distribution policy can be combined with time-based shaping
 - AVB endpoint talker and listener support ;
 - Support for arbitration between different priority traffic (for example, AVB class A, AVB class B, and non-AVB).

The IP protocol performance optimization features include:

- Operates on TCP/IP and UDP/IP and ICMP/IP protocol data or IP header only ;
- Enables wire-speed processing ;
- Supports IPv4 and IPv6 ;
- Transparent passing of frames of other types and protocols ;
- Supports VLAN tagged frames according to IEEE 802.1q with transparent forwarding of VLAN tag and control field ;
- Automatic IP-header and payload (protocol specific) checksum calculation and verification on receive ;
- Automatic IP-header and payload (protocol specific) checksum generation and insertion on transmit. Configurable on a per-frame basis ;
- Supports IP and TCP, UDP, ICMP data for checksum generation and checking ;
- Supports full header options for IPv4 and TCP protocol headers ;
- Provides IPv6 support to datagrams with base header only — datagrams with extension headers are passed transparently unmodified/unchecked ;
- Provides statistics information for received IP and protocol errors ;
- Configurable automatic discard of erroneous frames ;
- Configurable automatic host-to-network (RX) and network-to-host (TX) byte order ; conversion for IP and TCP/UDP/ICMP headers within the frame ;
- Configurable padding remove for short IP datagrams on receive ;
- Configurable Ethernet payload alignment to allow for 32-bit word-aligned header and payload processing ;
- Programmable store-and-forward operation with clock and rate decoupling FIFOs.

The IEEE 1588 features include:

- Supports all IEEE 1588 frames ;
- Allows reference clock to be chosen independently of network speed ;
- Software-programmable precise time-stamping of ingress and egress frames ;
- Timer monitoring capabilities for system calibration and timing accuracy management ;
- Precise time-stamping of external events with programmable interrupt generation ;

- Programmable event and interrupt generation for external system control ;
- Supports hardware- and software-controllable timer synchronization ;
- Provides a 4-channel IEEE 1588 timer. Each channel supports input capture and output compare using the 1588 counter.

Table 86. IC requirements traceability: Ethernet requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_HIO_2-2	This processor shall implement 2 Ethernet controllers	Must have	Yes
iMXRT2660_HIO_2-3	The Ethernet controllers shall support 10Mbps, 100Mbps, and 1Gbps full-duplex operation	Must have	Yes
iMXRT2660_HIO_2-4	The Ethernet controllers shall support 10Mbps and 100Mbps half-duplex operation	Must have	Yes
iMXRT2660_HIO_2-5	The Ethernet controllers shall support following interface to external Ethernet PHY 1) RGMII operating at 125MHz 2) RMII operating at 50MHz 3) MII operating at 25MHz	Must have	Yes
iMXRT2660_HIO_2-6	Both Ethernet ports must be able to independently source their clocks internally and operate independently.	Must have	Yes, see Section Error! Reference source not found.
iMXRT2660_HIO_2-7	The Ethernet controllers shall support preamble / Start of Frame Delimiter (SFD) generation	Must have	Yes for ENET (AVB)
iMXRT2660_HIO_2-8	The Ethernet controllers shall support frame padding.	Must have	Yes
iMXRT2660_HIO_2-9	The Ethernet controllers shall support CRC-32 generation and append on transmit for forwarding	Must have	Yes
iMXRT2660_HIO_2-10	The Ethernet controllers shall support CRC-32 checking at full speed	Must have	Yes
iMXRT2660_HIO_2-11	The Ethernet controllers shall support programmable MAC address	Must have	Yes
iMXRT2660_HIO_2-12	The two Ethernet controller each shall have their own 48-bit MAC address allocated in OTP	Must have	Targeted, Fusetmap to be completed during design phase
iMXRT2660_HIO_2-13	This processor shall support IEEE 1588 time synchronization protocol on both Ethernet ports.	Must have	Supported
iMXRT2660_HIO_2-14	The Ethernet controllers shall support auto-negotiation capabilities for each implemented speed step.	Must have	Yes
iMXRT2660_HIO_2-15	The Ethernet controllers shall support Remote Network Monitoring Management Information Base (RMON MIB) statistics.	Must have	Yes
iMXRT2660_HIO_2-16	The Ethernet controllers shall support Ethernet Pause flow control.	Must have	Yes
iMXRT2660_HIO_2-17	The Ethernet controllers shall support Virtual Local Area Network (VLAN) tag extraction	Must have	Yes
iMXRT2660_HIO_2-18	The Ethernet controllers shall support VLAN tag insertion	Must have	Yes
iMXRT2660_HIO_2-19	The Ethernet controllers shall support VLAN tag filtering	Must have	Yes
iMXRT2660_HIO_2-20	The Ethernet controllers shall support double VLAN tag (Q-in-Q support).	Must have	Rejected, not supported Open: Req. update ongoing

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_HIO_2-21	The Ethernet controllers shall support L3 Checksum offload (IP) for both receive and transmit	Must have	Yes for Rx
iMXRT2660_HIO_2-22	The Ethernet controllers shall support L4 Checksum (TCP/UDP) for both receive and transmit	Must have	Yes for TSN, in SW for AVB
iMXRT2660_HIO_2-23	The Ethernet controllers shall support MAC address filtering.	Must have	Yes
iMXRT2660_HIO_2-24	The Ethernet controllers shall support interrupt coalescing.	Must have	Yes
iMXRT2660_HIO_2-25	The Ethernet controllers shall support Receive Side Coalescing (RSC)	Must have	Rejected Open: Req. update ongoing
iMXRT2660_HIO_2-26	The Ethernet controllers shall support Receive Side Scaling (RSS)	Must have	Rejected Open: Req. update ongoing
iMXRT2660_HIO_2-27	The Ethernet controllers shall support symmetric hashing for TCP/UDP flows.	Must have	Rejected Open: Req. update ongoing
iMXRT2660_HIO_2-28	The Ethernet controllers shall support RSS on IPv4.	Must have	Rejected Open: Req. update ongoing
iMXRT2660_HIO_2-29	The Ethernet controllers shall support RSS on IPv6.	Must have	Rejected Open: Req. update ongoing
iMXRT2660_HIO_2-30	The Ethernet controllers shall support RSS on following protocols: UDP, TCP, SCTP	Must have	Rejected Open: Req. update ongoing
iMXRT2660_HIO_2-31	The Ethernet controllers shall support RSS on IP-NonFragTCP	Must have	Rejected Open: Req. update ongoing
iMXRT2660_HIO_2-32	The Ethernet controllers shall support RSS on IP-NonFragUDP	Must have	Rejected Open: Req. update ongoing
iMXRT2660_HIO_2-33	The Ethernet Controllers shall support RSS on internal IP or on external IP headers in case of IP tunneling (4-in-6 or 6-in-4).	Must have	Rejected Open: Req. update ongoing
iMXRT2660_HIO_2-34	The Ethernet controllers shall support L2 headers.	Must have	Yes
iMXRT2660_HIO_2-35	One of the Ethernet controllers shall support QoS which includes Time-Sensitive Networking (TSN) and Audio Video Bridging (AVB) support.	Must have	Yes
iMXRT2660_HIO_2-36	The Ethernet QoS controller shall include following TSN features: - Time aware shaper - Time synchronization - Frame pre-emption	Must have	Same IP as RT1180 
iMXRT2660_HIO_2-37	The Device shall support Media clock recovery and generation for AVB support.	Must have	Same IP as RT1170

6.4.3XENO Digital PHY (XENO)

The 10BASET1S digital PHY IP, also known as XENO IP, is a first generation digital IP that provides the PMA, PCS, and PLCA Reconciliation Sublayer building blocks compliant to the standard IEEE 802.3cg™ 10BASE-T1S Ethernet Physical Layer. The XENO IP supports the multi-drop variant of the 10BASET1S IEEE 802.3cg™ specification and targets the OpenAlliance TC14 PMD transceiver interface.

The XENO IP does not support the following IEEE standard optional features:

- Clause 146 10BASET1L long-range variant ;
- Clause 147 10BASET1S point-point variant ;
- Clause 98 Auto-Negotiation ;
- Clause 147 Heartbeat function (related to AN).

Fig 46 shows a high-level functional block diagram of the XENO IP.

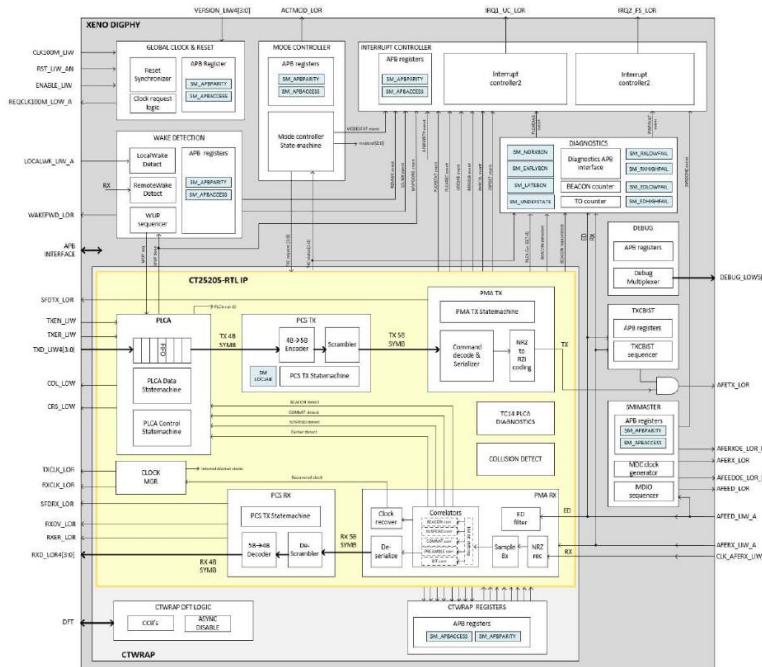


Fig 46. XENO Digital PHY IP block diagram

The XENO IP integrates the 3rd party CT25205-RTL IP from vendor CanovaTech. The CT25205-RTL IP provides the 10BASET1S data-path functionality like the PMA, PCS and PLCA layers.

The XENO IP provides a Media Independent Interface (MII) for interfacing with a IEEE802.3 compliant MAC. The MAC is required to support half-duplex operation at 10Mbps.

For interfacing with an MCU the XENO IP provides an AMBA peripheral BUS (APB) and two identical interrupt controllers; one for handling functional interrupts and one for handling safety-related interrupts. Each interrupt controller provides a single level sensitive active-high output that is asserted when one or more non-masked interrupts are active.

The i.MX RT2660 includes two XENO Digital PHY IPs, each one connecting to the MII interface of a given Ethernet module.

Table 87. IP configuration

Name	Size	Def	Description
			Default values for APB PHY Identifier register
P_DEF_PHYIDOUI	32	'h0	Default value for APB status bits PHYIDOUI
P_DEF_PHYIDICMODEL	32	'h0	Default value for APB status bits PHYIDICMODEL
P_DEF_PHYIDCHIPREV	32	'h0	Default value for APB status bits PHYIDCHIPREV
			Default values for APB TWEAKS register
P_DEF_TWEAKS_RXDELAY	32	'h0	Default value for APB control bits TWEAKS.RXDELAY
P_DEF_TWEAKS_NCOLM	32	'h0	Default value for APB control bits TWEAKS.NCOLM
P_DEF_TWEAKS_RXNRZ	32	'h0	Default value for APB control bits TWEAKS.RXNRZ
P_DEF_TWEAKS_ENIE	32	'h1	Default value for APB control bits TWEAKS.ENIE
			Default values for APB PMATUNE0 register
P_DEF_PMATUNE0_DRFTW	32	'h4	Default value for APB control bits PMATUNE0.DRFTW
P_DEF_PMATUNE0_NNTHR	32	'h20	Default value for APB control bits PMATUNE0.NNTHR
			Default values for APB PMATUNE1 register
P_DEF_PMATUNE1_JJTHR	32	'h20	Default value for APB control bits PMATUNE0.JJTHR
P_DEF_PAMTUNE1_JJHHTHR	32	'h33	Default value for APB control bits PMATUNE0.JJHHTHR
			Default values for APB PMATUNE2 register
P_DEF_PMATUNE2_TXSTATSEL	32	'h1	Default value for APB control bits PMATUNE2.TXSTATSEL
P_DEF_PMATUNE2_SUSPFILT	32	'h1	Default value for APB control bits PMATUNE2.SUSPFILT
P_DEF_PMATUNE2_CSRBYEDPLCA	32	'h0	Default value for APB control bits PMATUNE2.CSRBYEDPLCA
P_DEF_PMATUNE2_CSRBYEDCSMA	32	'h1	Default value for APB control bits PMATUNE2.CSRBYEDCSMA
P_DEF_PMATUNE2_EDLINEACT	32	'h1	Default value for APB control bits PMATUNE2.EDLINEACT
P_DEF_PMATUNE2_EDFILTDATA	32	'h53	Default value for APB control bits PMATUNE2.EDFILTDATA
P_DEF_PMATUNE2_RXBLANKING	32	'h1	Default value for APB control bits PMATUNE2.RXBLANKING
			Default values for APB WUPCFG register
P_DEF_WUPCFG_LCLWKUP	32	'h20	Default value for APB control bits WUPCFG.LCLWKUP
			Default values for APB WUPTUNE register
P_DEF_WUPTUNE_TTTHR	32	'h20	Default value for APB control bits WUPTUNE.TTTHR
			Default values for APB PCSTUNE register
P_DEF_PCSTUNE0_SFDRXMSK	32	'h1	Default value for APB control bits PCSTUNE0.SFDRXMSK

More detailed information of the XENO IP can be found in its integration guide [39].

6.4.4Universal Serial Bus (USB)

The i.MX RT2660 has two USB controller cores. Due to SoC die area reasons, one of them is a USB High-Speed (HS) controller equipped with an on-chip USB HS PHY. The other instance is a USB Full Speed (FS) controller equipped with the smaller on-chip USB FS PHY.

Table 88. IC requirements traceability: USB requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_HIO_1-3	The Device shall include 2x USB 2.0 controllers, which support dual role USB: Host and Device.	Must have	1x USB 2.0, 1x USB 1.1 Open: Req. update ongoing
iMXRT2660_HIO_1-4	The Device shall include 1xUSB 2.0 PHY connecting to the first USB controller to provide an USB 2.0 port, which support High-speed, Full-speed, and Low-Speed USB.	Must have	Yes
iMXRT2660_HIO_1-5	The Device shall include 1xUSB 1.1 PHY connecting to the second USB controller to provide a USB 1.1 port, which support only Full-speed and Low-Speed USB.	Must have	Yes
iMXRT2660_HIO_1-6	The ULPI IO interface of the second USB controller shall be multiplexed out on IO pads for connection to an external USB 2.0 PHY on board.	Must have	Rejected, no ULPI Open: Req. update ongoing
iMXRT2660_HIO_1-7	USB controller shall be compliant to USB Specification version 2.0.	Must have	Yes
iMXRT2660_HIO_1-8	USB 2.0 PHY shall be compliant to USB Specification version 2.0.	Must have	Yes
iMXRT2660_HIO_1-9	USB 1.1 PHY shall be compliant to USB Specification version 1.1	Must have	Yes
iMXRT2660_HIO_1-10	The USB Host shall be EHCI compatibility	Must have	Yes
iMXRT2660_HIO_1-11	The USB Device shall support up to 8 bidirectional endpoints, including a pair of Control endpoints.	Must have	Yes
iMXRT2660_HIO_1-12	The USB Device shall support configurable endpoint-type for each endpoint, except the Control endpoint.	Must have	Yes
iMXRT2660_HIO_1-13	The USB port shall support Crystal-less Full-Speed USB operation in Device mode	Should have	Targeted
iMXRT2660_HIO_1-14	The USB port shall support Link Power Management (LPM) mechanism.	Must have	Yes USB0 only
iMXRT2660_HIO_1-15	The USB port shall support DP/DM lane reversal.	Must have	USB1 only Open: Req. update ongoing
iMXRT2660_HIO_1-17	The USB port shall support Attach Detection Protocol (ADP).	Must have	Rejected Open: Req. update ongoing

6.4.4.1 USB HS PHY

The i.MX RT2660 makes use of an integrated USB High-Speed (HS) PHY module that has been designed in-house. The USB HS PHY module communicates with the USB HS controller using a standard UTMI+ interface. The PHY includes a 480 MHz PLL, digital logic and state machines, analog transceiver circuits, and an IPS bus interface for configuration and status reporting. The USB_DP and USB_DM pins connect directly to a USB connector. Fig 47 shows a high-level block diagram of the USB PHY module.

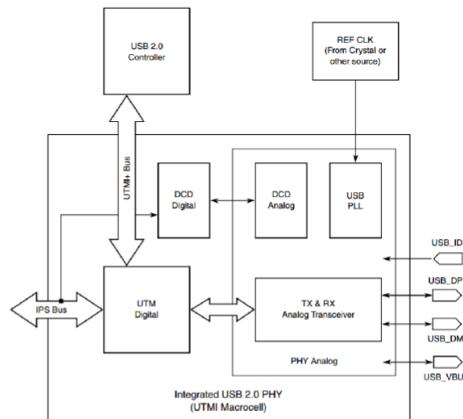


Fig 47. USB PHY module block diagram

The USB_ID is not used, but instead one can make use of a GPIO (interrupt) to mimic USB_ID function with more flexibility. This means that application software shall define a spare GPIO as USB_ID function.

The USB PHY IP is a new IP development for which a draft integration manual has been provided. For the i.MX RT2660, the following changes are needed to be accommodated:

- 480MHz PLL inside USB HS PHY shall support input clock frequency range: 16 – 40 MHz ;
- 480MHz PLL shall be able to operate standalone, i.e. independent from the USB HS PHY ;
- A PLL output of 48MHz clock shall be provided, to be used as input clock to USB1 instance that support FS operation.

More detailed information of the USB HS PHY IP can be found in its integration guide [40].

6.4.4.2 USB HS Controller

The USB HS controller shall be re-used from i.MX RT700. Fig 48 shows its high-level functional block diagram.

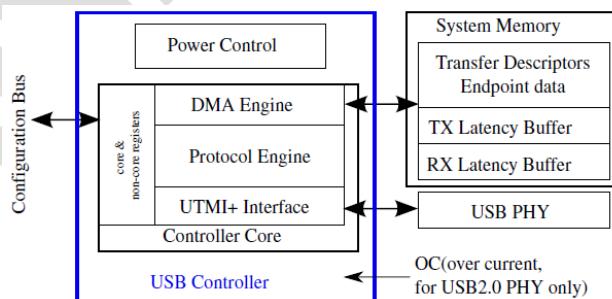


Fig 48. USB HS controller block diagram

The key features of the USB HS controller are as follows:

- HS/FS/LS dual role core ;
- HS/FS/LS UTMI compliant interface ;
- HS, FS and LS operation in HOST mode (with UTMI transceiver) ;
- HS and FS operation in Peripheral mode (with UTMI transceiver) ;
- 8 bidirectional endpoints ;
- Support charger detection ;

- Connected to on-chip PHY ;
- Low-power mode with local and remote wake-up capability ;
- Embedded DMA controller.

More detailed information of the USB HS Controller IP can be found in its block guide .

6.4.4.3 USB FS Controller & -Transceiver

The USB FS controller and transceiver shall be re-used from MCX. Fig 49 shows its high-level functional block diagram.

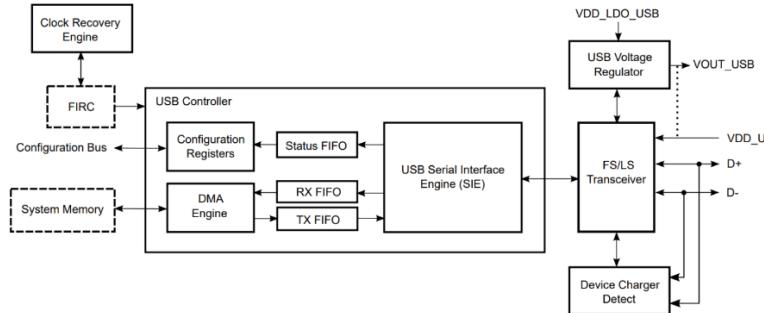


Fig 49. USB FS controller block diagram

The key features of the USB FS controller are as follows:

- Dual-role USB OTG-capable (On-The-Go) controller that supports Full Speed (FS) Device or FS/Low Speed (LS) Embedded Host operation. The controller operates with DMA or FIFO data stream interfaces and supports up to 16 bidirectional endpoints. The module complies with the USB 2.0 Specification.
- USB transceiver that includes internal 15 kΩ pulldowns on the D+ and D- lines for Host mode functionality and a 1.5 kΩ pullup on the D+ line for Device mode functionality.
- A 5.0 V to 3.3 V voltage regulator used for the USB transceiver ;
- USB Device Charger Detection module with features for USB Battery Charging 1.2 detection and signaling ;
- FIRC with clock recovery block to eliminate the need for a clock from a PLL or a 48 MHz crystal. The USB frequency tuning feature is available for USB Device mode operation only ;
- Status detection and wakeup functions for USB data pins, USB voltage regulator input pin and GPIO pins used for VBUS and OTG ID detection ;
- Keep Alive mode allowing operation in Sleep mode for certain USB low-traffic situations without needing to restart the USB session after exiting the low power mode. In this mode the USBFS subsystem can respond to IN tokens with NAK replies and initiate wakeup for SETUP or software-assigned tokens ;
- A configurable connection to allow any one of the LPUART transmit and receive pins to be connected to the Full Speed USB physical layer ;
- Lane reversal feature to allow switching the roles of package USB0_DM and USB0_DP pins providing additional flexibility for PC board layout.

More detailed information of the USB FS IP can be found in its block guide [41].

6.4.5xSPI Responder (xSPIR)

The xSPI responder (xSPIR) provides a method that external device can access memory mapped registers, memories in i.MX RT2660 SoC. The module works as a SPI follower; it communicates with another chip/FPGA via the SPI bus protocol. A remote chip with an SPI leader can read or write this block's internal registers, or it can access the SOC's address via this block's AXI bus. To avoid xSPIR

is used as a backdoor to sensitive data on chip, the xSPIR supports access control and read/write protection.

Fig 50 shows a high-level block diagram of the xSPIR module.

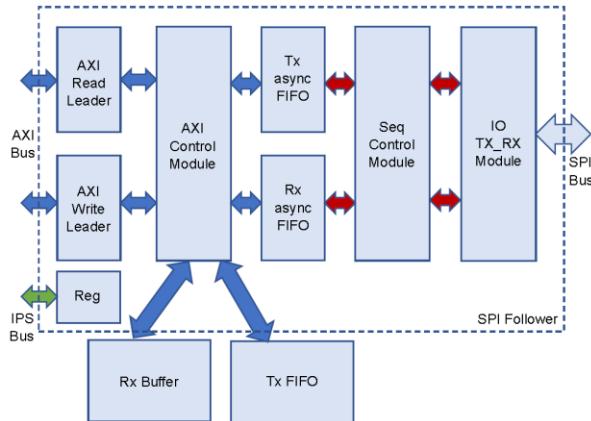


Fig 50. xSPI responder block diagram

The main features of the xSPIR module are:

- SPI support for DDR/SDR, Octal/Quad mode ;
- DQS output during read commands, assisting the SPI leader with data sampling ;
- DQS input during write commands, as DATA strobe only in Octal DDR mode to support unaligned writes ;
- Automatic stop of DQS toggling during read commands to avoid FIFO underflow ;
- Support for memory read and write commands, and for register read and write commands with configurable command code and dummy cycles ;
- Support for Inter-Processor Communication (IPC) protocol for SPI leader and follower communication ;
- Support for 9x32-bit mailbox regs which are writable/readable via the SPI leader, and are only readable via the SOC ;
- Support for asynchronous interrupt through mailbox which can be set by SPI leader ;
- Independent AXI write and read leaders ;
- Support for four independent read leaders ;
- Support for two different pairs of SPI memory read/write commands to access two different locations in SOC via the AXI Bus ;
- Support for configurable AXI memory-base-address setting and address-range setting via register ;
- Support for blocking AXI reads and writes, to ignore requests from SPI leader.

Table 89. **IC requirements traceability: XSPI responder requirements**

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_HIO_4-2	This processor shall implement one xSPI Responder controller, which can provide a memory-mapped interface to an external host processor.	Must have	Yes
iMXRT2660_HIO_4-3	The xSPI Responder interface shall be compliant to JEDEC XSPI standard specification v1.0	Must have	Yes
iMXRT2660_HIO_4-4	The xSPI Responder shall support both Profile 1 (Octal SPI protocol) and Profile 2 (HyperBus protocol) defined in the XSPI standard specification.	Must have	Yes
iMXRT2660_HIO_4-5	The xSPI Responder interface shall support 1-bit, 4-bit, and 8-bit IO modes	Must have	Quad/Octal yes, 1-bit not

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_HIO_4-6	The xSPI Responder shall operate up to 133MHz	Must have	Open: Req. update ongoing Yes
iMXRT2660_HIO_4-7	The xSPI Responder shall support SDR and DDR signaling	Must have	Yes
iMXRT2660_HIO_4-8	The xSPI Responder shall include a location DMA engine	Must have	No Open: Req. update ongoing
iMXRT2660_HIO_4-9	The xSPI Responder shall include the MU (Message Unit), which can provide a mailbox for inter-processor communication with the external host processor	Must have	Yes, 9x32-bit mailbox

6.4.6 Bus system

The ARM NIC-400 IP is the interconnect fabric of the COMM_SS, referred to as NIC_COMM. It runs at an operating frequency of up to 200 MHz. NIC_COMM maintains a 1:1 clock-synchronous relationship with its building blocks, and is configured as 64-bit bus fabric.

The following NIC_COMM configuration shall be supported:

- Hierarchical clock gating enabled ;
- Quality of Service feature enabled ;
- Arbitration shall be programmable ;
- 'Single Slave per ID' as Cyclic Dependency Avoidance Scheme (CDAS) ;

Table 90 lists the NIC_COMM path connectivity between ASIB and AMIB ports.

Table 90. Path connectivity of NIC_COMM bus fabric

ASIB port	AMIB port
USDHCO_AXIM	X
USDHCI_AXIM	X
USB0_AHB	X
USB1_AHB	X
xSPI Responder	X
ETH0_AXIM	X
ETH1_RX_AXIM	X
ETH1_TX_AXIM	X
GPV	

'X' indicates a connection, while '-' indicates no connection

Note that all input- and output ports shall be configured as clock synchronous 1:1 or clock asynchronous, depending on port type.

Table 91. Interface configuration of NIC_COMM

Ports		s_d_0	s_d_1	s_d_2	s_d_3	s_d_4	s_d_5	s_d_6	s_d_7	s_d_8	m_d_0
Specification	Hookup	USDHCO_AXIM	USDHCI1_AXIM	USB0_AHB	USB1_AHB	XSPI Responder	ETH0_AXIM	ETH1_RX_AXIM	ETH1_TX_AXIM	GPV	COMM2MAIN
	HierarchicalClockGating	yes	yes	yes	yes	yes	yes	yes	yes	yes	yes
	UppercaseRTLSignals	true	true	true	true	true	true	true	true	true	true
	QoSEnabled	true	true	true	true	true	true	true	true	true	true
	QVNEnabled	No	No	No	No	No	No	No	No	No	No
	AWUSERWidth	13	13	13	13	13	13	13	13	13	13
	ARUSERWidth	13	13	13	13	13	13	13	13	13	13
	WUSERWidth	0	0	0	0	0	0	0	0	0	0
	BUSERWidth	0	0	0	0	0	0	0	0	0	0
	RUSERWidth	0	0	0	0	0	0	0	0	0	0
ClockDomain	Name	comm	comm	comm	comm	comm	comm	comm	comm	gpv	comm
	Frequency	200M	200M	200M	200M	200M	200M	200M	200M	200M	200M
LocalGroup	Name	grp0	grp0	grp0	grp0	grp0	grp0	grp0	grp0	grp0	grp0
	ClockRef	comm	comm	comm	comm	comm	comm	comm	comm	comm	comm
	Protocol	AXI3	AXI3	AXI3	AXI3	AXI3	AXI3	AXI3	AXI3	AHBLiteTarget	AXI4
	AddressWidth	32	32	32	32	32	32	32	32	32	32
	DataWidth	32	32	32	32	64	64	64	64	64	64
	ARUSEREnabled	true	true	true	true	true	true	true	true	true	true
	AWUSEREnabled	true	true	true	true	true	true	true	true	true	true
	VIDWidth	8	8	4	4	8	4	4	4	NA	NA
	TrustZoneSlave	per_access_secure	per_access_secure	per_access_secure	per_access_secure	per_access_sec	per_access_se	per_access_sec	per_access_sec	secure	non_secure
	Readissuing/ReadAcceptance	2	2	8	8	2	8	8	8	1	8
	WriteIssuing/WriteAcceptance	4	4	8	8	4	8	8	8	1	8
	TotalIssuing	NA	NA	NA	NA	NA	NA	NA	NA	NA	8
	IDWidthReduction	NA	NA	NA	NA	NA	NA	NA	NA	NA	true
	OutputSignals	NA	NA	NA	NA	NA	NA	NA	NA	NA	true
	QoSType	programmable	programmable	programmable	programmable	programmable	programmable	programmable	programmable	fixed	NA
	Advanced	Prog.GPV	Prog.GPV	Prog.GPV	Prog.GPV	Prog.GPV	Prog.GPV	Prog.GPV	Prog.GPV	Config Port	Prog.GPV
	CDAS	slave_per_id	slave_per_id	slave_per_id	slave_per_id	slave_per_id	slave_per_id	slave_per_id	slave_per_id	single_slave	NA
	TransactionRateRegulation	true	true	true	true	true	true	true	true	true	NA
	OutstandingTransactionRegulation	true	true	true	true	true	true	true	true	true	NA
	LatencyPeriodRegulation	true	true	true	true	true	true	true	true	true	NA
Interface	BrokenBursts	NA	NA	NA	NA	NA	NA	NA	NA	TRUE	NA
Fifo	ar fifo	0	0	0	0	0	0	0	0	0	0
	aw fifo	0	0	0	0	0	0	0	0	0	0
	r fifo	0	0	0	0	0	0	0	0	0	0
	w fifo	0	0	0	0	0	0	0	0	0	0
	b fifo	0	0	0	0	0	0	0	0	0	0

6.4.7 Frequency Measure Unit (FREQME)

The main purpose of the FREQME unit to measure the frequency of the IP functional clocks and - bus clocks. Refer to Section 6.2.7 for a brief description about the FREQME unit

The COMM_SS includes one FREQME unit one to monitor the MODCON_COMM clock outputs (COMM.FREQME). Please refer to the RT2660_Clock_v<version>.xlsx in share point [Clock](#) for detailed assignment.

6.4.8 Cross-Trigger network

The i.MX RT2660 COMM_SS has one XBAR instance: XBAR0. Its purpose is to reduce the amount of COMM_SS trigger outputs towards the other i.MX RT2660 subsystems. The COMM_SS XBAR configuration is shown in Table 92 and Fig 51, respectively.

Table 92. i.MX RT2660 COMM_SS XBAR instance configuration

Instance	Number of inputs (N)	Number of outputs (M)	Number of outputs with control function (P)	Select registers	Control registers
XBAR0	21	10	0	XBAR0.SEL0	n/a

Fig 51 shows a high-level block diagram of the COMM_SS cross-trigger network.

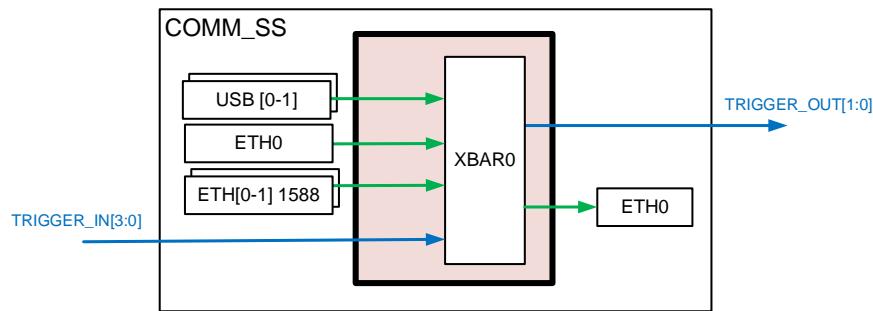


Fig 51. i.MX RT2660 COMM_SS cross-trigger network block diagram

Please refer to Section 6.3.8.2 for an overview on how the COMM_SS cross-trigger network shall be interconnected with the remainder of the SoC.

The i.MX RT2660 detailed Cross-Trigger Network assignments in a machine-readable format can be found at the following location: [XEA1_XbarMap.xlsx](#)

Please refer to the **COMM_SS HW.AS** document for a detailed COMM_SS trigger assignments [7].

6.5 AUDIO-VISUAL Domain: MEDIA Sub-System (MEDIA_SS)

The MEDIA subsystem of i.MX RT2660 is part of the AUDIO-VISUAL domain. It concerns a medium performance section that includes camera- and display interfaces as well as graphics processing blocks. It runs at an operating frequency of up to 350 MHz in Normal Run mode. The MEDIA_SS maintains a clock-asynchronous relationship with the rest of the SoC. Its architectural block diagram is shown in Fig 52. The MEDIA subsystem of i.MX RT2660 is a subset of the XEA-1 platform version.

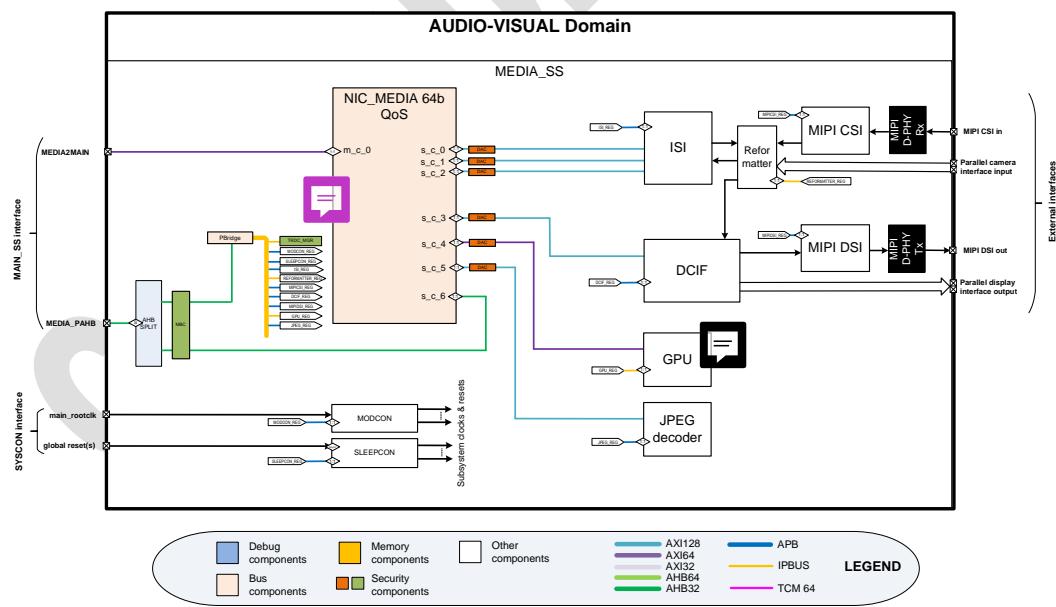


Fig 52. Architectural block diagram of i.MX RT2660's MEDIA_SS [5]

For the origin of the main building blocks, their maturity level and their legacy i.MX sourcing product, please refer to the IP Re-Use Sheet that is listed in Chapter 15. The MEDIA_SS building blocks has been described in more detail in the following sub-sections.

For more detailed information, please refer to the MEDIA_SS HW AS document [5]

This document includes the RT2660 specific IP configurations.

6.5.1 Camera

The i.MX RT2660 is targeting same camera subsystem as deployed on i.MX95, extended with a parallel camera interface. The i.MX RT2660 contains a camera sub-system that comprises of the following main components:

1. A Mobile Industry Processor Interface (MIPI) Display Serial Interface (DSI) D-PHY that supports serial camera interfaces with 1 clock- and 2 data lanes ;
2. A MIPI Camera Serial Interface (CSI) Host Controller implementing protocol functions compliant to the MIPI CSI Host Specification ;
3. A Reformatter, to convert pixel format of serial or parallel camera inputs to pixel link format for ISI, and to provide pixel link format from ISI to provide output directly to display controller ;
4. An Image Sensor Interface (ISI) block, with direct output to DCIF via Reformatter.

Fig 53 provides a high-level illustration of the camera subsystem of the i.MX RT2660.

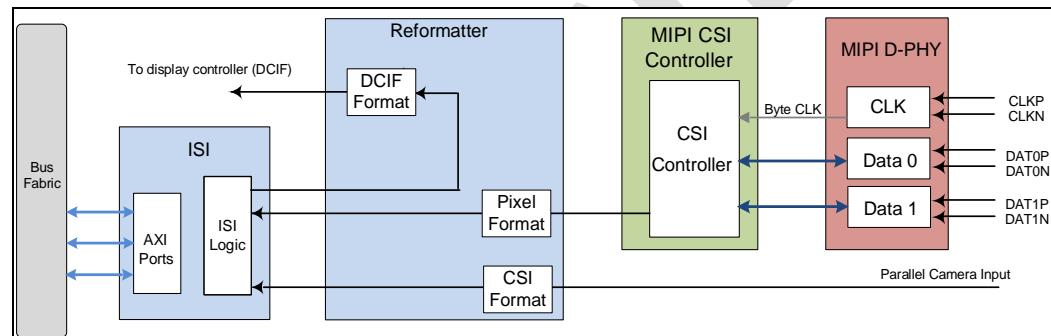


Fig 53. Camera signal chain in i.MX RT2660's MEDIA_SS

Table 93. IC requirements traceability: Camera requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_CAM_1-2	Camera performance	Heading	-
iMXRT2660_CAM_1-3	The camera subsystem shall be capable of supporting 2.3Mpixel camera resolution, 24bpp, up to 60fps on MIPI CSI interface.	Must have	Yes
iMXRT2660_CAM_1-4	The Device shall support 1x monochrome camera up to 3MP @ 30fps, with Y8 format, over MIPI CSI.	Must have	Yes
iMXRT2660_CAM_1-5	The camera subsystem shall be capable of supporting 2.3Mpixel camera resolution, 16bpp, up to 30fps on parallel interface.	Must have	Yes
iMXRT2660_CAM_9-1	Camera Subsystem	Heading	-
iMXRT2660_CAM_9-2	The Camera subsystem shall include: - The MIPI CSI controller. This IP will be licensed from an external IP vendor. - The MIPI D-PHY. This IP will be licensed from an external IP vendor. - Video MUX controller. This is an internal IP. - IO interface of the parallel camera interface. - Image Sensor Interface. This is an internal IP.	Must have	Yes The Video Mux is now called re-formater

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_CAM_9-5	The camera subsystem shall provide a parallel data interface to the display controller for camera preview use case, which has input video camera directly displayed on panel.	Must have	New IP development (Reformatter)
iMXRT2660_CAM_7-1	Camera I2C	Heading	-
iMXRT2660_CAM_7-2	This processor shall include a local I2C port to provide communication path to the camera sensor.	Should have	No, use I2C in HSP_SS
iMXRT2660_CAM_8-1	Camera sensor vendors	Heading	-
iMXRT2660_CAM_8-2	This processor shall support camera sensors of following vendors: Aptina, Magnachip, Omnivision, On Semi, Sony, SmartSens.	Must have	Rejected, need specific part numbers
iMXRT2660_CAM_8-3	The Device shall support ISP chips from following vendors: Omnivision, On Semi, Sony.	Must have	Rejected, need specific part numbers

6.5.1.1 MIPI CSI

Clarification item for PDA: It is decided to proceed with Mixel as third-party supplier for MIPI CSI solution. Sofar we have only received IP for evaluation purposes; chip lead to confirm whether no changes are applicable to the product IP version, and related IP documentation is to be provided for both MIPI D-PHY and Host controller.

A.1 MIPI D-PHY CSI-2

The 22FDX MIPI D-PHY solution from Mixel has been selected for usage in i.MX RT2660. Fig 54 shows a high-level block diagram of Mixel's MIPI D-PHY Rx IP for camera interfacing.

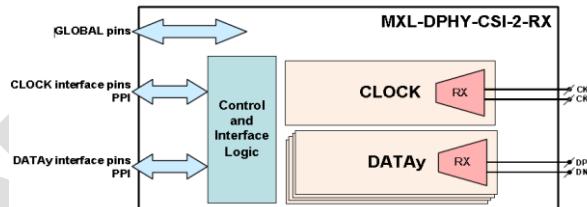


Fig 54. Mixel MIPI D-PHY block diagram

Table 94 provides a high-level overview of Mixel's 22FDX MIPI D-PHY main characteristics with a focus on the CSI-2/Rx functionality only.

Table 94. Mixel 22FDX MIPI D-PHY CSI-2 IP characteristics

Parameter	Mixel
IP name	MXL-DPHY-CSI2-RX
IP macro	Separate Rx macro, or single Tx/Rx combo
IP area	Rx: 0.23 mm ² (including IOs/ESD) Tx/Rx combo: 0.57mm ² (including IOs/ESD)
Metal stack	10M_2Mx_5Cx_1Jx_2Qx_LB
Power supply	Analog IO: 1.8V ±10% Analog core: 0.8V ±10%
Temperature range	-40 up to +125°C
Functionality	
Number of lanes	1 clock lane, up to 4 data lanes

Operating modes	High-Speed, Low-Power, Ultra-Low-Power, Power Down
MIPI Specification compliance	D-PHY version 2.1. Backward compatible w/ v1.2
High-speed de-serializers	Yes
Testability support	Yes (ATE, BIST)
Packaging support	Wirebond & flip-chip
High-Speed mode with 2-lane configuration	
Performance	80Mbps to 1.5Gbps per lane up to 2.5Gbps per lane (w/ Deskew)
Typical current @2.5Gbps	7.5mA (analog), 2.7mA (IO)
Low-Power mode with 2-lane configuration	
Performance	10Mbps data rate
Typical current (LP) @10Mbps	55.7µA (analog), 500µA (IO)
Power down mode	
Typical current	43µA (analog), 0.3µA (IO)

Table 95. IC requirements traceability: MIPI D-PHY CSI-2 requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_CAM_4-2	The CSI D-PHY shall meet all requirements listed in the MIPI performance and MIPI CSI interface.	Must have	Yes
iMXRT2660_CAM_4-3	The D-PHY configuration is 2 Rx data lane for CSI interface and IOs.	Must have	Yes
iMXRT2660_CAM_4-4	The D-PHY shall support scalable data lane: 1 or 2 data lanes can be configured.	Must have	Yes
iMXRT2660_CAM_4-5	The D-PHY IP shall include High Speed Serializers.	Must have	Yes
iMXRT2660_CAM_4-6	The D-PHY IP shall include all IO and PWR/GND pads in the PHY macro.	Must have	Yes
iMXRT2660_CAM_4-7	The D-PHY IP shall include all test functions.	Must have	Yes
iMXRT2660_CAM_4-8	The D-PHY shall support High Speed mode and Low Power mode.	Must have	Yes
iMXRT2660_CAM_4-9	The D-PHY shall support High Speed mode up to 2.5Gbps data rate.	Must have	Yes
iMXRT2660_CAM_4-10	The D-PHY shall support 10Mbps data rate in Low Power mode.	Must have	Yes

A.2 MIPI-CSI2 Controller V2

The MIPI-CSI2 Controller Core V2 is 3rd part IP from RAMBUS. The CSI-2 Controller Core V2 provides a flexible, high-performance, easy-to-use MIPI CSI-2 Controller.

Key features include:

- MIPI Alliance Standard for CSI-2 Version 2.1 compliant ;
- Implements all three CSI-2 MIPI Layers (Pixel to Byte packing, Low Level Protocol, Lane Management) ;
- Supports CSI-2 Unidirectional Master operation ;
- Transmitter and Receiver versions ;
- Scalable D-PHY data lane support, 1 to 8 Data Lanes ;
- Scalable C-PHY data lane support, 1 to 4 Data Lanes ;
- Supports high speed (4.5+ Gbit/s) D-PHY operation ;
- Supports high speed (2.5+ Gsym/s) C-PHY operation ;
- Support for all CSI-2 data types ;
- Virtual Channel support including optional VCX support ;
- Support for Per Lane Data Scrambling/Descrambling ;
- Support for D-PHY and C-PHY Ultra Low Power State (ULPS) ;

- Optional support for COMP8 compression
 - 10-8-10 and 12-8-12 ;
- Error collection support (Rx Only) ;
- Flexible pixel-based local user interface ;
 - Supports user generated packets ;
 - Supports packet interface mode for bypass byte<>pixel conversions ;
 - Supports a single, double, quad, or octal pixel interface ;
 - Optional FIFO if needed by customer's specific timing/bandwidth requirements ;
- Supports PHY Protocol Interface (PPI) compatible with MIPI D-PHYs, C-PHYs, and combo C-PHY/D-PHYs ;
- Optional TX Video Interface ;
- Optional RX Video Interface ;
- Optional APB Control and Status Register (CSR) interface with IRQ support.

Table 96. IC requirements traceability: MIPI CSI requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_CAM_2-2	This processor shall instantiate a MIPI CSI port.	Must have	Yes
iMXRT2660_CAM_2-3	The MIPI CSI shall have 2 lanes.	Must have	1 Clock- & 2 Data lanes
iMXRT2660_CAM_2-4	The MIPI CSI shall be compliant to MIPI standard CSI-2 Version 2.1.	Must have	Yes
iMXRT2660_CAM_2-5	The MIPI PHY shall be compliant to MIPI standard D-PHY Version 2.1 up to 2.5Gbps	Must have	Yes
iMXRT2660_CAM_2-6	The MIPI CSI shall support at least two virtual channels.	Must have	Yes

Table 97. IC requirements traceability: CSI Controller requirements (part i)

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_CAM_3-2	The CSI controller shall meet all requirements listed in the MIPI performance and MIPI CSI interface.	Must have	Yes
iMXRT2660_CAM_3-3	The CSI controller shall support PHY Protocol Interface (PPI) compatible MIPI D-PHY .	Must have	Yes
iMXRT2660_CAM_3-6	The CSI controller shall support scalable data lane: 1 or 2 data lanes can be configured.	Must have	Yes
iMXRT2660_CAM_3-8	The CSI controller shall support error correction	Must have	Yes
iMXRT2660_CAM_3-9	The CSI controller shall support High Speed and Low Power operation	Must have	Yes

6.5.1.2 Reformatter

The Reformatter is a gasket between MIPI CSI, Parallel CSI, ISI and DCIF. It shall implement the following main functions:

- Fix interface mismatch between MIPI CSI and ISI pixel link ;
- Fix interface mismatch between parallel camera sensor input and ISI pixel link ;
- Fix interface mismatch between ISI Display Output (pixel link) and DCIF.

The Reformatter a new IP development that needs to be started.

Bug fixes – The exists a legacy RT1170 Video Mux IP. Note that it must be confirmed that the following bugs due to design flaws in the RT1170 IP are not present with the new IP development:

- RAW data and YUV(10-bit/12-bit) formats are not supported on RT1170 due to design defects, which caused us to lose a lot of customers. Please refer to TKT0551654 ;

- Pixels from MIPI-CSI are forced to 32-bit on RT1170, which would waste memory spaces and bus bandwidth. For example, 16-bit RGB565 pixels from MIPI-CSI would be forced to 32-bit XRGB8888.

Table 98. IC requirements traceability: CSI Controller requirements (part ii)

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_CAM_3-4	The CSI controller shall support pixel-based user interface that is compatible with the ISI.	Must have	Targeted with Reformatter IP
iMXRT2660_CAM_3-5	The CSI controller shall implement any additional sideband signals for the seamless inter-operation with the ISI as necessary.	Must have	Targeted with Reformatter IP
iMXRT2660_CAM_3-7	The CSI controller shall implement all three CSI layers: - Pixel to Byte packing - Low level protocol - Lane management	Must have	Targeted with Reformatter IP
iMXRT2660_CAM_9-2	This processor shall include a parallel camera sensor interface.	Must have	Targeted with Reformatter IP
iMXRT2660_CAM_9-3	The parallel CSI shall support 8-bit, 16-bit, and 24-bit data port for YUV and RGB data input.	Must have	Targeted with Reformatter IP
iMXRT2660_CAM_9-4	The parallel CSI shall support 8-bit, 10-bit, and 16-bit data port for RAW (or Bayer) data input.	Must have	Targeted with Reformatter IP
iMXRT2660_CAM_6-2	This device shall include a Video MUX Controller as shown in the Camera subsystem diagram.	Must have	Targeted with ISI and new Reformatter IP

6.5.1.3 Image Sensor Interface (ISI)

In the i.MX RT2660, the Image Sensor Interface (ISI) module interfaces up to 2-pixel link sources to obtain the image data for processing in its pipeline channels. Each pipeline processes the image line from a configured source and performs one or more functions that are configured by software, such as down scaling, color space conversion, de-interlacing, alpha insertion, cropping and rotation (horizontal and vertical). The processed image is stored into programmable memory locations.

This i.MX RT2660 ISI module can process up to 2 image sources at the same time and can output the processed image to memory. This block can concatenate the internal line buffers such that higher resolution images can be processed. This module implements limited flow control mechanism to control output from its internal buffer flushing or sourcing an image from memory. Depending on the format type, this module is capable of processing and storing one line of pixels from the incoming frame.

The i.MX RT2660 ISI module is re-used from [i.MX 8ULP](#), which also concerns a 2-channel version. Fig 55 shows the high-level block diagram of the ISI module.

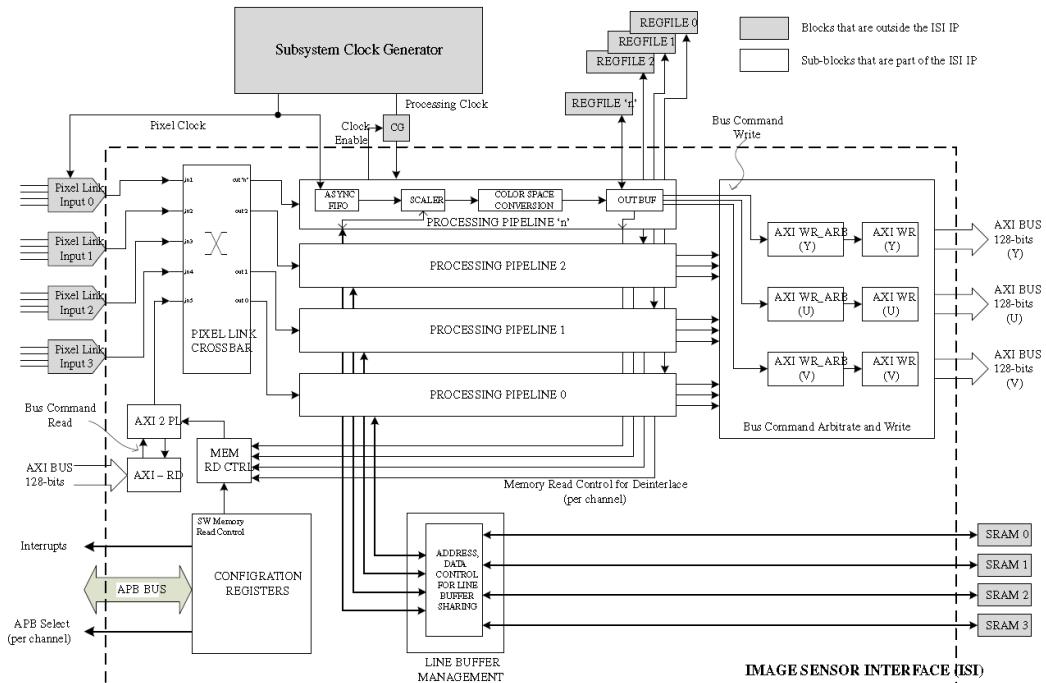


Fig 55. Image Sensor Interface block diagram

The i.MX RT2660 ISI module offers the following main features:

- Supports one source of 4K resolution at 30 fps (24bpp) ;
- Supports up to 2K resolution at 30 or 60 fps (24bpp) on each channel ;
- Input sources supported:
 - 2 pixel link interfaces running in parallel that can interface to 2 camera sensors ;
 - System Memory (AXI master; internally converted to Pixel Link Interface) ;
- Each processing pipeline can be assigned to the same or different pixel input source ;
- Stream Multiplexing
 - Differentiates multiple cameras from a single 2-lane MIPI input ;
 - Duplicates input stream into multiple outputs ;
 - Simple De-Interlacing methods supported for MIPI-CSI Interlaced input sources:
 - Weaving ;
 - Line Doubling ;
 - Linear Interpolation or Averaging ;
 - One input source can be processed in more than one processing channels ;
- Stream Manipulation Features
 - Supported Pixel Formats when storing image into memory
 - RAW8, RAW10, RAW12, RAW16 ;
 - RGB888, BGR888, RGB565, RGB 10-bit, BGR 10-bit ;
 - YUV444, YUV422, YUV420 (8-,10-,12-bit) in (semi-)planar formats;
 - Plus more formats listed in the description of FORMAT field in the channel's IMG_CTRL register ;
 - Downscaling of input image via Decimation and Bilinear filtering
 - Decimation by 2, 4, or 8 supported ;
 - Bilinear filter further downscals by 1.0 to 2.0 (fractional downscaling) ;
 - Color Space Conversion (CSC)
 - RgB, YUV, YCbCr ;
 - User defined color space matrix based conversion ;
 - Alpha channel insertion for RGB formats
 - Global alpha value ;

- Separate rectangular region of interest (ROI) alpha value. ROI alpha values have higher priority than global alpha value
 - Up to 4 ROI non-overlapping rectangles supported ;
- Mirroring (Image Flip): Horizontal and Vertical flips supported ;
- Frame Awareness, Frame Skipping
 - Clean frame start, shutdown based on HSYNC and VSYNC ;
 - Buffer overrun protection ;
 - Buffer under run deterministic behavior ;
- Stream Output Options
 - Output to Memory
 - Input source will be converted to and processed by the processing pipeline as YUV444 or RGB ;
 - Processed images will be output from pipeline and stored into memory location specified by software ;
 - Full line storage available at processing channel output before outputting data to AXI. This storage can automatically split or combine depending on the output format being used ;
 - Dual buffered addresses used in ping pong fashion with active buffer status indication ;
 - Line and Frame stored interrupt status to software to track progress of frame ;
- Flow Control
 - Panic indication to software and device to increase priority of its write transactions to avoid potential overflow in output buffers. Software can configure thresholds for panic indication ;
 - When pixels are sourced from memory or input line buffers are flushed, software has the option to program the rate at which pixels will be sent out. By default, one pixel per clock is sent out ;
 - Back pressure mechanism to stall the channel pipeline during line buffer flushing and sourcing image from memory, when AXI bus is unable accept data and the output buffers are low on storage.

Each ISI processing channel requires a number of 2-port register file instances as shown in the table below.

Table 99. **ISI local memories configuration for each ISI channel**

Target	Purpose	Total size	# words	# bits	# instances
2PREG	Line Buffer Channel	12KB	2048	24	2
2PREG	Y Buffer Register File 1 Channel	8KB	256	128	2
2PREG	Y Buffer Register File 2 Channel	8KB	256	128	2
2PREG	U Buffer Register File 1 Channel	8KB	256	128	2
2PREG	U Buffer Register File 2 Channel	8KB	256	128	2
2PREG	V Buffer Register File 1 Channel	8KB	256	128	2
2PREG	V Buffer Register File 2 Channel	8KB	256	128	2

Table 100. **IC requirements traceability: Image Sensor Interface requirements**

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_CAM_5-2	This processor shall include an Image Sensor Interface (ISI) to perform image processing operations on input data, such streaming multiplexing, downscaling, or color conversion.	Must have	Yes

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_CAM_5-3	The ISI controller shall implement any additional sideband signals for the seamless inter-operation with the CSI controller as necessary.	Must have	Yes
iMXRT2660_CAM_5-4	The ISI shall support multiple cameras from a single MIPI CSI interface.	Must have	Yes, Stream Multiplexing
iMXRT2660_CAM_5-5	The ISI shall support pixel formats from smart camera sensors, including: - RGB888, RGB565, RGB 10-bit - YUV444, YUV422, YUV420 - Y8, Y10, Y12 (TKT0615774) - RAW8, RAW10, RAW12, RAW16	Must have	CR needed
iMXRT2660_CAM_5-6	The ISI shall support downscaling of input image via Decimation and Bilinear filtering.	Must have	Yes
iMXRT2660_CAM_5-7	The ISI shall support Color Space Conversion (cSC) for RGB, YUV, YCbCr.	Must have	Yes

6.5.2 Display

The i.MX RT2660 contains a display sub-system that comprises of the following main components:

1. A MIPI DSI D-PHY that supports serial display interfaces with 1 clock- and 2 data lanes ;
2. A MIPI DSI Host Controller implementing protocol functions compliant to the MIPI DSI Host Specification ;
3. A Display Controller including a Frame Block De-Compression block.

Fig 56 provides a high-level illustration of the display subsystem of the i.MX RT2660.

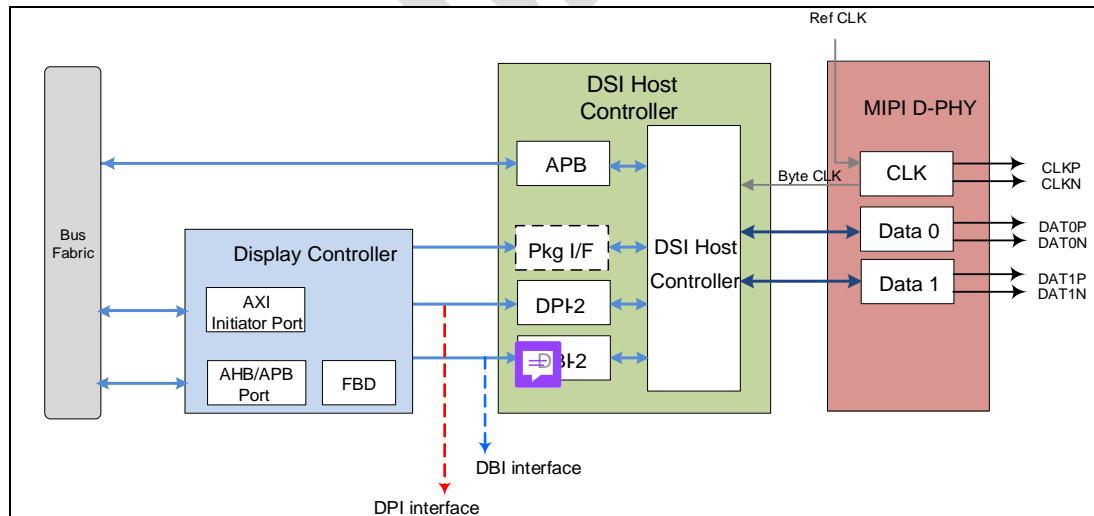


Fig 56. Display signal chain in i.MX RT2660's MEDIA_SS

Table 101. IC requirements traceability: Display subsystem requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_DIS_1-2	Display Performance	Heading	-
iMXRT2660_DIS_1-3	The display subsystem shall be capable of supporting 720p display resolution, 24bpp, up to 60fps on any display interface.	Must have	Yes

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_DIS_1-4	The display subsystem shall be capable of supporting 1080p display resolution, 24bpp, up to 30fps on any display interface.	Must have	Yes For smart screens
iMXRT2660_DIS_2-1	Display subsystem	Heading	-
iMXRT2660_DIS_2-2	The Display subsystem shall include: - The display controller. It presumes the in-house DCIF IP is the display controller on this MCU. - The MIPI DSI host controller. This IP will be licensed from an external IP vendor. - The MIPI D-PHY. This IP will be licensed from an external IP vendor. - The Frame Buffer De-Compression (FBD). It presumes this IP will be an in-house IP. - IO interface of the display port: MIPI DSI, DPI, and DBI.	Must have	Yes
'MXRT2660_DIS_2-5	It's imperative for the implementation team to document following details in one of the technical documents (Subsystem Architecture) delivered by the team: - Inter-connection between the modules in the display subsystem, - clock sources and clock frequency for each module, - data flow for each operation mode, i.e video mode, command mode, ULPS state, and display interface (DSI, DPI, DBI).	Must have	Shall become a design phase deliverable
'MXRT2660_DIS_2-6	It's imperative for the implementation team to provide an integration guide with the following details: - IP configuration parameters, - all signals interconnected among the modules of the Display subsystem, and - all signals interfaced to the rest of the SoC.	Must have	Shall become a design phase deliverable
'MXRT2660_DIS_2-7	It's imperative for the implementation team to specify the verification patterns for the whole subsystem for the target operation modes and use cases.	Must have	Shall become part of toplevel verification
'MXRT2660_DIS_2-8	It's imperative for the imp140ubsystem140on team to throughly verify all IP patterns and subsystem patterns.	Must have	Shall become part of toplevel verification
iMXRT2660_DIS_2-9	The display subsystem of this device is designed to support single display panel.	Must have	Yes
iMXRT2660_DIS_2-10	In case the display panel requires LVDS interface, either the parallel display interface or MIPI DSI interface can be used to connect to an external LVDS bridge, which will connect to the LVDS display panel.	Must have	Only with external LVDS driver Open: Req. update ongoing
iMXRT2660_DIS_9-1	Local PWM Timer	Heading	-
iMXRT2660_DIS_9-2	The display subsystem should include a PWM timer for backlight control.	Should have	No, use PWM timer in HSP_SS
iMXRT2660_DIS_10-1	Display vendors	Heading	-
iMXRT2660_DIS_10-2	This processor shall support display panels of following vendors: Matrix Orbital, Sitronix, Ilitek, AU Optronics, Himax	Must have	Rejected, need specific part numbers

6.5.2.1 MIPI Display Serial Interface (DSI)

Clarification item for PDA: It is decided to proceed with Mixel as third-party supplier for MIPI DSI solution. Sofar we have only received IP for evaluation purposes; chip lead to confirm whether no changes are applicable to the product IP version, and related IP documentation is to be provided for both MIPI D-PHY and Host controller.

A.3 MIPI DSI D-PHY

The 22FDX MIPI D-PHY solution from Mixel has been selected for usage in i.MX RT2660. Table 102 shows a high-level overview of the Mixel 22FDX MIPI D-PHY IP with a focus on the DSI/Tx functionality only.

Table 102. High-level overview of Mixel 22FDX MIPI D-PHY DSI IP

Parameter	Mixel
IP name	MXL-DPHY-CSI2-TX
IP macro	Separate Tx- & PLL macros, or single Tx/Rx combo
IP area	Tx+PLL: 0.38 mm ² (including IOs/ESD) Tx/Rx combo: 0.57 mm ² (including IOs/ESD)
Metal stack	10M_2Mx_5Cx_1Jx_2Qx_LB
Power supply	Analog IO: 1.8V ±10% Analog core: 0.8V ±10% PLL: 0.8V ±10%
Temperature range	-40 up to +125°C
Functionality	
Number of lanes	1 clock lane, up to 4 data lanes
Operating modes	High-Speed, Low-Power, Ultra-Low-Power, Power Down
MIPI Specification compliance	D-PHY version 2.1 Backward compatible w/ v1.2
High-speed serializers	Yes
Testability support	Yes (ATE, BIST)
Packaging support	Wirebond & flip-chip
High-Speed mode with 2-lane configuration	
Performance	80Mbps to 1.5Gbps per lane up to 2.5Gbps per lane (w/ Deskeew)
Typical current @2.5Gbps	Tx: 29mA (analog), 0.488mA (IO) PLL: 6.377mA (PLL), 0.702mA (IO)
Low-Power mode with 2-lane configuration	
Performance	10Mbps data rate
Typical current (LP)	0.5mA (analog), 1.7mA (IO)
Typical current (ULP)	PLL: see other modes
Power down mode	
Typical current	78µA (analog), 3µA (IO) PLL: 2.936 µA (PLL), 0.044µA (IO)

Table 103. IC requirements traceability: MIPI D-PHY DSI requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_DIS_6-2	The DSI D-PHY shall meet all requirements listed in the MIPI performance and MIPI DSI interface.	Must have	Yes
iMXRT2660_DIS_6-4	The D-PHY configuration is 2 Tx data lane for DSI interface, with PLL, and IOs.	Must have	Yes
iMXRT2660_DIS_6-5	The D-PHY shall support scalable data lane: 1 or 2 data lanes can be configured.	Must have	Yes
iMXRT2660_DIS_6-6	The D-PHY IP shall include High Speed Serializers.	Must have	Yes
iMXRT2660_DIS_6-7	The D-PHY IP shall include all IO and PWR/GND pads in the PHY macro.	Must have	Yes
iMXRT2660_DIS_6-8	The D-PHY IP shall include all test functions.	Must have	Yes

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_DIS_6-9	The D-PHY shall support High Speed mode and Low Power mode.	Must have	Yes
iMXRT2660_DIS_6-10	The D-PHY shall support High Speed mode up to 2.5Gbps data rate.	Must have	Yes
iMXRT2660_DIS_6-11	The D-PHY shall support 10Mbps data rate in Low Power mode.	Must have	Yes

A.4 DSI Host Controller

The MIPI-DSI Host Controller concerns a 3rd-party IP from Rambus.

Fig 57 shows a functional block diagram of the MIPI DSI Host Controller.

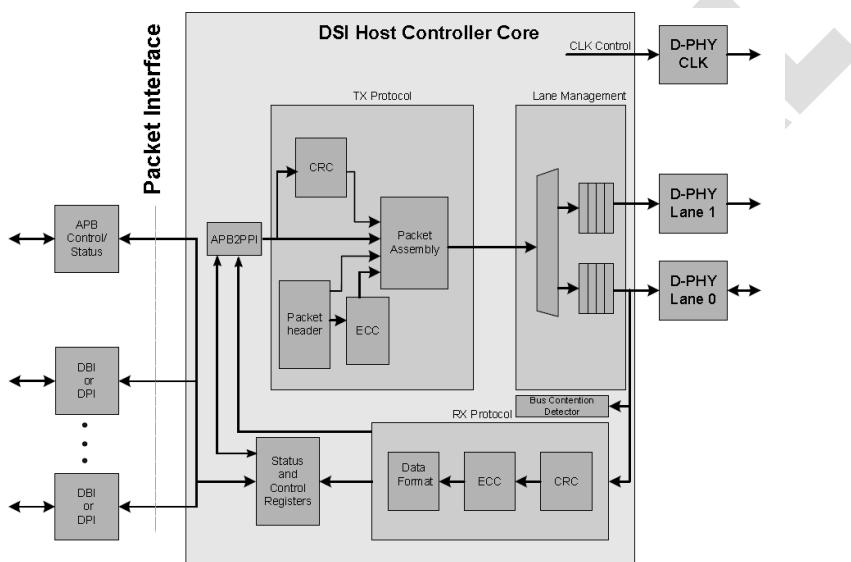


Fig 57. MIPI DSI Host Controller block diagram

The MIPI DSI Host Controller is a flexible, high-performance, and easy-to-use digital core that implements all protocol functions defined in the MIPI_DSI_HOST Specification. The MIPI DSI Host Controller provides an interface that allows communication with MIPI_DSI_HOST-compliant peripherals. Its key features include:

- Implementation of all three DSI Layers (Pixel to Byte packing, Low Level Protocol, Lane Management) ;
- Support for Command and Video Modes ;
- Host and Peripheral version ;
- Scalable data lane support, 1 to 4 Data Lanes:
 - Optional bidirectional support on lane 0 ;
- Supports High Speed (4.5+ Gbit/s) D-PHY operation ;
- Supports High Speed (2.5+ Gsym/s) C-PHY operation ;
- Support for all DSI-2 data types and formats ;
- Virtual Channel support ;
- Supports ULPS mode ;
- Full Low-Level Protocol Error and Contention detection and reporting ;
- Supports continuous and non-continuous Clock Lane operation ;
- Supports multiple packets per transmission ;
- Support for all three Video Mode packet sequences:
 - Non-Burst Mode with Sync Pulses ;
 - Non-Burst Mode with Sync Events ;

- Burst mode ;
- Support for bus turnaround signaling ;
- Flexible packet based user interface:
 - APB interface option (status and control) ;
- Optional multiport interface allows up to 4 interfaces to the DSI-2 ;
- Supports PHY Protocol Interface (PPI) compatible MIPI D-PHYs
 - Delivered fully integrated and verified with target MIPI PHY ;
- MIPI Alliance Specification for Display Serial Interface Version 1.1 compliant.

Table 104. IC requirements traceability: MIPI DSI interface & -controller requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_DIS_3-1	MIPI DSI interface	Heading	-
iMXRT2660_DIS_3-2	This processor shall instantiate a MIPI DSI port.	Must have	Yes
iMXRT2660_DIS_3-3	The MIPI DSI shall have 2 lanes.	Must have	Yes
iMXRT2660_DIS_3-4	The MIPI DSI controller shall be compliant to MIPI standard DSI-2 Version 1.0	Must have	Yes
iMXRT2660_DIS_3-5	The MIPI DSI PHY shall be compliant to MIPI standard D-PHY Version 1.2 up to 2.5Gbps.	Must have	Yes
iMXRT2660_DIS_3-6	The MIPI DSI port shall support Type 3 for Video mode and Type 2 for Command mode.	Must have	Yes
iMXRT2660_DIS_3-7	The display subsystem and the MIPI DSI shall fully support Ultra Low Power State (ULPS).	Must have	Yes
iMXRT2660_DIS_4-1	Parallel Display Interface	Heading	-
iMXRT2660_DIS_4-2	This processor shall implement MIPI DPI interface for parallel display port.	Must have	Ongoing with Rambus
iMXRT2660_DIS_4-3	The MIPI DPI interface shall be compliant to MIPI standard DPI Version 2.0	Must have	Ongoing with Rambus
iMXRT2660_DIS_4-4	This processor shall implement MIPI DBI interface for parallel display port.	Must have	Ongoing with Rambus
iMXRT2660_DIS_4-5	The MIPI DBI interface shall be compliant to MIPI standard DBI Version 2.0	Must have	Ongoing with Rambus
iMXRT2660_DIS_4-6	The MIPI DBI interface shall support Type A and Type B interface.	Must have	Ongoing with Rambus
iMXRT2660_DIS_5-1	MIPI DSI controller	Heading	-
iMXRT2660_DIS_5-2	The DSI controller shall meet all requirements listed in the MIPI performance and MIPI DSI interface.	Must have	Yes
iMXRT2660_DIS_5-4	The DSI controller shall support PHY Protocol Interface (PPI) compatible MIPI D-PHY .	Must have	Yes
iMXRT2660_DIS_5-5	The DSI controller shall support following interface to the display controller: - MIPI DPI-2 - MIPI DBI-2	Must have	Ongoing with Rambus
iMXRT2660_DIS_5-6	The DSI controller shall support scalable data lane: 1 or 2 data lanes can be configured.	Must have	Yes
iMXRT2660_DIS_5-7	The DSI controller shall implement all three DSI layers: - Pixel to Byte packing - Low level protocol - Lane management	Must have	Yes
iMXRT2660_DIS_5-8	The DSI controller shall support High Speed and Low Power operation.	Must have	Yes
iMXRT2660_DIS_5-9	The DSI controller shall support full Low-Level Protocol Error and Contention Detection and reporting error status.	Must have	Yes

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_DIS_5-10	The DSI controller shall support continuous and non-continuous Clock Lane operation.	Must have	Yes
iMXRT2660_DIS_5-11	The DSI controller shall support multiple packets per transmission.	Must have	Yes
iMXRT2660_DIS_5-13	The DSI controller shall support all three Video Mode packet sequences: - Non-Burst Mode with Sync Pulses - Non-Burst Mode with Sync Events - Burst mode	Must have	Yes
iMXRT2660_DIS_5-14	The DSI controller shall support bus turnaround signaling.	Must have	Yes

6.5.2.2 Display Controller Interface (DCIF)

The Display Control Interface (DCIF) is an AXI bus master that fetches graphics stored in memory and displays them on a TFT LCD panel or connects to a display interface depending on the chip configuration. A wide range of panel sizes are supported and the timing of the interface signals is highly configurable. Graphics are read directly from memory and blended in real-time, which allows for dynamic content creation with minimal CPU intervention.

Graphics can be encoded in a variety of formats for optimum memory usage.

Fig 58 shows a high-level functional block diagram of the DCIF module.

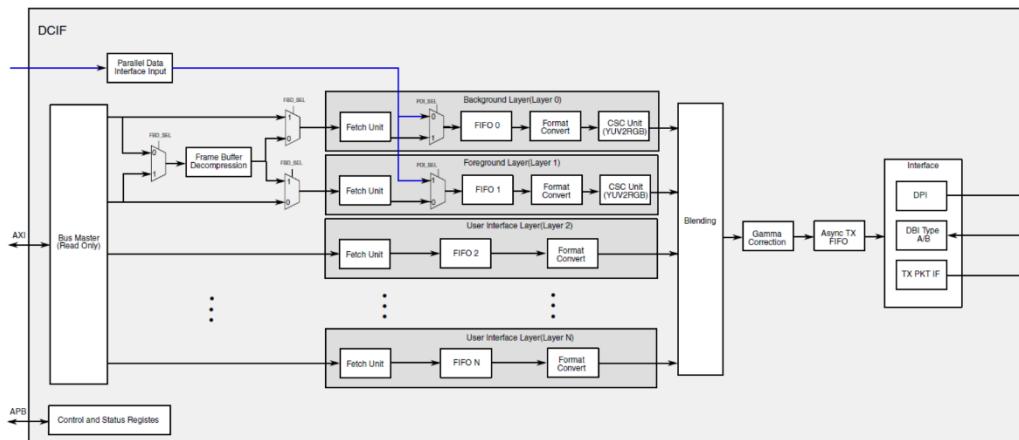


Fig 58. DCIF module block diagram

The DCIF includes the following features:

- Display output interface
 - Display Pixel Interface (DPI) - Parallel RGB
 - Programmable HSYNC, VSYNC, DE and pixel clock polarity ;
 - Display Bus Interface(DBI)
 - TX packet Interface
- Parallel Data Interface(PDI) Input
 - Programmable VSYNC, DE and pixel clock polarity
 - Layer encoding formats:
 - RGB444
 - RGB555
 - RGB565

- RGB666
- RGB888
- YCbCr422
- Display layers can support up to maximum 5 layers of alpha blending:
 - 1 background layer(Layer 0) ;
 - 1 foreground layer(Layer 1) ;
 - 2 user interface layer(Layer 2 ~ Layer 3)
 - A programmable constant color behind the background layer ;
- Each layer supports:
 - Programmable plane size (Width/Height/Pitch) and X/Y offset on the panel ;
 - Programmable background color for plane graphics ;
 - Embedded alpha and global alpha ;
 - Shadowed control registers for configuration ;
 - Layer encoding formats:
 - Index color 1/2/4/8 bpp format;
 - RGB565 ;
 - ARGb1555 ;
 - ARGB4444 ;
 - YCbCr422 or YUV422(only for background layer) ;
 - RGB888 ;
 - ARGB8888 ;
 - ABGR8888 ;
- Support gamma correction with 8-bit resolution on each color component

When corresponding interrupt enable register bit is set, interrupt flags can generate interrupt. The interrupt is de-asserted by clearing either the flag or the interrupt enable register bit. Each interrupt contains such sources as:

- Vertical Blanking Period Start ;
- Underrun ;
- VSYNC Start ;
- Layer n FIFO Empty ;
- Layer n DMA Done ;
- Layer n DMA Error ;
- Layer n FIFO Panic;
- TX Packet Interface Command Done Interrupt ;
- PDI buffer overrun Interrupt
- DBI Command Done Interrupt
- PDI Vsync Timeout Interrupt

Frame Buffer De-compression (FBD) engine is re-used from TinGPU, and needs to be added to the DCIF for reducing SoC integration complexity. **This requires a Change Request of DCIF block.**

The FBD block is used as an internal format between TinGPU and DCIF. It supports RGB888 and ARGB888 pixel formats only, while bypass other formats. The FBD format requires a fixed compression ratio. This allows a compressed image written by the TinGPU to be re-read by the DCIF display, which may require random access to any location within the image.

The lossy compression scheme shall be visually lossless (>40 dB PSNR).

As the TinGPU targets to operate on 8x8 tiles of pixels, the compression scheme shall operate on groups of pixels compatible with that. (examples: 4x4, 8x4, 4x8, 8x8, 8x1, 1x8).

The de-compressed formats shall target 16-32bpp, to complement the GPU's compressed formats ranging from around 8bpp to 16bpp.

Table 105. IC requirements traceability: Display controller requirements

AS/RS identifier	Contents	Classification	Covered
Display controller requirements			
iMXRT2660_DIS_7-3	The Display controller shall meet all requirements listed in the MIPI performance and MIPI DSI interface.	Must have	Yes
iMXRT2660_DIS_7-4	The Display controller shall support following interface to the display controller: - MIPI DPI-2 - MIPI DBI-2 - Optionally Packet interface (only for NW Logic/Rambus IP)	Must have	Yes for MIPI DPI-2 MIPI DBI-2
iMXRT2660_DIS_7-5	The Display controller shall implement any additional sideband signals for the seamless inter-operation with the DSI controller as necessary.	Must have	No sideband supported Open: Req. update ongoing
iMXRT2660_DIS_7-6	- The Display controller shall include a DMA engine to perform data move between internal FIFOs or memory buffers and system memory. - The DMA features and functions, including bus width, burst length, linked list, etc, are sufficiently and efficiently implemented to support the target display performance of this device.	Must have	Yes
iMXRT2660_DIS_7-7	- The Display controller shall implement any additional sideband signals for a seamless inter-operation with the FBD in front of its initiator bus interface.	Must have	Yes
iMXRT2660_DIS_7-8	The Display controller shall support up to 4 layers. Two layers supporting alpha blending is required.	Must have	2-8
iMXRT2660_DIS_7-9	Each layer shall support following encoding format: - Index color 1/2/4/8 bpp format (only for background layer) - RGB565 - ARGB1555 - ARGB4444 - YUV422 (only for background layer and foreground layer) - YUV420 (only for background layer) - YUV444 - RGB888 - ARGB8888 - GBR888 - AGBR8888	Must have	No support yuv420,yuv444,GBR888,ARGB8888 YUV22 can support foreground layer Open: Req. update ongoing
iMXRT2660_DIS_7-10	The Display controller shall support CSC operation.	Must have	Two layer for pdi input only
iMXRT2660_DIS_7-11	The Display controller shall support Format Conversion operation.	Must have	Yes
iMXRT2660_DIS_7-12	The Display controller shall support Alpha Blending operation.	Must have	Yes
iMXRT2660_DIS_7-13	The Display controller shall support Panning in all 4 directions.	Must have	Yes
iMXRT2660_DIS_7-14	The Display controller shall support Gamma correction.	Must have	Yes
iMXRT2660_DIS_7-15	The Display controller shall support a parallel data interface to receive input data directly from the camera subsystem. - The Display controller shall implement any additional sideband signals for a seamless inter-operation with the Camera subsystem.	Must have	Yes via VIDEO MUX
iMXRT2660_DIS_7-16	The Display controller shall support partial frame display for use cases that require memory bandwidth and memory footprint optimization.	Must have	support DBI Open: Req. update ongoing
Frame buffer compression			

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_DIS_8-2	This device shall include a FBC block in front of the Display controller to compress or decompress image.	Must have	Only decompress
iMXRT2660_DIS_8-4	The FBC shall work in conjunction with the Display controller to provide seamless operation on image decompression when a compressed image is read from system memory.	Must have	Yes
iMXRT2660_DIS_8-5	The FBC shall implement any additional sideband signals for a seamless inter-operation with the Display controller.	Must have	Not supported
iMXRT2660_DIS_8-6	Multiple formats The FBC shall support multiples Video and graphics formats - RGB565 - RGB888 - ARGB8888	Must have	RGB565 not supported
iMXRT2660_DIS_8-7	The FBC shall support fixed compression ratio 2:1.	Must have	At least 2:1
iMXRT2660_DIS_8-8	- The FBC shall support both Lossless and Lossy modes. - For Lossy mode, the visually lossless is 40dB PSNR or better.	Must have	Yes
iMXRT2660_DIS_8-9	The FBC shall support different block size; - 16x1 or 32x1 (raster scan) - 8x8 (tile) - 4x4 (tile) - 8x4 (tile)	Must have	Confirmed 32 x 1 Others tbc

6.5.3 Graphics Processing

6.5.3.1 Graphics Processing Unit (GPU)

The TinGPU is a new design that is currently under development by MME's Dig IP team. Hence, it will be deployed into i.MX RT2K products for the first time. This 2.5D GPU IP is intended to provide acceleration for vector and raster graphics as supported via the OpenVG Lite specification version 1.1, supporting the 8 ideal stages of the OpenVG Lite pipeline.

The TinGPU targeted for i.MX RT2660 shall support the following main features.

- Maximum display size of up to 1080p
 - Maximum display rate of up to 30 frames per second ;
 - Maximum pixel size of 24 bits per pixel ;
- Maximum display size of up to 720p
 - Maximum display rate of up to 60 frames per second ;
 - Maximum pixel size of 24 bits per pixel ;
- 1 pixel/clock for clear/fill, blit, stretch, shrink and rotate ;
- Embedded Frame buffer compression (FBC) engine
 - Supports both Lossless and Lossy compression modes
 - Lossy compression scheme shall be visually lossless (>40 dB PSNR).
 - Compression scheme to operate on groups of pixels up to 8x8 tiles of pixels ;
 - 2:1 fixed compression ratio ;
 - Supporting RGB888 and ARGB888 pixel formats, and bypass for others ;

The TinGPU version used for i.MX RT2660 does not require to support texture compression, or anything ASIL-B related.

As first-order estimation, it is expected that the targeted TinGPU version occupies similar silicon area as Verisilicon's GPU.

Table 106. IC requirements traceability: GPU requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_GFX_1-2	This processor shall include a GPU designed for 2.5D for OpenVG vector graphics processing.	Must have	GPU currently does not support VG
iMXRT2660_GFX_1-3	The GPU core shall support OpenVG-Lite1.1 acceleration graphics APIs.	Must have	Yes
iMXRT2660_GFX_2-1	GPU performance	Heading	-
iMXRT2660_GFX_2-2	This processor shall support graphics processing up to 1080p @30fps, 24bpp	Must have	Yes
iMXRT2660_GFX_2-3	This processor shall support graphics processing up to 720p @60fps, 24bpp	Must have	Yes
iMXRT2660_GFX_2-4	The GPU shall operate up to 350MHz.	Must have	Yes
iMXRT2660_GFX_2-4	The GPU shall support graphics processing up to 720p60, 24bpp and 1080p30, 24bpp	Must have	Yes
iMXRT2660_GFX_3-1	Graphics operations	Heading	-
iMXRT2660_GFX_3-2	The GPU shall support drawing primitives, including: - Pixel/Line drawing - Filled rectangles - Triangles - Quadrilaterals	Must have	Yes
iMXRT2660_GFX_3-2	The GPU shall support text rendering: - Bitmap antialiased (A4/A8) - Font Kerning - Unicode	Must have	Yes
iMXRT2660_GFX_3-4	The GPU shall support blending: - Porter-Duff alpha blending - Source/Destination color keying	Must have	Yes
iMXRT2660_GFX_3-5	The GPU shall support following image transformations: - Texture mapping - Point sampling - Biliner filtering - Blitting with antialiased - Rotation any angle - Mirroring - Stretch - Source and/or destination color keying - Format conversions	Must have	Yes
iMXRT2660_GFX_3-6	The GPU shall support following pixel formats: - Any RGB format - L8 (grayscale) - A4 - A8 - YUV422 - YUV420	Must have	Yes
iMXRT2660_GFX_3-7	The GPU shall support partial display rendering to reduce on-chip RAM footprint.	Must have	Yes
iMXRT2660_GFX_4-1	Frame Buffer Compression (FBC)	Heading	-
iMXRT2660_GFX_4-2	The GPU shall include a FBC block to compress or decompress image.	Must have	Yes
iMXRT2660_GFX_4-4	The FBC shall work in conjunction with the FBC in front of the Display controller to provide seamless operation on image decompression when a compressed image is read from system memory.	Must have	Yes

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_GFX_4-5	The FBC shall support fixed compression ratio 2:1.	Must have	Yes
iMXRT2660_GFX_4-6	Compression mode <ul style="list-style-type: none"> - The FBC shall support both Lossless and Lossy modes. - For Lossy mode, the visually lossless is 40dB PSNR or better. 	Must have	Yes

6.5.3.2 JPEG Decoder

The JPEG core is a standalone and high-performance JPEG decoder for still image and video decompression applications. Compliance with the Baseline and the Extended Sequential DCT modes of the ISO/IEC 10918-1 JPEG standard makes the JPEG core suitable for interoperable systems and devices, such as home entertainment devices (set-top boxes, network media players etc.), portable multimedia devices (media players, mobile phones etc.), digital printing devices, medical imaging systems, video conference systems, automotive systems and surveillance systems. The JPEG decoder is based on the JPEG-D-X from ALMA/CAST, and supports still and full motion. It offers the following features:

- Baseline and extended ISO/IEC 10918-1 JPEG compliance
 - Four Huffman tables (2DC and 2AC in maximum) ;
 - Four 8-bit or 16-bit quantization tables (in maximum) ;
 - Four color components (in maximum) ;
 - 8-bit and 12-bit pixels per sample ;
 - All possible scan configurations and JPEG formats for input data ;
 - 8K x 8K image size (in maximum) ;
 - Restart markers ;
- Additional processing capabilities, including motion JPEG payload decoding.

The JPEG decoder contains a wrapper that provides the bus interface and DMA controller for the JPEG decoder. The DMA controller offers DMA channels for bit stream fetching and decoded pixel data storing, as well as a register interface and chained descriptors for frame or bit stream buffer switching. The JPEG decoder wrapper also converts to memory the JPEG decoder core output images in the Micro Block Tile (MBT) format to linear format. The wrapper offers the following additional features:

- DMA engines for fetching the JPEG bit stream from system memory and feeding it to the decoder ;
- DMA engines for storing the decoded pixel data into the system memory ;
- Conversion of the pixel MBT format to linear format ;
- Multi-bit-stream context switch based on frame ;
- Chained DMA or bit stream descriptors for frame or bit stream buffer updates with minimum software interference ;
- Bit stream buffer, half or full, and return features for bit stream buffer management ;
- YUV444, YUV420, YUV422, RGB, ARGB, and Gray formats supported.

The JPEG decoder including wrapper is re-used from i.MX RT700.

The JPEG decoder requires a number of 2-port & single-port register files.

Table 107. **JPEG decoder local memories configuration**

Target	Purpose	Total size	# words	# bits	# instances
2PREG	Bitstream FIFO	512 B	32	128	1
2PREG	IDCT transpose memory	144 B	64	18	1
2PREG	Pixel output buffer	1.5 KB	96	128	1

2PREG	JPEG_D_SFIFO memory	128 B	128	8	1
2PREG	IDCT Buffer memory	240 B	128	15	1
2PREG	HUFMAN_D_SFIFO memory	864 B	256	27	1
SP-REG	JPEG_D_DQT memory	512 B	256	16	1
SP-REG	HUFMAN_D_TABLES memory	512 B	512	8	1

Concerning the performance target of the JPEG decoder for decompression of a 720p frame:

- One component per cycle, where RGB888 (24-bit) means 3 components ;
- For a 720p frame, the decompression requires $1280 \times 720 \times 3 = 2,764,800$ clock cycles.

As there are 17.5 MCycles when operating at a 350MHz clock, the JPEG decoder shall be able to achieve the required performance level only ~2.8M Cycles are required.

Table 108. IC requirements traceability: JPEG decoder requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_IMG_1-3	This processor shall include a JPEG Decoder to perform decompression of still image and video applications.	Must have	Yes
iMXRT2660_IMG_1-4	The JPEG Decoder shall support <ul style="list-style-type: none"> - decoding standard-compliant baseline and extended JPEG streams - decompressing video payload of standard motion JPEG container formats. 	Must have	IP supports Same as on RT700
iMXRT2660_IMG_1-5	The JPEG Decoder shall support up to 1080p frame resolution	Must have	Yes
iMXRT2660_IMG_1-6	The JPEG Decoder shall support following pixel formats <ul style="list-style-type: none"> - YUV444 - YUV422 - YUV420 - All RGB - All ARGB - Gray 	Must have	IP supports Same as on RT700
iMXRT2660_IMG_1-7	The JPEG Decoder shall support output packed format YUV where Y, U (Cb) and V (Cr) samples are packed together into macropixels which are stored in a single array. This pixel format would be more efficient for memory bus with relatively high overhead, like pSRAM.	Must have	Rejected, not supported by the 3PIP Open: Req. update ongoing
iMXRT2660_IMG_1-8	The JPEG Decoder shall support for the planar formats where each component is stored as a separate array.	Should have	Rejected, not supported by the 3PIP Open: Req. update ongoing
iMXRT2660_IMG_1-9	The JPEG Decoder must be capable to decompress a 720p frame within 50ms.	Must have	Yes

6.5.4 Bus system

The ARM NIC-400 IP is the interconnect fabric of the MEDIA_SS, referred to as NIC_MEDIA. It runs at an operating frequency of up to 350 MHz in Normal Run mode. NIC_MEDIA maintains a 1:1 clock-synchronous relationship with its building blocks, and is configured as 64-bit bus fabric.

The following NIC_MEDIA configuration shall be supported:

- Hierarchical clock gating enabled ;
- Quality of Service feature enabled ;
- Arbitration shall be programmable ;
- ‘Single Slave per ID’ as Cyclic Dependency Avoidance Scheme (CDAS) ;

Table 109 lists the NIC_MEDIA path connectivity between ASIB and AMIB ports.

Table 109. Path connectivity of NIC_MEDIA bus fabric

ASIB port	AMIB port
CAM_AXIM0	X
CAM_AXIM1	X
CAM_AXIM2	X
DSI_AXIM	X
GPU_AXIM	X
JPG_AXIM	X
GPV	

'X' indicates a connection, while '-' indicates no connection

Note that all input- and output ports shall be configured as clock synchronous 1:1 or clock asynchronous, depending on port type.

Table 110. Interface configuration of NIC_MEDIA

Specification	Ports	s_c_0	s_c_1	s_c_2	s_c_3	s_c_4	s_c_5	s_c_6	m_c_0
ClockDomain	Hookup	CAM_AXIMO	CAM_AXIMO	CAM_AXIMO	DIS_AXIM	GPU_AXIM	JPG_AXIM	GPV	MEDIA2MAIN
	HierarchicalClockGating	yes	yes						
	UppercaseRTLSignals	true	true						
	QoSEnabled	true	true						
	QVNEnabled	No	No						
	AWUSERWidth	13	13	13	13	13	13	13	13
	ARUSERWidth	13	13	13	13	13	13	13	13
	WUSERWidth	0	0	0	0	0	0	0	0
	BUSERWidth	0	0	0	0	0	0	0	0
	RUSERWidth	0	0	0	0	0	0	0	0
LocalGroup	Name	media	media	media	media	media	media	gpv	media
	Frequency	350M	350M						
	Name	grp0	grp0						
	ClockRef	media	media						
	Protocol	AXI3	AXI3	AXI3	AXI3	AXI3	AXI3	AHBLiteTarget	AXI4
	AddressWidth	32	32	32	32	32	32	32	32
	DataWidth	128	128	128	128	64	128	32	64
	ARUSEREnabled	true	true						
	AWUSEREnabled	true	true						
	VIDWidth	8	8	8	8	4	8	NA	NA
Interface	TrustZoneSlave	per_access_secure	non_secure						
	ReadIssuing/ReadAcceptance	8	8	8	8	8	16	1	8
	WriteIssuing/WriteAcceptance	8	8	8	8	8	16	1	8
	TotalIssuing	NA	8						
	IDWidthReduction	NA	true						
	OutputSignals	NA	true						
	QoSType	programmable	programmable	programmable	programmable	programmable	programmable	fixed	NA
	Advanced	Prog.GPV	Prog.GPV	Prog.GPV	Prog.GPV	Prog.GPV	Prog.GPV	Config Port	Prog.GPV
	CDAS	slave_per_id	slave_per_id	slave_per_id	slave_per_id	slave_per_id	slave_per_id	single_slave	NA
	TransactionRateRegulation	true	NA						
Fifo	OutstandingTransactionRegulation	true	NA						
	LatencyPeriodRegulation	true	NA						
	BrokenBursts	NA	NA	NA	NA	NA	NA	true	NA
	ar fifo	0	0	0	0	0	0	0	0
	aw fifo	0	0	0	0	0	0	0	0
Fifo	r fifo	0	0	0	0	0	0	0	0
	w fifo	0	0	0	0	0	0	0	0
	b fifo	0	0	0	0	0	0	0	0

6.5.5 Frequency Measure Unit (FREQME)

The main purpose of the FREQME unit to measure the frequency of the IP functional clocks and - bus clocks. Refer to Section 6.2.7 for a brief description about the FREQME unit

The MEDIA_SS includes one FREQME unit one to monitor the MODCON_MEDIA clock outputs (MEDIA.FREQME). Please refer to the RT2660_Clock_v<version>.xlsx in share point [Clock](#) for detailed assignment.

6.6 AUDIO-VISUAL Domain: AUDIO Sub-System (AUDIO_SS)

The AUDIO subsystem of i.MX RT2660 is part of the AUDIO-VISUAL domain. For i.MX RT2660, a strategy is followed to mainly make use of existing audio peripherals that have been deployed into previous i.MX RT products. It mainly concerns inclusion of audio input and -output functionalities, as there is no requirement for a dedicated audio DSP processor like Cadence's HiFi DSP. This makes the audio subsystem relatively light. For i.MX RT2660, the audio processing is envisioned to be performed by the ARM Cortex-M85 processor, optionally complemented by audio-related ML inference tasks processed by NXP Neutron NPU.

The AUDIO_SS bus fabric, bus interfaces and related infrastructure can run at an operating frequency of up to 200MHz (via sys_rootclk) or up to 196.608MHz/180.634MHz (via audio_rootclk as n x Fs multiples) as provided by the CGU. The AUDIO_SS maintains an asynchronous clock-

relationship with the rest of the SoC. Its architectural block diagram is shown in Fig 59. The AUDIO subsystem of i.MX RT2660 is a subset of the XEA-1 platform version.

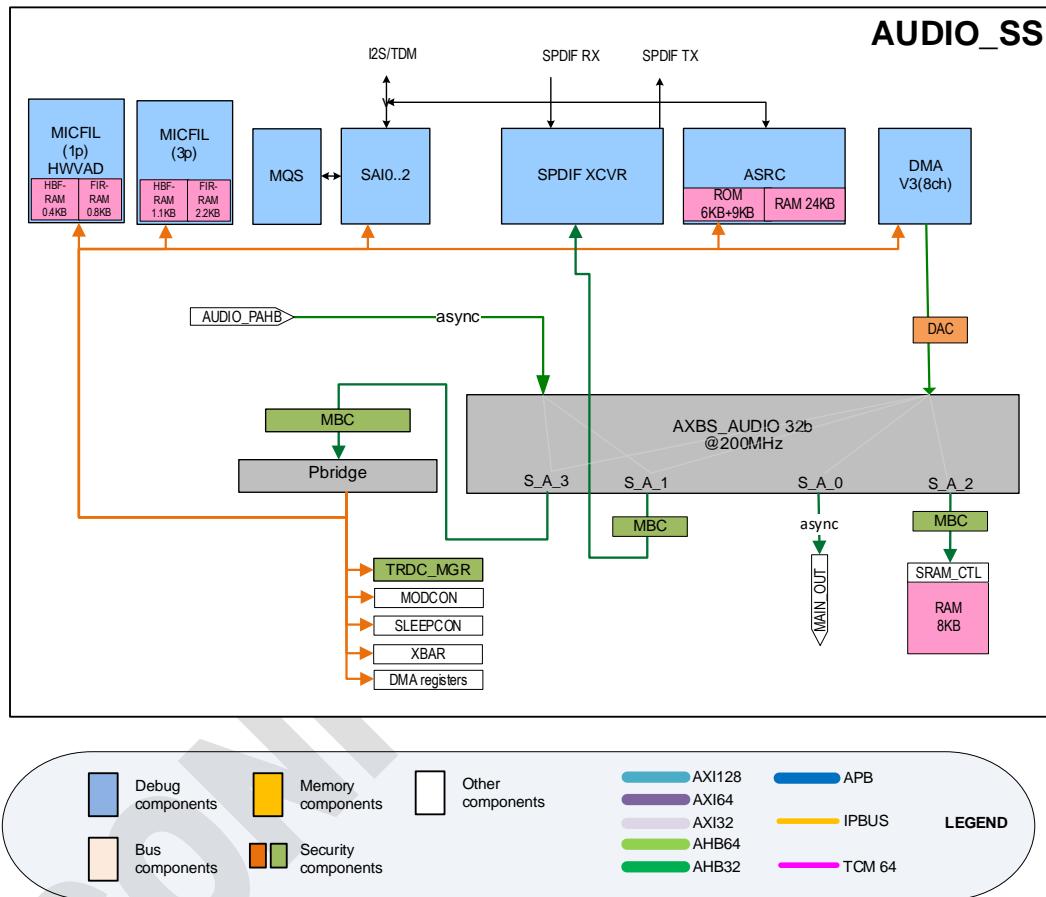


Fig 59. Architectural block diagram of i.MX RT2660's AUDIO_SS [6]

For more detailed information, please refer to the **AUDIO_SS HW.AS document** [6]

This document includes the **RT2660 specific IP configurations**.

Table 111. IC requirements traceability: Audio subsystem requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_AUD_6-2	This device shall include one digital microphone (MICFIL) instance in the Audio subsystem.	Must have	Yes
iMXRT2660_AUD_1-3	This processor shall include 3x I2S ports.	Must have	Yes

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_AUD_3-2	This processor shall include 1x S/PDIF module.	Must have	Yes
iMXRT2660_AUD_3-2	This processor shall include 1x MQS module.	Must have	Yes
iMXRT2660_AUD_4-2	This processor shall include 1x Audio Sample Rate Conversion (ASRC) module.	Must have	Yes
iMXRT2660_SCI_2-5	Another small DMA, with 8 channels or fewer, shall perform DMA transfers between audio peripherals and memory with minimum intervention from the CPU.	Must have	Yes
iMXRT2154ubsystem8-2	The audio subsystem shall fully support WM8960 audio codec.	Must have	Yes

6.6.1 Digital Microphone (DMIC)

The Digital Microphone (DMIC) is also referred to as Microphone Interface (MICFIL) IP. The MICFIL IP delivers audio from digital microphones to the CPU and/or NPU.

Today's digital audio systems use a multi-bit pulse-code modulation (PCM) signal to represent the audio signal. The MICFIL IP implements the required digital interface (a series of filters) to transform a pulse density modulation (PDM) coded microphone bitstream into a 24-bit pulse-code modulation (PCM) signal in the audio band, at a configurable output sampling rate.

Fig 60 shows the high-level functional block diagram of the MICFIL IP.

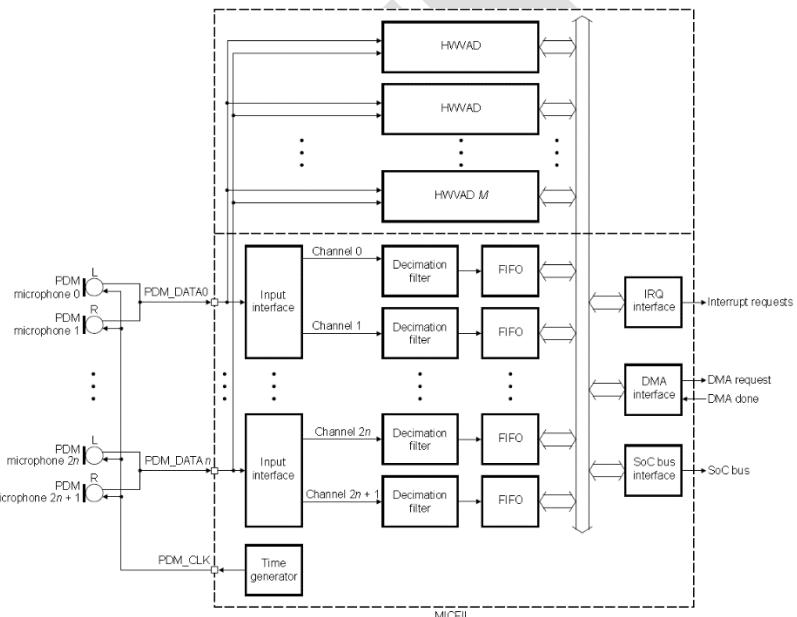


Fig 60. Microphone Interface (MICFIL) IP functional block diagram

The MICFIL used in i.MX RT2660 is configured to support the following main features:

- Support for 8 channels (4 pairs) ;
- Decimation filters:
 - Fixed-point filtering ;
 - 24-bit PCM audio output ;
 - Internal clock divider for a programmable PDM clock generation: clock divider ; bypass capability for low-frequency operations ;
 - Frame synchronization ;
 - Full or partial set of channel operations with individual enable controls ;

- Programmable decimation rate ;
- Programmable DC remover at output ;
- Range adjustment capability ;
- FIFOs with interrupt and DMA capability
 - Each FIFO having a length of 8 entries ;
- Hardware Voice Activity Detector (HWVAD), equipped with:
 - Interrupt capability ;
 - Zero-Crossing Detection (ZCD) option.

The i.MX RT2660 includes two instantiations of the MICFIL IP. The first MICFIL IP includes two microphone channels and implements the Hardware Voice Activity Detector (HWVAD) shall be utilized as wake-up source when the SoC is operating in ‘Deep Sleep’ mode. This requires placement of the HWVAD logic in an always-on domain – while the remaining part of the MICFIL IP can be power gated. The second MICFIL IP includes the remaining six microphone channels, and does not support the HWVAD, hence no power domain separation like the first MICFIL.

More detailed information of the MICFIL IP can be found in its block guide [42].

Table 112. IC requirements traceability: Digital Microphone requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_AUD_6-3	The MICFIL shall support 4 input lines with 2 channels per line.	Must have	Yes, distributed over 2 MICFIL IP [6]
iMXRT2660_AUD_6-4	Each MICFIL channel can be individually enabled or disabled.	Must have	Yes [6]
iMXRT2660_AUD_6-5	The MICFIL shall operate asynchronously down to Deep Sleep mode.	Must have	Yes [6]

6.6.2 Synchronous Audio Interface (SAI)

The SAI IP provides an interface that supports full-duplex serial digital audio interfaces with frame synchronization formats such as I2S, AC97, TDM, and Codec/DSP interfaces. Fig 61 shows a high-level block diagram of the different functions of the SAI IP. It comprises of an input audio path (Rx path) and an output audio data path (Tx path).

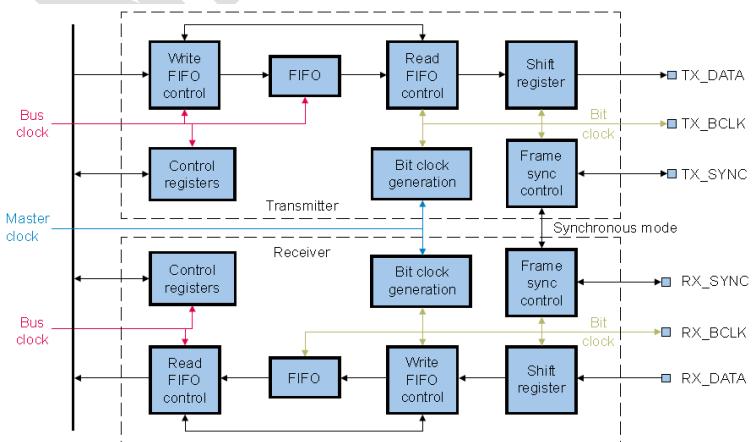


Fig 61. Synchronous Audio Interface (SAI) IP functional block diagram

The SAI IP supports the following main features:

- Transmitter with independent bit clock and frame sync supporting 1 data line ;

- Receiver with independent bit clock and frame sync supporting 1 data line ;
- Each data line supports a maximum frame size of 32 words ;
- Word length of 8 to 32 bits ;
- Word length configured separately for the first word and remaining words in a frame ;
- Asynchronous 8×32 -bit FIFO for each transmit and receive data line supports:
 - Graceful restart after FIFO error ;
 - Automatic restart after FIFO error without software intervention ;
 - 8- and 16-bit data packing into each 32-bit FIFO word ;
 - Independent 32-bit timestamp counters and bit counters for monitoring transmit and receive progress.

More detailed information of the SAI IP can be found in its block guide [43].

Table 113. IC requirements traceability: I2S port requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_AUD_1-4	2x I2S ports shall support 2 lanes.	Must have	Yes, SAI[1-2]
iMXRT2660_AUD_1-5	1x I2S port shall support 4 lanes.	Must have	Yes, SAI0
iMXRT2660_AUD_1-6	All I2S modules shall support 32-bit timestamp counter.	Must have	Yes, [6]

6.6.3 Sony/Philips Digital Interface (SPDIF)

The i.MX RT2660 re-uses of the SPDIF XCVR module of the i.MX95. This module is based on the version that is utilized in the eARC IP and supports SPDIF TX and RX functions in full duplex mode. It supports the following sample rates:

- SPDIF Receiver supporting for 32kHz - 192kHz sample rate ;
- SPDIF Transmitter supporting for 32kHz - 192kHz data tx rate ;

The SPDIF IP supports the following data formats:

Table 114. SPDIF supported data formats

Type	Channels	Payload Size	Frame Format
2-ch LPCM	2	16, 20 or 24	IEC60958
IEC61937	N/A	16	

Fig 62 shows a high-level block diagram of the different functions of the SPDIF XCVR IP.

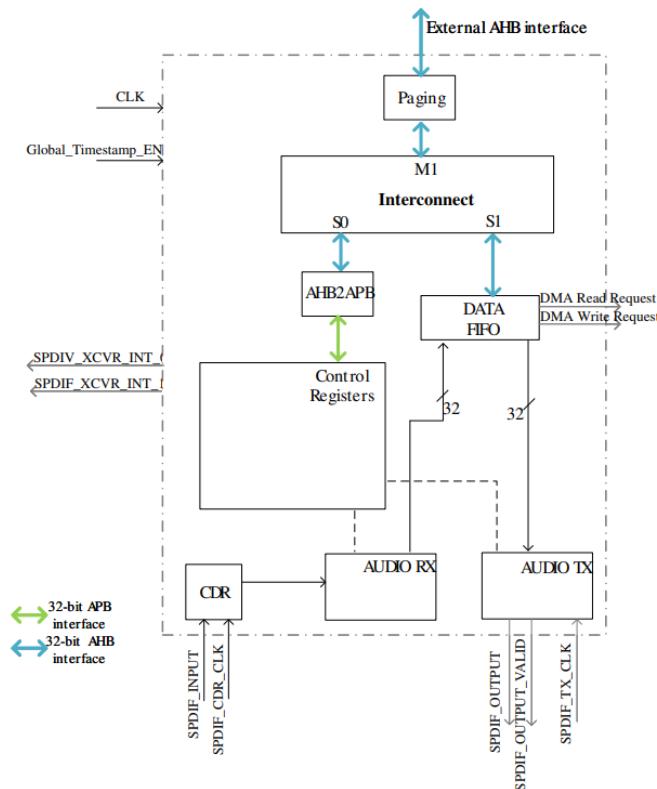


Fig 62. SPDIF XCVR IP functional block diagram

Table 115. IC requirements traceability: SPDIF IP requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_AUD_3-3	The new design used first in i.MX93 should be used, instead of the legacy S/PDIF version.	Must have	Yes, from i.MX95
iMXRT2660_AUD_3-4	The SPDIF Rx function should be multiplexed on at least two physical options that do not conflict with other audio pins.	Must have	Yes

6.6.4 Medium Quality Sound (MQS)

The medium quality audio (MQS) IP is used to generate medium quality audio via a standard GPIO in the pinmux, allowing the user to connect stereo speakers or headphones to a power amplifier without an additional external DAC chip.

Fig 63 shows the high-level functional block diagram of the MQS IP.

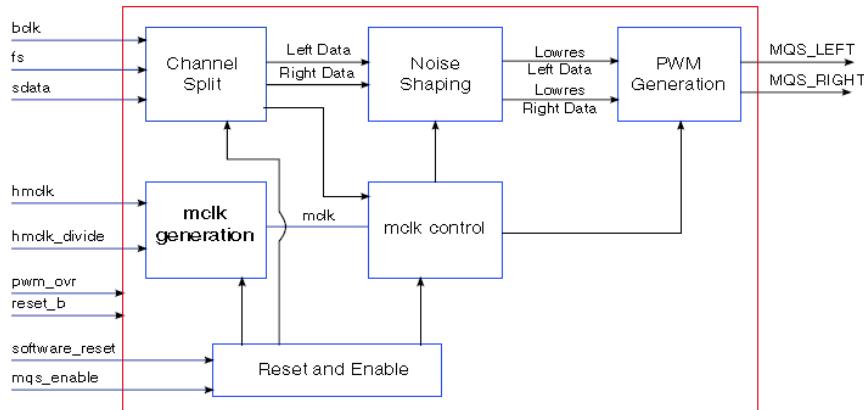


Fig 63. Medium Quality Sound (MQS) IP functional block diagram

The MQS IP contains the following sub-modules:

- Channel Split: Splits the I²S signals into separate left- and right channel audio data ;
- Noise Shaping: Uses the sigma-delta algorithm to generate low-resolution, very high sampling audio, while the audio sampling rate is increased ;
- PWM Generation: Generates the bit stream to the GPIO, which is then used to drive the amplifier and then to drive the external speakers or headphones ;
- Mclk Generation: Used to generate the master clock (mclk). The frequency of mclk is determined by the final bit duration of PWM generation module ;
- Mclk Control: Used as a metronome to co-ordinate the different functional blocks working synchronously ;
- Reset and Enable: Used to generate the reset and enable logic to different clock domains.

The MQS accepts 2-channel LSB-valid 16-bit, MSB shift-out first; frame sync asserting with the first bit of the frame, data shifted with the posedge of bit clock, 44.1kHz or 48kHz signals from SAI in left_justified format; and it provides the SNR target as no more than 20dB for the signals below 10kHz. The signals above 10kHz have worse THD+N values.

MQS provides only simple audio reproduction. No internal pop, click or distortion artifact reduction methods are provided.

This IP has no programming model of its own (other than a few register bits that must be allocated and provided from other general-purpose registers), as it taps the audio output from the SAI0 instance in i.MX RT2660.

6.6.5 Asynchronous Sample Rate Converter (ASRC)

The Asynchronous Sample Rate Converter (ASRC) converts the sampling rate of a signal associated with an input clock into a signal associated with a different output clock. The ASRC supports concurrent sample rate conversion of up to 10 channels of about -120dB THD+N. The ASRC supports up to three sampling rate pairs.

The incoming audio data to this SoC may be received from various sources at different sampling rates. The outgoing audio data of this SoC may have different sampling rates and it can also be associated with output clocks that are asynchronous to the input clocks.

The ASRC is implemented as a co-processor in hardware, with minimal ARM Cortex-M85 processor intervention required. The ASRC Filter Processor (FP) handles the main signal processing algorithm. It has its own simplified instructions. The FP resources (MIPS, RAM, ROM, ALU etc) are shared among the different conversion pairs.

Fig 64 shows the high-level functional block diagram of the ASRC IP.

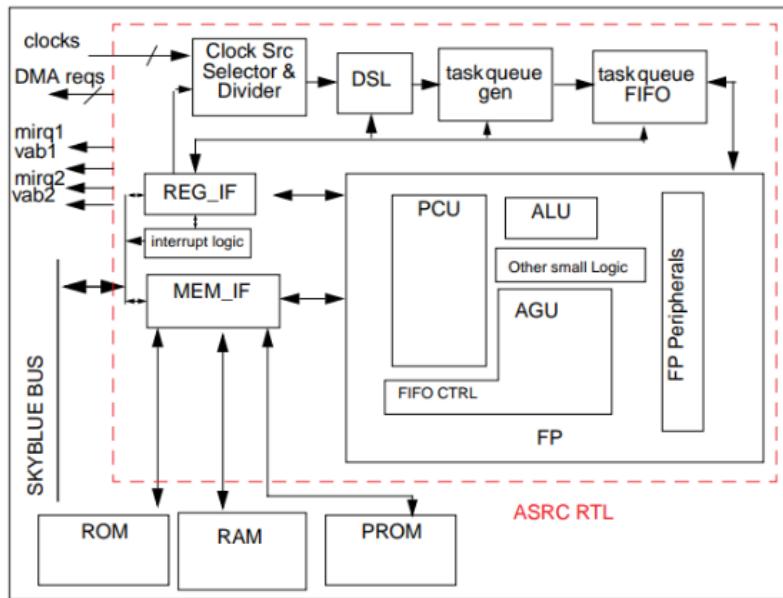


Fig 64. Asynchronous Sample Rate Converter (ASRC) IP functional block diagram

The main features of the ASRC are listed below:

- Any number (0-10) of contiguous channels can be associated to one of the sampling rate pairs ;
- Support user-programmable threshold for the input/output FIFOs ;
- Support flexible 8/16/24-bit width of input data, and 16/24-bit width of output data ;
- Designed for rate conversion between 32 kHz, 44.1 kHz, 48 kHz, 96 kHz, and 192 kHz. The useful signal bandwidth is below 24 kHz ;
- Other input sampling rates in the range of 8 kHz to 200 kHz are also supported¹ ;
- Other output sampling rates in the range of 30 kHz to 200 kHz are also supported¹ ;
- The limitation is the supported ratio (F_{sin}/F_{sout}) range (between 1/24 to 8) ;
- Automatic accommodation to slow variations in the incoming and outgoing sampling rates;
- Linear phase ;
- Tolerant to sample clock jitter ;
- Designed for real-time streaming audio usage. The output sampling clock must be always physically available in the system.

More detailed information of the ASRC IP can be found in its block guide [44].

Table 116. IC requirements traceability: ASRC IP requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_AUD_4-3	The ASRC shall support input clock measurement using timestamps from I2S module.	Must have	Yes, see Fig 87
iMXRT2660_AUD_4-4	The ASRC shall support input clock measurement using timestamps from external audio transceiver.	Must have	Yes, see Fig 87
iMXRT2660_AUD_4-5	The ASRC shall support software based input clock measurement.	Must have	Yes
iMXRT2660_AUD_4-6	The ASRC shall support 16-bit and 32-bit data format for both integer and floating data types	Must have	Yes

1. The ASRC designed input and output sampling rate are between 44.1 kHz, 32 kHz, 48 kHz, 96 kHz, and 192kHz. Useful signal bandwidth is below 24 kHz.

6.6.6 Frequency Measure Unit (FREQME)

The main purpose of the FREQME unit to measure the frequency of the IP functional clocks and - bus clocks. Refer to Section 6.2.7 for a brief description about the FREQME unit

The AUDIO_SS includes one FREQME unit one to monitor the MODCON_AUDIO clock outputs (AUDIO.FREQME). Please refer to the RT2660_Clock_v<version>.xlsx in share point [Clock](#) for detailed assignment.

6.6.7 DMA controller

The AUDIO_SS of i.MX RT2660 includes a 8-channel eDMA3 engine, which is capable of performing complex data transfers with minimal intervention from a host processor.

Refer to Section 6.3.6.2 for a high-level functional overview of eDMA3 controller.

6.6.8 Cross-Trigger network

The i.MX RT2660 AUDIO_SS has one XBAR instance: XBAR0. The purpose of this XBAR is to reduce the amount of AUDIO_SS trigger outputs towards the other i.Mx RT2660 subsystems. The AUDIO_SS XBAR configuration is shown in Table 117 and Fig 65, respectively.

Table 117. i.MX RT2660 AUDIO_SS XBAR instance configuration

Instance	Number of inputs (N)	Number of outputs (M)	Number of outputs with control function (P)	Select registers	Control registers
XBAR0	25	9	0	XBAR0.SELO	n/a

Note: The AUDIO_SS XBAR configuration might change according to definition change, please reference to i.MXRT2660_XBAR_v<version>.xlsx in share point [Interrupts_DMA_CrossTrigger](#) for latest update (if any).

Fig 65 shows a high-level block diagram of the AUDIO_SS cross-trigger network.

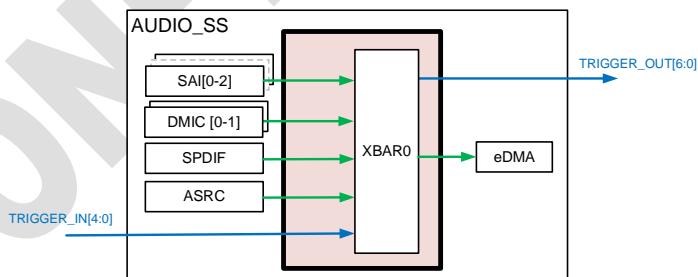


Fig 65. i.MX RT2660 AUDIO_SS cross-trigger network block diagram

Please refer to Section 6.3.8.2 for an overview on how the AUDIO_SS cross-trigger network shall be interconnected with the remainder of the SoC.

The i.MX RT2660 detailed Cross-Trigger Network assignments in a machine-readable format can be found at the following location: [XEA1_XbarMap.xlsx](#)

Please refer to the AUDIO_SS HW.AS document for a detailed AUDIO_SS trigger assignments [6].

6.7 COMMON Domain: Wake Sub-System (WAKE_SS)

The Wake sub-system (WAKE_SS) of i.MX RT2660 is a low-power section including low-power peripherals and -interfaces. UHVT cell shall be used to implement WAKE_SS. UHVT cell works in 0.8V, SoC need to add power switch between VDD_CORE and VDD_0V8. It runs at an operating frequency of up to 50 MHz. Its architectural block diagram is shown in Fig 66.

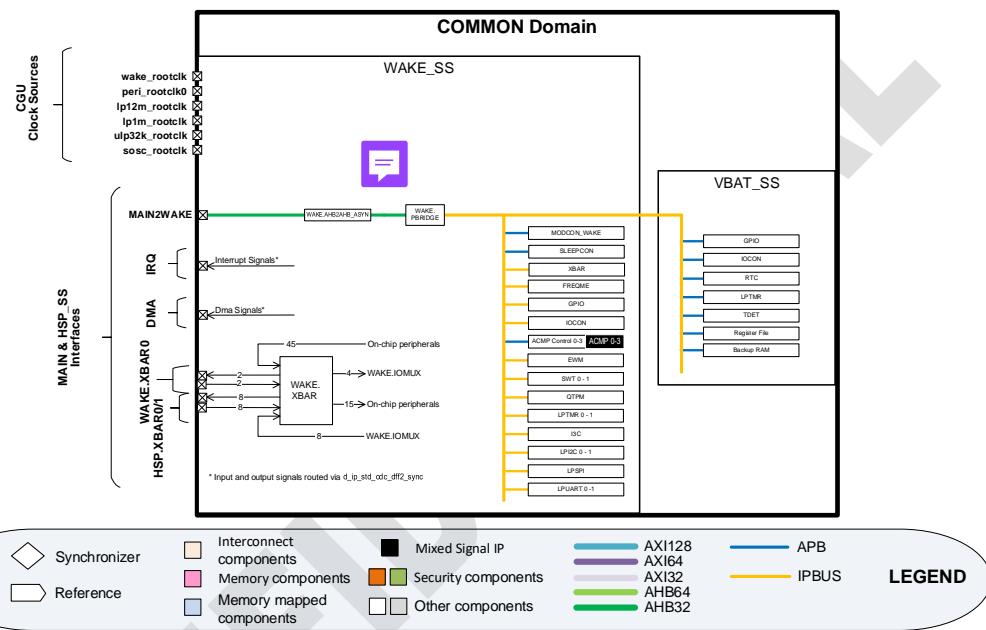


Fig 66. Architectural block diagram of i.MX RT2660's WAKE_SS [8]

For more detailed information, please refer to the WAKE_SS HW.AS document [8]

This document includes the RT2660 specific IP configurations.

6.7.1LPUART

The i.MX RT2660 contains eight LPUART modules in total, of which two reside in the WAKE_SS.

A functional description of the LPUART can be found in Section 6.3.7.2.

6.7.2LPSPI

The i.MX RT2660 contains six LPSPI modules in total, of which one resides in the WAKE_SS.

A functional description of the LPSPI can be found in Section 6.3.7.3.

6.7.3LPI2C

The i.MX RT2660 contains four LPI2C modules in total, of which two resides in the WAKE_SS.

A functional description of the LPI2C can be found in Section 6.3.7.4.

6.7.4I3C

The i.MX RT2660 contains two I3C modules in total, of which one resides in the WAKE_SS.

A functional description of the I3C can be found in Section 6.3.7.5.

6.7.5QTPM

The i.MX RT2660 contains four QTPM modules in total, of which one resides in the WAKE_SS.

A functional description of the QTPM can be found in Section 6.3.7.8.

6.7.6Low Power Timer (LPTMR)

The i.MX RT2660 contains two Low-Power Timer (LPTMR) modules.

The LPTMR module can be configured to operate as a time counter with optional prescaler, or as a pulse counter with optional glitch filter, across all power modes, including the low-leakage modes. It can also continue operating through most system reset events, allowing it to be used as a time of day counter.

The features of the LPTMR module include:

- 16-bit time counter or pulse counter with compare ;
- Optional interrupt can generate asynchronous wakeup from any low-power mode ;
- Hardware trigger output ;
- Counter supports free-running mode or reset on compare ;
- Configurable clock source for prescaler/glitch filter ;
- Configurable input source for pulse counter ;
- Rising-edge or falling-edge 

More detailed information on the LPTMR module can be found in its block guide [45].

Table 118. IC requirements traceability: Low Power Timer requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_TMR_3-3	This processor should include 2x instances of LPTMR in the Low Power subsystem.	Must have	Yes

6.7.7Software Watchdog Timer (SWT)

The Software Watchdog Timer (SWT) is a peripheral module that can prevent system lockup in situations such as software getting trapped in a loop or if a bus transaction fails to terminate. When enabled, the SWT requires periodic execution of a watchdog servicing operation. The servicing operation resets the timer to a specified time-out period. If this servicing action does not occur before the timer expires the SWT generates an interrupt or hardware reset. The SWT can be configured to generate a reset or interrupt on an initial time-out. A reset is always generated on a second consecutive time-out.

The i.MX RT2660 contains two SWT modules that are associated to the ARM Cortex-M85 core. One is intended as overwatch of the Non-Secure operations and the other one for the Secure operations.

Fig 67 shows a functional block diagram of the SWT module.

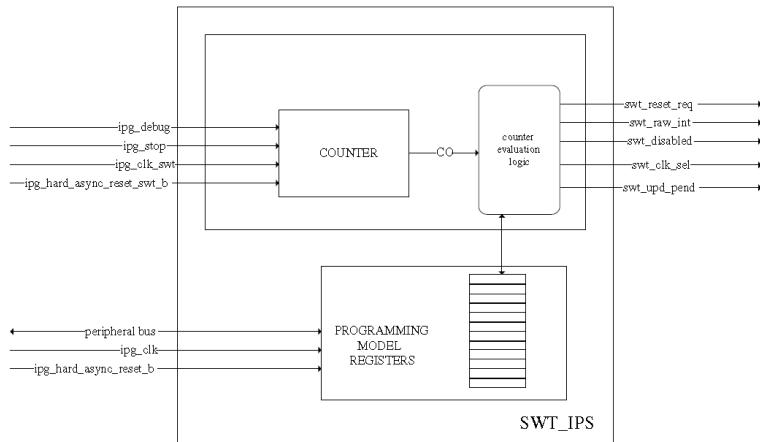


Fig 67. Software Watchdog Timer (SWT) functional block diagram

The SWT has the following features:

- 32-bit time-out register to set the time-out period ;
- Programmable selection of system or oscillator clock for timer operation ;
- Programmable selection of window mode or regular servicing ;
- Programmable selection of reset or interrupt on an initial time-out ;
- Programmable selection of the servicing mode ;
- Master access protection ;
- Hard and soft configuration lock bits.

More detailed information on the SWT module can be found in its block guide.

Table 119. IC requirements traceability: Watchdog Timer requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_TMR_7-3	This processor shall include 2x instances of WDOG, one for secure software and the other for non-secure software.	Must have	Yes, 2xSWT
iMXRT2660_TMR_7-4	WDOG reset should be treated as non-fatal Warm reset. The warning interrupt from WDOG should be an interrupt source to the main CPU interrupt controller.	Must have	Targeted

6.7.8 External Watchdog Monitor (EWM)

For safety, a redundant watchdog system, External Watchdog Monitor (EWM), is designed to monitor external circuits, as well as the MCU software flow. This provides a back-up mechanism to the internal watchdog that resets the MCU's CPU and peripherals.

The i.MX RT2660 makes use of one EWM module. This watchdog is generally used to monitor the flow and execution of embedded software within an MCU. The watchdog consists of a counter that if allowed to overflow, forces an internal reset (asynchronous) to all on-chip peripherals and optionally asserts a reset pin to external devices/circuits. The overflow of the watchdog counter must not occur if the software code works well and services the watchdog to re-start the actual counter. Fig 68 shows the EWM functional block diagram.

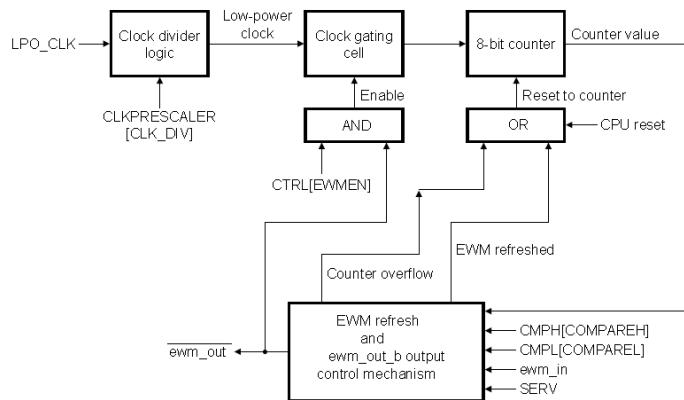


Fig 68. EWM module block diagram

From application perspective, the EWM differs from the internal watchdog in that it does not reset the Cortex-M85 and its peripherals. The EWM provides an independent EWM_OUT_b signal that when asserted resets or places an external circuit into a safe mode. The EWM_OUT_b signal is asserted upon the EWM counter time-out. An optional external input EWM_in is provided to allow additional control of the assertion of EWM_OUT_b signal.

More detailed information on the EWM module can be found in its block guide.

Table 120. IC requirements traceability: External Watchdog Timer requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_TMR_8-4	The EWM_OUT_b pin should be multiplexed on at least 3 GPIO locations. This signal can be used to reset or place an external circuit into a safe mode when EWM counter is overflowed.	Must have	Yes

6.7.9GPIO

Refer to Section 6.3.7.16 for a functional description of the GPIO.

6.7.10IOCON

Refer to Section 6.3.8.1 for a functional description on the IO multiplexing.

6.7.11Analog Comparator

The i.MX RT2660 includes four analog comparator (ACMP) modules. Each ACMP provides a circuit to compare two analog input voltages. The comparator circuit operates across the full range of the supply voltage, known as rail-to-rail operation.

The ACMP inputs are connected to multiplexer to select an analog input signal from eight channels. Six out of eight channels supporting input signals across the full range of the supply voltage (1.8V-3.3V typ.); the other two channels support up to 1.8V typ. input signals.

The ACMP includes a 8-bit DAC that provides a selectable voltage reference for applications requiring a voltage reference. It divides the DAC reference voltage into 256 voltage levels; one can select two different reference voltages: VREFP (1.8V) or VDDA_1V8 (1.8V).

The ACMP can operate in two modes: a Low Power mode optimized in ICC and a High Speed mode optimized for fast comparison.

Fig 69 shows a high-level functional block diagram of the ACMP analog portion.

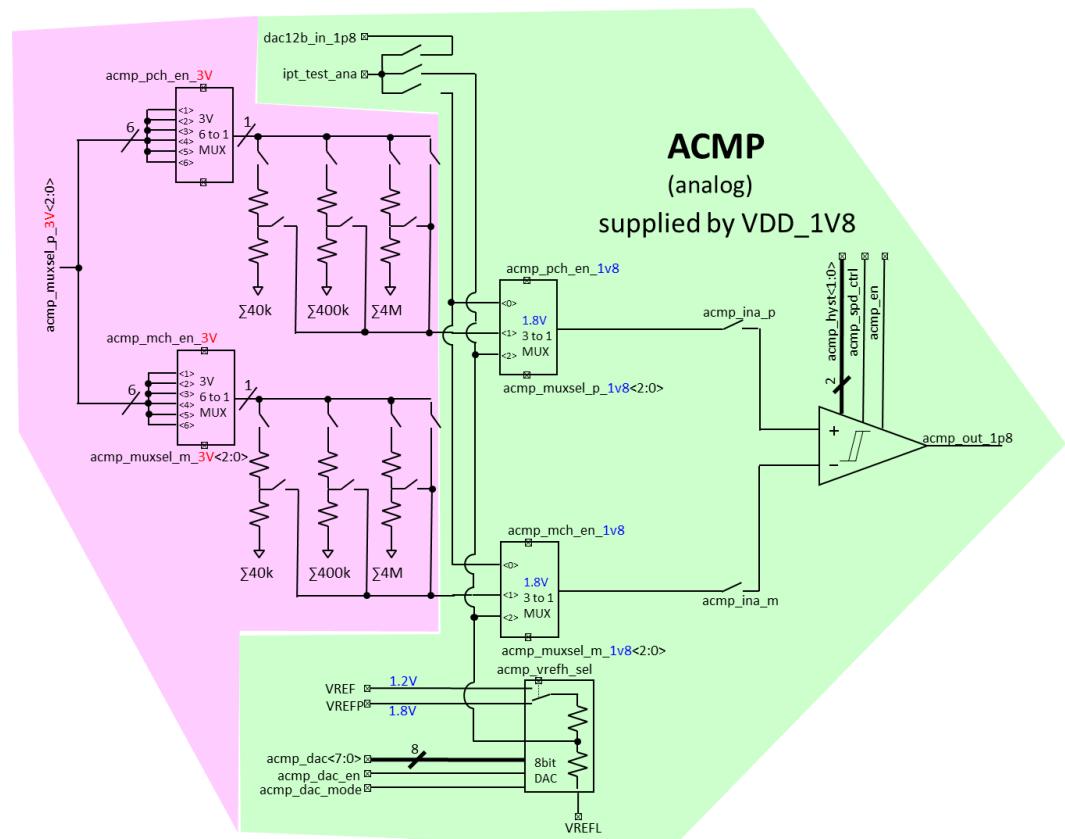


Fig 69. Analog Comparator (ACMP) analog block diagram

Fig 70 shows a high-level functional block diagram of the ACMP digital portion.

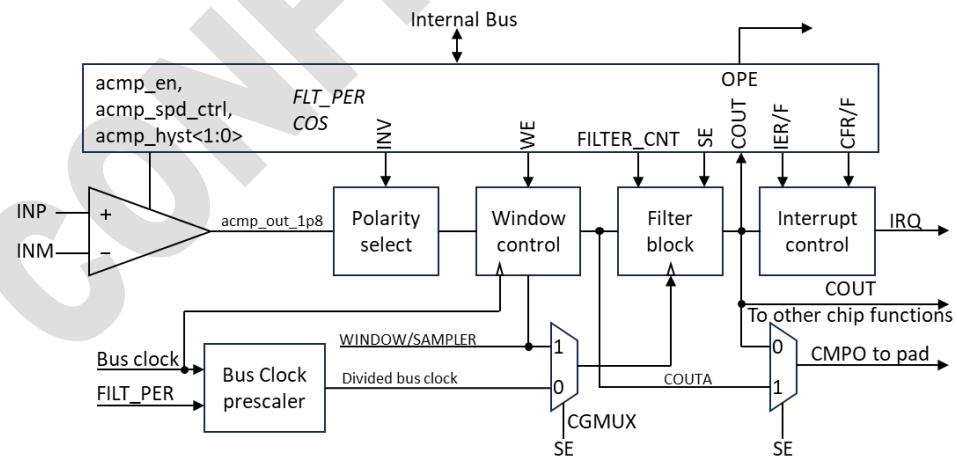


Fig 70. Analog Comparator (ACMP) digital block diagram

The main features of the ACMP are:

- Eight rail-to-rail input channels
 - Six input channels supporting up to 3.3V voltage range ;
 - Two input channels supporting up to 1.8V voltage ;

- Supports programmable 4-level hysteresis control ;
- Supports two software selectable performance levels:
 - Shorter propagation delay at the expense of higher power ;
 - Low power, with a longer propagation delay ;
- 8-bit monotonic DAC with two selectable voltage references
 - Supporting VREF 1.2V and VREFP 1.8V voltage reference ;
- Provides a selectable interrupt on rising-edge, falling-edge, or both comparator outputs ;
- Provides a selectable inversion on comparator output ;
- Includes the capability to produce a wide range of outputs, such as:
 - Sampled ;
 - Windowed, which is ideal for certain PWM zero-crossing detection applications ;
 - Digitally filtered:
 - Bypass filter ;
 - Clocks via an external Sample signal or a scaled bus block ;
- Uses external hysteresis at the same time that the output filter is used for internal functions;
- Supporting round robin mode ;
- Supports DMA transfer (CMP can select a comparison event to trigger a DMA transfer) ;
- Functional down to Deep Sleep mode:
 - CMP's window and filter functions are unavailable in Deep Sleep mode.
- Support Round robin feature in digital wrapper.

The ACMPs share the same 1.8V reference voltage with the ADCs (VREFP). One of the ACMP input channels provision for a connection from the 12-bit DAC and test-bus.

Table 121 shows the targeted ACMP IP key electrical specifications.

Table 121. Targeted i.MX RT2660 ACMP IP key electrical specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{DDA_3V3}	Analog supply voltage	2.4	3.3	3.6	V
V_{DDA_1V8}	Analog supply voltage	1.62	1.8	1.98	V
V_{DD_CORE}	Core (LV digital) regulated supply voltage	0.45	0.8	0.945	V
T_{pd}	Propagation delay – high-speed mode			50	ns
	Propagation delay – nano-power mode			5	μs
Input Muxes					
V_{in_3v3}	3.3V input channels – input voltage range	0		3.6V	V
V_{in_1v8}	1.8V input channels – input voltage range	0	1.8	1.98	V
Comparator					
V_{in}	Input voltage range	0	1.8	1.98	V
V_{offset}	Offset voltage – high-speed mode	-5		+5	mV
	Offset voltage – nano-power mode	-20		+20	mV
V_{hys}	Hysteresis voltage – setting 1	10			mV
	Hysteresis voltage – setting 2	20			mV
	Hysteresis voltage – setting 3	30			mV
I_{cmp}	Current consumption - high-speed mode	200			μA
	Current consumption - nano-power mode	400			nA
T_{init}	Initialization delay			40	μs
DAC					
V_{REF}	SoC internal reference voltage	1.2			V
V_{REFP}	SoC external reference voltage	1.8			V
Resolution	Resolution	8			bit

DNL	Differential Non-Linearity	-1	+1	LSB
INL	Integral Non-Linearity	-1	+1	LSB
FO	Offset error	-0.2	±0.1	%FSR
FG	Gain error	-0.2	±0.1	%FSR
I_{dac}	Current consumption - high-speed mode	10		μA
	Current consumption - nano-power mode	1		μA

More detailed information on the ACMP module can be found in its IP User Guide [46].

Table 122. IC requirements traceability: ACMP requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_AIO_3-2	This processor shall include 4x ACMP instances.	Must have	Yes
iMXRT2660_AIO_3-3	This processor shall also implement an input MUX that select how analog signals are routed to the plus or minus input of the comparator.	Must have	Yes, 8 channel input MUX
iMXRT2660_AIO_3-4	The ACMP shall operate from either 1.8V (nominal) or 3.3V (nominal) supply and cover the full voltage range.	Must have	Yes, 1.8V supported
iMXRT2660_AIO_3-5	The ACMP should support two different speed setting for trade-off between propagation delay and power consumption.	Must have	IP supports
iMXRT2660_AIO_3-6	The ACMP shall operate down to Deep Sleep mode.	Must have	Yes
iMXRT2660_AIO_3-7	The output of the comparator can be used in several different ways. The first is to have it route to a pin through with or without inversion. The second is through some digital filtering where it can be routed as an interrupt to the processor or as a trigger to peripherals. Some examples of peripherals that comparator are routed to are the timers, ADC, and DAC.	Must have	Yes

6.7.12 Frequency Measure Unit (FREQME)

The main purpose of the FREQME unit to measure the frequency of the IP functional clocks and - bus clocks. Refer to Section 6.2.7 for a brief description about the FREQME unit

The WAKE_SS includes one FREQME unit one to monitor the MODCON_WAKE clock outputs (WAKE.FREQME). Please refer to the RT2660_Clock_v<version>.xlsx in share point [Clock](#) for detailed assignment.

6.7.13 Cross-Trigger network

The i.MX RT2660 WAKE_SS has one XBAR instance. The purpose of these XBARs is to reduce the amount of WAKE_SS trigger outputs towards the other i.Mx RT2660 subsystems. The WAKE_SS XBAR configurations are shown in Table 123 and Fig 71, respectively.

Table 123. i.MX RT2660 WAKE_SS XBAR instance configuration

Instance	Number of inputs (N)	Number of outputs (M)	Number of outputs with control function (P)	Select registers	Control registers
XBAR	63	31	2	XBAR0.SEL[0-15]	n/a

Note: The WAKE_SS XBAR configuration might change according to definition change, please reference to i.MXRT2660_XBAR_v<version>.xlsx in share point [Interrupts_DMA_CrossTrigger](#) for latest update (if any).

Fig 51 shows a high-level block diagram of the WAKE_SS cross-trigger network.

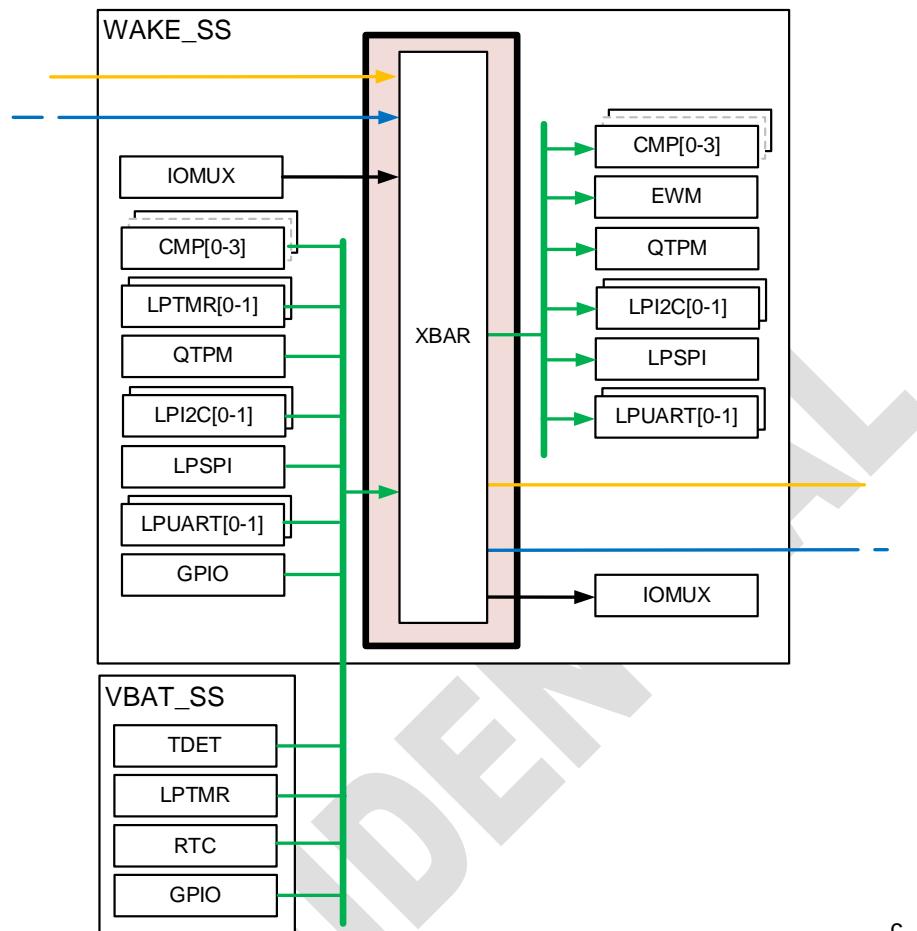


Fig 71. i.MX RT2660 WAKE_SS cross-trigger network block diagram

Please refer to Section 6.3.8.2 for an overview on how the WAKE_SS cross-trigger network shall be interconnected with the remainder of the SoC.

The i.MX RT2660 detailed Cross-Trigger Network assignments in a machine-readable format can be found at the following location: [XEA1_XbarMap.xlsx](#)

Please refer to the WAKE_SS HW.AS document for a detailed WAKE_SS trigger assignments [8].

6.8 COMMON Domain: System Control (SYSCON)

The System Control (SYSCON) subsystem brings together all building block related to power management, root clock generation and related control functionality. This concerns the Power Management Control subsystem (PMC_SS), the Clock Generation Unit (CGU), the global system controller comprising of two system control functions (RESETCON, POWERCON). The various IPs are connected to the MAIN_SS via the individual APB interfaces. Fig 72 shows a high-level block diagram of SYSCON.

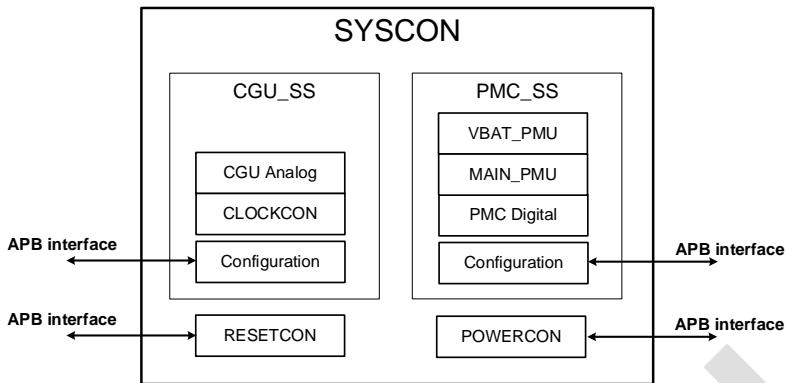


Fig 72. i.MX RT2660 SYSCON high-level block diagram

The following subsections describe the sub-block details.

6.8.1 Power Management Controller subsystem (PMC_SS)

The i.MX RT2660 power management controller sub-system (PMC_SS) comprises of embedded DC-DC conversion and LDO regulators to generate necessary on-chip power supply voltages.

Table 124 shows a high-level functional block diagram of the PMC_SS of i.MX RT2660. The PMC_SS consists of the following building blocks:

- VBAT PMU, which is the top-level of all VBAT power management analog functions ;
- MAIN PMU, which is the top-level of the other power management analog functions including the PMU clocking, supply supervision and SoC supply&temperature tamper detectors ;
- PMU Digital, which concerns the power management related statemachine ;
- APB configuration function of the PMC_SS, which is connected to the MAIN_SS.

Fig 73 shows a high-level functional block diagram of the i.MX RT2660 PMC_SS.

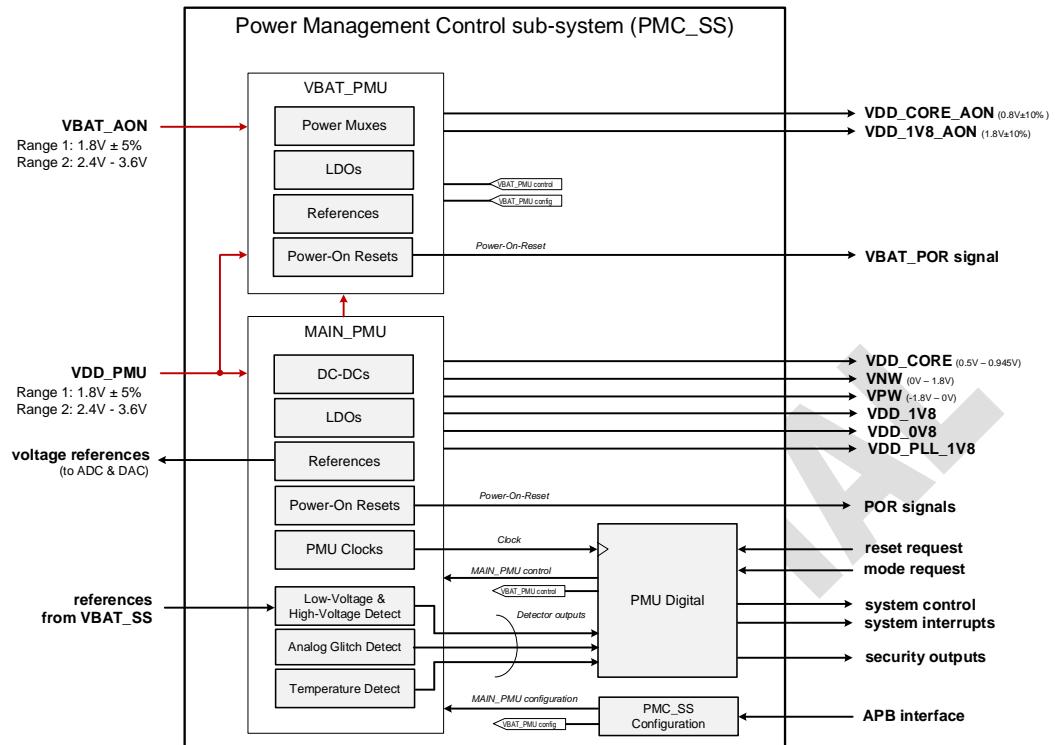


Fig 73. High-level functional block diagram of i.MX RT2660 PMC_SS

Chapter 8 provides more detailed information on the power architecture, power management unit and related control sequences. The following sub-sections provide a high-level functional overview of the different PMC_SS functions.

6.8.1.1 Supply voltage generation functions

Table 124 lists the DC-DC converters and LDO regulators that are included into the PMC_SS.

Table 124. PMC_SS supply voltage generation functions

IP block	VDD_IN	VDD_OUT	Description
MAIN PMU sub-components			
DCDC_CORE	1.8V ±5% 2.4V – 3.6V	0.45V – 0.945V	The DCDC_CORE operates from the main power supply input and generates the supply voltage of the digital core (VDD_CORE). Default, a VDD_CORE typical supply of 0.8V is generated, while supporting a range from 0.45V to 0.945V.
Body biasing	1.8V ±10%	0V – (1.5V±10%)	From LDO_1V8, a VNW voltage is generated to enable body biasing of the digital core.
		(-1.8V±10%) - 0V	From LDO_1V8, a VPW voltage is generated to enable body biasing of the digital core.
LDO_1V8 (2x)	1.8V ±5% 2.4V – 3.6V	1.8V ±5% 1.8V ±10%	The LDO_1V8 operates from the main power supply input and generates a fixed 1.8V supply voltage. The first LDO_1V8 (VDD_1V8) generates a supply for PHYs and Body Biasing IP. The second LDO_1V8

			(VDDA_1V8) generates a clean supply for the noise-sensitive blocks such as ADCs and DAC.
LDO_0V8 (2x)	1.8V \pm 5%	0.8V \pm 10%	The LDO_0V8 operates from the LDO_1V8 (VDD_1V8) and generates a fixed 0.8V supply voltage. The first LDO_0V8 (VDD_0V8) generates a supply for noisy blocks such as PHYs and IO. The second one (VDD_PLL_0V8) generates a clean supply for noise-sensitive blocks such as PLL.
LDO_1V5	1.8V \pm 5% 2.4V – 3.6V	1.5V \pm 10%	The LDO_1V5 operates from the VDD_PMU and generates a fixed 1.5V supply voltage (VDD_1V5) for PMU internal building blocks.
VBAT PMU sub-components			
PMUX_3V3	1.8V \pm 5% 2.4V – 3.6V	1.8V \pm 5% 2.4V – 3.6V	Power supply selection multiplexer, either selects VDD_PMU or VBAT_AON as input to VBAT_SS.
LDO_1V8	1.8V \pm 5% 2.4V – 3.6V	1.8V \pm 5% 1.8V \pm 10%	The LDO_1V8 operates from the PMUX_3V3 output and generates a fixed 1.8V Always-ON supply voltage needed for VBAT Reference sub-block.
PMUX_1V8	1.8V \pm 10%	1.8V \pm 10%	Power supply selection multiplexer, either selects LDO_1V8 output when operating from VBAT_AON or VDD_1V8 from MAIN_PMU.
LDO_0V8	1.8V \pm 5%	0.8V \pm 10%	The LDO_0V8 operates from the PMUX_1V8 output and generates a fixed 0.8V Always-ON supply voltage for various VBAT building blocks.
PMUX_0V8	0.8V \pm 10%	0.8V \pm 10%	Power supply selection multiplexer, either selects LDO_0V8 output when operating from VBAT_AON, or VDD_PMC_1V8 from PMC_SS
POR_1V8	1.8V \pm 10%	-	Power-On Reset associated to 1.8V supply at the output of the PMUX_1V8
POR_0V8	0.8V \pm 10%	-	Power-On Reset associated to 0.8V supply at the output of the PMUX_0V8

For more detailed information on the supply generation functions, please refer to the i.MX RT2660 Power Management Specification document [9].

The supply generation requirements & traceability are provided in Section 8.3

6.8.1.2 Reference voltage generation functions

The i.MX RT2660 does not include a programmable high accurate voltage reference. The associated area overhead of this accurate voltage reference is considered too large, while the need for a 1.8V voltage reference cannot be provided in all cases. Hence, it has been decided in close alignment with BL to drop the on-chip voltage reference circuit.

The required voltage reference to internal analog peripherals such as an ADC, DAC or analog comparator shall be provided externally (i.e. VREFP/VREFN pads) or via VDDA_1V8 supply.

Table 125. IC requirements traceability: VREF requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_AIO_4-1	The device shall embed as voltage reference buffer which can be used as voltage reference for ADCs and DAC.	Must have	Rejected, CR upcoming
iMXRT2660_AIO_4-2	The device shall implement a voltage reference buffer which can be used as voltage reference for ADCs and DAC.	Must have	Rejected, CR upcoming
iMXRT2660_AIO_4-3	The VREF shall include programmable trim register with 0.5 mV steps, automatically loaded with factory trimmed value upon reset.	Must have	Rejected, CR upcoming
iMXRT2660_AIO_4-4	The VREF shall support a VREF output to provide an reference input to external components, such as ADC, threshold detector, or programmable gain amplifier.	Must have	Rejected, CR upcoming
iMXRT2660_AIO_4-5	The VREF output pin will be 1.2V nominal at room temperature.	Must have	Rejected, CR upcoming

6.8.1.3 Supply supervision functions

The i.MX RT2660 PMC_SS makes use of Power-On-Reset (POR) blocks and Voltage Monitor blocks for checking proper startup of its input power supply as well as its generated supply voltages. Table 126 shows an overview of the targeted supply supervision blocks within PMC_SS.

Table 126. PMC_SS supply supervision functions

IP block	Related supplies	Description
POR_VSUPPLY	VDD_PMU, VBAT_AON	Low-power POR1V8 with 200mV hysteresis <ul style="list-style-type: none"> Low threshold: 1.4V; High threshold: 1.6V Low-power POR3V with 200mV hysteresis <ul style="list-style-type: none"> Low threshold: 2.1V; High threshold: 2.3V
POR_VDD_1V5	VDD_1V5	Low-power POR1V5 with 50mV hysteresis <ul style="list-style-type: none"> Low threshold: 1.25V; High threshold: 1.3V
VDD_CORE monitor	VDD_CORE	VDD_CORE monitor with 0.2V comparator hysteresis <ul style="list-style-type: none"> 0.450V ± 9mV for falling voltage threshold 0.650V ± 13mV for rising voltage threshold 0.2V ± 4mV hysteresis
VDD_0V8 monitor	VDD_0V8	VDD_0V8 monitor with 0.2V comparator hysteresis <ul style="list-style-type: none"> 0.450V ± 9mV for falling voltage threshold 0.650V ± 13mV for rising voltage threshold 0.2V ± 4mV hysteresis
VDD1V8 monitor	VDD_1V8	VDD_1V8 monitor with 50mV comparator hysteresis <ul style="list-style-type: none"> 1.4625V -0.325V~+0.275V for falling voltage threshold 1.5125V -0.325V~+0.275V for rising voltage threshold 50mV ± 1mV hysteresis
VDDA1V8 monitor	VDDA_1V8	VDDA_1V8 monitor with 50mV comparator hysteresis <ul style="list-style-type: none"> 1.4625V -0.325V~+0.275V for falling voltage threshold 1.5125V -0.325V~+0.275V for rising voltage threshold 50mV ± 1mV hysteresis
VDD_PMU_1V8 monitor	VDD_PMU_1V8	VDD_PMU_1V8 monitor with 50mV comparator hysteresis <ul style="list-style-type: none"> 1.4625V -0.325V~+0.275V for falling voltage threshold 1.5125V -0.325V~+0.275V for rising voltage threshold 50mV ± 1mV hysteresis
VDD_PMU_3V monitor	VDD_PMU_3V	VDD_PMU_3V monitor with 50mV comparator hysteresis

-
- 2.1375V -37.5mV~+42.5mV for falling voltage threshold
 - 2.1875V -37.5mV~+42.5mV for rising voltage threshold
 - 50mV ± 1mV hysteresis
-

Reference to PMU_RT2660_SPECIFICATION [47]

In order to minimize SoC static power consumption, the POR and monitor blocks shall be designed for low-power operation, e.g. preferably zero-power POR.

For more details on the POR and monitor blocks, please refer to the i.MX RT2660 Power Management Specification document [9].

6.8.1.4 Security related functions

A.3 Voltage sensors

The i.MX RT2660 PMC_SS makes use of voltage sensors for checking voltage excursions as well as voltage spikes on power supply nodes that are externally accessible. Such voltage excursions and voltage spikes provide insights whether power supply voltages are reliable, or whether a security/tampering event has occurred. Table 127 shows an overview of the targeted voltage sensor within the PMC_SS.

Table 127. **PMC_SS voltage sensor functions**

IP block	Related supplies	Description
VDD_0V8 sensor	VDD_0V8	Detection range: 0.875V±25mV – 1.025V±25mV; 50mV steps
		Detection range: 0.575V±25mV – 0.725V±25mV; 50mV steps
VDD_CORE sensor	VDD_CORE	Detection range: 0.875V±25mV – 1.025V±25mV; 50mV steps
		Detection range: 0.575V±25mV – 0.725V±25mV; 50mV steps
VDD_1V8 sensor	VDD_1V8	Detection range: 2.00V+100mV – 2.15V+100mV; 50mV steps
		Detection range: 1.45V+100mV – 1.60V+100mV; 50mV steps
VDDA_1V8 sensor	VDDA_1V8	Detection range: 2.00V+100mV – 2.15V+100mV; 50mV steps
		Detection range: 1.45V+100mV – 1.60V+100mV; 50mV steps
VDDPMU_1V8 sensor	VDD_PMU_1V8	Detection range: 2.00V+100mV – 2.15V+100mV; 50mV steps
		Detection range: 1.45V+100mV – 1.60V+100mV; 50mV steps
VDDPMU_3V sensor	VDD_PMU_3V	Detection range: 3.70V±75mV – 3.85V±75mV; 50mV steps
		Detection range: 2.20V±75mV – 2.35V±75mV; 50mV steps

Reference to PMU_RT2660_SPECIFICATION [47]

The voltage sensor blocks shall be capable of detecting voltage excursions as fast as 200ns, as well as detecting voltage spikes between 10ns and 200ns spike widths. In order to minimize SoC static power consumption, the voltage sensor blocks shall be designed for low-power operation, e.g. <10µA during SoC active mode operation while <50nA during SoC standby mode operation.

The output of the voltage sensor blocks shall be captured into status registers of the PMU Digital. The PMU Digital shall offer programmability on the downstream action after one or more voltage sensor blocks have triggered. These actions could be configured as:

- To signal a power supply voltage OK signal to the PMC FSM that is part of the PMC_SS. When not OK, the PMC FSM can trigger an exception condition such as system reset.

- Signaling an interrupt to the downstream security subsystem (i.e. BBSM) of i.MX RT2660, to indicate a possible tampering event.

For more details on the voltage sensor blocks, please refer to the i.MX RT2660 Power Management Specification document [9].

A.4 Temperature detector

The i.MX RT2660 PMC_SS makes use of temperature sensor for checking die temperature excursions. Such temperature excursions provide insights whether die temperature is within the expected range, or whether a security/tampering event has occurred. Both low-temperature and high-temperature warning is to be provided.

The temperature detector is capable of generating temperature warning interrupts when the die temperature exceeds a given low-temperature and high-temperature threshold.

- Two different low-temperature threshold can be chosen: $\{-40, -30\}^{\circ}\text{C} \pm 10^{\circ}\text{C}$
- Four different high-temperature thresholds can be chosen: $\{120, 125, 130, 135\}^{\circ}\text{C} \pm 5^{\circ}\text{C}$.

The output of the temperature detector shall be captured into status registers of the PMU Digital. The PMU Digital shall signal an interrupt to the downstream security subsystem (i.e. BBSM) of the i.MX RT2660, to indicate a possible tampering event.

For more details on the temperature detector block, please refer to the i.MX RT2660 Power Management Specification document [9].

6.8.2 Clock Generation Unit subsystem (CGU_SS)

The i.MX RT2660 clocking system comprises of a central clock generation unit subsystem (CGU_SS) that works together with local clock control units within the subsystems (as part of MODCON), and the ultra-low power clock sources in the VBAT domain. In this section, the main functionalities of the CGU_SS will be described. Chapter 6.10 provides an elaborated descriptions of the clock design philosophy and the clock architecture.

Fig 74 shows a high-level functional block diagram of the CGU_SS of i.MX RT2660. The CGU_SS comprises of the following main building blocks:

- CGU analog (CGUANA), which is the top level macro containing all CGU related analog modules. It generates the clock sources that are controlled by CGU digital ;
- CGU digital (CGUDIG), which is the toplevel macro containing the following sublevels:
 - Clock Control (CLOCKCON) for the SoC root clock generation ;
 - FRO Tuner for trimming FRO frequencies against a fixed reference clock ;
 - CGU_SS configuration register that can be accessed via the APB interface.

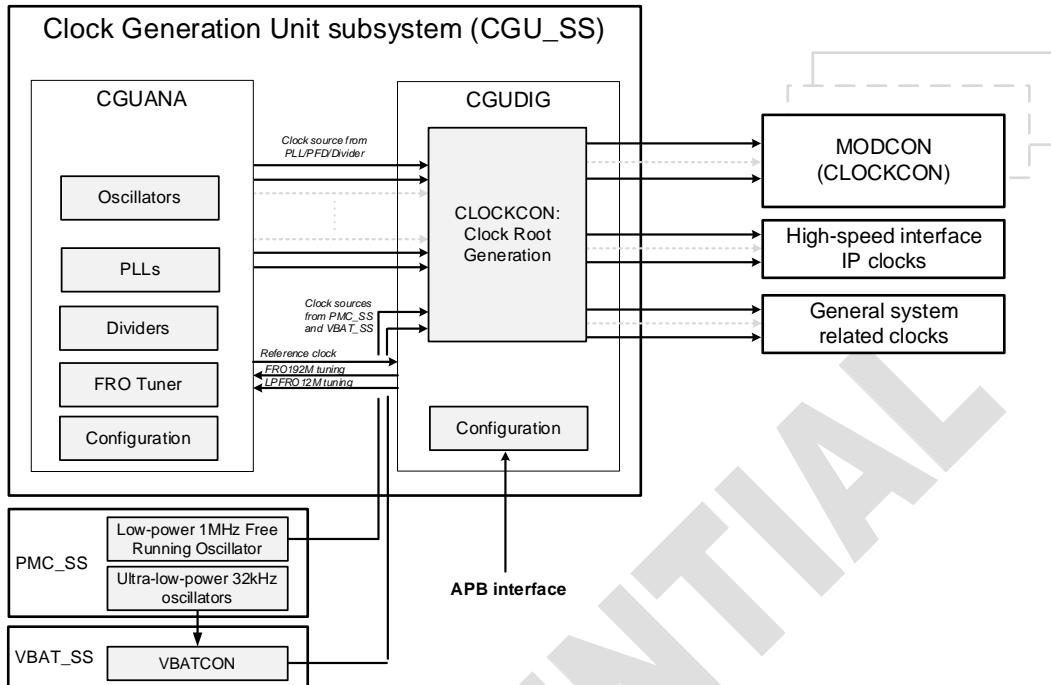


Fig 74. High-level functional block diagram of i.MX RT2660 CGU_SS

6.8.2.1 Clock sources

Table 128 shows an overview of the i.MX RT2660 clock sources.

Table 128. i.MX RT2660 CGU_SS clock sources

IP block	Hierarchy	Description
192MHz free-running oscillator (FRO192M)	CGUANA	The FRO192M is the SoC main system FRO, and is used as default source to the SoC until software decides otherwise. One of the main uses is to generate the 24MHz clock source for the chip during startup before the SXOSC is ready. It can also be used as the main clock source in system which does not have any crystal oscillator.
Crystal oscillator (SXOSC)	CGUANA	The SXOSC brings in the possibility to bring in an external clock source. The supported crystal frequencies ranging from 19.2MHz to 40MHz. Default is 24MHz. The SXOSC and selected crystals shall offer a frequency accuracy of $\pm 50\text{ppm}$ or better. From application perspective, it is envisioned that the SXOSC is the primary clock source for the PLLs.
12MHz low power oscillator (LPOSC12M)	CGUANA	The Low Power 12MHz FRO provides a low power clock source to processor, DMA controller, bus fabrics and/or peripherals in low-power use-case applications. The LPOSC12M is the main low-power clock reference for peripherals, and facilitates hardware voice activity detection by the Digital Microphone during Deep Sleep mode. .
External clock input	CGUANA	The XOSC crystal pads are re-purposed to provide an external clock as reference reference clock for the PLLs.
1MHz low power clock input	CGUDIG	The Low-Power 1MHz FRO clock is provided by the PMC_SS. Its main use is to provide a clock source to peripherals when the SoC is

		operating in a low-power scenario e.g. Low-Power Run mode or a SoC standby mode.
32kHz clock input	CGUDIG	The 32kHz clocks are provided by VBAT_SS to CLOCKCON, to provide a ultra-low-power clock source for time references. There are two 32kHz clocks, namely a crystal-based clock and a free-running-oscillator clock.

The clock source requirements & traceability are provided in Section 7.2.1

6.8.2.2 Generated clock sources

Next to the previously described clock sources, a number of subsequent clock sources are generated for downstream usage in the i.MX RT2660 SoC. Table 129 provides an overview of the generated clock sources.

Table 129. **i.MX RT2660 generated clock sources**

IP block	Hierarchy	Description
FRO192M clock divider	CGUANA	<p>Together with the FRO192M, synchronous dividers are used to create the following frequencies:</p> <ul style="list-style-type: none"> fro_192m: 192MHz frequency DIV2: 96MHz frequency (fro_96m) DIV4: 48MHz fixed frequency (fro_48m) DIV8: 24MHz fixed frequency (fro_24m) – PLL input clock default <p>Each frequency divider can be enabled individually.</p>
PLLs	CGUANA	<p>There are five PLLs: a core PLL, a main PLL, a system PLL, an audio PLL and a video PLL.</p> <ul style="list-style-type: none"> PLL_CORE : 0.5-1.2GHz VCO, set to 700MHz with 50% duty cycle for the SoC core to support maximum compute frequency operation ; PLL_MAIN : 2.0GHz VCO and derives four dividers to generate an accurate clock for the SoC core, ethernet IP and peripherals ; <ul style="list-style-type: none"> IDIV0: typically 500MHz, 50% duty cycle, ±50ppm accuracy IDIV1: typically 400MHz, 50% duty cycle, ±50ppm accuracy FDIV0: 133...400MHz flexible clock source ; FDIV1: 133...400MHz flexible clock source ; FDIV2: 133...400MHz flexible clock source. PLL_SYS : 2.0GHz VCO and derives four dividers to generate an accurate clock for high-speed interfaces w/ spread spectrum support; <ul style="list-style-type: none"> IDIV0: typically 500MHz, 50% duty cycle ; IDIV1: typically 400MHz, 50% duty cycle ; FDIV0: 333/320/266MHz typ., 50% duty cycle ; FDIV1: 333/320/266MHz typ., 50% duty cycle. PLL_AUDIO: 722-786MHz VCO, set to 786MHz used to generate a low-jitter reference clock for audio peripherals and audio interfaces. <ul style="list-style-type: none"> 786MHz – IDIV0: typically 49.152MHz (multiple of 16/32/48/96/192kHz sampling clock) 722MHz – IDIV1: typically 45.158MHz (multiple of 14.7/29.4/44.1/88.2/176.4kHz sampling clock) PLL_VIDEO: 722-786MHz VCO, set to 742.5MHz used to generate a flexible reference clock for display pixel clock <ul style="list-style-type: none"> 742.5MHz – IDIV0: typically 74.25MHz

Both the clock sources and the generated clock sources are inputs to the clock slices that are part of CLOCKCON, to create the root clocks for the downstream SoC components.

The generated clock source requirements & traceability are provided in Section 7.2.2

6.8.2.3 Clock root generation

The CGU_SS implements a flexible clocking scheme that is based on the usage of clock slices to create various root clocks for the subsystems of i.MX RT2660. Each clock slice takes the clock source from Oscillators, PLLs, or generated clock sources, and produces the clock root with the required frequency. Fig 75 shows a high-level diagram illustrating this scheme.

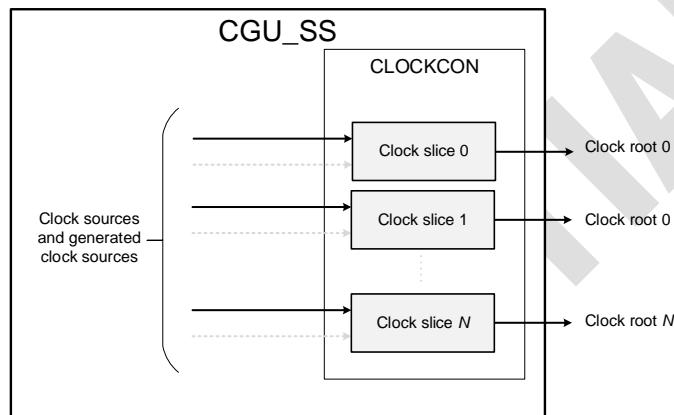


Fig 75. Overview of CLOCKCON clock slice approach for root clock generation

Section 7.2 provides detailed description of the CGU_SS generated clocks.

6.8.2.4 FRO Tuner

The CGUDIG contains FRO_TUNER modules that is used in conjunction with the FRO192M and LPFRO12M. The FRO_TUNER module generates system clock outputs that are based on a trimmable FRO clock source and a reference clock (e.g. SXOSC clock input). It offers the following operating modes:

- Open Loop (default): In this mode, the FRO trim value (that is configured either via the fuse option input or a programmable trim value written to FRO Trim register) specifies the FRO output clock frequency.
- Closed Loop: In this mode, FRO_TUNER provides the option for a built-in hardware to adjust the FRO output clock automatically until the output clock locks to a target frequency that can be configured into the FRO Expected Trim Count register. To allow for closed-loop operation, the FRO_TUNER requires a clock reference provide by another clock function e.g. SXOSC.

The i.MX RT2660 FRO_TUNER is based on the version used in i.MX RT700.

6.8.3 Reset Controller

The Reset Controller (RESETCON) is the SoC global reset controller that collates the different reset sources and generates the global cold reset and the global warm reset for all subsystems. It includes status registers to report the source of the latest global reset, individual subsystem power domain resets and sticky reset registers to enable debugging of multiple reset sources. The external reset pins (POR_b and RESET_b pins) are also controlled by the reset controller. RESETCON interfaces

to the SLEEPCON that in each main subsystem to generate the local warm reset and local cold reset for that subsystem.

More information on the RESETCON is provided in Section 7.6.3.

An overview of the i.MX RT2660 reset architecture is provided in Section 7.5.2.3.

6.8.4 Power Controller

The Power Controller (POWERCON) is used to set the power configuration for the device, including regulator settings (LDO, DCDC), voltage monitors, power domain and SRAM power switches, and power-down control for analog modules. POWERCON sets the power configuration for the device based on activity and wakeup signals sourced from the SLEEPCON instances within each subsystem, and from system level wakeup sources in the PMC and VBAT domains. Software assigns various activity and wakeup signals to select the different power configuration registers (PDCFG registers). Each PDCFG register is configured by software to specify the power state that needs to be applied when certain subsystems or wakeup sources are active. POWERCON uses the state of the various activity and wakeup signals to select one or more of the PDCFG registers for the device, which is then used to configure the various regulators and power switches appropriately.

More information on the POWERCON is provided in Section 8.6.

6.9 COMMON Domain: VBAT_SS

The VBAT_SS contains logic that retain powered in all power modes and that can be powered from an independent backup battery supply. This includes Real Time Clock and associated oscillators, tamper pins and wakeup pin functions. A small GPIO port is supported that remains powered with the VBAT_SS. The VBAT_SS interfaces to the PMC_SS and provides pin muxing functions for interfacing to an external PMIC or external switches.

Fig 76 shows a block diagram of the VBAT_SS and connection to related PMC_SS components.

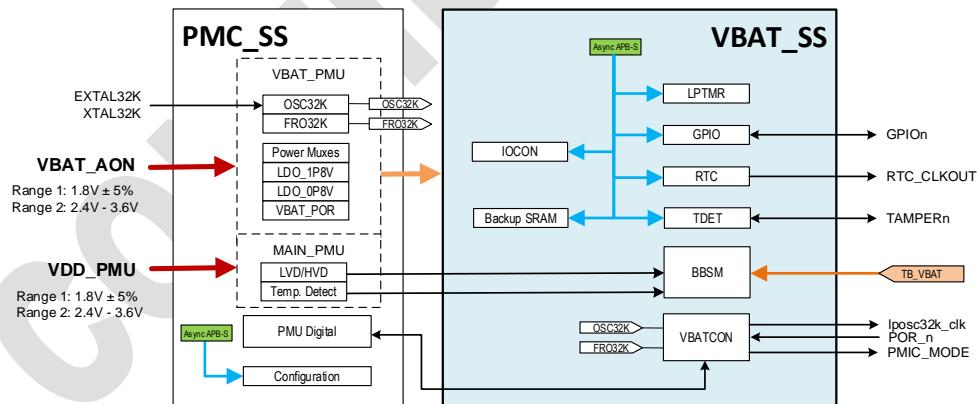


Fig 76. i.MX RT2660 VBAT_SS functional block diagram

The VBAT_SS includes the following main functionalities:

- Selection of ultra-low-power clock from nano-power 32kHz clock oscillator (OSC32K) or 32kHz Free Running Oscillator (FRO32K) ;
- Real-Time Clock function ;
- Low Power Timer function ;
- Configurable Always-On General-Purpose IO function ;
- 2KB Backup SRAM ;

- Battery Backed Security Module (BBSM) with 256-bit register file and internal tamper detection function ;
- Tamper Detect function to detect external tamper function with 2 tamper IO ;
- PMIC control interface.

The VBAT_SS is powered by the VBAT_PMU that resides in the PMC_SS. Refer to Section 0.

The remainder of this section provides an functional overview of the various components. More detailed information on the clock-, power management- and tamper related functions can be found in Section 6.9.4 and Chapter 9, respectively.

Table 130. **IC requirements traceability: VBAT_SS clock source requirements (part i)**

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_CLK_2-18	32kHz FRO - A low frequency clock generated internally to be used as an alternative to the RTC clock when the external RTC is not available.	Must have	Yes
iMXRT2660_CLK_4-2	The RTC oscillator is in the battery-backup domain.	Must have	Yes, in VBAT_PMU

6.9.1 VBAT_SS configuration

6.9.1.1 Digital interface

The VBAT_SS shall have the following interface to the rest of the i.MX RT2660 SoC.

Table 131. **i.MX RT2660 VBAT_SS digital interface**

Interface	Type	Direction	Description
APB_VBAT	APB	From WAKE_SS	Asynchronous APB for register accesses
TB_VBAT	APB	From CSSI	Asynchronous APB for Trust Bus access
GPIO[3:0]	Pad Interface	I/O	GPIO signals
TAMPER[1:0]	Pad Interface	I/O	TAMPER signals
RTC_CLKOUT	Pad Interface	O	RTC output signal
PMIC_MODE	Pad Interface	O	Output signals for PMIC
RTC Interrupt	Interrupt	O	Interrupt output
RTC Trigger	Trigger	O	RTC 1 Hz trigger output
TDET Interrupt	Interrupt	O	Interrupt output
TDET Trigger	Trigger	O	Trigger output (tamper detect)
TDET Reset	Reset	O	Warm reset request (tamper)
GPIO Interrupt	Interrupt	O	GPIO interrupt
GPIO DMA Request	DMA	I/O	GPIO DMA request and acknowledge
GPIO Trigger	Trigger	O	GPIO Trigger
PMC_SS	Digital	I/O	Mode Interface with PMC_SS
32kHz Clock	Clock	Output	32kHz clock output to SoC

6.9.1.2 Memory address map

The VBAT_SS local memory address map shall be as follows.

Table 132. **i.MX RT2660 VBAT_SS memory address map**

Interface	Type	Direction	Description
VBAT_PMC	0x0000_0000	0x0000_FFFF	64kB

RTC	0x0000_3000	0x0003_FFFF	64kB
TDET	0x0000_4000	0x0004_FFFF	64kB
LPTMR0	0x0000_5000	0x0005_FFFF	64kB
GPIO_VBAT	0x0000_6000	0x0006_FFFF	64kB
IOCON_VBAT	0x0000_7000	0x0007_FFFF	64kB
Backup SRAM	0x0000_8000	0x0008_FFFF	64kB

6.9.1.3 Reset & Control

All logic within VBAT_SS is reset by the VBAT POR. Modules may implement a software reset bit within the register map for each module.

The VBAT_SS is not anticipated to implement a MODCON instance, all module configuration should be integrated within the register map for each module.

The VBAT_SS does not implement any TRDC checkers within the subsystem, an MBC with 4kB block size is implemented in the MAIN_SS on the APB bus into the VBAT_SS.

6.9.1.4 System Configuration

The VBAT_SS is not anticipated to implement a MODCON instance, all module configuration should be integrated within the register map for each module. If a MODCON instance is implemented, then it shall be implemented such that there is no free-running MHz clock source available and it will support complete clock gating of the 32kHz clock tree at the clock root.

6.9.2 Clock functions

The VBAT_SS implements the following two clock domains:

- 32kHz Clock
 - Configured by software to either the FRO32K (default) or the OSC32K ;
 - The VBAT_SS shall select the 32 kHz oscillator clock source for the rest of the SoC from either the OSC32K or FRO32K ;
- Bus Interface Clock
 - This clock shall only be active during a register access to a module within the VBAT_SS ;

There shall be no free running MHz clock available in this subsystem.

6.9.2.1 32kHz clock oscillator

The VBAT OSC32K shall be implemented within the VBAT_PMU of the PMC_SS. It offers the following main features:

- Low power 32.768 kHz crystal oscillator ;
- Integrated load capacitors for EXTAL and XTAL pins ;
- Nano-power mode and higher performance mode ;
- Supports bypass option for 32.768 kHz clock source ;
- OSC32K output gated during startup ;
- Clock monitor for 32.768kHz clock input ;
- 32 KHz clock output that selects FRO32K by default and switches to OSC32K once clock is enabled and valid ;
- Software configured option to clock gate the 32.768kHz clock outputs to other subsystems.

Table 133. IC requirements traceability: VBAT_SS clock source requirements (part ii)

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_CLK_4-3	The RTC oscillator, in conjunction with an external crystal, generates a 32.768kHz real-time reference clock for this processor.	Must have	Supported, OSC32K
iMXRT2660_CLK_4-4	The RTC clock is always enabled.	Must have	Targeted

6.9.2.2 32kHz free running oscillator

The VBAT FRO32K shall be implemented within the VBAT_PMU of the PMC_SS. It offers the following main features:

- Low power 32.768 kHz internal clock source ;
- Factory trimmed (open loop) to +/- 2% ;
- Closed loop trimmable to +/- 250ppm from MHz crystal OSC and assuming temperature rate of change of <1°C every 1 second ;
- Frequency measurement logic is not implemented within FRO32K register map, must be implemented in another subsystem.

Table 134. IC requirements traceability: VBAT_SS clock source requirements (part iii)

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_CLK_8-2	This is a very low power 32KHz RC oscillator. This clock source should be a default if external 32KHz oscillator clock stops.	Must have	Targeted

6.9.2.3 Real-Time Clock (RTC)

Real Time Clock (RTC) is a low-power module that provides time keeping and calendaring functions, protection against spurious memory/register updates. It can also compensate the 1 Hz clock against variations in 32 kHz clock in oscillator due to crystal or temperature.

The i.MX RT2660 RTC function is based on the RTC function of MCX N10.

The RTC includes the following features:

- Designed for low power
 - Time and date counters are interleaved to prevent simultaneous toggling ;
- Basic clock functions
 - Separate counters for days, hour, minutes, and seconds
 - Calendaring support—Separate counters for year, month, and day of the week
 - Automatic adjustment for daylight saving with user-defined parameters ;
 - Automatic adjustment for month and leap year ;
 - External clock support to run the counters if you choose to provide an externally-compensated 1Hz clock ;
- Time zone offset—RTC uses local time which implicitly contains the time zone offset ;
- Programmable alarm with interrupt—Alarm is output from RTC in case the MCU uses it as a wake up event ;
- Periodic interrupts (sampling timer interrupts) ;
- Hardware compensation—Compensates 1 Hz clock (to the counters) against frequency variations in oscillator clock due to temperature changes or crystal characteristics. Programmable correction factor calculated by firmware ;
- 16-bit CPU register programming interface with protection against runaway code ;
- Option to output the buffered 32.768 or 16.384 kHz clock or the compensated 1 Hz clock.

The following change requests to Robust RTC shall be implemented:

- Update partitioning to reduce number of level shifters between LP and HP domains ;
- Support subsecond counter with wakeup capability; support atomic reading of subsecond counter (avoid multiple read and compare) ;
- Evaluate additional low power enhancements (eg: ripple counter).

6.9.3 Memory functions

6.9.3.1 BBSM retention registers

The Battery Backup Security Module (BBSM) implements 256-bit general purpose registers for secure key storage. The BBSM registers are accessible via a dedicated bus from CSSI module.

Table 135. **IC requirements traceability: VBAT Domain requirements (part i)**

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_SEC_20-8	The VBAT domain shall include 256 bits general purpose registers for key storage.	Must have	Targeted, BBSM

6.9.3.2 Retention memory

The retention memory is a 2 kB SRAM instance from the selected SRAM compiler. Given its small instance size and given the low-leakage performance of the selected SRAM compiler, it has been decided to not use the Synopsys ULL SRAM compiler.

Table 136. **Retention SRAM instance configuration with NXP's EFSPRAM compiler**

Total size	# words	# bits	# instances	Other configurations
2 KB	512	32	1	LVT, ZBB

The retention memory shall be configured for lowest leakage and shall run at reduced operating frequency for minimizing current consumption on VBAT_SS supply.

Table 137. **IC requirements traceability: VBAT Domain requirements (part ii)**

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_SEC_20-9	The VBAT domain shall include 2KB SRAM for sensitive information storage.	Must have	Yes

6.9.4 Security functions

6.9.4.1 External tamper detection

External Tamper Detection is a special mechanism provided through a chip pin to signal when the device encounters unauthorized opening or tampering. Inside the chip, the received signal is compared with the desired signal level, once an unequal, tamper event is found. When the desired signal is fixed, it is called passive tamper; when the desired signal level is also toggling with time, it is called active tamper.

The i.MX RT2660 shall support both passive and active tamper detection via two tamper pins. The Tamper Detection (TDET) module implements the external tamper detection as they require customer direct control. Refer to Section 6.9.4.3 for more information on the TDET module.

Table 138. **IC requirements traceability: VBAT Domain requirements (part iii)**

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_SEC_20-5	The VBAT domain shall include 2 tamper pins, which can be functional as two independent passive tamper pins or form one pair of active tamper.	Must have	Yes, TDET

6.9.4.2 BBSM internal tamper detection

The BBSM shall implement internal tamper detection based on 32 kHz clock monitoring, voltage monitoring (LVD/HVD) and temperate detector.

The OSC32K and FRO32K functions are implemented in the VBAT_PMU in the PMC_SS; the 32 kHz clock source selection shall be done within the VBAT_SS (e.g. VBATCON) under clock tamper monitoring of BBSM. This clock tamper monitoring shall be does in all power modes.

The voltage monitors and temperature detector function are implemented in the PMC_SS. The voltage monitoring and tamper detection shall be down in all power modes, except for Deep Power Down as per alignment with the target i.MX RT2660 security approach. The i.MX RT2660 shall always undergo a security boot after wake-up from Deep Power Down mode.

Table 139. IC requirements traceability: VBAT Domain requirements (part iv)

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_SEC_20-6	The VBAT domain shall support clock, voltage, and temperature monitor tamper.	Must have	Rejected, no voltage & temp tamper in DPD. Open: Req. update ongoing

6.9.4.3 Tamper Detect (TDET)

The Tamper Detect (TDET) is re-used from Nirvana; it supports the following main features:

- Up to 16 external tamper pins capable of generating interrupt or tamper event:
 - Configurable polarity and digital glitch filter with optional prescaler
 - Configurable for either passive or active tamper input
 - Supports software-initiated tamper pin assertion
 - Supports periodic sampling of the tamper pin
- Up to 14 internal tamper sources plus software-initiated tamper capable of generating interrupt or tamper event
- Tamper time register records time of tamper event
- Up to 4 active tamper shift registers each with configurable polynomial
- Register protection
 - Lock register requires VBAT POR or software reset to enable write access

The TDET of the i.MX RT2660 shall be configured as follows.

Table 140. i.MX RT2660 VBAT_SS TDET module configuration settings

Instance	Parameter	Value	Description
TDET	ADDR_MSB	16	Peripheral slot is 64kB
TDET	SECREG_EN	0	Secure register file implemented
TDET	SECREG_NUM	8	Secure register file is 256-bit
TDET	TAMPER_WD	0	Number of internal tamper sources

TDET	TAMPER_INV	0	Configures polarity of internal tamper sources
TDET	TAMPER_NUM	2	Number of Tamper pins implemented
TDET	ACTIVE_EN	1	Active Tamper function is implemented
TDET	ACTIVE_NUM	2	Number of active tamper shift registers with configurable polynomial
TDET	IRQE_RST	0	Interrupt disabled by default
TDET	LP_EN	1	Implement ripple counter for low power

6.9.4.4 VBATCON

VBATCON is glue logic implemented within the VBAT_SS and interfaces to PMC domain. It implements the following functions:

- Latch the VBAT POR and provide to RESETCON. Negate only when the PMC domain has powered up and acknowledged ;
- Latch the POR_b pin and provide to RESETCON. Negate only when the PMC domain has powered up and acknowledged ;
- Latch the full deep power down (FDPD) request from POWERCON. Negate on any wakeup source that is generated within the VBAT domain (including VBAT POR or POR_b pin) ;
- Force disable the PMC DCDC/LDO regulators during full deep power down mode ;
- Force the PMIC_MODE pins to "11" in full deep power down mode; otherwise force the PMIC_MODE pins to "00" on any wakeup source that is generated within the VBAT domain (including VBAT POR or POR_b pin); otherwise passthrough the PMIC_MODE pin value from POWERCON ;
- Receive the OSC32K and FRO32K clocks from the PMC domain, and selects the 32 kHz ultra-low-power clock source for the remainder of the SoC. Initially, this shall be the FRO32K clock, move to OSC32K when available and reliable, and revert back to FRO32K in case of unreliable OSC32K clock.

6.9.5 IO functions

6.9.5.1 GPIO

The GPIO module in the VBAT_SS includes the following features:

- Port Data Input (PDIR) register displays the logic value on each pin when the pin is configured for any digital function provided the corresponding Port Control and Interrupt module for that pin are enabled ;
- Port Data Output (PDOR) register with corresponding set/clear/toggle registers controls output data of each pin when the pin is configured for the GPIO function ;
- Port Data Direction (PDDR) register controls the direction of each pin when the pin is configured for the GPIO function ;
- Port Input Disable (PIDR) register controls the disable of the input for each general-purpose pin ;
- Pin interrupts
 - Interrupt flag and enable registers for each pin are functional in all digital pin muxing modes ;
 - Support for interrupt, peripheral trigger, or DMA request configured per pin ;
 - Support for edge sensitive (rising or falling, or both) or level sensitive (low, high) configured per pin ;
 - Asynchronous wake-up in Low-Power modes ;
 - GPIO module generates a total of 2 interrupts, 2 output triggers and 2 DMA requests ;

- Each pin can be used to generate a single interrupt, output trigger or DMA request ;
- Protection registers
 - Each pin is configured for Secure or Non-Secure and Privilege/Non-Privilege access ;
 - Each interrupt, trigger and DMA request domain is configured for Secure or Non-Secure and Privilege/Non-Privilege access

The GPIO of the i.MX RT2660 VBAT_SS shall be configured as follows.

Table 141. **i.MX RT2660 VBAT_SS GPIO module configuration settings**

Instance	Parameter	Value	Description
GPIO	ADDR_WD	16	Peripheral slot is 64kB
GPIO	PIN_DIS	4	Derived from GPIO_NUM
GPIO	IRQ_DIS	0	Interrupts supported on all pins
GPIO	IRQ_NUM	2	Each pin assigned to one of two different interrupt vectors
GPIO	PROT_EN	1	Enables secure and privilege access protection per pin
GPIO	ASYNC_EN	1	Enables asynchronous register interface and asynchronous interrupt generation (does not require free running bus clock). Note that when this option is selected the register interface is compatible with APB and not AHB

6.9.5.2 IOCON

Pad configuration and pin muxing registers for the VBAT_SS supplied GPIO pins.

- Individual pull control fields with pullup, pulldown, and pull-disable support ;
- Individual PCRn[PFE] fields that enable and disable individual input passive filters ;
- Individual PCRn[ODE] fields that enable and disable individual open drain outputs ;
- Digital input inversion to optionally invert the digital input ;
- Individual electrical fast transient (EFT) detect with an EFT detect flag and associated interrupt ;
- Digital PCRn[IBE] fields to configure between analog or disabled functions and digital functions ;
- Individual PCRn[MUX] fields supporting GPIO and up to 3 chip-specific digital functions.

The IOCON of the i.MX RT2660 VBAT_SS shall be configured as follows.

Table 142. **i.MX RT2660 VBAT_SS IOCON module configuration settings**

Instance	Parameter	Value	Description
IOCON	ADDR_MSB	16	Peripheral slot is 64kB
IOCON	PIN_DIS	4	Derived from GPIO_NUM.
IOCON	PINPUS_RST	0	Pull select reset to pulldown
IOCON	PINPUE_RST	0	Pull select reset to disable
IOCON	PINPUV_RST	0	Pull value reset to normal
IOCON	PINSRE_RST	0	Slew rate reset to fast
IOCON	PINPFE_RST	0	Passive filter reset to disabled
IOCON	PINODE_RST	0	Open drain reset to disabled
IOCON	PINDSE0_RST	0	Drive strength reset to low
IOCON	PINDSE1_RST	0	Drive strength reset to low
IOCON	PINMUX_RST	0	Pin mux reset to ALT0

IOCON	PINIBE_RST	0	Input buffer reset to disabled
IOCON	PINPUS_DIS	0	Pull select implemented
IOCON	PINPUE_DIS	0	Pull enable implemented
IOCON	PINPUV_DIS	0	Pull value implemented
IOCON	PINSRE_DIS	TBD	Slew rate implemented
IOCON	PINPFE_DIS	0	Passive filter implemented
IOCON	PINODE_DIS	0	Open drain implemented
IOCON	PINDSE0_DIS	TBD	Drive strength implemented
IOCON	PINDSE1_DIS	TBD	Drive strength implemented
IOCON	PINMUX0_DIS	0	Up to 4 pin mux slots in VBAT domain
IOCON	PINMUX1_DIS	0	Up to 4 pin mux slots in VBAT domain
IOCON	PINMUX2_DIS	32'hffff_ffff	Up to 4 pin mux slots in VBAT domain
IOCON	PINMUX3_DIS	32'hffff_ffff	Up to 4 pin mux slots in VBAT domain
IOCON	PINIBE_DIS	0	Input Buffer implemented
IOCON	PININV_DIS	0	Pin Invert implemented
IOCON	PINAUX_DIS	32'hffff_ffff	Aux function not implemented
IOCON	PINLOCK_DIS	0	Lock implemented
IOCON	PINEFT_DIS	32'hffff_ffff	EFT function not implemented
IOCON	PINMUX_NUM	4	Limited pin muxing in VBAT domain
IOCON	CALIB_WD	1	Calibration not implemented
IOCON	CALIB_RST	0	Calibration not implemented
IOCON	ASYNC_EN	1	Enables asynchronous register interface (does not require free running bus clock).

6.9.6 Glue function

6.9.6.1 VBATCON

VBATCON is glue logic implemented within the VBAT_SS and interfaces the PMC_SS that resides in SYSCON. It implements the following functions:

- Latch the VBAT POR and provide to RESETCON. Negate only when the PMC_SS has powered up and acknowledged ;
- Latch the POR_b pin and provide to RESETCON. Negate only when the PMC_SS has powered up and acknowledged ;
- Latch the full deep power down (FDPD) request from POWERCON. Negate on any wakeup source that is generated within the VBAT_SS (incl. VBAT POR or POR_b pin) ;
- Force disable the PMC_SS DCDC/LDO regulators during full deep power down mode ;
- Force the PMIC_MODE pins to "11" in full deep power down mode; otherwise force the PMIC_MODE pins to "00" on any wakeup source that is generated within the VBAT_SS (including VBAT POR or POR_b pin); otherwise passthrough the PMIC_MODE pin value from POWERCON ;

6.10 Input Output (IO)

Blocking item for PDA

- The small-sized Synopsys IO pads have been selected for i.MX RT2660 as plan of record. Synopsys IO libraries do not implement all pad functions needed for i.MX RT2660, i.e. lacking some required pad functionality. Synopsys has provided a quotation for missing IO development, but NXP rated this as too expensive. The delayed i.MX RT2660 A0 tapeout may give room for internal IO development.

- Currently, chip lead is the DRI that is working with NXP IO team on building an internal pad development plan for i.MX RT2K products based on pad specifications as provided by SoC Arch. Sofar no pad specifications and no plan are confirmed for i.MX RT2660. Without these confirmations, the i.MX RT2660 PDA gate is blocked.

In this version of the SoC HW.AS, we have still assume to proceed with the Synopsys IOs – until a new plan of record is confirmed including confirmed pad specifications and development plan.

6.10.1 Input Output pads

The i.MX RT2660 shall make use of Synopsys 22FDX DesignWare IO library. The usage of the Synopsys IO library is motivated due to two main reasons: 1) available off-the-shelf small-sized IO libraries, 2) NXP 22FDX IO library not meeting i.MX RT functional- and small-area IO needs while an updated IO library prior to i.MX RT2660 A0 tapeout date is not confirmed (yet).

The Synopsys IO library offers the following main features.

- Staggered pad (165µm height) and inline pad (100µm height) placement supported ;
- Supports 1.8 V/2.5 V/3.3 V IO voltage for GPIO and Oscillator ;
- Supports Nominal 0.8 V core voltage and Over drive 0.9 V core voltage ;
- Supports independent Core and IO power sequencing ;
- Supports various metal stacks including 10M_2Mx_5Cx_1Jx_2Qx_LB metal stack ;
- Supports Staggered and Inline layout configurations ;
- Supports Flip-chip and Wire-bond packaging ;
- Supports regular and fail-safe IOs.

The Synopsys IO library does impose several restrictions to the i.MX RT products:

- IO core supply limited to 0.72V minimum, while i.MX RT2660 digital core supply can be as low as 0.585V during operation and down to 0.5V in retention ;
- No IOs available that support up to 250 MHz operation as needed for xSPI interface ;
- IO pads do not support an analog input option as part of the GPIO pad, but a dedicated (separate) analog pad part of the IO library ;
- No IO pad available that can be used as tamper pad and/or reset pad ;
- Synopsys' ESD & industrialization solution instead of NXP solution.

Table 143. IC requirements traceability: IO general requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_IOP_1-3	All IO pads are designed for wirebond package	Must have	Yes
iMXRT2660_IOP_1-4	All IO pads shall has no power sequencing restrictions	Must have	Open
iMXRT2660_IOP_1-5	All IO pads shall be operate with core voltage in the supported voltage range.	Must have	No, IO core supply from VDD_0V8

6.10.1.1 Medium-Speed 1.8V/3.3V GPIO pads

This is a programmable Bidirectional IO (DWC_GPIO33_STAG(INLINE)_BD_H/V) cell with IO voltage support of 3.3 V, 2.5 V and 1.8 V. Both staggered (165µm x 25µm) and inline (100µm x 41µm) IO cells are available.

The main features of the Bidirectional IO cell are:

- 3.3V/2.5 V/1.8 V IO voltage support ;

- Minimum IO core voltage of 0.72 ;
- Programmable Output drive current option to support different frequencies ;
- Programmable Input Schmitt trigger ;
- Maximum GPIO operating frequency is 200 MHz for 1.8V and 3.3 V IO voltage ranges ;
- Programmable input options (Weak pull-up/down, Bus keeper, plain) ;
- NAND-tree structure for boundary scan ;
- Supports independent Core and IO power sequencing with the use of Power Management Cell (DWC_GPIO33_STAG(INLINE)_BIASGEN_H/V).

Fig 77 shows the high-level functional block diagram.

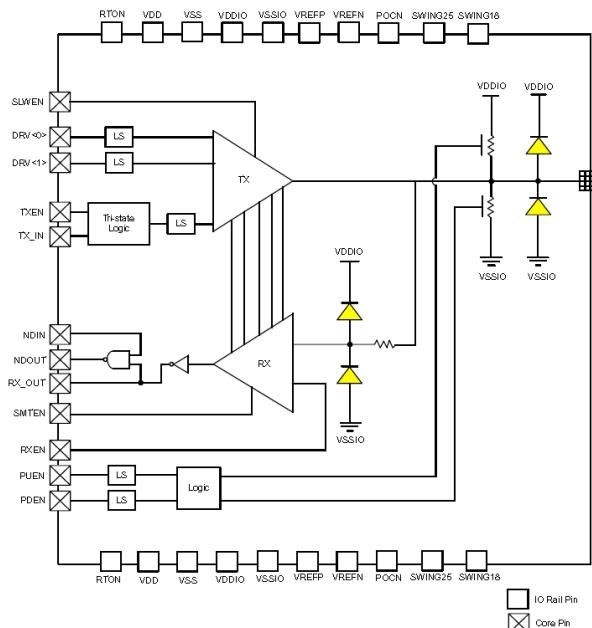


Fig 77. 1.8V/3.3V Bidirectional GPIO pad block diagram

This IO pad can be used in medium-speed general-purpose IO application up to 200 MHz without slew-rate controlled, and up to 100MHz with slew-rate controlled. It offers a general-purpose interface with full swing logic.

When IO core supply is turned off, the output of this IO pad is at High-Z state; state-retention is not supported. The typical pad leakage current is up to 22nA (VDD), and in addition 27nA (VDDIO) or 24nA (VDDIO) for 3.3V mode or 1.8 mode, respectively. Its maximum leakage is ~4.1 μ A (VDD), and in addition ~2.1 μ A (VDDIO) or ~3.4 μ A (VDDIO) for 3.3V mode or 1.8V mode, respectively.

For more information, please refer to the Synopsys 22FDX GPIO 3.3V databook [48].

Table 144. IC requirements traceability: 1.8V/3.3V LVCMOS GPIO pad requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_IOP_5-2	This IO pad shall support 1.8V nominal voltage and the full power supply range of 1.7V to 1.98V.	Must have	Yes, 1.62-1.98V
iMXRT2660_IOP_5-3	This IO pad shall support 3.3V nominal voltage and the full power supply range of 2.7V - 3.6V.	Must have	No, 2.97- 3.63V
iMXRT2660_IOP_5-4	This IO pad shall operate up to 100MHz.	Must have	Yes

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_IOP_5-5	This IO pad shall include programmable drive strength, 6-8mA and 10-12mA targets	Should have	Four options incl 6- & 12mA
iMXRT2660_IOP_5-6	This IO pad shall include programmable slew rate	Should have	Yes
iMXRT2660_IOP_5-7	This IO pad shall include selectable pull-up/pull-down, 50kohm	Must have	Yes
iMXRT2660_IOP_5-8	This IO pad shall include input buffer with selectable (enable/disable) hysteresis	Must have	Yes
iMXRT2660_IOP_5-9	This IO pad shall include state retention when core supply turned off	Must have	Not supported
iMXRT2660_IOP_5-10	Leakage current of this pad is less than 1uA.	Must have	~50nA typ

6.10.1.2 High-speed 1.8V/3.3V eMMC/SDIO pads

This IO pad (DWC_SDEMMC3318_BD_H/V) is designed to provide optimized I/O performance in 1.8V/3.3V eMMC/SDIO applications with a core voltage of 0.8V and overdrive voltage of 0.9V and supports IO supply voltage of 1.8V and 3.3 V. It makes use of a tall padframe (165µm x 55µm), compatible with the 1.8V/3.3V GPIO padframe and therefore can be placed in the same IO section.

This IO pad is not foundry sponsored and is available under a fee-based license.

Fig 78 shows the high-level functional block diagram.

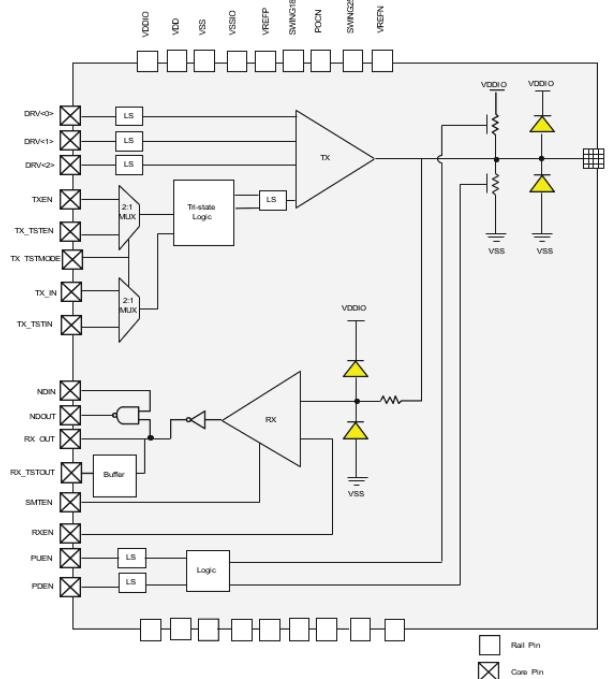


Fig 78. 1.8V/3.3V eMMC/SDIO pad block diagram

The main features of the 1.8V/3.3V eMMC/SDIO pad are:

- 1V8 and 3V3 signaling ;
- Compliant with eMMC 5.1 (JESD84-B51A) and SDIO 6.0 JEDEC Standard ;
- Supported Bus speed Modes are:
 - eMMC Modes
 - o Legacy SDR26: 3.3V/1.8V signaling, Frequency up to 26MHz ,up to 26MB/s
 - o HS-SDR/ SDR50: 3.3V/1.8V signaling, Frequency up to 52MHz ,up to 52MB/s

- HS -DDR/ DDR50: 3.3V/1.8V signaling, Frequency up to 52MHz ,up to 104MB/s
- HS200: 1.8V signaling, Frequency up to 200MHz ,up to 200MB/s
- HS400: 1.8V signaling, Frequency up to 200MHz ,up to 400MB/s
- SDIO Modes
 - Default Speed mode: 3.3V signaling , Frequency up to 25 MHz, up to 12.5 MB/s
 - High Speed mode: 3.3V signaling , Frequency up to 50 MHz, up to 25 MB/s
 - SDR12: UHS-I 1.8V signaling, Frequency up to 25 MHz ,up to 12.5 MB/s
 - SDR25: UHS-I 1.8V signaling, Frequency up to 50 MHz,up to 25 MB/s
 - SDR50/UHS50: UHS-I 1.8V signaling, Frequency up to 100 MHz,up to 50 MB/s
 - SDR104/UHS104: UHS-I 1.8V signaling, Frequency up to 208 MHz, up to 104 MB/s
 - DDR50: UHS-I 1.8V signaling, Frequency up to 50MHz ,sampled on both clock edges, up to 50MB/s
- Programmable input Schmitt trigger ;
- Programmable Weak pull-up/down ;
- Supports independent Core and IO power sequencing ;
- Programmable Speed Options.

This pad can be used in high-speed general-purpose IO application up to 208 MHz (1V8) and up to 50MHz (3V3). The pad is compliant with eMMC 5.1 (JESD84-B51A) and SDIO 6.0 JEDEC Standard. It further offers a general-purpose interface with full swing logic.

Synopsys does not support IOs that can run up to 250MHz at 1.8V – such IOs are required to support xSPI[1-2] pSRAM applications. However, this pad may suffice for the needed performance of the xSPI0 instance to support Flash applications.

Table 145. IC requirements traceability: 1.8V/3.3V eMMC/SDIO pad requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_IOP_7-2	This IO pad shall support 1.8V nominal voltage and the full power supply range of 1.7V to 1.98V.	Must have	1.67-1.95V
iMXRT2660_IOP_7-3	This IO pad shall support 3.3V nominal voltage and the full power supply range of 2.7V - 3.6V.	Must have	Yes, 2.7- 3.6V
iMXRT2660_IOP_7-4	This IO pad shall operate up to 250MHz at 1.8V.	Must have	No, up to 208MHz
iMXRT2660_IOP_7-5	This IO pad shall operate up to 133MHz at 3.3V.	Must have	No, up to 50MHz
iMXRT2660_IOP_7-6	This IO pad shall include programmable drive strength, 8-12mA and 15-20mA targets	Should have	Prog. drive strength via impedance control
iMXRT2660_IOP_7-7	This IO pad shall include programmable slew rate	Must have	Not supported
iMXRT2660_IOP_7-8	This IO pad shall include selectable pull-up/pull-down, 50kohm and 100kohm	Must have	Yes
iMXRT2660_IOP_7-9	This IO pad shall include state retention when core supply turned off	Must have	Not supported
iMXRT2660_IOP_7-10	Leakage current of this pad is less than 1uA.	Must have	~10uA max

6.10.1.3 High-speed 1.8V/3.3V MFIO pads

Synopsys does not support IOs that can run up to 250MHz at 1.8V – such IOs are required to support xSPI[1-2] PSRAM applications. This pad is required by i.MX RT2660 – currently no solution available, refer to aforementioned PDA gate blocking item.

NXP IO team is developing the SDIO3V3TF bidirectional I/O buffer in GF22FDXP technology utilizing a tall padframe ($165\mu\text{m} \times 50\mu\text{m}$). This IO padframe is not compatible with Synopsys IO padframes.

The design uses both thin gate oxide and thick gate oxide devices available in ten metal layers, including one ultra-thick metal. The cell also support general purpose bi-directional signaling at 1V8 and 3V3 voltages. The cell is designed to be used as clock and data interface for SD bus supporting up to SDR104 mode; it is designed to support 208 MHz max in 1.8V, and 166 MHz maximum frequency in 3.3V nominal signaling. **NXP IO team gave guidance that the performance of the cell could be beefed up to reach the 250MHz mark at 1.8V – OPEN.**

Fig 79 shows the high-level functional block diagram.

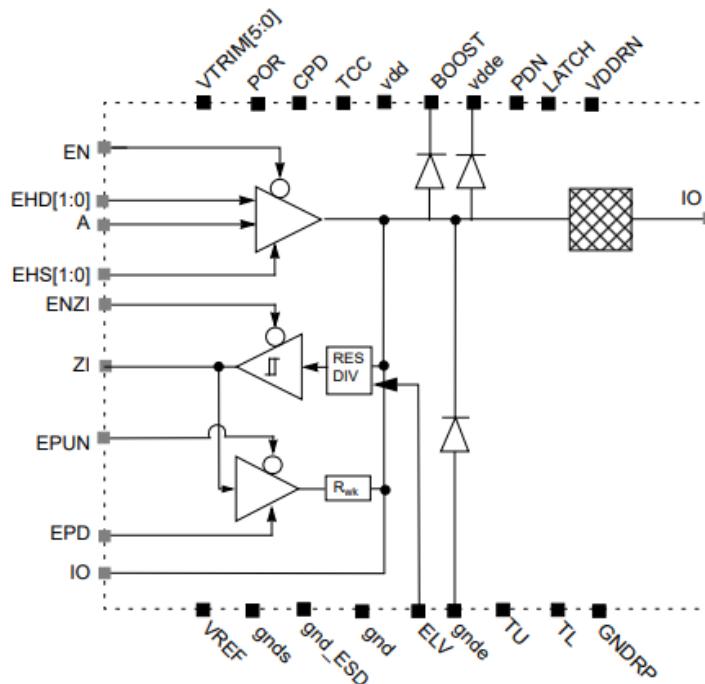


Fig 79. SDIO3V3TF 1.8V/3.3V pad block diagram

The main features of the 1.8V/3.3V SDIO pad are:

- 1V8 and 3V3 Signaling ;
- Tri-State output buffer ;
- Supports four drive modes (type- A,B,C,D) in accordance with SDIO specifications ;
- Programmable Speed Options ;
- Hysteresis receiver with receiver disable option ;
- Receiver state retention at IO power-down ;
- Programmable input options (pull-up, pull-down, repeater, or plain input) ;
- No power sequence requirement ;
- Core ground (gnd) isolated from substrate ;
- Antenna and CDM protection on all core side inputs.

This pad can be used in SD bus Interface meeting SDIO Specification for SDR104 mode. It also can be used in high speed general purpose IO application, offering a general-purpose interface with full swing logic.

Table 146. IC requirements traceability: 1.8V/3.3V LVC MOS IO pad for DDR clock requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_IOP_8-2	This IO pad shall support 1.8V nominal voltage and the full power supply range of 1.7V to 1.98V.	Must have	Yes, 1.62- 1.98V
iMXRT2660_IOP_8-3	This IO pad shall support 3.3V nominal voltage and the full power supply range of 2.7V - 3.6V.	Must have	No, 3.0- 3.6V
iMXRT2660_IOP_8-4	This IO pad shall operate up to 250MHz at 1.8V nominal.	Must have	No, 208MHz
iMXRT2660_IOP_8-5	This IO pad shall operate up to 133MHz at 3.3V nominal.	Must have	Yes, 166MHz
iMXRT2660_IOP_8-6	This module includes two pads and operates in two modes: - In SDR mode: two pads can be used as two high-speed GPIO pads have the same pad configuration. - In DDR mode, two pads can be used as pair of positive and negative clock signals to external memory device.	Must have	Open
iMXRT2660_IOP_8-7	This IO pad shall include programmable drive strength, 8-12mA and 15-20mA targets	Must have	Open
iMXRT2660_IOP_8-8	This IO pad shall include programmable slew rate	Must have	Open
iMXRT2660_IOP_8-9	This IO pad shall include selectable pull-up/pull-down, 50kohm and 100kohm	Must have	Open
iMXRT2660_IOP_8-10	This IO pad shall include state retention when core supply turned off	Must have	Open
iMXRT2660_IOP_8-11	Leakage current of this pad is less than 1uA.	Must have	Open

6.10.1.4 Open-Drain 1.8V/3.3V IO pads

Synopsys offers both I3C- and I2C open-drain IO pads, which are categorized as special pads that are not foundry sponsored and are available under a fee-based license. The I3C pad has been designed by INVECAS, and the 22FDX INVECAS IO Library IP has been acquired by Synopsys.

A.5 I3C pads

The INVECAS® I3C I/O library supports both push-pull and open-drain bi-directional I/O. An open-drain design requires an pull-up resistor to a high-voltage power supply. The sizing of resistor is application-dependent and varies with the load cap.

The I3C I/O library is designed for the I3C two-line interface and supports both push-pull and open-drain bi-directional I/O. An open-drain design requires an pull-up resistor to a high-voltage power supply. The following modes of operation are supported:

- I3C push-pull configuration supports a maximum frequency of 12.5MHz and drives up to 50pF load ;
- I3C open drain configuration supports a maximum frequency of 3MHz and drives up to 50pF load ;
- Legacy Open Drain configuration supports Fast mode (400kHz with 400pF) and Fast Mode Plus (1MHz with 550pF).

Note that the INVECAS I3C IO Library is not compatible with the Synopsys IO Library in terms of padframe

Fig 80 shows the high-level functional block diagram of the I3C IO pad.

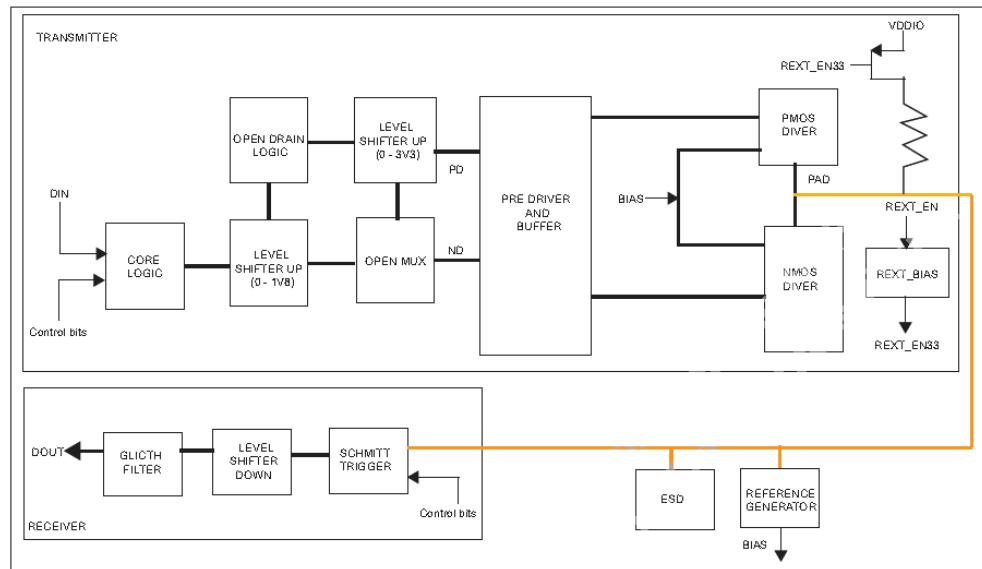


Fig 80. I3C pad block diagram

The main features of the I3C IO pad are:

- Supports Push-pull and Open drain I3C modes ;
- Support I2C Legacy Fast Mode and Fm+ Mode ;
- Specifications align with JEDEC Standard (mipi_I3C-Basic_specification_v1-0 '19July2018);
- Supports 1.8V/3.3V IO voltage ;
- Supports Schmitt Trigger ;
- 50 ns Filter for Spike rejection ;
- Supports Independent power supply sequence.

This pad can be used in low-speed IO applications. It offers an open-drain interface.

A.6 I2C pads

This IO pad is an open-drain bi-directional IO cell designed for the two-line I2C interface with a Pad tolerance up to 5 V. As an open-drain design, the I2C cell requires an external pull-up resistor to a power supply. The power supply (VBUS) for the pull-up is 1V8/3.3V and can go up to 5V in tolerant mode. VBUS is independent of IO power supply (VDDIO). The value of the external resistor is application-dependent and can be chosen based on the required rise time as per different BUS operating speed.

Both staggered (165µm x 44µm) and inline (100µm x 72µm) IO cells are available, compatible with the 1.8V/3.3V GPIO padframe and therefore can be placed in the same IO section.

The main features of the 1.8V/3.3V I2C pad are:

- 1V8 and 3V3 Signaling ;
- Compliance with JEDEC Standard (I2C-bus specification and User Manual - April 4, 2014) with I2C operating modes
 - Standard Mode: 100 kHz ;
 - Fast Mode: 400 kHz ;
 - Fast Plus Mode: 1 MHz ;
- 5V Fail-safe feature supported ;
- Fail-Tolerant feature supported
 - 5VFT (VDDIO=3.3V+/-10%, VPAD=5V+/-10%: No large current flow from VPAD) ;

- 3V3FT (VDDIO=1.8V+/-10%, VPAD=3.3V+/-10%: No large current flow from VPAD) ;
- 2V5FT (VDDIO=1.8V+/-10%, VPAD=2.5V+/-10%: No large current flow from VPAD) ;
- Input Schmitt trigger ;
- Filter of 50 ns for Spike rejection ;
- Supports independent Core and IO power sequencing.

This pad can be used in low-speed IO applications. It offers an open-drain interface.

Table 147. IC requirements traceability: I2C IO Pad requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_IOP_8-2	This IO pad shall have similar functionalities as Low-Speed GPIO pad 1.8V/3.3V with some modifications listed below	Must have	Yes
iMXRT2660_IOP_8-3	This IO pad shall include push pull/pseudo open-drain for standard, fast, and high-speed I2C operations	Must have	Open-drain
iMXRT2660_IOP_8-4	This IO pad shall include passive filter	Must have	Yes for spike rejection
iMXRT2660_IOP_8-5	This pad shall support all I2C modes, including HS-mode	Must have	No HS mode supported Open: Req. update ongoing

6.10.1.5 Low Voltage Differential Signaling Pads

The 1.8V LVDS (Low Voltage differential Signaling) library is used to build a LVDS based interface for high-speed interconnect applications. This library is designed to optimize I/O performance with a core voltage of 0.8V and overdrive voltage of 0.9V and supports IO supply voltage of 1.8V. It makes use of a tall padframe (120µm height), compatible with the 1.8V GPIO padframe and therefore can be placed in the same IO section.

The library contains an LVDS transmitter, LVDS receiver and a bandgap reference circuit that is used to supply the current reference for the transmitter/receiver. The LVDS IO library is compatible with the IEEE Std 1596.3-1996 and TIA/EIA - 644 -A.

This LVDS library is not foundry sponsored and is available under a fee-based license.

The main features of the 1.8V LVDS are:

- 1.8 V IO voltage ;
- Cells supported are LVDS TX, LVDS RX and BGR (Bandgap reference cell) ;
- LVDS TX @2 Gbps @2pF
 - Common mode 1.1V +/- 100 mV differential ;
- LVDS RX @3.6 Gbps; Low Power mode at 900 MHz
 - Common Mode range 0.2 V to VDDIO-0.2 V ;
- Input receiver sensitivity 75 mV peak differential without Hysteresis ;
- DC coupled LVDS ;
- Loop back option supported for both Pre/Post driver in LVDS TX ;
- Selectable Termination Impedance control in LVDS receiver ;
- Supports independent Core and IO power sequencing ;
- Power down mode to reduce leakage.

Table 148. IC requirements traceability: LVDS IO Pad requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_IOP_11-2	This IO pad shall conform to TIA/EIA-644-A Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuit Specification	Must have	Yes
iMXRT2660_IOP_11-3	This IO pad shall support 1.8V nominal	Must have	Yes
iMXRT2660_IOP_11-4	This IO pad shall operate up to 1.2GHz	Must have	Yes
iMXRT2660_IOP_11-5	This IO pad shall support selection of input/output function	Must have	Separate Tx/Rx pads
iMXRT2660_IOP_11-6	This IO pad shall be in tri-stated when IO supply or core supply is powered down	Must have	Yes
iMXRT2660_IOP_11-7	This IO pad shall operate without the need of an external resistor	Must have	Yes

6.10.1.6 VBAT_SS: Low-Leakage 1.8V/3.3V GPIO pads

This is a programmable Bidirectional IO (DWC_GPIO33_ULL_STAG(INLINE)_BD_H/V) cell with IO voltage support of 3.3V, 2.5V and 1.8 V. It makes use of a tall padframe (190µm x 45µm) or short padframe (120µm x 65µm), which are different than the aforementioned 1.8V/3.3V GPIO padframes.

Fig 78 shows the high-level functional block diagram.

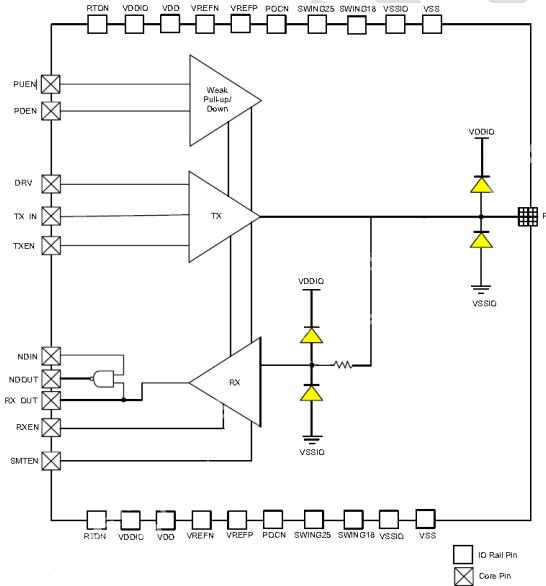


Fig 81. 1.8V/3.3V Bidirectional Low-Leakage GPIO pad block diagram

The following are the features of 3.3V Low-Leakage GPIO:

- 3.3V/2.5V/1.8V IO voltage support ;
- Minimum core voltage of 0.72V for low-power applications ;
- Typical VDDIO/VDD leakage <4nA in Standby mode (TT, 25°C, 3.3V/ 0.8V) ;
- Programmable o/p drive 8mA, 4mA (for 3.3V mode) ;
- Maximum operating Frequency of 50MHz at 3.3V with 15pF output load for maximum drive ;
- Programmable input Schmitt trigger ;
- Programmable input options (Weak pull-up/down, BUS-hold, Retention) ;
- NAND-tree structure for boundary scan ;
- Supports independent Core and IO power sequencing.

6.10.1.7 VBAT_SS: Tamper Pads

A tamper pad solution is currently not available – refer to PDA gate blocking item.

The purpose of the tamper detection mechanism is to provide evidence of any physical attempt to remove the device cover. The specific embedded mechanism drives to zeroing the sensitive date stored in the embedded memory.

Both passive and active tamper pad are required.

Table 149. IC requirements traceability: Tamper pad requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_IOP_11-2	This IO pad shall be used AON supply only.	Must have	Open
iMXRT2660_IOP_11-3	This IO pad shall support 1.8V input/output operation	Must have	Open
iMXRT2660_IOP_11-4	This IO pad shall include 200-300kohm pull-up/pull-down	Must have	Open
iMXRT2660_IOP_11-5	This IO pad shall include passive filter	Must have	Open
iMXRT2660_IOP_11-6	This IO pad shall has no latching or isolation	Must have	Open

6.10.1.8 Other Pads

Synopsys 1.8V/3.3V IO library supports the following other pads.

- Analog IO cells with HBM protection diodes connected between PAD to VDDIO/VSSIO ;
- Analog IO cells with HBM protection diodes connected between PAD to VDD/VSS ;
- Various 1.8V/3.3V supply cells for VDDIO and VDD ;
- Various ground cells for VSSIO and VSS ;
- Corner cells, splitter cells and filler cells of different widths (1µm, 5µm, 10µm, 20µm) ;
- Various IO interconnect cells that support interconnection between staggered and inline pad frames, between GPIO18 staggered and GPIO33 staggered pad frames and between GPIO18 inline and GPIO33 inline pad frames.

Table 150. IC requirements traceability: Other Pads requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_IOP_12-2	Analog pad for USB and RF	Must have	Yes, regular analog pads
iMXRT2660_IOP_12-3	1.2V/1.8V IO supply pad	Must have	Yes
iMXRT2660_IOP_12-4	1.8V/3.3V IO supply pad	Must have	Yes
iMXRT2660_IOP_12-5	Ground pad	Must have	Yes
iMXRT2660_IOP_12-6	Other basic cells such filler, corner, splitter, and bond pad, etc.	Must have	Yes

6.10.2 IO Pin Mux

The IO pinmux has been defined based on the following reference use-cases that are outlined in the i.MX RT2660 Requirement Specification (RS) document [2]. Refer to Appendix 14.

- Use-Case 1(A/B): Building Control ;
- Use-Case 2: Smart Home ;
- Use-Case 3: Backlight ;
- Use-Case 4: Camera Stabilizer ;
- Use-Case 5: Smart Door Lock ;

- Use-Case 6: Data Center Management ;
- Use-Case 7: Quad Motor Control ;
- Use-Case 8: Tactical Radio ;
- Use-Case 9: Automotive Smart Surface.

The pin mux configuration has been listed in the following file on RT2660 NPI Sharepoint:
[i.MXRT2660 IO ver 0.51.xlsx](#)

The pin mux configuration has been optimized for lowest pad count to keep the total IO required area as small as possible to minimize SoC die size impact.

In total, the pin mux configuration shows:

- An estimated total number of 290 pads for i.MX RT2660
- Up to 149 signal pads
 - 48 high-speed IO signal pads that shall operate up to 250 MHz ;
 - 93 medium-speed IO signal pads that shall operate up to 125 MHz ;
 - 8 low-speed IO signal pads that shall operate up to 10 MHz ;
- Up to 24 dedicated IO signal pads, including MIPI PHY pads, USB PHY pads, and other analog related pads ;
- An estimated total of 117 power/ground related pads, including accounting for the simultaneous switching IO requirements according to Synopsys guidelines.

The pin mux configuration has been developed by accounting for the pinout needs of 10 use-case scenarios that are listed in the i.MX RT2660 requirement specification [2]. From the assessed use-cases, Use-Case 1A, Use-Case 3, Use-Case 6 and Use-Case 7 are the ones that requiring most IO pins to be brought out as package pin. Table 151 shows a summary overview.

Table 151. **i.MX RT2660 estimated total amount of die pads and pins**

IO type	Total #pads	Total #pins	Utilized package pins per reference use-case								
			UC1A	UC1B	UC2	UC3	UC4	UC5	UC6	UC7	UC8
Multi-function IO	149	149	135	89	115	119	99	108	123	145	94
Dedicated IO	24	24	19	9	19	2	14	8	8	2	2
Power/Grounds	117	66	66	66	66	66	66	66	66	66	66
TOTAL	290	239	220	164	200	187	179	182	197	213	162
											155

OPEN: Pinmux update when Change Request gets accepted

- There seems to coming up a CR that requests for pin compatibility with RT1060 in a BGA196 package. This request seems to have a large implication on additional pad count (estimated impact of about +32 pads / +0.25mm²). Change Request is to be concluded.

7. Clock & Reset Architecture

This Chapter provides a description of the clock and reset architecture of the i.MX RT2660 SoC.

7.1 Clock architecture overview

Fig 82 shows the i.MX RT2660 clocking strategy which aims at minimizing power consumption of both clock generation and clock distribution by making use of distributed clock generation approach. A limited set of root clocks are generated by the CGU_SS that is located as part of SYSCON within the COMMON Domain.

The aforementioned root clocks are distributed to the MODCON IPs that are located locally within a subsystem. A CLOCKCON within the local MODCON takes care of generating the clock frequency for all sub-system building blocks - generally these clock frequencies are lower than the root clock.

Where applicable, the high-speed interface IP clocks as well as low-power peripheral IP clocks will be provided separately from the aforementioned main root clocks.

Fig 82. i.MX RT2660 SoC clock distribution strategy

To ensure maximum application flexibility on the usage of high-speed interfaces, the following high-speed interface IPs receive their own dedicated IP clock: XSPI, USDHC, USB, and ETH. Likewise, the low-power serial communication interfaces also received their own dedicated clock: I3C, I2C, SPI, UART, and CAN.

The following clock frequency tolerances have to be met for the peripherals listed in the table below. Note that this concerns the clock frequency tolerance at the peripheral clock input, i.e. end-to-end, from clock root via clock distribution net down to the peripheral clock input. In case of peripheral is not listed, there are no strict clock accuracy requirements.

Table 152. Required clock frequency tolerance for peripherals at peripheral side

Item	Supported frequency range	Typical frequency	Frequency offset	Clock accuracy requirement	Duty cycle requirement
xSPI IP clock	{500,400,333,320,267}MHz	500MHz 400MHz	±2%	±0.1%	50% ±4%
xSPIR IP clock	{267,200,160}MHz	267MHz	±2%	±0.1%	50% ±4%
uSDHC IP clock	{400,333,267}MHz	400MHz	±2%	±0.1%	50% ±4%
Ethernet RGMII	-	125MHz	-	±50ppm	50% ±5%
Ethernet RMII	-	50MHz	-	±50ppm	50% ±10%
Ethernet MII	-	25MHz	-	±100ppm	50% ±10%
USB HS PHY	{16,19.2,24,32,40}MHz	24MHz	-	±500ppm	50% ±10%
USB FS PHY (host mode)	48MHz	48MHz	-	±400ppm	-
USB FS PHY (device mode)	-	-	-	±0.5% (SOF trim)	-
DCIF Pixel Clock	5.85 MHz to 74.25 MHz	74.250MHz	-	±0.5%	-
MIPI D-PHY	24MHz to 200MHz	24MHz	-	±0.1%	50% ±10%

Table 153. IC requirements traceability: Clocking requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_CLK_1-4	The clock distribution should minimize the number of high frequency clocks and their routing distance in the SoC for power optimization.	Must have	Yes

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_CLK_1-5	This processor should implement extensive clock gating for power reduction.	Must have	<i>Targeted, to be confirmed during design phase</i>
iMXRT2660_CLK_1-6	Glitchless clock multiplexer implementation should minimize duty-cycle degradation.	Must have	Yes, refer to Fig 84
iMXRT2660_CLK_1-7	Most peripherals require fixed frequency clocks for their functional logics, such as generating the serial bit stream or reference timer. Therefore, peripheral functional clocks must be independent from the peripheral system bus clock, which can be changed during power mode transition.	Must have	Yes , see Sections 7.2 & 7.4
iMXRT2660_CLK_1-8	Each module that requires a functional peripheral clock should be assigned a separate clock multiplexer with source selection and programmable divider.	Must have	Yes , see Sections 7.2 & 7.4
iMXRT2660_CLK_1-9	High speed interfaces, like XSPI or SD/MMC host port, should have an independent high frequency clock source which can generate many frequency points. A PFD clock generated from PLL would satisfy this requirement.	Must have	Yes, see Error! Reference source not found.
iMXRT2660_CLK_1-10	The SoC should be partitioned in a way that high-speed IO interfaces, like XSPI or SD/MMCU host port, can maintain fixed frequency when the main SoC changes voltage level during DVS.	Must have	Yes, supported. See Error! Reference source not found.
iMXRT2660_CLK_1-11	A local generated low frequency clock, 8-12MHz, should be used as a clock option for peripherals in Low-power subsystem and audio subsystem in low power mode. For example, low power timer, analog comparator, ADC, and digital microphone are among peripherals need to operate down to Deep Sleep mode.	Must have	Yes , refer LPOSC12M

7.2 Clock Generation Unit subsystem (CGU_SS)

The clock generation unit subsystem (CGU_SS) contains the main clocking components: 1) clock sources and generated clock sources, and 2) clock slices for generating a main set of root clocks.

7.2.1 Clock sources

The following figure illustrates the input clock sources to the CGUANA, and the generated output clock sources to CLOCKCON.

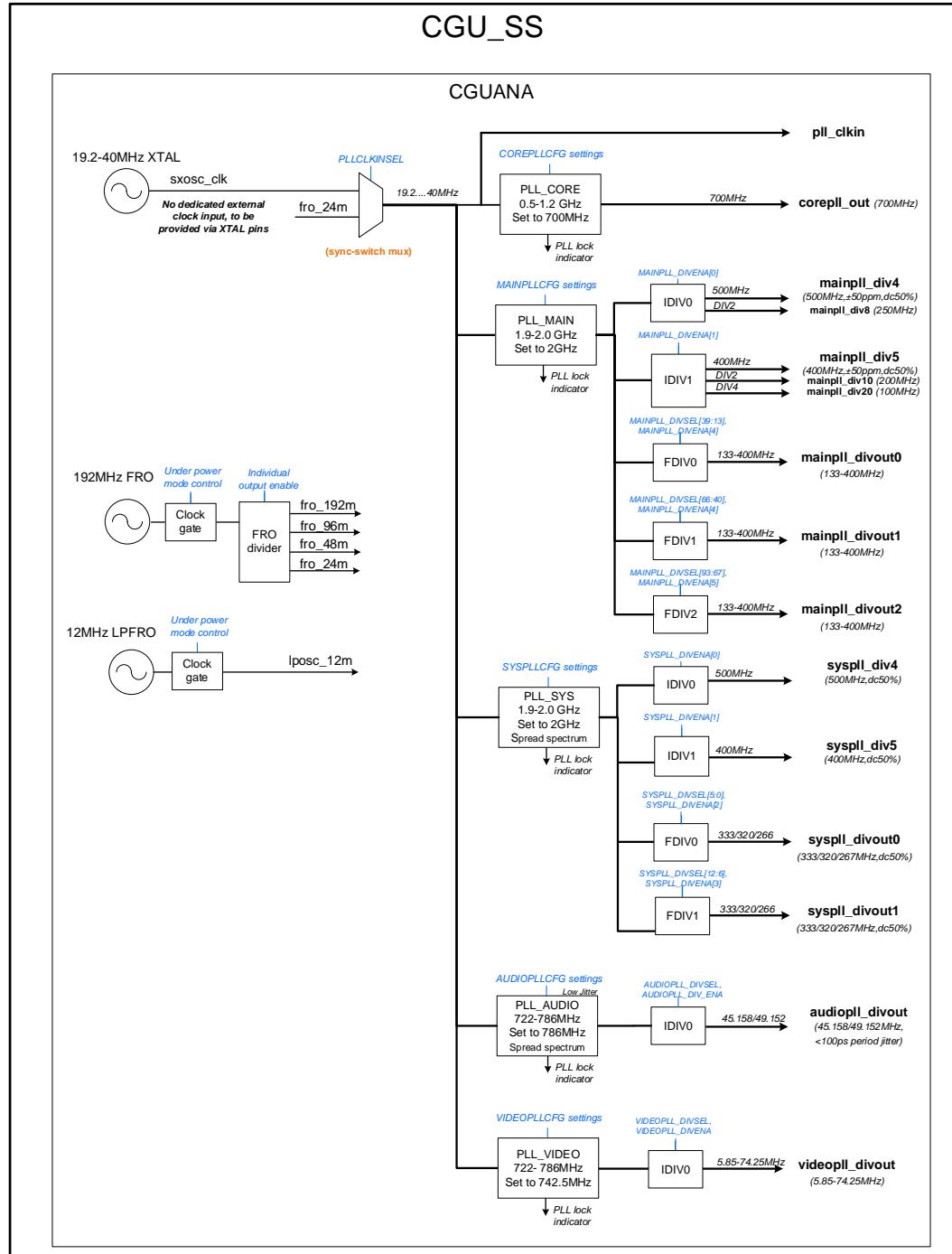


Fig 83. i.MX RT2660 CGU_SS clock sources block diagram

Glitch free clock switching is mandatory to ensure robust operation. Fig 84 shows an example schematic implementation of a glitch free clock switching multiplexer for two unrelated clocks. The design ensures that the new clock is not activated for few cycles after selection, while activation occurs during the clock low phase. This structure can be generalized for any number of clock

channels, e.g. for building a four-input glitch-free clock switching multiplexer. The impact on clock duty cycle when utilizing this structure is minimal.

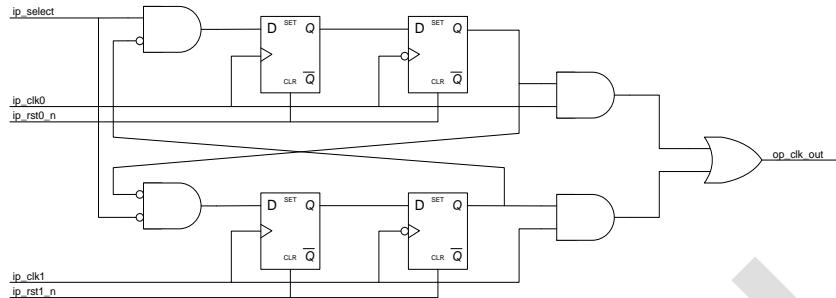


Fig 84. Example of a glitch free clock switch multiplexer of two unrelated clocks

Please Note, glitch-free clock switch required both clock source are available. For SXOSC_clk and fro_24m mux, even with glitch-free clock switch, the frequency/phase difference between SXOSC_clk and fro_24m may still result in PLL un-lock. By default, fro_24m is selected. If customer has crystal oscillator in PCB, customer should shift to SXOSC_clk before enable PLL.

Table 154. IC requirements traceability: Clock source requirements (part-I)

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_CLK_2-14	High frequency clock generated on-chip (400-500MHz) - A clock generated internally for core, bus, and peripherals for power saving.	Must have	Yes, Main PLL or System PLL +DIV{4 5}
iMXRT2660_CLK_2-15	Medium frequency clock generated on-chip (~200MHz) - A clock generated internally to be used as the default clock for core, bus, and peripherals.	Must have	Yes, Main PLL + DIV10
iMXRT2660_CLK_2-16	Low frequency clock generated on-chip (8-12MHz) - A clock generated internally to be used in low-power operation.	Must have	Yes, LPFRO12M
iMXRT2660_CLK_2-17	1MHz clock generated on-chip - A clock generated internally to be used as the system timer for the core. This clock may also be used in foundation IPs.	Must have	Yes, LPFRO1M as part of PMC_SS
iMXRT2660_CLK_9-1	PLLs	Heading	-
iMXRT2660_CLK_9-2	All PLLs should support reference input clock of 19.2MHz, 24MHz, 32MHz, and 40MHz	Must have	Yes
iMXRT2660_CLK_5-3	High frequency FRO	Heading	-
iMXRT2660_CLK_5-4	This clock should be used as a clock option for core, bus, and peripherals when PLLs are turned off for power saving.	Should have	Rejected non-significant power saving
iMXRT2660_CLK_5-5	This clock frequency shall be around 500MHz.	Should have	n/a
iMXRT2660_CLK_5-6	The FRO must meet frequency tolerance required by the supported peripherals.	Should have	n/a
iMXRT2660_CLK_5-7	The active current should be less than 150uA (typical).	Should have	n/a
iMXRT2660_CLK_5-8	The standby current should be less than 5uA (typical).	Should have	n/a
iMXRT2660_CLK_5-9	The start up time should be less than 0.5us.	Should have	n/a
iMXRT2660_CLK_6-1	Medium frequency FRO	Heading	-

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_CLK_6-2	This clock frequency should be around 200MHz. 192MHz FRO is preferred because it can generate 24MHz to be used as alternative reference clock to the PLLs.	Must have	Yes, FRO192M
iMXRT2660_CLK_6-3	This clock should be used as the default clock of CM85 core and system bus.	Must have	Yes
iMXRT2660_CLK_6-4	A 24MHz output clock from this FRO should be used as an alternative reference clock to all PLLs.	Must have	Yes see Fig 83
iMXRT2660_CLK_7-1	Low frequency FRO	Heading	-
iMXRT2660_CLK_7-3	This clock source should be used for peripherals operates in low power mode, for example, the low power timer or digital microphone in Deep Sleep mode. The 1MHz clock may be generated from this FRO.	Must have	Yes, LPFRO12M

7.2.1.1 System crystal oscillator

The system crystal oscillator (SXOSC) is used as the main input clock of the PLLs and USB PHY. It is designed to operate from a external crystal and support a bypass mode for applying an external clock via SXOSC input pin.

For the i.MX RT2660 SoC, the SXOSC shall support operation from crystal in the range of 19.2 MHz up to 40 MHz. The SXOSC shall be designed to support a wide range of crystal resonator within this frequency range. The SXOSC shall operate with the following reference crystal resonators.

Table 155. SXOSC list of reference crystal resonators

Supplier	Type number	Resonator frequency	Accuracy	Size
Murata	XRCGB24M000F2P91R0	24 MHz typ.	± 20ppm	2.0mm x1.6mm
TXC	8Q MHz Crystal	24-66 MHz	± 30/20/10ppm (25°C) ± 60ppm [-40,125]°C	1.6mm x 1.2mm

The following table shows the SXOSC IP key specification items; the targeted performance values are the result of the initial IP feasibility study.

Table 156. Targeted i.MX RT2660 SXOSC IP key specification items

Symbol	Parameter	Min	Typ	Max	Unit
T _{junction}	Operating temperature	-40	25	125	°C
V _{DD_1V8}	HV analog supply voltage	1.62	1.8	1.98	V
V _{DD_0V8}	LV analog supply domain	0.76	0.8	0.84	V
V _{DD_CORE}	Core (LV digital) regulated supply voltage	0.45	0.8	0.945	V
F _{osc}	Crystal frequency Range	19.2	24	40	MHz
F _{acc}	Frequency accuracy	-50		+50	ppm
F _{bypass}	Bypass frequency	16	24	80	MHz
I _{DD,osc}	DC current in steady state of OSC mode	0.3	0.6	mA	
I _{leak_1v8}	HV leakage current			10	µA
I _{leak_0v8}	LV leakage current			10	µA
t _{start}	Crystal startup time (ref. NDK 32MHz crystal)	0.3	2	ms	
t _{fast_start}	Crystal fast startup time (ref. NDK 32MHz crystal)	0.03	0.2	ms	

For further details and a more elaborated overview, please refer to the SXOSC IP-RS and IP-ES documents [49] [50].

Table 157. IC requirements traceability: system oscillator requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_CLK_3-4	The System oscillator, in conjunction with an external crystal or resonator, generates a high frequency reference clock for the SoC.	Must have	Yes, SXOSC
iMXRT2660_CLK_3-5	The System oscillator shall support input clock in the range of 16-40MHz.	Must have	19.2/24/32/40MHz (OSC), 16-40MHz (Bypass)
iMXRT2660_CLK_3-6	The System oscillator shall support input clock pass through the EXTAL pin when the external crystal or resonator is not used.	Must have	Yes, see Fbypass
iMXRT2660_CLK_3-7	The System oscillator clock shall be used as the main reference clock to the on-chip PLLs.	Must have	Yes, see Fig 83
iMXRT2660_CLK_3-8	The System oscillator clock should be used as a clock option for peripherals that require accurate clock.	Must have	Yes, see Fig 83

7.2.1.2 Medium-frequency FRO

The i.MX RT2660 SoC makes use of a medium-frequency 192MHz FRO which can be used for system clock as well as clock source for peripherals.

The interface of the FROs to the rest of the SoC shall be at VDD_CORE level. The 192MHz FRO shall be part of the CGU_SS.

Both 192MHz FRO shall be provisioned with trimming capabilities; this FRO shall support dynamic trimming capabilities via a frequency tuning function e.g. the FRO_TUNER function.

The following table shows the targeted FRO192M IP key specification items.

Table 158. Targeted i.MX RT2660 FRO192M IP key specification items

Symbol	Parameter	Min	Typ	Max	Unit
T _{junction}	Operating temperature	-40	25	125	°C
V _{DD_1V5}	Analog supply voltage	0.76	0.8	0.84	V
V _{DD_CORE}	Core (LV digital) regulated supply voltage	0.45	0.8	0.945	V
F _{osc}	Output clock frequency	96	192	240	MHz
F _{acc_temp}	Undivided Output Clock Frequency Accuracy Over Temperature After 1T-Trim	±1	±1.5	%	
F _{acc_vdd}	Undivided Output Clock Frequency Accuracy Over Supply Voltage After 1T-Trim	±0.5	±1	%	
F _{acc}	Undivided Output Clock Frequency Accuracy Over Temperature, Supply Voltage and Aging After 1T-Trim		±3.5	%	
F _{res}	Undivided output clock frequency resolution	0.1	0.5	%	
FOV	Frequency overshoot (at power up and during trim)		2	%	
DC	Output clock duty cycle – duty cycle correction disabled	45	50	55	%
I _{DD,FRO_0V8}	Active current consumption	125	250	μA	
I _{off}	Leakage current	5	10	μA	
t _{su}	Output frequency startup time – Fast startup disabled	40	60	μs	
t _{suf}	Output frequency startup time – Fast startup enabled	10	15	μs	

Table 159. IC requirements traceability: Medium frequency FRO requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_CLK_6-5	The FRO must meet frequency tolerance required by the supported peripherals.	Must have	IP verification during design phase

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_CLK_6-6	The active current should be less than 80uA (typical).	Must have	Not met
iMXRT2660_CLK_6-7	The standby current should be less than 5uA (typical).	Must have	Yes
iMXRT2660_CLK_6-8	The start up time should be less than 0.5us.	Must have	Not met

7.2.1.3 Low-frequency FRO

The i.MX RT2660 SoC makes use of two distinct low-power low-frequency FROs: a 12MHz Low-Power FRO (LPFRO12M) and a 1MHz Low-Power FRO (LPFRO1M). Both FROs are used a clock source to low-power peripherals.

The LPFRO12M is used as main clock source in Deep Sleep and optionally in Power-Down modes. The LPFRO12M and LPFRO1M are used as clock sources of low-power peripherals.

The interface of both FROs to the rest of the SoC shall be at VDD_CORE level. Both FROs shall be part of the CGU_SS. It can be acceptable when the LPFRO1M analog portion is implemented as part of the PMC_SS when the FRO related register map resides in the CGU_SS.

Both LPFRO12M and LPFRO1M shall be provisioned with trimming capabilities. It is currently not envisioned the LPOSC1M will make use of dynamic trimming capabilities like envisioned for LPFRO12M via the FRO_TUNER.

The following table shows the targeted LPOSC12M IP key specification items.

Table 160. Targeted i.MX RT2660 LPOSC12M IP key specification items

Symbol	Parameter	Min	Typ	Max	Unit
T _{junction}	Operating temperature	-40	25	125	°C
V _{DD_1V5}	Analog supply voltage	0.76	0.8	0.84	V
V _{DD_CORE}	Core (LV digital) regulated supply voltage	0.45	0.8	0.945	V
F _{osc}	Output frequency	1	12	12.288	MHz
F _{acc_temp}	Undivided Output Clock Frequency Accuracy Over Temperature After 1T-Trim	±1	±1.5	%	
F _{acc_vdd}	Undivided Output Clock Frequency Accuracy Over Supply Voltage After 1T-Trim	±0.5	±1	%	
F _{acc}	Undivided Output Clock Frequency Accuracy Over Temperature, Supply Voltage and Aging After 1T-Trim		±3.5	%	
I _{DD,osc}	Active current consumption	10	20	μA	
I _{off}	Leakage current	5	10	μA	
t _{start}	Output frequency startup time	10	20	μs	
t _{settling}	Output frequency settling time		50	μs	
DC	Duty cycle	45	55	%	

The following table shows the targeted LPOSC1M IP key specification items; this oscillator is part of the PMC_SS. The table below shows the targeted specification values of the LPOSC1M IP.

Table 161. Targeted i.MX RT2660 LPOSC1M IP key specification items

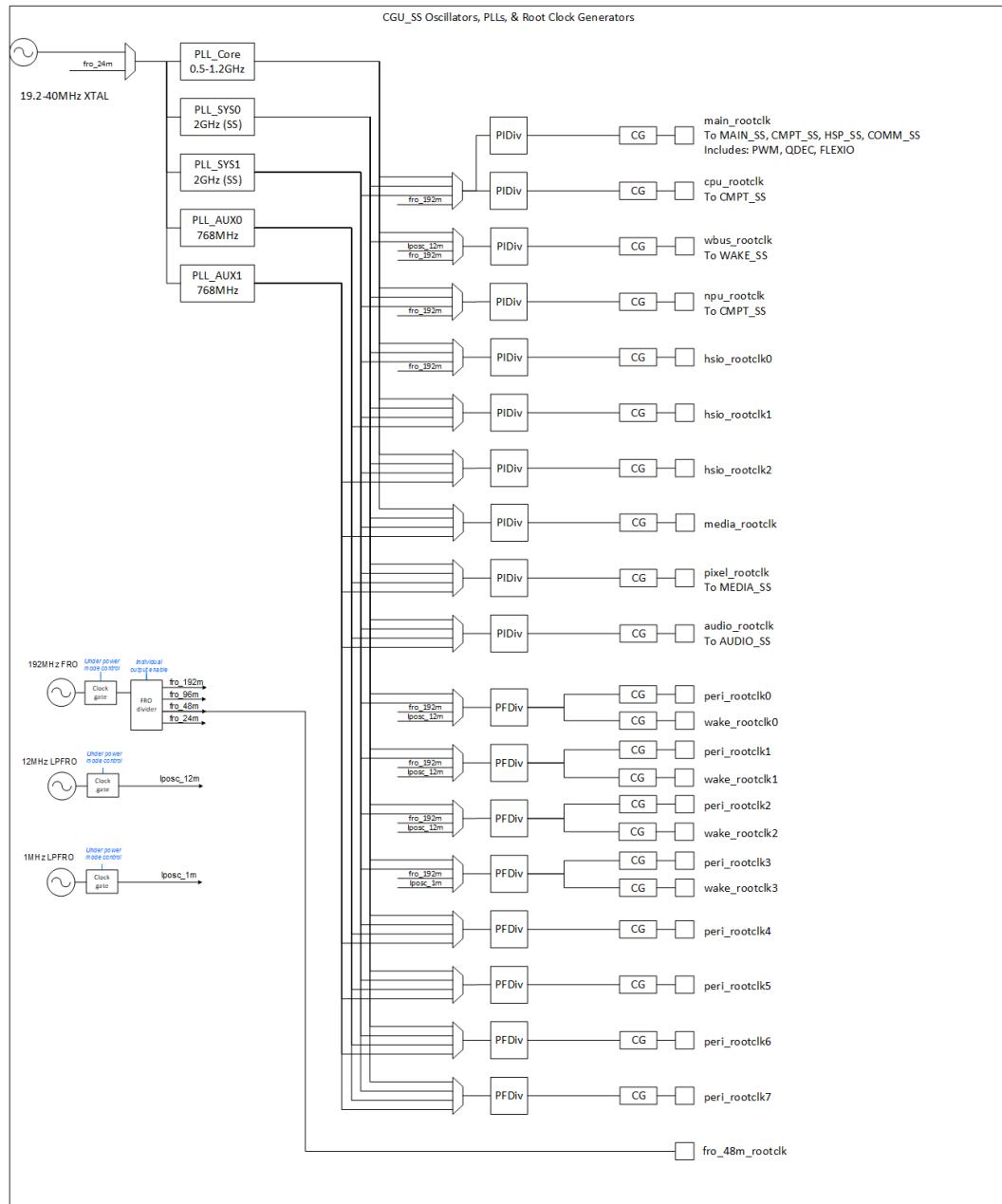
Symbol	Parameter	Min	Typ	Max	Unit
T _{junction}	Operating temperature	-40	25	125	°C
V _{DD_1V5}	Analog supply voltage	1.45	1.5	1.55	V
V _{DD_CORE}	Core (LV digital) regulated supply voltage	0.45	0.8	0.945	V
F _{osc}	Output frequency		1.024		MHz
ΔF _{osc_temp}	Output clock frequency accuracy over temperature	1	2	%	
F _{osc_overshoot}	Output clock frequency overshoot at startup		20	%	

$F_{osc_undershoot}$	Output clock frequency undershoot at startup	1	%
$\Delta F_{trim,step}$	Trim step	5	%
ΔF_{osc}	Trimmed output clock frequency accuracy over temperature, supply and aging	-5	+5 %
$I_{DD,osc}$	Active current consumption	1	μA
I_{off}	Leakage current at 85°C	100	nA
t_{start}	Output frequency startup time	150	400 ns
DC	Duty cycle	40	60 %

Table 162. IC requirements traceability: Low-frequency FRO requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_CLK_7-2	This clock frequency should be around 12MHz.	Must have	Yes, LPOSC12M
iMXRT2660_CLK_7-4	Active current should be less than 10uA.	Must have	Yes, 10uA
iMXRT2660_CLK_7-5	The standby current should be less than 2uA (typical).	Must have	Not met Open: Req. update ongoing
iMXRT2660_CLK_7-6	The start up time should be less than 0.5us.	Must have	Not met Open: Req. update ongoing
iMXRT2660_CLK_7-7	The FRO must meet frequency tolerance required by the supported peripherals.	Must have	IP verification during design phase

7.2.2CGU_SS Block Diagram



7.2.3CGU_SS interface

CGU_SS Interface

The CGU_SS includes a 32-bit APB target port for controlling register writes and reads to CGU.DIG. The CGU_SS generates the following outputs:

- main_rootclk: For clocking the MAIN_SS, CMPT_SS, the HSP_SS interconnect, and COMM_SS interconnect

- cpu_rootclk: For clocking the CPU core subsystem(s) inside CMPT_SS
- wbus_rootclk: For clocking the bus clocks in WAKE_SS
- emem_rootclk0: For clocking the xSPI and/or SRAMC interfaces (IO side)
- peri_rootclk0-7: For clocking functional clocks in the HSP_SS, AUDIO_SS, and COMM_SS
- wake_rootclk0-3: For clocking functional clocks in the WAKE_SS

In addition, depending on the particular device needs, the XEA_CGU_SS may generate the following clock root outputs

- npu_rootclk: For clocking the Neutron subsystem
- emem_rootclk1: An additional source for clocking XSPI and/or SRAMC interface IO
- media_rootclk: For clocking the MEDIA_SS interconnect, camera pipeline, display pipeline, GPU, JPEG, etc
- pixel_rootclk: For clocking the MEDIA_SS DCIF interface
- audio_rootclk: For clocking the AUDIO_SS interconnect and building blocks
- fro_48m_rootclk: Typically used for USB
- radio_rootclk: For clocking the RADIO_SS interconnect and building blocks. This clock is reserved for i.MXRT2520.

7.2.4 CGU_SS generated clocks

7.2.4.1 PLL_CORE, PLL_MAIN & PLL_SYS clocks

The i.MX RT2660 uses a three PLL approach for generating the required clock frequencies for system, core and high-speed communication interfaces (with the exception of USB and, audio and MIPI). The PLL_CORE is ONLY used for generating the main_rootclk. The PLL_SYS is only used for high-speed peripherals that require a spread spectrum modulated clock for EMI reduction. The PLL_MAIN is used to generate all other root clocks and is used to generate main_rootclk when PLL_CORE is turned off. All three PLLs shall be optimized for low power consumption. Table 163 shows the targeted use-case scenarios of three PLLs in the i.MX RT2660.

Table 163. Targeted PLL_CORE and PLL_MAIN usage in i.MX RT2660

IC MODE	PLL_CORE	PLL_MAIN	PLL_SYS
High-Performance Run	ON : used for main_rootclk only Optionally turn-off when $F \leq 500\text{MHz}$	ON	ON
Normal Run	OFF	ON	ON
Sleep		Optionally OFF	Optionally OFF
Deep Sleep	OFF	OFF	OFF
Power Down			
Deep Power Down			
Battery Backup			

Note: PLL_CORE can optional OFF, user must be noted about the PLL lock time so that user can balance power saving (if PLL lock time can be accepted) and PLL lock timer adder (if quick recovery is more important than power saving) in their use case.

The digital interface of the PLL to/from the rest of the SoC shall be at VDD_CORE level. All PLLs shall be implemented as part the CGU_SS macro block. Its related register map shall be located as part of the CGU_DIG.

The following table shows the PLL_CORE IP key specification items; the targeted performance values are the result of the initial IP feasibility study. The PLL_CORE will not support spread spectrum clocking technique for EMI reduction.

Table 164. Targeted i.MX RT2660 PLL_CORE IP key specification items

Symbol	Parameter	Min	Typ	Max	Unit
T _{junction}	Operating temperature	-40	25	125	°C
V _{DD_PLL_0V8}	LV analog regulated supply voltage	0.76	0.8	0.84	V
V _{DD_CORE}	Core (LV digital) regulated supply voltage	0.45	0.8	0.945	V
F _{PLL_CLKIN}	Input clock frequency	19.2	24	40	MHz
F _{CCO}	CCO usable frequency range	600		1200	MHz
F _{PLL_CLKOUT}	Output clock frequency	500	700	1200	MHz
D _{CCLKIN}	Input clock duty cycle	45	50	55	%
D _{CCLKOUT}	Output clock duty cycle	45	50	55	%
F _{PLLError}	Output clock frequency accuracy ¹ (Error from the target frequency when operating from crystal)	-50		+50	ppm
PER_jitter	Peak Period Jitter (from 1kHz to CLKOUT/2)	-3		+3	%peak
TIE_jitter	Short-term Peak TIE Jitter (10μs period, from 100kHz to CLKOUT/2)	-250		+250	pspeak
I _{DD_PLL_0V8}	LV active current when locked	300	600	μA	
I _{leak_PLL_0V8}	LV leakage current		10	μA	
t _{startup}	Startup time		25	μs	
t _{lock-freq}	Lock time (time from PLL enabled to output clock within specification)		50	μs	

¹ with crystal that offers ±50ppm operation or better

For further details and a more elaborated overview, please refer to the PLL_CORE IP-RS and IP-ES documents [51] [52].

The following table shows the PLL_MAIN IP key specification items; the targeted performance values are the result of the initial IP feasibility study. The PLL_MAIN will not support spread spectrum clocking technique for EMI reduction.

Table 165. Targeted i.MX RT2660 PLL_MAIN IP key specification items

Symbol	Parameter	Min	Typ	Max	Unit
T _{junction}	Operating temperature	-40	25	125	°C
V _{DD_PLL_0V8}	LV analog regulated supply voltage	0.76	0.8	0.84	V
V _{DD_CORE}	Core (LV digital) regulated supply voltage	0.45	0.8	0.945	V
F _{PLL_CLKIN}	Input clock frequency	19.2	24	40	MHz
F _{CCO}	CCO usable frequency range		2000		MHz
F _{PLL_CLKOUT_DIV4}	Output clock frequency CCO divided by 4		500		MHz
F _{PLL_CLKOUT_DIV5}	Output clock frequency CCO divided by 5		400		MHz
F _{PLL_CLKOUT_DIV6}	Output clock frequency CCO divided by 8		250		MHz
F _{PLL_CLKOUT_DIV10}	Output clock frequency CCO divided by 10		200		MHz
F _{PLL_CLKOUT_DIV20}	Output clock frequency CCO divided by 20		100		MHz
F _{PLL_CLKOUT_DIVOUT0}	Output clock frequency CCO fractionally divided utilizing 26 phases	133.3		400	MHz

$F_{PLL_CLKOUT_DIVOUT1}$	Output clock frequency CCO fractionally divided utilizing 26 phases	133.3	400	MHz
$F_{PLL_CLKOUT_DIVOUT2}$	Output clock frequency CCO fractionally divided utilizing 26 phases	133.3	400	MHz
DC_{CLKIN}	Input clock duty cycle	45	50	55 %
DC_{CLKOUT}	Output clock duty cycle (all outputs except divout2&-3)	48	50	52 %
DC_{CLKOUT}	Output clock duty cycle (divout2 & divout3)	48	50	52 %
$F_{PLLError}$	Output clock frequency accuracy ¹ (Error from the target frequency when operating from crystal)	-50	+50	ppm
PER_jitter	Peak Period Jitter – integer (from 100Hz to CLKOUT/2)	-3	+3	%peak
PER_jitter	Peak Period Jitter – fractional (from 100Hz to CLKOUT/2)	-6	+6	%peak
TIE_jitter	Short-term Peak TIE Jitter (10μs period, from 100kHz to CLKOUT/2)	-500	+500	pspeak
$I_{DD_PLL_0V8}$	LV active current when locked (PLL & all dividers active)	1600	3200	μA
$I_{DD_PLL_0V8}$	LV active current when locked (PLL only)	600	1200	μA
$I_{leak_PLL_0V8}$	LV leakage current		10	μA
$t_{startup}$	Startup time		25	μs
$t_{lock-freq}$	Lock time (time from PLL enabled to output clock within specification)		50	μs

¹ with crystal that offers ±50ppm operation or better

For further details and a more elaborated overview, please refer to the PLL_MAIN IP-RS and IP-ES documents [53] [54].

The PLL_SYS is a copy of PLL_MAIN, however, it shall be designed by making use of spread spectrum clocking technique for EMI reduction. The following table shows the PLL_SYS IP key specification items.

Table 166. Targeted i.MX RT2660 PLL_SYS IP key specification items

Symbol	Parameter	Min	Typ	Max	Unit
$T_{junction}$	Operating temperature	-40	25	125	°C
$V_{DD_PLL_0V8}$	LV analog regulated supply voltage	0.76	0.8	0.84	V
V_{DD_CORE}	Core (LV digital) regulated supply voltage	0.45	0.8	0.945	V
F_{PLL_CLKIN}	Input clock frequency	19.2	24	40	MHz
F_{CCO}	CCO usable frequency range		2000		MHz
$F_{PLL_CLKOUT_DIV4}$	Output clock frequency CCO divided by 4		500		MHz
$F_{PLL_CLKOUT_DIV5}$	Output clock frequency CCO divided by 5		400		MHz
$F_{PLL_CLKOUT_DIVOUT0}$	Output clock frequency CCO divided by 2 to 7.5 in steps of 0.25	266.7		1000	MHz
$F_{PLL_CLKOUT_DIVOUT1}$	Output clock frequency CCO divided by 2 to 7.5 in steps of 0.25	266.7		1000	MHz
DC_{CLKIN}	Input clock duty cycle	45	50	55	%
DC_{CLKOUT}	Output clock duty cycle (all outputs except divout2&-3)	48	50	52	%
DC_{CLKOUT}	Output clock duty cycle (divout2 & divout3)	48	50	52	%
$F_{PLLError}$	Output clock frequency accuracy ¹ (Error from the target frequency when operating from crystal)	-50	+50		ppm
PER_jitter	Peak Period Jitter – integer (from 100Hz to CLKOUT/2)	-3	+3		%peak
PER_jitter	Peak Period Jitter – fractional (from 100Hz to CLKOUT/2)	-6	+6		%peak
TIE_jitter	Short-term Peak TIE Jitter (10μs period, from 100kHz to CLKOUT/2)	-500	+500		pspeak
$I_{DD_PLL_0V8}$	LV active current when locked (PLL & all dividers active)	1600	3200		μA
$I_{DD_PLL_0V8}$	LV active current when locked (PLL only)	600	1200		μA

$I_{\text{leak_PLL_0V8}}$	LV leakage current	10	μA
t_{startup}	Startup time	25	μs
$t_{\text{lock-freq}}$	Lock time (time from PLL enabled to output clock within specification)	50	μs

¹. with crystal that offers $\pm 50\text{ppm}$ operation or better

For further details and a more elaborated overview, please refer to the PLL_MAIN IP-RS and IP-ES documents [53] [54].

Table 167. IC requirements traceability: Core/Ethernet/System PLL requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_CLK_10-1	Core PLL	Heading	-
iMXRT2660_CLK_10-2	This PLL is the main clock source for Cortex-M85 CPU and NPU. Multiple fractional dividers may be implemented to provide clock for bus and high-speed peripherals.	Must have	Yes, see Section 7.2.2
iMXRT2660_CLK_10-3	The VCO frequency range should be 500MHz - 1.2GHz (for future proof)	Must have	Yes, see PLL_CORE
iMXRT2660_CLK_10-4	The active current should be less than 5mA.	Must have	Yes, <600 μA PLL_CORE
iMXRT2660_CLK_10-5	CPU and NPU have relatively relaxed clock jitter requirement. However, if the Core PLL or its associated PFDs are used for peripheral interfaces, the Core PLL must meet frequency tolerance of those interfaces.	Must have	Yes, see PLL_CORE
iMXRT2660_CLK_13-1	Ethernet PLL	Heading	-
iMXRT2660_CLK_13-2	This PLL is primarily used for Ethernet interface. Fractional dividers may be implemented to provide additional clock sources to other peripherals.	Must have	Not needed MAIN_PLL +DIV{8 20}
iMXRT2660_CLK_13-3	The VCO frequency can be 500MHz.	Must have	n/a (PLL_MAIN)
iMXRT2660_CLK_13-4	The Ethernet PLL must meet Ethernet PHY typical frequency tolerance of $\pm 50\text{ppm}$.	Must have	Yes, see PLL_MAIN
iMXRT2660_CLK_13-5	The active current should be less than 3.5mA.	Must have	n/a (PLL_MAIN)
iMXRT2660_CLK_14-1	System PLL	Heading	-
iMXRT2660_CLK_14-3	The active current should be less than 3.5mA.	Must have	Yes, <3.2mA PLL_SYS
iMXRT2660_CLK_14-4	The PLL must meet frequency tolerance required by the supported peripherals.	Must have	Yes, see PLL_MAIN
iMXRT2660_CLK_14-5	This PLL shall support spread spectrum clocking technique for EMI reduction.	Must have	Yes, targeted for PLL_SYS

7.2.4.2 PLL_AUDIO & PLL_VIDEO clocks

The i.MX RT2660 uses dedicated PLL_AUDIO and PLL_VIDEO for generating the required clock frequency for audio subsystem and pixel clock of the media subsystem, respectively. The PLL_AUDIO is set to generate an output clock that is either a 16kHz sampling clock multiple, or a 44.1kHz sampling clock multiple. The audio clock provided to the AUDIO_SS is clock_gated, user should configure clock source and clock divider before clock gate off. The PLL_VIDEO is set to generate a pixel frequency as output clock e.g. 74.25MHz as default.

The PLL_AUDIO & PLL_VIDEO shall be optimized for low-jitter and good noise performance. This fractional PLL is designed by making use of spread spectrum clocking technique for EMI reduction.

The digital interface of the PLLs to/from the rest of the SoC shall be at VDD_CORE level. Both PLL_AUDIO and PLL_VIDEO instantiations shall be implemented as part of the CGU_SS macro block. Its related register map shall be located as part of the CGU_DIG.

The following table shows the PLL_AUDIO IP key specification items. The PLL_AUDIO shall with the jitter requirements based on AES-12id-2020 as shown in the table. The targeted performance values are the result of the initial IP feasibility study.

Table 168. Targeted i.MX RT2660 PLL_AUDIO IP key specification items

Symbol	Parameter	Min	Typ	Max	Unit
$T_{junction}$	Operating temperature	-40	25	125	°C
$V_{DD_PLL_0V8}$	LV analog regulated supply voltage	0.76	0.8	0.84	V
V_{DD_CORE}	Core (LV digital) regulated supply voltage	0.45	0.8	0.945	V
F_{PLL_CLKIN}	Input clock frequency	19.2	24	40	MHz
F_{CCO}	CCO usable frequency range	722.4		786.4	MHz
F_{PLL_CLKOUT}	Output clock frequency	45.158		49.152	MHz
DC_{CLKIN}	Input clock duty cycle	50		55	%
DC_{CLKOUT}	Output clock duty cycle	45	50	55	%
F_{PLLacc_ppm}	Output frequency accuracy offset	-100		+100	ppm
F_{PLLacc_Hz}	Absolute output frequency control (180.6-196.6MHz range)	-0.01		+0.01	Hz
Period jitter	RMS period jitter			100	ps(rms)
TIE jitter HP	RMS TIE High Pass (100Hz to 100MHz)			200	ps(rms)
TIE jitter BP	RMS TIE Band Pass (from 100Hz to 40kHz)			100	ps(rms)
LT jitter pk-pk	Long term jitter peak-peak		TBD		ps
$I_{DD_PLL_0V8}$	LV active current when locked	500	1000		µA
$I_{leak_PLL_0V8}$	LV leakage current			10	µA
$t_{startup}$	Startup time			50	µs
$t_{lock-freq}$	Lock time (time from PLL enabled to output clock within specification)			100	µs

For further details and a more elaborated overview, please refer to the PLL_AUDIO IP-RS and IP-ES documents [55] [56]. The PLL_VIDEO is based on the PLL_AUDIO, while only setting a different typical set frequency.

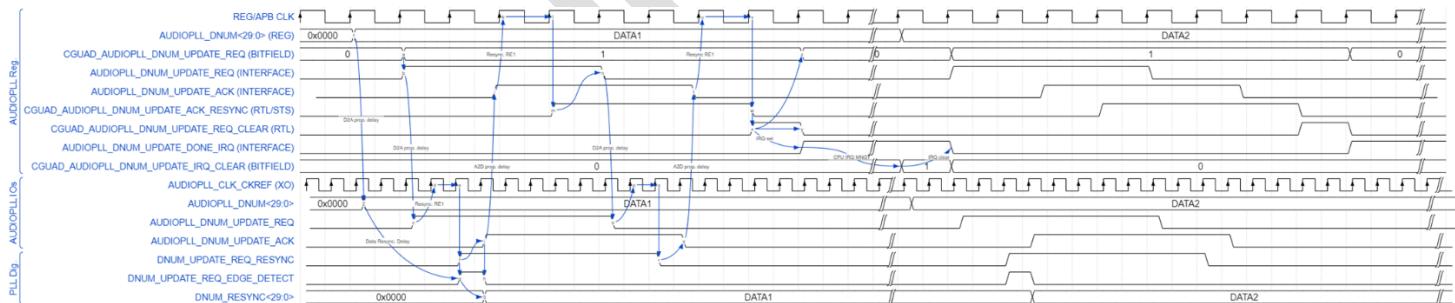
Table 169. Targeted i.MX RT2660 PLL_VIDEO IP key specification items

Symbol	Parameter	Min	Typ	Max	Unit
$T_{junction}$	Operating temperature	-40	25	125	°C
$V_{DD_PLL_0V8}$	LV analog regulated supply voltage	0.76	0.8	0.84	V
V_{DD_CORE}	Core (LV digital) regulated supply voltage	0.45	0.8	0.945	V
F_{PLL_CLKIN}	Input clock frequency	19.2	24	40	MHz
F_{CCO}	CCO usable frequency range	722.4	742.5	786.4	MHz
F_{PLL_CLKOUT}	Output clock frequency	5.85		74.25	MHz
DC_{CLKIN}	Input clock duty cycle	45	50	55	%
DC_{CLKOUT}	Output clock duty cycle	45	50	55	%
F_{PLLacc_ppm}	Output frequency accuracy offset	-100		+100	ppm
F_{PLLacc_Hz}	Absolute output frequency control (180.6-196.6MHz range)	-0.01		+0.01	Hz
$I_{DD_PLL_0V8}$	LV active current when locked	500	1000		µA
$I_{leak_PLL_0V8}$	LV leakage current			10	µA
$t_{startup}$	Startup time			50	µs
$t_{lock-freq}$	Lock time (time from PLL enabled to output clock within specification)			100	µs

Table 170. IC requirements traceability: Audio PLL requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_CLK_11-4	The output center frequency is an oversampling frequency of 16kHz, 32kHz, 48kHz, 96kHz, and 192kHz. The oversample factor is at least 256 or higher.	Must have	Yes, see Section Error! Reference source not found.
iMXRT2660_CLK_11-6	The output center frequency is an oversampling frequency of 44.1kHz. The oversample factor is at least 256 or higher.	Must have	Yes, see Section Error! Reference source not found.
iMXRT2660_CLK_11-8	This PLL shall support an adjustment step size less than 0.01Hz over supported range.	Must have	No, 0.01Hz step is not applicable. Even in RT10xx, we can only achieve 1Hz step with 32-bit FDIVm/32-bit DIVn.
iMXRT2660_CLK_11-9	The settling time and long-term jitter need to be specified to support high quality audio.	Must have	AES-12id-2020
iMXRT2660_CLK_11-10	The frequency update must be smooth with no glitches.	Must have	Yes, clock stop before frequency update
iMXRT2660_CLK_11-11	The active current should be less than 5mA.	Must have	Yes, <1mA PLL_AUDIO
iMXRT2660_CLK_11-12	This PLL shall support spread spectrum clocking technique for EMI reduction	Must have	Yes
iMXRT2660_AUD_1-12	Period jitter shall be better than 100ps RMS.	Must have	Yes, targeted
iMXRT2660_AUD_1-13	TIE base band jitter (3rd order 100kHz to 40kHz band-pass filtered) shall be better than 100ps RMS.	Must have	Yes, targeted
iMXRT2660_AUD_1-14	TIE wide band jitter (3rd order 100Hz high-pass filtered) shall be better than 200ps RMS.	Must have	Yes, targeted

The Audio PLL frequency update protocol for dynamic frequency adjustment is described in the timing diagram below:



The SW will have to write the new DNUM value when available in AUDIOPLL_DNUM register and write a "one" in CGUAD_AUDIOPLL_DNUM_UPDATE_REQ auto-clear bitfield to trig the update.

Then SW can either poll the same CGUAD_AUDIOPLL_DNUM_UPDATE_REQ to wait for the update to be performed, which will be indicated when the bitfield will be cleared by HW.

Or the AUDIOPLL_DNUM_UPDATE_DONE_IRQ interrupt signal may be used by interrupt controller at SOC level.

This corresponds to an asynchronous hand-shake protocol to manage PLL frequency update.

On the Audio PLL side, what will happen, is when DNUM_UPDATE_REQ_EDGE_DETECT signal will rise, the new DNUM value will be taken into account one PLL reference clock cycle later, the PLL will start locking to the new frequency without any clock interruption. It will be a smooth frequency transition from the previous frequency to the new one.

7.2.5 Root Clock Generators

The XEA_CGU_SS contains a root clock generator for each root clock it outputs. With some exceptions listed below, a root clock generator consists of:

TODO: Bullet

A 4-input MUX to select an oscillator or PLL source

A programmable clock divider, either integer or fractional

A clock gate [57]

7.2.5.1 i.MXRT2660 Clock Root Generator

See RT2660_Clock_v<version>.xlsx in share point [Clock](#)

7.2.5.2 CGU.cpu_rootclk Generator

The cpu_rootclk output of the XEA_CGU_SS provides the root clock to the CPU_SS0 inside XEA_CMPT_SS. This is typically the fastest clock on the SOC.

A CLKMUX4, referred to as CGU.cpu_root_mux, selects from the following inputs:

00: CGU.PLL_CORE

01: CGU.PLL_SYS0

10: CGU.PLL_SYS1

11: CGU.FRO192M

A Programmable Integer Divider, referred to as CGU.cpu_root_div, takes the output of the CGU.cpu_root_mux as the input clock and produces a divided output

A CLKGATE, referred to as CGU.cpu_root_gate, takes the output of CGU.cpu_root_div and generates a gated output root clock CGU.cpu_rootclk, [57]

7.2.5.3 CGU.main_rootclk Generator

The main_rootclk output of the XEA_CGU_SS provides the primary clock used by components and busses in MAIN_SS, CMPT_SS, HSP_SS, and COMM_SS.

A Programmable Integer Divider, referred to as CGU.main_root_div, takes the output of the CGU.cpu_root_mux as the input clock and produces a divided output

A CLKGATE, referred to as CGU.main_root_gate, takes the output of CGU.main_root_div and generates a gated output root clock CGU.main_rootclk

The CGU.main_rootclk is kept phase-aligned to the CGU.cpu_rootclk

7.2.5.4 CGU.wbus_rootclk Generator

The wbus_rootclk output of the XEA_CGU_SS provides the root clock to the WAKE_SS bus structure and non-IO peripherals

The wbus_rootclk is only used to clock portions of the WAKE_SS that are not powered in the lowest power states, and therefore the slowest clock included for input sources is the 12M FRO

A CLKMUX4, referred to as CGU.wake_root_mux, selects from the following inputs:

00: CGU.PLL_CORE

01: CGU.PLL_SYS0

10: CGU.LPOSC12M

11: CGU.FRO192M

A Programmable Integer Divider, referred to as CGU.wbus_root_div, takes the output of the CGU.wbus_root_mux as the input clock and produces a divided output

A CLKGATE, referred to as CGU.wbus_root_gate, takes the output of CGU.wbus_root_div and generates a gated output root clock CGU.wbus_rootclk [57]

7.2.5.5 CGU.npu_rootclk Generator

The npu_rootclk output of the XEA_CGU_SS provides the root clock to the Neutron Subsystem, NPU_SS, inside XEA_CMPT_SS

A CLKMUX4, referred to as CGU.npu_root_mux, selects from the following inputs:

- 00: CGU.PLL_CORE
- 01: CGU.PLL_SYS0
- 10: CGU.PLL_SYS1
- 11: CGU.FRO_192M

A Programmable Integer Divider, referred to as CGU.npu_root_div, takes the output of the CGU.npu_root_mux as the input clock and produces a divided output

A CLKGATE, referred to as CGU.npu_root_gate, takes the output of CGU.npu_root_div and generates a gated output root clock CGU.npu_rootclk [57]

7.2.5.6 CGU.emem0_rootclk Generator

The emem0_rootclk output of the XEA_CGU_SS provides the root clock to the external memory controllers such as XSPI, EMMC, SRAMC

A CLKMUX4, referred to as CGU.emem0_root_mux, selects from the following inputs:

- 00: CGU.PLL_CORE
- 01: CGU.PLL_SYS0
- 10: CGU.PLL_SYS1
- 11: CGU.FRO_192M

A Programmable Integer Divider, referred to as CGU.emem0_root_div, takes the output of the CGU.emem0_root_mux as the input clock and produces a divided output

A CLKGATE, referred to as CGU.emem0_root_gate, takes the output of CGU.emem0_root_div and generates a gated output root clock CGU.emem0_rootclk [57]

7.2.5.7 CGU.emem1_rootclk Generator

The emem1_rootclk output of the XEA_CGU_SS provides an alternate root clock to the external memory controllers such as XSPI, EMMC, SRAMC

The emem1_rootclk swaps the option of generating from the FRO192M with generating from the first Auxillary PLL. Having two root clocks options sourced from the same medium-speed source for high-speed devices is considered unnecessarily redundant, so this change provides greater flexibility

A CLKMUX4, referred to as CGU.emem1_root_mux, selects from the following inputs:

- 00: CGU.PLL_CORE
- 01: CGU.PLL_SYS0
- 10: CGU.PLL_SYS1
- 11: CGU.PLL_AUX0

If CGU.PLL_AUX0 is not present on a device, input 11 of the CLKMUX is changed to CGU.FRO192M

A Programmable Integer Divider, referred to as CGU.emem1_root_div, takes the output of the CGU.emem1_root_mux as the input clock and produces a divided output

A CLKGATE, referred to as CGU.emem1_root_gate, takes the output of CGU.emem1_root_div and generates a gated output root clock CGU.emem1_rootclk [57]

7.2.5.8 CGU.media_rootclk Generator

The media_rootclk output of the XEA_CGU_SS provides the root clock to the components and bus structure in the MEDIA_SS

The media rootclk includes an option to be generated from the same PLL that generates the pixel_rootclk output

A CLKMUX4, referred to as CGU.media_root_mux, selects from the following inputs:

- 00: CGU.PLL_CORE
- 01: CGU.PLL_SYS0

10: CGU.PLL_SYS1
11: CGU.PLL_AUX1

If CGU.PLL_AUX1 is not present on a device, input 11 of the CLKMUX is changed to CGU.PLL_AUX0

If both CGU.PLL_AUX1 and CGU.PLL_AUX0 are not present on a device, input 11 of the CLKMUX is changed to CGU.FRO192M

A Programmable Integer Divider, referred to as CGU.media_root_div, takes the output of the CGU.media_root_mux as the input clock and produces a divided output

A CLKGATE, referred to as CGU.media_root_gate, takes the output of CGU.media_root_div and generates a gated output root clock CGU.media_rootclk [57]

7.2.5.9 CGU.pixel_rootclk Generator

The pixel_rootclk output of the XEA_CGU_SS provides the root clock to the display interface module of the MEDIA_SS, which requires an accurate, specific clock frequency determined by the external display device, resolution, and frame rate

The pixel_rootclk is typically generated by the PLL_AUX1, but other sources are available for greater system flexibility

A CLKMUX4, referred to as CGU.pixel_root_mux, selects from the following inputs:

00: CGU.PLL_SYS0
01: CGU.PLL_SYS1
10: CGU.PLL_AUX0
11: CGU.PLL_AUX1

If CGU.PLL_AUX1 is not present on a device, input 11 of the CLKMUX is changed to CGU.FRO192M

If the device includes pixel_rootclk, then CGU.PLL_AUX0 must be present

A Programmable Integer Divider, referred to as CGU.media_root_div, takes the output of the CGU.media_root_mux as the input clock and produces a divided output

A CLKGATE, referred to as CGU.media_root_gate, takes the output of CGU.media_root_div and generates a gated output root clock CGU.media_rootclk [57]

7.2.5.10 CGU.audio_rootclk Generator

The audio_rootclk output of the XEA_CGU_SS provides the root clock to the AUDIO_SS, which requires a clock at a specific frequency based on the audio sampling rate

The audio_rootclk is typically generated by the PLL_AUX0, but other sources are available for greater system flexibility

A CLKMUX4, referred to as CGU.audio_root_mux, selects from the following inputs:

00: CGU.PLL_SYS0
01: CGU.PLL_SYS1
10: CGU.PLL_AUX0
11: CGU.PLL_AUX1

If CGU.PLL_AUX1 is not present on a device, input 11 of the CLKMUX is changed to CGU.FRO192M

If the device includes audio_rootclk, then CGU.PLL_AUX0 must be present

A Programmable Integer Divider, referred to as CGU.audio_root_div, takes the output of the CGU.audio_root_mux as the input clock and produces a divided output

A CLKGATE, referred to as CGU.audio_root_gate, takes the output of CGU.audio_root_div and generates a gated output root clock CGU.audio_rootclk [57]

7.2.5.11 CGU.peri_rootclk[0-3] Generator

The peri_rootclk[0-3] outputs of the XEA_CGU_SS provides the root clocks peripheral component functional clocks, such as SPI, UART, I2C, I3C, FLEXIO, CAN, and timers A set of CLKMUX4 blocks, referred to as CGU.peri_root_mux[0-3], select from the following inputs:

00: CGU.PLL_SYS0

01: CGU.PLL_SYS1
10: CGU.LPOSC12M
11: CGU.FRO192M

A set of Programmable Fractional Dividers, referred to as CGU.peri_root_div[0-3], takes the outputs of the CGU.peri_root_mux[0-3] as the input clocks and produces a divided outputs

A set of CLKGATE blocks, referred to as CGU.peri_root_gate[0-3], take the outputs of CGU.peri_root_div[0-3] and generate gated output root clocks CGU.peri_rootclk[0-3] [57]

7.2.5.12 CGU.peri_rootclk[4-7] Generator

The peri_rootclk[4-7] outputs of the XEA_CGU_SS provides the root clocks peripheral component functional clocks, such as SPI, UART, I2C, I3C, FLEXIO, CAN, and timers

A set of CLKMUX4 blocks, referred to as CGU.peri_root_mux[4-7], select from the following inputs:

00: CGU.PLL_SYS0
01: CGU.PLL_SYS1
10: CGU.PLL_AUX0
11: CGU.PLL_AUX1

If CGU.PLL_AUX1 is not present on a device, input 11 of the CLKMUX is changed to CGU.FRO192M

If CGU.PLL_AUX0 is not present on a device, input 11 of the CLKMUX is changed to CGU.LPOSC12M

A set of Programmable Fractional Dividers, referred to as CGU.peri_root_div[4-7], takes the outputs of the CGU.peri_root_mux[4-7] as the input clocks and produces a divided outputs

A set of CLKGATE blocks, referred to as CGU.peri_root_gate[4-7], take the outputs of CGU.peri_root_div[4-7] and generate gated output root clocks CGU.peri_rootclk[4-7] [57]

7.2.5.13 CGU.wake_rootclk[0-3] Generator

The wake_rootclk[0-3] outputs of the XEA_CGU_SS provides the root clocks peripheral component functional clocks inside the WAKE_SS, such as SPI, UART, I2C, I3C, FLEXIO, CAN, and timers

The wake_rootclk[0-3] outputs are identical to the peri_rootclk[0-3] outputs, but with independent clock gates to enable power savings when in sleep modes by gating off the peri_rootclk[0-3] to the higher speed systems while leaving peripheral clocks active for the WAKE_SS

A set of CLKGATE blocks, referred to as CGU.wake_root_gate[0-3], take the outputs of CGU.peri_root_div[0-3] and generate gated output root clocks CGU.wake_rootclk[0-3] [57]

7.2.5.14 Low-power system clock references

Fig 85 shows the clock slice block diagram of the low-power system clock references including the control of the clock input sources.

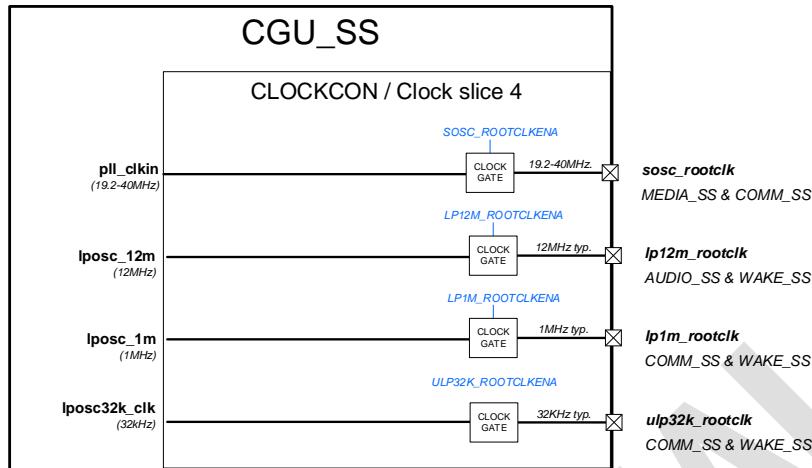


Fig 85. i.MX RT2660 CGU_SS clock slice diagram for the system clock references

The *sosc_rootclk* provides a system rootclock that is generated by the system crystal oscillator or by a 24MHz frequency as deduced from the 192MHz FRO. This clock is used in the MEDIA_SS and COMM_SS for MIPI D-PHY or USB PHY, respectively.

The *lp12m_rootclk* provides a system rootclock that is generated by the 12MHz low-power FRO. This clock is used in the AUDIO_SS as reference clock for the DMIC, or in the WAKE_SS as reference clock for I3C, LPI2C, LPUART and QTPM for lower-power use-cases.

The *lp1m_rootclk* provides a system rootclock that is generated by the 1MHz low-power FRO. This clock is used in the COMM_SS as USB wakeup reference clock as well as for timer purposes in the WAKE_SS.

The *ulp32k_rootclk* provides a 32 kHz system rootclock that is generated by VBAT, either 32 kHz crystal based or 32 kHz FRO based. This clock is used in the COMM_SS as USB wakeup reference clock or as reference clock to USDHC timers; in addition, this clock is also used for LPUART and timer purposes in the WAKE_SS.

7.2.6 Dedicated PLLs

7.2.6.1 USB PLL

High Speed USB PHY in COMM_SS has a build in 480MHz USB PLL. The USB PLL can generate a low jitter output clock of 480MHz from 16,19.2,24,30,32 MHz reference clock. It is an Integer-N synthesizer for which the frequency multiply factor should be: 30,25,20,16,15. The main features of the USB PLL are:

- Fast start up with PLL lock time of about 10 μ s typ. ;
- 9 Phases of VCO output. $F_{VCO} = F_{REF} * \text{selDiv}$;
- 1 Post divided output, divide values 1 through 6.

The maximum peak-to-peak period jitter is targeted to be 120ps max. The USB PLL power consumption is TBD.

In order to meet USB 2.0 specification, a data rate of 480 Mb/s \pm 500 ppm must be supported for USB High-Speed (HS). This means that a clock frequency accuracy of \pm 500 ppm must be supported; the clock duty cycle shall be lower than \pm 5%. The USB PLL shall be able to achieve this when the reference crystal clock has an accuracy \pm 100 ppm or below.

The USB PLL is integrated into the USB PHY IP. For more information, please refer to the DA_IP_HS_USB2_PHY_GF22FDX integration guide [40].

Table 171. IC requirements traceability: USB PLL requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_CLK_12-2	This PLL is primarily used for USB controller and PHY.	Must have	Yes
iMXRT2660_CLK_12-3	The VCO frequency is 480MHz.	Must have	Yes
iMXRT2660_CLK_12-4	The USB PLL must meet USB frequency tolerance of +/-50ppm.	Must have	Open
iMXRT2660_CLK_12-5	The active current should be less than 3.5mA.	Must have	Open
iMXRT2660_CLK_12-6	This PLL shall support spread spectrum clocking technique for EMI reduction	Should have	No

7.2.6.2 MIPI D-PHY PLL

The Mixel PLL is included in the MIPI D-PHY Tx. Its main specification parameters have been listed below.

Table 172. Mixel MIPI D-PHY PLL IP key specification items

Symbol	Parameter	Min	Typ	Max	Unit
T _{junction}	Operating temperature	-40		125	°C
V _{DD_PLL}	Analog supply voltage	0.72	0.8	0.88	V
V _{DD_HA}	IO analog supply voltage	1.62	1.8	1.98	V
F _{IN}	Input clock frequency before input divider	24		200	MHz
F _{FF}	Input frequency after input divider at FF point	24		50	MHz
F _{VCOUT}	VCO output frequency range	1250		2500	MHz
DC _{CLKIN}	Input clock duty cycle	35		70	%
DC _{CLKOUT}	Output clock duty cycle	45	50	55	%
I _{DD_PLL}	Power-up current V _{DD_PLL}		6.377	7.142	mA
I _{DD_HA}	Power-up current V _{DD_HA}		0.702	0.709	mA
I _{leak_PLL}	Power-down current V _{DD_PLL}		2.936	241.7	µA
I _{leak_HA}	Power-down current V _{DD_HA}		0.044	1.217	µA
t _{startup}	Startup time			2	µs
t _{lock-freq}	Time required for PLL to lock			5000	F _{FF} cycles

For further details, please refer to the Mixel's PLL Specification document [58]

7.2.7 Peripheral clock

See RT2660_Clock_v<version>.xlsx in share point [Clock](#)

7.3 VBAT Clocks

The i.MX RT2660 contains two ultra-low-power oscillators; the first one concerns a 32kHz crystal oscillator (OSC32K) and the other one a 32kHz free running oscillator (FRO32K). The 32kHz FRO is intended to be used as alternative clock source when the OSC32K frequency is not available. Although it does provide the similar clock frequency, its clock accuracy is limited as compared to a crystal based clock.

Fig 86 shows a high-level block diagram of the VBAT related clock sources as well as clock monitor, -control and selection circuitry. The 32kHz clock are utilized in the VBAT_SS by the Realtime Clock and wakeup timer.

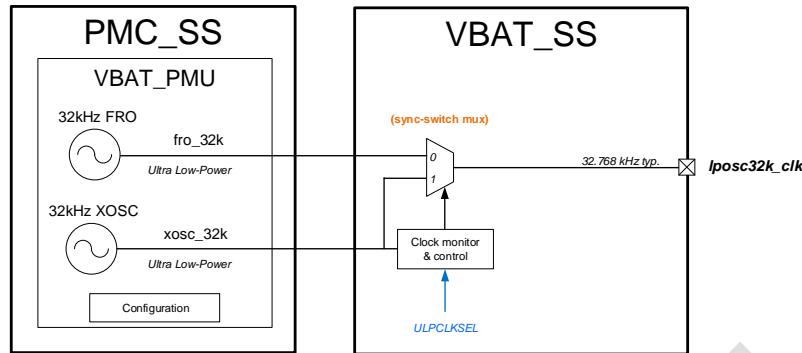


Fig 86. i.MX RT2660 VBAT clock sources block diagram

Both FRO32K and OSC32K clock sources reside within the VBAT_PMU, including its configuration registers. The consolidated clock output *iposc32k_clk* is provided to the CGU_SS, for further distribution within the SoC.

The FRO32K and OSC32K shall be designed to offer ultra-low power consumption. It shall be ensured that there always exists a 32kHz clock, i.e. either the FRO32K or OSC32K is running. When the OSC32K is not present or fails, the FRO32K shall provide the 32kHz clock. The clock monitor & control block shall ensure such functionality.

7.3.132KHz Crystal Oscillator (OSC32K)

The following table shows the OSC32K IP key specification items; the targeted performance values are the result of the initial IP feasibility study.

Table 173. Targeted i.MX RT2660 OSC32K IP key specification items

Symbol	Parameter	Min	Typ	Max	Unit
$T_{junction}$	Operating temperature	-40	25	125	°C
V_{DD_1V8}	HV analog supply voltage	1.62	1.8	1.98	V
V_{DD_CORE}	Core (LV digital) regulated supply voltage	0.45	0.8	0.945	V
F_{osc}	Crystal frequency		32.768		kHz
F_{acc}	Frequency accuracy	-500		+500	ppm
F_{bypass}	Bypass frequency	32		100	kHz
$I_{DD,xo32k.nano}$	VDD_1V8 power consumption at nano-power mode	50			nA
$I_{DD,xo32k.high}$	VDD_1V8 power consumption at high-power mode	500			nA
$I_{DD,clkmon}$	VDD_1V8 power consumption of clock monitor	30			nA
I_{leak_1v8}	VDD_1V8 leakage current when inactive			TBD	nA
t_{start}	Crystal startup time	25	2000		ms

For further details and a more elaborated overview, please refer to the XO32K IP-RS and IP-ES documents [59] [60].

7.3.232KHz Free Running Oscillator (FRO32K)

The following table shows the FRO32K IP key specification items; the targeted performance values are the result of the initial IP feasibility study.

Table 174. Targeted i.MX RT2660 FRO32K IP key specification items

Symbol	Parameter	Min	Typ	Max	Unit
$T_{junction}$	Operating temperature	-40	25	125	°C

V_{DD_1V5}	Analog supply voltage	1.8	V
V_{DD_CORE}	Core (LV digital) regulated supply voltage	0.45	0.8 0.945 V
F_{osc}	Output frequency	32	kHz
ΔF_{osc_temp}	Output clock frequency accuracy over temperature	1	2 %
$F_{osc_overshoot}$	Output clock frequency overshoot at startup	20	%
$F_{osc_undershoot}$	Output clock frequency undershoot at startup	1	%
$\Delta F_{trim,step}$	Trim step	5	%
ΔF_{osc}	Trimmed output clock frequency accuracy over temperature, supply and aging	-5	+5 %
$I_{DD,osc}$	Active current consumption	1	μ A
I_{off}	Leakage current at 85°C	100	nA
t_{start}	Output frequency startup time	150	400 ns
DC	Duty cycle	40	60 %

Table 175. IC requirements traceability: 32kHz FRO requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_CLK_8-3	Active current consumption must be less than 200nA.	Must have	To be confirmed
iMXRT2660_CLK_8-4	The start up time should be less than 120us.	Must have	Yes, targeted

7.4 Module Configuration

*For more detailed description of the MODCON,
please refer to the RT2660 System Control HW.AS document [10]*

The module configuration (MODCON) implements all device level module specific registers, including software resets, clock configuration, input trigger mux configuration and other module specific configuration registers. The registers are organized per module, rather than per function, to simplify software access and to enable fine grained access permissions for configuring the clocks and resets for each module. Each subsystem implements a physically separate MODCON module for the local modules implemented within each subsystem.

The MODCON registers are organized by peripheral and not by function. Each subsystem shall implement a separate MODCON instance to control the modules implemented within that subsystem. The following (superset) registers are to be implemented within MODCON for each module instance that requires SoC specific configuration registers:

- Access control
 - Controls which Domain ID can update the configuration registers for a given module instance ;
- Software reset
 - Allows software to assert the warm reset to the module ;
 - If a module implements a software reset, then there is separate control over the warm reset and software reset ;
 - If a module implements a cold reset, then there is software control over that reset but it shall default to disabled ;
- Bus initiator control
 - AXI bus initiators shall implement a control bit to block the acceptance of new AXI transactions by the AXI bus fabric and a status bit to indicate when all accepted AXI transfers have completed ;

- This function can use the NIC-400 low power interface if desired ;
- Software shall use this function before asserting the software reset to an AXI bus initiator to guarantee there are no in-flight AXI transactions in the bus fabric when the module is reset ;
- These bits are optional but recommended for AHB bus initiators.
- Low Power Clock Gating
 - Clock configuration to configure if module clock is disabled, enabled when CPU is active (e.g. gated in sleep mode), enabled when subsystem is active (gated in deepsleep mode) or if functional clock is always enabled ;
 - If dynamic or architectural clock gating is supported by the module, then one or more override bits to force clocks enabled (default disabled) ;
 - If clock gating handshake is supported by the module, then option to mask the clock gating handshake ;
- Clock Slice configuration
 - Functional clock mux select and clock divider ;
- Configuration module inputs to be controllable by software at device level
 - If any (module specific) ;
 - An example implementation of this field is software configuration of the vector base address register for a core ;
- Status module outputs to be made readable by software at device level ;
 - If any (module specific).

The actual clock divider, clock mux and clock gates may be implemented in MODCON or in a separate clock generation module provided that they are both implemented in the same subsystem as the module.

Phantoming of a module instance shall be supported by a dedicated input which can block write access to that module's configuration registers. Phantoming is therefore only supported for modules that default to disabled.

The i.MX RT2660 contains six MODCON IPs:

- MODCON_CMPT: module configuration of CMPT_SS ;
- MODCON_MAIN: module configuration of MAIN_SS ;
- MODCON_MEDIA: module configuration of MEDIA_SS ;
- MODCON_AUDIO: module configuration of AUDIO_SS ;
- MODCON_COMM: module configuration of COMM_SS ;
- MODCON_WAKE: module configuration of WAKE_SS .

This following sections describe the MODCON IPs with a focus on the clock related portion. The MODCON IPs make use of a multiplexer for clock selection, and a unified clock divider that supports divider ratios from 1 up to 128. The need for such unified divider is on request of the SW team, to ensure clock programming model compatibility versus the legacy i.MX RT1180 product.

For detailed clock slices, reference to RT2660_Clock_v<version>.xlsx in share point [Clock](#)

7.5 Subsystem clock interconnect

7.5.1 ASRC system diagram

Fig 87 shows the ASRC system overview for the i.MX RT2660 SoC.

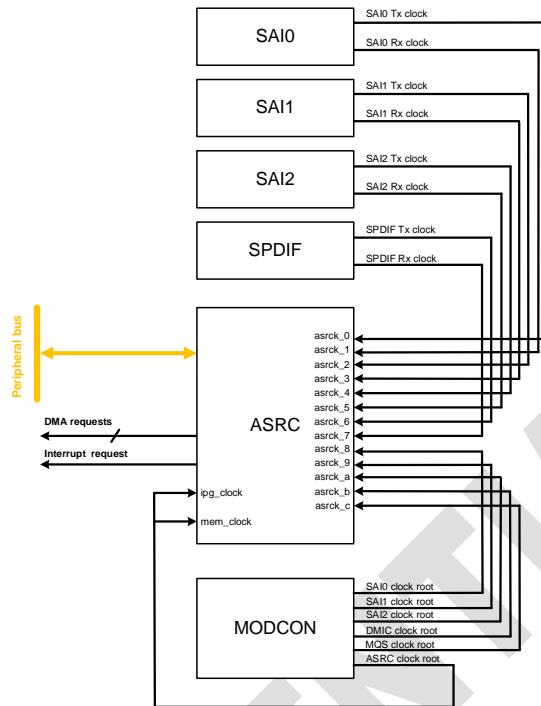


Fig 87. ASRC system overview of the i.MX RT2660

The ASRC is connected to the SoC is as follows:

- The sampling rate clocks are directly connected to the ASRC block. The ratio estimation of the input clocks with output clocks are done in ASRC hardware when both input/output sampling clocks are physically available ;
- When both the input sampling clock and the output sampling clock are physically available, the rate conversion can work by configuring the physical clocks ;
- When the input sampling clock is not physically available, the rate conversion can still work by setting ideal-ratio values into ASRC interface registers ;
- The clock signals come from the following blocks:
 - SAI, receiving bit clock and transmitting bit clock ;
 - SPDIF XCVR, receiving bit clock and transmitting bit clock ;
 - SAI, DMIC or MQS clock roots.
- The Digital Servo Loop (DSL) is a digital PLL for tracking the relationship between input/output sampling clocks. It is shared among all pairs in a first-come-first-serve form ;
- The exchange of audio data is done by the processor accessing ASRC block through registers defined on shared peripheral bus.

7.5.2 IP wrapper clock connectivity

This section description the local clock connectivity needs around IP that shall become part of the the wrapper around the related IP.

7.5.2.1 MAIN_SS IP wrappers

The following figure shows the clock connectivity for the xSPI IP that shall be part of the xSPI IP wrapper.

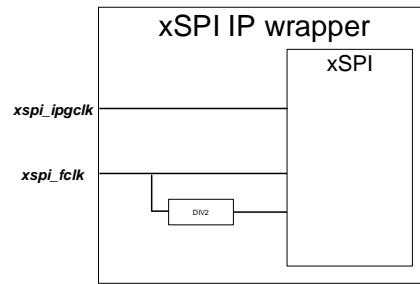


Fig 88. MAIN_SS IP wrapper clock connectivity

7.5.2.2 AUDIO_SS IP wrappers

The following figure shows the clock connectivity for the AUDIO_SS IP that shall be part of IP wrappers.

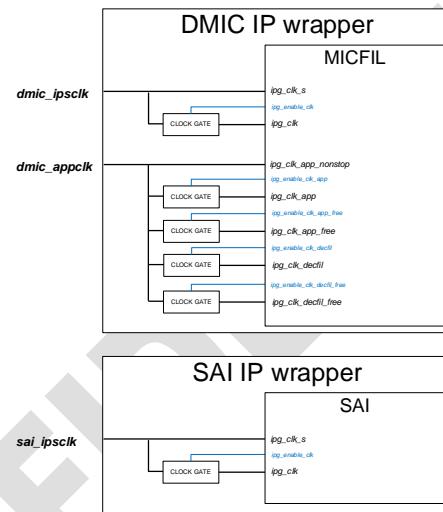


Fig 89. AUDIO_SS IP wrapper clock connectivity

7.5.2.3 COMM_SS IP wrappers

The following figure shows the clock connectivity for the COMM_SS IP that shall be part of IP wrappers.

The 480MHz PLL shall output a 48MHz clock that shall be capable to provide one of the input clock options for the USB1 FS IP. This has been illustrated in the corresponding USB[0-1] wrapper diagrams.

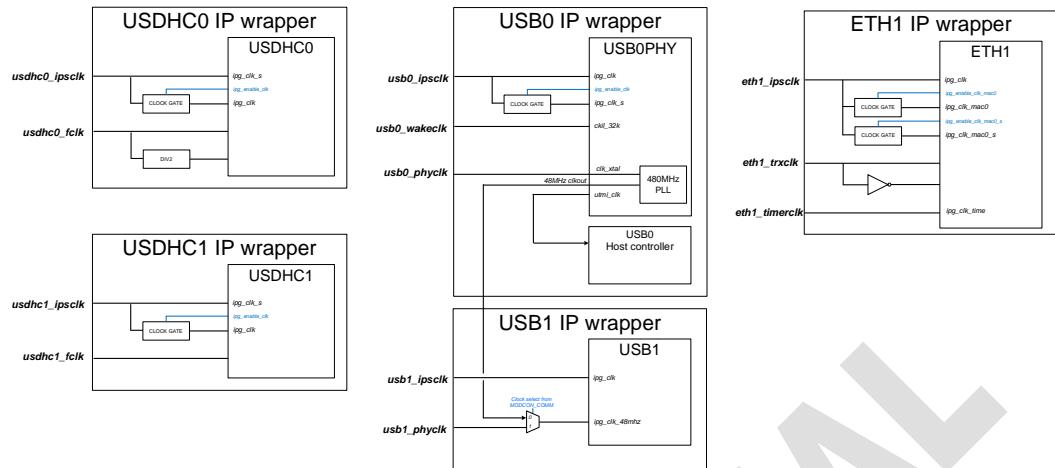


Fig 90. COMM_SS IP wrapper clock connectivity

To provide flexibility for Ethernet 1G/100M/10M modes, the following logic may be required for ETH0 module (TSN). This logic may be re-used from i.MX RT1170.

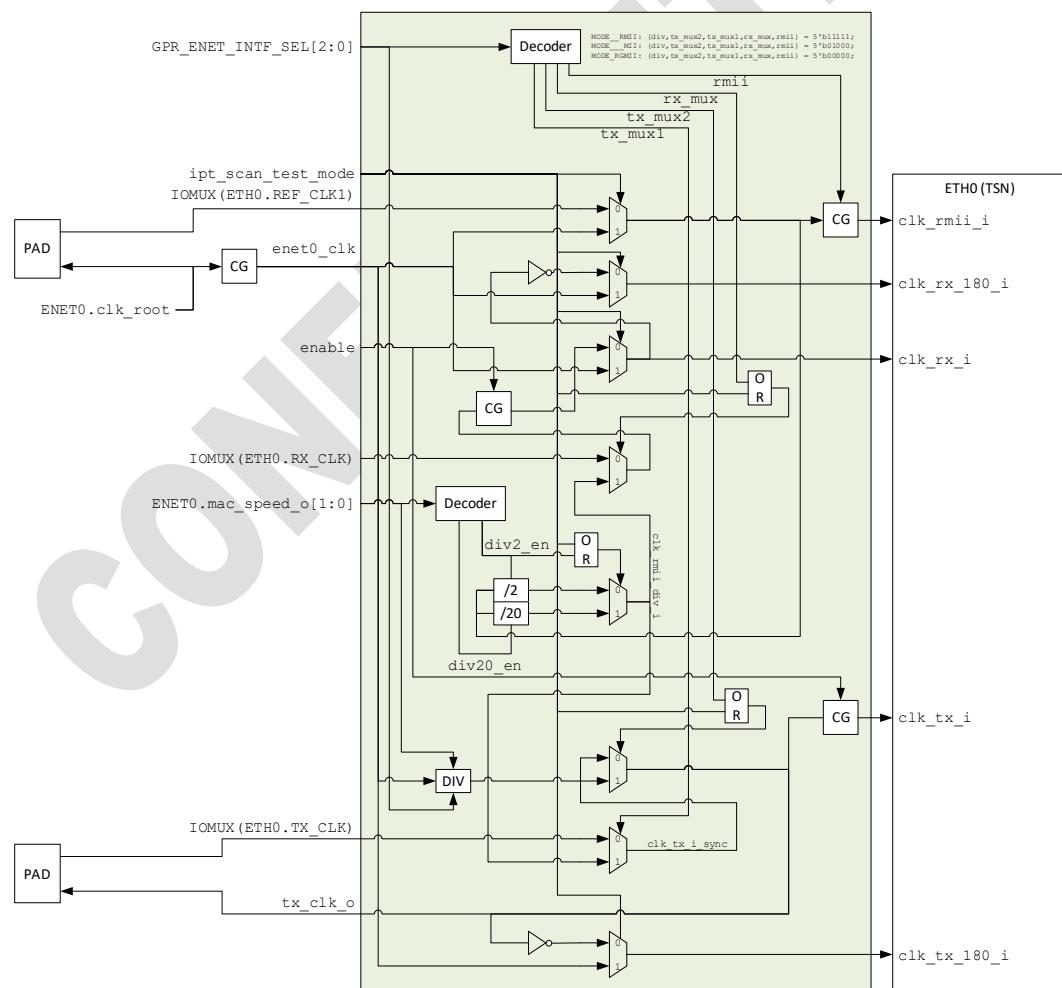


Fig 91. ETH0 wrapper logic for MAC clock

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7.6 Reset architecture overview

Generally, there exists two main types of resets that can be distinguished, namely a cold reset and a warm reset. A cold reset refers to a reset that asserts when the device first powers up or whenever a power domain is powered up. Cold resets are generally used to reset logic that survives a warm reset event, such as debug logic, clock/reset/power control and RTC/tamper pin related functions. A warm reset refers to a reset that asserts for any functional reason, this can include watchdog timeout, software request or other event. Warm resets are generally used to reset most of the SoC logic.

The i.MX RT2660 reset architecture is based on the proposed components of the XEA-1 platform. The i.MX RT2660 reset architecture makes use of following main components:

- Internal reset sources
 - A power-on-reset in the VBAT domain acts as cold reset source for all power domains;
 - Power-on-reset and voltage monitors within the PMC_SS monitor the PMC_SS related voltage rails and act as cold reset source for all domains except for the VBAT domain;
 - Warm resets initiated by watchdog timeout, software request or other events like debug related reset.
- External reset sources
 - An input-only POR_B pin in the VBAT I/O domain can act as cold reset source for all domains, except for the VBAT domain;
 - A bidirectional RESET_B pin in the debug I/O domain can act as warm reset source for all domains.
- A reset controller (RESETCON) that collates both internal and external reset sources, and distributes the system reset sources. The RESETCON is located within the SYSCON subsystem;
- Multiple power domain controller (PDCON) slices that sequences the local resets together with power control sequencing for each power domain based on received inputs from RESETCON and POWERCON.

Fig 92 shows the high-level overview of the reset architecture of the i.MX RT2660.

The i.MX RT2660 reset architecture is acting in close collaboration with the i.MX RT2660 power architecture. The collaborating components are: 1) the reset controller (RESETCON), 2) the power domain controller slices (PDCON), 3) the power mode controller (POWERCON), and 4) the VBAT controller (VBATCON). A detailed description of the i.MX RT2660 power architecture including the power domains can be found in Chapter 8.

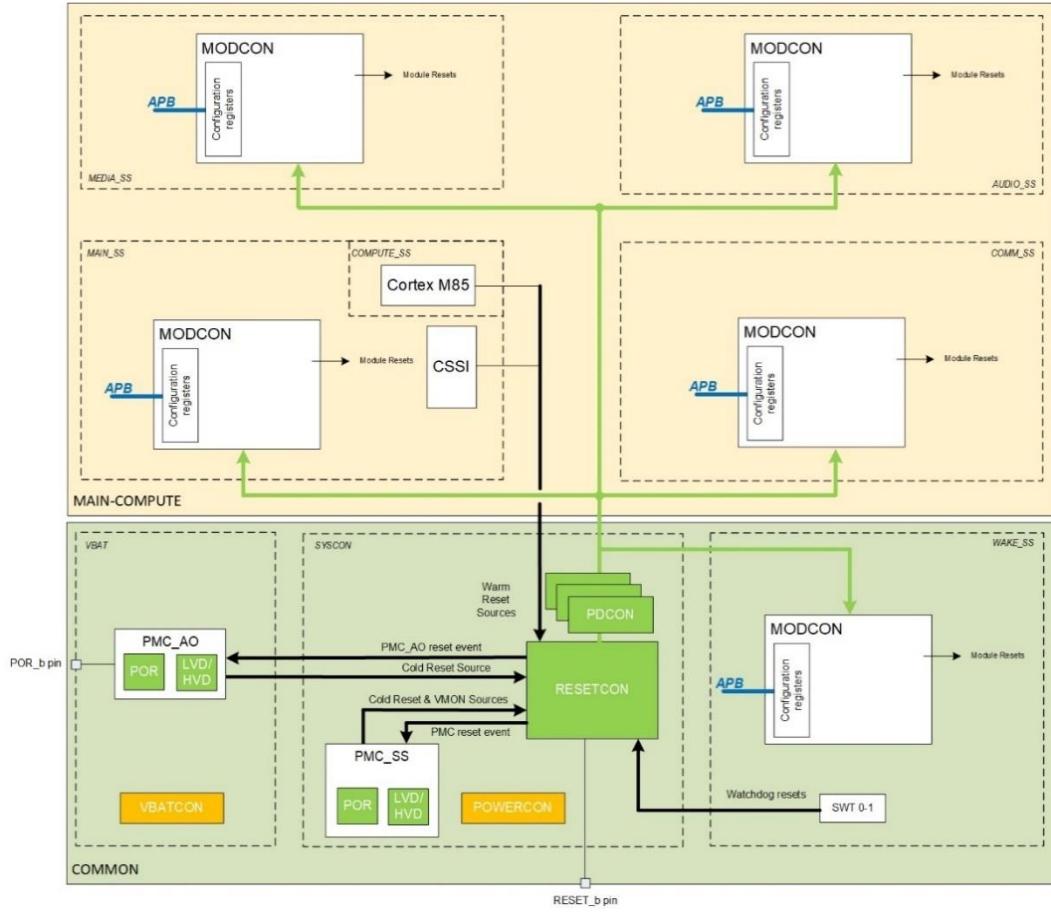


Fig 92. High-level overview of i.MX RT2660 reset architecture

The following subsections provide a further description of the reset functions of the i.MX RT2660.

Table 176. IC requirements traceability: Reset general requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_RnB_1-3	This Device shall implement Power-On reset at initial power up.	Must have	Yes, PMC-POR
iMXRT2660_RnB_1-16	A VBAT Power-On Reset shall also reset the entire chip.	Must have	Yes, VBAT-POR
iMXRT2660_RnB_1-9	This processor shall implement Power-On Reset to the VBAT domain is asserted anytime the input voltage is below an appropriate voltage.	Must have	Yes, VBAT-VMON
iMXRT2660_RnB_1-17	The Device shall implement a reset pin to allow an external device, such as a companion PMIC, to assert the pin externally to force the Device in Pin reset condition.	Must have	Yes, POR_b
iMXRT2660_RnB_1-18	The Reset pin shall be a bi-directional open-drain pin with internal pull-up resistor. During reset, the Reset pin remains asserted until the chip completes hardware initialization, at which point the Reset pin is released.	Must have	Yes, RESET_b
iMXRT2660_RnB_1-19	Filtering logic shall be implemented on the input reset pin to prevent glitch.	Must have	Yes, RESET_b digital filter; analog filter TBD
iMXRT2660_RnB_1-20	Pin reset shall generate a WARM reset condition to the SoC .	Must have	Yes, RESET_b
iMXRT2660_RnB_1-21	The Device shall implement reset_out signals. Reset_out can be optionally used to reset external components in the event of an MCU reset.	Must have	Yes, RESET_b; additional pins TBD

AS/RS identifier	Contents									Classification	Covered									
Reset_out signals can be multiplexed on 1-2 GPIO pins.																				
7.6.1 Reset sources and scope																				
Two types of reset sources can be distinguished, namely global reset- and local reset sources. Table 177 shows an overview of the global reset sources and their reset scope.																				
Reset source	Type	Severity	Reset scope			Description														
			VBAT_SS Cold Reset	PMC_SS Status Reset	PMC_SS Cold Reset	PMC_SS Warm Reset	*_SS Retention Reset	*_SS Cold Reset	*_SS Warm Reset											
VBAT-POR	Internal	Cold	yes	yes	yes	yes	yes	yes	yes	VBAT supply ramp										
POR_b pin	External	Cold	no	yes	yes	yes	yes	yes	yes	Power-on reset from POR_b pin										
PMC-POR	Internal	Cold								PMC supply ramp										
VBAT WU	Internal	Cold								Wakeup from VBAT standby mode										
CORE-VMON	Internal	Cold	no	no	yes	yes	yes	yes	yes	PMC_SS voltage monitor(s) for CORE supplies										
IO-VMON	Internal	Cold								PMC_SS voltage monitor(s) for IO supplies										
VBAT-VMON	Internal	Cold								VBAT voltage monitor(s)										
PMC-VMON	Internal	Cold								PMC_SS voltage monitor(s) for PMC supplies										
RESETCON	Internal	Cold								Error condition detected in RESETCON										
Escalated Reset	Internal	Cold								Warm reset source can be escalated to cold reset										
RESET_b pin	External	Warm	no	no	no	yes	yes	no	yes	Warm reset from RESET_b pin										
SW reset	Internal	Warm								Software initiated reset										
CSSI reset	Internal	Warm								Security reset from CSSI-110										
TDET reset	Internal	Warm								Tamper pin reset from TDET										
JTAG reset	Internal	Warm								JTAG Boundary scan reset										
DAP reset	Internal	Warm								Warm reset invoked by Debug Mailbox										
CPU RESETREQ	Internal	Warm								Warm reset invoked by software										
CPU LOCKUP	Internal	Warm								Warm reset triggered by CPU lockup state										
Clock Monitor	Internal	Warm								Warm reset triggered by PLL loss of clock/lock										
Temp Monitor	Internal	Warm								Warm reset triggered by temperature monitor										
Code Watchdog	Internal	Warm								Warm reset invoked by code watchdog										
System Watchdog	Internal	Warm								Warm reset invoked by system watchdog timeout										
DPD WU	Internal	Cold	no	no	no	no	yes	yes	yes	Wakeup from Deep Power Down standby mode										
*_SS WU	Internal	SS	no	no	no	no	no	*	*	Any SS while power gated										
*_SS SW	Internal	SS	no	no	no	no	*	*	*	Software initiated SS reset										

Local reset sources concern software generated resets that can be either warm or cold resets. Their reset scope may concern one or more main sub-systems or simply a reset of a given IP module. All local reset sources are assumed of a “non-fatal” severity level as they are invoked by software.

All non-logic voltage rails (such as IO or analog rails) shall implement separate POR and isolation signals that assert on the relevant cold reset event, under software control, or in low power modes if configured by software (for example, if the IO or analog rail is externally gated as a result of entering a low power mode).

Table 178. IC requirements traceability: Reset sources requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_RnB_1-4	This Device shall implement Power-On reset the SoC logic on the core supply upon detection of a low-voltage or high-voltage condition on the core supply.	Must have	Yes, as per Table 177
iMXRT2660_RnB_1-9	A pre-programmable time period at minimum 256 clock cycles of the System Oscillator clock is specified for each non-fatal reset source.	Must have	To be confirmed during design phase
iMXRT2660_RnB_1-11	A WARM reset event shall not reset the on-chip DC/DC and LDO operation status.	Must have	Yes, as per Table 177
iMXRT2660_RnB_1-12	A WARM reset event shall not reset on-chip SRAM.	Must have	Yes, SRAM contents not powered off on reset
iMXRT2660_RnB_1-13	A WARM reset event shall not reset any debug logic.	Must have	Yes, Debug logic reset by cold reset
iMXRT2660_RnB_1-14	The Device shall support COLD reset and WARM reset options by software.	Must have	Yes, Reset Escalation Register

7.6.2Reset pins

The i.MX RT2600 contains two reset related pins: the POR_B pin and the RESET_B pin.

POR_B is input-only pin that resides in the VBAT I/O domain. Its purpose is to provide an external power-on reset option for user applications and could be driven by an external PMIC. Once invoked, it initiates a cold reset to all domains, except for the VBAT domain.

RESET_B is a bi-directional reset pin that resides in the JTAG I/O domain. Its purpose is to provide a warm reset to all domains and could be driven by a debug interface or an external device to initiate entry into ISP mode. The RESET_B pin shall drive low on any cold or warm reset source (other than powerup of internal power domain) until the device has completed initialization (including valid lifecycle). The RESET_b is then tristated and internal reset to the boot core is gated until the RESET_b pin negates (pulls high), allowing an external debugger or tester to hold the RESET_b pin low externally after the lifecycle is valid but before the boot core starts ROM execution.

7.6.3Reset Controller

For more detailed description of the RESETCON and the related sequences, please refer to the RT2660 System Control HW.AS document [10]

The reset controller (RESETCON) is the SoC global reset controller that collates the different reset sources and generates the global cold reset and the global warm reset for all subsystems. It includes

status registers to report the source of the latest global reset, individual power domain resets and sticky reset registers to enable debugging of repeating reset events. The external reset pins (POR_b and RESET_b pins) are also controlled by the reset controller.

The RESETCON is part of the SYSCON subsystem and shall implement the following functions:

- Interface to the VBAT domain to receive the VBAT POR and POR_b input pin;
- Drive the RESET_b pin low on any reset source and tri-state at the end of the reset sequence;
- Generate the RESETCON status register reset, cold reset & warm reset for the PMC_SS;
- Generate the global cold reset and global warm reset from all the reset sources and provide to each PDCON slice;
- Wait for reset done or reset error signals from all modules that perform reset initialization steps during the reset sequence;
- Generate end of reset sequence for all PDCON slices;
- Latch the state of the boot mode configuration registers at the end of the reset sequence;
- Reset state machine shall be implemented using one-hot FSM encoding with glitch protection and shall force a global cold reset if an invalid state is detected;
- Implement the register interface for RESETCON.

All warm reset sources shall be collated at the RESETCON and the RESETCON shall generate a global warm reset event for all logic power domains. If configured by software, the reset controller shall support a delay of the warm reset event while an interrupt is generated.

If a warm reset event is delayed while an interrupt is generated, an independent clock source shall be used to generate a timeout that forces the warm reset event when the timeout counter expires. This is intended to allow software to save the state of the device immediately before the reset event or for trace logic to finish storing recent activity to on-chip or off-chip memory.

The RESETCON shall handshake with each module that performs initialization sequences during the reset flow. Initialization sequences can include loading trims, SRAM repair or initializing memory contents. The reset controller shall receive either a reset done or reset error at the end of the initialization sequence and shall collate the error signals (eg: ECC errors) and make them available to the boot software.

The RESETCON shall capture the reset source that triggered the last cold or warm reset, although the reset source shall not include the assertion of the RESET_b pin in response to a different reset source assertion. A sticky version of the reset source register shall be captured at the end of each reset sequence, these registers shall include all reset sources that have been triggered from previous reset sequences until each has been cleared by software.

7.6.4 Reset Sequence

7.6.4.1 Cold Reset Sequence

The reset sequence for global cold resets is described in the following table.

Table 179. Cold Reset Sequence

Sequence Number	Module	Reset Source	Delay	Description
1	PMC_VBAT	VBAT	Tbd	VBAT POR asserts during power ramp
	VBATCON		Async	VBAT_SS cold reset asserts
	PMC_SS	PMC	Tbd	PMC POR asserts during power ramp
	RESETCON		Async	PMC_SS warm/cold resets assert

Sequence Number	Module	Reset Source	Delay	Description
				Global warm/early/cold reset assert RESETCON status reset asserts RESET_b pin asserts
	PMC_SS		Tbd	PMC VMON assert during power ramp
2	PMC_VBAT	VBAT	Tbd	VBAT POR negates when voltage stable
	PMC_SS	PMC	Tbd	PMC POR negates when voltage stable
3	VBATCON	VBAT	Async	VBAT_SS cold reset negates
	PMC_SS	PMC	Async	PMC_SS FSM clock is enabled PMC_SS core regulators enabled
4	PMC_SS		Tbd	PMC VMON negate when voltage stable
	RESETCON		N cycles	PMC_SS cold reset negates RESETCON status reset negates Global cold reset negates
5	PDCON PD_*		N cycles	Local cold resets negate
6	SoC		Minimum 256 cycles	Cold reset initialization sequence starts (eg: OCOTP, CSSI, etc)
7	SoC		N cycles	Cold reset initialization sequence completes with modules asserting done or error signal to RESETCON
8	RESETCON		N cycles	RESETCON asserts trim valid signal to initiate hardware loading of trims, or trim error signal if device has not been trimmed or an error was detected
9	PMC_SS		TBD	PMC_SS asserts boot ready output indicating that trims are loaded and Main PLL is locked
10	RESETCON		N cycles	PMC_SS warm reset negates Global early warm reset negates
11	PDCON PD_*		N cycles	Clock roots disabled Local early warm resets negate Clock roots enabled
12	SoC		TBD	Warm reset initialization sequence starts (eg: MTR, etc)
	SoC		N cycles	Warm reset initialization sequence completes with modules asserting done or error signal to RESETCON
13	RESETCON		N cycles	RESET_b pin is tristated with pullup resistor enabled
15	SoC		Tbd	External RESET_b pin negates
16	RESETCON		N cycles	Global warm reset negates Mode pins are latched Sticky reset status register updates
17	PDCON PD_*		N cycles	Local warm resets negate

7.6.4.2 Warm Reset Sequence

The reset sequence for global cold resets is described in the following table.

Table 180. Warm Reset Sequence

Sequence Number	Module	Reset Source	Delay	Description
1	SoC	Warm	Varies	Warm reset source asserts
2	RESETCON		Async	PMC_SS warm reset asserts Global warm reset asserts
3	PDCON PD_*		N cycles	Clock roots disabled Local warm resets assert
4	POWERCON		Varies	Switch power configuration to Reset PDCFG
5	PDCON PD_*		N cycles	Local early warm resets negate Clock roots enabled
6	SoC		TBD	Warm reset initialization sequence starts (eg: MTR, etc)
7	SoC		N cycles	Warm reset initialization sequence completes with modules asserting done or error signal to RESETCON
8	RESETCON		N cycles	RESET_b pin is tristated with pullup resistor enabled
9	SoC		Tbd	External RESET_b pin negates
10	RESETCON		N cycles	Global warm reset negates Mode pins are latched Sticky reset status register updates
	PDCON PD_*		N cycles	Local warm resets negate

7.6.5 Power Domain Resets

Each power domain implements a power domain control (PDCON) slice that sequences the resets, isolation signals, power switches and root clock enables for that power domain. The power domain controllers receive global warm reset and global cold reset from RESETCON and the power domain related signals from POWERCON.

The power domain controller implements the following functions:

- Combine power domain reset and global resets to generate the local warm reset and local cold reset for the power domain ;
- Sequence the clock root enables for the power domain to ensure clocks are disabled during assertion of local resets and during the negation of local resets ;
- Sequence the power switch and isolation signals during entry into low power modes that include power gating.

7.6.6 Local Module Resets

Software controlled resets for individual modules are implemented within MODCON. Synchronization of the module reset to a given module's functional clock domain may be implemented in MODCON if not implemented internal to the module.

All AXI bus initiators shall implement control bits within MODCON to block new AXI transactions on the bus and status bits to indicate when outstanding AXI transactions have completed. This enables software to first ensure all outstanding AXI transactions have completed before the module is reset by software.

7.6.7 Implementation

RESETCON is implemented in the same power and clock domain as POWERCON and the PMC register interface. The register interface may be implemented on either the PMC FSM clock or an asynchronous bus clock. Some of the status registers are reset by the RESETCON status reset.

The RESETCON shall not implement a free running clock. The RESETCON shall generate a clock request to the PMC that asserts asynchronously if any reset source asserts and negates at the end of the reset sequence (or if the reset interrupt is cancelled or the RESET_b pin filter is idle). The register interface shall only require a clock during the reset sequence or during a register access.

The RESETCON state machine shall be implemented using one-hot encoding and encoded in two separate registers with opposite polarities. Any non-valid (or non-matching) state shall trigger a cold reset.

All reset source inputs into RESETCON shall be captured asynchronously using individual reset synchronizers. The outputs of these synchronizers shall be combined (eg: ANDed for active low signals) and used to asynchronously generate the various reset outputs that are also implemented using reset synchronizers. The cascading of reset synchronizers is required since the reset source inputs can be asynchronously reset by the RESETCON generated resets.

Cold resets are asynchronous and treated as level sensitive, so the cold reset output from RESETCON must be used to reset the source of the cold reset when it is generated by digital logic (eg: RESETCON error). In RTL simulations this does create a “0 wide” glitch, but this is expected and unavoidable.

Warm resets are also captured asynchronously but assertion is effectively edge sensitive and negation is level sensitive (eg: RESET_B pin falling edge triggers the global warm reset assertion but does not delay initialization sequence; the RESET_B pin has to negate before ROM execution can start). Note that there is a delay between when RESET_b pin is no longer asserted by RESETCON and when the RESET_b pin input pulls high, this period must not generate a new warm reset event due to the RESET_b pin input.

Reset controllers have previously made use of asynchronous set and reset flops, to capture the different reset sources. This can be avoided by using asynchronous set flops that assert on either the RESETCON status reset or the reset source. A flop that detects a RESETCON status reset is then used to mask the other reset sources.

Once the initial reset source is captured, the other reset sources should be masked to ensure only the initial reset source is captured. The RESET_b pin shall not be captured as a reset source just because the RESET_b pin asserted as a result of a different reset source.

To maintain System SRAM contents during warm reset, there are a few system requirements:

- At a basic level, warm reset shall not power off the SRAM. This will be software configurable in POWERCON using the PDCFG_RESET configuration ;
- An asynchronously generated reset that occurs at the same time as an SRAM access can theoretically corrupt one or more random addresses in SRAM. There are no timing checks on asynchronous reset assertion (only asynchronous reset negation which must be synchronous) ;
- A reset that asserts synchronously and is synchronously used to safe-state an SRAM (eg: negate chip select) will ensure timing checks are performed and that the SRAM is safe stated without corruption of SRAM ;
- A reset that asserts asynchronously but is synchronously used to safe-state an SRAM (eg: negate chip select) creates a race condition between the propagation time to the safe-

stating logic and the asynchronous reset propagating time to the logic on the fan-in to the SRAM ;

- Other approaches including disabling of system clock source before propagating the reset are also possible.

Maintaining System SRAM contents during cold reset is not guaranteed, since cold reset may involve the SRAM array losing state.

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8. Power Architecture

The i.MX RT2660 power architecture is defined in context of its targeted use-case scenarios based on the assumption that the off-chip power supply is provided by a low-cost Power Management IC (PMIC) and/or by a Lithium coin cell battery. The key power supply scenarios to be supported are listed in Section 5.2. This Chapter provides a more detailed insight into the targeted Power Architecture for the i.MX RT2660.

8.1 Power Supply Overview

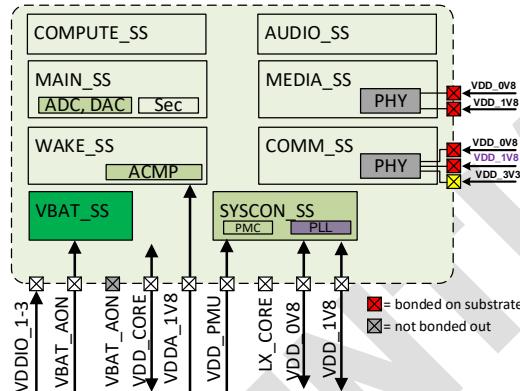


Fig 93. i.MX RT2660 SoC power supply overview

The i.MX RT2660 makes use of an embedded Power Management Unit (PMU) to generate the different supply voltages required by the SoC. This helps to reduce the amount of different supply voltages that need to be supported externally and eases chip integration into the system. The main input supply pins of the i.MX RT2660 are VDD_PMU, VBAT_AON and VDDIO.

Fig 93 shows the different supply pins that power the different SoC subsystems. VDDIO supports the external supply to the IO sections. VDD_CORE, VDDA_1V8, VDD_1V8 and VDD_0V8 pins can derive their supply from the VDD_PMU using the internal regulators or they may supplied externally. The analog blocks (ADC, DAC, ACMP) are supported from VDDA_1V8 while VDD_0V8 support the various PHYs (USB and MIP) and IO core supply. 1.8V and 3.3 voltage ranges are supported on the three input rails. Table 181 summarises the voltage range of the supply pins.

The VBAT domain also features internal power mux to allow use of VDD_PMU, VDDA_1V8 and VDD_CORE for the major part and can switch to a battery-supplied standby voltage for backup retention. The internal power mux are controlled by the PMC_SS FSM, to ensure that the correct VBAT domain supply source is selected for tamper monitoring and low-power optimization dependent on operating mode. This is further detailed out in [61].

Table 181. Voltage range on RT2660 supply pins

Supply Pin	Range 1		Range 2	
	V _{min} [V]	V _{max} [V]	V _{min} [V]	V _{max} [V]
VDD_PMU	1.71	1.89	2.4	3.6
VDD_1V8	1.71	1.89		
VDDA_1V8	1.71	1.89		
VDD_IO[1-3]	1.71	1.89	2.4	3.6

Supply Pin	Range 1		Range 2	
	V _{min} [V]	V _{max} [V]	V _{min} [V]	V _{max} [V]
VDD_0V8	0.72	0.88		
VDD_CORE	0.5	0.945		
VBAT_AON	1.71	1.89	2.4	3.6

8.2 Power Architecture

Fig 94 shows a high-level overview of the various components of the i.MX RT2660 power architecture as well as their connectivity.

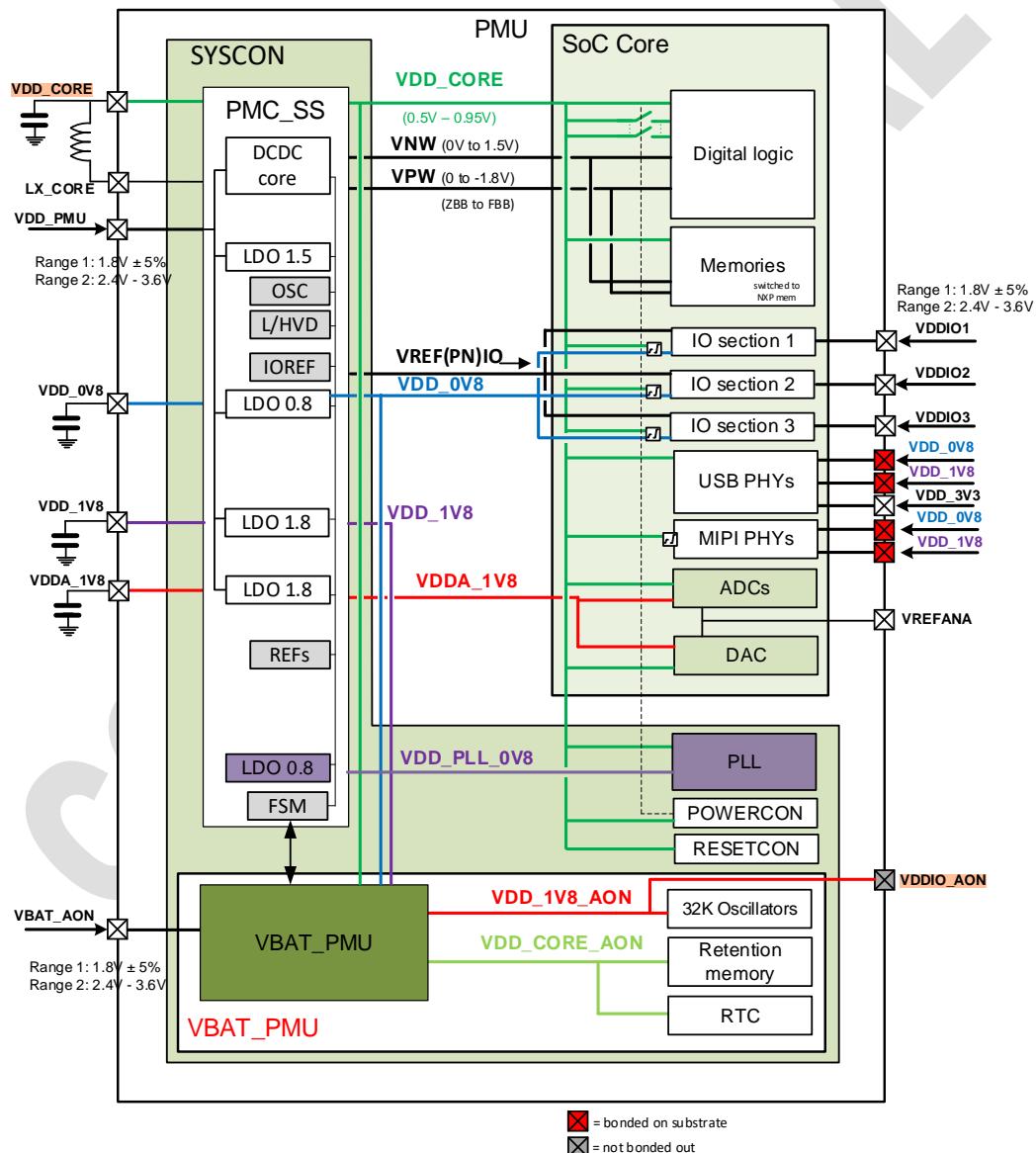


Fig 94. i.MX RT2660 SoC power architecture

The SoC is powered from two on-chip Power Management Units (PMUs), namely the main PMU subsystem (PMU) and the battery domain PMU (VBAT PMU). Refer to Section 8.3.

The digital core of the SoC is powered from a single voltage supply in order to reduce SoC cost. The digital logic and memories operate from the same supply voltage rail that is provided from a single output (VDD_CORE) from the PMC_SS. This:

- 1) enables a single power grid design for the digital core which results into smallest die size;
- 2) avoids level shifters between logic and memories, which is good for achieving high performance;
- 3) reduces SoC implementation complexity.

However, the memory V_{Dmin} poses a limit to the minimum voltage operation for digital logic. During active operation mode, the VDD_CORE can be nominal (0.8V typ.) or overdrive (0.9V typ) during active operation mode. During standby modes, the VDD_CORE can be nominal (0.8V typ.) or 0.65V typical, for reduced retention voltage during standby modes. Refer to Section 8.3.1.1.

The digital core of the SoC supports body biasing for power-performance control. At a high-level, there exists a high-performance body bias domain utilizing a flipped-well structure supporting forward body biasing, and zero body biasing. The body bias voltages are provided by the PMC_SS (VNW, VPW). Refer to Section 8.3.4.

For all integrated analog modules, their 1.8V analog power will be supplied by the PMC_SS. The PMU_SS generates a 1.8V analog supply (VDDA_1V8) for powering as clean supply to noise-sensitive analog IPs. It generates a 0.8V supply (VDD_PLL_0V8) to not impact PLL analog performance. A third 0.8V supply (VDD_0V8) for SoC power- and PHY infrastructure is provisioned which is also used to power IO core supply; this allows potentially-noisy supply to be isolated from the sensitive rails. A fourth VDD_1V8 supports PHYs with the 1.8V supply.

For high-speed interface modules, their 0.8V PHY supply is generated by the PMC_SS (VDD_0V8) and their digital power will be supplied by VDD_CORE. This is to be turned-off during SoC standby modes in order to save power and leakage. Any USB PHY 3.3V needs (where applicable) will be supplied externally through power pads.

The VBAT subsystem of the i.MX RT2660 is supplied from a dedicated on-chip PMU (VBAT_AON) tailored to operate at the very low-power consumption mandated by battery-backed operation (during deep power down). The VBAT_AON contains supply power muxing to select its supply input from VDD_PMU, VDD_1V8 or VDD_CORE when these supplies are available, or alternatively select the VBAT_AON input respectively. All functions that are part of the VBAT_SS are powered from a supply voltage that is generated by the VBAT PMU, i.e. either the VDD_AON (0.8V) or VDD_AON_1V8 (1.8V) output supply.

Finally, the i.MX RT2660 offers IOs with 1.8V/3.3V signalling capabilities. The IO supply is provided externally and IO power supply voltage in the range of 1.8V-10% up to 3.3V+10% is supported. Three IO sections are provisioned to which a different IO supply voltage can be applied, to support mix 1.8V/3.3V supply use-cases (VDDIO1, VDDIO2 and VDDIO3). This is in addition to an always-on IO section for tamper detection and wakeup management from the lowest power modes. These AON pads are contained in the VBAT_SS and consists of two dedicated GPIO and two tamper pads, one wake and one reset pin which are supplied from a 1.8V provided by the VBAT_SS itself.

8.3 SoC power architecture components

This Section describes the various power architecture components of the i.MX RT2660 SoC.

8.3.1 Power Management Unit

Fig 95 shows a high-level block diagram of the i.MX RT2660 Power Management Unit (PMU), which constitutes of the main PMU also referred to as PMC_SS, and the VBAT PMU. The PMU definition has been tailored to i.MX RT2660 requirements.

For a detailed description of the PMU, please refer to the PMC_SS HW.AS document [9].

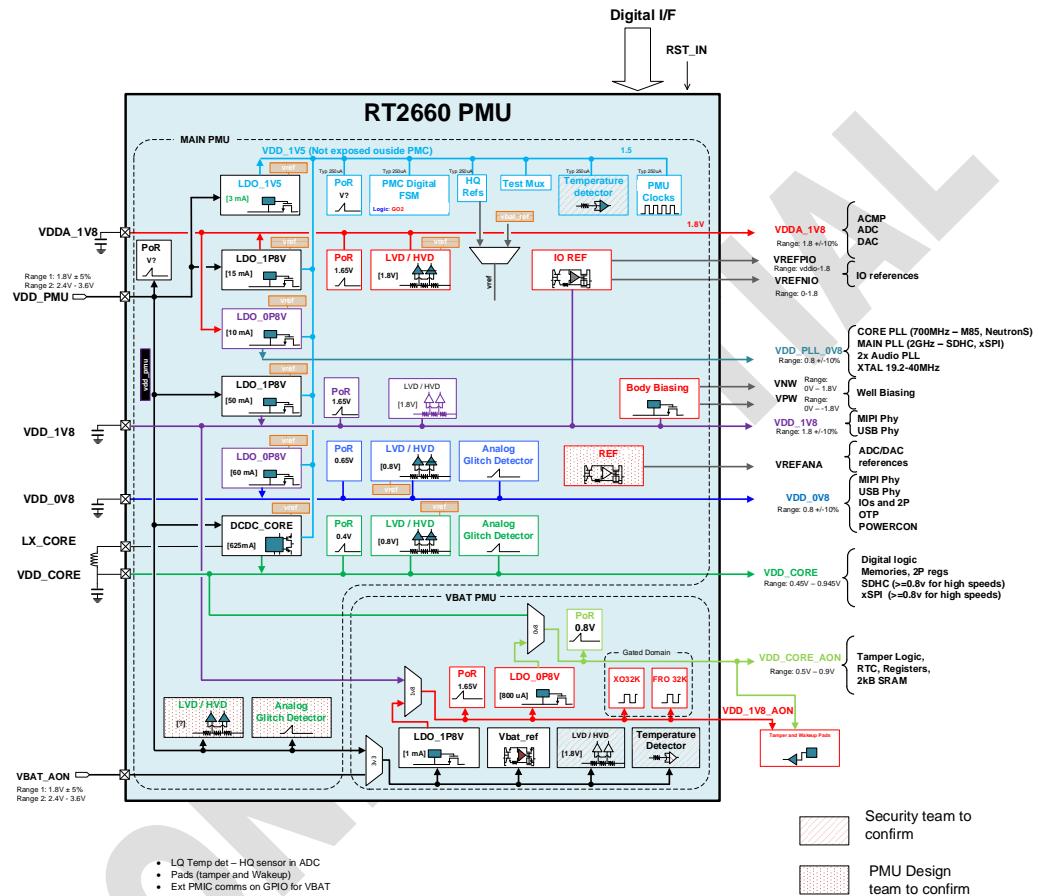


Fig 95. i.MX RT2660 Power Management Unit block diagram

All PMU components shall be optimized for highest power efficiency and low power consumption. The PMU shall be provided as a hard macro to the SoC implementation team. The digital interface of the PMU macro shall operate at VDD_CORE signalling levels.

The PMC_SS uses a DC-DC conversion for efficient power consumption from an external higher supply voltage (VDD_PMU) to the internal lower supply voltage of the SoC. DC-DC conversion over LDO's has been chosen to increase power conversion efficiency because of the large difference between input- and output supply voltage as well as the large output load current range associated to the digital core.

The DCDC_CORE shall support a ultra-low-power operation to supply VDD_CORE during i.MX RT2660 standby modes. In fact, DCDC_CORE shall consume less than **TBD µA** during standby operation, while at the same time being capable to supply up to **TBD mA** maximum load current.

LDO_0V8 block generate the 0.8V supply VDD_0V8 to support IOs and level shifting as needed. Although the usage of DCDC conversion was interesting from a power conversion efficiency perspective, it has been decided otherwise to avoid yet another external inductor and related DCDC pins.

Two LDO_1V8 blocks generate 1.8V supplies: VDD_1V8 and VDDA_1V8. The VDD_1V8 is mainly intended to generate a 1.8V supply for MIPI PHYs, USB PHYs and Body Biasing IP. The VDDA_1V8 is mainly intended to provide a clean supply voltage for analog modules such as ADC, DAC and ACMP. This supply is also used by the clock generator (CGU) which further uses a VDD_0V8 regulator internally. When VDD_PMU is 1.8V $\pm 5\%$, both LDO_1P8V blocks shall be turned-off and bypassed; If this is the default mode of operation, the board may this may be provisioned by shorting VDD_PMU, VDD_1V8 and VDDA_1V8 externally (see Section 5.2).

The LDO_1V5 is mainly used to power the PMC_SS power management controller hardware state machine (PMC digital) as well as other PMC_SS internal components.

All MAIN_PMU generated power supplies with external pad presence make use of Low-Voltage-Detector (LVD), High-Voltage-Detector (HVD) and Analog Glitch Detector (AGDET) as voltage monitors. The main purpose of those voltage monitors is to check whether supply voltages are within the expected voltage ranges, e.g. to detect supply voltage related tamper events. No LVD/HVD/AGDET is provisioned for VDD_PLL_0V8 and VDD_1V5 in order to save power consumption, while it is not accessible from outside.

Fig 95 also shows a high-level block diagram of the VBAT_SS power management. This definition is not based on i.MX RT2660 requirements alone, but also considering re-use possibilities for other XEA-1 platform based products such as i.MX RT2770 and i.MX RT2520W.

The VBAT_PMU makes use of three distinct input power supplies, a first one provided by VBAT_AON, a second one from the main VDD_PMU, and a third one from VDD_CORE. The selection of the input supply is based on the presence of those supplies. The power muxes default to VBAT_AON until the FSM switches the muxes to VDD_PMU. The power multiplexers in the VBAT_SS are expected to have overrides and/or inputs from the POWERCON. The intent of the power muxing configurability is to be able to save battery current in case a backup battery is connected to VBAT_AON, by powering VBAT_SS by the main power supply (VDD_PMU) as provided by VDD_1V8.

The oscillators are expected to be low power and can remain always ON. This portion also supports retention of RTC, memory and tamper logic and some dedicated IOs.

Table 182. IC requirements traceability: SoC VDD requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_SEC_21-2	This processor shall support power glitch detection on the main power supply pin (VCC).	Must have	Yes

Table 183. IC requirements traceability: Power architectural requirements – part I

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_PWR_4-2	DCDC converters	Heading	-
iMXRT2660_PWR_4-3	This processor shall include a DCDC converter to generate the digital core power supply in accordance with the chip operation modes.	Must have	Yes
iMXRT2660_PWR_4-4	The DCDC has typical efficiency of 90% or better.	Must have	IP verification during design phase
iMXRT2660_PWR_4-5	The DCDC shall support dynamic voltage scaling.	Must have	Yes,

AS/RS identifier	Contents	Classification	Covered
			0.585-0.945V
iMXRT2660_PWR_4-6	The DCDC can be bypassed when an external PMIC directly supplies the digital core.	Must have	Yes
iMXRT2660_PWR_4-6	The DCDC converter shall implement Enablement logic internally, removing the requirement for a power switch pad, to reduce the risk of start up failure, save power, save a pad, and simplify external circuit.	Must have	Targeted, to be concluded during design phase
iMXRT2660_PWR_4-7	LDOs	Heading	-
iMXRT2660_PWR_4-8	This processor shall implement LDOs for internal logic power supply as needed	Must have	Yes
iMXRT2660_PWR_4-9	This processor shall implement a LDO for the battery-backup domain	Must have	Yes

Table 184. IC requirements traceability: Battery-Backup (VBAT) Domain requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_SEC_20-2	This processor shall implement a battery-backup domain, which can be powered from a separate backup battery in case of the main power supply turned off.	Must have	Yes
iMXRT2660_SEC_20-3	The VBAT domain shall be powered from the main power supply when that power supply is available in order to save the battery life. The VBAT domain shall switch to the backup power supply only when the main power supply is turned off.	Must have	Yes
iMXRT2660_SEC_20-4	The VBAT domain shall include a RTC oscillator to receive the 32.768kHz real-time reference clock from an external RTC crystal oscillator.	Must have	Yes
iMXRT2660_SEC_20-5	The VBAT domain shall include 2 tamper pins, which can be functional as two independent passive tamper pins or form one pair of active tamper.	Must have	Yes, targeted
iMXRT2660_SEC_20-6	The VBAT domain shall support clock, voltage, and temperature monitor tamper.	Must have	Rejected voltage & temp. Open: Req. update ongoing
iMXRT2660_SEC_20-7	The VBAT domain shall support HVD/LVD detection on VBAT power supply pin.	Must have	Rejected Open: Req. update ongoing
iMXRT2660_SEC_20-8	The VBAT domain shall include 256 bits general purpose registers for key storage.	Must have	Yes (BBSM)

8.3.1.1 Minimize DCDC output change

TKT0654328 shows when loading change significantly, DCDC output may overshoot and trigger system reset. For i.MXRT2660, need to handle this by IP and SoC level.

1. DCDC need to add simulation to find out SPEC of max loading change.
2. SoC need to provide power simulation result and

8.3.2 Power-performance control components

8.3.2.1 Power switch components

The i.MX RT2660 makes use of extensive power switching approach, in order to reduce leakage current when given functionality is not needed during application or in case of a derivative product e.g. a phantom device. Fig 96 shows a high-level circuit diagram of the main power switches used in the i.MX RT2660 SoC.

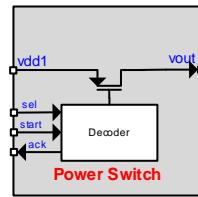


Fig 96. i.MX RT2660 power switches

The power switches are inserted into the SoC core area on given locations in close proximity to the power switchable power domain. One shall pay close attention to ensure a low-resistance connection between power connectivity of the power-switchable domain. Retention will be provided from the DCDC and hence the power switch shown in Fig 96(right) shall be used for turning off non retention logic while providing retention power for the retentive portions. Logic retention can also be turned off during power down modes when only SRAM is retained.

Table 185. IC requirements traceability: Power architectural requirements – part III

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_PWR_4-11	This processor shall implement power switches for fine-grain power mode management as needed.	Must have	Yes

8.3.2.2 Level Shifting for IOs

The i.Mx RT2660 core operates at wide voltage-frequency points that are appropriate for the required performance and power targets. However, IOs have limited range for accepting input voltages. Level shifting is a key component in such cases. Level shifting is not needed for SoG area since all SoG operates at a single voltage. When power gating between domains (discussed in Section 1.1.1.1) isolation is needed but not level shifting. It is anticipated that memory will also work down to core voltages. Therefore, the use of level shifters in the i.Mx RT2660 is limited to core-IO domain crossover signals.

Fig 97 shows an example level-up shifter available for perusal by implementation teams as part of the power management IP kit. Here, VDDI is the low supply expected to operate at core voltage levels. 'A' is the input referred to VDDI levels. VDD is the higher voltage supply compatible with IOs (0.8V typ). EN allows the level shifter to be put into a low-leakage mode and the output is clamped to a known voltages. EN is referred to VDD levels.

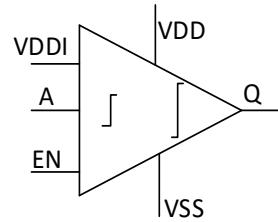


Fig 97. i.MX RT2660 Level Up Shifters for IO

Level shifters that clamp low and clamp high are both available making implementation easier. In addition, the anticipate supply routing overheads are minimal since VDD is a rail that is required by IOs and VDDI is a core supply rail that is needed for the nearest core cell.

The level shifters allow significant dynamic power savings in LP mode and also in deep sleep it is absolutely essential to scale supply voltage for achieving the required power targets. The current estimated current overheads are expected to be 33% of IO LV side leakage. The estimated values are listed in Table 186.

Table 186. i.MX RT2660 Level Shifter overheads (estimated UDP116LVT36_LVLDBUFE0_1)

Condition	IO cells		EN=0		EN=1		TT25C 100MHz		FF125C 200MHz	
	Max	Typ	VDDI	VDD	VDDI	VDD	VDDI	VDD	VDDI	VDD
Unit Cell	18µA	22nA	2.8pA	8nA	315pA	10nA	200nA	1.7µA	550nA	4.6µA
RT2660 159 IOs	3mA	3.2 µA	450pA	1.3µA	50nA	1.6µA	32µA	270µA	85µA	750µA

8.3.2.3 SoC power domain partitioning

The i.Mx RT2660 is partitioned into a total of seventeen power domains including analog, IO and retention domains. Few of these power domains support power gating in order to save active leakage power consumption when the domain is not needed.

The digital core domain operates from a single power supply voltage (*vdd_core*); it consists of three switchable power domain and one always-on domain. Some of the functional subsystems contain non-switchable always-on sections to retain state information such as MODCON, configuration settings etc. These always-on sections operate from the *vdd_core* supply.

Table 187 shows a list of the available power domains of the i.MX RT2660 SoC. The supply source in column 'Supply' is the primary supply for the domain. There are secondary or tertiary sources required for level shifting or for analog operation. Some switchable domains have retention enabled.

Table 187. i.MX RT2660: on-chip power domains and supply rails per domain

Voltage Domain	Power Domain	can be gated?	~Gate Count [Million]	Supply1	Supply2	Supply3	Supply4
vdd_core	pd_core_main	Yes	1.71	vdd_core	vnw, vpw		
	pd_core_npu	Yes	2.3	vdd_core	vnw, vpw		
	pd_core_avc	Yes	1.65	vdd_core	vnw, vpw		
	pd_core	No	1.13	vdd_core			
vdd_0v8	pd_mipi_lv	Yes ¹	Phy	vdd_0v8	vdd_core	vddio1/2/3	

Voltage Domain	Power Domain	can be gated?	~Gate Count [Million]	Supply1	Supply2	Supply3	Supply4
vdd_1v8	pd_usb_lv	Yes ¹	Phy	vdd_0v8	vdd_core	vddio1/2/3	
	pd_wake	Yes ¹		vdd_0v8	vdd_core		
vdda_1v8	pd_mipi_hv	No	Phy	vdd_1v8	vdd_core	vddio1/2/3	
	pd_usb_hv	No	Phy	vdd_1v8	vdd_core	vddio1/2/3	
vddio	pd_ana	No	Analog	vdda_1v8	vdd_core	vddio1/2/3	
vddio	pd_io3	No	IO	vddio	vdd_core	vdd_0v8	
	pd_io2	No	IO	vddio	vdd_core	vdd_0v8	
vdd_pmu	pd_io1	No	IO	vddio	vdd_core	vdd_0v8	
	pd_pmu	No	PWR+CLK	vdd_0v8	vdd_core	vdd_pmu	vbat_aon
vdd_core_aon	pd_vbat_0v8	No	0.03	vdd_core_aon	vdd_core	vddio1/2/3	
vdd_1v8_aon	pd_io_aon	No	IO	vdd_1v8_aon	vdd_core_aon	vdd_core	vdd_0v8

Fig 98 provides a visual overview of the voltage domain partitions of the i.Mx RT2660. All of the SoG is the vdd_core domain. The vbat domain is split into 1V8 and 0V8 domains with the 0V8 being implemented using uHVT devices. The vdd_pmu voltage domain cover the PMU and the CGU as it depends on the supplies derived from the VDD_PMU pin.

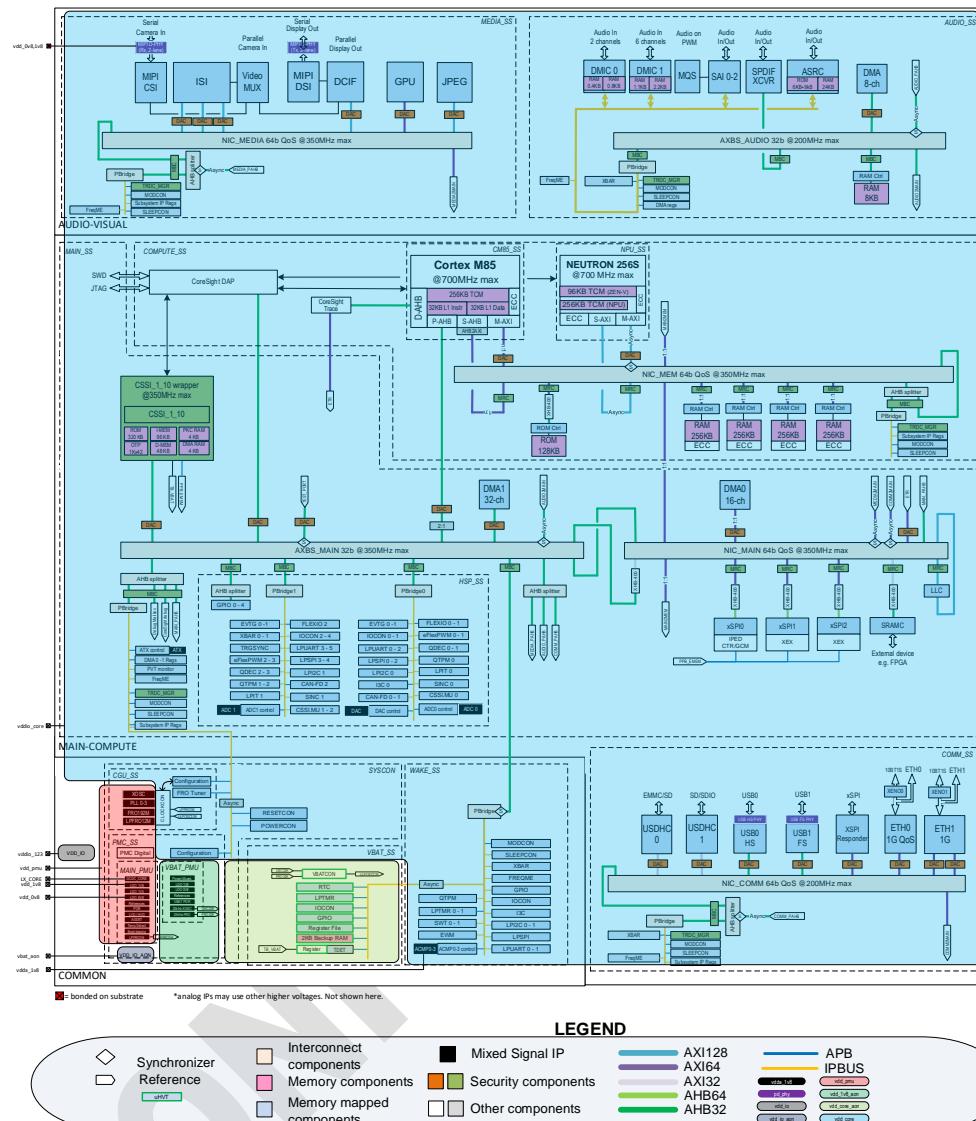


Fig 98. i.MX RT2660 voltage domain partitioning

Fig 99 depicts the power domain partitions of the i.Mx RT2660. The *pd_core* domain is always on on *vdd_core* supply. This includes sys, wake and some parts of audio sub-system. The *pd_avc* and *pd_npu* are switchable and can be off for normal operation. The *pd_vbat* domain shall make use of uHVT devices to minimize leakage during power down and deep power down modes.

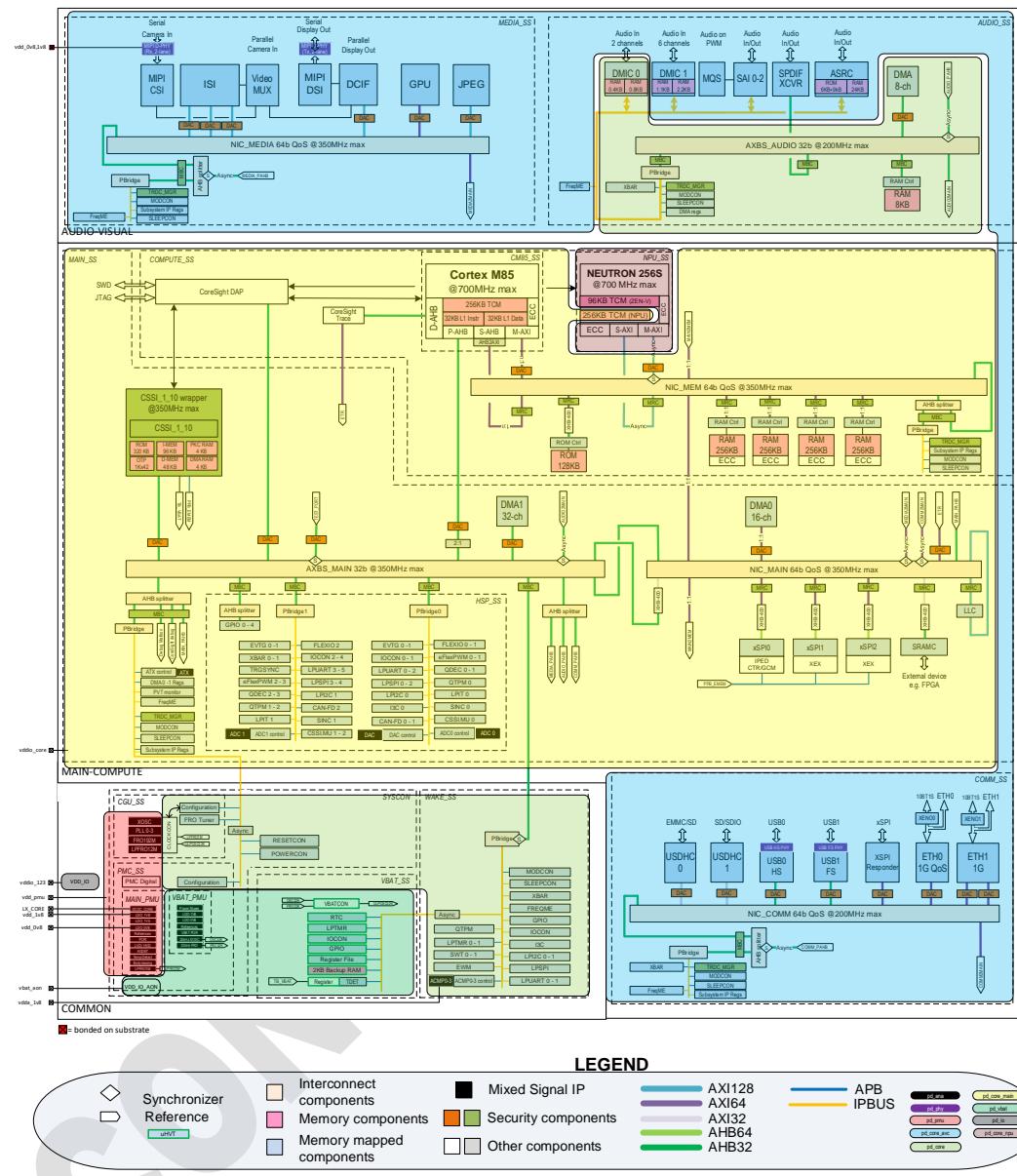


Fig 99. i.MX RT2660 power domain partitioning

Table 188 lists the different IPs from different subsystems and different power domains that are planned for retention. All the IPs listed for retention are in vdd_core voltage domain

Table 188. i.MX RT2660 IP retention section per subsystem and power domain

Item#	Subsystem	P domain	Retained IP	IP type
1	COMM_SS	pd_core_avc	MBC_AhbSplitter	BUS
2	COMM_SS	pd_core_avc	TRDC_COMM	LOGIC
3	COMM_SS	pd_core_avc	SLEEPCON_COMM	LOGIC
4	COMM_SS	pd_core_avc	MODCON_COMM	LOGIC
5	COMM_SS	pd_core_avc	COMM_IP_Regs	LOGIC
6	COMM_SS	pd_core_avc	DAC_uSDHC0	BUS
7	COMM_SS	pd_core_avc	DAC_uSDHC1	BUS
8	COMM_SS	pd_core_avc	DAC_USB0_HS	BUS

Item#	Subsystem	P domain	Retained IP	IP type
9	COMM_SS	pd_core_avc	DAC_USB1_FS	BUS
10	COMM_SS	pd_core_avc	DAC_XSPI Resp	BUS
11	COMM_SS	pd_core_avc	DAC_ETH0 1G QoS	BUS
12	COMM_SS	pd_core_avc	DAC_ETH1 1G_0	BUS
13	COMM_SS	pd_core_avc	DAC_ETH1 1G_1	BUS
14	COMPUTE_SS	pd_core_npu	NPU-ECC	LOGIC
15	COMPUTE_SS	pd_core_main	CM85	LOGIC
16	COMPUTE_SS	pd_core_main	256kB M85 TCM	MEM
17	COMPUTE_SS	pd_core_main	TRDC_COMP	LOGIC
18	COMPUTE_SS	pd_core_main	SLEEPCON_COMP	LOGIC
19	COMPUTE_SS	pd_core_main	MODCON_COMP	LOGIC
20	COMPUTE_SS	pd_core_main	COMP_IP_Regs	LOGIC
21	COMPUTE_SS	pd_core_main	MBC_COMP	BUS
22	COMPUTE_SS	pd_core_main	MRC_MEM0	BUS
23	COMPUTE_SS	pd_core_main	MRC_MEM1	BUS
24	COMPUTE_SS	pd_core_main	MRC_MEM2	BUS
25	COMPUTE_SS	pd_core_main	MRC_MEM3	BUS
26	COMPUTE_SS	pd_core_main	DAC_M85	BUS
27	COMPUTE_SS	pd_core_main	DAC_NPU	BUS
28	COMPUTE_SS	pd_core_main	MRC_M85	BUS
29	COMPUTE_SS	pd_core_main	MRC_NPU	BUS
30	COMPUTE_SS	pd_core_main	MRC_ROM	BUS
31	COMPUTE_SS	pd_core_main	MEM0_256kB	MEM
32	COMPUTE_SS	pd_core_main	MEM1_256kB	MEM
33	COMPUTE_SS	pd_core_main	MEM2_256kB	MEM
34	COMPUTE_SS	pd_core_main	MEM3_256kB	MEM
35	MAIN_SS	pd_core_main	TRDC_MAIN	LOGIC
36	MAIN_SS	pd_core_main	SLEEPCON_MAIN	LOGIC
37	MAIN_SS	pd_core_main	MODCON_MAIN	LOGIC
38	MAIN_SS	pd_core_main	MAIN_IP_Regs	LOGIC
39	MAIN_SS	pd_core_main	DAC_CSSI	BUS
40	MAIN_SS	pd_core_main	DAC_DEBUG	BUS
41	MAIN_SS	pd_core_main	DAC_TESTP	BUS
42	MAIN_SS	pd_core_main	DAC_CM85	BUS
43	MAIN_SS	pd_core_main	DAC_DMA1	BUS
44	MAIN_SS	pd_core_main	DAC_DMA0	BUS
45	MAIN_SS	pd_core_main	DAC_ETR	BUS
46	MAIN_SS	pd_core_main	MBC_MAIN_Pbridge	BUS
47	MAIN_SS	pd_core_main	MBC_HSP_Pbridge0	BUS
48	MAIN_SS	pd_core_main	MBC_HSP_Pbridge1	BUS
49	MAIN_SS	pd_core_main	MBC_MAIN_GPIO	BUS
50	MAIN_SS	pd_core_main	MBC_MAIN_AVC	BUS
51	MAIN_SS	pd_core_main	MRC_XSPI0	BUS
52	MAIN_SS	pd_core_main	MRC_XSPI1	BUS
53	MAIN_SS	pd_core_main	MRC_XSPI2	BUS
54	MAIN_SS	pd_core_main	MRC_SRAMC	BUS
55	MAIN_SS	pd_core_main	MRC_LLC	BUS
56	MAIN_SS	pd_core_main	CSSI-110	LOGIC
57	MEDIA_SS	pd_core_avc	TRDC_MEDIA	LOGIC
58	MEDIA_SS	pd_core_avc	MODCON_MEDIA	LOGIC
59	MEDIA_SS	pd_core_avc	SLEEPCON_MEDIA	LOGIC
60	MEDIA_SS	pd_core_avc	MEDIA_IP_Regs	LOGIC
61	MEDIA_SS	pd_core_avc	MBC_AhbSplitter	BUS
62	MEDIA_SS	pd_core_avc	ISI_DAC0	BUS
63	MEDIA_SS	pd_core_avc	ISI_DAC1	BUS
64	MEDIA_SS	pd_core_avc	ISI_DAC2	BUS
65	MEDIA_SS	pd_core_avc	DCIF_DAC	BUS
66	MEDIA_SS	pd_core_avc	JPEG_DAC	BUS
67	MEDIA_SS	pd_core_avc	GPU_DAC	BUS

The following table shows the power domain dependencies for the domains controlling the SoG area. For majority of the applications, it is essential for *pd_core_main* to be ON. For either or both *pd_core_npu* and *pd_core_avc* domains, *pd_core_main* is required to be ON. i.MX RT2660: Power domain dependency.

Table 189. i.MX RT2660: Power domain dependency

If ON ↓ then ON →		<i>pd_vbat</i>	<i>pd_core</i>	<i>pd_core_main</i>	<i>pd_core_avc</i>	<i>pd_core_npu</i>
<i>pd_vbat</i>	-	X	X	X	X	
<i>pd_core</i>	ON	-	X	X	X	
<i>pd_core_main</i> ¹	ON	ON	-	X	X	
<i>pd_core_avc</i> ¹	ON	ON	ON	-	X	
<i>pd_core_npu</i> ¹	ON	ON	ON	X	-	

¹ switchable domains with retention IP

This table does not include memories as SRAM IP features internal power switches. Note that all domains have registers that can be retained. However, since the retention rail is powered from the same DCDC source, the lowest retention voltages will not be possible when any domain is in active or sleep mode.

Table 190 shows the power domain dependencies for the domains controlling the SoG area. As long as *pd_core_main* is ON and active, the power mode is active (or sleep if the core enters sleep). For Deep Sleep mode, the rail voltage is dropped to 0.65V and *pd_core* and *sys* domains can remain active at low clock frequency (~12MHz typ). In Power Down mode, the *pd_core_main* is switched off except for 64kB memory.

Table 190. i.MX RT2660 Inferred power state table

Item#	Mode	<i>pd_core</i>	<i>pd_core_main</i>	<i>pd_core_avc</i>	<i>pd_core_npu</i>	<i>pd_vbat</i>
0	OFF	OFF	OFF	OFF	OFF	OFF
1		ON_0.8	ON_0.8	ON_0.8	ON_0.8	ON_0.8
2		ON_0.8	ON_0.8	ON_0.8	ON_0.8	ON_0.8
3		ON_0.8	ON_0.8	ON_0.8	OFF	ON_0.8
4		ON_0.8	ON_0.8	ON_0.8	ON_0.8	ON_0.8
5		ON_0.8	ON_0.8	ON_0.8	ON_0.8	ON_0.8
6		ON_0.8	ON_0.8	ON_0.8	OFF	ON_0.8
7		ON_0.8	ON_0.8	OFF	ON_0.8	ON_0.8
8		ON_0.8	ON_0.8	OFF	ON_0.8	ON_0.8
9		ON_0.8	ON_0.8	OFF	OFF	ON_0.8
10		ON_0.65	ON_0.65	ON_0.65	ON_0.65	ON_0.8
11	Deep Sleep	ON_0.65	ON_0.65	ON_0.65	OFF	ON_0.8
12		ON_0.65	ON_0.65	OFF	ON_0.65	ON_0.8
13		ON_0.65	ON_0.65	OFF	OFF	ON_0.8

14	Power Down	ON_0.65	Retn_64KB	OFF	OFF	ON_0.8
15	Deep Power Down	OFF	OFF	OFF	OFF	ON_0.8

8.3.2.4 SoC body bias domain strategy

The i.MX RT2660 is partitioning into two main body bias domains, one high-performance domain in which Forward Body Biasing (FBB) or Zero Body Biasing (ZBB) can be utilized, and one low-power domain in which only ZBB is utilized.

During PA phase, feedback from SoC Design is needed whether more subsystems can be targeted to Low-Power domain for timing closure, to benefit SoC implementation wrt body bias grids. As power architecture has been compromised by dropping Low Power Run mode (see Section 6.1.5), the VDD_CORE minimum voltage is constrained to 0.72V during active operation. Consequently, the FBB application of subsystems with maximum frequency of up to 200MHz makes not much sense. Due to this constraint, the following subsystem allocation to body bias domain is envisioned.

Table 191. **i.MX RT2660: body bias domain strategy**

Subsystem	High-Performance Run mode	Normal Run mode	Standby modes
CMPT_SS	FBB	FBB	ZBB
MAIN_SS	FBB	FBB	ZBB
MEDIA_SS	FBB	FBB	ZBB
AUDIO_SS	ZBB	ZBB	ZBB
COMM_SS	ZBB	ZBB	ZBB
WAKE_SS	ZBB	ZBB	ZBB
SYSCON	ZBB	ZBB	ZBB
VBAT_SS	ZBB	ZBB	ZBB

8.3.2.5 Power-performance control strategy

In general it is expected that customer will choose a VDD_CORE value statically operate at either Normal Run mode or High-Performance Run mode (for highest performance). For the High-Performance domain, body biasing is applied in conjunction with supply voltage setting to improve on SoC power-performance outcome.

The effectiveness of joint VDD+FBB control is higher to reduce power consumption when peak performance is not required. However, the i.MX RT2660 power architecture has been compromised as the Low Pow Run mode has been dropped, for which the background is provided in Section 6.1.5. This means that the i.MX RT2660 A0 silicon will only see a limited improved power efficiency as the VDD_CORE minimum voltage is constrained to 0.72V; the BL has accepted this shortcoming for i.MX RT2660 A0 silicon.

Hence, the following body bias strategies shall be deployed in i.MX RT2660.

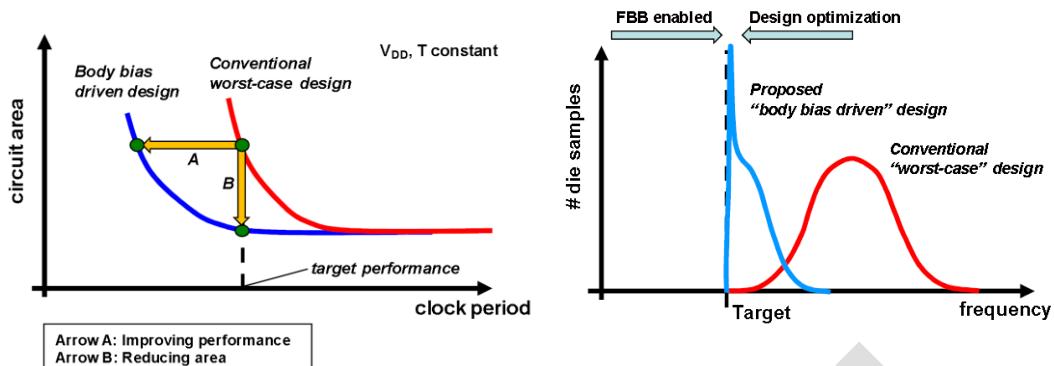


Fig 100. Body bias strategies for i.MX RT2660: body bias driven digital design (left), and process compensation (right)

Body Bias Driven Design: Alleviating worst-case design approach by utilizing FBB enabled logic design for slow PVT conditions, to reduce digital logic over-design and achieving a smaller silicon area for digital logic core [REF]. Also refer to Arrow B in Fig 100(left).

(Slow) Process Compensation: Calibrating slow corner samples with FBB at production test, to achieve target performance [REF]. Fig 100(right) illustrates the approach in combination with Body Bias Driven Design. This calibration is chip sample specific, and trim code shall be stored in OTP. This concerns both balanced or unbalanced silicon outcomes, while calibrating them towards balanced silicon operation at target performance.

8.3.3 IO powering strategy

The i.MX RT2660 is envisioned to make use of three IO sections that can be separately power externally. Fig 101 shows a high-level block diagram of the powering approach for the IO section.

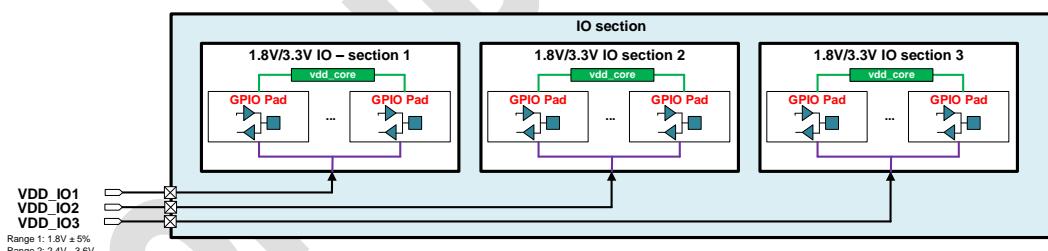


Fig 101. i.MX RT2660 IO powering approach

8.3.4 IO ESD strategy

The i.MX RT2660 has an ESD requirement of 500V CDM and 200V MM while the HBM limit is at 2kV. ESD protection is offered by ensuring the ESD energy is redirected through diodes to the nearest clamp before causing any irreversible damage to the active devices. The i.MX RT2660 uses GO2 devices in PMU and IOs. These devices are protected by clamps present in VDDIO and VSSIO power supply pads. Since a large number of IO supply pads are recommended to keep SSN under the desired threshold, GO2 devices are expected to have sufficient protection.

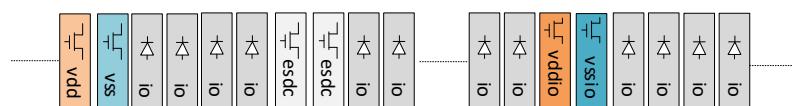


Fig 102. i.MX RT2660 IO ESD strategy using power clamps for GO2 IOs and esd core clamps with vdd and vss pads for GO1 device protection

The strategy for core devices is slightly more complex for i.MX RT2660 since fewer VDD VSS pairs are required relative to VDDIO VSSIO. As shown in Fig 102, additional esdcore clamp cells are available to be used in the IO ring to provide the desired ESD protection. The VDD and VSS GPIO cells need to be also placed when a break or termination of the IO ring is expected.

Fig 103 shows a sample IO section marked with IOs in VDDIO1 section which is always-on. The core side of VDDIO2-3 can be powered down when not used. Such IOs are unmarked in Fig 103. The PMC specific pads are expected to be delivered as part of the PMC macro. This includes input-only tamper pads, pads for crystal oscillators etc. PMC section may reuse the existing GPIOs for providing wakeup pins in the VBAT_SS.

The MEDIA_SS and COMM_SS also have PHYs that have pads associated with them that will require placing within given IO sections. Generally, the IO ring is expected to use VDDIO, VSSIO, VDD and VSS rails as the main rails. These may be broken to provision different sections as needed. In addition to these main power rails, the IO ring is expected to use SWING, POC and RTON rails. The SWING signals the expected voltage swing level on the IO and POCN signals the presence of core supply.

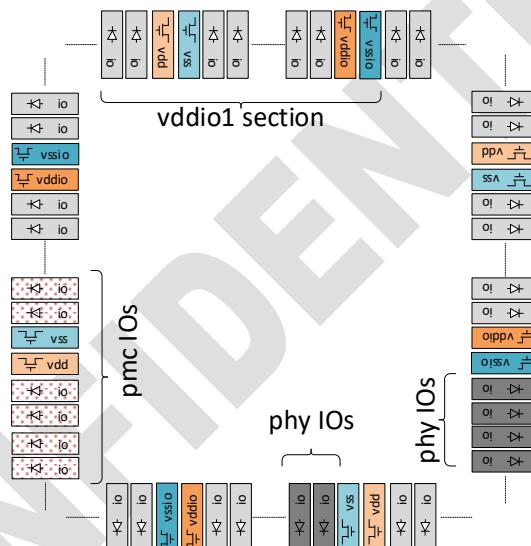


Fig 103. i.MX RT2660 Example IO sections with MFIOs, PHY and PMC IOs

Rails are also required for IO reference voltages (VREFPIO and VREFNIO) that are generated by the BIASGEN cells or by the PMC_SS. As baseline plan, it is currently envisioned that these bias voltages are generated centrally within the PMC_SS; however, the feasibility of this is to be further worked out – currently, gated by the ambiguity on which IO libraries are to be used for i.MX RT2660., i.e. either Synopsys IO or NXP IO library. Once this is cleared out, the IO ESD strategy will be re-checked and revisited when needed. **Decision on the IO libraries including development plan and agreement on the IO specification is a blocking item that needs to be resolved before i.MX RT2660 PDA gate.**

8.4 SoC operating modes

The i.MX RT2660 has four main modes of operation, two transitory and two resident modes. Table 192 lists the high-level modes and the state of major supply rails along with intended body bias conditions per mode. Table 193 describes the entry exit conditions per power mode and a detailed state of the different regulators in the PMU and the SoC rails.

Table 192. SoC operating modes and body bias conditions

Mode	V_{BAT_AON}	V_{DD_CORE}	V_{DDA_1V8}	V_{BB}
POR	X ^[1]	X ^[1]	X ^[1]	ZBB
BOOT	on	on	on	ZBB
ACTIVE	on	on	on	ZBB / FBB, default: ZBB
STANDBY	on	on/off	on/off	ZBB

[1] "X" means that the actual supply voltage level is unclear, i.e. the related supply is being ramped-up in POR mode. At the end of the POR mode, the related supply is turned-on.

[2] Low power domain is always in ZBB mode.

Table 193. SoC operating modes and rail voltages

		Mode	Entry	Exit	V_{DD_CORE}	V_{DD_1V8}	V_{DDA_1V8}	BodyBias [#]	$V_{DD_PLL_0V8}$	$V_{DD_CORE_AON}$	$V_{DD_1V8_AON}$	V_{DD_0V8}	$V_{DDIO}\text{ (1-3)}$	V_{REFIO}^{b}
POR	POR	HW or SW or POR event	PMU and main osc ready	r r r r r r r r r r r r										
BOOT	Boot	POR or LP exit	boot complete or PMU fail	Y O O N Y Y\$ Y\$ Y Y Y Y										
ACTIVE	HP	SW or NP exit	SW or PMU fail	Y Y Y O Y Y\$ Y\$ Y Y Y Y										
	NP	SW or BOOT or LP exit	SW or PMU fail	Y Y Y O Y Y\$ Y\$ Y Y Y Y										
STANDBY	Sleep	SW LP Call	Periph, RTC or GPIO event or PMU fail	Y Y Y O Y Y\$ Y\$ Y Y Y Y										
	Deep Sleep	SW LP Call	Periph, RTC or GPIO event or PMU fail	Y* N Y N Y* Y\$ Y\$ Y* Y Y										
	Power Down	SW LP Call	RTC or GPIO or SYS event or PMU fail	Y** N N N N N Y\$ Y Y* O Y										
	Deep Power Down	SW LP Call	RTC or GPIO or SYS event or PMU fail	N N N N N N Y\$ Y N O Y										

Y = ON, N=OFF, O=optional, r=ramping, * in LP mode, ** in ULP mode. # O=FBB/ZBB and N=ZBB, \$Bypassed to VDD_PMU,

^bShould be derived from VDDIO

The PoR and Boot modes are transitory and are intended to allow a safe and deterministic operating condition for the two resident modes – active and standby. The PoR mode exit into Boot is determined by hardware events (voltage stable and clock valid). Exit from the Boot mode into the resident modes is determined by Boot code.

8.4.1 Active modes

Active operation supports two performance modes: High-Performance Run and Normal Run. These modes allow software to achieve the desired performance or hit a run-time balance between low-power and performance. Additionally, active mode allows a range of forward body bias to be applied to achieve the desired performance. The audio, comms, wake, sys and vbat power domains however always operate with zero body bias.

Table 194. SoC Active modes, rail voltages and body bias conditions.

Mode	VDD_CORE [V]	High-performance domain					Low-power domain			
		compute_clk [MHz]	main_clk [MHz]	media_clk [MHz]	Body Bias	audio_clk [MHz]	comm_clk [MHz]	wake_clk [MHz]	Body Bias	
High-Performance Run	0.9 typ.	>700,	F _{cmpt_clk} /2	F _{cmpt_clk} /2	FBB	≤ 200	≤ 200	≤ 100	ZBB	
	0.945 max.	F _{max} tbd								
	0.81 min.									
Normal Run	0.8 typ.	≤ 700	≤ 350	≤ 350	FBB					
	0.88 max.	≤ 500		≤ 250	≤ 250	ZBB				
	0.72 min.									

[1] In all modes, VDD_1V8 is at 1.8V and VDD_PMC and VDD_PHY are at 0.8V range

8.4.1.1 High-Performance Run

In high performance mode, the core operates at the highest voltage with a frequency chosen to meet the software performance requirement. Forward body bias is applied to all subsystems except the WAKE_SS and VBAT_SS. There is a need to support 0.9V for maximizing the operating frequency although this is not a targeted KPI for RT2660.

8.4.1.2 Normal Run

In Normal performance mode, the core operates with a scaled voltage and the frequency chosen to ensure the right balance between performance and power.

Active mode is terminated after one of the following events:

- Software request to move to STANDBY operation mode ;
- Power-on reset condition ;
- Brownout condition because of battery end-of-life, as detected by software.

8.4.2 Standby modes

Standby modes allow the system to duty cycle itself so as minimize power while providing the required performance. Four standby modes are provisioned as described below.

Table 195. SoC Standby modes, rail voltages and retention conditions

Mode	V _{DDCORE} [V]	Body Bias	Clock Source ^s						Logic and SoG			Memory	IO	
			FRO32k	XOSC32k	LPOSC1M	LPOSC12M	FRO192M	XOSC24/32M	PLL_CORE	PLL_MAIN	PLL_AUDIO	CPU and NPU		
Sleep ³	0.72 to 0.945	FBB / ZBB	Y ¹	Y ¹	Y	Y	Y	Y	Y	Y	Y	WFI	Unused fuctions are clock or power gated	All on, Static
Deep Sleep	0.65 typ	ZBB	Y ¹	Y ¹	Y	Y	Y ²	N	N	N	N	State Retn	All off except DMIC and I2C	64kB default, all mem ³
Power Down	0.55 min 0.65 typ	ZBB	Y ¹	Y ¹	Y	N	N	N	N	N	N	OFF	OFF	≤ 64kB
Deep Power Down	OFF	OFF	Y ¹	Y ¹	N	N	N	N	N	N	N	OFF	OFF	≤ 2kB

¹Either FRO32k or XOSC32k, ²Externally supplied – optional on/off, ³applies to both HP and NP, ⁴peripherals and clock shall be configured prior to entry

8.4.2.1 Sleep Mode

Sleep mode is entered when a fast wake up is desired. The compute cores are clock gated by architecturally supported clock gating mechanisms. Peripherals may be optionally made inactive depending on the application and desired wakeup sources. This mode allows the SRAM to be fully retained.

The body bias setting of the active mode that called the sleep will be retained during sleep to ensure fast response on wake up.

8.4.2.2 Deep Sleep

Deep sleep mode requires greater wakeup time (~150µs) but provides lower power standby state since majority of the high frequency clocks, including PLLs, can be turned off. The compute cores are clock gated similar to sleep mode but peripherals may be optionally power gated depending on the application and desired wakeup sources. This mode allows 64KB SRAM to be retained by default but can be reconfigured to retain the full SRAM content.

8.4.2.3 Power Down

Power down mode requires ~0.5ms wakeup time but provides aggressive power saving since the core leakage is cut off. All oscillators except the RTC is also turned off. NXP memory has build-in power switch, SoC need dedicated control bit for each NXP memory cut. A maximum of 64KB SRAM can be retained but can be reconfigured to retain the full SRAM content. Majority of the IOs can also be powered down although this is a system option since IOs are externally powered.

8.4.2.4 Deep Power Down

In addition to the Power down mode, Deep power down provides improved leakage mitigation by limiting the SRAM retention to 2KB. All oscillators except the RTC, and all IOs except the VBAT_SS and tamper protected IOs can also be turned off. Limited (2KB) SRAM and RTC can be retained so that software can retain essential data for a future restore. All of the rails and SoC is powered down except VBAT_AON rail and SRAM in the VBAT_SS domain. Other than tamper logic and wakeup, no chip functionality is provisioned in this mode. RTC (or TDET) wakeup is possible through PMIC_MODEn pins that update on wakeup. This requires an external PMIC or board level power switch to restore power to the rest of the device (Also supported by existing RT and MCX devices).

8.4.3 IP state by power mode

This section lists the different IP states during the different power modes for implementation and design to check dependencies and also to enable early power estimation activity. Active and sleep are combined here highlighting that fast entry and exit is possible. The tables show the max and min cases with options for the any other combinations as dictated by use-case.

Table 196. i.MX RT2660 Audio SS IP state for different power modes

Item#	P domain	IP	IP type	ACT/SLP max	ACT/SLP Other	ACT/SLP min	DSLP max	DSLP min	PDN	DPDN
1	pd_core	AIPS bridge_AUDIO	BUS	N	N	N	N	N	N	F
2	pd_core	MBC_Pbridge	BUS	N	N	N	N	N	N	F
3	pd_core	AXBS_AUDIO_32b	BUS	N	N	N	N	N	N	F
4	pd_core	TRDC_AUDIO	LOGIC	N	N	N	N	N	N	F
5	pd_core	MODCON_AUDIO	LOGIC	N	N	N	N	N	N	F

Item#	P domain	IP	IP type	ACT/SLP max	ACT/SLP Other	ACT/SLP min	DSLP max	DSLP min	PDN	DPDN
6	pd_core	SLEEPCON_AUDIO	LOGIC	N	Z	Z	N	N	N	F
7	pd_core	DMA_IP_Regs	LOGIC	Z	Z	Z	Z	Z	Z	F
8	pd_core	DMIC0	LOGIC	N	N	N	N	N	N	F
9	pd_core_avc	DMIC1	LOGIC	N	G/F	F	F	F	F	F
10	pd_core	DMIC0_SRAM_0k4	MEM	N	N	N	N	N	N	F
11	pd_core	DMIC0_SRAM_0k8	MEM	N	N	N	N	N	N	F
12	pd_core_avc	DMIC1_SRAM_1k1	MEM	N	G/F	F	F	F	F	F
13	pd_core_avc	DMIC1_SRAM_2k2	MEM	N	G/F	F	F	F	F	F
14	pd_core_avc	MQS	LOGIC	N	G/F	F	F	F	F	F
15	pd_core_avc	SAI0	LOGIC	N	G/F	F	F	F	F	F
16	pd_core_avc	SAI1	LOGIC	N	G/F	F	F	F	F	F
17	pd_core_avc	SAI2	LOGIC	N	G/F	F	F	F	F	F
18	pd_core	XBAR_AUDIO	LOGIC	N	N	N	N	N	N	F
19	pd_core_avc	FREQME_AUDIO	LOGIC	N	G/F	F	F	F	F	F
20	pd_core	DMA_8CH	LOGIC	N	N	N	N	N	N	F
21	pd_core_avc	ASRC_ROM	LOGIC	N	G/F	F	F	F	F	F
22	pd_core_avc	ASRC_RAM	LOGIC	N	G/F	F	F	F	F	F
23	pd_core_avc	ASRC	LOGIC	N	G/F	F	F	F	F	F
24	pd_core	RAM8kB_AUDIO	MEM	N	N	N	N	N	N	F
25	pd_core	RAM_AUDIO_CTRL	LOGIC	Z	N	N	N	N	N	F
26	pd_core	DAC_AUDIO_DMA	BUS	Z	N	N	N	N	N	F
27	pd_core	RAM_AUDIO_MBC	BUS	Z	N	N	N	N	N	F
28	pd_core_avc	SPDIF_XCVR	LOGIC	N	G/F	F	F	F	F	F
29	pd_core	SPDIF_XCVR_MBC	BUS	N	N	N	N	N	N	F

N=ON, G= clock gated, R=retn, F=Off, all IPs are in vdd_core voltage domain

Table 197. i.MX RT2660 CGU SS IP state for different power modes

Item#	P domain	V domain	IP	IP type	ACT/SLP max	ACT/SLP Other	ACT/SLP min	DSLP max	DSLP min	PDN	DPDN
1	pd_pmu	vdd_pmu	XO32M	MSIP	N	N	N	F	F	F	F
2	pd_pmu	vdd_pmu	PLL0	MSIP	Z	N	N	F	F	F	F
3	pd_pmu	vdd_pmu	PLL1	MSIP	Z	N	N	F	F	F	F
4	pd_pmu	vdd_pmu	PLL2	MSIP	Z	N	N	F	F	F	F
5	pd_pmu	vdd_pmu	PLL3	MSIP	Z	N	N	F	F	F	F
6	pd_pmu	vdd_pmu	FRO192M	MSIP	Z	N	N	N	N	N	F
7	pd_pmu	vdd_pmu	LPFRO12M	MSIP	Z	N	N	N	N	N	F
8	pd_core	vdd_core	FRO_TUNER	LOGIC	N	N	N	N	N	N	F
9	pd_core	vdd_core	PMC_CONFIG	LOGIC	N	N	N	N	N	N	F
10	pd_core	vdd_core	CGU_CONFIG	LOGIC	N	N	N	N	N	N	F
11	pd_core	vdd_core	CGU_DIG	LOGIC	N	N	N	N	N	N	F

N=ON, G= clock gated, R=retn, F=Off, vdd_pmu can be multiple voltages for MSIP

Table 198. i.MX RT2660 COMM SS IP state for different power modes

Item#	IP	IP type	ACT/SLP max	ACT/SLP Other	ACT/SLP min	DSLP max	DSLP min	PDN	DPDN
1	AIPS_bridge_COMM	BUS	N	G/F	F	F	F	F	F
2	AHB_Splitter_COMM	BUS	N	G/F	F	F	F	F	F
3	MBC_AhbSplitter	BUS	N	G/F/R	F	R	F	F	F
4	NIC_COMM_64b	BUS	N	G/F	F	F	F	F	F

Item#	IP	IP type	ACT/SLP max	ACT/SLP Other	ACT/SLP min	DSP max	DSP min	PDN	DPDN
5	TRDC_COMM	LOGIC	N	G/F/R	F	R	F	F	F
6	SLEEPCON_COMM	LOGIC	N	G/F/R	F	R	F	F	F
7	MODCON_COMM	LOGIC	N	G/F/R	F	R	F	F	F
8	COMM_IP_Regs	LOGIC	N	G/F/R	F	R	F	F	F
9	uSDHC0	LOGIC	N	G/F	F	F	F	F	F
10	uSDHC1	LOGIC	N	G/F	F	F	F	F	F
11	USB0_HS	LOGIC	N	G/F	F	F	F	F	F
12	USB1_FS	LOGIC	N	G/F	F	F	F	F	F
13	USB0_HS_PHY*	MSIP	N	G/F	F	F	F	F	F
14	USB1_FS_PHY*	MSIP	N	G/F	F	F	F	F	F
15	XSPI Responder	LOGIC	N	G/F	F	F	F	F	F
16	ETH0 1G QoS	LOGIC	N	G/F	F	F	F	F	F
17	ETH1 1G	LOGIC	N	G/F	F	F	F	F	F
18	DAC_uSDHC0	BUS	N	G/F/R	F	R	F	F	F
19	DAC_uSDHC1	BUS	N	G/F/R	F	R	F	F	F
20	DAC_USB0_HS	BUS	N	G/F/R	F	R	F	F	F
21	DAC_USB1_FS	BUS	N	G/F/R	F	R	F	F	F
22	DAC_XSPI Responder	BUS	N	G/F/R	F	R	F	F	F
23	DAC_ETH0 1G QoS	BUS	N	G/F/R	F	R	F	F	F
24	DAC_ETH1 1G_0	BUS	N	G/F/R	F	R	F	F	F
25	DAC_ETH1 1G_1	BUS	N	G/F/R	F	R	F	F	F
26	XENO0	LOGIC	N	G/F	F	F	F	F	F
27	XENO1	LOGIC	N	G/F	F	F	F	F	F
28	XBAR	LOGIC	N	G/F	F	F	F	F	F
29	FREQME	LOGIC	N	G/F	F	F	F	F	F

N=ON, G= clock gated, R=retn, F=Off, all IPs belong to pd_core_avc power domain and vdd_core voltage domain except the USB Phys

Table 199. i.MX RT2660 COMPUTE SS IP state for different power modes

Item#	IP	IP type	ACT/SLP max	ACT/SLP Other	ACT/SLP min	DSP max	DSP min	PDN	DPDN
1	N256S	LOGIC	N	G/R/F	F	R	F	F	F
2	NPU-ECC	LOGIC	N	G/R/F	F	R	F	F	F
3	s-AXI	LOGIC	N	G/F	F	F	F	F	F
4	m-AXI	LOGIC	N	G/F	F	F	F	F	F
5	mem-NPU-ECC	LOGIC	N	G/F	F	F	F	F	F
6	96kB TCM	MEM	N	G/F	F	F	F	F	F
7	256kB NPU TCM	MEM	N	N	N	F	F	F	F
8	CM85	LOGIC	N	N	N	R	R	F	F
9	p-AHB	BUS	N	N	N	F	F	F	F
10	s-AHB	BUS	N	N	N	F	F	F	F
11	m-AXI	BUS	N	N	N	F	F	F	F
12	d-AHB	BUS	N	N	N	F	F	F	F
13	mem-M85-ECC	LOGIC	N	N	N	F	F	F	F
14	32k L1 Dcache	MEM	N	N	N	F	F	F	F
15	32k L1 Icache	MEM	N	N	N	F	F	F	F
16	256kB M85 TCM	MEM	N	N	N	R	R	F	F
17	AHB2AXI	LOGIC	N	N	N	F	F	F	F
18	Coresight Trace	LOGIC	N	N	N	F	F	F	F
19	Coresight DAP	LOGIC	N	N	N	F	F	F	F
20	NIC_MEM_64b	BUS	N	N	N	F	F	F	F
21	TRDC_COMP	LOGIC	N	N	N	R	R	F	F
22	SLEEPCON_COMP	LOGIC	N	N	N	R	R	F	F

Item#	IP	IP type	ACT/SLP max	ACT/SLP Other	ACT/SLP min	DSLP max	DSLP min	PDN	DPDN
23	MODCON_COMP	LOGIC	N	N	N	R	R	F	F
24	COMP_IP_Regs	LOGIC	Z	Z	Z	R	R	F	F
25	MBC_COMP	BUS	N	N	N	R	R	F	F
26	MRC_MEM0	BUS	N	N	N	R	R	F	F
27	MRC_MEM1	BUS	N	N	N	R	R	F	F
28	MRC_MEM2	BUS	N	N	N	R	R	F	F
29	MRC_MEM3	BUS	N	N	N	R	R	F	F
30	DAC_M85	BUS	N	N	N	R	R	F	F
31	DAC_NPU	BUS	N	N	N	R	R	F	F
32	MRC_M85	BUS	N	N	N	R	R	F	F
33	MRC_NPU	BUS	N	N	N	R	R	F	F
34	MRC_ROM	BUS	N	N	N	R	R	F	F
35	ROM_CTRL	LOGIC	N	N	N	F	F	F	F
36	ROM128kB	MEM	N	N	N	F	F	F	F
37	MEM0_RAM_CTRL	LOGIC	N	N	N	F	F	F	F
38	MEM1_RAM_CTRL	LOGIC	N	N	N	F	F	F	F
39	MEM2_RAM_CTRL	LOGIC	N	N	N	F	F	F	F
40	MEM3_RAM_CTRL	LOGIC	N	N	N	F	F	F	F
41	MEM0_256kB	MEM	N	N	N	R	R	F	F
42	MEM1_256kB	MEM	N	N	N	R	R	F	F
43	MEM2_256kB	MEM	N	N	N	R	R	F	F
44	MEM3_256kB	MEM	N	N	N	R	R	F	F
45	MEM0_ECC	LOGIC	N	N	N	F	F	F	F
46	MEM1_ECC	LOGIC	N	N	N	F	F	F	F
47	MEM2_ECC	LOGIC	N	N	N	F	F	F	F
48	MEM3_ECC	LOGIC	N	N	N	N	N	F	F
49	AHB_SPLITTER_COMP	BUS	N	N	N	N	N	F	F
50	PBRIDGE_COMP	BUS	N	N	N	N	N	F	F

N=ON, G= clock gated, R=retn, F=Off, all IPs belong to pd_core_main power domain and vdd_core voltage domain

Table 200. i.MX RT2660 MAIN_HSP_SS IP state for different power modes

Item#	IP	IP type	ACT/SLP max	ACT/SLP Other	ACT/SLP min	DSLP max	DSLP min	PDN	DPDN
1	HSP_AHBSplitter	BUS	N	N	N	F	F	F	F
2	HSP_PBridge0	BUS	N	N	N	F	F	F	F
3	HSP_Pbridge1	BUS	N	N	N	F	F	F	F
4	GPIO0	LOGIC	N	N	N	F	F	F	F
5	GPIO1	LOGIC	N	N	N	F	F	F	F
6	GPIO2	LOGIC	N	N	N	F	F	F	F
7	GPIO3	LOGIC	N	N	N	F	F	F	F
8	GPIO4	LOGIC	N	N	N	F	F	F	F
9	ADC0	MSIP	N	N	N	F	F	F	F
10	ADC1	MSIP	N	N	N	F	F	F	F
11	DAC	MSIP	N	N	N	F	F	F	F
12	ADC0_CTRL	LOGIC	N	N	N	F	F	F	F
13	ADC1_CTRL	LOGIC	N	N	N	F	F	F	F
14	DAC_CTRL	LOGIC	N	N	N	F	F	F	F
15	CSSI_MU2	LOGIC	N	N	N	F	F	F	F
16	CSSI_MU1	LOGIC	N	N	N	F	F	F	F
17	EVTG0	LOGIC	N	N	N	F	F	F	F
18	EVTG1	LOGIC	N	N	N	F	F	F	F
19	HSP_XABR0	LOGIC	N	N	N	F	F	F	F

Item#	IP	IP type	ACT/SLP max	ACT/SLP Other	ACT/SLP min	DSLP max	DSLP min	PDN	DPDN
20	HSP_XBAR1	LOGIC	N	N	N	F	F	F	F
21	TRGSYNC	LOGIC	Z	Z	Z	F	F	F	F
22	eFLEXPWM2	LOGIC	N	N	N	F	F	F	F
23	eFLEXPWM3	LOGIC	N	N	N	F	F	F	F
24	QDEC2	LOGIC	N	N	N	F	F	F	F
25	QDEC3	LOGIC	N	N	N	F	F	F	F
26	QTPM1	LOGIC	N	N	N	F	F	F	F
27	QTPM2	LOGIC	N	N	N	F	F	F	F
28	LPIT1	LOGIC	N	N	N	F	F	F	F
29	FLEXIO2	LOGIC	N	N	N	F	F	F	F
30	IOCON2	LOGIC	N	N	N	F	F	F	F
31	IOCON3	LOGIC	N	N	N	F	F	F	F
32	IOCON4	LOGIC	N	N	N	F	F	F	F
33	LPUART3	LOGIC	N	N	N	F	F	F	F
34	LPUART4	LOGIC	N	N	N	F	F	F	F
35	LPUART5	LOGIC	N	N	N	F	F	F	F
36	LP SPI3	LOGIC	N	N	N	F	F	F	F
37	LP SPI4	LOGIC	N	N	N	F	F	F	F
38	LPI2C1	LOGIC	N	N	N	F	F	F	F
39	CAN-FD2	LOGIC	N	N	N	F	F	F	F
40	SINC1	LOGIC	N	N	N	F	F	F	F
41	EVTG2	LOGIC	N	N	N	F	F	F	F
42	EVTG3	LOGIC	N	N	N	F	F	F	F
43	IOCON0	LOGIC	N	N	N	F	F	F	F
44	IOCON1	LOGIC	N	N	N	F	F	F	F
45	LPUART0	LOGIC	N	N	N	F	F	F	F
46	LPUART1	LOGIC	N	N	N	F	F	F	F
47	LP SPI0	LOGIC	N	N	N	F	F	F	F
48	LP SPI1	LOGIC	N	N	N	F	F	F	F
49	LP SPI2	LOGIC	N	N	N	F	F	F	F
50	LPI2C0	LOGIC	N	N	N	F	F	F	F
51	I3C0	LOGIC	N	N	N	F	F	F	F
52	CAN-FD0	LOGIC	N	N	N	F	F	F	F
53	CAN-FD1	LOGIC	N	N	N	F	F	F	F
54	CSSI_MU0	LOGIC	N	N	N	F	F	F	F
55	FLEXIO0	LOGIC	N	N	N	F	F	F	F
56	FLEXIO1	LOGIC	N	N	N	F	F	F	F
57	eFLEXPWM0	LOGIC	N	N	N	F	F	F	F
58	eFLEXPWM1	LOGIC	N	N	N	F	F	F	F
59	QDEC0	LOGIC	N	N	N	F	F	F	F
60	QDEC1	LOGIC	N	N	N	F	F	F	F
61	QTPM0	LOGIC	N	N	N	F	F	F	F
62	LPIT0	LOGIC	N	N	N	F	F	F	F
63	SINCO	LOGIC	N	N	N	F	F	F	F

N=ON, G= clock gated, R=retn, F=Off, all IPs belong to pd_core_main power domain and vdd_core voltage domain except the MSIPs

Table 201. i.MX RT2660 MAIN SS IP state for different power modes

Item#	IP	IP type	ACT/SLP max	ACT/SLP Other	ACT/SLP min	DSLP max	DSLP min	PDN	DPDN
1	TRDC_MAIN	LOGIC	N	N	N	R	R	F	F
2	SLEEPCON_MAIN	LOGIC	N	N	N	R	R	F	F
3	MODCON_MAIN	LOGIC	N	N	N	R	R	F	F

Item#	IP	IP type	ACT/SLP max	ACT/SLP Other	ACT/SLP min	DSLP max	DSLP min	PDN	DPDN
4	MAIN_IP_Regs	LOGIC	N	Z	Z	R	R	F	F
5	ATX	MSIP	Z	Z	Z	F	F	F	F
6	ATX_CTRL	LOGIC	N	N	N	F	F	F	F
7	DMA0 Reg	LOGIC	N	N	N	F	F	F	F
8	DMA1 Reg	LOGIC	N	N	N	F	F	F	F
9	PVT MON	LOGIC	N	N	N	F	F	F	F
10	FREQME_MAIN	LOGIC	N	N	N	F	F	F	F
11	DAC_CSSI	BUS	N	N	N	R	R	F	F
12	DAC_DEBUG	BUS	N	N	N	R	R	F	F
13	DAC_TESTP	BUS	N	N	N	R	R	F	F
14	DAC_CM85	BUS	N	N	N	R	R	F	F
15	DAC_DMA1	BUS	N	N	N	R	R	F	F
16	DAC_DMA0	BUS	N	N	N	R	R	F	F
17	DAC_ETR	BUS	N	N	N	R	R	F	F
18	MBC_MAIN_Pbridge	BUS	N	N	N	R	R	F	F
19	MBC_HSP_Pbridge0	BUS	N	N	N	R	R	F	F
20	MBC_HSP_Pbridge1	BUS	N	N	N	R	R	F	F
21	MBC_MAIN_GPIO	BUS	N	N	N	R	R	F	F
22	MBC_MAIN_AVC	BUS	N	N	N	R	R	F	F
23	MRC_XSPI0	BUS	N	N	N	R	R	F	F
24	MRC_XSPI1	BUS	N	N	N	R	R	F	F
25	MRC_XSPI2	BUS	N	N	N	R	R	F	F
26	MRC_SRAMC	BUS	N	N	N	R	R	F	F
27	MRC_LLC	BUS	N	N	N	R	R	F	F
28	DMA1-32Ch	LOGIC	N	N	N	F	F	F	F
29	Pbridge_AXBS	BUS	N	N	N	F	F	F	F
30	AHBSplitter_AXBS	BUS	N	N	N	F	F	F	F
31	AHBSplitter_AVC	BUS	N	N	N	F	F	F	F
32	AXBS_MAIN_32b	BUS	N	N	N	F	F	F	F
33	CSSI-110	LOGIC	N	N	N	R	R	F	F
34	CSSI_ROM	MEM	N	N	N	F	F	F	F
35	CSSI OTP	MEM	N	N	N	F	F	F	F
36	CSSI_IMEM	MEM	N	N	N	F	F	F	F
37	CSSI_DMEM	MEM	N	N	N	F	F	F	F
38	CSSI_PKCRAM	MEM	N	N	N	F	F	F	F
39	CSSI_DMA_RAM	MEM	N	N	N	F	F	F	F
40	LLC	LOGIC	N	N	N	F	F	F	F
41	DMA-16ch	LOGIC	N	N	N	F	F	F	F
42	NIC_MAIN_64b	LOGIC	N	N	N	F	F	F	F
43	SRAMC	LOGIC	N	N	N	F	F	F	F
44	XSPI0	LOGIC	N	N	N	F	F	F	F
45	XSPI1	LOGIC	N	N	N	F	F	F	F
46	XSPI2	LOGIC	N	N	N	F	F	F	F
47	XSPI0_IPED_CTR	LOGIC	N	N	N	F	F	F	F
48	XSPI1_XEX	LOGIC	N	N	N	F	F	F	F
49	XSPI2_XEX	LOGIC	N	N	N	F	F	F	F

N=ON, G= clock gated, R=retn, F=Off, all IPs belong to pd_core_main power domain and vdd_core voltage domain except the ATX MSIP

Table 202. i.MX RT2660 MEDIA SS IP state for different power modes

Item#	IP	IP type	ACT/SLP max	ACT/SLP Other	ACT/SLP min	DSLP max	DSLP min	PDN	DPDN
1	TRDC_MEDIA	LOGIC	N	G/R/F	F	R	F	F	F

Item#	IP	IP type	ACT/SLP max	ACT/SLP Other	ACT/SLP min	DSLP max	DSLP min	PDN	DPDN
2	MODCON_MEDIA	LOGIC	N	G/R/F	F	R	F	F	F
3	SLEEPCON_MEDIA	LOGIC	N	G/R/F	F	R	F	F	F
4	MEDIA_IP_Regs	LOGIC	N	G/R/F	F	R	F	F	F
5	FREQME_MEDIA	LOGIC	N	G/F	F	F	F	F	F
6	AIPS bridge_MEDIA	BUS	N	G/F	F	F	F	F	F
7	AHB_Splitter_MEDIA	BUS	N	G/F	F	F	F	F	F
8	MBC_AhbSplitter	BUS	N	G/R/F	F	R	F	F	F
9	NIC MEDIA_64b	BUS	N	G/F	F	F	F	F	F
10	MIPI CSI	LOGIC	N	G/F	F	F	F	F	F
11	MIPI RX PHY	MSIP	N	G/F	F	F	F	F	F
12	MIPI DS1	LOGIC	N	G/F	F	F	F	F	F
13	MIPI TX PHY	MSIP	N	G/F	F	F	F	F	F
14	ISI	LOGIC	N	G/F	F	F	F	F	F
15	ISI_DAC0	BUS	N	G/R/F	F	R	F	F	F
16	ISI_DAC1	BUS	N	G/R/F	F	R	F	F	F
17	ISI_DAC2	BUS	N	G/R/F	F	R	F	F	F
18	VIDEO_MUX	LOGIC	N	G/F	F	F	F	F	F
19	DCIF	LOGIC	N	G/F	F	F	F	F	F
20	DCIF_DAC	BUS	N	G/R/F	F	R	F	F	F
21	GPU	LOGIC	N	G/F	F	F	F	F	F
22	JPEG	LOGIC	N	G/F	F	F	F	F	F
23	GPU_DAC	BUS	N	G/R/F	F	R	F	F	F
24	JPEG_DAC	BUS	N	G/R/F	F	R	F	F	F

N=ON, G= clock gated, R=retn, F=Off, all IPs belong to pd_core_avc power domain and vdd_core voltage domain except the MIPI Phys

Table 203. i.MX RT2660 WAKE and SYS SS IP state for different power modes

Item#	IP	IP type	ACT/SLP max	ACT/SLP Other	ACT/SLP min	DSLP max	DSLP min	PDN	DPDN
1	SWT0	LOGIC	N	N	N	N	N	N	F
2	SWT1	LOGIC	N	N	N	N	N	N	F
3	EWM	LOGIC	N	N	N	N	N	N	F
4	Quad TPM	LOGIC	N	N	N	N	N	N	F
5	LP TIMER 0	LOGIC	N	N	N	N	N	N	F
6	LP TIMER 1	LOGIC	N	N	N	N	N	N	F
7	ACMP0-3 CTRL	LOGIC	N	N	N	N	N	N	F
8	SLEEPCON_WAKE	LOGIC	N	N	N	N	N	N	F
9	MODCON_WAKE	LOGIC	N	N	N	N	N	N	F
10	LPSPI - 16 word FIFO	LOGIC	N	N	N	N	N	N	F
11	LPI2C - 8 word FIFO	LOGIC	N	N	N	N	N	N	F
12	LPUART- 16 word FIFO	LOGIC	N	N	N	N	N	N	F
13	I3C	LOGIC	N	N	N	N	N	N	F
14	IOMUX	LOGIC	N	N	N	N	N	N	F
15	GPIO (per pin)	LOGIC	N	N	N	N	N	N	F
16	AIPS bridge_WAKE	BUS	N	N	N	N	N	N	F
17	XBAR	LOGIC	N	N	N	N	N	N	F
18	FREQME	LOGIC	N	N	N	N	N	N	F
19	IOCON	LOGIC	N	N	N	N	N	N	F
20	POWERCON*	LOGIC	N	N	N	N	N	N	F
21	RESETCON*	LOGIC	N	N	N	N	N	N	F

N=ON, G= clock gated, R=retn, F=Off, all IPs belong to pd_core power domain and vdd_core voltage domain, *=SYS subsystem, WAKE otherwise

Table 204. i.MX RT2660 PMC SS IP state for different power modes

Item#	IP	IP type	ACT/SLP max	ACT/SLP Other	ACT/SLP min	DSLP max	DSLP min	PDN	DPDN
1	PMC_DIG	LOGIC	N	N	N	N	N	N	F
2	DCDC_CORE	MSIP	N	N	N	N	N	N	F
3	LDOA_1V8	MSIP	N	N	N	N	N	N	F
4	LDO_1V5	MSIP	N	N	N	N	N	N	F
5	LDOC_0V8	MSIP	N	N	N	N	N	N	F
6	HQ Refs	MSIP	N	N	N	F	F	F	F
7	VBAT_POR	MSIP	N	N	N	N	N	N	F
8	LVD/HVD	MSIP	N	N	N	N	N	N	F
9	AGDET	MSIP	N	N	N	N	N	N	F
10	Temp Det	MSIP	N	N	N	N	N	N	F
11	Body Bias	MSIP	N	N	N	F	F	F	F
12	LPFRO_1M	MSIP	N	N	N	N	N	N	F
13	LDO_1V8	MSIP	N	N	N*	F	F	F	F
14	LDO_0V8@	MSIP	N	N	N	N	N	N	F
15	Monitors	MSIP	N	N	N	N	N	N	F

N=ON, G= clock gated, R=retn, F=Off, all IPs belong to pd_pmu power domain and vdd_pmu voltage domain, *needed for body bias

@PHY rails are switched off.

Table 205. i.MX RT2660 VBAT SS IP state for different power modes

Item#	V domain	IP	IP type	ACT/SLP max	ACT/SLP Other	ACT/SLP min	DSLP max	DSLP min	PDN	DPDN
1	vdd_core_aon	RTC*	LOGIC	N	N	N	N	N	N	N
2	vdd_core_aon	LPTMR*	LOGIC	N	N	N	Z	Z	Z	Z
3	vdd_core_aon	IOCON*	LOGIC	N	N	N	Z	Z	Z	Z
4	vdd_core_aon	GPIO (per pin) *	LOGIC	N	N	N	N	N	N	N
5	vdd_core_aon	Backup Register*	LOGIC	N	N	N	N	N	N	N
6	vdd_core_aon	2kB Backup RAM	MEM	N	N	N	N	N	N	N
7	vdd_core_aon	TDET_CTRL*	LOGIC	N	N	N	N	N	N	N
8	vbat_aon	LP Refs	MSIP	N	N	N	N	N	N	N
9	vbat_aon	VBAT_POR	MSIP	N	N	N	N	N	N	N
10	vbat_aon	FRO32k\$	MSIP	F	F	F	F	F	F	F
11	vbat_aon	XO32k	MSIP	N	N	N	N	N	N	N
12	vbat_aon	IO_AON	MSIP	N	N	N	N	N	N	N
13	vbat_aon	LDO_0V8	MSIP	N	N	N	N	N	N	N
14	vbat_aon	LDO_1V8	MSIP	N	N	N	N	N	N	N
15	vbat_aon	Pwr MUX	MSIP	N	N	N	N	N	N	N
16	vbat_aon	VBAT_DIG	MSIP	N	N	N	N	N	N	N
17	vbat_aon	VBAT_0V8_POR	MSIP	N	N	N	N	N	N	N
18	vbat_aon	VBAT_1V8_POR	MSIP	N	N	N	N	N	N	N
19	vdd_core_aon	VBATCON*	LOGIC	N	N	N	N	N	N	N

N=ON, G= clock gated, R=retn, F=Off, all IPs belong to pd_vbat power domain, *logic in uHVT, \$ ON during boot, XO selected after boot

8.4.4 Mode transitioning

Transition between active modes and to from standby modes is sequenced by software and hardware and/or external events. Before a transition, software must program the SYSCON registers informing the hardware of the intended mode on subsequent SLEEP. Once programmed, the CPU can enter WFI which asserts the core's SLEEPING signal. This is captured by the PMU and after handshaking to ensure that there are interim interrupts or events causing the SLEEP request to be voided, the PMU initiates the mode transition.

This allows for a clean mode transition with no clock or reset cross overs getting affected. When in standby modes, the exit back to Active mode is initiated by external (interrupts on GPIO) or hardware events (RTC, Timer, ADC etc.) Once again, the software should preprogram SYSCON before standby entry, as to which Active mode to enter when the standby exit conditions are satisfied.

Battery backed mode is an exception to this since all of the SoC, except retention portions of the VBAT_SS, is turned off. Upon wakeup the SoC is expected to restart from a normal PoR. It is the responsibility of the bootcode to determine how retained contents in the VBAT_SS will be utilized in the boot and process and thereafter.

8.4.5 SoC power sequences

Transition between active modes and to from standby modes is sequenced by software and hardware and/or external events. Before a transition, software must program the SYSCON registers informing the hardware of the intended mode on subsequent SLEEP. Once programmed, the CPU can enter WFI which asserts the core's SLEEPING signal. This is captured by the PMU and after handshaking to ensure that there are interim interrupts or events causing the SLEEP request to be voided, the PMU initiates the mode transition.

This allows for a clean mode transition with no clock or reset cross overs getting affected. When in standby modes, the exit back to Active mode is initiated by external (interrupts on GPIO) or hardware events (RTC, Timer, ADC etc.) Once again, the software should preprogram SYSCON before standby entry, as to which Active mode to enter when the standby exit conditions are satisfied.

Deep power down mode is an exception to this since all of the SoC, except retention portions of the VBAT_SS, is turned off. Upon wakeup the SoC is expected to restart from a normal PoR. It is the responsibility of the bootcode to determine how retained contents in the VBAT_SS will be utilized in the boot and process and thereafter.

8.4.5.1 SoC power-up sequence

From power-up, all domains necessary for boot will be turned on (as in active normal-performance mode). Specialist IPs, PLLs and PHYs etc. can remain off. No FBB is applied. The core DCDC starts with default trims to power the core logic. Finer trims and mode specific trims are loaded later once the security system has authenticated the settings or images. From this power-up state, the PMU has to signal *PGOOD* and *CLK_VALID* to indicate that the rail voltages and clocks required for boot are functional and safe. This combination releases the security core from reset.

The security core first loads the ROM patch data to address any bootcode or data table issues. The secure core under control of boot code then evaluates the security and life-cycle registers to determine the remainder of the sequence.

Depending on the chosen boot sequence, normal or ISP or security-failed. In case of security failure, the device enters infinite sleep or ISP mode depending on lifecycle setting.

ISP mode uses serial download through SPI, UART, USB or other device pins. The exact mode used depends on boot_config which is populated using pin status as read during POR exit.

Normal mode is where the secure core hands off to the main core to execute from a preloaded image. In normal mode, the secure core locates the boot image and execute secure boot if security is enabled. Optionally, TRDC default settings is loaded and Trustzone is configured. After this the main core is ready for image execution. As part of normal boot, the device may be configured to perform a fast low-power boot to support power down with retention conditions. This routine skips image authentication to enable faster boot.

If a debugger is detected during the boot process, the debug elements are activated and the boot control is transferred to debugger.

The trigger for the SoC to power up is the presence of VDD_PMU and VBAT_AON supplies along with a rising edge on the POR_b pin. This starts the PMU boot process starting from internal references and the LDO_1V5 in the PMU. This powers up internal regulators, higher precision references and the 1MHz LPOSC. This oscillator starts the FSM which sequences further all the oscillators before handing off control for digital sequencing.

The sequence is enumerated below while finer details are being worked out:

1. VDD_PMU and VBAT_PWR_OK are triggered when input supply has settled at the correct levels
2. Internal references and LVD/HVD assert starting the PMU internal FSM
3. The DCDC is initialized in PFM mode which asserts the VDD_CORE valid signal
4. CGU starts the 192MHz FRO clock
5. This triggers the SOC_PWR_OK signal which starts the trim load sequence. OTP uses the 24MHz (divided from FRO192M) clock.
6. When trims are complete, the trims are latched in the PMU internal 1.5V domain.
 - a. Untrimmed devices will assert trim_error signal
7. The PMU will restart with new trim values and clocks will be restarted.
8. Trim autoload complete is signalled which causes DCDC to switch to PWM mode.
9. The HW POR mode is ended once the generated power supplies are available, and the SoC is set to operate in Normal mode at 500 MHz main_rootclk frequency.
10. Next the BOOT mode is reached, the security core starts and memory repair is initiated.
11. Reset negates and CM85 is ready to boot from ROM.

The SoC power up sequence is to be confirmed by the PMU team.

8.4.5.2 SoC LP entry sequence

RT2660 LP ENTRY SEQUENCE (V0p1)
July 2, 2024

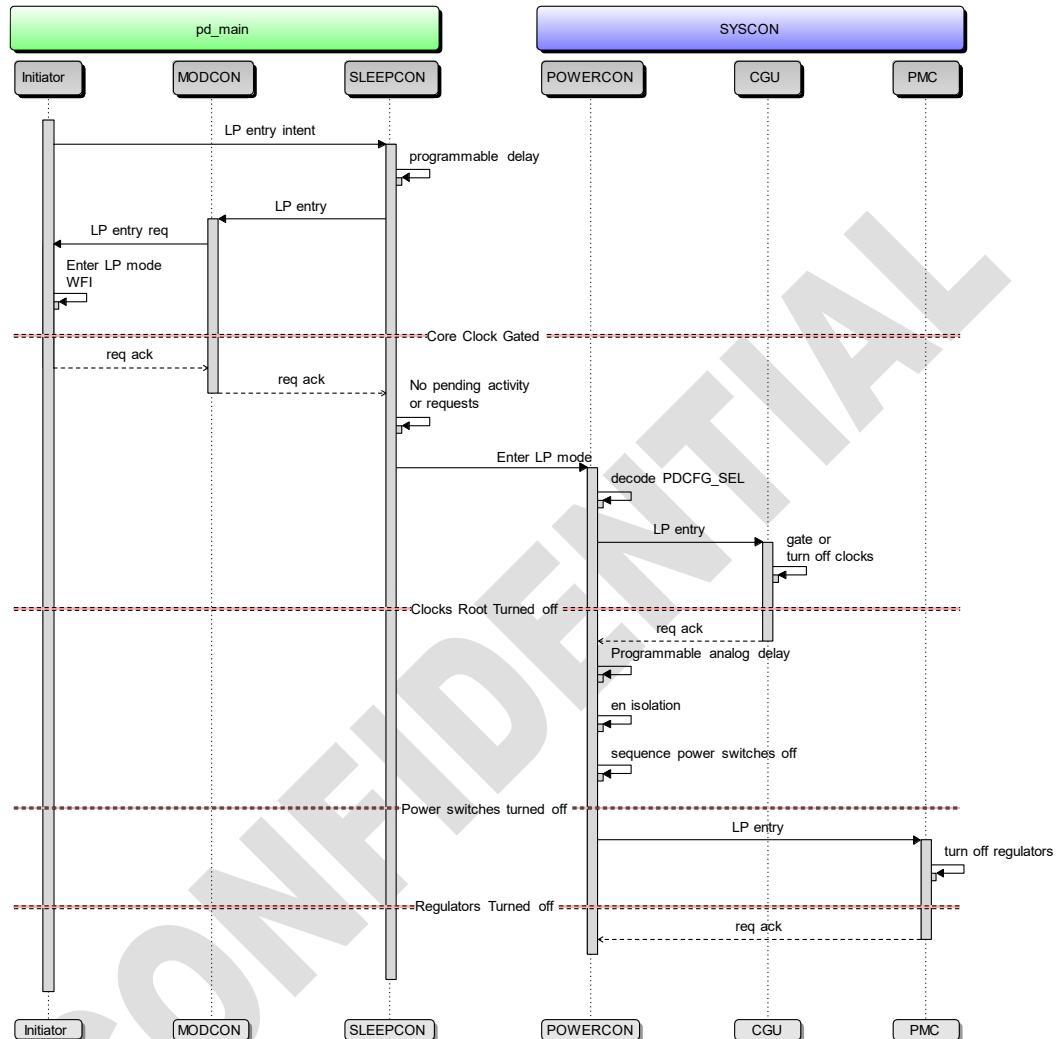


Fig 104. i.MX RT2660 LP entry sequence

LP Entry starts with the initiator subsystem (Typically compute SS) with the initiator (Typically CPU or NPU) signalling to the SLEEPCON its LP entry intent. The SLEEPCON aggregates these requests and uses a programmable delay to preempt any immediate wakeup requests. If no further mode change requests appear within this timeout period, the SLEEPCON signals MODCON for reset and clock control. The MODCON has further handshakes with initiator to ensure a clean LP entry by the initiator and acknowledges to the SLEEPCON.

Assuming no pending requests to switch to active mode and depending on the LP mode (deepsleep, powerdown or deep powerdown), the SLEEPCON then signals to the POWERCON to enter LP mode. The POWERCON now decodes the PDCFG and sequences all tasks in this process. It first signals LP entry to CGU which can turn off root clocks. The POWERCON then uses an analog delay to

preempt any immediate wakeup requests. If no further mode change requests are pending, power switches are turned off (no sequencing for turning off).

The POWERCON then signals the PMC to turn off unused regulators. This completes the LP entry sequence.

8.4.5.3 SoC LP exit sequence

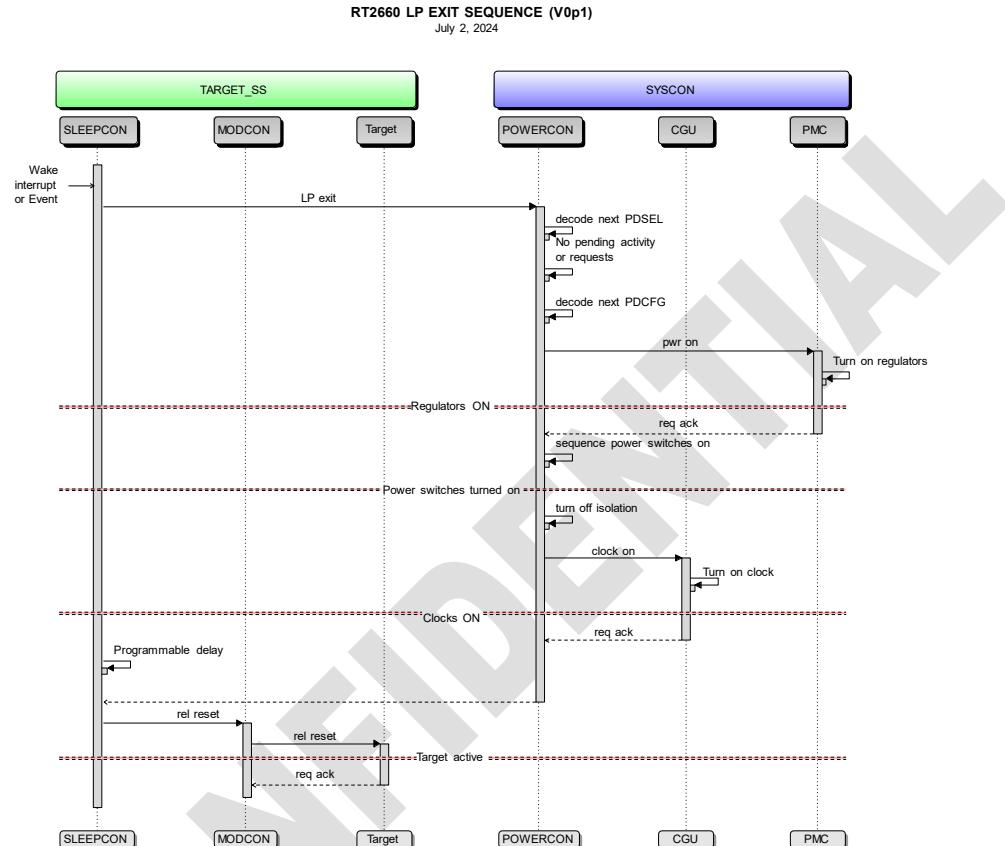


Fig 105. i.MX RT2660 LP exit sequence

Exit from LP modes is triggered by wakeup events in the SoC or external interrupts on GPIOs. These are currently configured to be received in WAKE_SS. This initiates the SLEEPCON to start the LP exit sequence. It is assumed that the clocks are off for the lowest power modes and hence the SLEEPCON triggers the powercon to configure the voltage regulators through the PMC. Once the voltages are stable, the POWERCON sequences on the power switches for the various switchable domains as required by the wake configuration set up. The isolation is disengaged and the clock is started through the interface to the CGU. Once the clocks are configured for the wake up state, the SLEEPCON triggers the MODCON to wake the target subsystem.

8.4.5.4 SoC LP active mode change sequence

RT2660 ACTIVE MODE CHANGE SEQUENCE (V0p1)
July 2, 2024

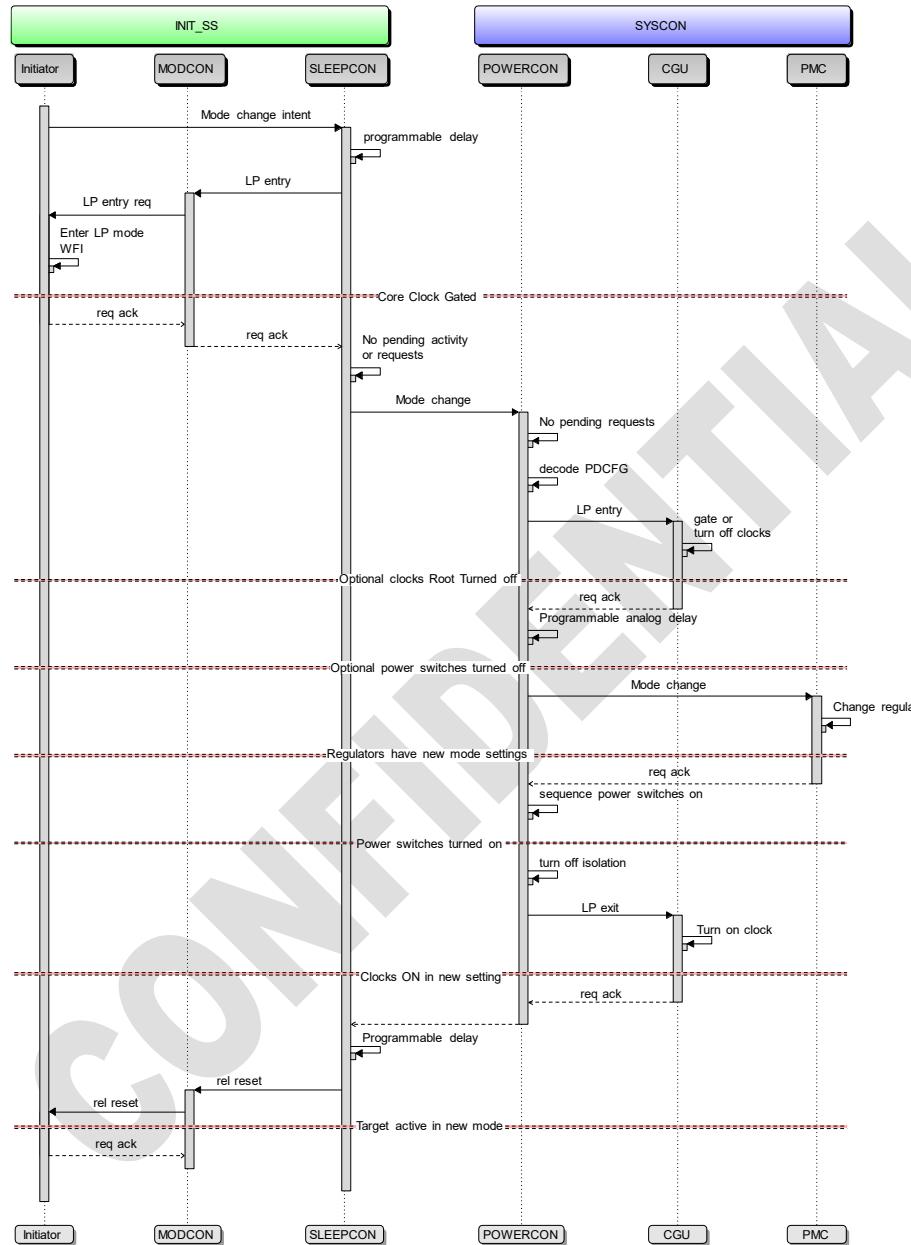


Fig 106. i.MX RT2660 LP active mode change sequence

Active mode changes involve bodybias condition changes, additional domains being turned on or off and potentially also supply voltage changes. To accommodate these, the SLEEPCON aggregates requests and depending on the power domain dependencies; the mode change is initiated by first placing the initiator in a LP mode. Next POWERCON is triggered to change the domains that are on or off and the clock settings. This sequence is similar to LP entry sequence. However at the end of

the PMC acknowledgement that the rails are at the new requested voltages, the POWERCON hand control back to SLEEPCON to further wake up the initiator in the new mode.

8.5 Sleep Controller

For more detailed description of the SLEEPCON and the related sequences, please refer to the RT2660 System Control HW.AS document [10]

SLEEPCON is used to configure the system level clock mode for each subsystem and to collate the various local wakeup sources in order to generate a wakeup signal for the power controller (POWERCON). Software configures which cores, DMA controllers and other masters need to remain active for the subsystem to be considered active. Once a subsystem is no longer active, SLEEPCON signals to MODCON to update the clock gating for the various system and functional clocks within the subsystem. Once this is completed, SLEEPCON interfaces to POWERCON to indicate the subsystem is no longer active and POWERCON can potentially initiate a change in power mode. SLEEPCON also generates a software configured wakeup signal to indicate if one of the modules in the local subsystem has generated a wakeup from low power modes. The separate active and wakeup signals enable different power configurations to be applied depending on the wakeup source.

Fig 107 shows the high-level overview of the sleep controllers on the i.MX RT2660.

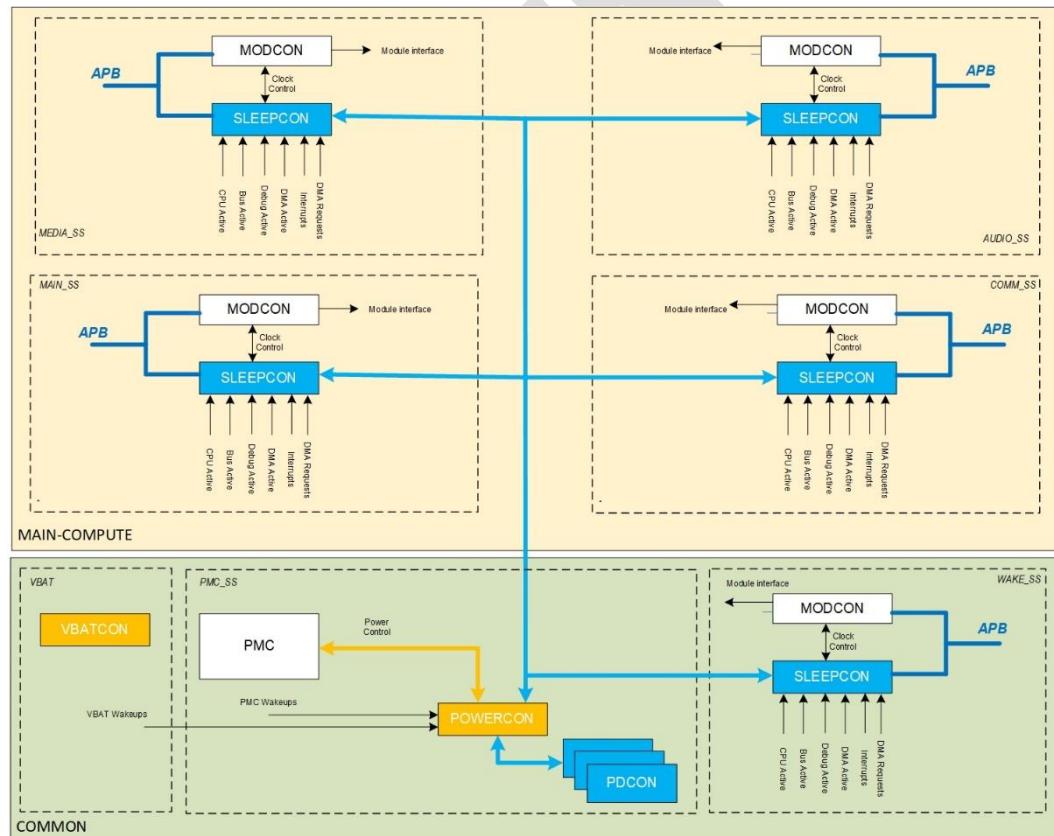


Fig 107. High-level overview of i.MX RT2660 sleep controllers

The sleep controller (SLEEPCON) is instantiated within each major subsystem and implements the following functions:

- Receive signals from the CPU, DMA, bus masters, bus fabric, debug logic and then based on software configuration registers, determine if the subsystem is active or not;
- When a subsystem is no longer active, handshake with the bus fabric and local bus initiators and then handshake with local MODCON clock sources to ensure clocks are gated in a safe manner, and then signal POWERCON that the subsystem is no longer active and the subsystem root clock can be gated ;
- When a subsystem becomes active, signal POWERCON and then handshake with the local MODCON clock sources to ensure clocks are enabled and handshakes with the bus fabric and local bus initiators. An attempted bus access to an inactive subsystem shall result in the bus access stalling until the clocks are enabled ;
- Collate interrupt wakeup signals from the various interrupt sources within the subsystem and based on software configuration registers, generate an interrupt wakeup signal to POWERCON ;
- Collate DMA wakeup signals from the various DMA sources within the subsystem and based on software configuration registers, generate a DMA wakeup signal to POWERCON.

8.6 Power Controller

*For more detailed description of the POWERCON and the related sequences,
please refer to the RT2660 System Control HW.AS document [10]*

The intention is that POWERCON is a parameterizable module that can be implemented as a reusable component on all future XEA1 platform devices. It partitions the SOC level power control (eg: POWERCON) from the MSIP owned blocks and their digital wrappers. The interface between POWERCON and the PMC module is TBD but shall be standardized (eg: Arm P-channel or similar).

POWERCON registers are intended to control functions that update as a result of an operating mode change (eg: reset, active, standby, etc). Functions that are set once due to board level configurations shall be controlled by registers in the MSIP digital wrapper (eg: disable LDO because it is bypassed on the board). These functions shall be protected from accidental software updates and reset on cold reset (eg: voltage monitor assertion).

Support for AVS (adaptive voltage scaling) is not anticipated to be controlled by POWERCON since this is not tied to an operating mode transition.

POWERCON configures the various power options for the device based on the different operating modes. The power configuration for the device is set using different PDCFG registers, as follows:

- PDCFG_STANDBY – Sets the power configuration during standby, software configures this register based on the specific low power mode that is required
- PDCFG_RESET – Sets the power configuration during reset, software configurability is restricted to ensure a consistent power state during boot
- PDCFG_ACTIVE – Sets the power configuration during active modes, software dynamically updates this register depending on the desired active mode operationg conditions
- PDCFG_WAKEUP – Optional power configuration that can be used to set the power configuration on wakeup from standby mode

Each PDCFG register implements common bit fields in the same bit positions. If a given PDCFG register does not support configuring a certain function, then that field is implemented with a fixed read-only value.

The power configuration options that can be set by the various PDCFG registers include the following, although note that the specific options supported vary by device:

- External PMIC mode pin state
- Internal PMC modes of operation and output voltage levels (per regulator)
- Bandgap and internal reference mode of operation
- Voltage monitor(s) mode of operation
- Power switches (both subsystem and SRAM)
- I/O rail isolation and retention control
- Clock generation module enables
- Analog module enables

POWERCON receives standby request and wakeup request inputs from the various SLEEPCON instances on the device, and wakeup request inputs from the modules in the VBAT domain. The standby requests are used to configure entry into Standby mode, while the wakeup requests are used to configure exit from Standby mode.

Request registers are implemented for the Active and Wakeup power configurations, these configure which of the standby request and wakeup request inputs are used to select the Active and Wakeup power configurations. The POWERCON Active and Wakeup power configurations can be used in one of the following modes.

- Only Active power configuration is enabled and Wakeup power configuration is disabled. The Active request register configures which subsystems trigger entry into Standby mode and which wakeup sources trigger wakeup from Standby mode.
- Both Active and Wakeup power configurations are enabled. The Active request register configures which subsystems trigger entry into Standby mode and the Wakeup request register configures which wakeup sources trigger wakeup from Standby mode. After wakeup, software initiates the transition from the Wakeup power configuration to the Active power configuration. It is also possible to transition back to Standby mode from the Wakeup power configuration.

Fig 108 shows the high-level overview of the power controller on the i.MX RT2660.

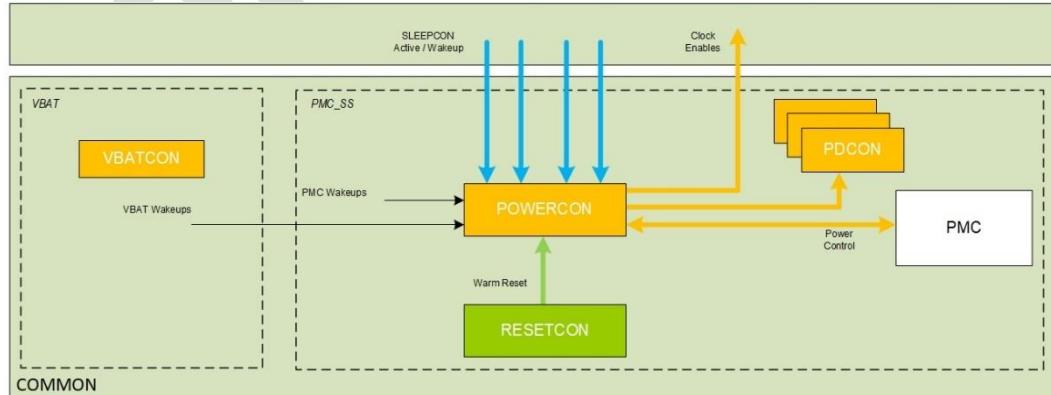


Fig 108. High-level overview of i.MX RT2660 power controller

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8.7 Power KPIs

Below an initial table that summarizes the initial power assessment during PDA phase.

Table 206. i.MX RT2660 Power KPI as power estimation during PDA phase

Metric	Mode	Condition	Unit	Requirements	Estimated
				(@1.8V)	Logic + PMU
Active (DCDC eff = 95%)	HP (700MHz)	Full Soc Max Activity (FF) ¹	mW	?	2500
		Full Soc Typ Activity ²	mW	?	950
	NP (500 MHz)	CPU Typ Activity ²	mW	200	192+5
		CPU Typ wih 256kB mem ²	mW	140	122+5
	LP (192MHz)	CPU + DMA + I2C + UART+ 256kB mem ²	mW	103	56+5
Standby (DCDC eff = 90%)	Sleep	SoC static All mem ^{2,7}	mW	32	25+0.9
	Deepsleep	SoC power off, All mem ^{3,7}	mW	1.8	1.5+0.1
	Powerdown	64kB mem ^{3,7}	µW	150	125+32
	Deep Powerdown	2kB mem ⁴	µW	15	15+9
Wake Latency	Sleep	WFI	Cycle	1	1
		w/ SLEEPCON handshake	µs	10	1.2
	Deepsleep	Typical ⁵	µs	150	TBC
	Powerdown	Typical ⁶	µs	650	TBC
	Deep Powerdown	Typical ⁶	µs	1000	Boot time

¹ FF, 0.88V 125C 5% activity

² TT, 0.8V 25C 3% activity

³ TT, 0.65V 25C 0% activity

⁴ TT, @3V 25C 0% activity, no DCDC

⁵ Assumes SXOSC, DCDC, FRO and PLL need to start back, USB Wakeup not supported

⁶ Assumes Full CGU, DCDC and SYSCON delay (500 1MHz cycles)

⁷ MIPI Phy leakage not accounted, Media, Audio and Comms subsystems are off.

9. Security & Safety Requirements

The i.MX RT2660 is a general purpose MCU developed to be compliant with NXP's EdgeLock® Assurance Program.

*For more detailed information on the RT2660 SoC security,
please refer to the i.MX RT2660 Security HW.AS document [11]
and the CSSI S110 HW.RS requirements [62]*

9.1 Overview of security functions

By controlling access to the device as well as providing trusted computing environment, this chip offers various security features and tools that allow customers to protect their assets. This section lists down the security functions that shall be guaranteed by the chip along with the components that support enabling these functions.

Secure isolation – This SoC shall include the following components to enable secure isolation functionality:

- ARM's TrustZone-M for armv8-M architecture included as part Cortex-M85 ;
- NXP's Trusted Resource Domain Controller (TRDC) is essential in enabling isolation between various processes running within the SoC. It is used to define and enforce separation between security critical and other processes by introducing the notion of domain IDs, as well as enforcing the trusted execution environment defined by ARM TrustZone-M ;

Refer to Section 9.3 "Secure isolation" for more details.

Cryptographic acceleration – This SoC shall include the following components for Cryptographic acceleration:

- CSSI_1_10 / Sentinel S110 secure enclave that includes cryptographic accelerators, hash/cypher algorithms and True Random Number Generator (TRNG).

Refer to Section 9.4 "Cryptographic acceleration" for more details.

Key store and management – This SoC shall include the following components for keys management:

- CSSI_1_10 (S110) is the primary block for keys management including Physically Unclonable Function to create device unique root of trust key ;
- OCOTP controller including key management functionality.

Security configuration storage – This SoC shall include the following components for secured storage of security configuration:

- OCOTP controller for secured storage of the security configuration ;
- XSPI with IPED functionality.

Anomaly or intrusion detection – This SoC shall include an Anomaly Detection and Response subsystem to enable this key security feature in the chip. This subsystem has the following anomaly event detectors and sensors:

- Battery Backed Security Module (BBSM) & Tamper Detect (TDET) ;
- Two Software Watchdog Timer (SWT) ;
- One External Watchdog Monitor (EWM) ;
- Voltage level and spike sensors per security sensitive voltage rail as part of PMC_SS
- Temperature detector as part of PMC_SS ;

- Clock frequency monitor for 32KHz RTC crystal oscillator as part of VBAT_SS.

Refer to Section 9.5 “Anomaly Detection and Response subsystem” for more details.

Immutable Root of Trust (RoT) – Immutable RoT in the chip is maintained by the truly immutable hardware logic (including analog and digital logic), read-only memory (ROM), one-time programmable memory (OTP) and the BootROM. The BootROM in the chip supports the following security features:

- Life cycle management ;
- Secure boot ;
- Secure update ;
- Secure debug ;
- Secure provisioning ;
- Secure device identification solutions ;
- Secure attestation.

Refer to Section 9.6 “Immutable Root of Trust (RoT)” for more details.

9.2 General security requirements

Table 207. IC requirements traceability: General security requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_SEC_1-3	Security Level	Heading	-
iMXRT2660_SEC_1-4	The Device shall meet EdgeLock 500B security level.	Must have	Yes, HW [11] [62]
iMXRT2660_SEC_1-6	The Device shall meet EdgeLock 600B security level.	Should have	Yes HW+SW [11] [62]
iMXRT2660_SEC_2-1	Security Certification & Compliance	Heading	-
iMXRT2660_SEC_2-2	A full vulnerability pre-analysis shall be completed on the proposed security architecture prior to silicon tapeout.	Must have	To be completed during design phase
iMXRT2660_SEC_2-4	SEIP2 Secure MCU/MPU Protection Profile with Software Attacker Resistance.	Must have	Yes HW+SW [11] [62]
iMXRT2660_SEC_2-5	SEIP3 Secure MCU/MPU Protection Profile with Physical Attacker Resistance	Should have	Yes HW+SW [11] [62]
iMXRT2660_SEC_2-6	ARM PSA L2	Must have	Yes Yes HW+SW [11] [62]
iMXRT2660_SEC_2-7	ARM PSA L3	Should have	Yes HW+SW [11] [62]
iMXRT2660_SEC_2-8	NIST CAVP; no CMVP or FIPS-140(-ready) compliance required	Must have	To be completed during qualification
iMXRT2660_SEC_2-9	The development of the device shall follow NXP's ISO/SAE 21434 compliant processes	Must have	Yes HW+SW [11] [62]
iMXRT2660_SEC_2-10	IEC62443 SL2 ready – The Device must support customer product to pass IEC62443 SL2 certification without external security component, and provide mapping migration guide.	Must have	Yes HW+SW [11] [62]

9.3 Secure isolation

For security and reliability of the system (customer end product), software or firmware running on the chip is partitioned into multiple components based on functionality and are isolated from each other. Secure isolation is a key security feature that enables:

- Enhanced protection from hackers as the partitioning mechanism limits the reachability for the hackers ;
- Partition reboot to recover rather than a full system reboot, which could interrupt vital operations ;
- Support for partial updates of one or a few partitions ;
- Higher reliability and safety ;
- Isolation of low-quality or unknown quality software ;
- Better plug-in modularity ;
- Easier incorporation of legacy software using isolated partitions.

The i.Mx RT2660 contains multiple processing domains with bus architecture partitioned according to XEA-1 architecture. The processing engines (CPU, CSSI, GPU) reside in domains with process isolation while interconnected through bus fabrics to connect to on-chip memories and peripherals that need further cross-domain protections. This SoC makes use of following components and design architecture to provide secure isolation:

- Functional domains with bus matrices whose security attributes are configured using separate instances of Trusted Domain Resource Controller (TRDC) ;
- Compute Subsystem contains CPU & NPU, interconnected to a Network Interconnect (NIC) bus fabric to on-chip shared SRAM ;
 - Neutron-256S NPU with dedicated control processing engine (ZEN-V core) and tightly-coupled memories ;
- Main Subsystem contains CSSI secure enclave and peripheral subsystem ;
 - CSSI Secure enclave with dedicated processing engine (ZEN-V core) and cryptographic accelerators providing fully isolated security functions.
- Media Subsystem contains display and high-speed peripherals with GPU engine ;
- Further isolation within processing engine is provided by ARM's TrustZone for armv8-M architecture. For this the SoC instantiates the ARM Cortex-M85 with:
 - Non-Secure Memory Protection Unit configured with 16 software programmable memory protection regions ;
 - Secure Memory Protection Unit configured with 16 software programmable memory protection regions ;
 - Security Attribution Unit configured with 8 software configurable attribution regions ;
 - Refer to ARM documentation for details on TrustZone for armv8-M architecture.
- Domain Assignment Controllers provide register to define which domains can access shared SRAM and peripherals present. The i.MX RT2660 makes use of an Implementation Defined Attribution Unit (IDAU) with, address bit 28 is used to identify secure (address bit 28 = 1) or non-secure (address bit 28 = 0).

9.4 Cryptographic acceleration

9.4.1CSSI_1_10 / Sentinel S110 secure enclave

The CSSI_1_10 (S110) is a security subsystem that supports a wide range of cryptographic algorithms and provides strong key isolation from the rest of chip. CSSI_1_10 is the main building block of the chip immutable Root of Trust. It is used as part of the trust anchor during secure boot, secure debug access, lifecycle management, and trust provisioning.

Fig 109 shows a high-level functional block diagram of CSSI_1_10.

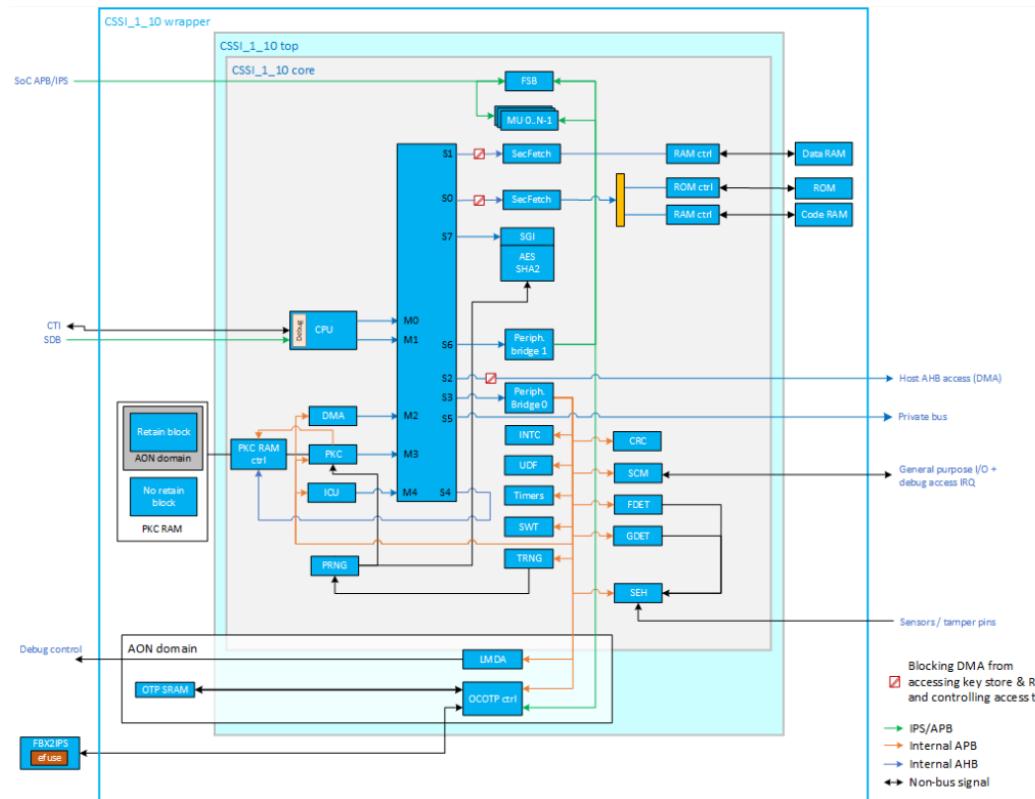


Fig 109. Functional block diagram of the CSSI_1_10 (S110) Security Enclave

The CSSI_1_10 is configured to offer the following key features:

- to provide the resistance against side-channel attacks ;
- to provide cryptographic algorithms ;
- to provide secure isolation ;
- to provide minimum security strength of 192-bits when generating random numbers:
 - DRBG compliant to NIST specification ;
 - TRNG compliant to NIST specification ;
- to enable attestation of software and hardware state using Runtime Finger Print (RTF) ;
- to provide Key Management services.

For a detailed overview of the CSSI_1_10 and supported features, please refer to the [62].

Table 208. IC requirements traceability: Cryptographic accelerator requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_SEC_3-1	Symmetric Key Encryption	Heading	-
iMXRT2660_SEC_3-2	The security subsystem shall implement Advanced Encryption Standard (AES) <ul style="list-style-type: none"> 1) AES-128 – TBD clock cycles per 64-bits 2) AES-192 – TBD clock cycles per 64-bits 3) AES-256 – TBD clock cycles per 64-bits 	Must have	Yes, [62]
iMXRT2660_SEC_3-3	The security subsystem shall implement the following confidentiality modes <ul style="list-style-type: none"> 1) Electronic Codebook (ECB) 	Must have	Yes, [11] [62]

AS/RS identifier	Contents	Classification	Covered
	<ul style="list-style-type: none"> 2) Cipher Block Chaining (CBC) 3) Cipher Feedback (CFB) 4) Output Feedback (OFB) 5) Counter (CTR) 		
iMXRT2660_SEC_3-5	The security subsystem shall implement the following confidentiality modes <ul style="list-style-type: none"> 1) Cipher Block Chaining Message Authentication Code (CBC-MAC) 	Must have	Yes, [11] [62]
iMXRT2660_SEC_3-7	The security subsystem shall implement the following confidentiality modes <ul style="list-style-type: none"> 1) Counter with CBC-MAC (CCM) 	Must have	Yes, [11] [62]
iMXRT2660_SEC_3-9	The security subsystem shall support Authenticated encryption with Associated Data (AEAD) mode using Galois Counter Mode (GCM)	Must have	Yes, [11] [62]
iMXRT2660_SEC_3-10	The Device shall implement hardware acceleration for authenticated encryption with ChaCha20-Poly1305	Should have	Yes, HW+SW [62]
iMXRT2660_SEC_3-12	The Device shall implement hardware acceleration for AES-CMAC.	Should have	Yes, HW+SW [62]
iMXRT2660_SEC_3-14	Performance of all Symmetric Key Encryption algorithms shall be better than RT1060 and RT1180 at customer API level on throughput.	Should have	Performance to be assessed during design phase
iMXRT2660_SEC_4-1	Asymmetric Key Encryption	Heading	-
iMXRT2660_SEC_4-2	The security subsystem shall implement Rivest-Shamir-Adleman (RSA) based on the ANSI X9.31 / IEEE 1363 standard <ul style="list-style-type: none"> 1) RSA-1024 2) RSA-2048 3) RSA-3072 4) RSA-4096 	Must have	Yes, HW+SW [62]
iMXRT2660_SEC_4-3	The security subsystem shall implement Elliptic Curve Cryptography (ECC) based on the NIST publication "Recommended Elliptic Curves for Federal Government Use": <ul style="list-style-type: none"> 1) NIST P-192 2) NIST P-224 3) NIST P-256 4) NIST P-384 5) NIST P-521 	Must have	Yes, HW+SW [62]
iMXRT2660_SEC_4-4	The security subsystem shall implement Elliptic Curve Cryptography (ECC) to meet HomeKit requirements: <ul style="list-style-type: none"> 1) Curve 25519 2) Curve ed25519 	Must have	Yes, HW+SW [62]
iMXRT2660_SEC_4-5	The security subsystem shall implement Elliptic Curve Cryptography (ECC) specified as per RFC-5639: <ul style="list-style-type: none"> 1) brainpoolP192r1 2) brainpoolP224r1 3) brainpoolP256r1 4) brainpoolP384r1 5) brainpoolP512r1 	Must have	Yes, HW+SW [62]
iMXRT2660_SEC_4-6	Performance of all Asymmetric Key Encryption algorithms shall be better than RT1060 and RT1180 at customer API level on throughput.	Must have	Performance to be assessed during design phase
iMXRT2660_SEC_5-1	Hash Algorithms	Heading	-
iMXRT2660_SEC_5-2	The security subsystem shall implement Secure Hash Algorithm 1 (SHA-1) as per NIST FIPS 180-1.	Must have	Yes, SW only [62]
iMXRT2660_SEC_5-3	The security subsystem shall implement Secure Hash Algorithm (SHA-2) as per NIST FIPS 180-4: <ul style="list-style-type: none"> 1) SHA-224 2) SHA-256 	Must have	Yes, HW [62]

AS/RS identifier	Contents	Classification	Covered
	3) SHA-384 4) SHA-512		
iMXRT2660_SEC_5-4	All crypto operations shall support multiple context	Must have	Yes HW+SW [11] [62]
iMXRT2660_SEC_5-5	This Device shall implement HMAC as per FIPS 198-1.	Must have	Yes HW+SW [11] [62]
iMXRT2660_SEC_5-6	Performance of all Hash Algorithms shall be better than RT1060 and RT1180 at customer API level on throughput.	Must have	Performance to be assessed during design phase
iMXRT2660_SEC_6-1	Signature Authentication	Heading	-
iMXRT2660_SEC_6-2	The Device shall support following signature authentication algorithms:	Must have	Information item
iMXRT2660_SEC_6-3	1) ECDSA on P-256/P-384	Must have	Yes HW+SW [11] [62]
iMXRT2660_SEC_6-4	2) AES-CMAC-256	Should have	Yes HW+SW [11] [62]
iMXRT2660_SEC_6-5	3) PQC with Dilithium/LMS	Must have	Yes HW+SW [11] [62]
iMXRT2660_SEC_6-6	The Device shall provide a mechanism, for example OTP setting, for customer to select a signature authentication scheme for each security function, including secure boot, secure firmware update, and secure debug.	Must have	Yes HW+SW [11] [62]
iMXRT2660_SEC_6-7	Performance of all Signature Authentication Algorithms shall be better than RT1060 and RT1180 at customer API level on throughput.	Must have	Performance to be assessed during design phase
iMXRT2660_SEC_8-1	Random Number Generator	Heading	-
iMXRT2660_SEC_8-2	This Device shall implement SP800-90A compliant random number generator seeded with SP800-90B compliant entropy source.	Must have	Yes HW+SW [11] [62]
iMXRT2660_SEC_8-3	The RNG shall follow the recommendation in: 1) NIST FIPS-186 2) NIST 800-90 A/B/C	Must have	Yes HW+SW [11] [62]
iMXRT2660_SEC_8-4	The RNG must pass the test based on: 1) NIST SP 800-22	Must have	Yes HW+SW [11] [62]
iMXRT2660_SEC_8-5	This Device shall support 256-bit PRNG/DRBG.	Must have	Yes HW+SW [11] [62]
iMXRT2660_SEC_13-1	Secure communication	Heading	-
iMXRT2660_SEC_13-2	The device shall support secure communication using one of the supported cipher suites for confidentiality protection over wireless connectivity (Wi-Fi) and wired connectivity (Ethernet or USB).	Must have	Yes, HW+SW [62]
iMXRT2660_SEC_13-4	1) AES_256_GCM_SHA384	Must have	Yes, HW+SW [62]
iMXRT2660_SEC_13-5	2) AES_128_GCM_SHA256	Must have	Yes, HW+SW [62]
iMXRT2660_SEC_13-6	3) AES_128_CCM_8_SHA256	Must have	Yes, HW+SW [62]
iMXRT2660_SEC_13-7	4) AES_128_CCM_SHA256	Must have	Yes, HW+SW [62]
iMXRT2660_SEC_13-8	The security unit shall support encryption of video stream data up to 1MP resolution, 30fps, 16bpp using one of the supported cipher suites in the TLS1.3 protocol.	Must have	To be confirmed during design phase

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_SEC_14-1	Secure Storage	Heading	-
iMXRT2660_SEC_14-2	The security subsystem shall store locally minimum 3 key pairs of type ECC P-256, ECC P-384, ECC P-521, RSA 4096.	Must have	Targeted
iMXRT2660_SEC_14-3	The security subsystem shall store locally minimum 10 AES keys.	Must have	Targeted
iMXRT2660_SEC_14-4	The security subsystem shall support wrapping of key material to mass storage outside the security subsystem. This requirement is for inline encryption/decryption and authentication through XSPI interfaces.	Must have	Yes HW+SW [11] [62]
iMXRT2660_SEC_14-6	Flash Config Block (FCB) authentication The security subsystem shall authenticate the FCB file before allowing the system ROM to program it into the external flash device.	Must have	No, not needed as part security approach

9.5 Anomaly Detection and Response subsystem

9.5.1 Tamper Detect

The i.Mx RT2660 includes a Battery Backed Security Module (BBSM) and a Tamper Detect (TDET) module in the VBAT Subsystem. These modules provide a mechanism to configure the response action for an intrusion event detected by on-chip security sensors. Intrusion response is the action a chip performs in order to prevent misuse of the device or disclosure of critical assets (cryptographic keys, personal data) that are generated or stored within the device. The sensor response shall feed to the CSSI event inputs; the sensor response is configurable in the ITRC, handled by ROM during boot.

Refer to Section 6.9.4 for more information on the supported security function in the VBAT_SS.

Table 209. IC requirements traceability: Physical protection requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_SEC_7-1	Physical Protection	Heading	-
iMXRT2660_SEC_7-2	This Device shall support protection against side channel analysis (SCA) attacks for power analysis.	Must have	Yes, as per scope defined in [62]
iMXRT2660_SEC_7-3	This Device shall support protection against side channel attacks for timing analysis.	Must have	Yes, as per scope defined in [62]
iMXRT2660_SEC_7-4	This Device shall support protection against side channel attacks for electromagnetic analysis.	Must have	Yes, as per scope defined in [62]
iMXRT2660_SEC_7-5	This Device shall support protect voltage glitch/low-cost fault injection attacks.	Must have	Yes, as per scope defined in [11] [62]
iMXRT2660_SEC_7-6	This Device shall support protection against clock manipulation attacks.	Must have	Yes, as per scope defined in [11] [62]
iMXRT2660_SEC_7-7	This Device shall support protection against temperature manipulation attacks.	Must have	Yes, as per scope defined in [11]
iMXRT2660_SEC_7-8	This Device shall support protection against Electro magnetic fault inject (EMFI) attacks.	Should have	Open, to be closed during design phase
iMXRT2660_SEC_20-1	Battery-Backup (VBAT) Domain	Heading	-
iMXRT2660_SEC_20-10	General purpose register and SRAM storage in the VBAT domain shall be erased upon detection of a security violation.	Must have	Yes, see [11] [62]

9.5.2 Software Watchdog Timer

The i.MX RT2660 contains three Software Watchdog Timer (SWT) modules. For more details on the SWT module, please refer to Section 6.7.7.

Table 210. IC requirements traceability: Security Software Watchdog Timer requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_SEC_16-2	This Device shall implement watchdog timer(s) that can prevent system lockup in situations such software getting trapped in a loop or if a bus transaction fails to terminate.	Must have	Yes, 2x SWT
iMXRT2660_SEC_16-3	The watchdog timer can be configured to generate a reset or interrupt on an initial time-out. A reset is always generated on a second consecutive time-out.	Must have	Yes, targeted
iMXRT2660_SEC_16-4	A watchdog timer module can be dedicated to secure software when secure TrustZone is enabled.	Must have	Yes, targeted

9.5.3 External Watchdog Monitor

The i.MX RT2660 shall contain one External Watchdog Monitor (EWM) module. For more details on the EWM module, please refer to Section 6.7.8.

9.5.4 PMC_SS voltage sensors

The i.MX RT2660 shall contain voltage sensors to detect voltage excursions and voltage spikes on all power supply voltage rails that are accessible externally. For more details on the voltage sensors, please refer to Section 6.8.1.4.

9.5.5 PMC_SS temperature sensor

The i.MX RT2660 shall contain a temperature detector to detect a low-temperature and high-temperature excursion of the SoC die temperature. For more details on the temperature detector, please refer to Section 6.8.1.4.

9.5.6 VBAT_SS clock frequency monitor

The i.MX RT2660 VBAT_SS shall contain a clock monitoring function on the 32 kHz clock.

It concerns monitoring of the 32 kHz crystal oscillator for detecting possible tampering evening and/or whether this clock is running stable. Such tampering event could occur via the external crystal related pins. In case of anomalies, it shall be ensured that the FRO32K takes over the 32 kHz output, and flagging of the anomaly shall be done to the security subsystem who can then take care of an appropriate response. This clock monitoring function should be implemented as part of the BBSM.

The FRO32K is not monitored explicitly, however monitored through indirect measurement such as voltage sensors or temperature detectors.

For more details on the clock monitoring, please refer to the Security HW.AS [11]

9.6 Immutable Root of Trust (RoT)

9.6.1 Life cycle management

During its lifespan, a typical chip finds itself in various places around the world. It is manufactured in a semiconductor factory, tested and packaged in silicon manufacturer facilities, sold to various distributors, sold further to the Original Equipment Manufacturer (OEM), assembled, tested and provisioned by their Contract Manufacturers and, finally, delivered to the end-customer. In the case of failure, the device is returned to OEM or even back to the silicon manufacturer for further failure analysis.

Chip lifecycle state is used to reflect the actual state of the device, which is further used to instruct the chip on how exactly to protect the assets a device hosts during specific time. For example, when a chip is being tested at a silicon manufacturer facility and no OEM or end-customer assets have been provisioned on it, then access to the chip, in terms of debug or test, is less restrictive than when it is with the end-customer.

Lifecycle state is monotonic, meaning it can only always be increased. Immutable RoT is in charge of lifecycle management and it enforces device access policies accordingly.

Please refer to Section 9.8 for a description on i.MXRT2660's supported life cycle management.

9.6.2 Secure boot

Secure Boot ensures authenticity, integrity and confidentiality of the chip bootloader, firmware, and other software during the boot process and ensures that the intended secure life-cycle state is reached.

After powering on or waking up of the device from one of the low-power modes, the first thing it does is it verifies authenticity or integrity of the code it is going to execute next. Functional integrity of Boot ROM is ensured by design. The BootROM in combination with HW accelerators verifies authenticity or integrity of the ROM patch and the FW image. Before handing the control over to FW, the BootROM makes sure the ROM patch, TRDC, and OTP are all secured.

Refer to Section 10.2 for more information on the Boot ROM.

9.6.3 Secure update

Secure Update is the process used to securely update the firmware image in the field. Secure update ensures authenticity and confidentiality of the firmware image, using ECDSA signature verification and AES encryption and SHA hashing mechanisms. An update stays due when the running FW gets compromised or a new feature is added to the firmware. Secure update guarantees authenticity and confidentiality of the new image. It also ensures that the new image is up-to-date, preventing the rollback to an older image. Running firmware is in charge of receiving and verifying the new firmware image. The follow-up Secure Boot verifies the new firmware image again, making sure the Immutable RoT is still in charge of ensuring authenticity of the latest firmware.

9.6.4 Secure debug

Secure Debug is the process used to securely access debug, following the policy defined by the lifecycle management. When a debugger wants to debug a device, it indicates that through a debug mailbox. The chip checks the debug mailbox and starts a debug authentication mechanism. Debug is allowed only after successful authentication.

Debug mailbox is a module integrated in this chip that offers a register-based mailbox or interaction mechanism for external debuggers. For more information, refer to i.MX RT2660 SW.AS document.

Table 211. IC requirements traceability: Secure debug requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_SEC_18-2	This Device shall support JTAG based Signed Command or Firmware Signed Command using NXP SRK root for Sentinel security subsystem debug.	Must have	Yes, JTAG. Rest see SW.AS.
iMXRT2660_SEC_18-3	This Device shall support JTAG Password Challenge Response, JTAG based or Firmware Signed Command using OEM SRK root, for the rest of SoC debug.	Must have	Yes, JTAG. Rest see SW.AS.
iMXRT2660_SEC_18-4	This Device shall support debug authentication using crypto algorithm defined in CNSA1.0 and CNSA2.0 using an appropriate supported crypto algorithm.	Must have	To be confirmed

AS/RS identifier	Contents	Classification	Covered
			to security DRI

9.6.5 Secure provisioning

Secure provisioning is a process to provide a cryptographic proof of the device's origin and to offer a set of tools to OEM for secure provisioning of their own assets. The BootROM and the firmware from NXP supports the following to ensure secure provisioning of the device:

- ~~HSM provisioning flow~~ ;
- Java card-based OEM Trust Provisioning ;
- Compatibility with EdgeLock® 2Go provisioning service.

Please refer to Section 9.8 for a further description on i.Mx RT2660's provisioning.

Table 212. IC requirements traceability: Trust provisioning requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_SEC_19-2	This processor shall support secure provisioning of OEM assets using Device HSM flow.	Must have	Yes, HW supports [11]
iMXRT2660_SEC_19-3	The VBAT domain shall include 2KB SRAM for sensitive information storage.	Must have	Yes, HW supports [11]
iMXRT2660_SEC_19-4	This processor shall support secure provisioning of OEM assets using EdgeLock2Go (Cloud HSM) flow.	Must have	Yes, HW supports [11]
iMXRT2660_SEC_19-5	This processor shall support harvesting of device identity in NXP factory	Must have	Yes, HW supports [11]
iMXRT2660_SEC_19-6	This processor shall support provisioning of genuine "NXP device certificate" in NXP factory	Must have	Yes, HW supports [11]
iMXRT2660_SEC_19-7	This processor shall support mRoT key hierarchy defined CCC&S specification for NXP factory provisioning use cases	Must have	Yes, HW supports [11]

9.6.6 Secure device identification solutions

Secure identification of the device is applied by cryptographically binding the following:

- Universally Unique Identifier (UUID) – A unique number linked to the device ;
- Device Unique Key (DUK) ;
- Root-of-Trust material – Information stored in immutable memory (OTP, or BootROM)
- Device state – A function of device Lifecycle state, boot state and run-time state.

Secure device identity of the device is configured to evolve together with the life of the device. Initially, the device identity is created during the trust provisioning process at the NXP facility. The UUID number, the NXP configuration data, its secrets and the device unique keys are provisioned. This, together with the current state of the device, determines its identity. The device is then shipped to OEM where the trust provisioning process continues. OEM configuration data, key material and the initial firmware are provisioned, which determines the new device identity. This new identity is then used by the OEM to enable services for that particular device.

Table 213. IC requirements traceability: Secure device identification solution requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_SEC_9-1	OTP/Unique ID	Heading	-

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_SEC_9-2	This Device shall support a mechanism for creating a 128-bit device unique ID (RFC4122).	Must have	Yes, mechanism as per [11]
iMXRT2660_SEC_9-3	The Device unique ID shall be securely stored in OTP.	Must have	<i>Targeted, to confirm during design phase</i>
iMXRT2660_SEC_9-4	The Unique ID can be used by OEM application in a secure way.	Must have	Yes, via S110 [11]
iMXRT2660_SEC_9-5	The OTP implementation shall include ECC or redundancy.	Must have	Yes, see OTP + Ctrl
iMXRT2660_SEC_9-6	This Device shall support testing of all security features during development life cycle without programming fuses. This can be achieved by using shadow register or RAM.	Must have	Yes, see [11]
iMXRT2660_SEC_9-7	This device shall provide the ability for OEM to select a regional configuration by fuse burning in their manufacturing, each configuration selecting a set of crypto options.	Must have	Unclear requirement
iMXRT2660_SEC_9-8	This Device shall support secure way to patch the ROM code to fix critical bugs with in-field patchability	Must have	Yes, via S110 [11]
iMXRT2660_SEC_9-9	OTP Patch storage shall be integrity protected.	Must have	Yes, see OTP + Ctrl
iMXRT2660_SEC_9-10	OTP Patch storage shall be protected from rollback attacks.	Must have	Yes, via Fusemap + S110/SW [62]
iMXRT2660_SEC_9-11	The device shall support proof of genuineness (a.k.a. Entity attestation token with NXP credentials, SKU and security feature versioning information)	Must have	Yes HW+SW [62]
iMXRT2660_SEC_10-1	Key management	Heading	-
iMXRT2660_SEC_10-2	The security subsystem shall support implicit key management logic (usage, LC state, temporal boot state, transaction level -hprot/pprot, debug state).	Must have	Yes HW+SW [62]
iMXRT2660_SEC_10-3	The security subsystem shall support key derivation functions (KDF) per SP 800-56C specification: - One step KDF using SHA256-HMAC - Two step KDF using AES-CMAC	Must have	Yes HW+SW [62]
iMXRT2660_SEC_10-4	The security subsystem shall support KDF per SP 800-108 specification.	Must have	Yes HW+SW [62]
iMXRT2660_SEC_10-5	The security subsystem shall support key wrapping/unwrapping per SP 800-38F specification for loading & unloading keys to security subsystem.	Must have	Yes HW+SW [62]
iMXRT2660_SEC_10-6	The security subsystem shall support DICE-CDI based key hierarchy.	Must have	To be confirmed to security DRI
iMXRT2660_SEC_10-7	The security subsystem shall support hardware state aware key derivation functions.	Must have	Yes HW+SW [62]
iMXRT2660_SEC_10-8	The security subsystem shall support Device Unique root key (DUK).	Must have	Yes HW+SW [62]
iMXRT2660_SEC_10-9	The security subsystem shall support re-keying of Device Unique root key (DUK) in return life-cycle states. To allow full functional testing without compromising customer and NXP assets.	Must have	Yes HW+SW [62]
iMXRT2660_SEC_10-10	The Device shall implement Root of Trust.	Must have	Yes HW+SW [11] [62]
iMXRT2660_SEC_10-11	The Device shall support Life Cycle Management Enforcement.	Must have	Yes HW+SW [11] [62]

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_SEC_10-12	The security subsystem shall implement a secured mechanism to provide keys to crypto blocks in the xSPI memory controller.	Must have	Yes, via S110 private bus [11] [62]
iMXRT2660_SEC_10-13	This MCU product shall have the ability to support on-die encryption as well as offline encryption. Offline encryption means customer will encrypt the code (or data) with an external tool then program the encrypted code (or data) onto NVM device.	Must have	To be confirmed to security DRI

9.6.7 Secure attestation

Secure Attestation is a set of mechanisms used to provide evidence to a remote party on the device's genuine identity, its software and firmware versions, as well as its integrity and lifecycle state. Device Identity Composition Engine (DICE), as defined by Trusted Computing Group, uses Immutable RoT during boot time to create a unique Device Identity which takes into account Unique Device Secret (UDS), hardware state of the device and its firmware. The DICE feature is implemented using the ELS Runtime Fingerprint (RTF) in this device. RTF is the NXP-proprietary attestation mechanism, which measures the device's state during boot-time and run-time as well.

9.7 Trusted Resource Domain Controller

9.7.1 Overview

The Trusted Resource Domain Controller (TRDC) provides an integrated and scalable architectural framework for access control, system memory protection, and peripheral isolation. It allows software to assign chip resources including processor cores, non-core bus masters, memory regions, and slave peripherals to processing domains to support enforcement of robust operational environments.

- First, each bus mastering resource is assigned to a domain identifier (domainID, DID). Typically, each processor is assigned to a unique domainID and all remaining nonprocessor bus masters assigned to a different domainID ;
- Next, the access control policies for the individual domains are programmed into any number of registers implemented in the slave memory block and region checkers ;
- Finally, all accesses throughout the device are monitored concurrently to determine the validity of each access. If a reference from a given domain has sufficient access rights, it is allowed to continue, else the access is aborted and error information captured.

The access control scheme that TRDC defines supports a 4-level model, combining the traditional privileged (also known as supervisor) and user modes with an additional signal defining the secure, nonsecure attributes of each memory reference. The result is a 4-level hierarchical access control mechanism with different access control policies based on read, write, and execute references, where:

SecurePriv > SecureUser > NonsecurePriv > NonsecureUser

Combined with the secure/nonsecure and privileged/user attributes, a domainID is associated with every system bus transaction and forms the hardware basis for the implementation of TRDC's access control mechanisms.

For more detailed description, please refer to the RT2660 TRDC HW.AS document [63]

9.7.1.1 Submodules

The TRDC implementation is distributed across multiple submodules instantiated throughout the device. The TRDC submodules include:

- **TRDC_MGR:** The Manager (MGR) submodule coordinates all programming model reads and writes ;
- **TRDC_DAC:** The Domain Assignment Controller (DAC) submodule handles resource assignments and generation of the domain identifiers ;
- **TRDC_MBC:** The Memory Block Checker (MBC) submodule implements access controls for on-chip internal memories and slave peripherals based on a fixed-sized block format ;
- **TRDC_MRC:** The Memory Region Checker (MRC) submodule implements the access controls for external off-chip memories and peripherals based on the pre-programmed region descriptor registers.

9.7.1.2 Features

- Ability to assign chip resources to processing "domains":
 - Processor cores, non-core bus masters, slave memories, and slave peripherals ;
 - Each processing domain is assigned a unique domain identifier (domainID, DID);
 - DomainID is an attribute associated with every system bus transaction ;
 - Used in conjunction with secure/nonsecure, privileged/user attributes ;
- Defines access rights to slave targets in MBCs for on-chip memories and peripherals and in MRCs for external memories and peripherals ;
- Built upon a 4-level hierarchical access control model:
 - SecurePriv > SecureUser > NonsecurePriv > NonsecureUser ;
 - Defined by multiple sets of user-programmable R/W/X (Read, Write, Execute) flags per access state ;
- Distributes programming model and hardware implementation across multiple submodules:
 - Supports a broad, highly-configurable architecture definition ;
 - Supports efficient mechanisms for memory space context switch state changes using nonsecure enables (NSE) for memory blocks and regions.

9.7.2 TRDC requirements

The TRDC is used during the boot process to enforce the following requirements:

- All bus accesses are blocked from bus initiators that are not involved in the boot process ;
- Access permissions to memory regions used for authenticating code are controlled by CSSI during boot mode only:
 - SRAM memory regions are read-write before code authentication ;
 - External (e.g. NVM) memory regions are read-only before code authentication ;
 - Memory code regions are read-only during authentication ;
 - Memory code regions that have passed code authentication are read-execute ;
 - Peripheral regions are read-write; the TRDC registers are only accessible to TRDC software manager (initially CSSI but then handed over to application core)

- Access permissions for a TCM backdoor port have no impact on the CPU accessing its own TCM; access permissions from a CPU to its own TCM are generally limited by the MPU configuration which is generally only accessible to that CPU ;
- Subsystems that remain powered in low power modes are not reset on wakeup even if the main subsystem is going through a boot sequence:
 - Local TRDC registers are retained in this mode and control access permissions for accesses that are local to the subsystem ;
 - Accesses that are contained within these subsystems before and during the main boot process are allowed and controlled by local TRDC instances ;
 - Accesses to outside these subsystems during the main boot process shall be blocked ;
- Subsystems that can be powered on without the main subsystem do not involve a normal boot sequence:
 - Local TRDC registers are reset in this mode and return to default configuration ;
 - Accesses into these subsystems shall be limited to the default Domain ID used by the TRDC software manager ;
 - Accesses to outside these subsystems shall be blocked until the TRDC software manager can configure the TRDC registers ;
- When SoC DFT access is enabled (by CSSI), TESTPORT has full access to all memory regions, including TRDC registers ;
- The boot core can optionally load a preset TRDC configuration at the end of boot that is stored with the customer image
 - If this is not configured then a default TRDC configuration shall be used that is permissive in order to simplify customer application development, including full debug access ;
- NXP assets that are accessible from the system bus during boot, shall be locked during the boot process to block any access until the next reset (e.g. temporal isolation)
 - NXP assets in other subsystems shall be protected by a TRDC instance in the MAIN_SS to avoid bypassing the protection through power gating ;
 - NXP assets that need to be accessible to CSSI during active mode (e.g.: outside of the boot process) could be supported using a private NXP Domain ID that can only be selected by CSSI (or similar device under the control of NXP firmware) ;
- TRDC register accesses shall be minimized during boot mode to reduce ROM complexity and improve boot time
 - Controlling access using different Domain IDs is quicker than updating every single block and region checker ;
 - Using region checkers to update access permissions for code regions is quicker than using block checkers.

During active mode, the TRDC software manager is owned by OEM software. The TRDC is primarily responsible to isolate computing cores from each other and from other non-core bus masters.

9.7.3 Deny by default

The TRDC deny by default logic is used to enable TRDC by default and restrict bus accesses to a list of parameterized Domain IDs only. The deny by default logic is disabled once TRDC registers have been fully configured.

The XEA-1 platform will not implement deny by default due to the following limitations:

- Deny by default is controlled by a single wire that is sampled once at end of reset and is potentially glitchable by an attacker ;
- Deny by default is not flexible enough to meet all boot requirements and requires all TRDC registers to be updated during boot, increasing boot time ;

The alternative solution for XEA-1 platform is to define an “access denied” domain ID that is the default domain ID for all non-boot bus initiators and to implement intelligent reset values for all TRDC registers.

[Change Request]: XEA1 platform requires a change request on TRDC to support parameterizable master reset values.

9.7.4TZ-M implementation

The i.MX RT2660 makes use of TrustZone-M on the ARM Cortex-M85 core, as indicated in Section 6.2.1. The TRDC ensures that core(s) and non-core bus initiators can operate together in a scalable architectural framework for access control, system memory protection, and peripheral isolation.

The i.MX9 family of devices requested a change request on TRDC that allows secure masters to access non-secure regions of memory. This change was requested to be compatible with the Cortex-A version of TrustZone.

For a TZ-M implementation, this means that TRDC will allow secure bus masters to execute from non-secure regions of memory. This shall be fixed so that secure bus masters can only read or write to non-secure regions of memory but instruction fetches are blocked.

Note that TRDC block and region checkers do not verify that a secure alias is only accessed via a secure access and a non-secure alias is only accessed via non-secure access. The TRDC block and region checkers do mask out the address bit used for secure/non-secure accesses (parameterized per instance).

The DAC instances for non-core masters can instantiate a local IDAU that asserts a violation output if the alias address does not match that access type. The use of this feature is TBD. More details on the IDAU implementation can be found in [63].

Table 214. IC requirements traceability: Trustzone and access protection requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_SEC_15-2	This Device shall enable TrustZone-M on Cortex-M core(s) to provide two domains of separation: Secure and Non-Secure.	Must have	Yes, see Section 6.2.1
iMXRT2660_SEC_15-3	This Device shall provide implementation for how the core(s) and non-core bus initiators can work together without creating exposure whereby hackers could take control of the core(s) through another core or non-core bus initiators. This may include isolation and protection for memory and peripheral while allowing acceptable shared space in memory among core(s) and non-core bus initiators.	Must have	Yes, Cortex-M + TRDC

9.7.5Domain ID

The TRDC shall be configured to support four Domain IDs, plus an additional Domain ID is used as the default domain that does not permit any bus accesses. The Domain ID for each master can be either driven as an input or assigned by software using the DAC. Within the XEA-1 platform, certain Domain IDs are reserved for certain purposes, as documented in the following table.

Table 215. i.MX RT2660 Domain ID assignment

Domain ID	Used by	Active Mode Default	Description
0	Any	CSSI, CPU0, DAP, MTR	Domain ID can be configured by OEM software. This domain is required by the TRDC software manager.
1	Any	DMA (all)	Domain ID can be configured by OEM software.
2	Any	Non-Media Initiators	Domain ID can be configured by OEM software.
3	Any	MEDIA_SS	Domain ID can be configured by OEM software.
15	Deny By Default	n/a	Domain ID value that is driven by any DAC that has not been configured by software (used during boot as the default domain). Accesses using this domain ID are always blocked.

[Change Request]: XEA1 platform requires a change request on TRDC DAC to add a parameter that configures what Domain IDs can be configured by software.

9.7.6 TRDC configuration

The TRDC shall support the following configuration options:

- Number of Domain IDs is 4
- Deny by default mode is disabled (inputs tied)
- TRDC manager instances are parameterized as follows:
 - IDAU valid bit is parameterized to reset to 1
 - TRDC manager global valid bits are parameterized to reset to 1
- DAC instances are parameterized as follows:
 - Process ID logic is disabled (single DAC register per instance)
 - PID input is disabled
 - Known Physical Address is disabled
 - Stream ID is disabled
 - Default DID is enabled
 - CSSI does not implement a DAC (defaults to domain 0 secure privilege)
 - CPU0 and MTR default to domain 0, secure user
 - All others default to domain 15, non-secure user
- MBC instances are parameterized as follows:
 - Global access registers are parameterized to required values
 - MBACSEL are parameterized to required values, per domain
- MRC instances are parameterized as follows:
 - Region size is parameterized to required values
 - Global access registers are parameterized to required values
 - Region 0 registers are parameterized to required values, per domain

9.7.7 TDRC Change Requests

The following minimum changes are required to TRDC to meet the requirements of the XEA1 platform.

- TKT0652703, closed
 - TRDC_MGR
 - Implement parameter VALID_RST that when set resets glb_valid_mdac, glb_valid_mrc, glb_valid_mbc to 1'b1. The rc_cr_lck still resets to 1'b0, allowing software to disable TRDC.
 - rc_global_valid_m <= VALID_RST;
 - rc_global_valid_b <= VALID_RST;

- `rc_global_valid_r <= VALID_RST;`
- TRDC_DAC
 - Implement parameters to set default access permissions from DAC when TRDC is enabled (global valid is set) but DAC configuration is invalid (suggest parameters MDAC_DACC_EN to enable default access permissions, MDAC_DACC_NS to set default non-secure attribute, MDAC_DACC_PR to set default privilege level):
 - assign {`s_rprot1, s_wprot1, s_rnonsecure_int, s_wnonsecure_int`} = (`s_valid_out`) ? {`md_s_rprot1, md_s_wprot1, md_s_rnonsecure, md_s_wnonsecure`} : (`glb_valid & MDAC_DACC_EN`) ? {`MDAC_DACC_PR, MDAC_DACC_PR, MDAC_DACC_NS, MDAC_DACC_NS`} : {`m_rprot1, m_wprot1, m_rnonsecure, m_wnonsecure`};
 - Remove “& did_mask[3:0]” from int_s_rdid and int_s_wdid outputs to allow MDAC_DDID to be set larger than TRDC_NUM DID. Change is backwards compatible provided MDAC_DDID < TRDC_NUM DID.
- TRDC_MBC
 - Fix security issue that allows secure bus initiators to execute from non-secure region of memory (since this is a security fix, it does not need to be parameterized)
 - `d_s?_glbac_mask[11:0] = tzm_enable ? {2'b11, ~s0_nse, 2'b11, ~s0_nse, {6{s0_nse}}}` : 12'hfff,
- TRDC_MRC
 - Implement the parameters GLBAC_RST and GLBAC_LK_RST (same implementation as existing MBC parameters)
 - Implement parameters REG0W0_RST[511:0] and REG0W1_RST[511:0] which set the 32-bit reset value for the Region 0 Descriptor Word 0 and 1, separately for each of the 16 possible domains:
 - `rd_rgn_cfg_w0[a] <= (a == 0) ? REG0W0_RST[31:0]` : 32'h0;
 - `rd_rgn_cfg_w1[a] <= (a == 0) ? REG0W1_RST[31:0]` : 32'h0;
 - Note that different parameter index is passed through to each trdc_mrc_dx_regs instance
 - Fix security issue that allows secure bus initiators to execute from non-secure region of memory (since this is a security fix, it does not need to be parameterized)
 - `nse_qual[i] = tzm_enable ? {2'b11, ~slv_rgn_cfg_w1[i][4], 2'b11, ~slv_rgn_cfg_w1[i][4], {6{slv_rgn_cfg_w1[i][4]}}}` : 12'hfff;
- TKT0655851
 - TRDC_MBC
 - Implement parameters Sn_MBACSEL_RST[63:0] which sets the 4-bit reset value that applies to all blocks within a given instance, separately for each of the 16 possible domains:
 - `rd_m0_cfg_w[d] <= { 8 { S0_MBACSEL_RST[2:0] } }`;
 - `rd_m1_cfg_w[d] <= { 8 { S1_MBACSEL_RST[2:0] } }`;
 - `rd_m2_cfg_w[d] <= { 8 { S2_MBACSEL_RST[2:0] } }`;
 - `rd_m3_cfg_w[d] <= { 8 { S3_MBACSEL_RST[2:0] } }`;

- Note that a different parameter index is passed through to each trdc_mbc_dx_regs instance (e.g.: S0_MBACSEL_RST[d*4+:4])
- Defining 4-bits per domain is based on the register definition for each block: { NSE, MBACSEL[2:0] }. Although NSE must always reset to 1'b0, keeping the parameter as 4-bits will greatly simplify readability and for specifying the reset value in CRR.

9.8 Device life cycle management

The i.MX RT2660 supports a security life cycle state model. The current lifecycle state determines the device functionality, debug and test port availability, and asset accessibility. The life cycle state is controlled by the LC_STATE fuse value, and state values are selected so that additional fuse bits are burned to advance the state. Because fuses control the life cycle state, moving to a more advanced state is an irreversible and permanent process. The life cycle can only be advanced and cannot return to a previous state.

The Boot ROM is responsible for checking the life cycle state. Based on the lifecycle state, the ROM determines what boot flow is used, including if control is passed to application code or not. The ROM also handles the opening of test and debug ports based on the life cycle state. If the part is in the Bricked state or any invalid life cycle state, then the ROM locks the part.

For the i.MX RT2660, the following life cycle state model shall be implemented under control of the CSSI_1_10 (S110) secure enclave.

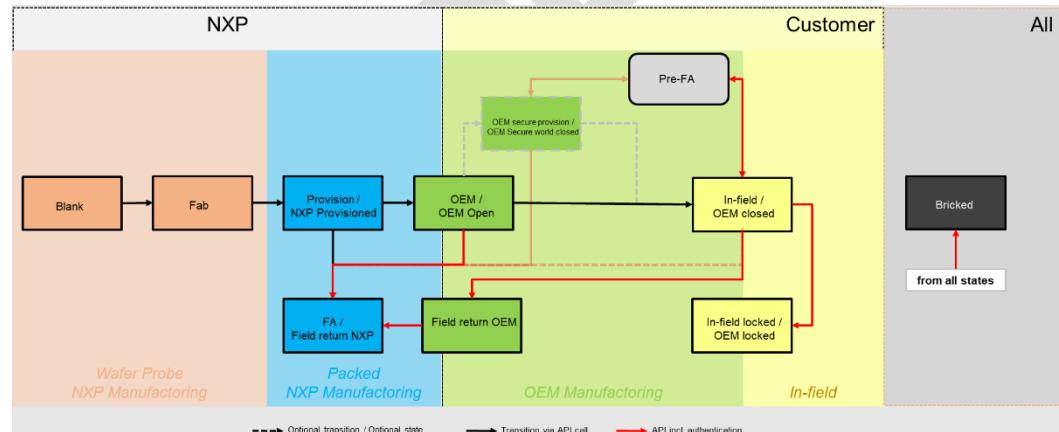


Fig 110. i.MX RT 2660 life cycle state model

For more information about device lifecycle management, please refer to the Security HW.AS document [11].

9.9 Encryption/Decryption functions for external memories

Table 216 lists requirement traceability of the security encryption/decryption external memories from SoC hardware perspective.

Table 216. IC requirements traceability: Security encryption/decryption external memories requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_SEC_11-1	On-The-Fly Encryption/Decryption for external NVM storage device	Heading	-
iMXRT2660_SEC_11-2	This Device shall support on-the-fly decryption and encryption of serial NOR flash or other NVM RAM device, such as MRAM or FRAM, connected to the first xSPI interface.	Must have	Yes, IPED [11]
iMXRT2660_SEC_11-3	The first xSPI interface shall support PRINCE CTR mode for inline encryption and decryption.	Must have	Yes, IPED [11]
iMXRT2660_SEC_11-4	The first xSPI interface shall support PRINCE GCM mode for inline encryption/decryption and authentication.	Must have	Yes, IPED [11]
iMXRT2660_SEC_11-5	The first xSPI interface shall support both Prince CTR & GCM modes simultaneously for different contexts.	Must have	Yes, IPED [11]
iMXRT2660_SEC_11-6	The encryption/decryption mechanism shall support up to four memory regions.	Must have	To be confirmed to security DRI
iMXRT2660_SEC_11-7	The encryption/decryption mechanism is compatible with wrap around reads for cache fills.	Must have	To be confirmed to security DRI
iMXRT2660_SEC_11-8	Encrypted/decrypted memory access through this xSPI interface shall be transparency to software, i.e. no configuration, control, or interrupts).	Must have	Yes, IPED after initial conf. [11]
iMXRT2660_SEC_11-9	Crypto performance requirement on the first xSPI interface is captured in the Memory section.	Must have	Information item
iMXRT2660_SEC_12-1	Inline Encryption/Decryption for External DRAM Memory	Heading	-
iMXRT2660_SEC_12-2	The second xSPI interface shall support PRINCE XEX mode for inline encryption and decryption.	Must have	Yes, IPED [11]
iMXRT2660_SEC_12-3	The encryption/decryption mechanism shall support up to four memory regions.	Must have	To be confirmed to security DRI
iMXRT2660_SEC_12-4	Encrypted/decrypted memory access through this xSPI interface shall be transparency to software, i.e. no configuration, control, or interrupts).	Must have	Yes, IPED after initial conf. [11]
iMXRT2660_SEC_12-5	This processor shall support 128-bit AES-CTR-KO (AES-CTR Keystream Only) mode provides AES-CTR keystream data.	Must have	Yes, IPED [11]

9.10 Safety

Table 217 lists the Safety traceability requirements from SoC hardware perspective.

Table 217. IC requirements traceability: Safety requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_SAF_1-1	Safety	Heading	-
iMXRT2660_SAF_1-4	This Device shall support Safety Manual.	Must have	Documentation item
iMXRT2660_SAF_1-5	This Device shall support ECC in CM85 TCMs, NPU TCM, and general purpose SRAM.	Must have	Yes, see CMPT_SS
iMXRT2660_SAF_1-6	The Device shall support ECC in the security subsystem for reliability purpose.	Should have	No, due to area reasons
iMXRT2660_SAF_1-7	This Device shall support FMEDA.	Must have	To be done during design phase
iMXRT2660_SAF_1-8	This Device shall support CM85 self-test library.	Must have	Software item, see SW.AS

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_SAF_1-9	This Device shall support internal memory self-test library.	Must have	Software item, see SW.AS
iMXRT2660_SAF_1-10	This Device shall meet standard IEC 60730 class B library.	Must have	Software item, see SW.AS
iMXRT2660_SAF_2-1	On-chip CRC	Heading	-
iMXRT2660_SAF_2-2	This Device shall implement a CRC module, which support 16-bit and 32-bit CRC operation.	Must have	Yes, see CRC module
iMXRT2660_SAF_2-3	The CRC module shall support user configurable polynomial.	Must have	Yes, see CRC module
iMXRT2660_SAF_2-4	The CRC module shall support user programmable seed value.	Must have	Yes, see CRC module
iMXRT2660_SAF_2-5	The CRC module shall support bitwise and byte wise transposition.	Must have	Yes, see CRC module
iMXRT2660_SAF_2-6	The CRC module shall support CRC result inversion.	Must have	Yes, see CRC module
iMXRT2660_SAF_3-1	On-chip ECC	Heading	-
iMXRT2660_SAF_3-3	This Device shall implement ECC on SRAM used for long-term key storage, if applicable.	Must have	To be confirmed to security DRI

10. System Boot & Configuration

*For more detailed information on the boot process,
please refer to the i.MX RT2660 Software RS document [17]*

10.1 Boot flow introduction

After a POR or WARM reset sequence, the CSSI_1_110 (S110) initiates a boot process by reading the content of the OTP memory, and storing the content into registers. The S110 then applies a reset configuration to the boot core (ARM Cortex-M85 in CMPT_SS) as indicated by the OTP memory. These configuration details are TBD, but may include items such as a boot vector, TZEN, TCM enables and ranges, etc. Having applied the reset configuration to the boot core, the S110 releases the boot core from reset.

The boot core then continues the boot process by executing code in the Boot ROM. The ROM will read the register copies of OTP configuration options to determine the boot device and its configuration, and proceed to boot from the device indicated, requesting authentication services from the S110 as indicated by the OTP options. The primary boot device may result in the downloading and executing of a secondary bootloader used to continue the boot process from a more complicated interface, such as Ethernet.

Table 218. IC requirements traceability: Boot requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_RnB_2-2	Coming out of reset, this processor always boot from Boot ROM on chip.	Must have	Yes

10.2 Boot ROM

The internal Boot ROM memory is used to store the boot code for the device. The boot functions implemented in the boot code shall at least include :

- Preparation of the system for execution of customer code residing in external memory ;
- ~~Provide the means to program the external flash memory ;~~
 - Initial program of a blank device ;
 - Erasure and re-programming of a previously programmed device ;
 - Programming of the external flash memory by the application program in a running system ;
- A Secure Boot which establishes a root-of-trust when the system comes out of reset ;
- Dual-image boot supported on xSPI interface; eXecute-In-Place boot from Octal/Quad/Dual/Single bit flash or Hyper-Flash connected to xSPI ;
- ~~Dual-image boot supported on eMMC and SD memory devices. Offset of second image configured by user in OTP ;~~
- Load-to-RAM and execute boot from:
 - Octal/Quad/Dual/Single bit flash or Hyper-Flash connected to xSPI ;
 - eMMC memory devices ;
 - eSD/SD/SDHC card memory devices.

- The boot flow defaults to serial download (or kboot) on the initial programming of a blank device or in case of a boot failure. Supported serial interfaces include USB, UART, SPI, and I2C ;
- ~~Boot ROM supports debugger mailbox requests, including debug authentication;~~
- Recovery boot from following interfaces: 1-bit SPI-flash connected to a LPSPI defined by user in OTP, and I2C.
- When waking up from a lower power mode that has SRAM retention, Boot ROM provides an option for the system to take low power wakeup flow without going through the full secure boot (or normal boot) process ;
- ROM patching is available to either patch code routines or fix data tables in Boot ROM area before executing the normal boot flow.
- The Boot ROM shall at least support the following secure boot features:
 - Supports encrypted boot for application image in external NVM device ;
 - ECDSA signature verification of image computed using NIST specifications ;
 - ~~Anti-rollback checking of firmware version.~~

Boot modes and boot decisions are controlled using pins and OTP fuses ;

For more information on Boot ROM firmware, please refer to the i.MX RT2660 SW.AS.

Table 219. IC requirements traceability: Boot ROM requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_RnB_4-1	Recovery boot	Heading	-
iMXRT2660_RnB_4-3	Boot from an I2C port which is attached to backup boot media on board, such as an EEPROM. The backup boot memory may contain a recovery boot image in case the main boot memory is not accessible or the boot image(s) on the main boot media failed.	Must have	Yes , HSP.LPI2C0 <i>Refer to SoC SW.AS</i>
iMXRT2660_RnB_4-4	Similar to Serial download via I2C port, SPI is another serial port commonly used for EEPROM.	Must have	Yes , HSP.LPSP0 <i>Refer to SoC SW.AS</i>
iMXRT2660_RnB_4-5	The Device shall provide an option for OEM to disable the recovery boot mechanism in a secure manner.	Must have	To be confirmed
iMXRT2660_RnB_5-1	Redundant Images	Heading	-
iMXRT2660_RnB_5-3	The Boot ROM shall support Redundant images boot by booting to the secondary image in case the boot to primary image fails.	Must have	<i>Refer to SoC SW.AS</i>
iMXRT2660_RnB_5-4	The Device shall implement a mechanism to mark the primary image failure, so the Boot ROM can boot from the secondary image in the subsequent boot cycles.	Must have	<i>Refer to SoC SW.AS</i>
iMXRT2660_RnB_5-5	The Device shall provide an option for OEM to disable the redundant images boot mechanism in a secure manner.	Must have	<i>Via user bits in OTP. To be defined</i>
iMXRT2660_RnB_6-1	Dual Images	Heading	-
iMXRT2660_RnB_6-2	The Device shall support firmware update. The Device will go through a full boot sequence after the new image was successfully stored in the NVM device. The ROM bootloader will load the new image.	Must have	<i>Refer to SoC SW.AS</i>
iMXRT2660_RnB_6-3	In case the Device successfully boot from the new image, the firmware version counter will advance and the old image is discarded.	Must have	<i>Refer to SoC SW.AS</i>

AS/RS identifier	Contents	Classification	Covered
	In case the Device fails to boot from the new image, the boot ROM will boot to the old image again. The boot failure will be logged.		
iMXRT2660_RnB_10-1	ROM Patch	Heading	-
iMXRT2660_RnB_10-2	The Device must support the ability to patch the on chip Boot ROM in a secure manner. This mechanism will enable software/manufacturing based patching of the boot ROM in case of error. The mechanism must be lockable by NXP (manufacturing change). Patches should be loaded only in the manufacturing flow and the mechanism should ensure that only patches from the fuse are possible. This is loaded by ROM code at the start of the boot process and after this is done the write permission to the space is removed and the execute permission enabled via a one way process. In addition as part of the end of the manufacturing flow all unused patches should be permanently disabled.	Must have	Targeted, orchestrated via S110 <i>To be verified during design phase</i>

10.3 Boot Memory devices

The i.MX RT2660 shall support boot from the following external memory devices

- Serial NOR flash via XSPI0 interface ;
- Serial NAND flash via XSPI0 interface ;
- eMMC Flash via USDHC0 interface ;
- SD removable card flash via USDHC0 interface.

Table 220. IC requirements traceability: Boot memory device requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_RnB_2-5	1) Serial NOR flash	Must have	Yes , via MAIN.XSPI0
iMXRT2660_RnB_2-6	2) Serial NAND flash	Must have	Yes , via MAIN.XSPI0
iMXRT2660_RnB_2-7	3) eMMC flash	Must have	Yes , via COMM.USDHC0
iMXRT2660_RnB_2-8	4) SD removable card flash	Must have	Yes , via COMM.USDHC0
iMXRT2660_RnB_2-9	The Boot ROM shall support bootloader from external Quad SPI NOR flash as specified in the Memory requirement section.	Must have	Yes from HW , refer to SW.AS
iMXRT2660_RnB_2-10	The Boot ROM shall support bootloader from external Octal SPI NOR flash as specified in the Memory requirement section.	Must have	Yes from HW , refer to SW.AS
iMXRT2660_RnB_2-11	The Boot ROM shall support bootloader from external Quad SPI NAND flash as specified in the Memory requirement section.	Must have	Yes from HW , refer to SW.AS
iMXRT2660_RnB_2-12	The Boot ROM shall support bootloader from external Octal SPI NAND flash as specified in the Memory requirement section.	Must have	Yes from HW , refer to SW.AS
iMXRT2660_RnB_2-13	In case the serial NAND ECC is disabled to reduce boot time, the boot ROM shall include SW ECC operation.	Must have	Yes from HW , refer to SW.AS
iMXRT2660_RnB_2-14	The Boot ROM shall support bootloader from eMMC flash as specified in the Memory requirement section.	Must have	Yes from HW , refer to SW.AS
iMXRT2660_RnB_2-15	The Boot ROM shall support eMMCV5.0 and eMMCV5.1 flash.	Must have	Yes from HW , refer to SW.AS
iMXRT2660_RnB_2-16	The Boot ROM shall support bootloader from removable SD card as specified in the Memory requirement section.	Must have	Yes from HW , refer to SW.AS

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_RnB_2-17	The Boot ROM shall support SD3.0 card flash.	Must have	Yes from HW, refer to SW.AS
iMXRT2660_RnB_2-18	The Device shall support bootloader from Low-Voltage (LV) SD card. The Boot ROM must include LV SD card identification sequence.	Must have	Yes from HW, refer to SW.AS

10.4 Boot Configuration

Settings that affect the boot flow include the state of the BOOT_MODE pin, security and lifecycle fuses, and Boot Configuration fields in the OTP fuses.

10.4.1 Boot Pins

The state of the BOOT_MODE pin decides whether Boot ROM takes the normal boot flow, or forces a serial download path. This signal is muxed on PIO6_12 and PIO6_13 pins. BOOT_MODE is the default function on this GPIO.

The value of the BOOT_MODE pin is sampled at the exit of a system reset event and stored in a system configuration register. The Boot ROM reads this register bit to determine the boot path.

Table 221. i.MX RT2660 Boot pin configuration

BOOT_MODE[1:0]	Boot device	Comment
00	xSPI0	
01	Auto ISP	UART, SPI-slave, I2C-slave, USB-HID
10	xSPI1	
11	xSDHC0	eMMC or SD set in OTP

This assumes pull-down resistor are enabled by default on these pins and default configuration is xSPI0. Single pin is needed to toggle between xSPI0 and ISP mode.

The boot interface assignments is part of PinMux. Please refer to sheet "Boot Pin" of file i.MXRT2660 IO ver <version>.xlsx in share point [Peripheral Input Mux](#). Table 222 is a snapshot, of boot pin and subject change.

Boot pin assignment table			
Boot interface	Pins		Comments
xSPI	XSPI0-NOR/NAND FLASH BOOT		
	PIO6_0	1 MAIN.XSPI0_SCLK0	XSPI0-NOR/NAND Flash boot
	PIO6_1	1 MAIN.XSPI0_SS0_N	XSPI0-NOR/NAND Flash boot
	PIO6_2	1 MAIN.XSPI0_DATA0	XSPI0-NOR/NAND Flash boot
	PIO6_3	1 MAIN.XSPI0_DATA1	XSPI0-NOR/NAND Flash boot
	PIO6_4	1 MAIN.XSPI0_DATA2	XSPI0-NOR/NAND Flash boot
	PIO6_5	1 MAIN.XSPI0_DATA3	XSPI0-NOR/NAND Flash boot
	PIO6_6	1 MAIN.XSPI0_DQSO	XSPI0-NOR/NAND Flash boot
	PIO6_7	1 MAIN.XSPI0_DATA4	XSPI0-NOR/NAND Flash boot
	PIO6_8	1 MAIN.XSPI0_DATA5	XSPI0-NOR/NAND Flash boot
	PIO6_9	1 MAIN.XSPI0_DATA6	XSPI0-NOR/NAND Flash boot
	PIO6_10	1 MAIN.XSPI0_DATA7	XSPI0-NOR/NAND Flash boot
	PIO6_11	1 MAIN.XSPI0_SS1_N	XSPI0-NOR/NAND Flash boot
	XSP11-PSRAM		
	PIO5_0	1 MAIN.XSP11_SS0_N	XSP11-PSRAM boot
	PIO5_1	1 MAIN.XSP11_DATA0	XSP11-PSRAM boot
	PIO5_2	1 MAIN.XSP11_DATA1	XSP11-PSRAM boot
	PIO5_3	1 MAIN.XSP11_DATA2	XSP11-PSRAM boot
	PIO5_4	1 MAIN.XSP11_DATA3	XSP11-PSRAM boot
	PIO5_5	1 MAIN.XSP11_SCLK0	XSP11-PSRAM boot
	PIO5_6	1 MAIN.XSP11_DATA4	XSP11-PSRAM boot
	PIO5_7	1 MAIN.XSP11_DATA5	XSP11-PSRAM boot
	PIO5_8	1 MAIN.XSP11_DATA6	XSP11-PSRAM boot
	PIO5_9	1 MAIN.XSP11_DATA7	XSP11-PSRAM boot
	PIO5_10	1 MAIN.XSP11_DQSO	XSP11-PSRAM boot
	PIO5_11	1 MAIN.XSP11_SCLK0_N	XSP11-PSRAM boot
	PIO5_12	1 MAIN.XSP11_DATA8	XSP11-PSRAM boot
	PIO5_13	1 MAIN.XSP11_DATA9	XSP11-PSRAM boot
	PIO5_14	1 MAIN.XSP11_DATA10	XSP11-PSRAM boot
	PIO5_15	1 MAIN.XSP11_DATA11	XSP11-PSRAM boot / USDHC0 boot
	PIO5_16	1 MAIN.XSP11_DQS1	XSP11-PSRAM boot / USDHC0 boot
	PIO5_17	1 MAIN.XSP11_DATA12	XSP11-PSRAM boot / USDHC0 boot
	PIO5_18	1 MAIN.XSP11_DATA13	XSP11-PSRAM boot / USDHC0 boot
	PIO5_19	1 MAIN.XSP11_DATA14	XSP11-PSRAM boot / USDHC0 boot
	PIO5_20	1 MAIN.XSP11_DATA15	XSP11-PSRAM boot / USDHC0 boot
USB	USB0_VBUS	USB0_VBUS	
	USB0_DM	USB0_DM	
	USB0_DP	USB1_DP	
SPI	PIO3_28	8 HSP.LPSP10_PCS0	SPI boot
	PIO3_29	8 HSP.LPSP10_SCK	SPI boot
	PIO3_30	8 HSP.LPSP10_SDO	SPI boot
	PIO3_31	8 HSP.LPSP10_SD1	SPI boot
I2C Slave	PIO2_5	8 HSP.LP12C0_SDA	I2C slave boot
	PIO2_6	8 HSP.LP12C0_SCL	I2C slave boot
UART	PIO2_7	1 HSP.LPUART0_TX	UART boot
	PIO2_8	1 HSP.LPUART0_RX	UART boot
USDHC 0	PIO5_15	2 COMMUSDHCO_CLK	XSP11-PSRAM boot / USDHC0 boot
	PIO5_16	2 COMMUSDHCO_CMD	XSP11-PSRAM boot / USDHC0 boot
	PIO5_17	2 COMMUSDHCO_DATA0	XSP11-PSRAM boot / USDHC0 boot
	PIO5_18	2 COMMUSDHCO_DATA1	XSP11-PSRAM boot / USDHC0 boot
	PIO5_19	2 COMMUSDHCO_DATA2	XSP11-PSRAM boot / USDHC0 boot
	PIO5_20	2 COMMUSDHCO_DATA3	XSP11-PSRAM boot / USDHC0 boot
BOOT_MODE[1:0]	PIO6_12	1 ISP boot select 0	11 - xSP11 10 - Auto ISP (UART, SPI-slave, I2C-slave, USB-HID, eUSB)
	PIO6_13	1 ISP boot select 1	01 - xSPI0 00 - SDHC0 (eMMC or SD set in OTP)

Table 222. Fig 122. Overview of i.MX RT2660 assigned boot interfaces and -pins

Table 223. IC requirements traceability: Boot configuration requirements – part i

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_RnB_9-2	The Device should designate pins which can be used to indicate desired boot modes. The number of boot mode pins should be kept at minimum (not more than 2 pin).	Must have	Yes, 2 boot pins

10.4.2 Security and lifecycle fuses

During its life, a device goes through several lifecycle states. Some of the lifecycle states are there to ease the testing and development when the device is physically present in different environments, E.G., manufacturing fab, silicon manufacturer's test floor, silicon manufacturer's inventory, OEM's

contract manufacturer facilities, OEM facilities, in field, etc. While easing the testing and development, it is important to protect security assets available on a device in a given lifecycle state. For each lifecycle state, we define access rights, i.e., what kind of access to the device internals is allowed under what conditions. We also define what assets are available and what kind of asset protection is implemented. Transition between different lifecycle states is an irreversible process.

The security and lifecycle state of the device affects boot flow. The security configuration and device lifecycle are controlled with a set of fuses in the OTP. There is an 8-bit word defined for security and lifecycle of this device. The security and lifecycle word is output from the OTP during the reset sequence and is visible from the registers in the Secure Miscellaneous System Control Module (SMSCM). The Boot ROM accesses the security and lifecycle state registers early in the boot process to make decisions that affect the boot flow.

For more information on security and lifecycle fuses, please refer to the Security HW.AS [11].

10.4.3 Boot Configuration OTP

The OTP contains the following field settings that affect boot flow.

- Boot mode
 - Enable BOOT_MODE pin ;
- System configuration
 - Boot speed selection ;
- External memory configuration
 - Type of flash device ;
 - Flash auto probe ;
 - Flash auto probe type ;
 - Flash device dummy cycle ;
 - Hold time ;
 - Flash operating frequency ;
- Serial download peripheral configuration
 - Enable peripherals (USB, LPUART, LPSPI, ~~LPI2C~~) ;
 - Peripheral detection timeout ;
 - USB VID / USB PID ;
 - USB descriptor strings ;
 - ~~I2C slave address~~ ;
 - SPI NOR flash address size (3 or 4 bytes) ;
- Secure boot options
 - Failure mode: Infinite sleep or serial download ;
 - Failure indicator.

Table 224. IC requirements traceability: Boot configuration requirements – part ii

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_RnB_9-3	The Device should instantiate OTP which enable any combination of boot modes and boot configurations. The OEM can program these OTP which will then tell The Device which boot source will be looked at for a valid image and how to configure the resources on The Device to support the select boot source and boot mode.	Must have	Yes, Targeted
iMXRT2660_RnB_9-4	The Device shall implement a mechanism to allow user to configure boot modes and boot options without programming OTP. This feature is useful during product development.	Must have	Yes, via boot pins

10.5 POR and Boot process

10.5.1POR hardware sequence

The power-on-reset sequence is taken care of by the finite state machine of the PMC_SS [9]. The exact sequence is still to be detailed out. The requirement of the POR hardware sequence is as follows:

- Total duration of the POR hardware sequence shall target a duration of below 2ms. Up to 5ms max. can be acceptable across process-voltage-temperature corners.
- The trigger for the SoC to power up is the presence of VDD_PMU and VBAT_AON supplies along with a rising edge on the POR_b pin ;
- During the POR hardware sequence, the PMC_SS and CGU_SS are started ;
- The SoC is supply- and clocks shall be auto-trimmed by restoring the trim settings of the trimmed supply-, reference and clock components as stored in OTP ;
- The POR hardware sequence is ended once the PMC_SS output supplies are available, and the SoC is set to operate in Normal mode at 500 MHz main_rootclk frequency.

The details of the SoC power up sequence are to be further outlined by the analog team during design phase.

10.5.2Boot process

There are two main boot flows from a POR: (1) Fast Boot, (2) Normal Boot.

The Fast Boot mechanism is defined for implementations where there is a need for an OEM image to respond to a CAN BUS query/message from a certified CAN stack within a 50ms time frame. The NXP SW mechanisms cannot provide this response, so the boot must proceed in a manner in which the OEM image can be launched as quickly as possible. Since there must be time for the OEM image to initialize, recognize the CAN query, and provide a response, the NXP HW + SW cannot utilize the full measure of the 50ms target time frame. To facilitate this, Fast Boot is defined with the following restrictions:

- The OEM image must be limited in size i.e. up to 3 MBytes ;
- The OEM image is in XIP memory (meaning the image is not loaded during boot), and will be validated and executed from this location ;
- Fast Boot is only supported on one boot device (xSPI0) ;
- The Fast Boot flow is selected by a flag set in the OEM container, this flag can be read by the boot core from the OEM container found on the boot device ;
- All of the above conditions must be met for the Fast Boot sequence to be selected – if any of these conditions are NOT met, the boot defaults to a Normal Boot.

These may be further subdivided by update and recovery mechanisms which are defined later.

10.5.3Normal Boot

Boot ROM follows this path when device goes through a WARM reset or POR, except for low-power wakeup. Boot ROM prepares the system for execution of application code residing in external NVM device.

Boot ROM performs the following tasks in normal boot sequence:

- Locates boot image ;
- Executes secure boot with S-110 if security function is enabled ;
- **Optionally loads initial TRDC setting from an extended header, that is part of the signed image, and configures TrustZone-M if enabled ;**
- Starts image execution.

In case normal boot fails, for example if the boot image is not found, the Boot ROM executes a serial download protocol. The following sequences described the different boot stages of the i.MX RT2660 under the normal boot sequence.

time	Boot Core – cm85 TZ executing SysBootROM	signal / event	SE state	signal / event	Apps core – cm85 executing non-secure	Notes
t0	POR	power-on	POR		POR	
t1	POR		execute ROM init (+patch)		POR	
t2	POR		set tRDC R/W		POR	
t3	execute ROM init	←	release boot core from reset		---	
t4	bootflow or provision (b)	---		---	---	
t5	check boot device	---		---	---	via pins
t6	cfg flash interface	---		---	---	
t7	load s110 FW image	---		---	---	NXP container
t8	signal validation	→	validate s110 FW		---	
t9	---		validate s110 FW		---	
t10	---		execute s110 FW		---	
t11	check Fast Boot flag (y)	←	signal ready		---	FB flag in OEM container
t12	signal FB validation	→	validate XIP OEM image		---	
t13	---		validate XIP OEM image		---	
t14	---		set tRDC wide open for Apps core		---	
t15	branch to non-secure XIP and execute OEM image	←	signal ready		---	
t16	---		---	→	execute init & CAN response	

Fig 111. i.MX RT2660 normal boot sequence

10.5.4Fast Boot

The main purpose of the fast boot sequence is to address a boot requirement for automotive use case. From power on, the device must go through cold boot, which include secure Boot sequence, and respond to a CAN message within 50ms, assuming the boot image is 3MB and resides on an external NOR flash device.

The i.MX RT2660 shall detect the fast boot selection from OTP memory of via boot pins. The fast boot sequence is followed after a WARM reset or POR, optionally for low-power wakeup. Boot ROM prepares the system for execution of application code residing in external NVM device.

Boot ROM performs the following tasks in fast boot sequence:

- Locates boot image ;
- Executes secure boot with S-110 if security function is enabled ;
- Optionally loads initial TRDC setting from an extended header, that is part of the signed image, and configures TrustZone-M if enabled ;
- Starts image execution.

In case fast boot fails, for example if the boot image is not found, the Boot ROM executes a serial download protocol. The following sequences described the different boot stages of the i.MX RT2660 under the fast boot sequence.

time	Boot Core – cm85 TZ executing SysBootROM	signal / event	SE state	signal / event	Apps core – cm85 executing non-secure	Notes
t0	POR	power-on	POR		POR	
t1	POR		execute ROM init (+patch)		POR	
t2	POR		set tRDC R/W		POR	
t3	execute ROM init	←	release boot core from reset		---	
t4	bootflow or provision (b)		---		---	
t5	check boot device		---		---	via pins
t6	cfg flash interface		---		---	
t7	load s110 FW image		---		---	NXP container
t8	signal validation	→	validate s110 FW		---	
t9	---		validate s110 FW		---	
t10	---		execute s110 FW		---	
t11	check Fast Boot flag (y)	←	signal ready		---	FB flag in OEM container
t12	signal FB validation	→	validate XIP OEM image		---	
t13	---		validate XIP OEM image		---	
t14	---		set tRDC wide open for Apps core		---	
t15	branch to non-secure XIP and execute OEM image	←	signal ready		---	
t16	---		---	→	execute init & CAN response	

Fig 112. i.MX RT2660 fast boot sequence

Table 225. IC requirements traceability: Boot time requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_RnB_11-2	The Device shall support time constraint boot requirement for automotive use case. From power on, the device must go through cold boot, which include secure Boot sequence, and respond to a CAN message within 50ms, assuming the boot image is 3MB and resides on an external NOR flash device.	Must have	Yes, when booting at 250MHz Refer to SW.RS [17]

10.6 Serial Download

The serial download protocol is used to load a boot image from an external device through the supported interface. The serial download protocol can be used to:

- Program the application image into external flash for customer factory programming or during development ;
- Re-program the image for a software update or when the part fails to boot in the field ;

The i.MX RT2660 shall support serial download through COMM.USBO or through HSP.LPUART0 or HSP.LPSPI0 or HSP.LPI2C0. When serial download protocol detects an active interface, it responds to the commands sent by a host communicating on one of these ports. The host can be a firmware download application running on a PC or an embedded host processor communicating with the serial

download protocol. Commands are provided to write external flash or RAM and get/set bootloader options and property values.

Table 226. IC requirements traceability: Serial download requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_RnB_3-4	1) USB	Must have	Yes, USB0
iMXRT2660_RnB_3-5	2) UART	Must have	Yes, LPUART0
iMXRT2660_RnB_3-6	3) SPI	Must have	Yes, LPSPIO
iMXRT2660_RnB_3-7	The Device shall boot from an USB port which is attached to the outside world, such as an user's PC. This boot option is a common practice during silicon bring up to product development. This boot option is sometimes used for boot in the field for product diagnostic	Must have	Targeted, to be verified during design phase
iMXRT2660_RnB_3-8	The Device shall boot from an UART port which is attached to the outside world, such as an user's PC. Similar to Serial download via USB port, UART is another serial port commonly used for this purpose.	Must have	Targeted, to be verified during design phase
iMXRT2660_RnB_3-9	The Device shall boot from a SPI port which is connected to another external MCU or MPU device on board. The external MCU/MPU will act as the host processor providing the downloading image to this MCU device.	Must have	Targeted, to be verified during design phase

10.7 Low-power Wakeup

The low-power wakeup is an optional path, focused on reducing boot time to start executing application code as soon as possible. The device wakes up from Power Down mode, which has RAM retention, and resumes operation after exiting the wakeup routine.

Upon detecting low-power wakeup condition, Boot ROM takes the boot flow to the wakeup routine. Boot ROM recovers CPU state, checks stack pointer, computes CRC of stack pointer and core state, and reloads the TRDC configuration. If CRC is failed, Boot ROM will save the CRC failure status for use later by "system health check" code, and take the device through normal boot path.

The wakeup routine skips boot image authentication to reduce boot time. It can be assumed that code was successfully authenticated on the last full boot before the device enters Power Down / Deep Power Down mode and skips secure boot when it wakes.

10.8 Debugger Request

The main purpose of this boot mode is debug authentication. It allows the debugger to authenticate over SWD or JTAG port connected to the device. Upon detection pending request from debugger, the Boot ROM enters request/response handler.

10.9 Secure Boot

A key feature of the Boot ROM is the ability to perform a secure boot. This is supported by the nboot security library which is a sub-component of the ROM code. nboot uses a combination of hardware and software with a Public Key Infrastructure (PKI) protocol to protect the system from executing unauthorized programs.

The secure boot process requires a signed image. The signing process is done during the image build process by the private key holder, and the signatures are then included as part of the final application image. If secure boot is enabled, the Boot ROM verifies the signature verification to authenticate the application image.

In addition to secure boot, an nboot API is exported for use by the customer application. This allows the application to authenticate pieces of code and data.

Table 227. **IC requirements traceability: Secure boot & firmware update requirements**

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_RnB_7-2	The Device shall support Secure Boot at boot time. Secure boot requirements are specified in the Secure section (tap).	Must have	Yes
iMXRT2660_SEC_17-2	The Device shall support Secure Boot at boot time. During Secure boot, the software image is authenticated versus its signature using a selected signature authentication algorithm.	Must have	Yes, targeted
iMXRT2660_SEC_17-5	This Device shall support image signing key revocation. With a minimum revocation count of 16 incidents.	Must have	Targeted, to be confirmed during design phase
iMXRT2660_SEC_17-6	This Device shall support at least 4 immutable root key hashes in OTP hardware.	Must have	Targeted, to be confirmed during design phase
iMXRT2660_SEC_17-7	Boot keys or hashes thereof shall never be visible outside the security enclave block without specific reason. In most cases these are not vulnerable if visible but the assumption should be to minimize exposure.	Must have	Yes, HW+SW [11] [62]
iMXRT2660_SEC_17-8	This Device shall support ability for individual images to be signed with NXP only or OEM key.	Must have	Yes, HW+SW [11] [62]
iMXRT2660_SEC_17-9	This Device shall allow OEM signature verification covering NXP signed images. In other words, an OEM will have the option to include NXP firmware that are going to run on the main CPU loaded to the SOC via OEM signature verification along with any OEM-specific firmware that needs to be signed.	Must have	Targeted, to be confirmed during design phase
iMXRT2660_SEC_17-10	The Device shall support secure firmware update based on the ECDSA on P-256/P-384 algorithm or the PQC scheme with Dilithium/LMS.	Must have	Yes, HW+SW [62]
iMXRT2660_SEC_17-11	This Device shall support anti-rollback mechanism during secure boot and secure update.	Must have	Yes, HW+SW [11] [62]
iMXRT2660_RnB_8-2	The Device shall implement ROM mechanism to support fully encrypted boot when boot from external serial NOR flash.	Must have	Yes, HW+SW [11] [62]

10.10 OTP fuse map

The i.MX RT2660 Fuse map template shall be based on the template from i.MX product family, e.g. Fuse map from i.MX95 . The template file can be found here:

[i.MX RT2660 Fusemap template.xlsx](#)

TODO: Should sync with the fuse Kaizen team to make sure you are using the best template. You might need to look at Tunis instead of i.MX 95

This Section lists the Fuse map items. Note that this list not an exhaustive list at this stage of the project. The Fuse map needs to be further matured by the next phase gate (PPA), and the initial version shall be documented as part of the Detailed Technical Specification (DTS).

Fuse allocation items:

- Lock Configuration ;
- DEVICE_ID /SID Configuration ;

- HW/SW Configuration, Tester Configuration ;
- Boot Configuration ;
- Analog Configuration ;
- MTR ;
- Memory Configuration ;
- CSSI_1_10 fuses ;
- CSSI_1_10 IPED Config ;
- ROM Patch (CSSI_1_10) ;
- ROM Patch (M85) ;
- General Purpose fuses (NXP) ;
- General Purpose fuses (Customer) ;
- CRC ;
- ECC.

11. System Debug

This Chapter provides a description of the system debug infrastructure of the i.MX RT2660 SoC.

11.1 Overview

The i.MX RT2660 debug & trace architecture is partitioned among system level blocks as shown in the following figure. The external debugger is connected to the JTAG/SWD Test Access Port, as referred to as JTAG/SWD-TAP port. The test access port is used by NXP Product & Test Engineering team for performing SoC production testing. The JTAG/SWD-TAP port is connected to the Debug Access Port (DAP).

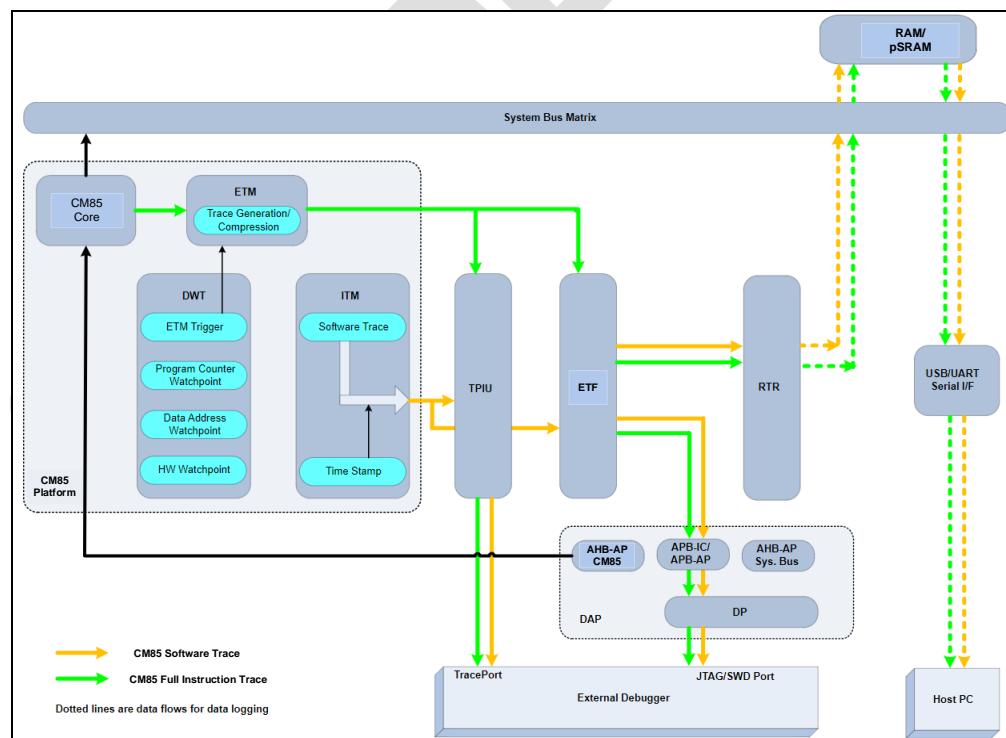


Fig 113. High-level overview of the i.MX RT2660 Debug architecture

The debug & trace architecture provides support for debug and trace of core modules. Some of the features the debug system provides are:

- Support both 1149.1 JTAG 5-pin interface and Arm Serial Wire Device (SWD) 2-pin interfaces
 - The ARM Debug Port (DP) can switch between JTAG and SWD ;
 - The SWJ-DP routes JTAG/SWD accesses to the appropriate Access Port (AP) ;
- Support both non-intrusive trace and halt-mode debug options ;
- Supports capture of trace data using any of the following:
 - ARM CoreSight Embedded Trace FIFO (ETF) with 8kB SRAM ;
 - System memory (on-chip SRAM or external XSPI memory) via the ARM CoreSight Embedded Trace Router (ETR) ;
 - ARM CoreSight Trace Port Interface Unit with 4-pin parallel interface ;
 - ARM CoreSight Serial Wire Output (SWO) ;
- Timestamp distribution to the different trace modules ;
- Cross Triggering to pass debug events between different cores and trace components.

Table 228. IC requirements traceability: Debug requirements

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_DEB_1-4	Debug viewpoints	Heading	-
iMXRT2660_DEB_1-5	Hardware debug – debug by the design team of hardware issues within specific cores during development	Must have	Yes, see debug infra
iMXRT2660_DEB_1-6	DFT/Failure analysis – debug of a part after production to understand issues or for manufacturing test.	Must have	Yes via JTAG
iMXRT2660_DEB_1-7	Firmware debug – debug of chip level firmware (primarily in the system controller)	Must have	Yes, supported
iMXRT2660_DEB_1-8	Secure/privileged debug – debug of software which is required to be controlled to specific scenarios, as an example secure debug.	Must have	Yes, via S110
iMXRT2660_DEB_1-9	Debug of a particular context – debug of a main CPU or security unit. The latter is restricted to NXP-only debug.	Must have	Yes via CoreSight
iMXRT2660_DEB_1-10	Noninvasive debug – tracing or monitoring of the behavior of a particular context or set of contexts.	Must have	Yes via CoreSight
iMXRT2660_DEB_1-11	Performance analysis – collection of information to understand overall system behavior at a high level for performance or power analysis	Must have	Yes, via measurement
iMXRT2660_DEB_1-12	User part – extremely limited or no access	Must have	Yes, via lifecycle
iMXRT2660_DEB_2-1	Debug Methods	Heading	-
iMXRT2660_DEB_2-2	Debug may be carried out by several different methods irrespective of the actual viewpoint of the operation. This processor should support following debug methods.	Must have	Supported
iMXRT2660_DEB_2-3	Debug via a host, here a hardware debug unit connected to an external PC is used via the CoreSight infrastructure.	Must have	Yes, see Fig 113
iMXRT2660_DEB_2-4	Debug via logic analyzer, here we are doing hardware debug via the debug mechanisms or scan dump primarily, but it may also include parts of the CoreSight infrastructure.	Must have	Yes, see Fig 113
iMXRT2660_DEB_2-5	Software level debug where we have a running RTOS system, for example, and we use the system monitor tools, such as an USB or UART connection.	Must have	Yes, supported

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_DEB_2-6	Self-hosted debug where the debug monitor is running on the debug core. Debug events cause exceptions, and these software exception handlers drive the core debug logic.	Must have	Yes, supported
iMXRT2660_DEB_3-1	Debug mechanism	Heading	-
iMXRT2660_DEB_3-2	This processor shall implement two underlying mechanisms to support these debug approaches: - CoreSight debug: a mechanism provided by ARM to allow access for debug to particular cores. - Hardware test & debug: a mechanism which gives access to underlying hardware.	Must have	Yes, via JTAG/SWD-TAP
iMXRT2660_DEB_3-4	Control and access to these mechanisms is dependent on credentials and shall be largely managed in the security functions of the processor.	Must have	Yes, via S110 [11]

11.2 Debug Access Port (DAP)

The DAP is a standard Arm component, comprising of several components. These components are used to access the DAP from an external debugger, and Access Ports to access on-chip debug system resources. The DAP supports 1149.1/Arm SW-DP interface, which means that the JTAG interface can be operated in either standard 5-pin JTAG-DP interface or in 2-pin SW-DP interface. Serial Wire port (SWJ-DP) consists of a wrapper around the JTAG-DP and SW-DP. It selects JTAG or SWD as the connection mechanism and enables either JTAG-DP or SW-DP as the interface to the various on-chip debug/trace components.

Fig 114 shows a block diagram of the i.MX RT2660 DAP.

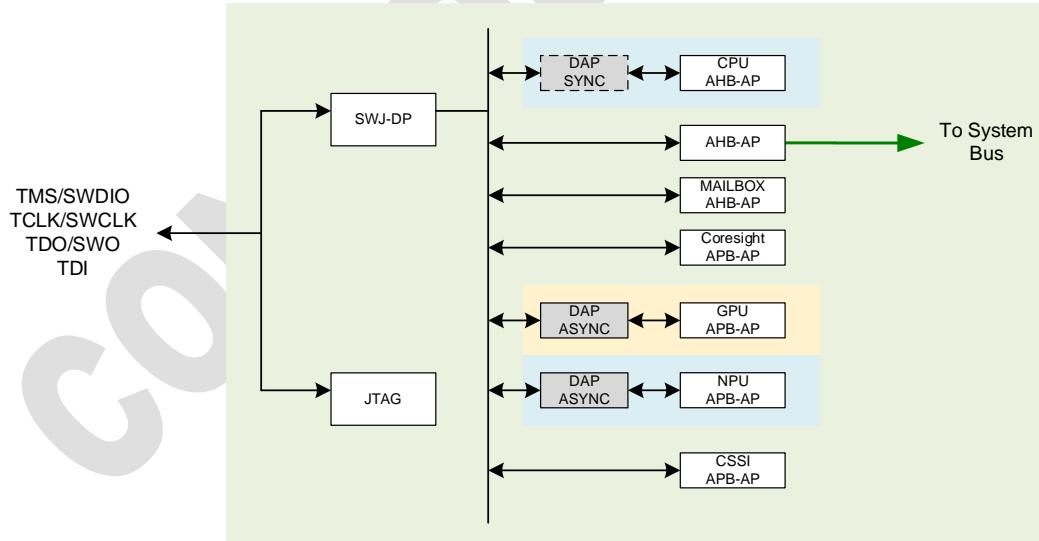


Fig 114. i.MX RT2660 Debug Access Port (DAP) block diagram

The selection of different access ports in the DAP is done based on the APSEL value set in the SELECT register of SWJ-DP. APSEL is 31:24 bit field of the DAP SELECT register. Internal cores are implemented at the end of the address range so debug tools need to explicitly select them. The APSEL shall be decoded as given in the following table.

Table 229. i.MX RT2660 DAP AP selection

Destination	APSEL	Interface
CM85	00h	AHB-AP
SoC AHB-AP	01h	AHB-AP
Debug Mailbox (ISP-AP)	02h	AHB-AP
Coresight Registers (APBIC)	03h	APB-AP
<reserved>	04h - 1Bh	Default response
GPU ZEN-V	1Ch	APB-AP
NPU ZEN-V	1Dh	APB-AP
CSSI ZEN-V	1Fh	APB-AP

Table 230. IC requirements traceability: CoreSight debug & trace requirements (part i)

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_DEB_4-3	The DAP and associated functions which provide control of overall CoreSight system. User should be able to access the DAP either via JTAG/SWD pins or via an internal set of registers.	Must have	Yes

11.3 JTAG

The ARM SWJ-DP and SoC JTAG controller are implemented in parallel and sharing the same pins. The SoC JTAG controller implements different JTAG instructions (IRCODE) from the SWJ-DP, so each JTAG instruction selects either the SoC JTAG controller or the SWJ-DP. The SWJ-DP implements instructions related to debug access to the device and the SoC JTAG controller implements the boundary scan and test mode related instructions.

The JTAG instruction decoding should be aligned with i.MX2660_DFT_AS_v<version>.xlsx in share point [DFT](#).

Table 231. i.MX RT2660 JTAG instruction decoding – subject to change.

Instruction	Value	Module	Description
EXTEST	0000b	JTAGC	Boundary Scan
PRELOAD / SAMPLE	0001b	JTAGC	Boundary Scan
HIGHZ	0010b	JTAGC	Boundary Scan
CLAMP	0011b	JTAGC	Boundary Scan
IDCODE	0100b	JTAGC	Boundary Scan
MAIN_TCB	0101b	JTAGC	Test Mode
SEC_TCB	0111b	JTAGC	Test Mode
ABORT	1000b	SWJ-DP	Arm Debug
CLK_TCB	1001b	JTAGC	Test Mode
DPACC	1010b	SWJ-DP	Arm Debug
APACC	1011b	SWJ-DP	Arm Debug
IDCODE	1110b	SWJ-DP	Arm Debug
BYPASS	1111b	JTAGC	Bypass Mode

11.3.1 JTAG IDCODE

Each device shall implement a single hardcoded JTAG IDCODE, that is readable via the JTACG IDCODE instruction and by a memory mapped register in SYSCON.

The JTAG IDCODE shall follow the NXP numbering scheme.

11.3.2 JTAG activity

The JTAG controller (or other debug logic) shall generate one or more signals that indicate activity for the CSSI-110. This could be a single signal that indicates any activity, or it could be multiple signals that differentiate between:

- JTAG/SWD activity (such as selecting SWD or non-Bypass instruction) ;
- Test activity (such as decoding a test register or when a valid test password is entered) ;
- Debug activity (such as DBGPWRUPREQ asserted or a memory access on a AHB-AP/APB-AP other than Debug Mailbox) ;
- Trace activity (such as TRCENA from CPU asserted).

Table 232. **IC requirements traceability: Hardware test & debug requirements (part i)**

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_DEB_5-3	This processor shall include a standard JTAG port.	Must have	Yes

11.4 Security Control

*For more detailed information on the RT2660 SoC security,
please refer to the i.MX RT2660 Security HW.AS document [11]*

Debug access is controlled by the CSSI-110 through decoding of the lifecycle state as programmed in OTP memory. In certain lifecycles, debug access is contingent upon a debug authentication handshake with CSSI-110.

The following usecases shall be considered when defining the debug access control:

Access to the Debug Mailbox is supported in all life cycles.

- In OEM Open the application cores (eg: CM85) shall support a debug connection during warm reset to halt core execution before the first instruction. Debug access to system memory or TCM contents is not required until the application core is released from reset ;
- In OEM Open the SoC AHB-AP does not require access until the application core is released from reset ;
- Debug access to NXP internal cores shall only be enabled when debug access to application cores has been enabled via lifecycle or authentication ;
- The application core shall support a debug connection during warm reset in an NXP lifecycle for the purpose of debugging the BootROM execution ;
- The NXP security core (CSSI-110) shall require authentication before enabling any debug access to the security core ;
- The TCU (with a valid test password and when in a lifecycle state that supports test) can enable debug access via the SoC level AHP-AP (and/or TESTPORT) during warm

reset. The TRDC shall support register accesses from the AHB-AP and/or TESTPORT to the CSSI-110 and other test infrastructure components.

To meet these usecases, the following sections describe what debug functions should be available in each life cycle state.

11.4.1BLANK

The following debug functions shall be supported in this lifecycle:

- Debug access to application CPU shall be disabled ;
- Debug access to SoC AHB-AP shall be disabled (test mode entry is enabled and TCU can enable the AHB-AP during warm reset with a valid test password) ;
- Debug access to Debug Mailbox shall be always enabled ;
- Debug access to CoreSight registers shall be disabled ;
- Debug access to NXP internal cores shall be disabled ;
- Debug access to NXP security core shall be disabled.

11.4.2NXP Fab/Provisioned/Return

The following debug functions shall be supported in these lifecycles:

- Debug access to application CPU shall be enabled during warm reset ;
- Debug access to SoC AHB-AP shall be enabled at end of boot (test mode entry is enabled and TCU can enable the AHB-AP during warm reset with a valid test password) ;
- Debug access to Debug Mailbox shall be always enabled ;
- Debug access to CoreSight registers shall be enabled during warm reset ;
- Debug access to NXP internal cores shall be enabled during warm reset ;
- Debug access to NXP security core shall be disabled; they can be enabled by NXP secure firmware.

11.4.3OEM Open/Return

The following debug functions shall be supported in these lifecycles:

- Debug access to application CPU shall be enabled during warm reset ;
- Debug access to SoC AHB-AP shall be enabled at end of boot (test mode entry is enabled and TCU can enable the AHB-AP during warm reset with a valid test password) ;
- Debug access to Debug Mailbox shall be always enabled ;
- Debug access to CoreSight registers shall be enabled during warm reset ;
- Debug access to NXP internal cores shall be disabled; they can be enabled by NXP authentication ;
- Debug access to NXP security core shall be disabled; they can be enabled by NXP secure firmware.

11.4.4OEM Secure World

The following debug functions shall be supported in this lifecycle:

- Debug access to application CPU shall be disabled; non-secure debug access shall be enabled at end of boot; full debug access can be enabled by OEM authentication ;
- Debug access to SoC AHB-AP shall be disabled; non-secure debug access shall be enabled at end of boot; full debug access can be enabled by OEM authentication ;
- Debug access to Debug Mailbox shall be always enabled ;

- Debug access to CoreSight registers shall be disabled; full debug access can be enabled by OEM authentication ;
- Debug access to NXP internal cores shall be disabled; they can be enabled by NXP authentication provided OEM secure debug is enabled ;
- Debug access to NXP security core shall be disabled; they can be enabled by NXP secure firmware provided OEM secure debug is enabled.

11.4.5 OEM Closed

The following debug functions shall be supported in this lifecycle:

- Debug access to application CPU shall be disabled; debug access can be enabled by OEM authentication ;
- Debug access to SoC AHB-AP shall be disabled; debug access can be enabled by OEM authentication ;
- Debug access to Debug Mailbox shall be always enabled ;
- Debug access to CoreSight registers shall be disabled; debug access can be enabled by authentication ;
- Debug access to NXP internal cores shall be disabled; they can be enabled by NXP authentication provided OEM secure debug is enabled ;
- Debug access to NXP security core shall be disabled; they can be enabled by NXP secure firmware provided OEM secure debug is enabled.

11.4.6 OEM Locked / BRICKED

The following debug functions shall be supported in this lifecycle:

- Debug access to application CPU shall be disabled ;
- Debug access to SoC AHB-AP shall be disabled ;
- Debug access to Debug Mailbox shall be always enabled ;
- Debug access to CoreSight registers shall be disabled ;
- Debug access to NXP internal cores shall be disabled ;
- Debug access to NXP security core shall be disabled.

11.5 APB Interconnect

The CoreSight APB Interconnect (APBIC) enables the debug port to access CoreSight component registers directly via an APB-AP, while also supporting on-device software to access the CoreSight component registers. The address decoding for the APBIC accessible components is described in the following table.

Table 233. [Address decoding i.MX RT2660 CoreSight APBIC components](#)

Destination	APBIC_TA_REG [23:16]	Size	Memory Mapped Address
Debug Access Port ROM (DAPROM)	00h	64kB	0x41F0_0000
CoreSight Trace Port Interface Unit (TPIU)	02h	64kB	0x41F2_0000
CoreSight Trace Funnel	06h	64kB	0x41F6_0000
CoreSight Timestamp (TS-GEN)	01h	64kB	0x41F1_0000
CoreSight Serial Wire Output (SWO)	03h	64kB	0x41F3_0000

Destination	APBIC_TA_REG [23:16]	Size	Memory Mapped Address
CoreSight Embedded Trace Router (ETR)	05h	64kB	0x41F5_0000
CoreSight Embedded Trace FIFO (ETF)	04h	64kB	0x41F4_0000
CoreSight Cross Trigger Interface 1 (CTI1)	08h	64kB	0x41F8_0000
CoreSight Cross Trigger Interface 0 (CTI0)	07h	64kB	0x41F7_0000

11.6 Debug Cross-triggers

Debug Embedded Cross Trigger (ECT) comprises a set of CoreSight Cross Trigger Interface (CTI) and Cross Trigger Matrix (CTM) components connected together. The main function of the ECT is to pass debug events from one core to another. For example, the ECT can communicate debug state information from one core to another, so that program execution on both cores can be stopped at the same time if required.

A block diagram of the trigger connections is shown below.

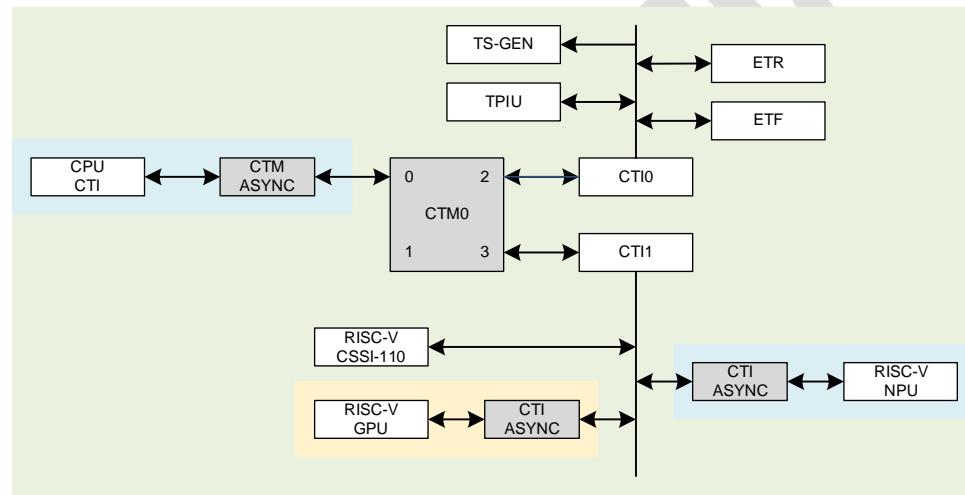


Fig 115. i.MX RT2660 Debug Embedded Cross Trigger (ECT) block diagram

Table 234. IC requirements traceability: Hardware test & debug requirements (part ii)

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_DEB_4-5	The trigger infrastructure which is used to propagate events across the system to allow for breakpoints, interrupts or other related behavior.	Must have	Yes

11.6.1 CTM connections

The Cross Trigger Matrix (CTM) shall be implemented with the following connections.

Table 235. i.MX RT2660 CTM connections

Port	Connection
0	CM85 CTI
1	<reserved>

Port	Connection
2	SoC CTI0 - CoreSight Components
3	SoC CTI1 – Auxiliary Cores

11.6.2 CPU CTI connections

The ARM CPU based Cross Trigger Interface (CTI) shall be implemented. The standard connections are described in the following table.

Table 236. i.MX RT2660 CM85 Cross Trigger Interface (CTI) connections

Input Description	Input Source	Index	Output Destination	Output Description
	CTITRIGIN	7	CTITRIGOUT	ETM Input 3
	CTITRIGIN	6	CTITRIGOUT	ETM Input 2
ETM Output 1	CTITRIGIN	5	CTITRIGOUT	ETM Input 1
ETM Output 0 or DWT Output 3	CTITRIGIN	4	CTITRIGOUT	ETM Input 0
DWT Output 2	CTITRIGIN	3	CTITRIGOUT	Interrupt Request 1
DWT Output 1	CTITRIGIN	2	CTITRIGOUT	Interrupt Request 0
DWT Output 0	CTITRIGIN	1	CTITRIGOUT	Processor Restart Request
Processor Halted	CTITRIGIN	0	CTITRIGOUT	Processor Halt Request

The CTI interrupt requests shall be connected to the NVIC of the CPU to facilitate self-hosted debug software that is executing on the CPU.

11.6.3 CTI0 connections

The Cross Trigger Interface (CTI0) shall be implemented at the SoC level to connect various CoreSight components to the CTM. The connections are described in the following table.

Table 237. i.MX RT2660 Cross Trigger Interface 0 (CTI0) connections

Input Description	Input Source	Index	Output Destination	Output Description
		7		
		6	TSGEN HLTDDBG	Halt Debug
		5	TPIU TRIGIN	Trigger Input
		4	TPIU FLUSHIN	Flush Request
Trace capture stopped	ETR ACQCM	3	ETR TRIGIN	Trigger Input
Trace buffer full	ETR FULL	2	ETR FLUSHIN	Flush Request
Trace capture stopped	ETF ACQCM	1	ETF TRIGIN	Trigger Input
Trace buffer full	ETF FULL	0	ETF FLUSHIN	Flush Request

11.6.4 CTI1 connections

The Cross Trigger Interface (CTI1) shall be implemented at the SoC level to connect various auxiliary cores to the CTM. The connections are described in the following table.

Table 238. i.MX RT2660 Cross Trigger Interface 1 (CTI1) connections

Input Description	Input Source	Index	Output Destination	Output Description
GPU Debug Event	ZEN-V EXT_TRIG_OUT[1]	7	ZEN-V EXT_TRIG_IN[1]	GPU Debug Event
GPU Debug Event	ZEN-V EXT_TRIG_OUT[0]	6	ZEN-V EXT_TRIG_IN[0]	GPU Debug Event
NPU Debug Event	ZEN-V EXT_TRIG_OUT[1]	5	ZEN-V EXT_TRIG_IN[1]	NPU Debug Event
NPU Debug Event	ZEN-V EXT_TRIG_OUT[0]	4	ZEN-V EXT_TRIG_IN[0]	NPU Debug Event
CSSI Debug Event	ZEN-V EXT_TRIG_OUT[1]	3	ZEN-V EXT_TRIG_IN[1]	CSSI Debug Event
CSSI Debug Event	ZEN-V EXT_TRIG_OUT[0]	2	ZEN-V EXT_TRIG_IN[0]	CSSI Debug Event
		1		
		0		

11.7 Trace overview

A block diagram for the system level trace components is shown below.

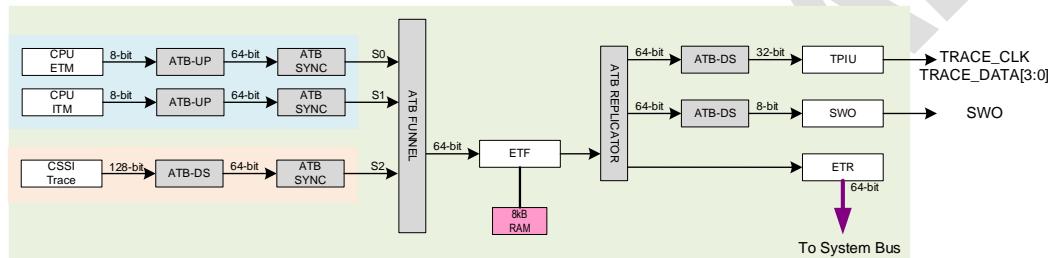


Fig 116. i.MX RT2660 Debug Trace infrastructure block diagram

Table 239. IC requirements traceability: Hardware test & debug requirements (part iii)

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_DEB_4-4	The trace infrastructure which is used to transfer trace information into on-chip RAM or external pSRAM via ETR or output trace data on TPIU trace port.	Must have	Yes

11.8 Timestamp generator (TS-GEN)

The timestamp implementation supports correlation between the trace data across different cores. The timestamp generator is a 64-bit counter that is distributed to the various cores via various synchronous or asynchronous bridges. The TS-GEN module implements control registers to enable/disable the timestamp.

A block diagram for the system level timestamp components is shown below.

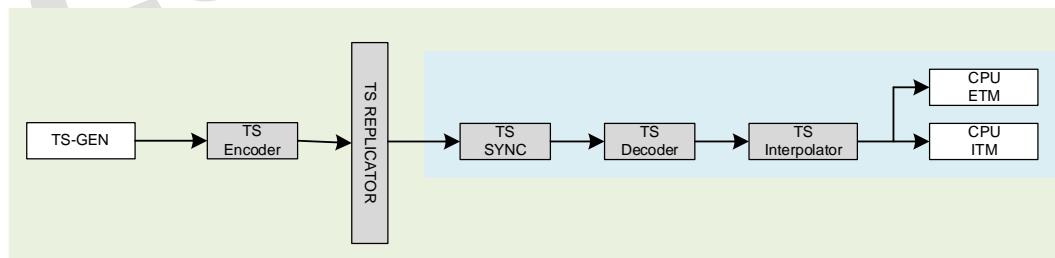


Fig 117. i.MX RT2660 Debug Timestamp Generator (TS-GEN) block diagram

TODO: RISC-V core has similar time stamp input, namely *timebase*, so the time stamp need to send to CSSI RISC-V core.

11.9 Low Power Debug

11.9.1 Clock Gating

The DBGPWRUPREQ shall be synchronized to the system clock domain and used to generate the acknowledge DBGPWRUPACK back to the SWJ-DP.

All debug and trace components shall be clock gated such that the clocks are only enabled if one of the following is true:

- DBGPWRUPACK is asserted (indicating a debugger is connected) ;
- Any application CPU has asserted output TRCENA (indicating the CPU has enabled on-chip trace) ;
- A memory mapped register (eg: MODCON) can provide an override to also enable the debug/trace clock.

The DBGQACTIVE (or similar) output from the application CPU may be an appropriate substitute for this.

11.9.2 Low Power Modes

A SLEEPCON register bit will control if an attached debugger keeps the device active or if the device should enter a low power mode even with an attached debugger. If a device enters a low power mode when a debugger is attached, then the DBGPWRUPACK will be forced low as part of the low power mode entry and the device will fully enter the low power mode with the debug/trace logic clock gated. If an attached debugger is keeping the device active, then the lowest power mode that can be entered is essentially Sleep mode (eg: WFI or WFE).

11.10 Secure Debug

*For more detailed information on the RT2660 SoC security,
please refer to the i.MX RT2660 Security HW.AS document [11]*

The CSSI ensure that multiple Execution environments may be debugged at the same time.

A Execution environment Debug Card provides the credentials to authenticate for a EENV debug session. This card may be presented through the external JTAG interface or remotely via e.g. wireless communications link. The vendor uses this debug card when requesting a debug session of a EENV. If a vendor happens to be in possession of multiple debug cards then multiple EENV can be enabled for debug within a debug session. The secure enclave honors the debug cards which maps EENV "Elements" to system resources including cores, security levels and debug domain IDs.

The secure enclave (e.g. CSSI, HSE, Sentinel) is the security subsystem that for debug purposes provides access control to the SoC debug features. It authorizes requests to debug according to SoC lifecycle, fuses, and authentication.

11.10.1 Blank to FAB Life Cycle

When the chip is in a pristine wafer state it is configured in the Blank lifecycle state. The product team uses the blank-to-fab control bit to burn the lifecycle state fuse to transition to the Fab lifecycle state. The control bit activates a state machine that performs the fuse burning sequence. Without this fuse burned then the cores will not run. Control for this is in the JTACG. Status to determine if in the blank, fab, or bricked lifecycles is in the JTACG as well.

11.10.2 Debug Authorization Process

Debug Authorization indicates that debug is allowed. Depending on the state of the device, authentication may or may not be required to gain permission to debug a cohort. Once debug is authorized then first, if needed, CSSI ensures residual secrets are erased and then second, configures the various debug components and resource/region domain controllers for identity assignment and access rights.

Once debug access is granted it remains granted until the next power cycle of the SoC. While any debug access is granted, this is considered a debug session.

11.10.3 Debug Access Based on Lifecycle

CSSI uses the SoC lifecycle state to help determine access rights to the debug features. The following table shows the possible access controls for each debug system throughout the SoC life cycle phases.

State	CSSI subsystem	Rest of SoC debug
Blank	Not available	Not available
Fab	CSSI authentication	Authorized
Provision	CSSI authentication	Authorized
OEM (Trustzone)	CSSI authentication	Authorized
OEM2	CSSI authentication*	Cohort authentication
In Field (also Pre-FA)	CSSI authentication*	Cohort authentication
Locked	Not available	Not available
Bricked	Not available	Not available
Field Return OEM	CSSI authentication	Authorized
Field Return NXP	CSSI authentication	Authorized

Fig 118. i.MX RT2660 debug access controls during the SoC lifecycles

Non-functioning states include the Blank and Bricked states. In Blank, manufacturing progresses the lifecycle state to Fab for enablement of the CSSI and other cores. Brick is an end-of-life cycle where the chip is made permanently inoperable.

When the Lifecycle is in one of the “Open” state then for all subsystems except for the CSSI, no authentication verification step is needed to allow access to the debug infrastructure, meaning debug is automatically authorized. The CSSI itself always requires NXP-signed authentication in all operable states. When the lifecycle is in the OEM Closed state then the debug user, using a Debug Card, must successfully perform one or more EENV authentication sequences with the CSSI to be granted access to the debug infrastructure. EENV debug access is limited to the debug domains and cohort identities for which the Cohort Debug Card and CSSI allow. The Locked Lifecycle state prohibits all debug.

Note in the OEM Closed lifecycle state that CSSI authentication requires

- Not available: Debug is not possible in this state (not even via a challenge/response handshake) ;
- Authorized: Debug is automatically authorized (open) for all subsystems except the CSSI ;
- Cohort authentication: To debug a EENV, a debug card authentication sequence is required ;
- CSSI authentication: NXP signed debug card required.

The i.MX RT2660 shall support for two Debug domains: 1) CSSI 110, and 2) Rest of System. Hence, two debug enables shall be supported. All debug enablement for rest of system should be controlled through debug Enables /SPIDEN/SPNIDEN provided on CSSI boundary.

The i.MX RT2660 Debug Authentication should be retained across different power modes.

Table 240. **IC requirements traceability: Secure debug requirements**

AS/RS identifier	Contents	Classification	Covered
iMXRT2660_DEB_5-1	Hardware test & debug	Heading	-
iMXRT2660_DEB_5-4	The processor shall implement following JTAG security modes: - Mode 1: no debug. All JTAG features disabled. - Mode 2: Secure JTAG. JTAG access is limited by using challenge/response based authentication mechanism - Mode 3: JTAG enabled. All JTAG features are enabled.	Must have	To be confirmed during design phase
iMXRT2660_DEB_5-6	This processor must have the ability to reset the SoC and gain control via JTAG at the reset vector through JTAG. This will enable boot debugging.	Must have	To be confirmed during design phase
iMXRT2660_DEB_6-1	Secure debug	Heading	-
iMXRT2660_DEB_6-2	The debug infrastructure must read the debug enable signal before beginning or allowing debug operations.	Must have	Yes, targeted via CSSI
iMXRT2660_DEB_6-3	In certain circumstances of the life cycle, security privilege may be invoked or revoked which will change the visibility of the debug infrastructure and what it can see or not see during its operations. The debug infrastructure must read the security privilege levels enabled for that portion of the life cycle before proceeding	Must have	Yes, Fig 118
iMXRT2660_DEB_6-4	The debug infrastructure must honor a signal which enables or disables tracing.	Must have	Yes, targeted via CSSI
iMXRT2660_DEB_6-6	The debug infrastructure must honor a signal which enables or disables secure mode tracing.	Must have	Yes, targeted via CSSI
iMXRT2660_DEB_6-7	The debug infrastructure must generate a signal anytime the JTAG block is active. Examples of this would be if it is performing any activity or that is it coming out of reset which can be read by the security unit.	Must have	To be confirmed during design phase
iMXRT2660_DEB_6-8	The debug logic shall support full shut off for production devices. An example of how to do this would be having power go to a debug power ball which is grounded for production on the PCB.	Must have	To be confirmed during design phase
iMXRT2660_DEB_7-1	Debug observability	Heading	-
iMXRT2660_DEB_7-2	Debug observability signals at IP level or SoC level shall be multiplexed out on IO pads for debug purpose	Must have	To be confirmed during design phase

12. Physical Implementation Requirements

12.1 PMC_SS macro

The i.MX RT2660 PMC_SS macro block shall be designed by the WCS analog team and SoC design team. The details of the PMC_SS memory map, digital interfacing and digital partitioning within the PMC_SS macro shall be converged during the design phase.

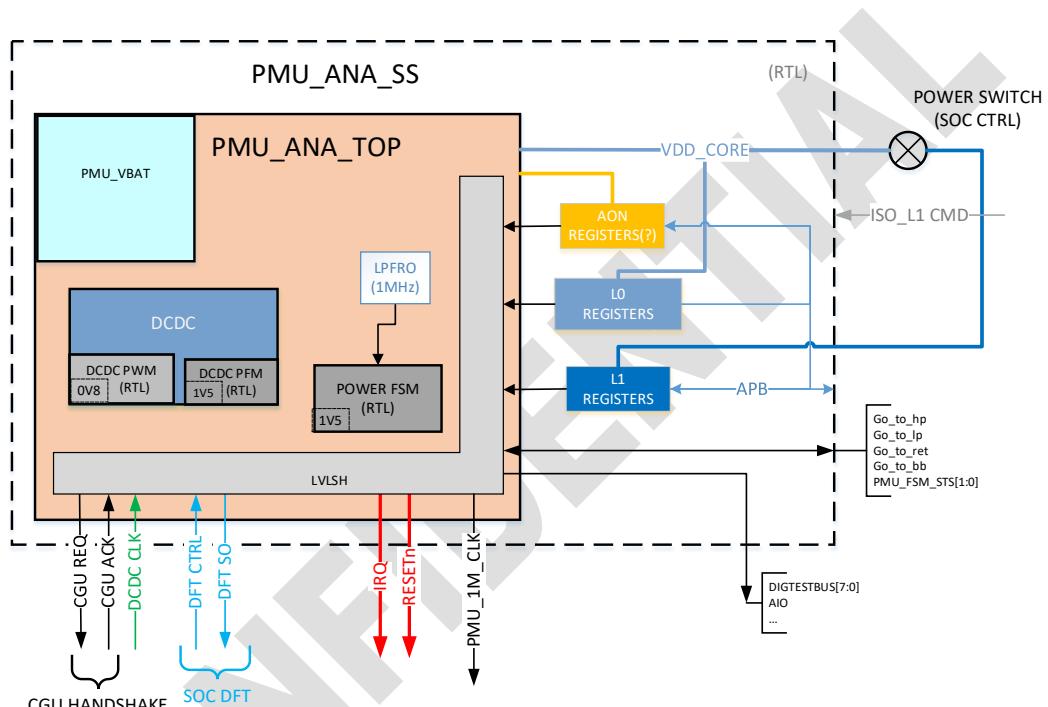


Fig 119. i.MX RT2660 PMC_SS macro block

12.2 CGU_SS macro

A CGU_SS macro block shall be designed by WCS analog team and SoC design team. The details of the analog and digital partitioning within the CGU_SS macro shall be converged during design phase.

The CGU_SS macro block shall be implemented as a hard macro block, preferably a single hard macro block that includes CGU_SS analog and digital functions. Please refer to the description of the i.MX RT2660 clock strategy and clock architecture to Section 6.1.2 and Section 7.1, respectively.

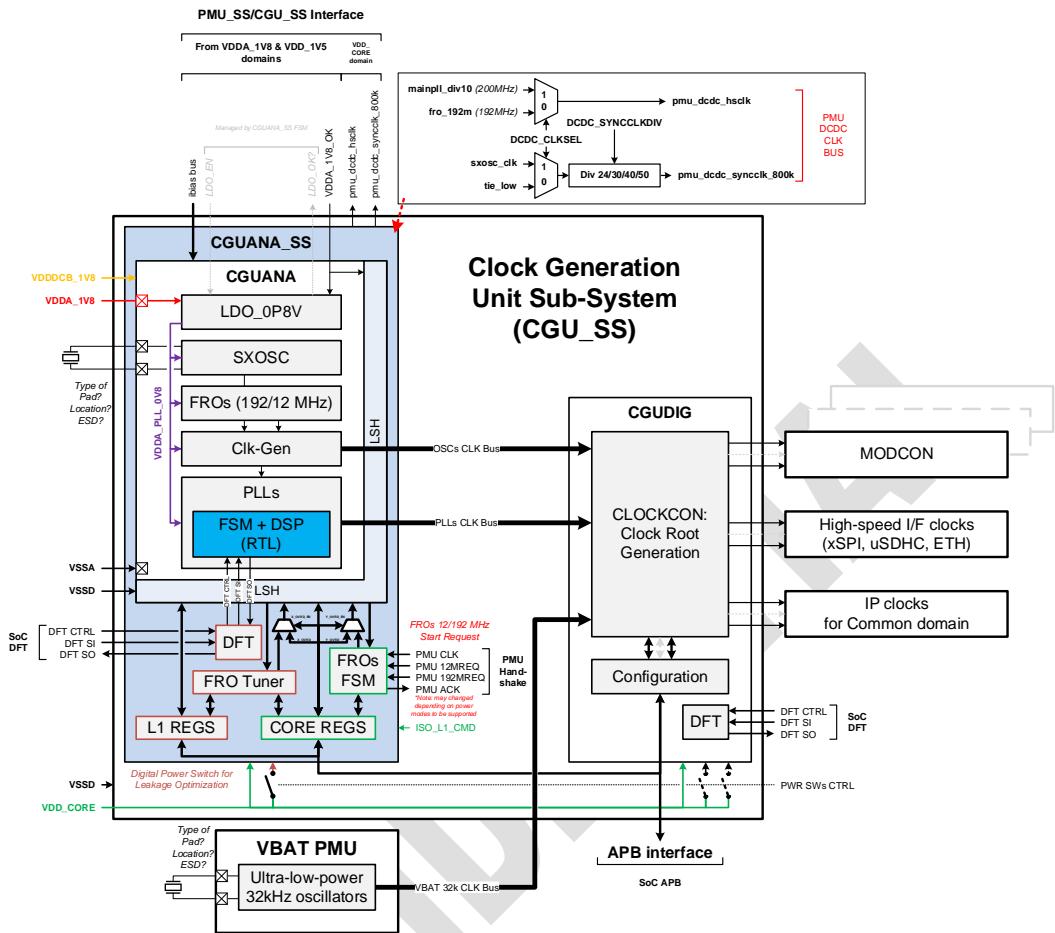


Fig 120. i.MX RT2660 CGU_SS macro block

13. Application Information

Application diagram is to be added here.

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14. Use-Case Information

The Chapter provides a high-level overview of the main application use-cases for the i.MX RT2660 SoC that have been outlined in the i.MX RT2660 Requirement Specification document [2].

14.1 Use-Case 1: Building Control

14.1.1UC1A: High Pin count Scenario

Building automation networks and room controllers enable the adoption of new technologies to achieve sustainability, health, and productivity goals in modern intelligent buildings. The diagram below shows RT2660 as the main application MCU in a building control system.

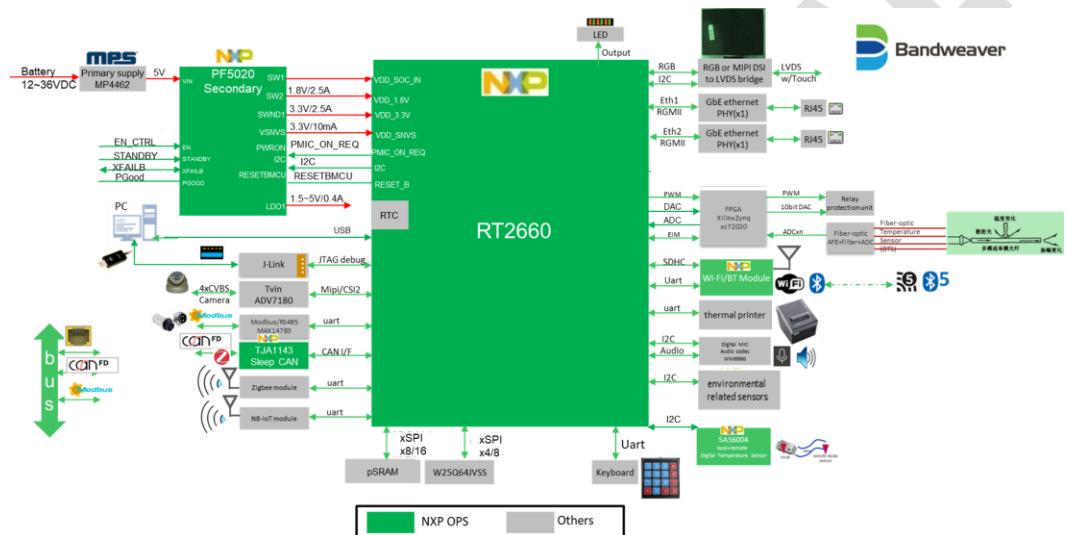


Fig 121. Use-Case 1A: RT2660 in Building Control application

One use-case scenario has been identified concerning face recognition. Fig 122 shows the data traffic related to the Auto Smart Surface application.

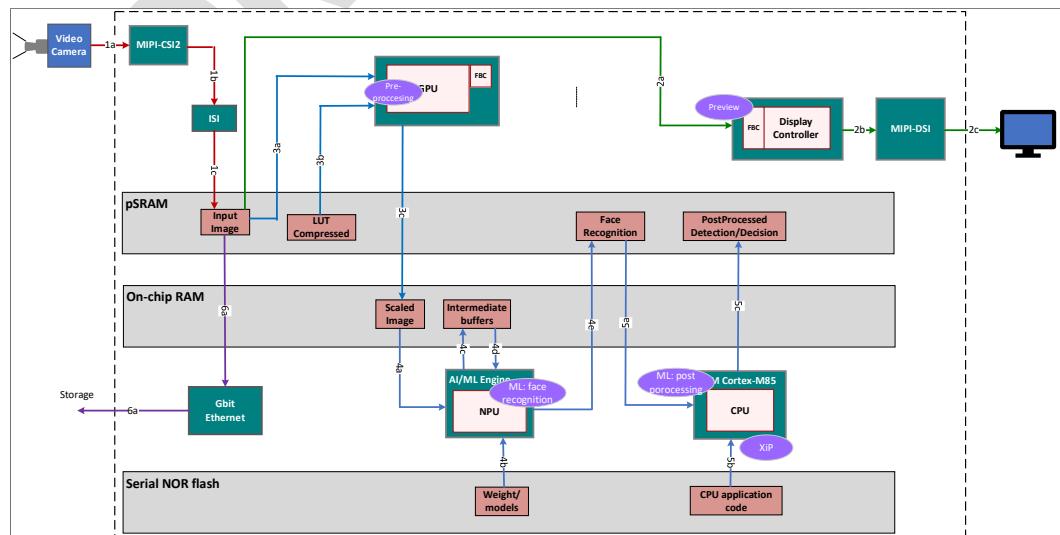


Fig 122. Use-Case 1A: Data traffic in Building Control application

The performance requirement of this Face Recognition use-case has been elaborated below.

Face Recognition - High end product with NOR flash

1. MIPI CSI/ISI writes camera input data to pSRAM.
 - MIPI CSI routes input video data to ISI
 - ISI writes video image data to pSRAM
 - The video resolution is up to 720p at 30fps in YUV422 (16-bit) format.
2. Display controller shows preview of the video image on the display panel.
 - DCIF reads image frame from pSRAM and displays on LCD panel for preview.
 - The reads image resolution of 720p at 30fps in YUV422 (16-bit) format.
 - DCIF converts the image to 24-bit RGB for preview.
3. GPU performs pre-processing on input video image and writes scaled images to pSRAM.
 - GPU reads input video frame from pSRAM, frame size is 720p
 - GPU performs pre-processing on the captured video image and produces scaled image of 320x320 for ML processing
 - GPU writes the scaled images to on-chip RAM
4. NPU performs face recognition ML processing.
 - NPU reads 320x320 images from SRAM
 - NPU reads weight and models stored on serial NOR flash
 - On-chip RAM is used as intermediate buffers to temporarily stored weight of early rounds and intermediate data.
 - NPU writes output data to pSRAM
5. CPU performs ML post-processing for detection and decision.
 - CPU XiP from NOR flash while performing ML post processing.
6. Ethernet sends recording video to storage.

Total pSRAM memory bandwidth requirement:

- Stream 1: ISI writes to pSRAM: 69.7MBps
- Stream 2: DCIF reads from pSRAM: 55.3MBps
- Stream 3: GPU Reads video frame from pSRAM: 55.3MBps
- Stream 4: GPU Writes scaled image to pSRAM: 6.144MBps
- Stream 5: NPU reads scaled image from pSRAM: 6.144MBps
- Stream 6: NPU writes output data to pSRAM: 6.144MBps
- Stream 7: CPU reads from pSRAM on ML detection post-processing: 65.6MBps
- Stream 8: CPU writes to pSRAM on ML detection post-processing: 74.4MBps
- Stream 9: ETH reads video image from pSRAM for storage: 55.3MBps
- Total memory bandwidth: **382MBps**

The use-case is rated as a SHOULD-HAVE use-case. Please refer to i.MX RT2660 System.RS for more information about this use-case [2]. **TODo: to verify memory bandwidth 382MBps, Multiple comments in AS v0.8, not resolved in AS v0.9 yet.**

- Why NPU write bandwidth is 6.144Mbps(stream6), but CPU read bandwidth is 65.6Mbps(stream7)
- For stream8, if CPU write the post-processing to pSRAM, Is there one master to read and use this data? if we don't need use this data, why we need to write them to pSRAM?
- Not match RS_V0.75 target 375.6MB/s

14.1.2UC1B: Medium Pin count Scenario

Building automation networks and room controllers enable the adoption of new technologies to achieve sustainability, health, and productivity goals in modern intelligent buildings. The diagram below shows RT2660 as the main application MCU in a building control system.

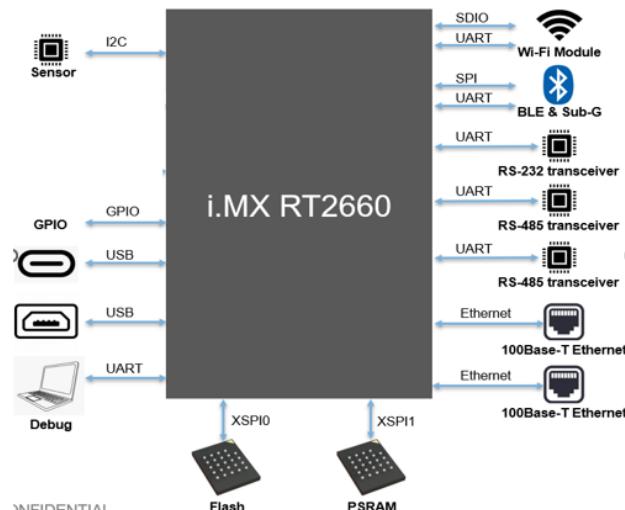


Fig 123. Use-Case 1B: RT2660 in Building Control application

The use-case is rated as a MUST-HAVE use-case. Please refer to i.MX RT2660 System.RS for more information about this use-case [2].

14.2 Use-Case 2: Smart Home

Smart thermostats are advanced temperature control devices that allow users to manage their home's heating and cooling remotely using their smartphone or computer. They use advanced algorithms and machine learning to learn users' temperature preferences and adjust the temperature settings accordingly. They can also learn users' daily routines and automatically adjust the temperature when they away from home to save energy.

The diagram below shows RT2660 in a embedded MCU design for entry-level smart thermostat.

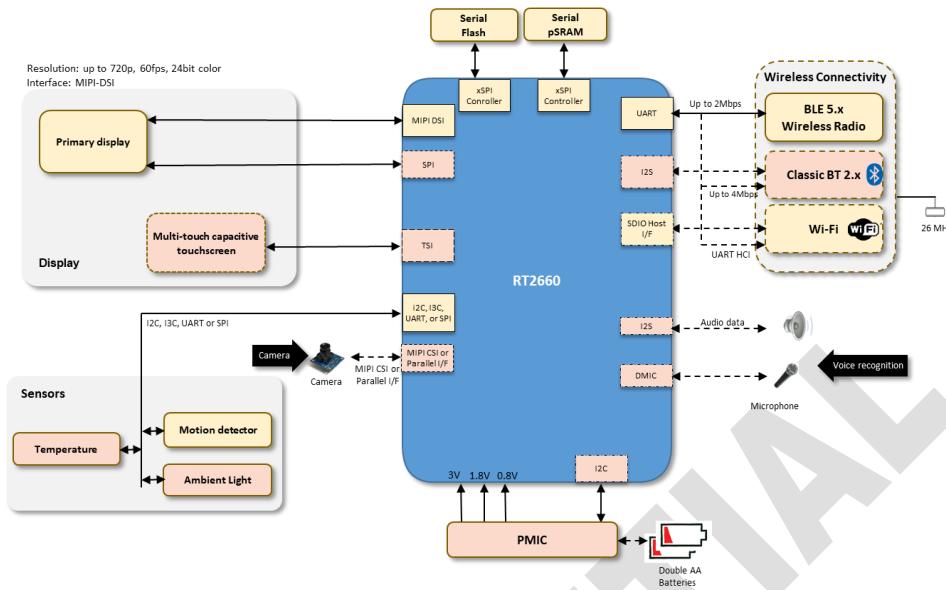


Fig 124. Use-Case 2: RT2660 in Smart Home application

The use-case is rated as a MUST-HAVE use-case. Please refer to i.MX RT2660 System.RS for more information about this use-case [2].

14.3 Use-Case 3: Backlight Control

This processor is used to control multiple backlight controllers on LED TV.

The figure below shows the IO interface requirements for this application.

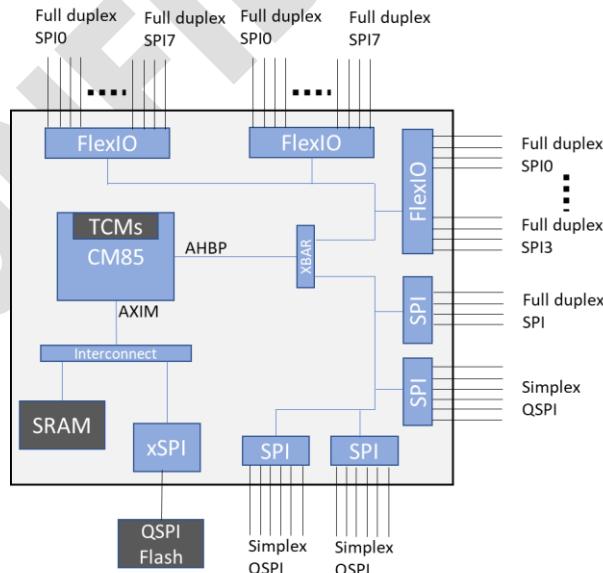


Fig 125. Use-Case 3: RT2660 in LED TV Backlight Control application

The use-case is rated as a MUST-HAVE use-case. Please refer to i.MX RT2660 System.RS for more information about this use-case [2].

14.4 Use-Case 4: Camera Stabilizer

This processor is used for camera stabilization e.g. drones.

The figure below shows the IO interface requirements for this application.

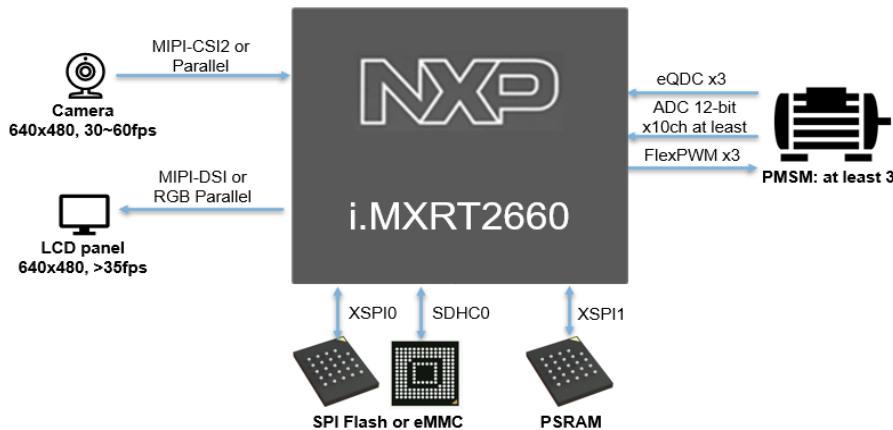


Fig 126. Use-Case 4: RT2660 in Camera Stabilizer application

The use-case is rated as a MUST-HAVE use-case. Please refer to i.MX RT2660 System.RS for more information about this use-case [2].

14.5 Use-Case 5: Smart Door Lock

Home security is an increasing concern as crime rates continue to rise around the world. The smart lock market is projected to grow to over 2.7 billion by 2023 across various applications including residential, commercial and industrial. NXP has developed a broad portfolio of scalable security solutions that provide a foundation for achieving the most effective security levels based on the potential security attacks on a system.

The diagram below shows RT2660 in a embedded MCU design for entry-level door smart lock.

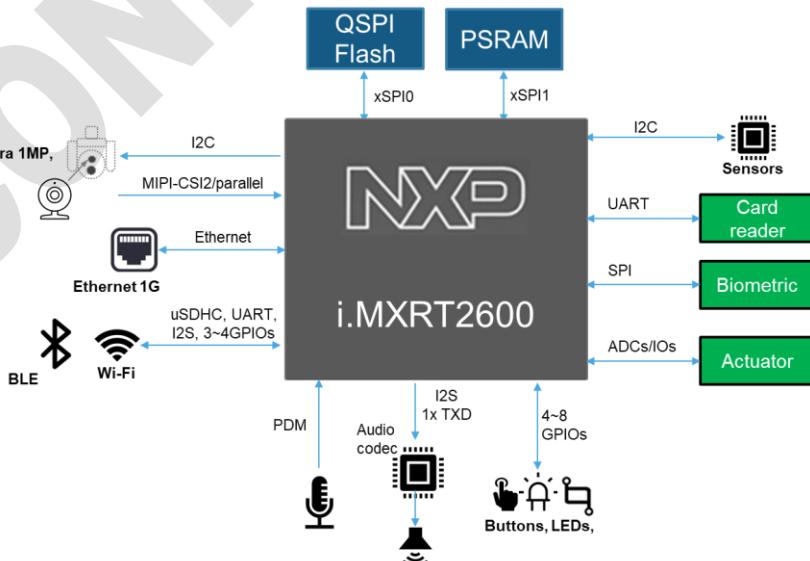


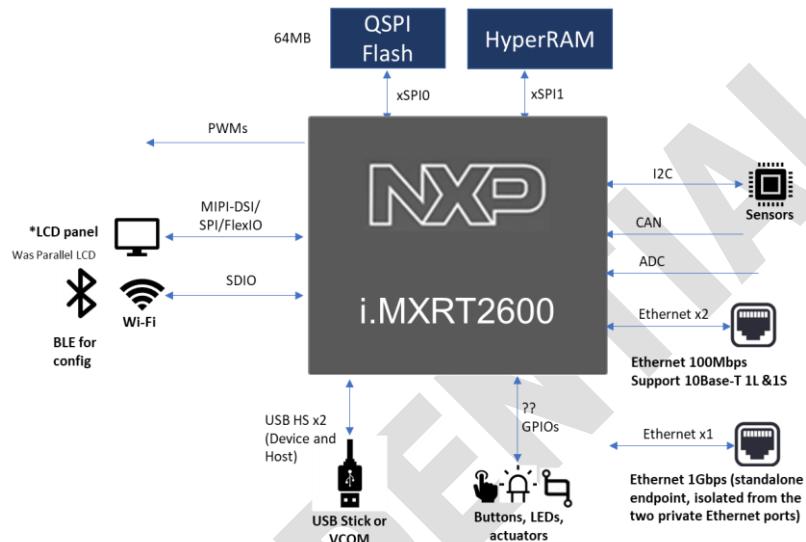
Fig 127. Use-Case 5: RT2660 in Smart Door Lock application

The use-case is rated as a MUST-HAVE use-case. Please refer to i.MX RT2660 System.RS for more information about this use-case [2].

14.6 Use-Case 6: Data Center Management

This processor is used for data center management applications.

The figure below shows the IO interface requirements for this application.

**Fig 128. Use-Case 6: RT2660 in Data Center Management application**

The use-case is rated as a MUST-HAVE use-case. Please refer to i.MX RT2660 System.RS for more information about this use-case [2].

14.7 Use-Case 7: Quad Motor Control

This processor is used in a brushed motor control application which has 4 motors. The figure below shows the IO interface requirements for this application.

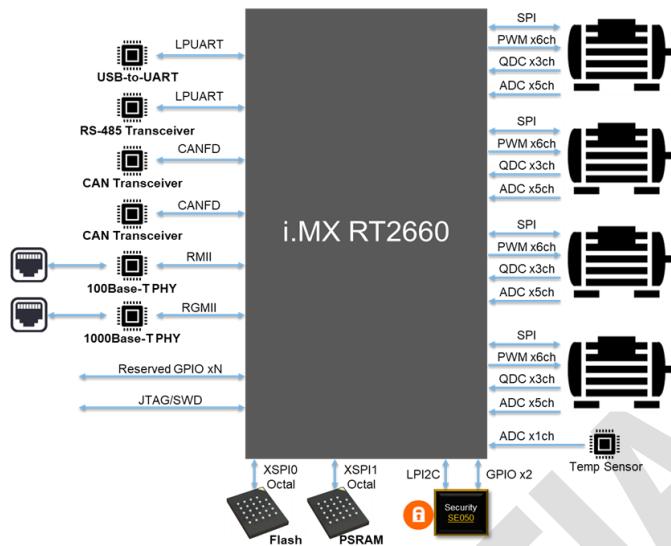


Fig 129. Use-Case 7: RT2660 in Quad Motor Control application

The use-case is rated as a MUST-HAVE use-case. Please refer to i.MX RT2660 System.RS for more information about this use-case [2].

14.8 Use-Case 8: Tactical Radio

This MCU is used as the main processor of a low-end 2-way radio. The figure below shows the IO interface requirements for this application.

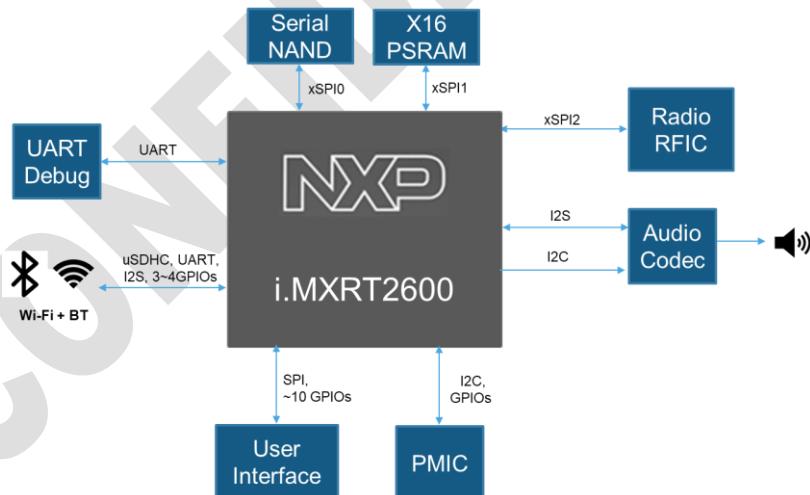


Fig 130. Use-Case 8: RT2660 in Tactical Radio application

The use-case is rated as a MUST-HAVE use-case. Please refer to i.MX RT2660 System.RS for more information about this use-case [2].

14.9 Use-Case 9: Automotive Smart Surface

This device targets multiple automotive smart surface use cases.

- Smart Panel (Armrest panel, Air-condition control screen, Touch panel and smart button)

- Smart button
- Gateway (Lixiang project)
- Co-processor (Joynext)

The figure below shows the IO interface requirements for this application.

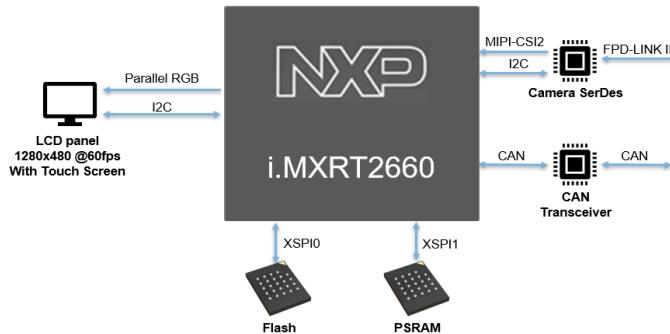


Fig 131. Use-Case 9: RT2660 in Automotive Smart Surface application

Fig 132 shows the data traffic related to the Auto Smart Surface application.

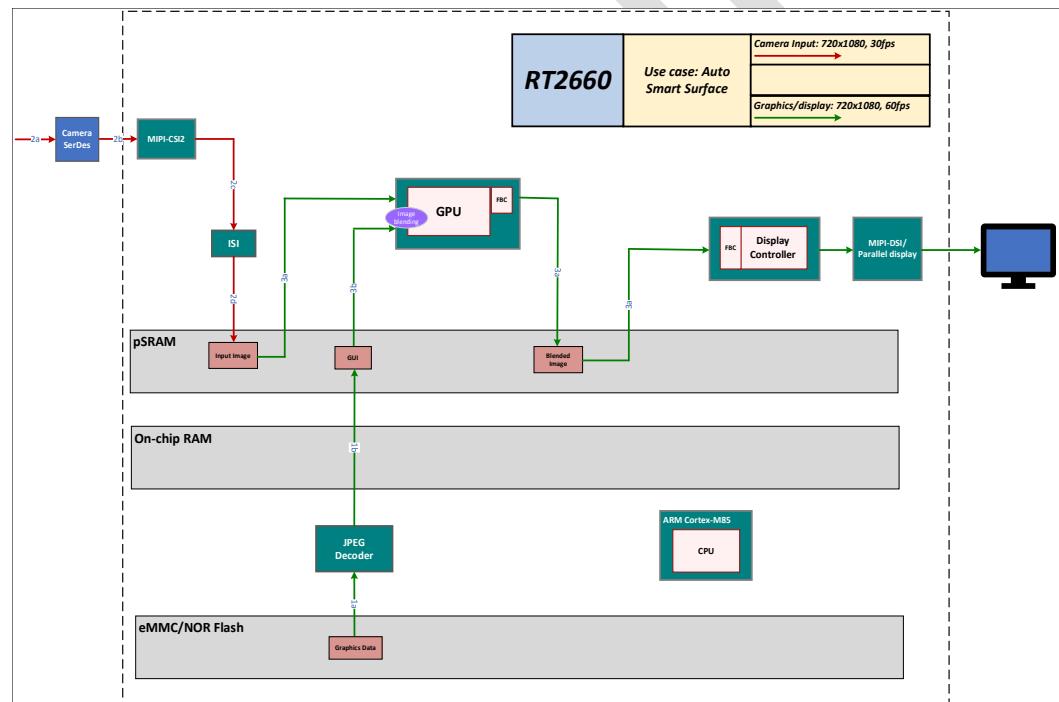


Fig 132. Use-Case 9: Data traffic in Automotive Smart Surface application

Two main Smart Panel usage scenarios have been identified, each with their own performance requirements. The use-case scenarios have been elaborated below.

Smart Panel usage scenario 1 - High end product with NOR flash

1. MIPI CSI/ISI writes video input data to pSRAM.

- Input video from infotainment system through MIPI CSI. Input video resolution and frame rate (TBD).

- MIPI CSI routes input video data to ISI.
 - ISI performs image preprocessing and writes video image data to pSRAM.
 - The video resolution is 1280 x640 @10fps in RGB888 format.
 - This video image is input stream 1 to the GPU.
2. JPEG Decoder compressed images from NOR flash
- JPEG Decoder loads compressed images from serial NOR flash
 - JPEG Decoder decode the images and writes output data to pSRAM memory with resolution 1280x640 @10fps.
 - This is the input stream 2 to the GPU.
3. GPU performs image blending
- GPU reads two input streams from pSRAM at the rate of 1280x640 @30fps.
 - GPU performs image blending and output image resolution of 1280x640 @60fps in RGB888. – **60fps is not applicable, two input streams of GPU refer to S1 and S2 channels. If they are 30fps, the output image should also 30fps. Why it changes to 60fps here?**
 - GPU compresses the blended image with 2.4:1 compression ratio.
 - GPU writes the compressed image to pSRAM.
4. Display
- DCIF reads the compressed image from pSRAM
 - DCIF decompressed the image and send it to the MIPI DSI.
 - The MIPI DSI driver sends the display image to the display panel.
 - The display resolution is 1280x640 @ 60fps in RGB888.

Total pSRAM memory bandwidth requirement:

- Stream 1: ISI writes to pSRAM: 73.728MBps
- Stream 2: JPEG Decoder writes to pSRAM: 24.576MBps
- Stream 3: GPU Reads first input stream 73.728MBps
- Stream 4: GPU reads second input stream 73.728MBps
- Stream 5: GPU writes compressed output image to pSRAM 61.44MBps
- Stream 6: DCIF reads compressed image from pSRAM 61.44MBps
- Total memory bandwidth: **368.64MBps**

Smart Panel usage scenario 2 – Mid end product with NOR flash

1. MIPI CSI/ISI writes video input data to pSRAM.
- Input video from infotainment system through MIPI CSI. Input video resolution and frame rate (TBD).
 - MIPI CSI routes input video data to ISI.
 - ISI performs image preprocessing and writes video image data to pSRAM.
 - The video resolution is 800 x480 @10fps (TBC) in RGB888 format.
 - This video image is input stream 1 to the GPU.
2. JPEG Decoder compressed images from NOR flash
- JPEG Decoder loads compressed images from serial NOR flash
 - JPEG Decoder decode the images and writes output data to pSRAM memory with resolution 800x480 @10fps.
 - This is the input stream 2 to the GPU.
3. GPU performs image blending
- GPU reads two input streams from pSRAM at the rate of 800x480 @30fps.
 - GPU performs image blending and output image resolution of 800x480 @60fps in RGB888.
 - GPU compresses the blended image with 2.4:1 compression ratio.
 - GPU writes the compressed image to pSRAM

4. Display

- - DCIF reads the compressed image from pSRAM
- - DCIF decompressed the image and send it to the MIPI DSI.
- - The MIPI DSI driver sends the display image to the display panel.
- - The display resolution is 800x480 @ 60fps in RGB888.

Total pSRAM memory bandwidth:

- Stream 1: ISI writes to pSRAM: 34.56MBps
- Stream 2: JPEG Decoder writes to pSRAM: 11.52MBps
- Stream 3: GPU Reads first input stream 34.56MBps
- Stream 4: GPU reads second input stream 34.56MBps
- Stream 5: GPU writes compressed output image to pSRAM 28.8MBps
- Stream 6: DCIF reads compressed image from pSRAM 28.8MBps
- Total memory bandwidth: **172.8MBps**

The use-case is rated as a MUST-HAVE use-case. Please refer to i.MX RT2660 System.RS for more information about this use-case [2].

15. IP Re-Use Overview

Table 241. RT2660 IP Re-Use Overview

IP block	PDM name	PDM version	Maturity	Comments
Cores and masters				
ARM Cortex-M85	C_IP_CM85 MCU_BASE	1.1 or newer	New	Re-use ARM Cortex-M85 processor and design new sub-system to i.MX RT2660 requirements
	C_IP_CM85 FPU_BASE	1.1 or newer		
Neutron-256S	D_IP_NEUTRON_NPU_SYN	1.27 or newer	Update	Sourcing product: i.MX943 Update on DFT related enhancements
eDMAv5	D_IP_SPP_DMA5_SYN	1.17 or newer	Re-use	Sourcing product: i.MX943
eDMAv3	D_IP_SPP_DMA3_SYN	1.17 or newer	Re-use	Sourcing product: i.MX700
Bus fabrics & infrastructure				
AXI Bus Matrix - NIC400		Latest version	New	ARM® CoreLink™ QoS-400 Network Interconnect Advanced Quality of Service Several dedicated NIC components for various sub-systems according to i.MX RT2660 structure
AHB Bus Matrix - AXBS	D_IP_AXBS_SYN	1.11 or newer	Re-use	Several dedicated AXBS components for various sub-systems according to i.MX RT2660 structure
XHB-400		Latest version	Re-use	ARM® CoreLink™ AXI4 to AHB-Lite XHB-400 Bridge
Peripheral Bridge	D_IP_AHB_PBRIDGE3_SYN	Latest version	Re-use	Sourcing product: Nirvana
IP Synchronizer	ipv_ipsync	001 or newer	Re-use	Sourcing product: RT500 (?)
Coresight Debug Integration	d_ip_dbg_trace_rt700_syn	1.15 or newer	Re-use	Sourcing product: RT700
Debug mailbox	D_IP_DEBUG_MAILBOX_SYN	1.8 or newer	Re-use	Sourcing product: Nirvana
Message Unit	D_IP_MU_SYN	1.47 or newer	Re-use	Sourcing product: RT700
Trigger XBAR	D_IP_XBAR_SW_DSC_SYN	1.13 or newer	Re-use	Sourcing product: RT1180
Event Generator	D_IP_EVTG_SYN	1.7 or newer	Re-use	Sourcing product: MCXA1
CRC	D_IP_CRC_16_32_PROG_SYN	1.15 or newer	Re-use	Sourcing product: RT1180
Memory infrastructure & -interfaces				
ROM controller with patch capability	D_IP_ROMCP_SYN	1.17 or newer	Re-use	Sourcing product: RT700
SRAM controller (AXI-based)	D_IP_ACP_AXI_SRAM_CTL	1.32 or newer	Re-use	Sourcing product: i.MX 943
SRAM controller (AHB-based)	D_IP_ACP_PRAM_E2E_ECC_SYN		Re-use	
SRAMC for external devices	D_IP_AHB_SRAMC_SYN	1.6 (no ips interface)	Re-use	Sourcing product: i.MX RT1180

IP block	PDM name	PDM version	Maturity	Comments
xSPI	D_IP_XSPI_SYN	1.14.1.6 or newer	Update	Improved XSPI design from XSPI design used in K5. Several CRs – refer to section 6.3.2 TKT0633648, TKT0633650, TKT0633651, TKT0633653, TKT0633665, TKT0633666, TKT0633667, TKT0633668, TKT0633670, TKT0633671, TKT0633999
	_delay_chain_hm		New	Hardening of delay chain in 22FDX+
IPED (PRINCE)	D_IP_PRINCECTR_RT7_SYN		Re-use	Sourcing product: RT700
XEX (PRINCE)	D_IP_PRINCEXEX_RT7_SYN		Re-use	Sourcing product: RT700
Security components				
Sentinel 110			New	New design by Security team
TRDC	D_IP_TRDC_SYN	Latest version	Update	Several CRs – refer to Section 9.7.7 Change requests concern TRDC_MNGR, TRDC_DAC, TRDC_MBC, TRDC_MRC
OTP FBX2IPS Bridge			New	Local IP for RT2660
OTP wrapper			New	
OTP controller			New	Synopsys OTP controller, associated to Synopsys 22FDX+ OTP memory
OTP 1Kx42 array			New	Synopsys OTP memory
Analog peripherals				
ADC	ADC analog		New	New design by MSIP team
	ADC digital wrapper	Latest version	Re-use	Sourcing product: TBD
DAC	DAC analog		New	New design by MSIP team
	DAC digital wrapper	Latest version	Re-use	Sourcing product: TBD
ACMP	ACMP analog		New	New design by MSIP team
	ACMP digital wrapper	Latest version	Re-use	Sourcing product: TBD
Communication peripherals				
USB HS controller	d_ip_usb2_hs_otg_syn	1.12 or newer	Update	Sourcing product: RT700 CR for USB Crystalless FS: TKT0636965
USB HS PHY	DA_IP_HS_USB2_PHY_GF22FDX	1.2	New	New 22FDX+ design by MSIP team Update 19.2-40MHz input clock range, 24MHz typ
USB FS	DA_IP_FS_USB11_PHY_GF22FDX	1.1	Re-use	Sourcing product: MCX A
USB FS PHY	A_IP_FS_USB11_PHY_GF22FDX	1.1	New	New 22FDX+ design by MSIP team
USDHC	DA_IP_USDHC_WRAP_GF22FDX	1.1 or newer	Update	Sourcing product: i.MX93
	ipv_usdhc	1.64 or newer	Re-use	Sourcing product: i.MX93 Change request: TKT0645633 – TBD LVS feature is really needed?
	DA_IP_USDHC_DELAY_CHAIN_H_M_GF22FDX	1.11 or newer	New	Hardening of delay chain in 22FDX+

IP block	PDM name	PDM version	Maturity	Comments
SAI	D_IP_SAI_SYN	1.41 or newer	Re-use	Sourcing product: RT700
SPDIF	d_ip_audio_xcvr_syn Module: d_ip_spdif_xcvr_syn	Latest version	Re-use	Re-use IP from i.MX RT1180 need update BG & IG
MQS	ipv_mqs	1.10 or newer	Re-use	Sourcing product: i.MX93 need update BG & IG
ASRC	ipv_asrc	1.7 or newer	Re-use	Sourcing product: i.MX RT1170 need update BG & IG
LPUART	D_IP_LPUART_SYN	1.46 or newer	Re-use	Sourcing product: RT1180
LPSPI	D_IP_LPSPi_SYN	1.29 or newer	Re-use	Sourcing product: RT1180
LPI2C	D_IP_LPI2C_SYN	1.31 or newer	Re-use	Sourcing product: RT1180
I3C	D_IP_MIPI_I3C_SYN	1.4.1.33 or newer	Re-use	Sourcing product: Nirvana
FlexCAN	ipv_flexcan3_syn	1.11.2.1 or newer	Re-use	Sourcing product: RT1170
Xeno Digital Phy	ivn_dig_10bt1sdigphy	1.3 or newer	Re-use	From BL AA, PL IVN
Ethernet 1Gb TSN	D_IP_3P_DWC_ENET_QOS	1.12.1.9 or newer	Re-use	From IMX8DXL
Ethernet 1Gb AVB	D_IP_ENET_MACAXI_1G_SYN	1.33 or newer	Update	TKT0628517 (confirm SW workaround) DFT related fixes: TKT0563453, TKT0563454, and TKT0563455
xSPI Responder	D_IP_XSPI_SLV_SYN	1.17 or newer	Re-use	Sourcing product: RT1180
SINC filter	IP_SINC_FILTER_SYN	1.13.2.14 or newer	Re-use	Sourcing product: RT1180
HMI				
FLEXIO	D_IP_FLEXIO_SYN	1.45 or newer	Re-use	Sourcing product: RT700
Digital Microphone	D_IP_MICFIL_SYN	1.43 or newer	Re-use	Sourcing product: RT700 TKT0630956, need update BG & IG
GPIO	D_IP_RGPIO_SYN	1.12 or newer	Re-use	Sourcing product: i.MX95
IOMUXC				-
IOMUX				-
MIPI-CSI Controller 2-lane	DA_IP_3P_MXL_DPHY_CSI2RX2L_GF22FDX	1.2 or newer	New	-
D-PHY Rx				
MIPI-DSI Controller 2-lane	DA_IP_3P_MXL_DPHY_PLL_DSIT_X_GF22FDX	1.2 or newer	New	-
D-PHY Tx				
ISI – single camera	D_IP_ISI_SYN	1.68 or newer	Re-use	Sourcing product: i.MX95 Change Requests: TKT0625797, TKT0615775, TKT0615774
Video Mux Controller	d_ip_video_mux_syn	-	New	Update the IP used in i.MX RT1170 Bug fixes needed: TKT0551654

IP block	PDM name	PDM version	Maturity	Comments
				Need IP change to bridge from parallel CSI and MIPI-CSI to DCIF and ISI Pixel Link TKT0649084
GPU-2.5D	D_IP_TIN_GPU_SYN	1.5 or newer	New	New Technology Initiative project
DCIF	D_IP_DCIF_SYN	1.12 or newer	New	New development ongoing based on i.MX 943 IP. Frame Buffer Decompression block to be added
JPEG Decoder IP	D_IP_3P_JPEG_DECODER	1.4 or newer	Re-use	-
JPEG Decoder Wrapper	D_IP_JPEG_DEC_WRAP_SYN	1.3 or newer	Re-use	-
Timer Peripherals				
FlexPWM	D_IP_eFlexPWM_SYN	1.64 or newer	Re-use	Sourcing product: RT1180
Quadrature Decoder	d_ip_quad_dec_syn	1.12 or newer	Re-use	Sourcing product: RT1180
TPM	D_IP_LPTPM_SYN	1.22.1.2 or newer	Update	Sourcing product: RT1180 TKT0642229
Quad TPM wrapper	D_IP_QUADTPM_SYN	1.2 or newer	New	New wrapper around TPM, replaces QuadTimer
LPIT	D_IP_LPIT_SYN	1.20 or newer	Re-use	Sourcing product: RT1180
Low Power Timer	D_IP_LPTIMER_SYN	1.15 or newer	Re-use	Sourcing product: RT1180
Robust RTC	D_IP_Robust_RTC_v2_SYN	1.56 or newer	Re-use	Sourcing product: Nirvana
VBAT Regfile	D_IP_REGFILE_SYN	009 or newer	Re-use	Sourcing product: Nirvana
TDET – Tamper Pin Detect	D_IP_DRYICE_SYN	1.15 or newer	Re-use	Sourcing product: Nirvana
Software Watchdog	D_IP_SWT_SYN	1.10 or newer	Re-use	Sourcing product: S32K5
EWM	D_IP_EWM_SYN	1.19 or newer	Re-use	Sourcing product: RT1180
Frequency Measurement	D_IP_FMEASURE_SYN	1.16 or newer	Re-use	Sourcing product: RT700
Power Management				
Reset Control			New	
Power Control			New	
Sleep Control			New	
Module Control			New	
VBAT Control			New	
PMC_SS			New	
Body Bias IP			New	
OSC32K Digital			New	
FRO32K Digital			New	
PVT Monitor			New	
Process Monitors – SIST			New	
Ring Oscillator			New	
Process Monitors – PMRO			New	
Ring Oscillator			New	
Clock Control				

IP block	PDM name	PDM version	Maturity	Comments
CGU_SS			New	
CGU_ANA			New	
CGU_DIG			New	
FRO_TUNER			New	
Test				
Testport	D_IP_TESTPORT_SYN	1.9 or newer	Re-use	Sourcing product: RT1020
ATX			New	
MTR			New	
JTAGC	D_IP_JTAGC_SYN	1.41 or newer	Re-use	Sourcing product: RT1180
Libraries and Compilers				
I/O Pads	Synopsys IO or NXP IO?		New	
PDK	GF_22FDXP_PDK_1.2		Re-use	
DDK Mixed VT 1.8V EGO (10T)			Re-use	
Synopsys UHVT Library 8T			Re-use	
ULL Library			Re-use	
Synopsys LVT Library 104CPP 6.75T			Re-use	
Synopsys VLVT Library 104CPP 6.75T			Re-use	
Two Port High Density Register File	gf_22fdx_snps_ad2preg_1.2		Re-use	
Single Port SRAM compiler	nxp_elmspram		New	New development by CTO memory team, with first time adoption in RT2660
Single Port High Density Register File	gf_22fdx_snps_adspreg_1.2		Re-use	
Single Port High Density Via 12 ROM	gf_22fdx_snps_adv1rom_1.2		Re-use	
Single Port High Speed Register File	gf_22fdx_snps_afspreg_1.2		Re-use	
Two Port Ultra High Density Register File	gf_22fdx_snps_au2preg_1.2		Re-use	
Single Port Ultra High Density Register File	gf_22fdx_snps_ulsreg_1.2		Re-use	

16. Abbreviations

ACMP	Analog Comparator
ADC	Analog Digital Convertor
ASRC	Asynchronous Sample Rate Convertor
BGA	Ball Grid Array
CAN-FD	Controller Area Network with Flexible Datarate
CDM	Charged Device Model
CNN	Convolutional Neural Network
CPU	Central Processing Unit
CSI	Camera Serial Interface
CTI	Cross Triggering Interface
DAC	Digital Analog Convertor
DCDC	Direct Current Direct Current
DMA	Direct Memory Access
DSI	Display Serial Interface
ECC	Error Correction Code
eMMC	embedded MultiMedia Card
FBB	Forward Body Bias
FPU	Floating Point Unit
FuSa	Functional Safety
GPIO	General Purpose Input Output
GPU	Graphics Processing Unit
HBM	Human Body Model
HVD	High Voltage Detector
HMI	Human Machine Interface
I2C	Inter Integrated Circuit
I2S	Inter IC Sound
IOT	Internet of Things
KB	1024 Byte
kB	1000 Byte
Kb	1024 Bit
LDO	Low Dropout
LPIT	Low Power Periodic Interrupt Timer
LVD	Low Voltage Detector
MM	Machine Model
MCU	Microcontroller Unit
MIPI	Mobile Industry Processor Interface
ML	Machine Learning
MPU	Memory Protection Unit
MRAM	Magnetic Random Access Memory
MQS	Medium Quality Sound
MVE	M-Profile Vector Extension
NAND	Not AND
NIC	Network Interconnect
NOR	Not OR
NPU	Neural Processing Unit
NVIC	Nested Vectored Interrupt Controller
PACBTI	Pointer Authentication and Branch Target Identification
PMIC	Power Management IC
PMU	Power Management Unit
POR	Power-On Reset
QDEC	Quadrature Decoder
QTPM	Quad Timer/Pulse Width Modulator Module
RBB	Reverse Body Bias
RNN	Recurrent Neural Network
ROM	Read Only Memory

RTC	Real-Time Clock
SAI	Synchronous Audio Interface
SD	Secure Digital
SDIO	Secure Digital Input Output
SDRAM	Synchronous Dynamic Random Access Memory
SPDIF	Sony Philips Digital Interface Format
SoG	Sea of Gate
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
TCM	Tightly Coupled Memory
TPIU	Trace Port Interface Unit
TRDC	Trusted Resource Domain Controller
USB	Universal Serial Bus
USDHC	Ultra Secure Digital Host Controller
XEA	Crossover Evolved Architecture
XSPI	Expanded Serial Peripheral Interface
ZBB	Zero Body Bias

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