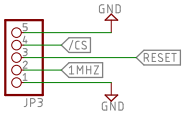
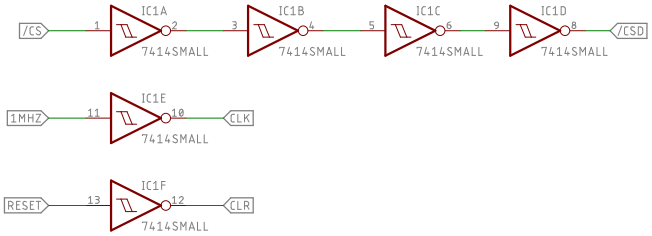
the INPUT section:
/CS (from Pin12 / U3) gets through four INVERTERS and becomes /CSD (chip select delayed)
RESET gets through one INVERTER and becomes CLR (clearing the D-FF)
1MHz gets through one INVERTER and becomes CLK (clocking the D-FF)

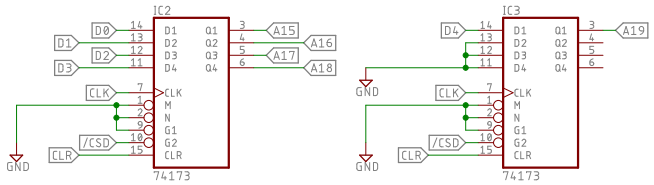
the /CS signal from
Pin12 of U3
gets triggert from HIGH to Low
by POKE 55040

the 1MHz system clock
syncronizes the /CS signal

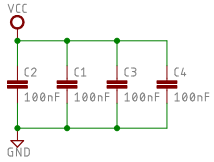




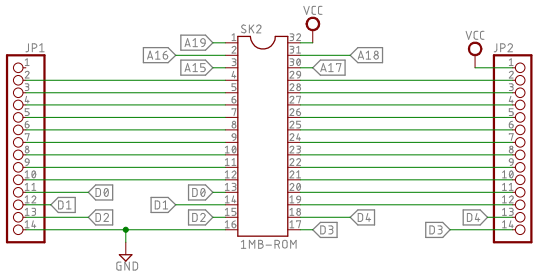
the ADDRESS switching section:
if the CLK inputs changes from LOW to HIGH. the value of D0-D4 is wrtitten to A15-A19.
this addresses the bigger ROMs.



the POWER section:
the power indicater LED and the decoupling capacitors.



the ROM adapter section:
adapts the 28pin ROM socket to the 32pin ROM socket



CREDITS:
Special thanks to @kinzi (from Forum64) who pushed me forward and helped me with troubleshooting and fixing the problem.
Thanks to all who were are involved in this project.

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