APPLICATION		REVISION			
NEXT ASSY.	USED ON	LTR	DESCRIPTION	DATE	APPROVED
	A300/A500 Plus	**A**	**SPECIFICATION RELEASE**		

1.0 DESCRIPTION

This specification describes the GAYLE gate array IC used in the Amiga A600 and related systems. GAYLE shall be capable of operating a 68000 based Amiga with ECS chipset at a processor clock speed of 7.16 MHz. GAYLE shall provide the following functions:

- Address decoding and timing for:
  system ROM, optional flash ROM, chip RAM, chip registers, 8520 CIA's, real time clock (RTC), Credit card connector, IDE hard disk drive, and COM200020 ArcNet chip

-Generation of ECLK clock signal
-Data buffer control
-System RESET logic
-Floppy Glue

1.1 CONFIGURATION

This device shall be configured as a standard 84-pin plastic leaded chip carrier (PLCC) with pin configuration as in Figure 1 and dimensions as in Figure 2.

1.2 SOURCES

Refer to Approved Vendors List.

1.3 APPLICABLE DOCUMENTS

Commodore Engineering Policy 1.02.007 Integrated Circuit Qualification Procedure
Commodore Engineering Policy 1.02.008 Integrated Circuit Process Test Specification

COMMODORE P. N.	STATUS				
391155-01	ACTIVE				
391155-02	ACTIVE				

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES: ANGLES +/- 1 DEGREE 2 PLACE DECIMALS +/- 0.02 3 PLACE DECIMALS +/- 0.010	DRAWN Mike Rivers	DATE	**Commodore** 1200 WILSON DRIVE WEST CHESTER, PA. 19380 (215) 431-9100
	SYSTEM ENG.	DATE	
	TEST ENG	DATE	
COPYRIGHT 1991 COMMODORE ELECTRONICS LTD INFORMATION CONTAINED HEREIN IS THE UNPUBLISHED AND CONFIDENTIAL PROPERTY OF COMMODORE ELECTRONICS LIMITED. USE, REPRODUCTION OR DISCLOSURE OF THIS INFORMATION WITHOUT THE PRIOR WRITTEN PERMISSION OF COMMODORE IS STRICTLY PROHIBITED. ALL RIGHTS RESERVED.	COMP. ENG Drew Shannon	DATE	TITLE: **IC, SM, GATE ARRAY, 4145R0F020, GAYLE**
	CIRCUIT ENG.	DATE	
			SIZE A / DRAWING NUMBER **391155**
			SCALE / SHEET 1 OF 6

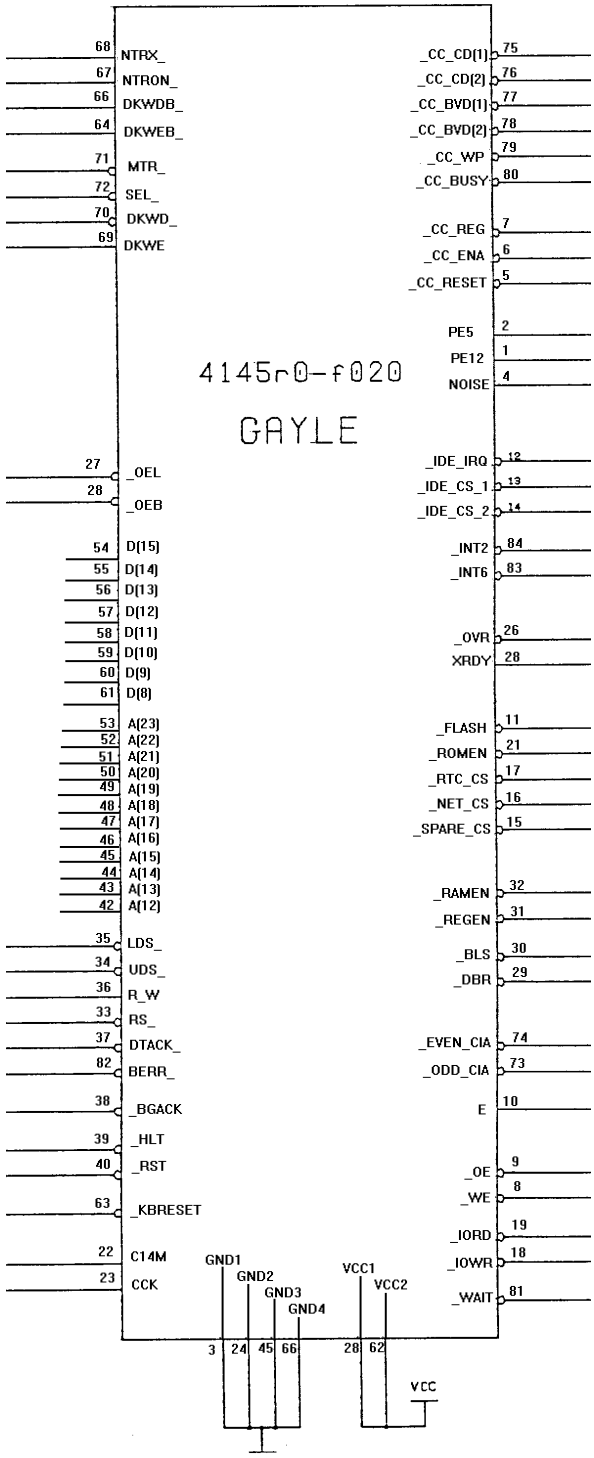
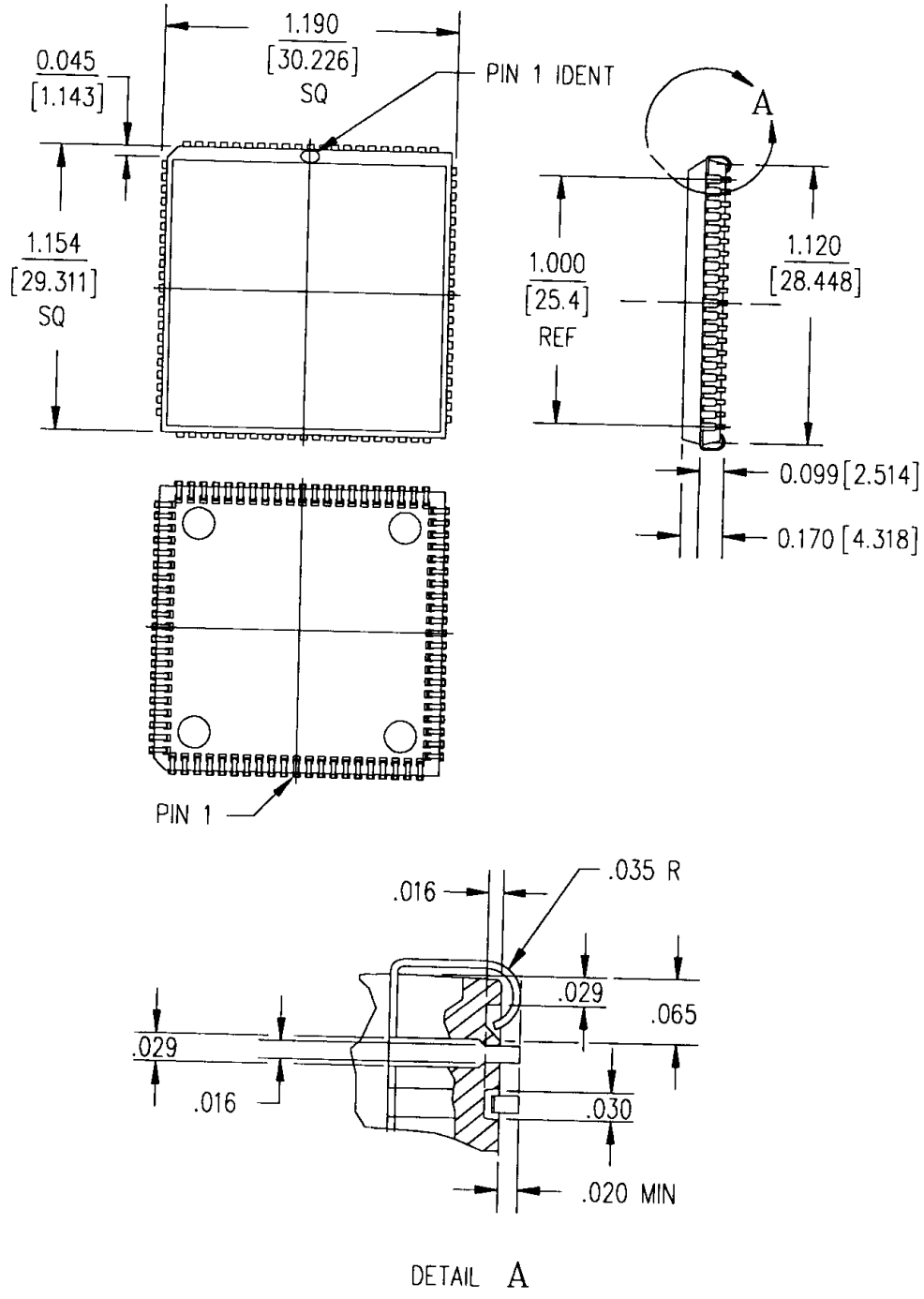


FIGURE 1 - PINOUTS

Commodore	TITLE **IC, SM, GATE ARRAY, 4145R0F020, GAYLE**	
SIZE DRAWING NUMBER **391155**	REV. SCALE A	SHEET 2 OF 6



NOTES:
1. Dimensions in brackets are millimeters
2. Tolerances are .XXX ± 0.005 [0.127mm]

FIGURE 2 - PACKAGE DIMENSIONS

Commodore		TITLE	**IC, SM, GATE ARRAY, 4145R0F020, GAYLE**	
SIZE	DRAWING NUMBER	REV.	SCALE	SHEET 3 OF 6
	391155	A		

2.0 PIN DESCRIPTIONS

NUM	CLASS	NAME	DESCRIPTION
1	OUT	PE12	Program Voltage 12V Enable
2	OUT	PE5	Program Voltage 5V Enable
3	PWR	Gnd1	Ground
4	TS	NOISE	Digital Audio
5	OUT	CC_RESET	Memory Card Reset
6	OUT	_CC_ENA	Memory Card Enable
7	OUT	_CC_REG	Memory Card "Register" Space
8	OUT	_CC_CEL	Memory Card Chip Enable Low byte
9	OUT	_CC_CEU	Memory Card Chip Enable High byte
10	OUT	E	CIA Phi 2
11	OUT	_FLASH	Flash Memory Chip Enable
12	IN	_IDE_IRQ	IDE Drive Interrupt Request
13	OUT	_IDE_CS(1)	IDE Drive Chip Select 1
14	OUT	_IDE_CS(2)	IDE Drive Chip Select 2
15	OUT	_SPARE_CS	Spare Chip Select
16	OUT	_NET_CS	Network Controller Chip Select
17	OUT	_RTC_CS	Real Time Clock Chip Select
18	OUT	_IOWR	I/O Write Strobe
19	OUT	_IORD	I/O Read Strobe
20	PWR	Vcc1	+5V
21	OUT	_ROMEN	ROM Chip Enable
22	IN	C14M	14 MHz Clock In (master)
23	IN	CCK	CCK Clock IN (sync)
24	PWR	Gnd2	Ground
25	IN	XRDY	Expansion Bus Wait
26	IN	_OVR	Expansion Bus Decode Override
27	OC	_OEL	Chip->68000 Bus Buffer Enable
28	OC	_OEB	68000->Chip Bus Buffer Enable
29	IN	_DBR	Agnus Chip Data Bus Required
30	OUT	_BLS	Agnus Chip Blitter Slowdown
31	OUT	_REGEN	Agnus Chip Register Enable
32	OUT	_RAMEN	Agnus Chip RAM Enable
33	IN	_AS	68000 Address Strobe
34	IN	_UDS	68000 Upper Data Strobe
35	IN	_LDS	68000 Lower Data Strobe
36	IN	R_W	68000 Read/Write
37	TS	_DTACK	68000 Data Transfer Acknowledge
38	IN	_BGACK	68000 Bus Grand Acknowledge
39	OC	_HLT	68000 Halt
40	OC	_RST	68000 Reset
41	IN	A12	68000 Address Bit 12
42	IN	A13	68000 Address Bit 13
43	IN	A14	68000 Address Bit 14
44	IN	A15	68000 Address Bit 15
45	PWR	Gnd3	Ground
46	IN	A16	68000 Address Bit 16
47	IN	A17	68000 Address Bit 17
48	IN	A18	68000 Address Bit 18
49	IN	A19	68000 Address Bit 19
50	IN	A20	68000 Address Bit 20

51	IN	A21	68000 Address Bit 21
52	IN	A22	68000 Address Bit 22
53	IN	A23	68000 Address Bit 23
54	IO	D7	68000 Data Bit 7
55	IO	D6	68000 Data Bit 6
56	IO	D5	68000 Data Bit 5
57	IO	D4	68000 Data Bit 4
58	IO	D3	68000 Data Bit 3
59	IO	D2	68000 Data Bit 2
60	IO	D1	68000 Data Bit 1
61	IO	D0	68000 Data Bit 0
62	PWR	Vcc2	+5V
63	IN	_KBRESET	Keyboard Reset In
64	OUT	DKWEB	Floppy Write Enable Out
65	OUT	DKWDB	Floppy Write Data Out
66	PWR	Gnd4	Ground
67	OUT	MTRON	Floppy Motor On Out
68	OUT	MTRX	Floppy Motor Out
69	IN	DKWE	Floppy Write Enable In
70	IN	_DKWD	Floppy Write Data In
71	IN	_MTR	Floppy Motor In
72	IN	_SEL	Floppy Select In
73	OUT	_ODD_CIA	CIA Odd Chip Select
74	OUT	_EVEN_CIA	CIA Even Chip Select
75	IN	_CC_CD(1)	Memory Card Card Detect 1
76	IN	_CC_CD(2)	Memory Card Card Detect 2
77	IN	_CC_BVD(1)	Memory Card Battery Voltage Detect 1
78	IN	_CC_BVD(2)	Memory Card Battery Voltage Detect 2
79	IN	CC_WP	Memory Card Write Protect
80	IN	_CC_BUSY_IREQ	Memory Card Busy/Interrupt Request
81	IN	_WAIT	Memory Card Wait
82	OC	_BERR	Bus Error Interrupt Request
83	OC	_INT6	High Priority Interrupt Request
84	OC	_INT2	Low Priority Interrupt Request

3.0 PHYSICAL REQUIREMENTS

3.1 MARKING

Parts shall be marked with Manufacturer's Part Number, Manufacturer's Identification, and EIA Date Code.

3.2 PACKAGING

The interconnected logic circuitry shall be contained in an 84-pin plastic leaded chip carrier (PLCC) plastic package with exterior dimensions per Figure 2.

4.0 ENVIRONMENTAL REQUIREMENTS

Units furnished to the requirements of this specification shall meet the following environmental resistance requirements (vendors shall furnish supporting documentation upon request):

Operating Temperature	0 to 70 deg. C
Operating Humidity	5 to 95% RH non-condensing
Operating Altitude	0 to 3000 meters
Storage Temperature	- 20 to + 85 deg. C
Storage Humidity	5 to 95% RH non-condensing
Storage Altitude	0 to 15,000 meters

4.1 PROCESS QUALIFICATION TESTS

Integrated circuits supplied to the requirements of this specification shall meet the requirements of Engineering Policy No. 1.02.008. Supporting documentation shall be supplied by vendor upon request.

4.2 ENVIRONMENTAL TEST CONDITIONS

Devices shall comply with the following environmental resistance tests per Commodore Engineering Policy 1.02.007.

1. Temperature/humidity (85 deg. C and 95% RH non-condensing) for 168 hours.
2. Operating life (1000 hours at 70 deg. C ambient temperature)
3. Solderability per MIL-STD-883, Method 2003
4. Pressure cooker (15 psig, 120 deg. C, and 100% RH for 24 hours)
5. Solvent resistance per MIL-STD-883,Method 2015, using water and trichloroethane
6. Solder temperature resistance (250 deg. C for five seconds)
7. ESD requirement MIL-STD 1686 Group 3

Note: Devices shall meet this specification's operating performance requirements after the above tests are completed.

4.3 MINIMUM ACCEPTANCE LEVEL

The minimum acceptance level of any lot shall be an AQL of 0.65 as defined by MIL-STD 105 single sampling techniques.

4.4 AGE OF DEVICES

Unit shall be rejected if EIA Date Code indicates an age of three (3) or more years.

APPROVED VENDOR LIST

This sheet must be removed from this document before the document is shown or transmitted to a vendor.

Commodore Part Number	Vendor	Vendor Part Number
391155-01	CSG	4145R0FO20
391155-02	CSG	4145R0FO20A

Commodore

TITLE

IC, SM, GATE ARRAY, 4145R0F020, GAYLE

SIZE	DRAWING NUMBER	REV.	SCALE	SHEET i OF i
	391155	A		