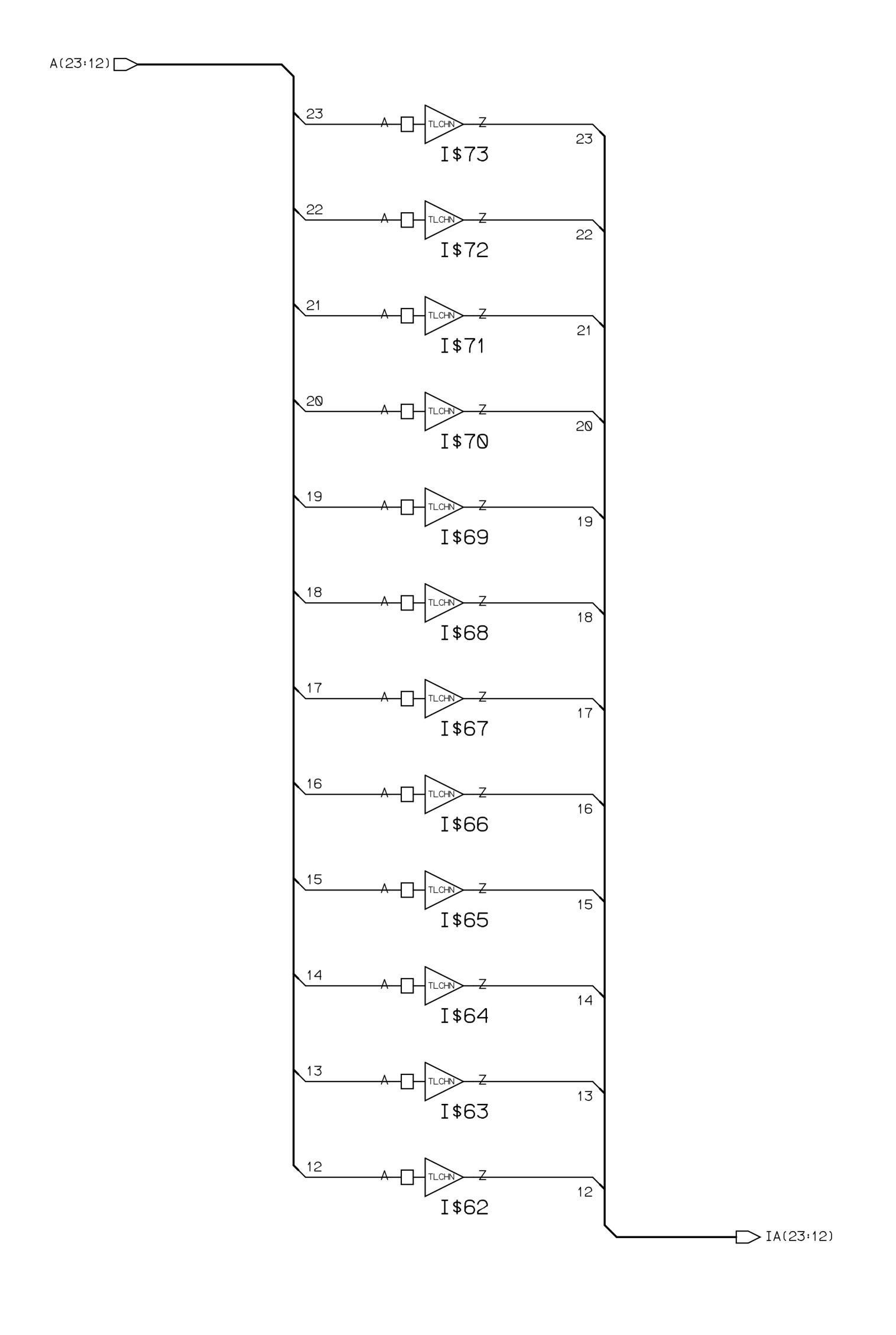


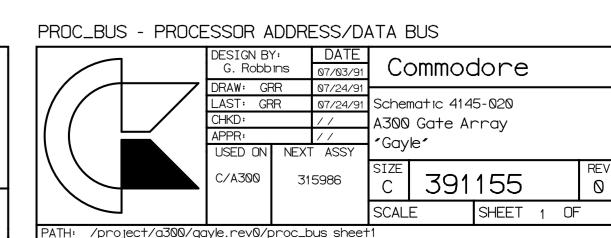
ADDRESS BUS

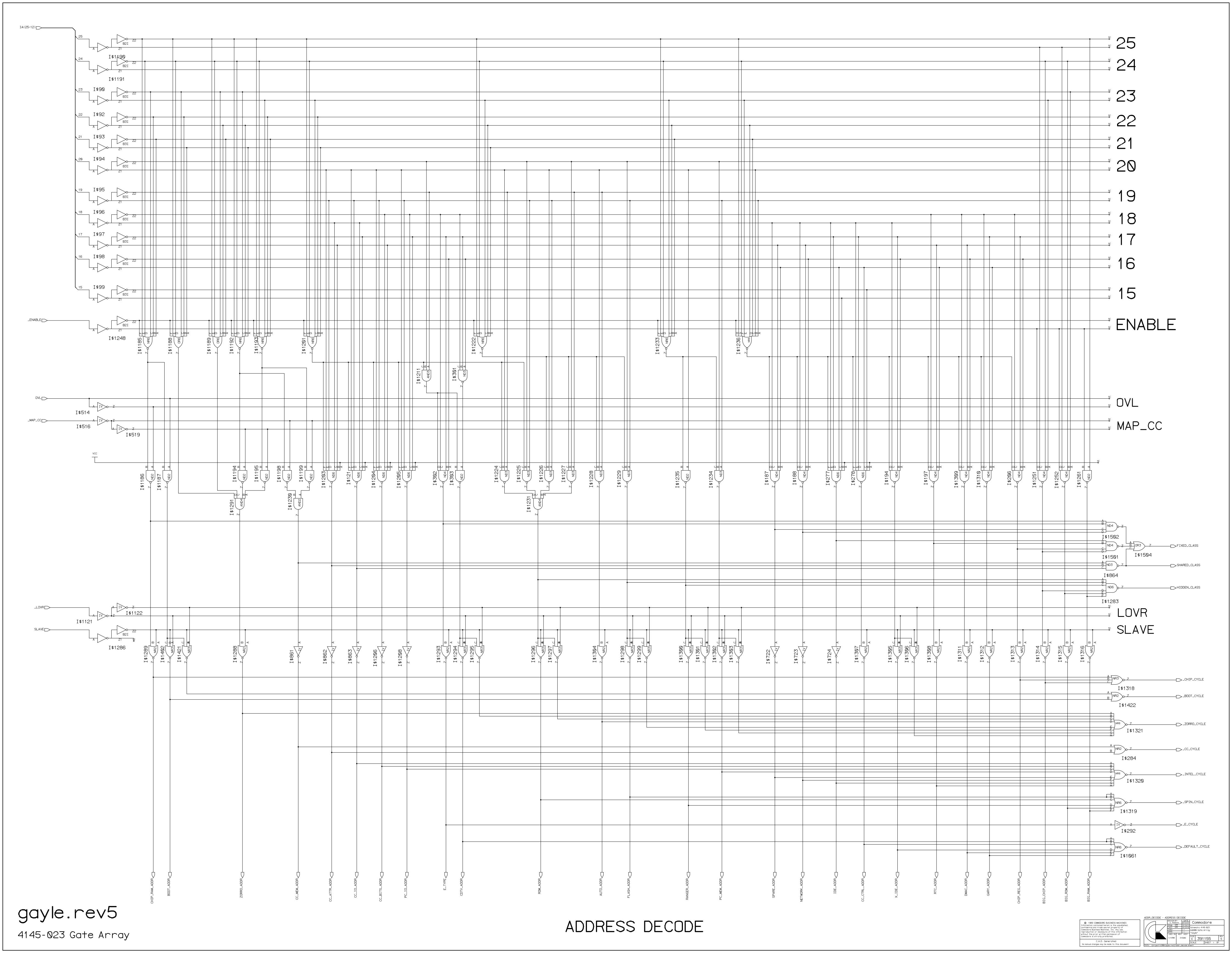


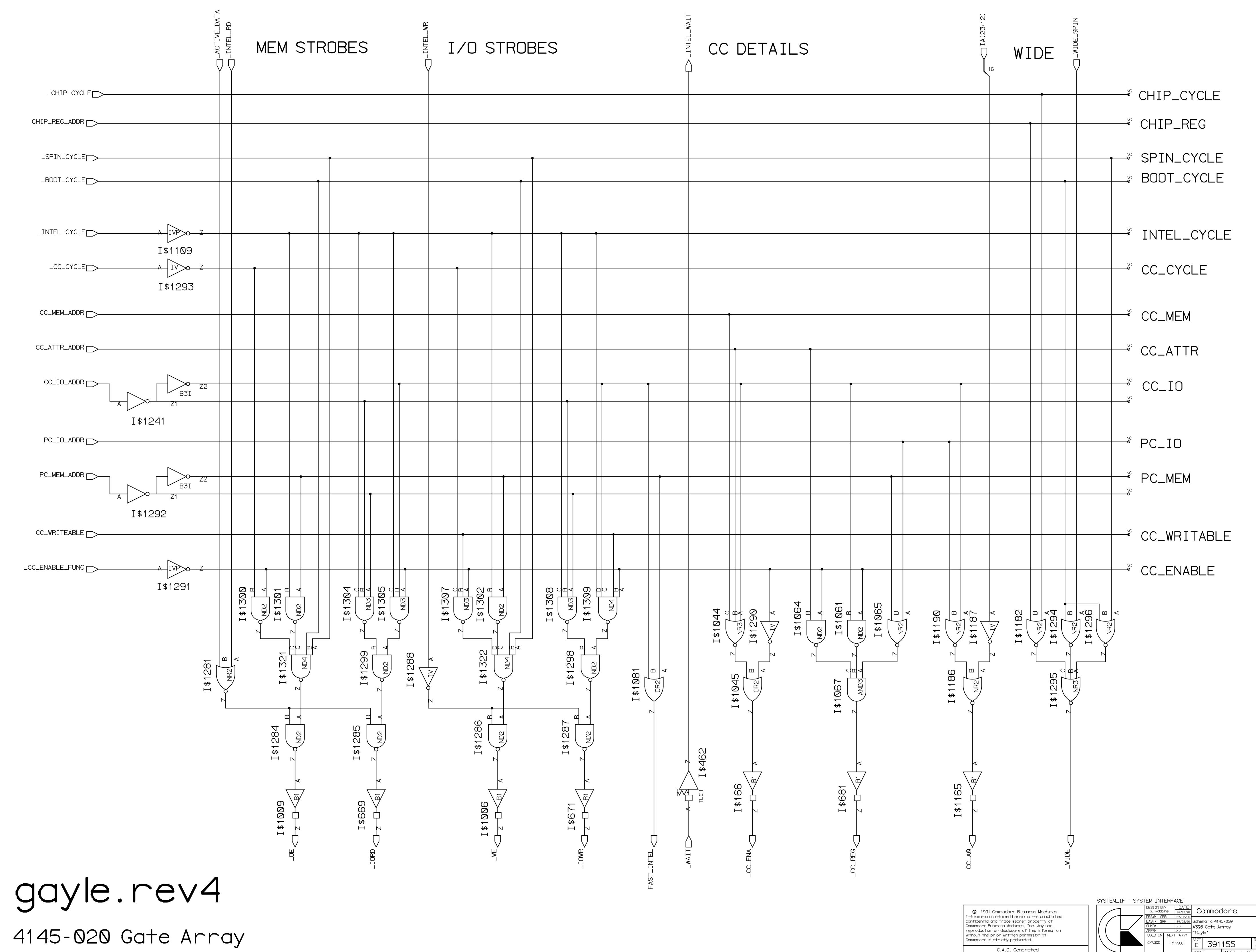
gayle.rev0

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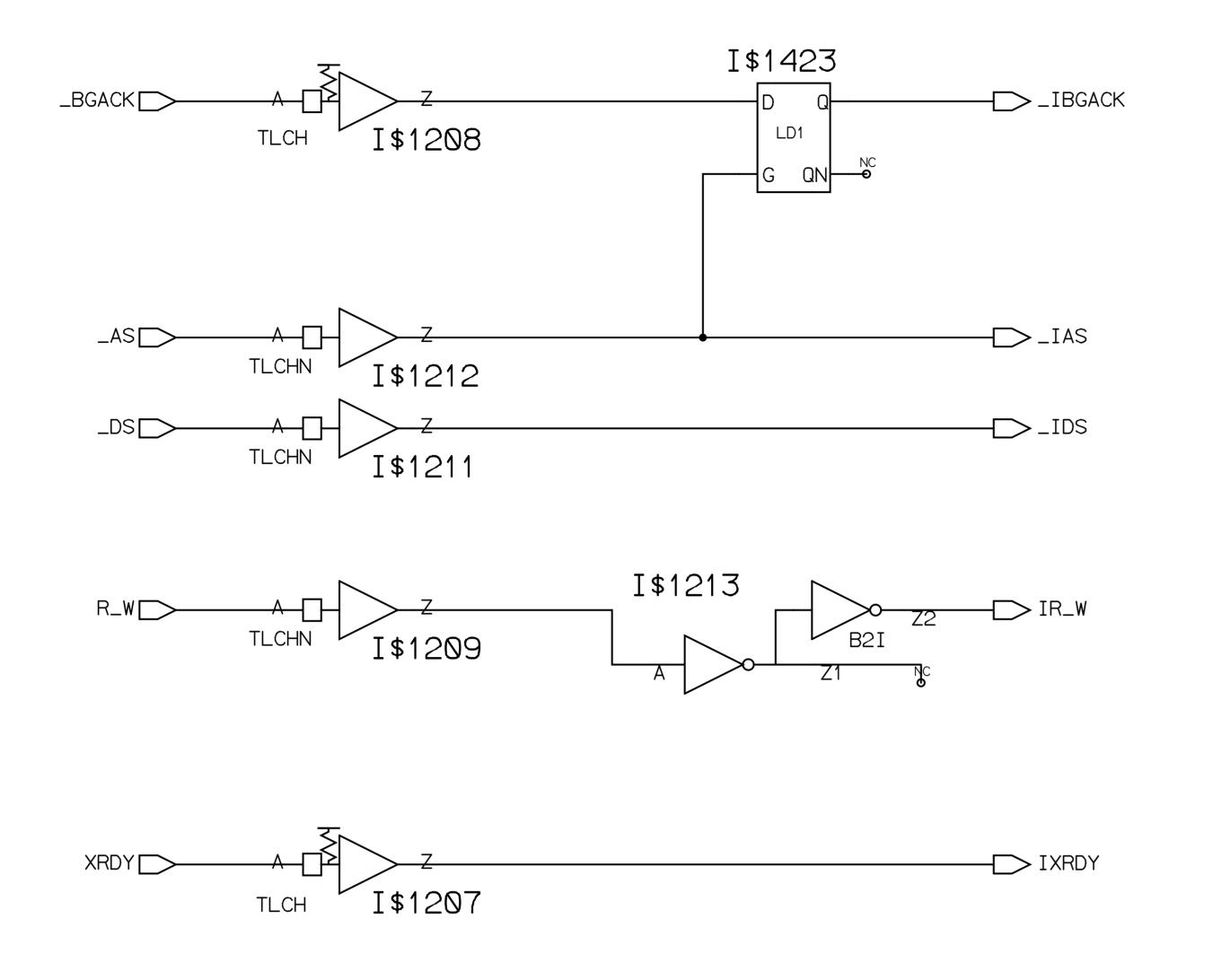


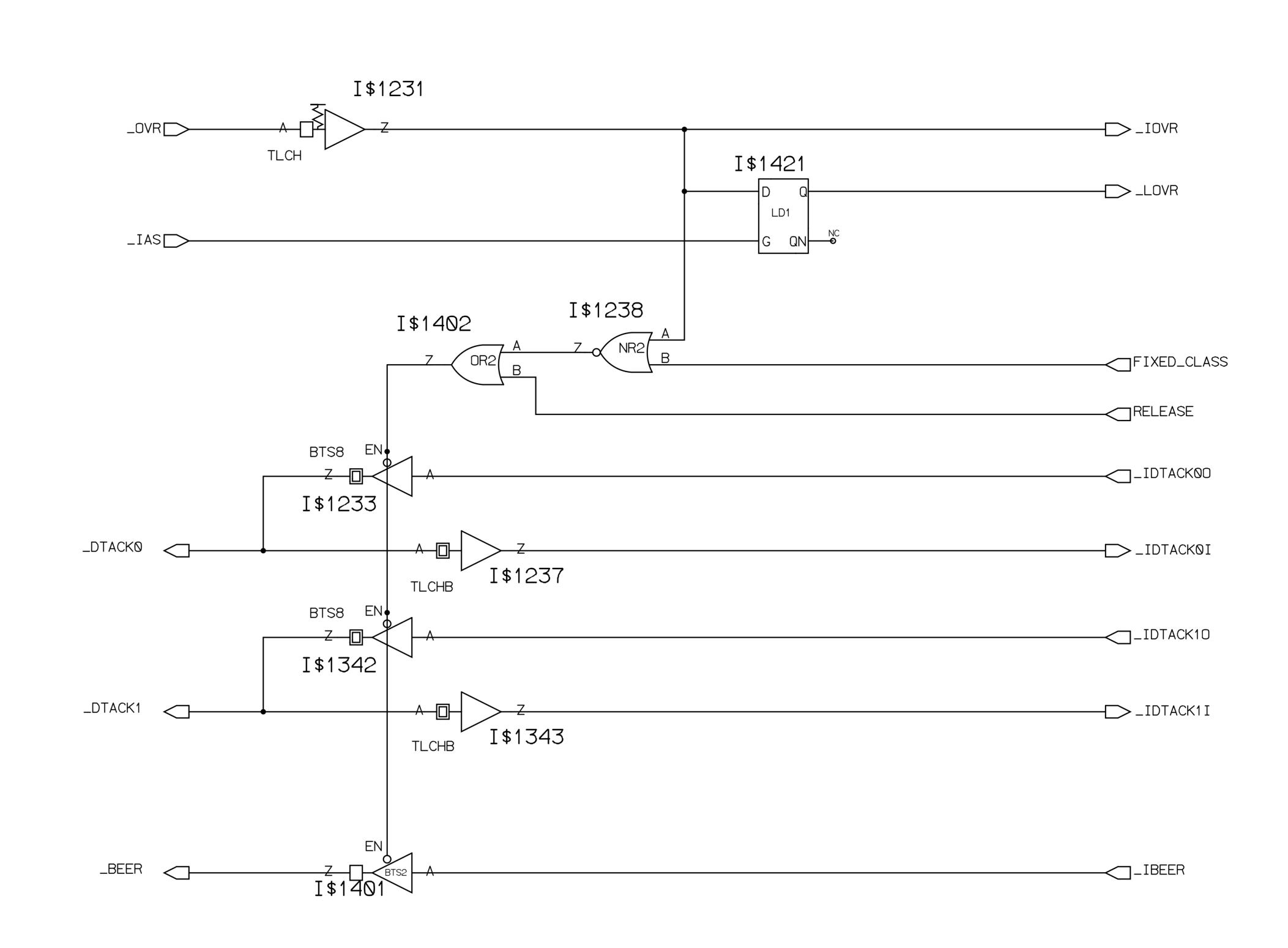


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ASSORTED SIGNALS

DTACK vs. OVERRIDE





PROC_IF - PROCESSOR INTERFACE

SIZE C 391155 SCALE SHEET 1 OF

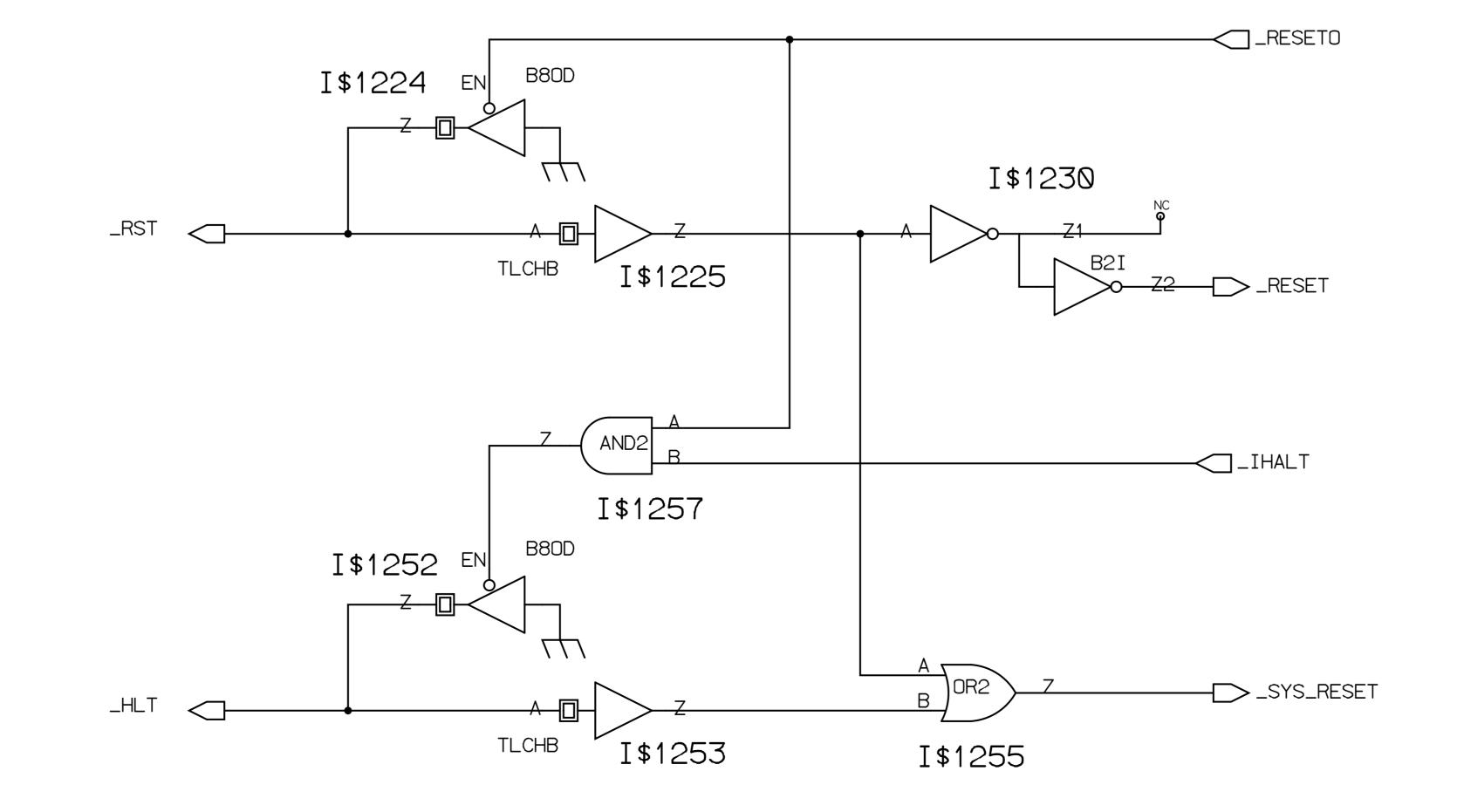
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RESET LOGIC

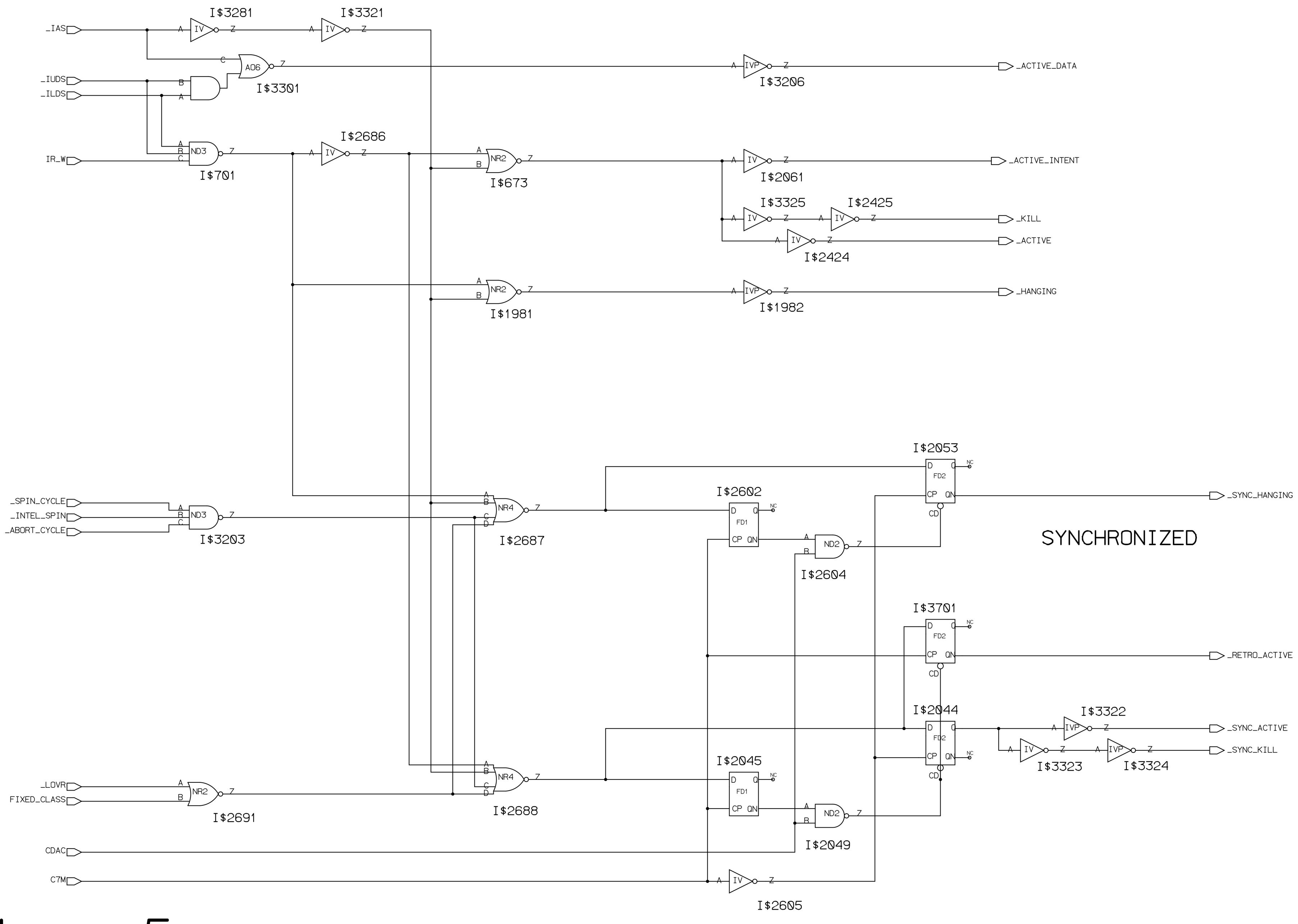


gayle.rev5

4145-023 Gate Array

CYCLE QUALIFICATION

ASYNCHRONOUS



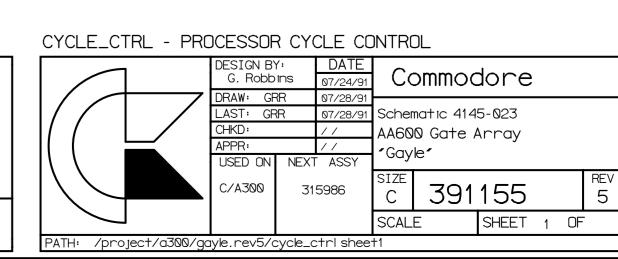
gayle.rev5

GENNIE HAZARD FREE SYNCHRONIZER, SURE!

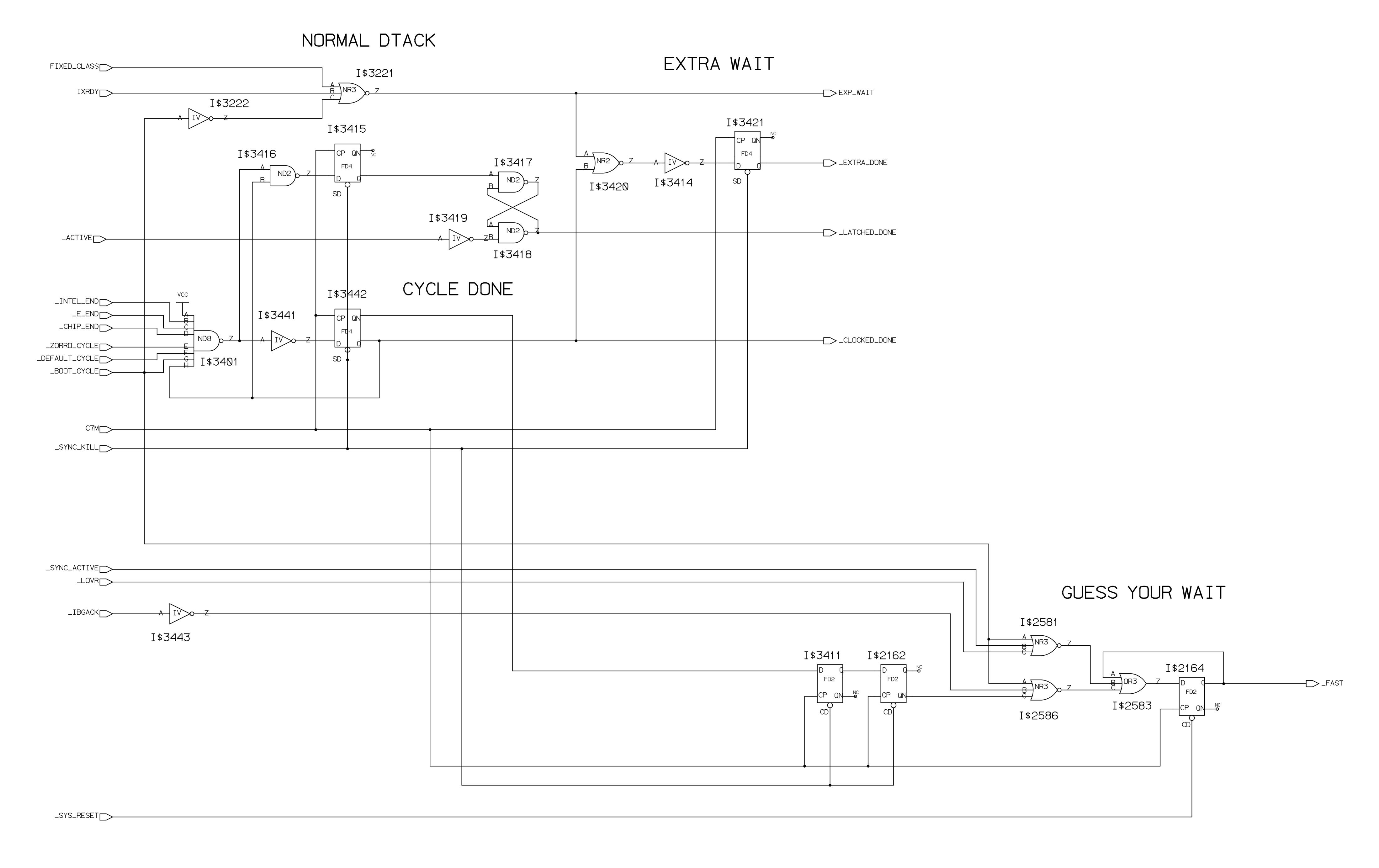
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CYCLE END AND WAIT ESTIMATION



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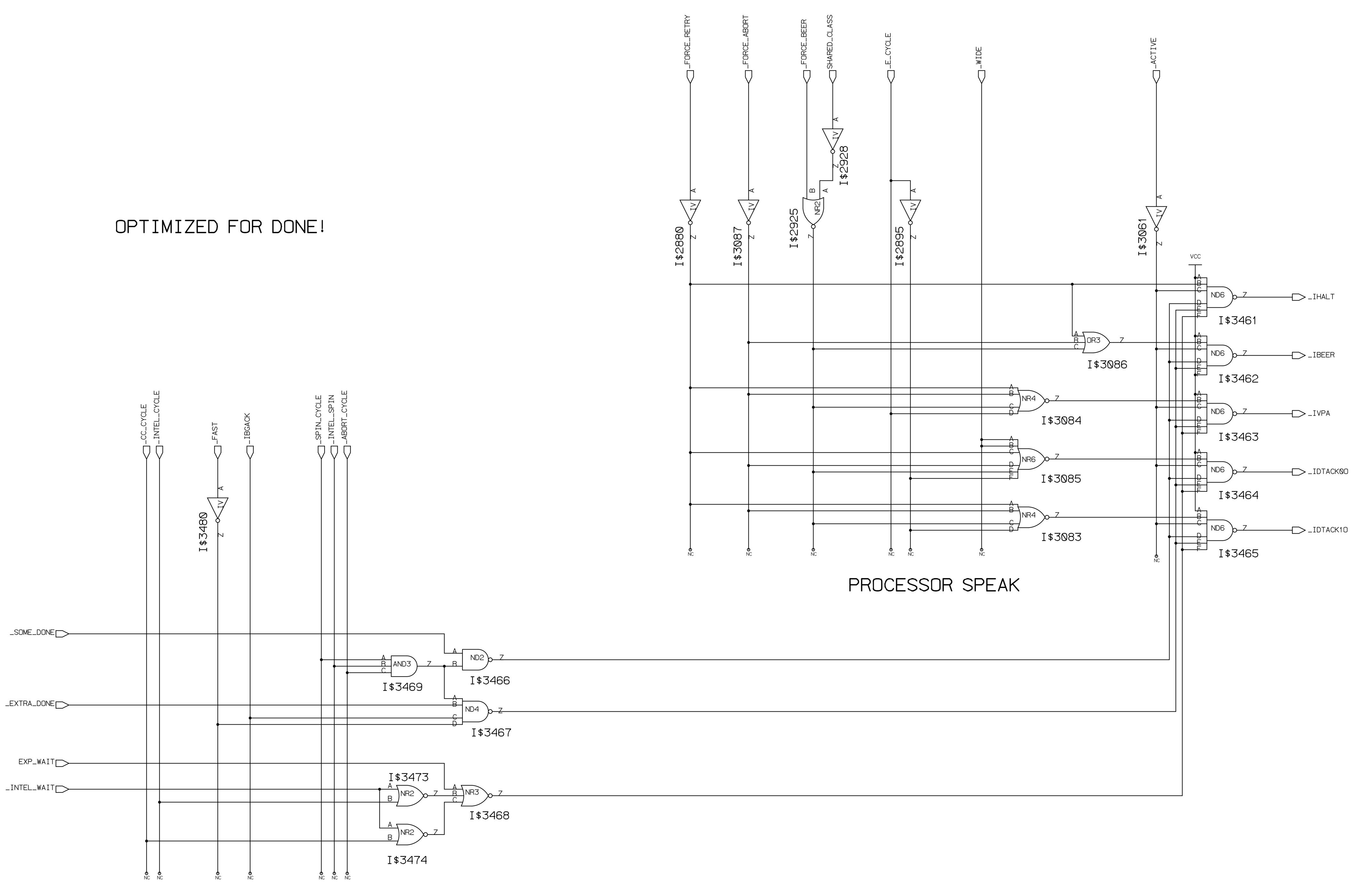
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CYCLE_CTRL - 68K CYCLE TERMINATION

SCALE SHEET 2 OF

CYCLE TERMINATION CONT'D



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WAIT CONDITIONS

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CYCLE_CTRL - 68K CYCLE TERMINATION

DESIGN BY: DATE G. Robbins 07/24/91

DRAW: GRR 07/28/91

LAST: GRR 05/28/92

CHKD: // APPR: // USED ON NEXT ASSY

C/A300 315986

COMMODOR

Schematic 4145-023

AA600 Gate Array

'Gayle'

SIZE C 391155

SCALE SHEET 3 OF

PATH: /project/a300/gayle.rev5/cycle_ctrl sheet3

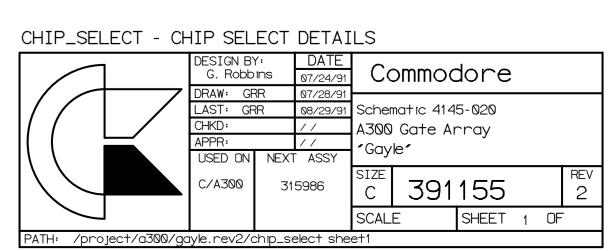
CHIP SELECT DECODE I\$122 * ACTIVE * ACTIVE_DATA ⊸ VMA ⊸^{NC} R_W

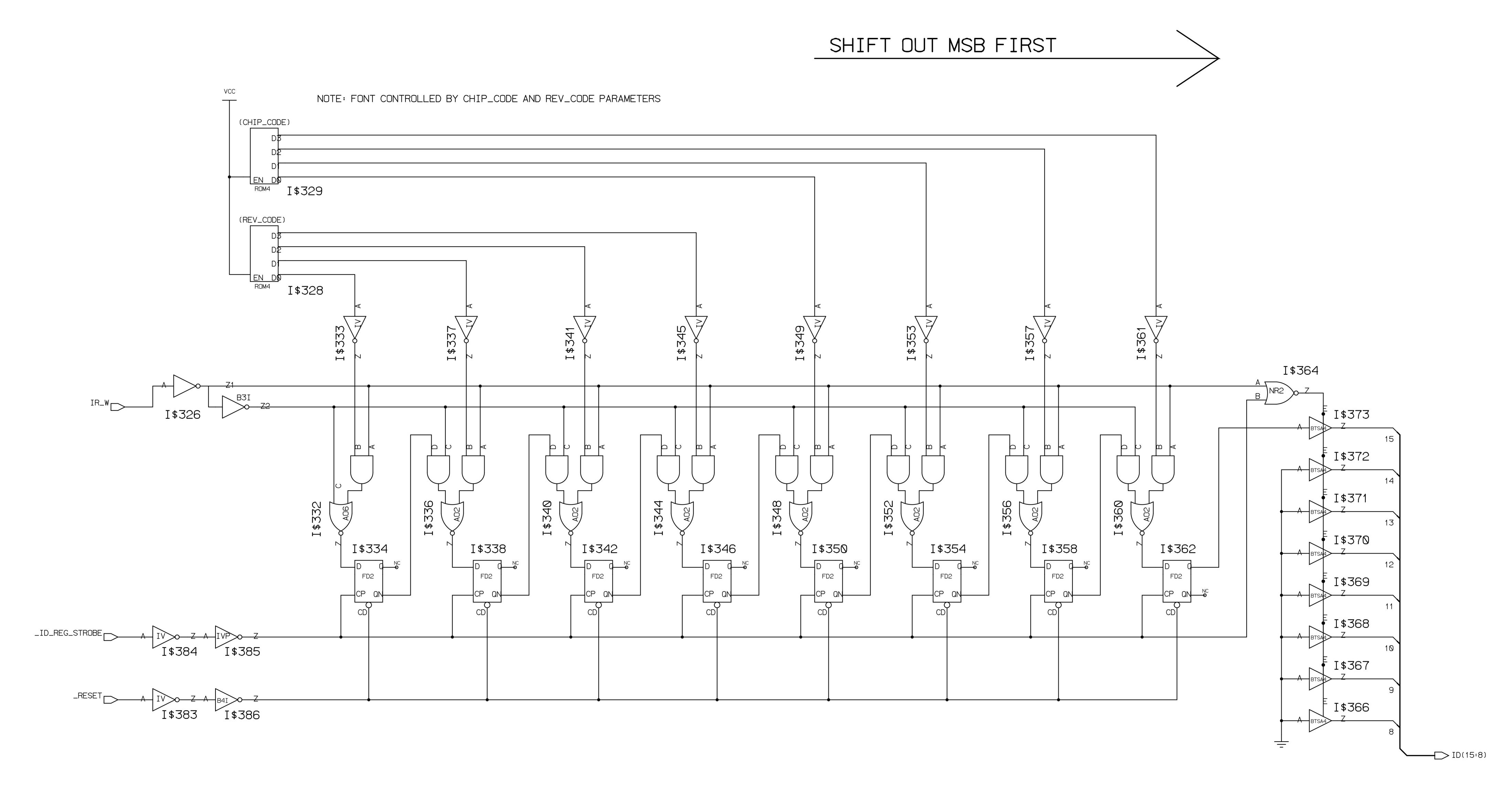
gayle.rev2 4145-020 Gate Array

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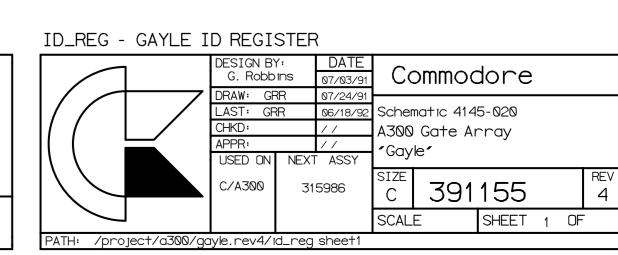
AUGI'S ID REGISTER

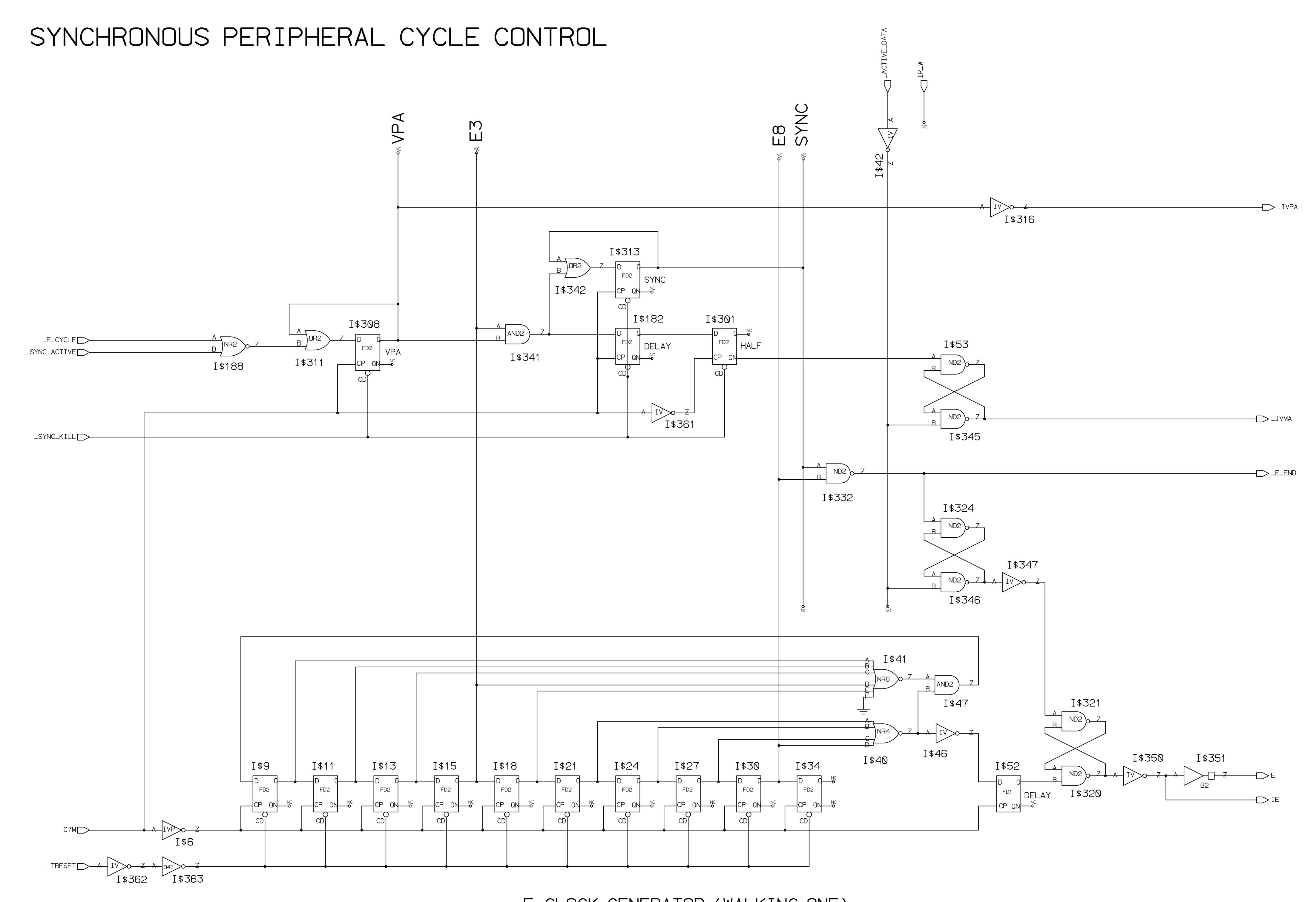
gayle.rev4

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E-CLOCK GENERATOR (WALKING ONE)

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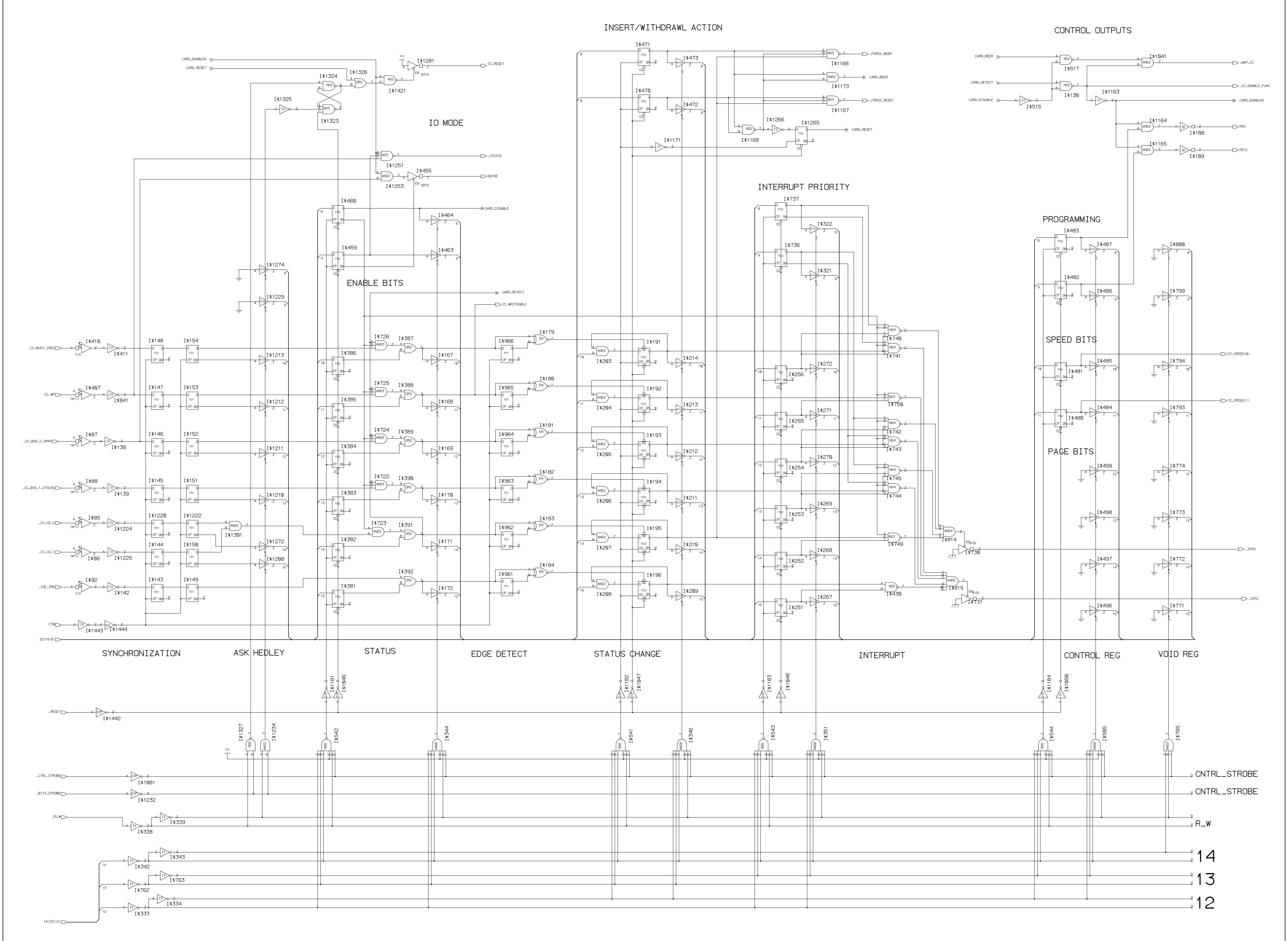
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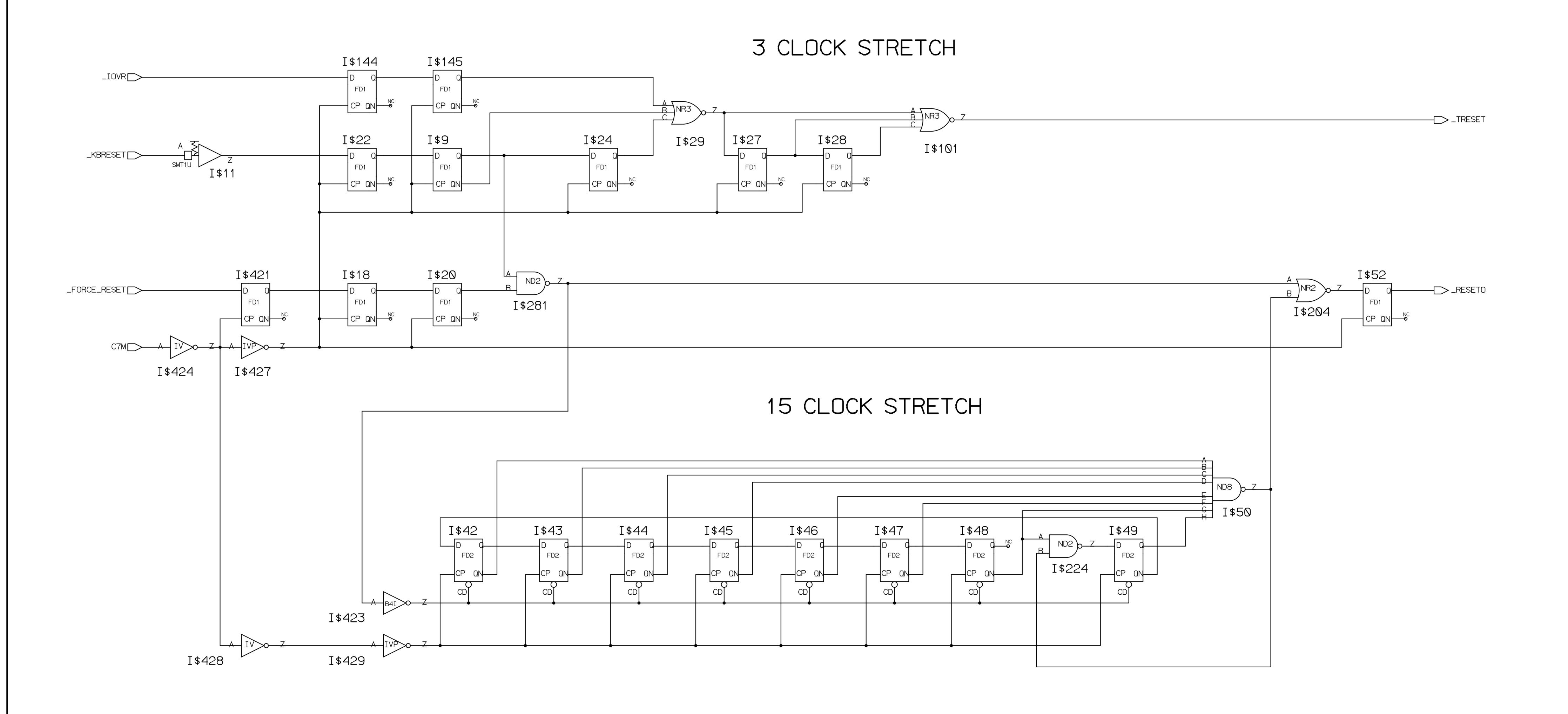
E_CLO

E_CLO

FATH:



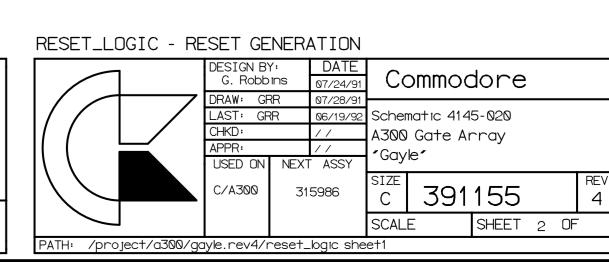
RESET LOGIC

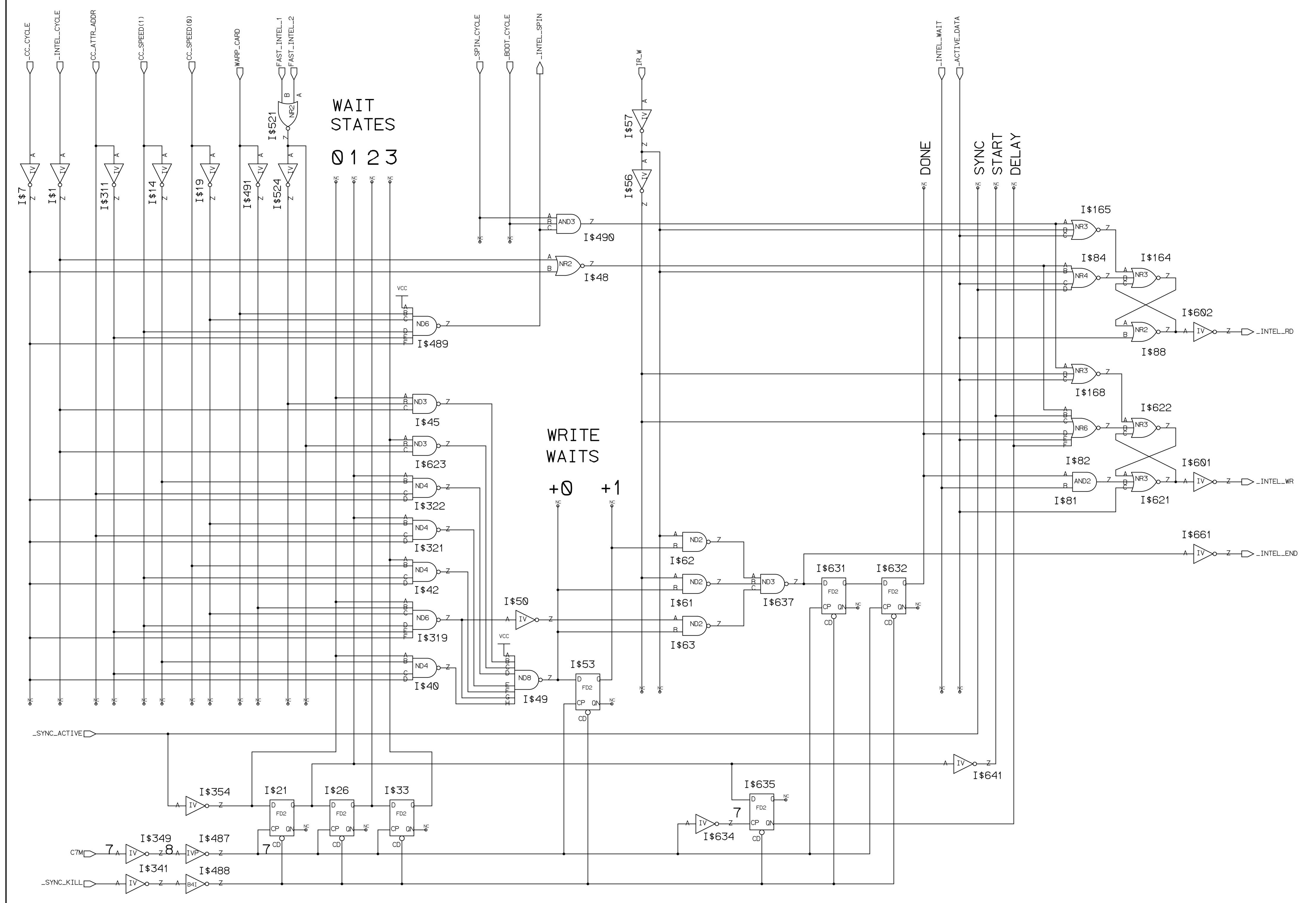


Note: _TRESET is Test Reset

gayle.rev4 4145-020 Gate Array

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INTEL CYCLE CONTROL

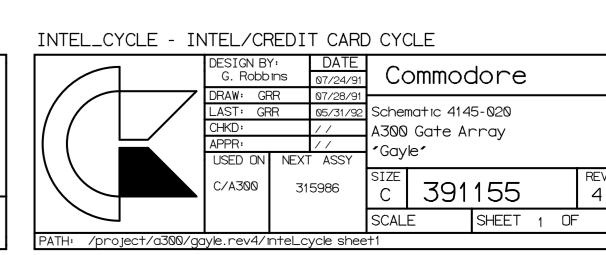
INTEL_CYCLI

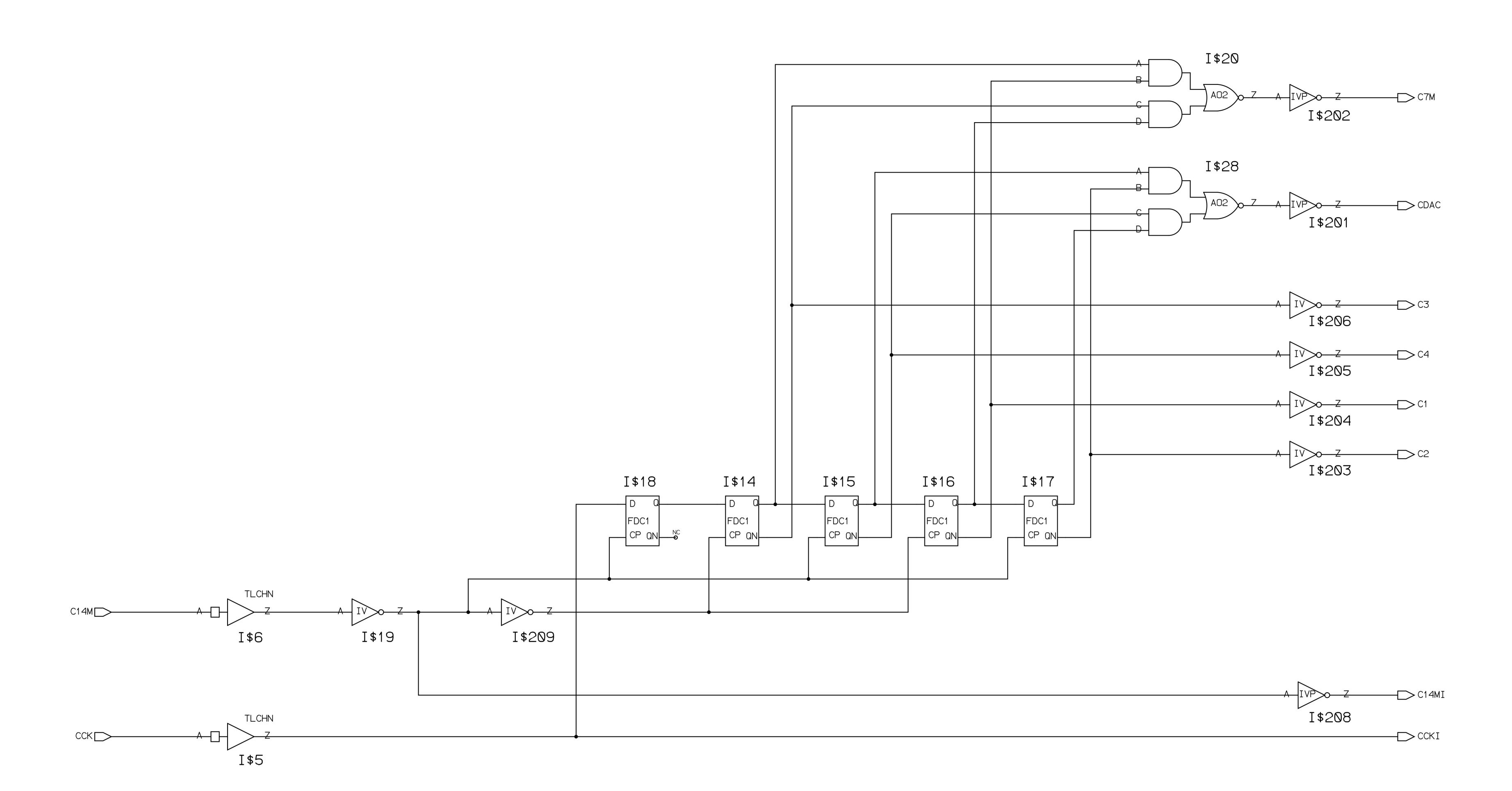
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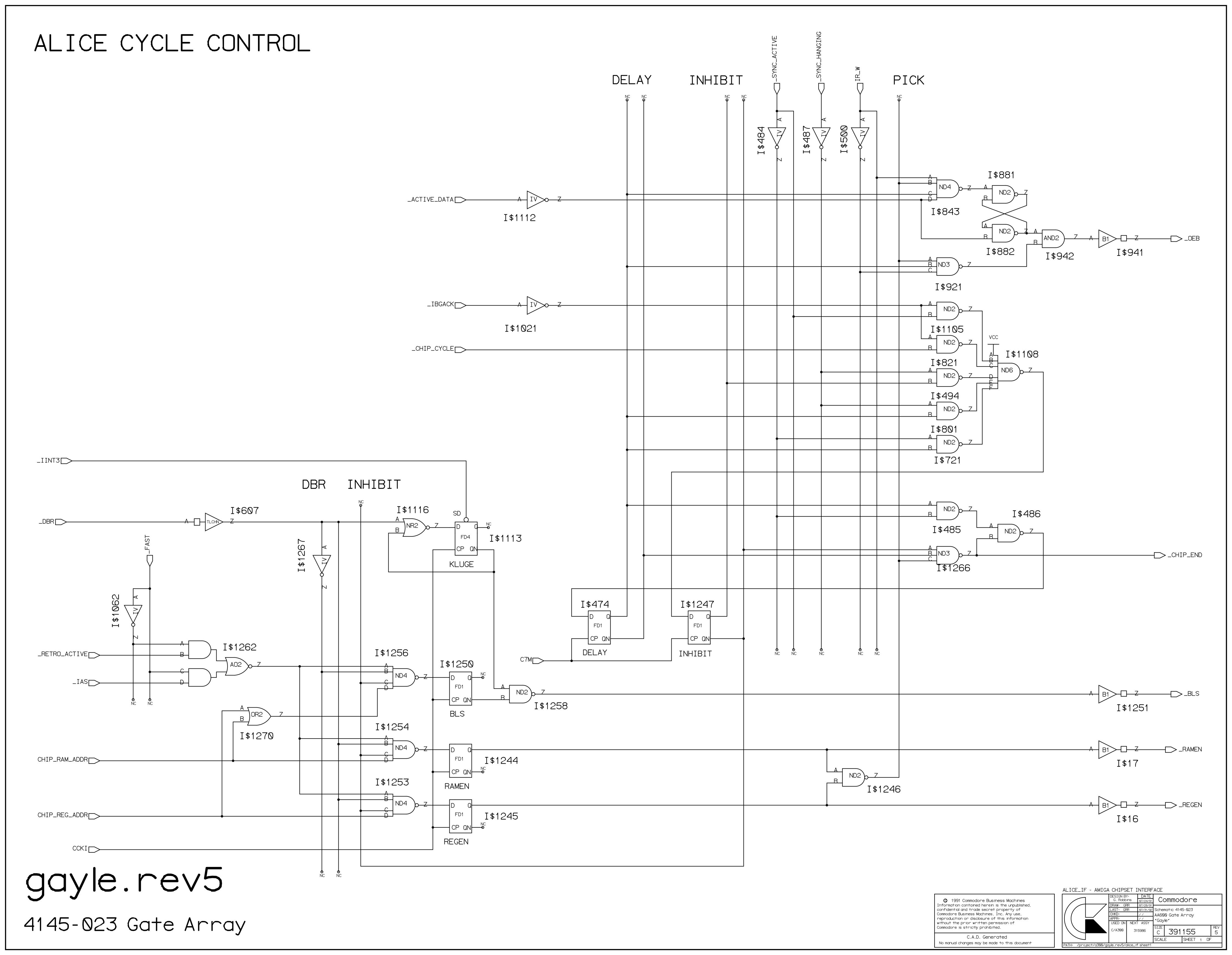
INTEL_CYCLI



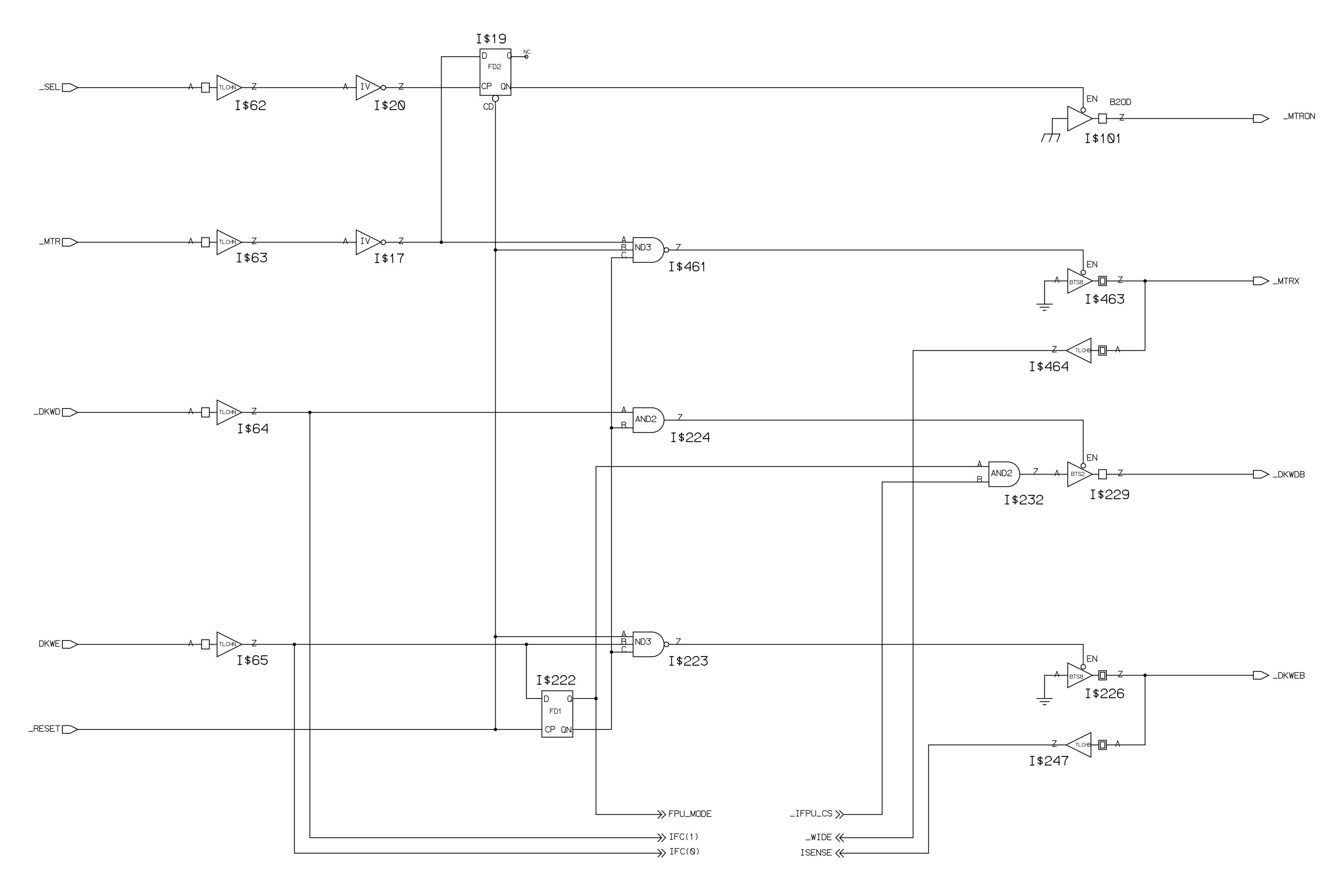


gayle.rev0 4145-020 Gate Array

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FLOPPY LOGIC AND PERVERSIONS



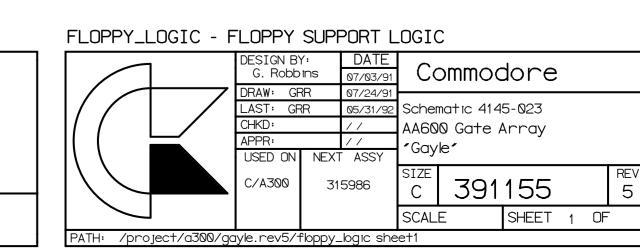
DKWE high at reset enables FPU mode Kludges here, logic on the next page

gayle.rev5

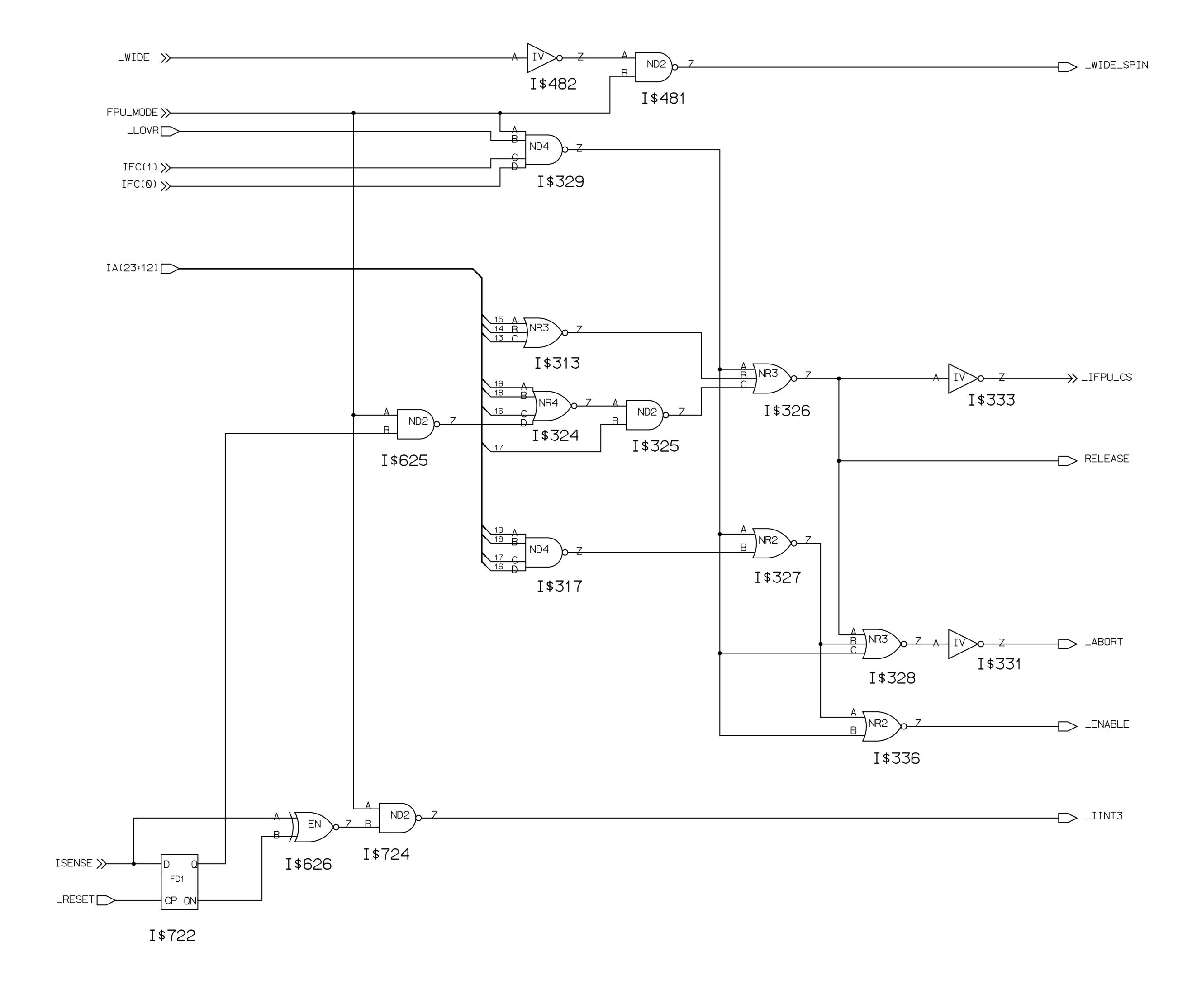
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FUNCTION CODE FOLLIES



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